Consider the FPGA system from exercise (1) connected to the memory and cpu below

Tsu = 2 ns  
Th = 1.5 ns

Memory FPGA Memory

Data

ADDR

U0

D Q

TW1 TW2

D

TPD,MAX = 5 ns  
TPD,MIN = 3 ns

D Q

Tclk1

Tclk2 Tclk3

Clock

*f = 100 MHz*

1. **Using the datasheet on the backside, calculate what values should be assigned to set\_input\_delay and set\_output\_delay if the wire delay values Tclk1 = Tclk2 = Tclk3 = TW1 = TW2 = 0 ns. Assume the memory speed grade is the -133 MHz version.**

**set\_input\_delaymin = clock-to-out delay of driving chip + board delay = 0 ns + 0 ns = 0 ns**

**set\_input\_delaymax = clock-to-out delay of driving chip + board delay = 4 ns + 0 ns = 4 ns**

**set\_output\_delaymin = -(hold time of the receiving chip) + board delay = -1 ns + 0 ns = -1 ns**

**set\_output\_delaymax = setup time of the receiving chip + board delay = 2.1 ns + 0 ns = 2.1 ns**

1. **Calculate the setup and hold slack of the U0 flip-flop in the FPGA.**
2. **Does it meet timing requirements? At what frequency will it pass?**

**No, this does not meet timing requirements.**

1. **Repeat part (a), but for Tclk1 = Tclk2 = Tclk3 = 1ns ± 0.5 ns, TW1 = 1.5 ± 1 ns, TW2 = 2 ns ± 0.5 ns**

