ASC_ODC.adl

L1:ASC

State-vector (ODC)

[L1:ASC-ODC_CHANNEL_LATCH]

(in bitmask?) Bit 1: Master WFS Gain (bit on?)

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

Bitmask: 0x1c3ffe

DoF Control Signals

		PIT		YAW	
INP1	PIT:	0.000	< 500.000		
	YAW:	0.000	< 200.000		
INP2	PIT:	0.000	< 100.000		
	YAW:	0.000	< 10.000		
PRC1	PIT:	0.000	< 500.000		
	YAW:	0.000	< 600.000		
PRC2	PIT:	0.000	< 3000.000		
	YAW:	0.000	< 3000.000		
MICH	PIT:	0.000	< 2500.000		
	YAW:	0.000	< 500.000		
SRC1	PIT:	0.000	< 4000.000		
	YAW:	0.000	< 3500.000		
SRC2	PIT:	0.000	< 100.000		
	YAW:	0.000	< 50.000		
DHARD	PIT:	0.000	< 3000.000		
	YAW:	0.000	< 3000.000		
DSOFT	PIT:	0.000	< 400.000		
	YAW:	0.000	< 400.000		
CHARD	PIT:	0.000	< 5000.000		
	YAW:	0.000	< 5000.000		
CSOFT	PIT:	0.000	< 300.000		
	YAW:	0.000	< 100.000		

		PIT		YAW	
				0x87ff87ff	
				0x2800280	BIT 18:
				0x7c007c	BIT 19:
				0x2fd02fd	BIT 20:
TRANS_X_A	PIT:	-1.906	< 0.200		BIT 14:
	YAW:	-2.339	< 0.200		
TRANS_X_B	PIT:	-156422.566	< 0.200		BIT 15:
	YAW:	-441649.164	< 0.400		
TRANS_Y_A	PIT:	-5.977	< 0.200		BIT 16:
	YAW:	-1.881	< 0.200		
TRANS_Y_B	PIT:	3145443.261	< 0.100		BIT 17:
	YAW:	-2150723.022	< 0.300		

QPD Saturations

REFL A RF9	BIT 2:	
REFL A RF45	BIT 3:	
REFL A DC	BIT 4:	
REFL B RF9	BIT 5:	
REFL B RF45	BIT 6:	
REFL B DC	BIT 7:	
AS A RF36	BIT 8:	
AS A RF45	BIT 9:	
AS A DC	BIT 10:	
AS B RF36	BIT 11:	
AS B RF45	BIT 12:	
AS B DC	BIT 13:	