LSC_ODC.adl

L1:LSC

State-vector (ODC)

[L1:LSC-ODC_CHANNEL_LATCH]

(in bitmask?) Bit 1:

Master Switch

(bit on?)

Bitmask: 0x7e

Control filters

DARM MICH PRCL SRCL CARM XARM YARM

0x8000

BIT 2: 0x2

BIT 3: 0x4

BIT 4: 0x8

DARM
Trig Current filter state 0x0
Nominal filter state 0x0
Important filter bits 0x7ffffffc

MICH
Trig Current filter state 0x6c00334
Nominal filter state 0x6cff3f4
Important filter bits 0x7ffffffc

PRCL
Trig Current filter state 0x63cc304
Nominal filter state 0x63fcfc4
Important filter bits 0x7ffffffc

SRCL
Trig Current filter state 0x6c30304
Nominal filter state 0x6c30ff4
Important filter bits 0x7ffffffc

CARM
Trig Current filter state 0x0
Nominal filter state 0x0
Important filter bits 0x7ffffffc

XARM
Trig Current filter state 0x7003c04
Nominal filter state 0x4c03f04
Important filter bits 0x7ffffffc

YARM
Trig Current filter state 0x200fcc4
Nominal filter state 0x200fcc4
Important filter bits 0x7ffffffc

Transmitted arm power:

X -9.268 >= 850.000 BIT 5:

Y -24.250 >= 1000.000 BIT 6:

PD power

POP DC

-0.134 >= 30.000

1.187 >= 0.900

-0.053 >= 20.000

BIT 7: 0x1

REFL DC

2.057 >= 20.000

1.984 >= 0.100

5.769 >= 0.100

BIT 8: 0x1

AS DC

-38.133 >= 1.000

-0.853 >= 0.300

BIT 9: 0x3

POP18

-19.762 >= 6500.000 BIT 10:

POP90

118.764 >= -2.000 BIT 11:

AS18

-46.795 >= -1.000 BIT 12:

AS90

-364.193 >= -2.000 BIT 13:

Saturations

POP 9

-2.782 -2.039 -0.434 -3.416 | lul | 32000.000 32000.000

BIT 14: 0x3

POP 45

-0.231 1.499 -0.175 -4.370 | lul | 32000.000 8000.000

BIT 15: 0x3

REFL 9

-2.592 -2.202 -1.275 -2.257 | lul | 10000.000 10000.000

BIT 16: 0x3

REFL 45

-0.868 -2.717 2.950 -4.304 | lul | 10000.000 8000.000

BIT 17: 0x3

REFL 27

5.568 311.354 | lul | 10000.000

BIT 18:

REFL 135

433.532 -185.754 | lul | 20000.000

BIT 19:

AS 45

398.661 -167.359 | lul | 32000.000

BIT 20:

OMC DC Power

1950.000 <= -0.054 <= 2150.000 BIT 21:

DARM control range

-40000.000 <= 0.000 <= 40000.000 BIT 22:

MICH control range

-250000.000 <= 0.000 <= 300000.000 BIT 23:

PRCL control range

-20000.000 <= 0.000 <= 20000.000 BIT 24:

SRCL control range

-70000.000 <= 0.000 <= 30000.000 BIT 25:

CARM control range

0.600 <= 0.000 <= 0.500 BIT 26:

ARM control range

X 0.000 <= 0.000 <= 0.000

Y 0.000 <= 0.000 <= 0.000

BIT 27: