

L1:LSC

State-vector (ODC)

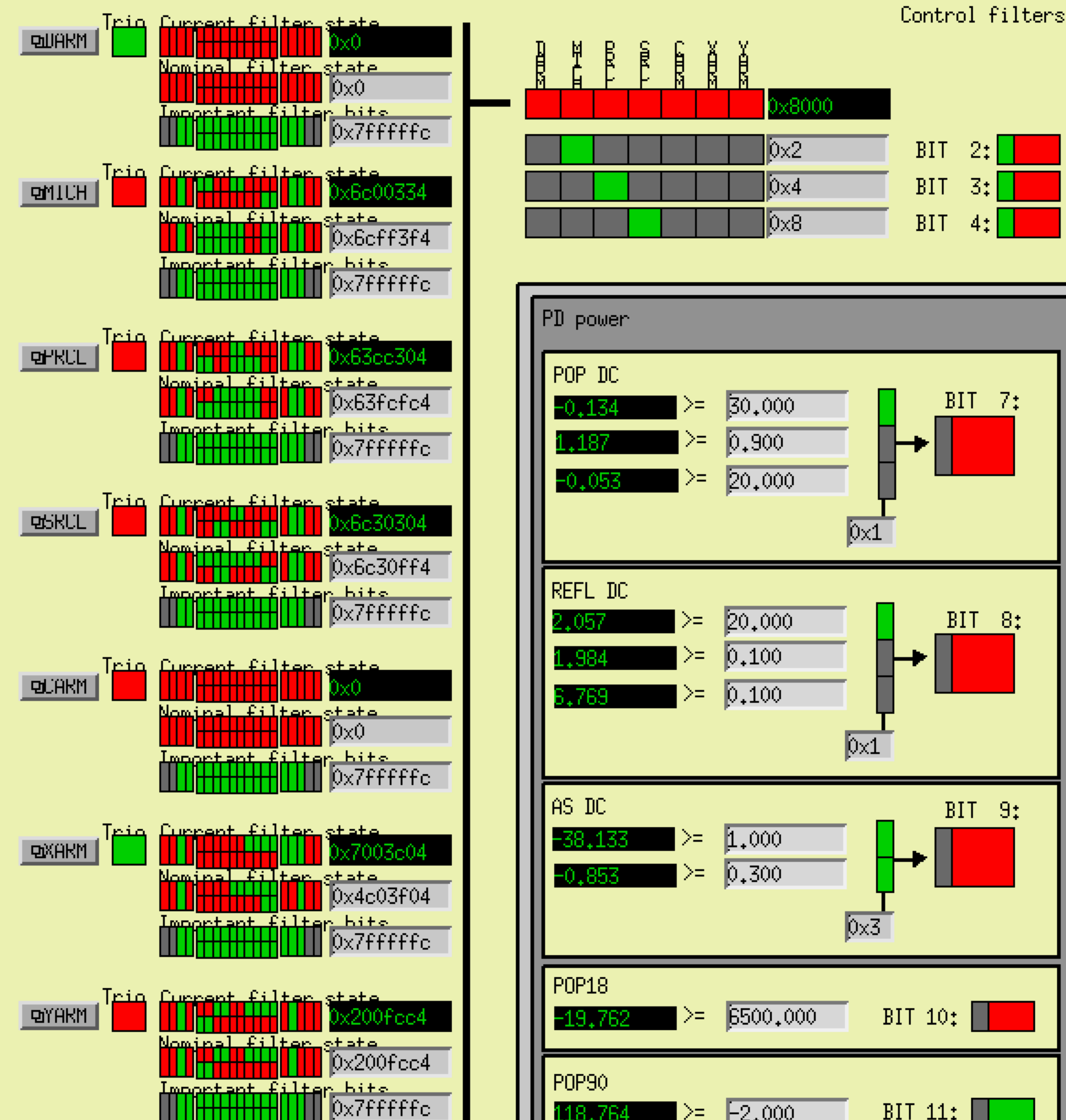
[L1:LSC-ODC_CHANNEL_LATCH]

(in bitmask?)

Bit 1:

Master
Switch

(bit on?)

Bitmask+
0x7e

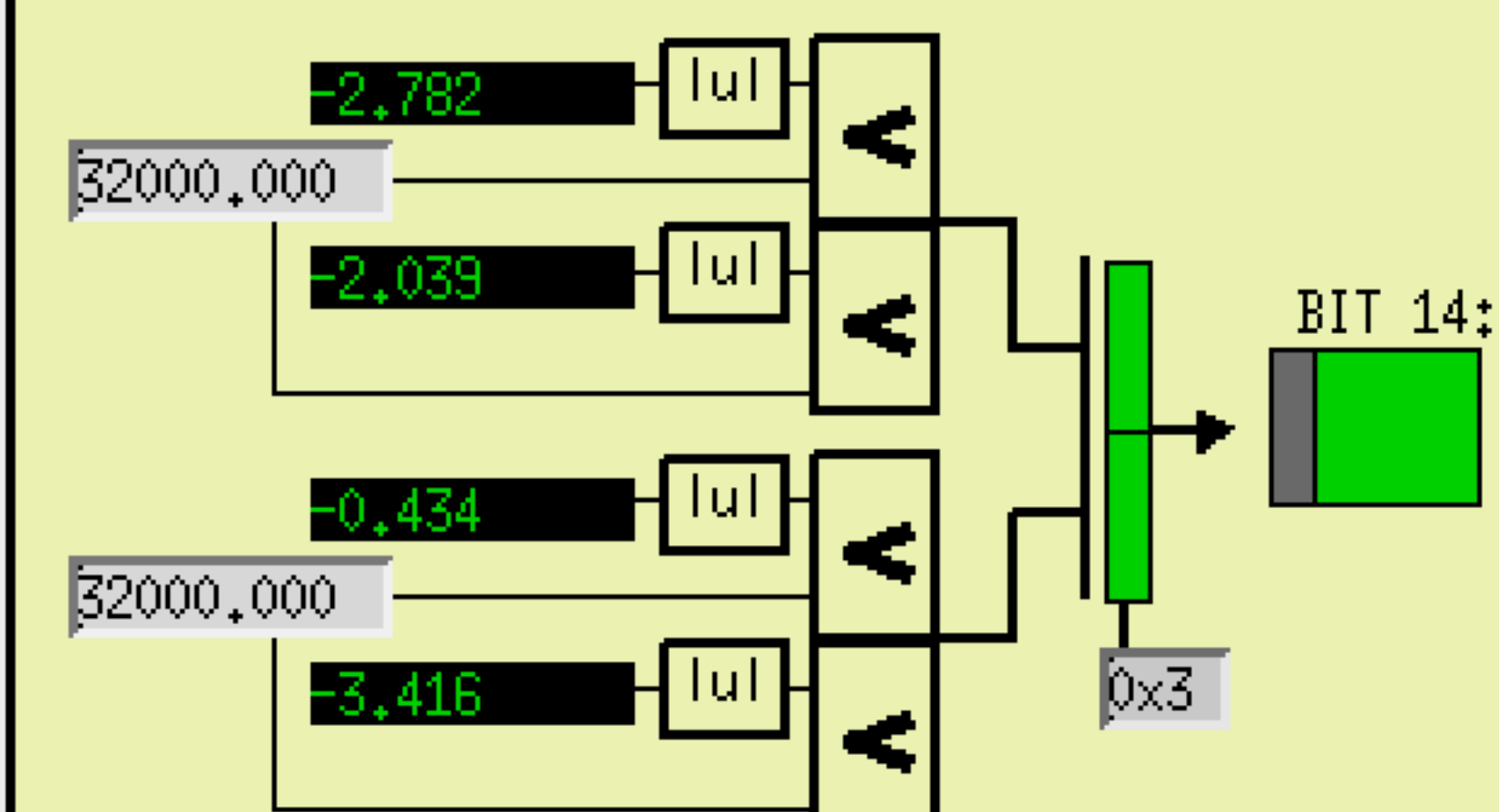
Transmitted arm power:

X -9.268 >= 850.000 BIT 5:

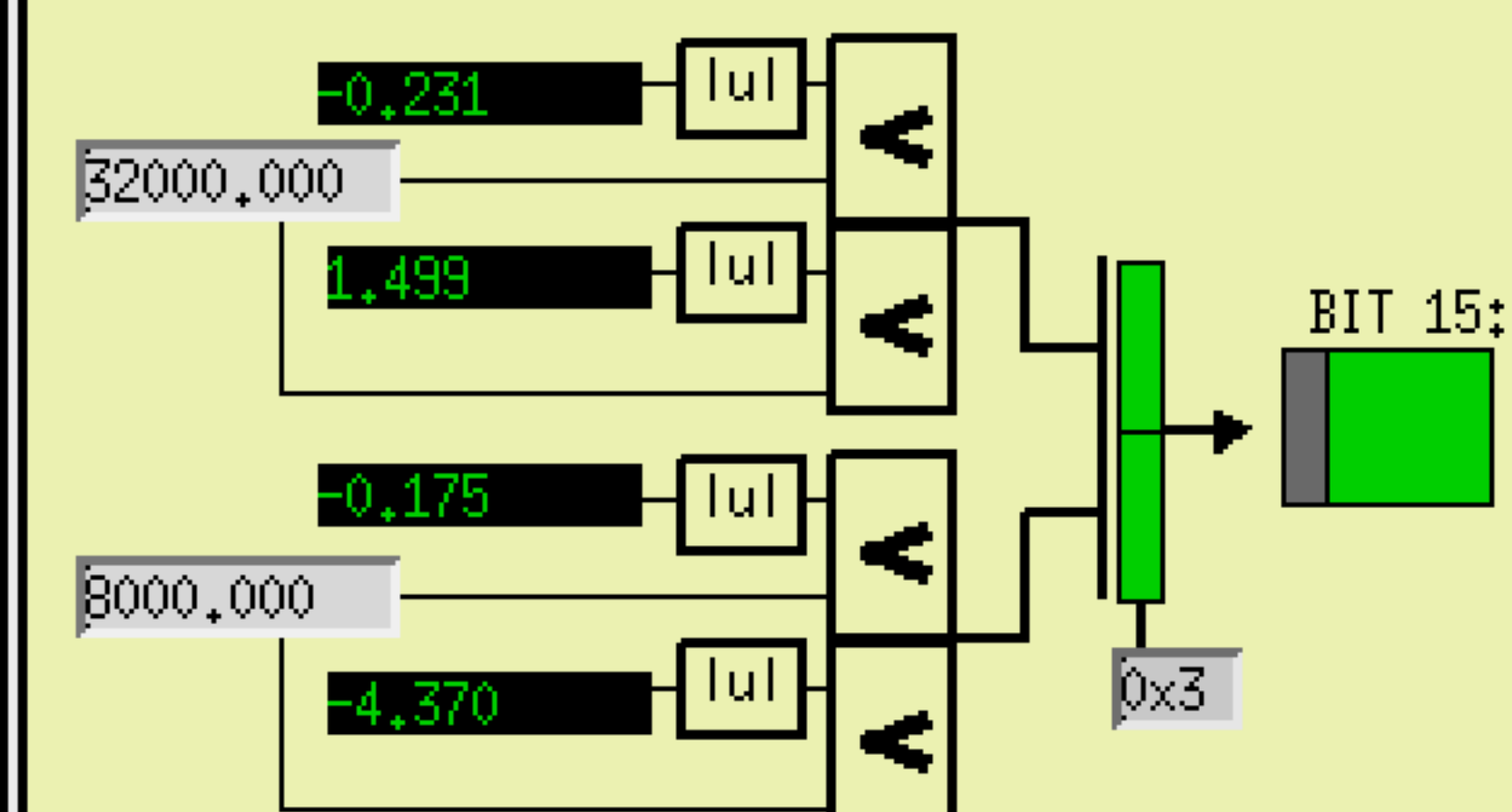
Y -24.250 >= 1000.000 BIT 6:

Saturations

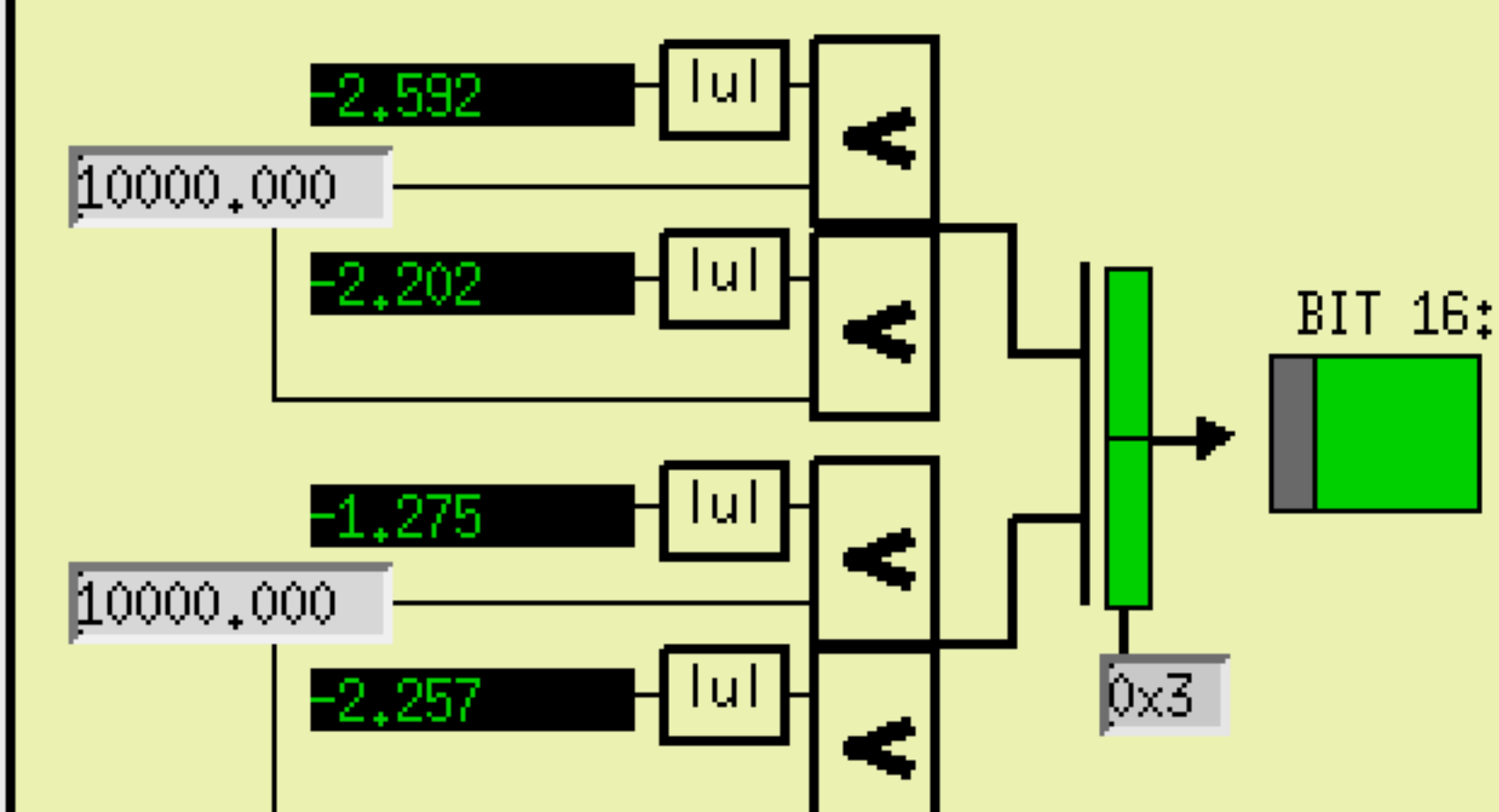
POP 9



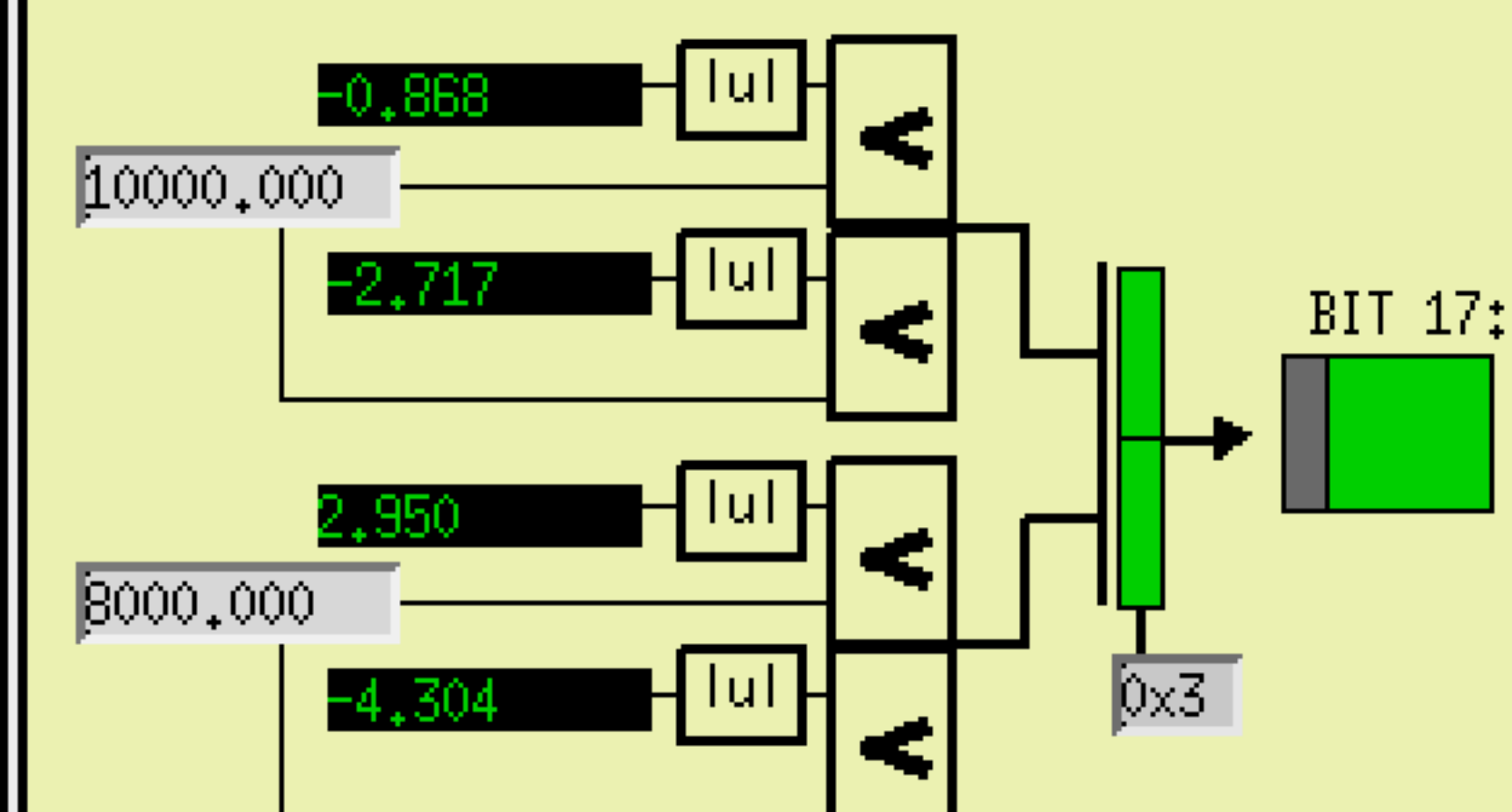
POP 45



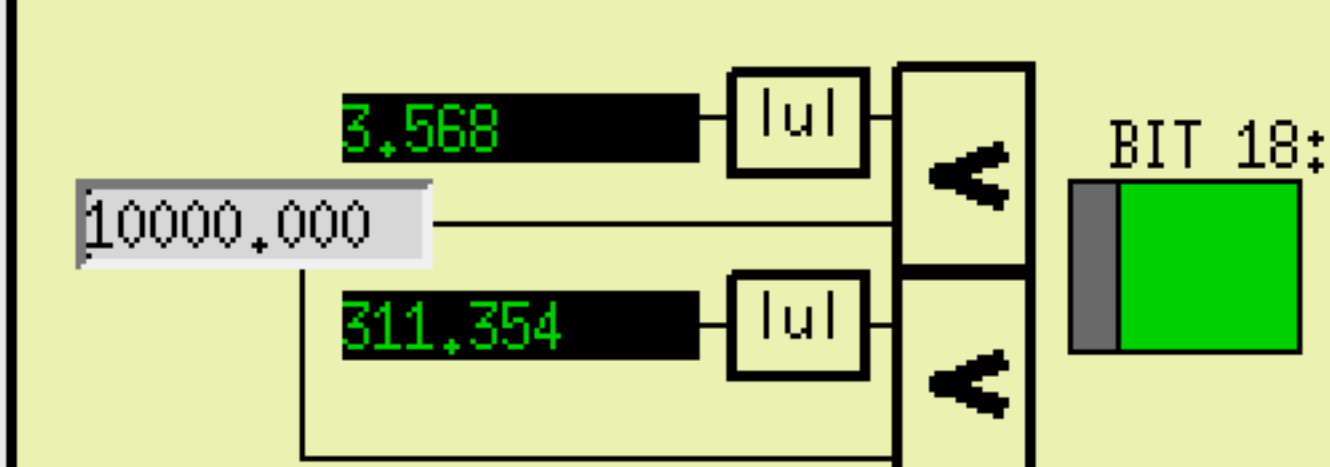
REFL 9



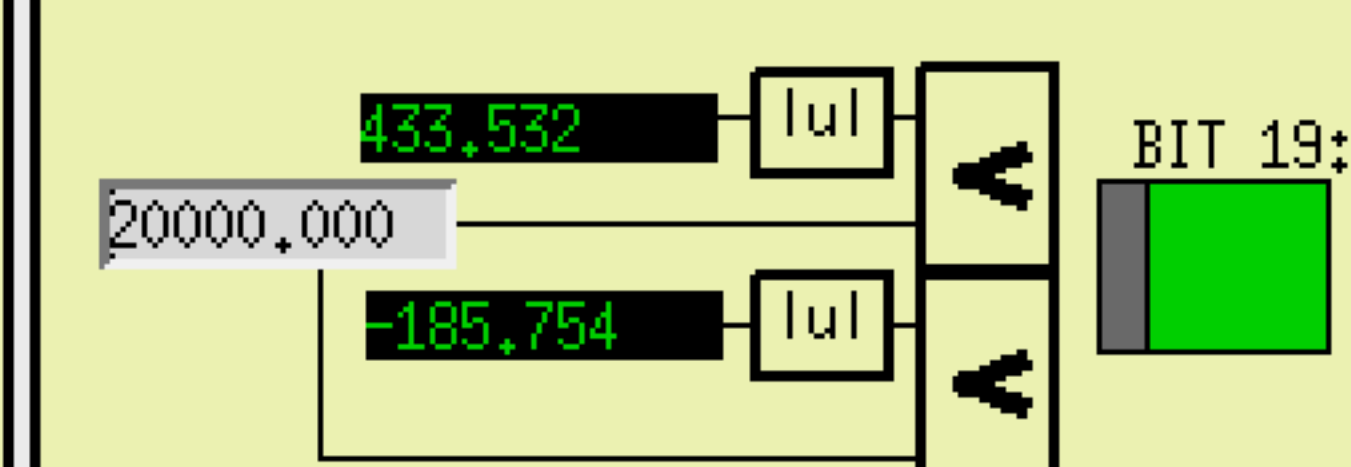
REFL 45



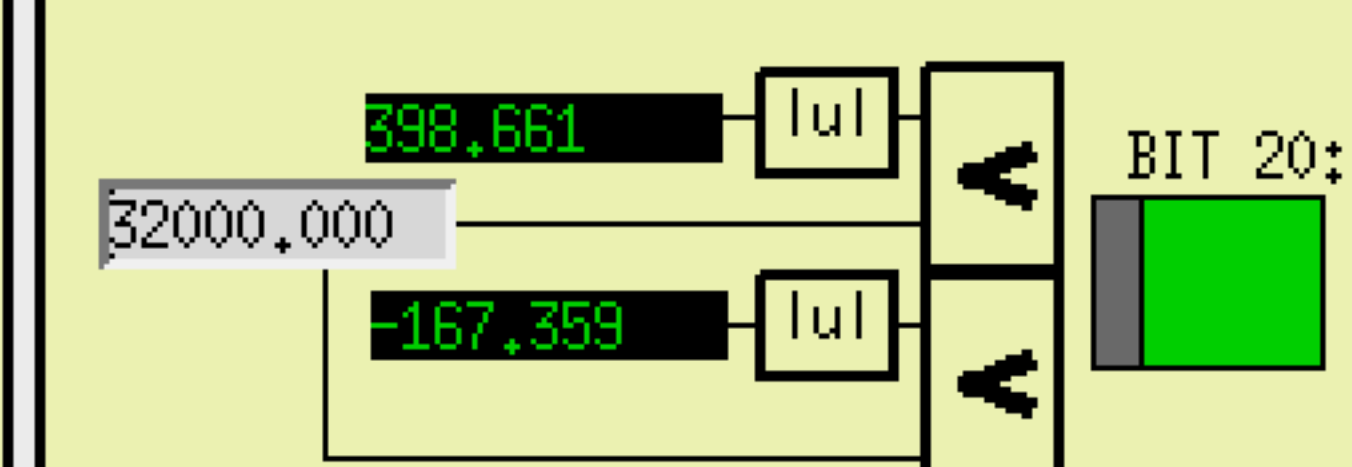
REFL 27



REFL 135



AS 45



OMC DC Power BIT 21:

1950.000 <= -0.054 <= 2150.000

DARM control range BIT 22:

-40000.000 <= 0.000 <= 40000.000

MICH control range BIT 23:

-250000.000 <= 0.000 <= 300000.000

PRCL control range BIT 24:

-20000.000 <= 0.000 <= 20000.000

SRCL control range BIT 25:

-70000.000 <= 0.000 <= 30000.000

CARM control range BIT 26:

0.600 <= 0.000 <= 0.500

ARM control range BIT 27:

X 0.000 <= 0.000 <= 0.000

Y 0.000 <= 0.000 <= 0.000