Swetha Varadarajan
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EDUCATION

PhD., Computer Science, Colorado State University - Fort Collins, CO, October 2021, GPA: 3.9/4
M.S., Electrical Engineering, Colorado State University - Fort Collins, CO, October 2017, GPA: 3.6/4
B.Tech.(Hons), Electronics & Communication Engineering, SASTRA university - TN, India, May 2013, GPA: 4/4

SKILL SET

C, C++, Python, Bash, OpenMP, MPI, CUDA. Novice: VHDL, Java, OpenCL, Verilog, SystemC, FORTRAN

INDUSTRY EXPERIENCE

Intel Corporation, Santa Clara, CA, March 2022 - Present
Graphics Hardware Engineer, Division - GPU Projection and Validation

- Hands-on experience in pre-Si GPU modeling of HPC and ML workloads, targeting Aurora Supercomputer.
- Activities include correlating the performance gap between two simulators, correlating the performance gap between the simulator/emulation/Silicon models, validating the performance of the GPU architecture for various frequency and architectural configurations, mapping and modeling of new hardware features.

ACADEMIA EXPERIENCE

Brown University, Providence, RI, Sept 2021 - Dec 2021
Research Software Engineer - HPC Team

- Conducted office hours and helped with HPC related consulting. Helped with organizing workshops on topics related to Slurm, Linux, and Matlab optimizations on the local supercomputer.
- I was also responsible for refactoring the python scientific codes. I helped with code assessment (identify hotspots and optimization opportunities) of Matlab-based scientific applications.

Colorado State University, Fort Collins, CO, Jan 2018 - July 2021
Graduate Research Assistant - HPC and Combinatorial Optimization

- Worked on hybrid genetic algorithms using local search and deterministic crossover operators to solve the jump function in O(N) time. Paper published in PPSN 2018.
- Developed a new genetic algorithm solver called the Mixing Genetic Algorithm (MGA) for the Traveling Salesman Problem (TSP). Key properties include reduced memory and zero communication costs during crossover operation. Paper published in GECCO 2019, SLS 2019, and GECCO 2020.
- Worked on perceptron-based neural network algorithms for biological modeling of female hormones.
- Parallelization of the MGA using OpenMP, MPI. Paper published in GECCO 2021.
- Parallelization of the MGA using CUDA on the GPUs.

Colorado State University, Fort Collins, CO, Aug 2014 – Oct 2017
Graduate Research Assistant – High-Performance Computing

- (MS Thesis) Parallelization and optimization of computations found in RNA-RNA interaction applications. The main computation was found to have a pattern similar to the Optimal String Parenthesization (OSP) problem but in 4D data space and 6D time. Improved the performance of the dominant computation found in these applications by 17x on single core and 112x on 6-core Intel Broadwell machines.

- **AlphaZ-apps:** Worked on writing polyhedral parts of large applications using a polyhedral DSL toolset called AlphaZ to generate optimized OpenMP C code. Paper published in RWDSL@CGO 2019.
    - List of Applications explored: RNA Folding, ABC (a quantum reactive scattering program), NuPACK, piRNA, IRIS, BPMax, RNA Secondary structure prediction.
    - Micro-benchmarking on CPU: Kernels include TMI, MM, OSP, DSYR2K
    - Micro-benchmarking on GPU: Kernels include MM and its variations, Knapsack
    - Tools used: Roofline Toolkit, Intel VTuneAmplifier, Cachebench, LMBench3, PAPI, ISL, Intel Memory Latency Checker, Processor Counter Monitor.
    - List of polyhedral tools used: AlphaZ, Pluto, Autogen.

INTERNSHIP EXPERIENCES

Singular Computing LLC, Boston, MA
Research Intern, Summer 2018

- Developed new heuristic-based algorithms for solving the Traveling Salesman Problem to be implemented on massively parallel SIMD approximate computing mesh architecture with 34,000 cores.
- Challenge was in the communication overhead. Obtained 2% of the optimal solution for 1,000 cities

Colorado State University, Fort Collins, CO
Research Programmer - Department of Forest, Rangeland and Watershed Stewardship, Summer 2014

- Studied and analyzed a CUDA application for calculating Haralick texture features.
- Adopted it for geo-referencing features and algorithms.

Lucas-TVS, Chennai, India
Intern – Embedded systems laboratory, Dec 2012 – April 2013

- Responsible for exploring the features of the Simulink-Stateflow model, implementing two applications using it, and giving a demo on using the tool to the company employees.
- Developed a Simulink-Stateflow model for the automatic stop-start mechanism of modern cars.
- Generated the code for TI's TMS320F controller series using Embedded Coder and TI's CCS.
- Developed PCB design for input and output signal conditioning. Simulated signals through switches, and function generators and ran laboratory-level experimentation using the TMS320F series microcontroller.

PEER-REVIEWED CONFERENCE PAPERS (selected)

S. Varadarajan and L.D. Whitley. A Parallel Ensemble Genetic Algorithm for the Traveling Salesman Problem, Genetic and Evolutionary Computation Conference (GECCO) 2021

S. Varadarajan, L.D. Whitley and G. Ocho. Why Many Traveling Salesman Problem Instances are Easier Than You Think, Genetic and Evolutionary Computation Conference (GECCO) 2020

S. Varadarajan and L.D. Whitley. The Massively Parallel Mixing Genetic Algorithm for the Traveling Salesman Problem, Genetic and Evolutionary Computation Conference (GECCO) 2019

L.D. Whitley, **S. Varadarajan**, R. Hirsch, and A. Mukhopadhyay. Exploration and Exploitation Without Mutation: Solving the Jump Function in O(n) time, Parallel Problem Solving from Nature (PPSN), 2018

EXTENDED ABSTRACTS

S. Varadarajan. Optimizing RNA-RNA interaction computations, IEEE/ACM International Symposium on Code Generation and Optimization (CGO), 2019 (**Poster** Presented on the same, **ACM SRC** at CGO 2019)