AT32 New Clock Configuration Tool

Introduction

This manual introduces how to configure AT32 MCU clock path and parameters using the clock configuration tool provided by ARTERY, and generate the corresponding clock configuration process code.

List of applicable Artery MCUs:

Part number	AT32F403
	AT32F403A
	AT32F407
	AT32F413
	AT32F415
	AT32F421
	AT32F435
	AT32F437
	AT32F425
	AT32WB415
	AT32L021

Contents

List of Tables

List of figures

1 Introduction

The AT32 clock configuration tool is a graphical configuration tool developed by ARTERY to facilitate the clock configuration of AT32 MCUs. It can help users clearly understand the clock path and configure the desired clock frequency.

1.1 Environmental requirements

- Software requirements

Windows 7 and above is required.

- Hardware requirements

PC/AT compatible, Pentium or higher CPU
XVGA (1024*768) color display
At least 512 M RAM
At least 100 M disk space

1.2 Installation

- **Software installation**

No need to install software, just run the executable program AT32_New_Clock_Configuration.exe.

2 Function overview

This section gives an overview of tool operations. The startup interface and configuration interface are shown below.

Figure 1. Startup interface

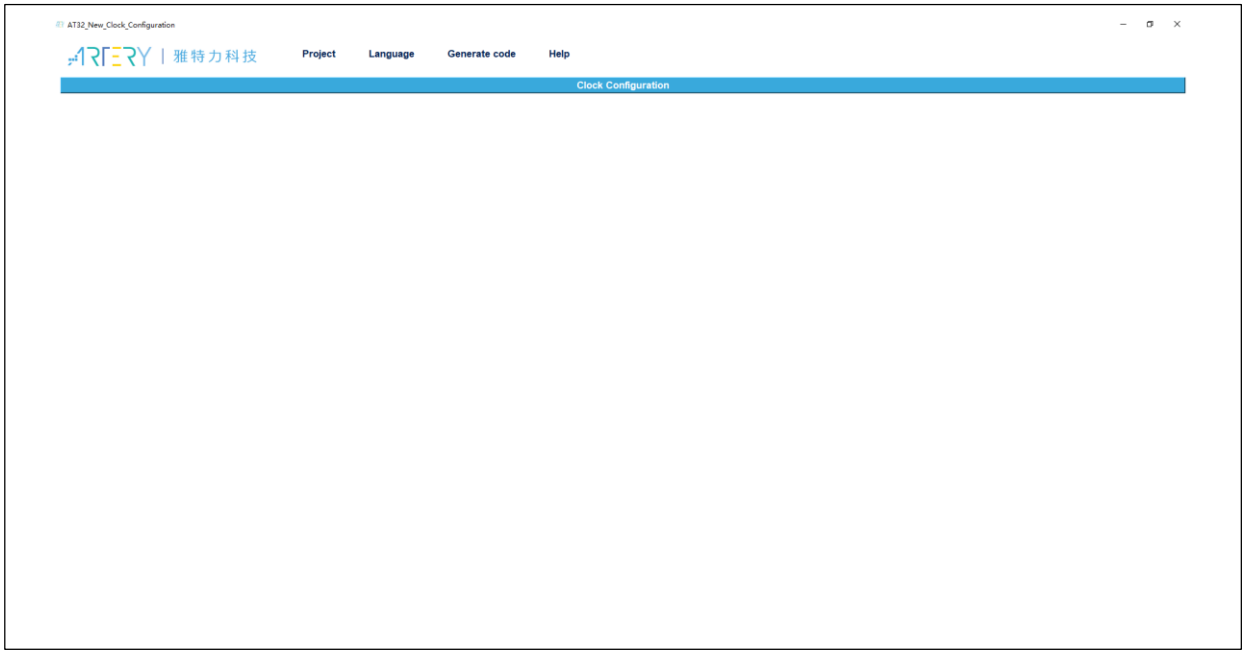
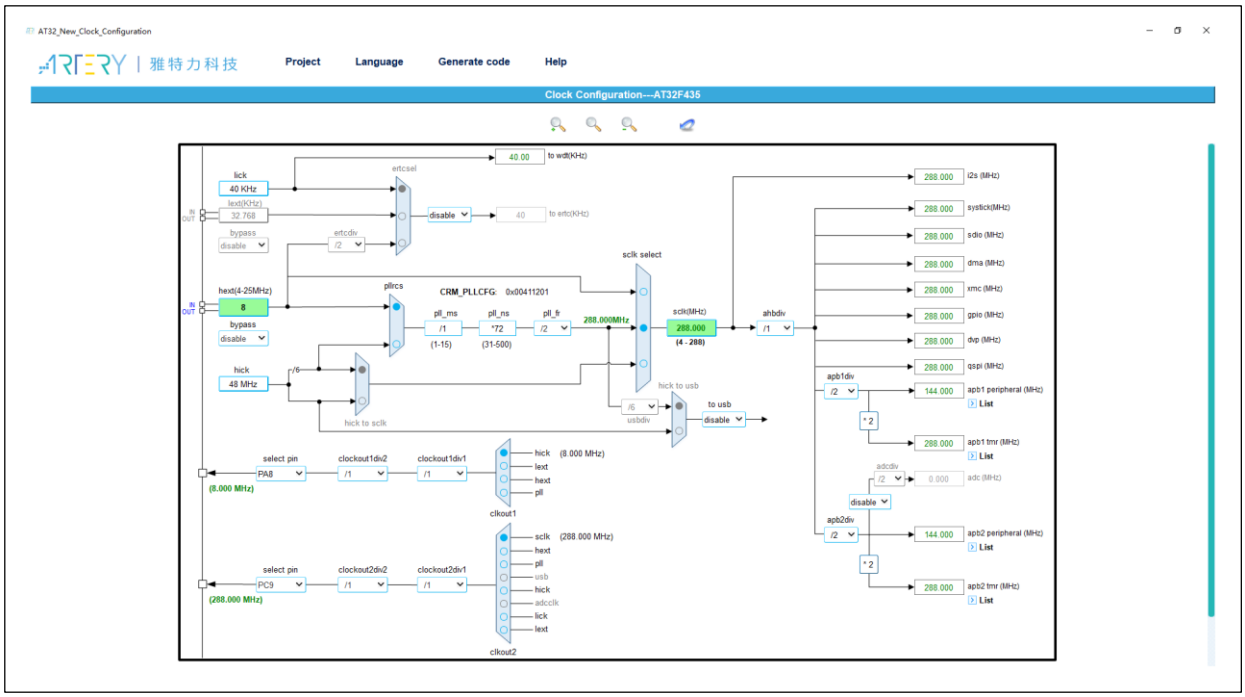


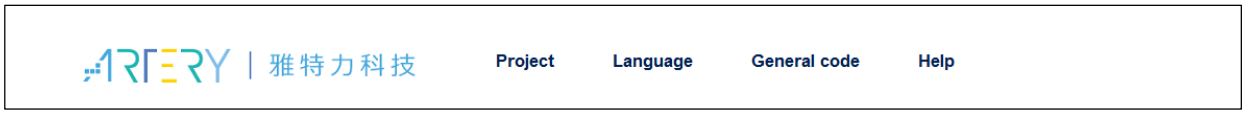
Figure 2. Configuration interface



2.1 Menu bar

The content of Menu Bar is shown in Figure 3.

Figure 3. Menu bar



- **“Project” menu**

  New: Create a new clock configuration project.

  Open: Open an existing configuration project.

  Save: Save the currently open configuration project.

- **“Language” menu**

  English: Select English as display language.

  Chinese: Select Chinese (Simplified) as display language.

- **“Generate code” menu**

  After configuring the desired clock path and clock frequency on the configuration interface of the corresponding part number, click “Generate code” to select the storage path and generate the corresponding source code file.

- **“Help” menu**

  Open Manual: Open the software manual. Please install a PDF browsing software on PC.

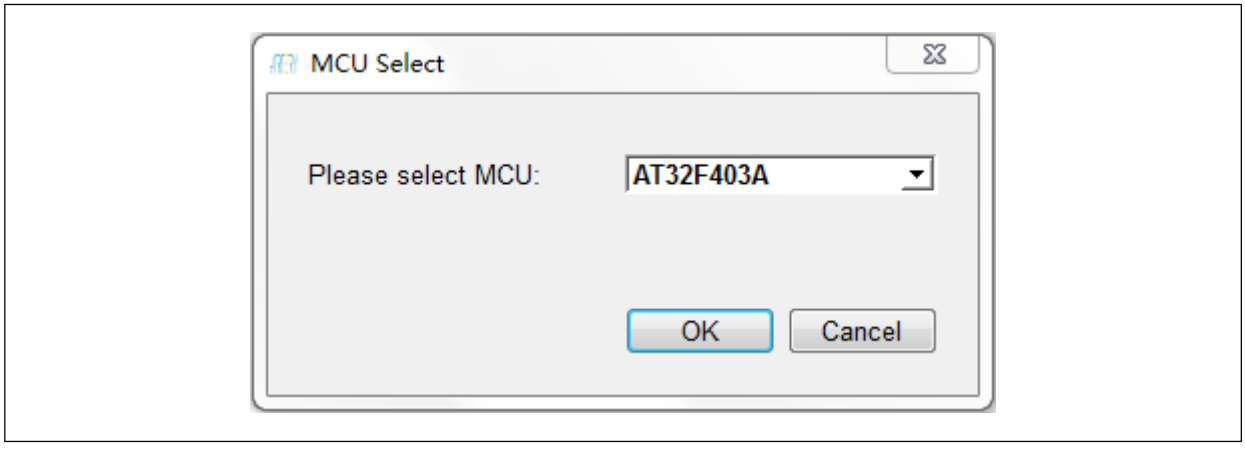
  New version download: Connect to the Internet to download the new version.

  Version: View the current version.

2.2 Create new configuration project

Double-click to open the clock configuration tool, and the startup interface will appear. Click “Project” –> “New” to create a new configuration project. Then, select the chip family, as shown in Figure 4.

Figure 4. MCU select interface



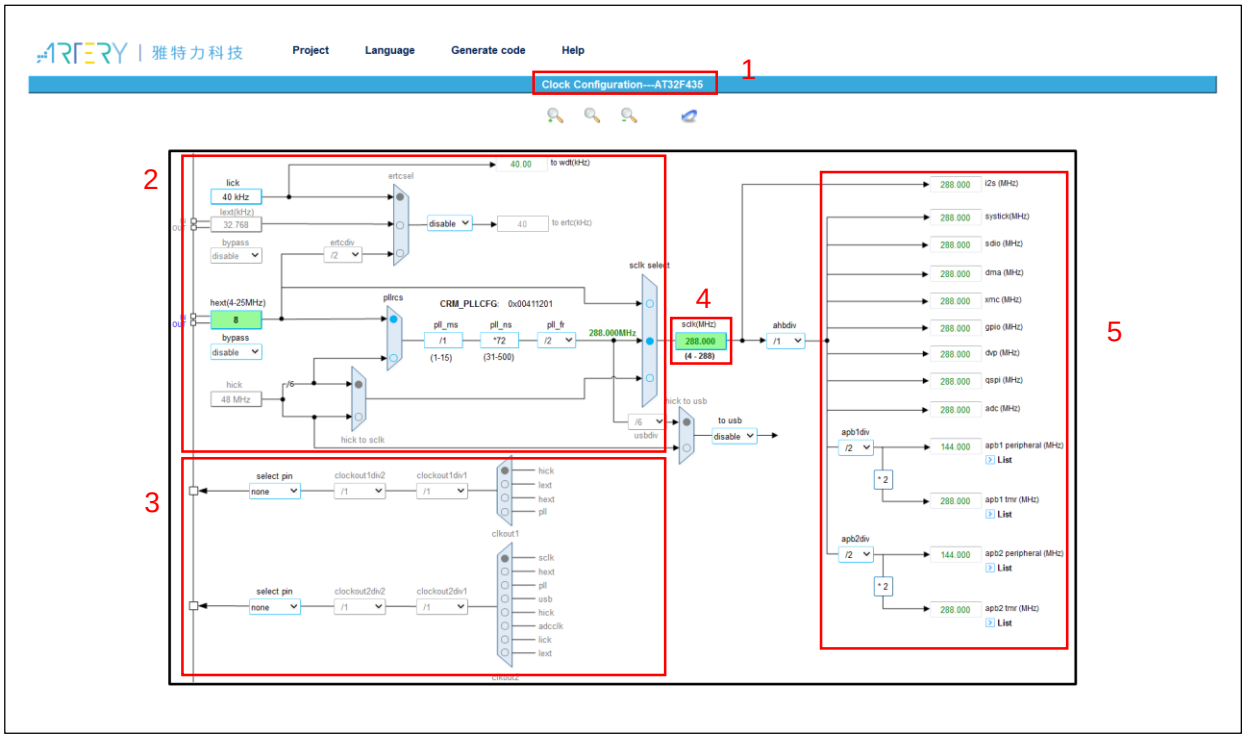
Click the drop-down box to select a MCU series. Then click “OK” to enter the clock configuration interface.

2.3 Configuration interface operation

Users can configure the clock path and parameters in the configuration interface. This section uses AT32F435 series as an example, and other series can be configured in a similar way.

The entire configuration interface can be divided into five blocks, as shown below.

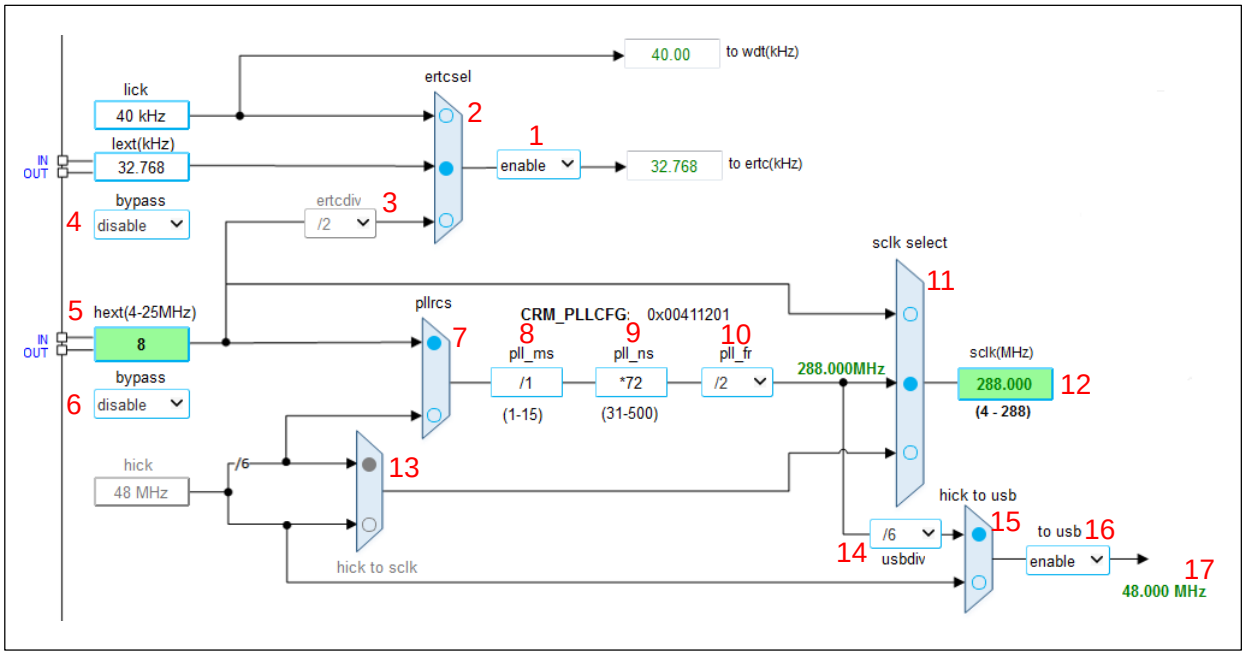
Figure 5. Configuration interface framework



1. Title: Display the MCU family selected for the current configuration project.
2. Configuration: Select and configure the clock path and parameters to meet application requirements.
3. Output: Configure the clock output (CLKOUT).
4. When PLL is selected as the system clock, the SCLK block can be used as the input box, and users can input the desired system clock frequency to automatically configure frequency multiplication parameters in a reverse way.
5. Result: Display the clock frequency used by the current peripherals, and peripherals on the bus.

Next is about the configuration block of the interface. Process interfaces in the configuration block correspond to MCU clock tree. The process interfaces may be different for each MCU series, but are used in a similar way. The configuration of clock path can be selected by clicking on each switch according to the process. The configuration block is shown in Figure 6, and functions of each process point are detailed below.

Figure 6. Clock configuration block



1. ertc enable: The “Enable” drop-down box for ERTC clock code configuration.
2. ertcsel: Check box, used to select the ertc clock source. When ertc is enabled, this check box can be configured.
3. ertcdiv: Drop-down box. When the HEXT is selected as the ERTC clock source, use this drop-down box to select the divider factor.
4. lext bypass: LEXT bypass enable.
5. hext: Input box. 8 MHz is the default frequency of the selected external clock source. Users can change the frequency according to the actual external clock source. (Note: When the default frequency of 8 MHz is changed, the HEXT_VALUE macro definition in inc/at32f435_437_conf.h in the demo directory of the corresponding BSP should also be modified consistently, or the at32f435_437_conf.h file generated by tools can be used).
6. hext bypass: HEXT bypass enable.
7. pllrcs: Check box, used to select HEXT or HICK to be the PLL clock source.
8. pll_ms: Input box. The PLL pre-divider factor is in the range of 1~15, and it is used to prescale the PLL input clock.
9. pll_ns: Input box. The PLL frequency multiplication parameter is in the range of 31~500, and it is used to multiply the frequency of the prescaled clock by PLL_MS.
10. pll_fr: Drop-down box. The PLL post-divider factor can be 1, 2, 4, 8, 16 or 32, and it is used to post-divide the frequency of the clock multiplied by PLL_NS. The clock derived from frequency division is the PLL clock.
11. sclk select: Check box. Select HEXT, PLL or HICK as the system clock.
12. sclk frequency: When using forward configuration, it displays the system clock frequency configuration. When using it as an input box, enter the desired frequency and hit the Enter key, and a set of PLL configuration parameters that are appropriate or closest to the desired value will be calculated inversely based on this input value.
13. hick to sclk: Check box. When HICK is selected as the system clock in “sclk select” block, the HICK can be set as 8 MHz or 48 MHz (Note: When 48 MHz HICK is selected as the system clock, the frequency when CLKOUT outputs HICK is also 48 MHz).
14. usbdiv: drop-down box. When PLL clock is selected as the USB clock source, users can

configure the division factor from PLL clock to USB clock.

15. hick to usb: Check box. The USB clock source can be set as PLL clock or HICK 48 MHz. Click the drop-down box “to sub” to select the USB clock configuration code. Because the USB clock needs to be set as fixed 48 MHz, the frequency multiplied by PLL may not meet the USB 48 MHz requirement under the premise that the division factor can be configured in usbdiv.
16. USB enable: Drop-down box, used to enable the USB clock code configuration.
17. USB clock frequency display. This display field will calculate USB clock frequency in real time and display the frequency value. If the USB clock is not configured to 48 MHz, the USB clock frequency will be displayed in red. When USB clock is not used in practical application, select “disable”, and no frequency value will be displayed (Note: This is only for the configuration of USB clock frequency, and users need to enable the USB peripheral clock separately).

2.4 Generate code

When the clock configuration is completed, click to generate code, then select the code generation path and confirm. Then, two folders (inc and src) will be generated in the selected directory. The source files are stored in the “src” folder, and header files are stored in the “inc” folder. These files can be used in conjunction with projects in BSP_V2.x.x. Users can use the newly generated clock code file (at32f4xx_clock.c/ at32f4xx_clock.h/ at32f4xx_conf.h) to replace the corresponding files in the original BSP demo, and call the system_clock_config function in the main function.

2.5 Precautions

When using this clock configuration tool, please pay attention to:

1. The clock configuration source files generated by this tool should be used in conjunction with the BSP_V2.x.x provided by ARTERY.
2. The clock configuration source files generated by different MCUs cannot be mixed, and can only be called in the corresponding project.
3. After modifying parameters in each input box of the configuration tool, please press “Enter” key to complete modification.

For more details on the use of AT32_New_Clock_Configuration too, AT32 clock configuration process and code analysis, please refer to the AN of each model. Users can download the following ANs from ARTERY official website.

Table 1. Clock configuration application note

Model	Application note
AT32F403A/407	AN0082
AT32F435/437	AN0084
AT32F421	AN0116
AT32F415	AN0117
AT32F413	AN0118
AT32F425	AN0121
AT32L021	AN0134

3 Revision history

Table 2. Document revision history

Date	Version	Changes
2022.07.15	1.0.1	1. Support for AT32L021.
2022.06.09	1.0.0	Initial version

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