Roderick S. Bayliss III

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Education

Ph.D. in Electrical Engineering — Expected May 2026
University of California, Berkeley, CA
Research Focus: Power Electronics – *Advisor:* Dr. Robert Pilawa-Podgurski

M.Eng. in Electrical Engineering — December 2020
Massachusetts Institute of Technology, Cambridge, MA
Research Focus: Power Electronics – *Advisor:* Dr. David J. Perreault
Thesis: Design, Implementation, and Evaluation of High-Efficiency High-Power Radio-Frequency Inductors

B.S. in Electrical Engineering — December 2019
Massachusetts Institute of Technology, Cambridge, MA

Research Experience

Graduate Research Assistant — January 2021 - Present
University of California, Berkeley – *Advisor:* Dr. Robert Pilawa-Podgurski

- Developed and experimentally evaluated control algorithms for the FCML converter utilizing active flying capacitor voltage balancing to enable Buck-type PFC applications.
- Analyzed both the circuit dynamics and relevant parasitics of the FCML converter to characterize and understand underlying dynamic behavior.
- Developed a high-performance FCML converter testbed to validate high bandwidth controls and flying capacitor voltage estimation using a single voltage sensor.
- Integrated multiple high performance FCML converter prototypes and developed motor control algorithms and firmware to enable a dynamometer testbed for high level count FCML converters.

Graduate Research Assistant — January 2020 - December 2020
Massachusetts Institute of Technology, Cambridge, MA – *Advisor:* Dr. David J. Perreault

- Designed and manufactured a high efficiency, radio frequency inductor for high current applications.
- Designed a high accuracy test fixture to characterize RF high-Q inductors at high currents.

Research Student — January 2018 - December 2019
Massachusetts Institute of Technology – *Advisor:* Dr. David J. Perreault

- Researched the behavior of high frequency magnetic materials for power stage components.

Selected Academic Honors and Awards

2022	The Hertz Foundation: Hertz Fellow
2021	University of California, Berkeley: Chancellor's Fellowship
2021	IEEE Applied Power Electronics Conference, Best Presentation Award
2019	IEEE Power and Energy Scholarship Plus Initiative, Scholarship Recipient

Publications

Journal Publications

2. **R. S. Bayliss III**, N. C. Brooks, R. C. N. Pilawa-Podgurski, "On the Role of Switch Output Capacitance on Passive Balancing within the Flying Capacitor Multilevel Converter," *IEEE Transactions on Power Electronics*, vol. 40, no. 2, pp. 3275-3285, Feb. 2025

1. R. K. Iyer, I. Z. Petric, **R. S. Bayliss**, N. C. Brooks, R. C. N. Pilawa-Podgurski, "A High-Bandwidth Parallel Active Balancing Controller for Current-Controlled Flying Capacitor Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 39, no. 10, pp. 12951-12965, Oct. 2024

Conference Publications and Presentations

10. **R. S. Bayliss III**, R. C. N. Pilawa-Podgurski, "A Buck-Type PFC Rectifier Employing the Flying Capacitor Multilevel Converter for Data Center Power Delivery," *2024 Open Compute Project Future Technologies Symposium*, San Jose, California, 2024
9. M. V. Joisher, **R. S. Bayliss**, M. K. Ranjram, R. S. Yang, A. Jurkov and D. J. Perreault, "High-Performance High-Power Inductor Design for High-Frequency Applications," *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA, 2024
8. **R. S. Bayliss**, N. C. Brooks, R. C. N. Pilawa-Podgurski, "A Combined Power Factor Correcting and Active Voltage Balancing Control Technique for Buck-Type AC/DC Grid-Tied Flying Capacitor Multilevel Converters," *2023 IEEE 24rd Workshop on Control and Modeling for Power Electronics (COMPEL)*, Ann Arbor, Michigan, 2023
7. R. K. Iyer, I. Z. Petric, **R. S. Bayliss**, N. C. Brooks, R. C. N. Pilawa-Podgurski, "A High-Bandwidth Parallel Active Balancing Controller for Current-Controlled Flying Capacitor Multilevel Converters," *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Orlando, FL, 2023
6. **R. S. Bayliss**, R. K. Iyer, R. Liou, R. C. N. Pilawa-Podgurski, "A Segmented Electric Aircraft Drivetrain Employing 10-Level Flying Capacitor Multi-Level Dual-Interleaved Power Modules," *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Orlando, FL, 2023
5. **R. S. Bayliss**, N. C. Brooks and R. C. N. Pilawa-Podgurski, "On the Role of Switch Output Capacitance on Passive Balancing within the Flying Capacitor Multilevel Converter," *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL)*, Tel Aviv, Israel, 2022
4. N. C. Brooks, R. K. Iyer, **R. S. Bayliss** and R. C. N. Pilawa-Podgurski, "Fundamental State-Space Modeling Methodology for the Flying Capacitor Multilevel Converter," *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL)*, Tel Aviv, Israel, 2022
3. N. Pallo, **R. S. Bayliss** and R. C. N. Pilawa-Podgurski, "A Multi-Phase Segmented Drive Comprising Arrayed Flying Capacitor Multi-Level Modules," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA, 2021
2. **R. S. Bayliss**, R. S. Yang, A. J. Hanson, C. R. Sullivan and D. J. Perreault, "Design, Implementation, and Evaluation of High-Efficiency High-Power Radio-Frequency Inductors," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA, 2021 [**Best Presentation Award**]
1. A. Jackson, N. Pallo, **R. S. Bayliss** and R. C. N. Pilawa-Podgurski, "A Modular Multi-Phase Actively Controlled Resistive Load Bank with Zero-Current Switching Capability and Integrated Snubbers," *2021 IEEE Power and Energy Conference at Illinois (PECI)*, Urbana, IL, USA, 2021

Theses

1. **R. S. Bayliss**, "Design, Implementation, and Evaluation of High-Efficiency High-Power Radio-Frequency Inductors," M.Eng Thesis, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, 2021 [Online]. Available: https://dspace.mit.edu/handle/1721.1/130679

Teaching/Mentoring Experience

Teaching Assistant — January 2024 - May 2024
University of California, Berkeley — Evaluation Score: 6.95/7.0

- EE 113B - Power Electronics Design. Learn-by-design power electronic components, PCB layout, closed-loop control, and experimental validation.

Teaching Assistant — January 2024 - May 2024
University of California, Berkeley — Evaluation Score: 6.98/7.0

- EE 213B - Graduate Level Power Electronics Design. Learn-by-design power electronic components, PCB layout, closed-loop control, and experimental validation.

Research Mentor — August 2019 - Present
University of California, Berkeley

- Supervised and mentored several undergraduate students.
- Provided technical guidance and feedback and set project goals.

Graduate Student Advisor May 2021 - Present
Formula SAE Electric at University of California, Berkeley
- Taught engineering fundamentals such as best design and test practices in addition to high voltage safety.
- Held several design reviews evaluating student projects and providing explicit guidance.
- Guided students through project management and team organization to achieve the timeline required for building a competition ready racecar.

Teaching Assistant August 2020 - December 2020
Massachusetts Institute of Technology
- 6.002 - Circuits and Electronics. Fundamentals of lumped circuit abstraction.

Teaching Assistant January 2020 - May 2020
Massachusetts Institute of Technology
- 6.302 - Feedback Sytsem Design. Learn-by-design introduction to modeling and control of continuous and discrete-time systems.

Industry Experience

Vehicle Performance Modeling Intern Summer and Fall 2023
Tesla, Palo Alto, CA
- Worked closely with power electronics, drive inverter, and cell engineering teams to understand the vehicle level impact of new onboard charger and high voltage architectures.

Power Electronics Intern Summer 2020
SpaceX, Hawthorne, CA
- Reduced both size and cost of valve driver circuit by $> 55\%$ and verified performance with prototype design.

Power Electronics Intern Summer 2019
Tesla, Palo Alto, CA
- Used ANSYS Maxwell to perform design analysis on various transformer designs in high power dc-dc converters, optimizing for power density and efficiency.
- Characterized a vast amount of magnetic core materials across size and temperature to develop a material selection guide for future designs

Hardware Test Engineering Intern Summer 2018
Apple, Cupertino, CA
- Developed a Linux-based diagnostics system that sped up the development cycle by reducing the data acquisition time.
- Created power diagnostics for the Intel CPU such as verifying P and C-States

Invited Talks

April 26, 2023 "Next Generation Power Electronics: Overcoming Key Barriers for Electric Aircraft and Ultra Efficient Power Delivery for Data Centers", Stanford Electrical Engineering Colloquium Series, Palo Alto, CA.

Professional Service

2018 - Present Reviewer for the *IEEE Journal on Emerging and Selected Topics on Power Electronics*, *IEEE Applied Power Electronics Conference*, *IEEE Conference on Control and Modeling of Power Electronics*.

2024 - 2025 Hertz Foundation Summer Workshop Planning Committee Member

2025 University of California, Berkeley Graduate Admissions Student Reviewer for Energy Area

2021 IEEE PES/PELS UC Berkeley Student Chapter – Social Chair