

Electronics at U of T

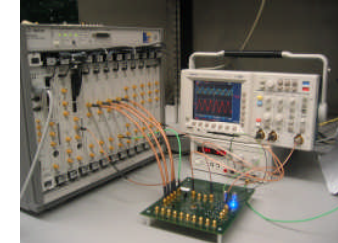
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Canada Research Chair in Integrated Systems
University of Toronto
www.eecg.utoronto.ca/~tcc

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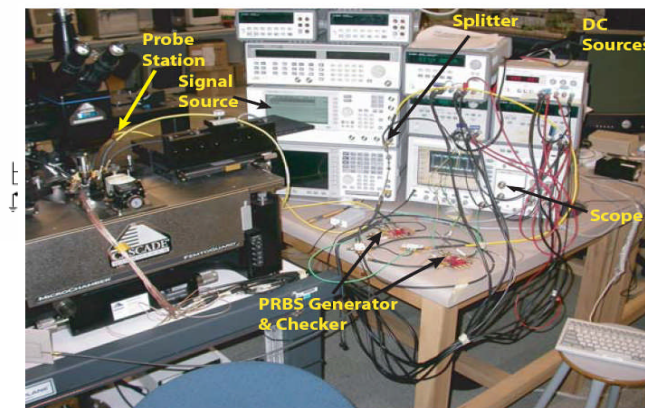
Some applications

- Digital communication
 - Biomedical
 - Radar
 - High-speed computing
 - Memories
 - Sensor networks
 - Reconfigurable hardware
 - Energy conversion
- and more...



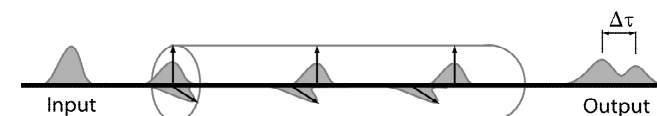
<http://www.vrg.utoronto.ca/EG/>

Integrated Circuits Research



Example M.A.Sc. Project

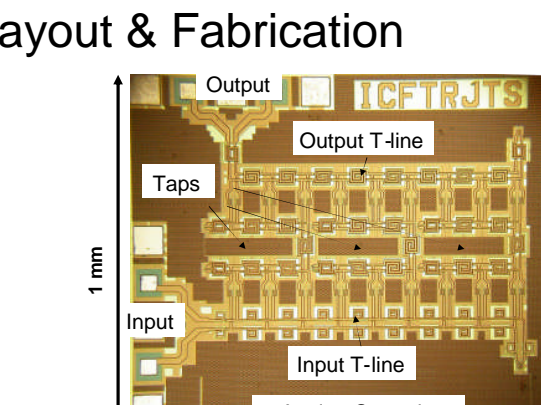
- 40-Gb/s optical fiber communications
- Polarization-mode dispersion



System-Level Analysis

- Matlab simulations used to identify difficult channels & derive specs for a compensator

A 3D surface plot showing the ISI Penalty (dB) as a function of the normalized time delay $\frac{\Delta\tau}{T_B}$ (ranging from 0 to 1) and the parameter γ (ranging from 0 to 1). The plot shows a sharp peak in ISI Penalty at $\gamma = 0.5$ and $\frac{\Delta\tau}{T_B} = 0.5$. A red circle highlights the peak region, and a red arrow points to it with the text: "Combinations of $(\gamma, \Delta\tau)$ with poor performance correspond to 2 equally split pulses:". To the right, a 2D plot shows two equally split pulses, each with a peak value of $\gamma = 0.5$.

- # Layout & Fabrication
- 
- A micrograph of the IC layout and fabrication. The image shows a complex circuit with various components labeled: Output, Output T-line, Taps, Input, Input T-line, and Analog Controls. The layout is rectangular, with a vertical dimension of 1 mm and a horizontal dimension of 1 mm. The circuit is fabricated on a brown substrate, and the components are interconnected by a network of gold-colored lines. The text "ICFTRJTS" is visible in the top right corner of the layout.

Circuit Design

- Adaptive equalizer

The diagram illustrates an adaptive equalizer circuit consisting of two parallel ladder networks. The top network, representing the feedforward path, starts with an input 'out' connected to a series inductor of value $L/4$. This is followed by a ladder structure of alternating series inductors ($L/2$) and shunt capacitors ($C/2$), with a final shunt capacitor $C/2$ and a series inductor $L/4$ leading to a load resistor R . The bottom network, representing the feedback path, starts with an input 'in' connected to a series inductor of value $L/4$. It follows a similar ladder structure of alternating series inductors ($L/2$) and shunt capacitors ($C/2$), ending with a series inductor $L/4$ and a load resistor R . The two networks are interconnected at three points, labeled p_1 , p_2 , and p_3 , which are indicated by dashed boxes and arrows. Each connection point p_i is represented by a trapezoidal block.

- # Testing
-
- The diagram illustrates a testing setup for a DFE (Digital Feed Forward Equalizer) circuit. The setup includes the following components and connections:
- Centellax OTB3P1A 10-Gbps PRBS Generator:** Two units are used. The left unit provides a Clock Input (0.5V, 100mV) and a Data Output (10GHz) to the DFE circuit. The right unit provides a Clock Input (0.5V, 100mV) and a Data Output (10GHz) to the DFE circuit.
 - Centellax AS64M1 40-Gbps 4-to-1 MUX:** A central multiplexer that receives signals from the two PRBS generators and outputs to the DFE circuit.
 - DFE Circuit:** The core component being tested, labeled "DFE". It has multiple inputs and outputs, including a 50GHz input, a 60GHz input, and a 40GHz output.
 - Agilent 86100C oscilloscope:** Connected to the DFE circuit to measure the output signal.
 - Agilent ER254D Signal Source:** A reference signal source connected to the DFE circuit via a Splitter and a 40GHz cable.
 - Cables and Probes:** Various cables (Long Cable, Short Cable) and probes (DC Block, 50GHz, 60GHz) are used to connect the components.
 - Power and Timing:** The setup is powered by -3.3V (100mA) and -3.3V (100mA) sources. The clock signal is 10GHz, and the data output is 10GHz.



<http://www.vrg.utoronto.ca/EG/>

Speakers:

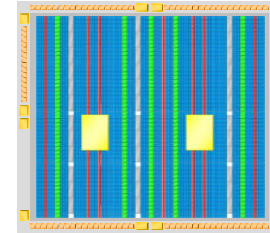
- Prof. J. Rose
- Prof. W.T. Ng
- Prof. R. Genov
- Prof. Y. Sun

FPGA Research: Architecture, CAD, Soft Processors and Systems

Jonathan Rose
Computer Engineering Group
and Electronics Group

Field-Programmable Gate Arrays

- Are pre-fabricated digital chips
 - Programmed to become anything
 - Including large systems!



FPGAs vs. Custom Silicon (ASICs)

- Advantages of FPGAs
 - Instant fabrication: **Seconds vs. Months**
 - Low cost prototyping; **\$100 vs. \$1M**
 - Cheaper at low volume
 - Don't need to sweat deep-submicron issues!
- Disadvantages of FPGAs
 - 20-30x more area
 - 3-4x slower
 - 10x more power consumption

If VLSI is the Technology of Our Time ...

FPGAs Democratize Technology of Our Time

- Make it accessible to everyone
 - Not just the rich who can afford ASICs
 - The small outfit in Singapore, Texas, Winnipeg
 - Small parts of large companies

My Goal

- To replace all digital silicon with FPGAs!
 - By making them better (architecture, CAD, ease of creation)
 - And using them in new ways for new applications
- The score so far:
 - \$4B FPGA, \$31B Custom Silicon (ASICs)
 - But 99% of all design is done with FPGAs!
 - Very few ASICs gather most of the market



How: FPGA Research: Architecture

- Make better FPGAs by improving their architecture
 - What is the logic
 - How to make the routing better

- Central Question of FPGA Architecture:

What logic should be made “hard”?

- Where can we reduce the costly flexibility?
 - Deep question with interesting theoretical & practical branches



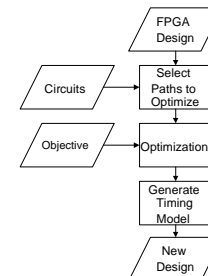
How: Computer-Aided Design

- Better tools make FPGAs faster, smaller, lower power
- High Level Synthesis
- Logic Synthesis
- Packing (memory, special structures, logic)
- Placement
- Routing
- To optimize: area, speed, power (dynamic and static)



How: The Creation of FPGAs Themselves

- Automated Layout of *FPGAs themselves*
- Automated Circuit Design of FPGAs
- Current Project:
 - Automating the transistor-level design of FPGAs



Systems & Applications

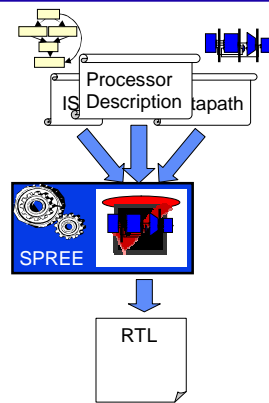
- The Transmogrieffier Project
 - Creation of programmable systems
- New System: The Transmogrieffier-4:
- Interested in applications on
 - Vision
 - Graphics
 - Bioinformatics – simulation
- Next Generation: Transmogrieffier-5
 - Super cheap
 - Portable – wireless/full system



Soft Processors

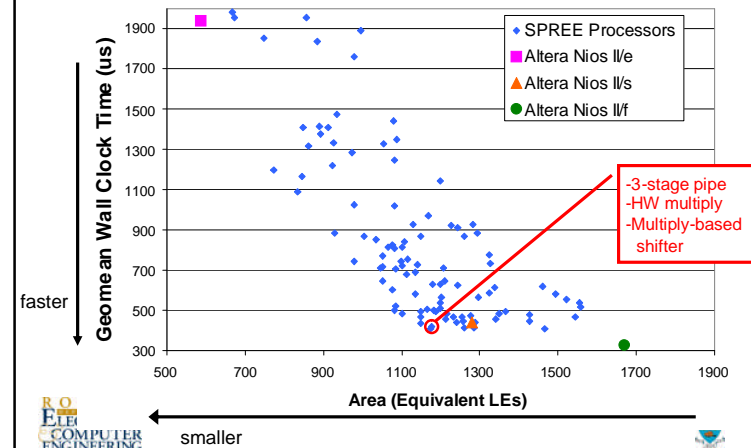
- For FPGAs to conquer, they must have good processors
- *Soft* processors are processors built on FPGA fabric
 - Fabric makes them slower, bigger than hard processors
 - Must use FPGA's flexibility to get this back!
- Example Projects:
 - Exploration of Soft Processor Micro-architecture
 - Super Small Soft Processor
 - Super Fast Soft Processor

Soft Processor Rapid Exploration (SPREE)



- Input: Processor Description
 - Hand-coded components, Datapath
- CAD/Compiler:
 1. Verifies ISA against datapath
 2. Instantiates Datapath
 3. Generates Control
- Output: Synthesizable Verilog

Spanning the Area/Speed Space

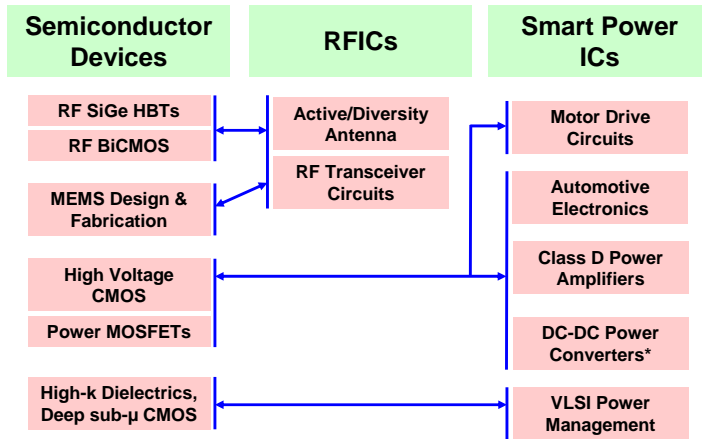


FPGAs: Poised To Conquer!

Smart Power ICs & Device Fabrication

Prof. W.T. Ng

Associate Chair, Undergraduate Studies



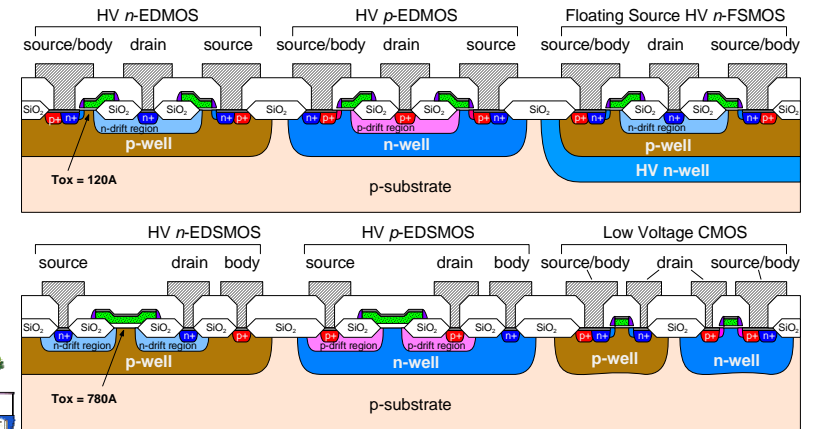
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* Also in collaboration with Prof. Prodic's Laboratory for Low-Power Management and Integrated Switch-Mode Power Supplies



HVCMOS – Customized VLSI Fabrication Process for Smart PIC applications

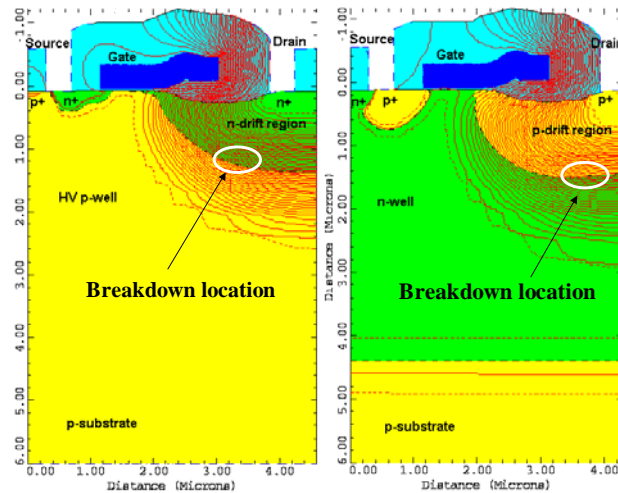
- A variety of HV, Power MOSFETs can be integrated onto the IC chip, accommodating both data processing and power electronic circuits.



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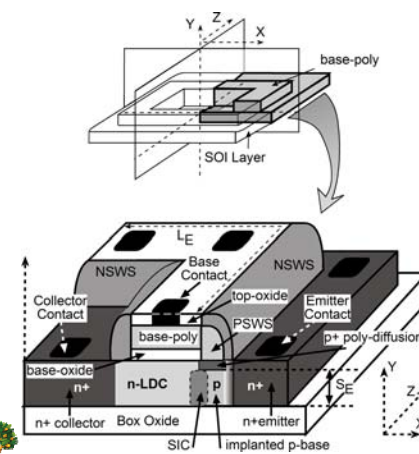
HVCMOS – Customized VLSI Fabrication Process for Smart PIC applications



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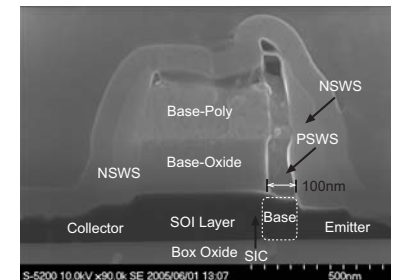


RF Devices: Lateral BJT on SOI



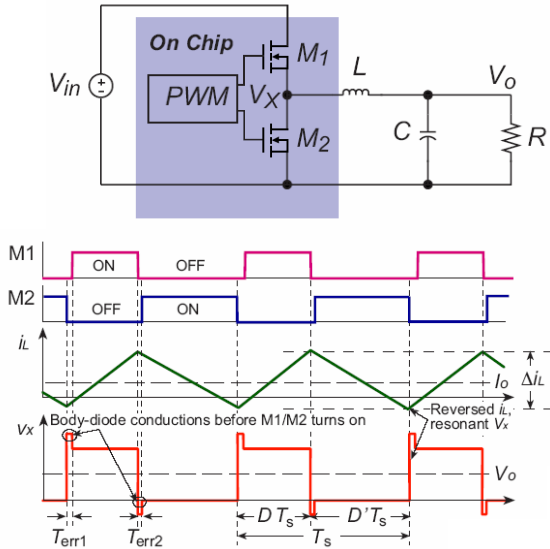
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* Best Young Researcher Award at ISPSD 2005
M.I-Shan Sun



High Efficiency Integrated DC-DC Converters

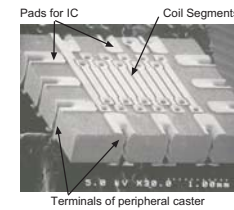
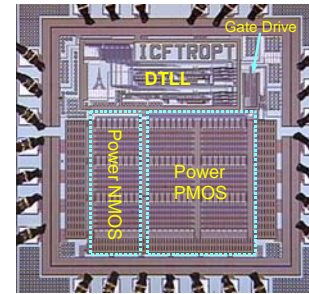
- Integrated PWM controller allows high switching speed e.g. > 5MHz
- Accurate gate drive timing to reduce unwanted switching losses.
- Requires predictive gate timing to make sure that the gate signal arrives at exactly the right moment.



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High Efficiency Integrated DC-DC Converters

- Design versatile digital controllers for various mode of DC-DC switching operations
- Use of miniaturized inductors to build true chip-size DC-DC converter modules.



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