Computer Architecture and Compilers

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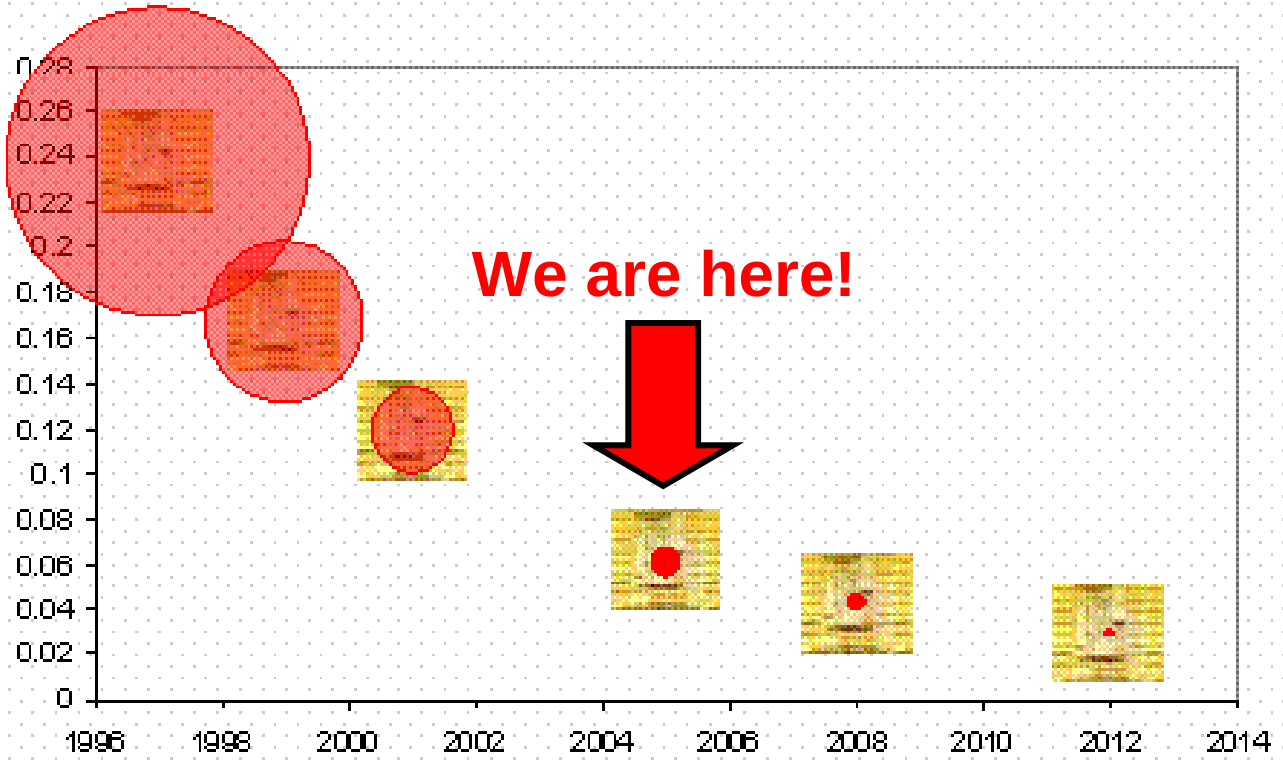
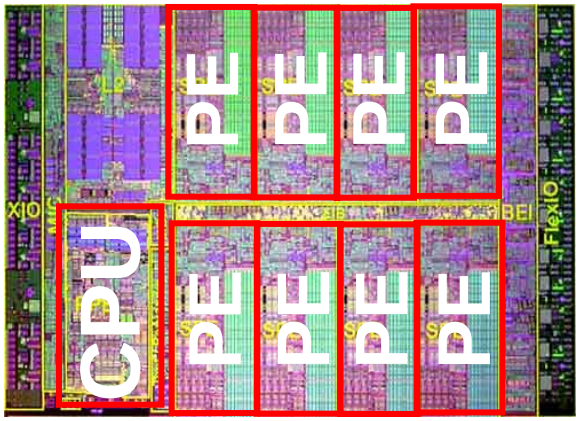
Trend1: Range of a Wire in One Clock Cycle



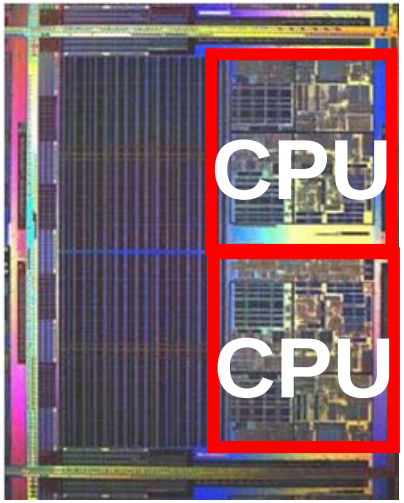
☞ **having one big processor soon infeasible**

☞ **this motivates distributed processing on a chip**

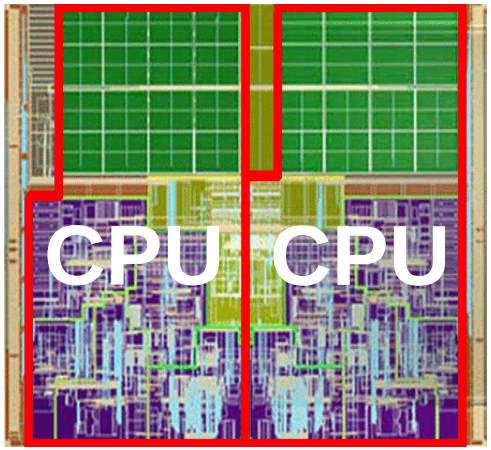
Some Current Chip Multiprocessors



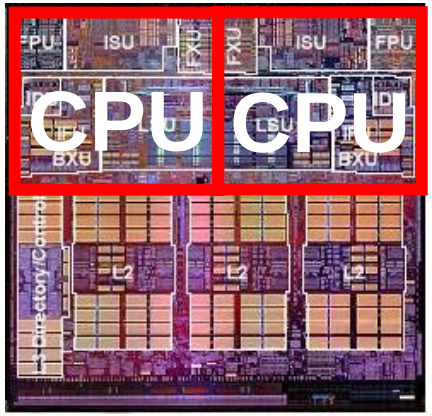
IBM Cell



AMD Opteron



Intel Yonah

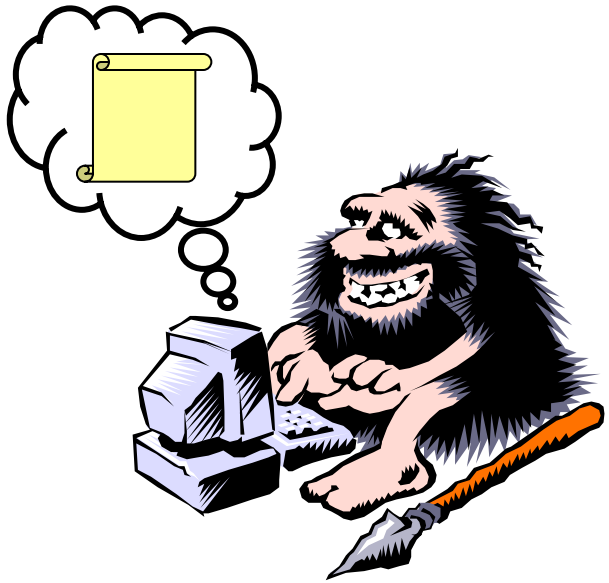


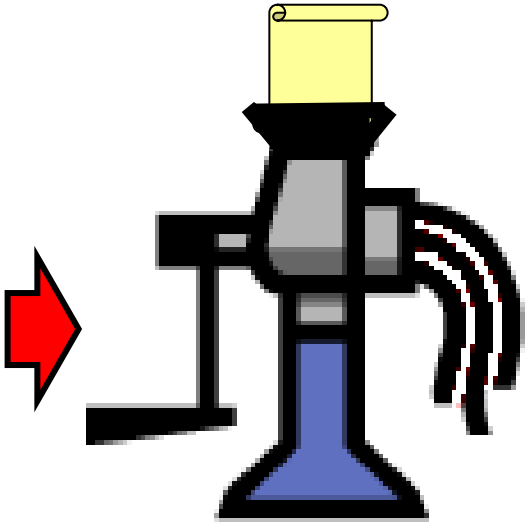
IBM Power4

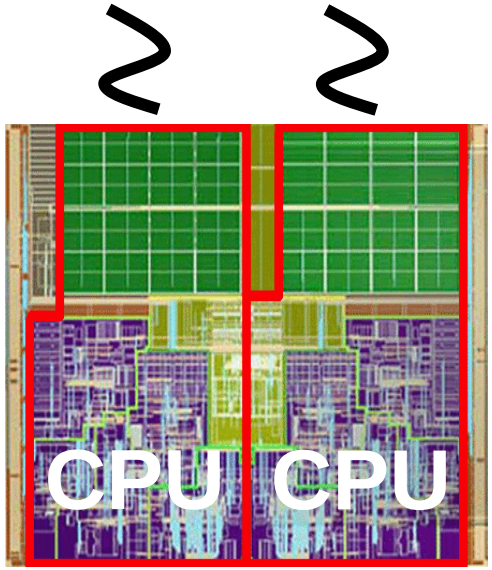
☞ **Improved throughput is straightforward**

☞ **How can these run one program faster?**

The Dream: Automatic *Parallelization*







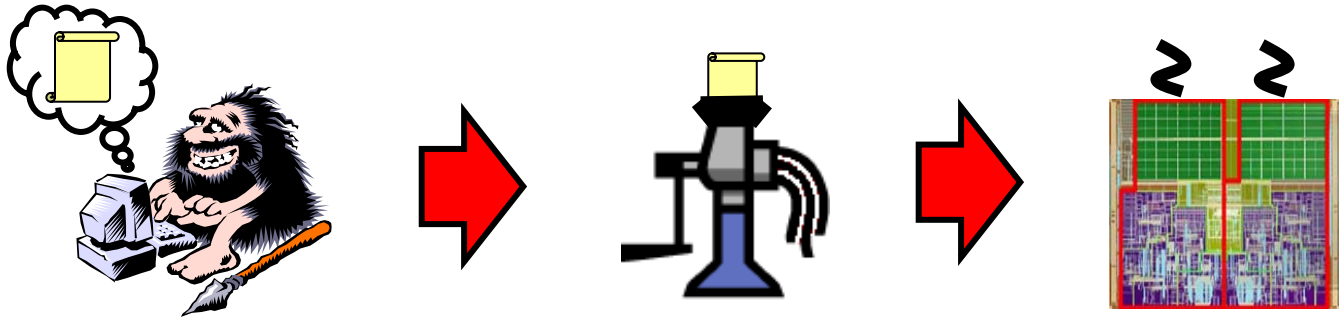
User writes a sequential program

Compiler and Runtime System *Parallelize* it

Multiple CPUs Execute the Program

☞ **easily exploit chip multiprocessors**

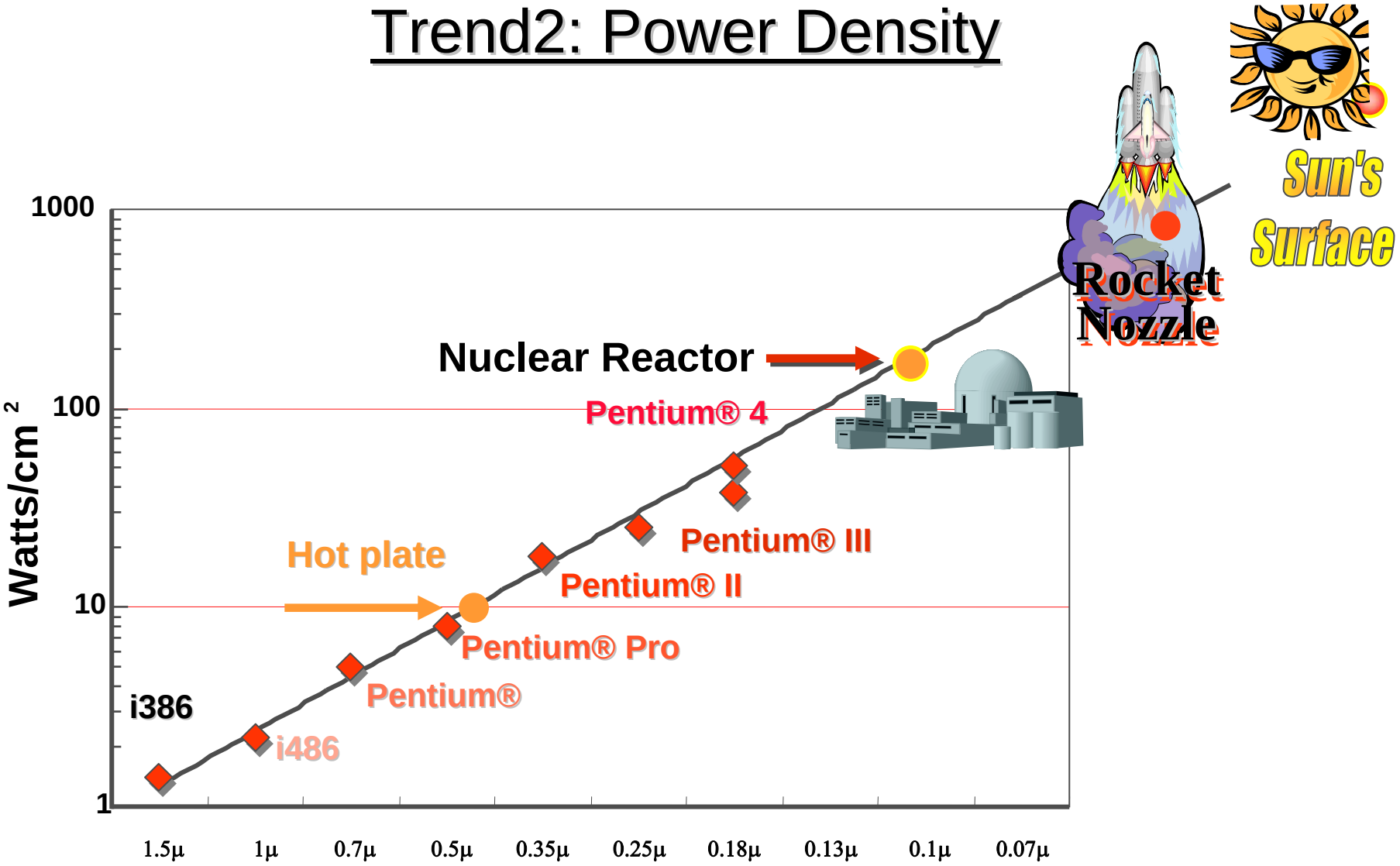
My Research (Part1)



- Making parallelization easier
  - For desktop apps, scientific simulations, databases…
- New chip multiprocessor architectures
- New compiler technologies

☞ **towards automatic parallelization**

Trend2: Power Density



The Dream: Doing More with Less Power

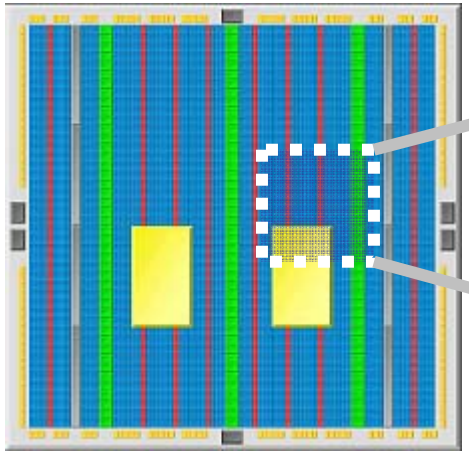
cell phone + PDA + MP3 player + digital camera + TV + ?

Ultra-Efficient Systems: Chameleon Computing

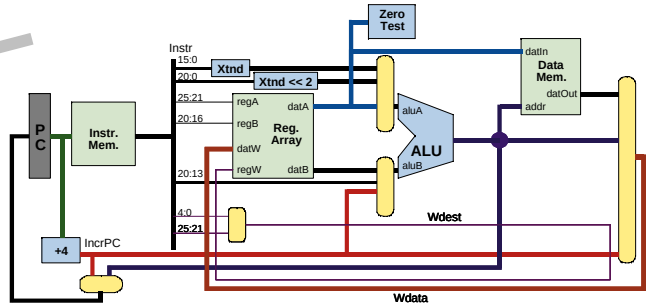
- Hardware that can be reconfigured
  - To exactly match application requirements
- Design custom systems automatically
  - To enable really fast time-to-market

My Research (Part2)

FPGA

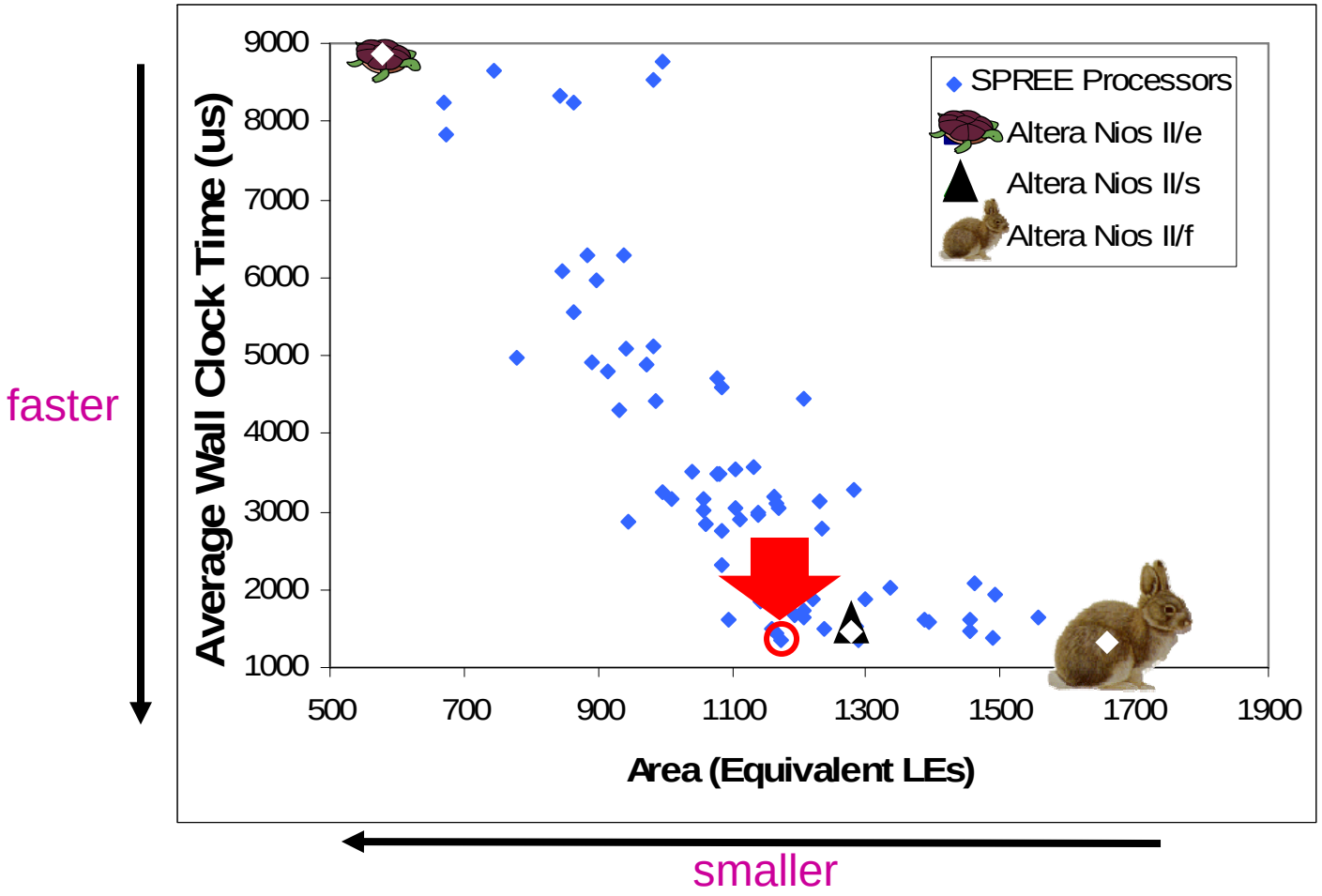


Processor



- Understanding "soft processor" architecture
  - A processor built out of an FPGA's reconfigurable logic
  - Revisit processor architecture in this new context
- "Soft Systems" that target FPGAs
  - New processors, compilers, OSs, platforms, applications

Our Soft Processors vs Altera Nios II Variants



☞ Competitive and can dominate (9% smaller, 11% faster)

The PaCRaT Team

Parallelization and Customization Research at U of Toronto