COMPUTER ORGANIZATION & ARCHITECTURE(COA)
[CS-2006]
Home Assignment-1

Roll Number:		**Section:**	
Name in Capital:			

Instruction: Answer all questions.

Find out the hexa-decimal equivalent of your roll number. Convert the last two hexa-decimal digits into octal number system.

Answer (Write here directly or paste here the image of your answer written on plane paper)

What is difference between Big Endian and Little Endian byte order. Explain with a computer system where each memory word consumes b bytes and machine is byte addressable by drawing suitable diagram(s). Take your roll number as the starting memory address. Take b (b≠0) as the last digit of your roll number. If it is zero take b=3.

Answer (Write here directly or paste here the image of your answer written on plane paper)

Let each memory word consumes 3 bytes and machine is byte addressable. The memory stores numbers from 1 to 20 sequentially starting from memory location ROLL that represent your roll number. The register R1 and R2 contain value 10 and 20 respectively. In each instruction, assume (from left to right) first operand as source, second operand as source as well as destination.

```
Move #ROLL, R0
Add  R1, 6(R0)
Move 3(R0), R1
Add #3, R0
Add (R0), R2
Sub R2, (R0)
```

After performing the following operations in sequence, find out the content of aligned addresses of your roll number. Show upto five consecutive word allignment.

Answer (Write here directly or paste here the image of your answer written on plane paper)

Let register R1 contains the binary equivalent of the last two digit of your ROLL NUMBER. Perform the following operations on R1 separately. Assume b is the number bits to be shifted or rotated. b=ROLL NUMBER % 7 +1.

LShiftL #b, R1
AShiftL #b, R1
LShiftR #b, R1
AShiftR #b, R1
RotateL #b, R1
RotateLC #b, R1 if C=0
RotateR #b, R1
RotateRC #b, R1 if C=0

Answer (Write here directly or paste here the image of your answer written on plane paper)

Consider a processor having four types of instruction classes, A, B, C and D, with the corresponding CPI values 1.a, 1.b, 2.c and 3.d respectively, where a, b, c & d represent the last four digit of your roll number counted from left to right. The processor runs at a clock rate of r GHz, where r is the sum of the digits of your roll number reducing to a single digit. For a given program, the instruction counts for the four types of instructions are 5, 10, 15 and 20 million respectively. Calculate the MIPS rating of this processor.

Answer (Write here directly or paste here the image of your answer written on plane paper)

The contents of memory locations 5000, 5100 and 6000 are 1000, 40 and 90 respectively before the following program is executed. [Here, the 2nd operand is the destination]

```
MOV #5000, R1
MOV 100(R1), R2
ADD R2, 6000
ADD (R1)+, R2
MOV R2, (5000)
```

What will be the contents memory locations 1000, 5000, 6000 and register R1 and R2 after the program is executed? Find out the number of memory references required for each of the instructions in the above program.

Answer (Write here directly or paste here the image of your answer written on plane paper)

A. Write the equivalent assembly code for the given pseudo code and write the values of the variables (both in decimal and binary) after executing each instruction present in the equivalent assembly code. Assume X is the sum of the last 3 digits of your roll number and memory size of the operand is 1 byte. [Note: if the Roll No = 20051123, then X =1+2+3=6][Assume the number is represented in 2's complement format]

```
A = (X +5);
B = -(X +4);
C = X ;
A>>2;          // Bitwise Right shift by 2bits
B<<1;                    // Bitwise left shift by 1 bit
Rotate_left(C, 2bit);      // Rotate Left by 2 bits
```

Answer (Write here directly or paste here the image of your answer written on plane paper)

A processor has 32 integer registers and and 16 floating point registers. It uses 2-byte instruction format. It has two types of instructions: Imm-type and REG-type. Each Imm-type instruction contains an opcode, an integer register name, and a 4-bit immediate value. Each REG-type instruction contains an opcode, 2 floating point register and one integer register names. If there are 16 distinct Imm-type opcodes, then what is the maximum number of distinct REG-type opcodes is possible ?

Answer (Write here directly or paste here the image of your answer written on plane paper)