**Sample Question Format**

**KIIT Deemed to be University**
**Online Mid Semester Examination (Spring Semester-2022)**

**Subject Name & Code:** Computer Architecture(CS-2006) **Applicable to Courses: 4th**

**Full Marks=20** **Time:1 Hour**

**SECTION-A(Answer All Questions. All questions carry 2 Marks)**

**Time:20 Minutes** **(5×2=10 Marks)**

<table>
<tr><th>Question No</th><th>Question Type(MCQ/SAT)</th><th>Question</th><th>Answer Key(if MCQ)</th><th>CO Mapping</th></tr>
<tr><td>Q. No :1(a)</td><td>Which of the following options represents the correct matching?
<table>
<tr><td>Addressing Mode</td><td>Description</td></tr>
<tr><td>1. Immediate</td><td>A. The address field refers to the address of a word in the memory, which in-turn contains the address of the operand.</td></tr>
<tr><td>2. Direct</td><td>B. The address field contains the address(in main memory) where the operand is stored.</td></tr>
<tr><td>3. Indirect</td><td>C. Operand value is present in the instruction itself(address field)</td></tr>
<tr><td>4. Register Direct</td><td>D. The address field of the operand is a register</td></tr>
</table>
a. 1->A; 2->D; 3->C; 4->B;<br>
b. 1->C; 2->B; 3->D; 4->A;<br>
c. 1->C; 2->B; 3->A; 4->D;<br>
d. 1->A; 2->D; 3->B; 4->C;</td><td>Question -1 on concept 1</td><td>C</td><td></td></tr>
<tr><td></td><td>An instruction SUB 3000<br>
a) Subtracts 3000 to the value in Accumulator and stores the result in the memory location 3030<br>
b) Subtracts the value in memory location 3000 to the value in Accumulator and stores the result in Accumulator<br>
c) Subtracts 3000 to the value in Accumulator</td><td></td><td>B</td><td></td></tr>
</table>

| | | | | |
|---|---|---|---|---|
| | and stores the result in Accumulator<br>d) None of the above | | | |
| | With reference to Addressing Modes consider the following statements:<br>a. In Implied Addressing mode the operands are specified implicitly in the definition of the instruction.<br>b. Zero-address instructions in a stack-organized computer are implied-mode instructions since the operands are implied to be on top of the stack.<br>c. In Immediate Addressing mode the operand is specified in the instruction itself.<br>d. In Register Addressing mode the instruction specifies a register in the CPU whose contents give the address of the operand in memory.<br>Which of the following statement/s are NOT correct?<br>A. Only (a)<br>B. Only (a), (b) and (c)<br>C. Only (d)<br>D. All of the above | | C | |
| | An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. If a processor register R1 contains the number 200 then the effective address for immediate and index with R1 as the index register addressing mode of the instruction will be:<br>a. 301 and 600 respectively<br>b. 400 and 702 respectively<br>c. 200 and 600 respectively<br>d. 702 and 400 respectively | | A | |
| Q. No :1(b) | After branch instruction execution, PC will updated to ______ ? (initial value of R1=100, R2=200 and SUB R1, R2 is equivalent to R2 <- [R2]-[R1])<br>(a) If it is Branch >0 1000<br>(b) If it is Branch <0 2000<br>(c) If it is JUMP 3000 | Question -1 on concept 2 | C | |

<table>
<tr><td></td><td>
<table>
<tr><td>Memory Location</td><td>Instruction</td></tr>
<tr><td>5000</td><td>SUB R1, R2</td></tr>
<tr><td>5004</td><td>Branch instruction</td></tr>
</table>
A. (a) PC=5008, (b) PC=5008, (c) PC=5008<br>
B. (a) PC=5008, (b) PC=6008, (c) PC=8008<br>
C. (a) PC=6008, (b) PC= 5008, (c) PC= 8008<br>
D. (a) PC=6008, (b) PC=8008, (c) PC= 5008
</td><td></td><td></td><td></td></tr>
<tr><td></td><td>Consider the code given below. What will be the offset for the instruction BGTZ to branch to the location labeled LOOP? All the instructions are 4 bytes in length.
<table>
<tr><td>5000</td><td>MOV #100,R1</td></tr>
<tr><td></td><td>MOV #LOCA,R2</td></tr>
<tr><td></td><td>CLEAR R3</td></tr>
<tr><td>LOOP</td><td>ADD (R2), R3</td></tr>
<tr><td></td><td>INCR R2</td></tr>
<tr><td></td><td>DEC R1</td></tr>
<tr><td></td><td>BGTZ ?</td></tr>
</table>
a) -8<br>
b) -12<br>
c) 8<br>
d) -16
</td><td>Question -2 on concept 2</td><td>D</td><td></td></tr>
<tr><td></td><td>A. Let R1 and R2 two 4-bit register that stores no in 2’s complement for operation<br>
R1 + R2. Which of the following values gives overflow:<br>
<br>
a. R1= 1111 R2=1101<br>
b. R1=1110 R2=1100<br>
c. R1=1000 R2=1100<br>
d. R1=1010 R2=1110
</td><td></td><td>C</td><td></td></tr>
<tr><td></td><td>B. Let R1 and R2 two 4-bit register that stores no in 2’s complement for operation<br>
R1 + R2. Which of the following values does not give overflow:<br>
<br>
a. R1= 1011 R2=1100<br>
b. R1=1010 R2=1101<br>
c. R1=1111 R2=1101<br>
d. R1=1110 R2=1001
</td><td>Question -4 on concept 2</td><td>C</td><td></td></tr>
</table>

| | | | | |
|---|---|---|---|---|
| Q. No :1( c) | A subroutine “**SUB**” is located at an address **100** in memory. **After the execution** of the following instruction, what will be the value of **offset**?<br>**Call SUB** // The instruction is located at address 3**00** and the length of the instruction is **4 bytes**.Processor uses byte addressable.<br>A. 200<br>B. 204<br>C. -204<br>D. -104 | Question -1 on concept 3 | C | |
| | The content of the top of memory stack is 2350. The content of SP is 1352. A two-word call subroutine instruction is located in memory address 4550 followed by<br>address field of 2454 at location 4554. What are the content of PC, SP and top of Stack, after the execution of **RETURN** instruction in sub-routine?<br>A. 4558, 1352, 2350<br>B. 4550, 1352, 2350<br>C. 2454, 1348, 4558<br>D. None of these | Question -2 on concept 3 | A | |
| | A subroutine “**ADD**” is located at an address **5000** in memory. **After the execution** of the following instruction, what will be the value of PC?<br>**Call ADD** // The instruction is located at address **1000** and the length of the instruction is **4 bytes**.<br>A) 5000<br>B) 1004<br>C) 11004<br>D) 5004 | Question -3 on concept 3 | A | |
| | A subroutine “**SUB**” is located at an address **2000** in memory. **After the execution** of the following instruction, what will be the value of **PC**?<br>**Call SUB** // The instruction is located at address 1**000** and the length of the instruction is **4 bytes**.<br>A. 1004<br>B. 2004<br>C. 2000<br>D. 2004 | Question -4 on concept 3 | C | |
| Q. No :1( d) | Two processor register R1 and R2 hold signed operand. If the binary value of the R1 is 0110 and R2 is 1000 then What will be the content of the registers R1 and R2 after the following instructions are executed. [Assume the Format | Question -1 on concept 4 | B | |

| | | | | |
|---|---|---|---|---|
| | of the instruction is **opcode source,source/Dst** and the size of each register is 4bit] [Assume the numbers are represented in 2's complement format]<br><br>ADD R1, R2<br>AShiftL #2, R1<br>AShiftR #1, R2<br>After the execution of the above three instructions<br>a. R1 and R2 both results in overflow.<br>b. R1 will overflow and R2 content will be 1111<br>c. R1 is 1110 and R2 will be 0111<br>d. None of the above | | | |
| | Two processor register R1 and R2 hold signed operand. If the binary value of the R1 is 1010 and R2 is 0001 then What will be the content of the registers R1 and R2 after the following instructions are executed. [Assume the Format of the instruction is **opcode source,source/Dst** and the size of each register is 4bit] [Assume the numbers are represented in 2's complement format]<br>ADD R1, R2<br>AShiftL #2, R1<br>AShiftR #2, R2<br>After the execution of the above three instructions<br>a. R1 and R2 both results in overflow.<br>b. R1 content will be 0,100 and R2 content will be 1110<br>c. R1 is 1110 and R2 will be 1,110<br>d. None of the above | Question -2 on concept 4 | D | |
| | Two processor register R1 and R2 hold signed operand. If the binary value of the R1 is 1111 and R2 is 1110 then What will be the content of the register R1 and R2 after the following instructions are executed. [Assume the Format of the instruction is **opcode source,source/Dst** and the size of each register is 4bit] [Assume the numbers are represented in 2's complement format]<br>ADD R1, R2<br>AShiftL #2, R1<br>AShiftR #1, R2<br>After the execution of the above three instructions<br>a. R1 = 1100 and R2 = 1110 | Question -3 on concept 4 | A | |

| | | | | |
|---|---|---|---|---|
| | b. R1 = 1100 and R2 = 1111<br>c. R1 = 1101 and R2 = 1110<br>d. None of the above | | | |
| | Two processor register R1 and R2 hold signed operand. If the binary value of the R1 is 1111 and R2 is 1111 then What will be the content of the register R1and R2 after the following instructions are executed. [Assume the Format of the instruction is **opcode source,source/Dst** and the size of each register is 4bit] [Assume the numbers are represented in 2's complement format]<br>ADD R1, R2<br>AShiftL #2, R1<br>AShiftR #1, R2<br>After the execution of the above three instructions<br>a. R1 = 1100 and R2 = 1111<br>b. R1 = 1100 and R2 = 1110<br>c. R1 and R2 result in overflow<br>d. None of the above | Question -4 on concept 4 | A | |
| Q. No :1(e) | Choose the correct Instruction that produces following control sequence in a 3-Bus Organization of the datapath inside a Processor.<br>1 PCout, R=B, MARin, Read<br>2 IncPC, MDRinE, WMFC<br>3 MDRoutB, R=B, IRin<br>4 Offset-field-of-IRout A, PCout, Add, PCin, End<br>A. Add R1, R2<br>B. Branch < 0 Label1<br>C. Jump L1<br>D. Add 20(R1), R2<br>E. None of the Above | Question -1 on concept 5 | C | |
| | Choose the correct Instruction that produces following control sequence in a 3-Bus Organization of the datapath inside a Processor.<br>1 PCout, R=B, MARin, Read<br>2 IncPC, MDRinE,WMFC<br>3 MDRoutB, R=B, IRin | Question -2 on concept 5 | C | |

| | | | | |
|---|---|---|---|---|
| | 4 Offset-field-of-IRout, R1out$_B$, SelectA, add, MARin, Read<br>5. WMFC<br>6. MDRout$_B$, R2out$_A$, SelectA, Mul, R2in, end<br>A. Mul R1, R2<br>B. Branch < 0 Label1<br>C. Mul 20(R1), R2<br>D. Jump L1<br>E. None of the Above | | | |
| | Which of the following is **NOT** the correct Sequence of Control Steps required to execute the following instruction in single bus organization?<br>Instruction: **ADD #10, (R2)** // 2nd operand is the destination<br>A.<br>1. R2out, MARin, Read<br>2. MDRinE, WMFC<br>3. MDRout, Yin<br>4. Offset_Field_Of_IRout, SelectY, ADD, Zin<br>5. R2out, MARin<br>6. Zout, MDRin, Write<br>7. WMFC<br>8. end<br>B.<br>1. R2out, MARin, Read<br>2. Offset_Field_Of_IRout, Yin, MDRinE, WMFC<br>3. MDRout, SelectY, ADD, Zin<br>4. R2out, MARin<br>5. Zout, MDRin, Write<br>6. WMFC<br>7. end<br>C.<br>1. R2out, MARin, Read<br>2. Offset_Field_Of_IRout, Yin, MDRinE, WMFC<br>3. MDRout, Yin, SelectY, ADD, Zin<br>4. R2out, MARin<br>5. Zout, MDRin, Write<br>6. WMFC<br>7. end<br>D.<br>1. R2out, MARin, Read<br>2. MDRinE, WMFC | Question -3 on concept 5 | C | |

| | | | | |
|---|---|---|---|---|
| | 3. Yin, MDRout<br>4. Offset_Field_Of_IRout, SelectY, ADD, Zin<br>5. R2out, MARin<br>6. Zout, MDRin, Write<br>7. WMFC<br>8. end<br>Answer: Option C | | | |
| | Which of the following is the correct Sequence of Control Steps required to execute the following instruction in single bus organization?<br>Instruction: **ADD #10, (R2)** // 2nd operand is the destination<br>A.<br>9. R2out, MARin, Read<br>10. Offset_Field_Of_IRout, Yin, MDRinE, WMFC<br>11. MDRout, SelectY, ADD, Zin<br>12. Zout, MDRin<br>13. R2out, MARin, Write<br>14. WMFC<br>15. end<br><br>B.<br>8. R2out, MARin, Read<br>9. Offset_Field_Of_IRout, Yin, MDRinE, WMFC<br>10. MDRout, SelectY, ADD, Zin<br>11. R2out, MARin<br>12. Zout, MDRin, Write<br>13. WMFC<br>14. end<br><br>C.<br>8. R2out, MARin, Read<br>9. Offset_Field_Of_IRout, Yin, MDRinE, WMFC<br>10. MDRout, Yin, SelectY, ADD, Zin<br>11. R2out, MARin<br>12. Zout, MDRin, Write<br>13. WMFC<br>14. end<br><br>D.<br>9. R2out, MARin, Read<br>10. MDRinE, WMFC<br>11. MDRout, Yin<br>12. Offset_Field_Of_IRout, ADD, Zin<br>13. R2out, MARin<br>14. Zout, MDRin, Write<br>15. WMFC<br>16. end | Question -4 on concept 5 | B | |

| | | | | |
|---|---|---|---|---|
| | Answer: Option B | | | |
| | | | | |
| | | | | |

SECTION-B(Answer Any One Question. Each Question carries 10 Marks)

Time: 30 Minutes (1×10=10 Marks)

| Question No | Question | CO Mapping |
|---|---|---|
| Q. No :2 | A. Write the equivalent assembly code for the given pseudo code and write the values of the variables (both in decimal and binary) after executing each instruction present in the equivalent assembly code. Assume X is the sum of the last 3 digits of your roll number and memory size of the operand is 1 byte. [Note: if the **Roll No = 20051123, then X =1+2+3=6**][Assume the number is represented in 2's complement format]<br><br>A = (X +5);<br>B = -(X +4);<br>C = X ;<br>A>>2; // Bitwise Right shift by 2bits<br>B<<1; // Bitwise left shift by 1 bit<br>Rotate_left(C, 2bit); // Rotate Left by 2 bits | |
| | | |

Representing the data in binary before and after = 4 marks
+ assembly code for shift and rotate 2 X3 =6 data

| | |
|---|---|
| *A* | *11* |
| *B* | *-10* |
| *C* | *6* |
| | |
| | |
| | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| *0* | *0* | *0* | *0* | *1* | *0* | *1* | *1* |

AShiftR A, 2 // before shift A=11
// After shift A =2

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| *0* | *0* | *0* | *0* | *0* | *0* | *1* | *0* |

AshiftL B,1 // before shift B= -10

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

// After Shift B= -20

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |

ROT L C,2 // before rotate C=6
//After rotate C=24

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

Q.3. A. Write the equivalent assembly code for the given pseudo code and write the values of the variables (both in decimal and binary) after executing each instruction present in the equivalent assembly code. Assume Y is the last digits of your roll number and memory size of the operand is 1 byte. [Note: if the **Roll No = 20051123, then Y =23**][Assume the number is represented in 2's complement format]

```
A = (Y +8);
B = -(Y + 3);
C = Y;
A<<1;          // Bitwise Right shift by 1bit
B<<2 ;           // Bitwise left shift by 2 bits
Rotate_right(C, 2bit)   // Rotate right by 2bits
}
```

Representing the data in binary before and after = 4 marks
+ assembly code for shift and rotate 2 X3 =6 data

| | |
|---|---|
| A | 31 |
| B | -26 |
| C | 23 |
| | |
| | |
| | |

AShiftR A, 1 // before shift A=31

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

//After shift A =15

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

AshiftL B,2 // before shift B= -26

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

// After Shift B= -104

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

ROT R C,2 // before rotate C=23
//After rotate C=-59

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

Q.4. A. Represent **-w** in little endian and big endian format starting at address 5000. The machine is byte addressable and each word consists of 2 bytes. Where w= last 4 digits of your roll no. [Note: if the **Roll No = 20051123, then w=1123**]

B. A processor has 32 integer registers and and 16 floating point registers. It uses 2-byte instruction format. It has two types of instructions: Imm-type and REG-type. Each Imm-type instruction contains an opcode, an integer register name, and a 4-bit immediate value. Each REG-type instruction contains an opcode, 2 floating point register and one integer register names. If there are 16 distinct Imm-type opcodes, then what is the maximum number of distinct REG-type opcodes is possible ?

C. Explain Call and Compare instruction

**ANS:**

**[2+2]**

Let ROLL NO=20051123

W=1123 -w=-1123

$(1123)_{10}=(0000\ 0010\ 0110\ 0011)_2$

$(-1123)_{10}=(1111\ 1101\ 1001\ 1101)_2=(FD9D)_{16}$

**Big endian**:

| **ADDRESS** | **VALUE** | **VALUE** |
|---|---|---|
| **5000** | **FD** | **9D** |
| **5002** | | |

**Little endian:**

| **ADDRESS** | **VALUE** | **VALUE** |
|---|---|---|
| **5000** | **9D** | **FD** |
| **5002** | | |

**QB**.A processor has 32 integer registers and and 16 floating point registers. It uses 2-byte instruction format. It has two types of instructions: Imm-type and REG-type. Each Imm-type instruction contains an opcode, an integer register name, and a 4-bit immediate value. Each REG-type instruction contains an opcode, 2 floating point register and one integer register names. If there are 16 distinct Imm-type opcodes, then what is the maximum number of distinct REG-type opcodes is possible ?

**ANS**:

**[4]**

Length of instruction=2byte=16 bits

No of integer registers=32

No of floating point register=16

No of Imm-type instruction=16

Format of Imm-type instruction

| Opcode(7) | I.R(5) | Imm value(4) |
|---|---|---|

Format of REG-type instruction

| Opcode(3) | F.R(4) | F.R(4) | I.R(5) |
|---|---|---|---|

Maximum no of instruction=$2^{16}$

No of REG-type instruction=x

$(16*2^5*2^4)+(x*2^4*2^4*2^5)=2^{16}$

**So x=7(maximum number of distinct REG-type opcode)**

**QC**.Explain Call and Compare instruction

**ANS:**

**[1+1]**

**Compare**:program control instruction.

**CMP dst,src**

Performs the operation

[dest]-[src] and sets the condition code flags based on result

obtained.Neither operand is changed nor the result is stored anywhere.

**Call**:program control instruction.

**CALL SUBROUTINE**

It firsts pushes the return address(Updated value of PC) on to the stack and then branches to SUBROUTINE.

Stack[--top]=[PC]

PC=ADDRESS of the subroutine

Q.5. A. CPU has only three instructions I1, I2 and I3, as follows:

I1: AND R1, R2

I2: Branch=0 LOOP1

I3: Move R7, A

Write the logic function and draw the circuit for generating the End and MARin signal for single bus CPU organization. Assume 2nd operand is the destination?

Solution:

I1: AND R1, R2

1. PCout, MARin,Read,Select Y,Add, Zin
2. Zout, PCin, Yin,WMFC
3. MDRout,IRin
4. R1out, Yin
5. R2out, Select Y, AND, Zin
6. Zout, R2in, End

I2: Branch=0 test

1. PCout, MARin,Read,Select Y,Add, Zin
2. Zout, PCin, Yin,WMFC
3. MDRout,IRin
4. Offset_field_IRout, Select Y, Add, Zin,If Z=0, Then End
5. Zout, PCin, End

I3: Move R7, A

1. PCout, MARin, Read, Select Y, Add, Zin
2. Zout, PCin, Yin,WMFC
3. MDRout, IRin
4. Address_field_of_IRout, MARin
5. R7out, MDRin, Write
6. WMFC
7. End

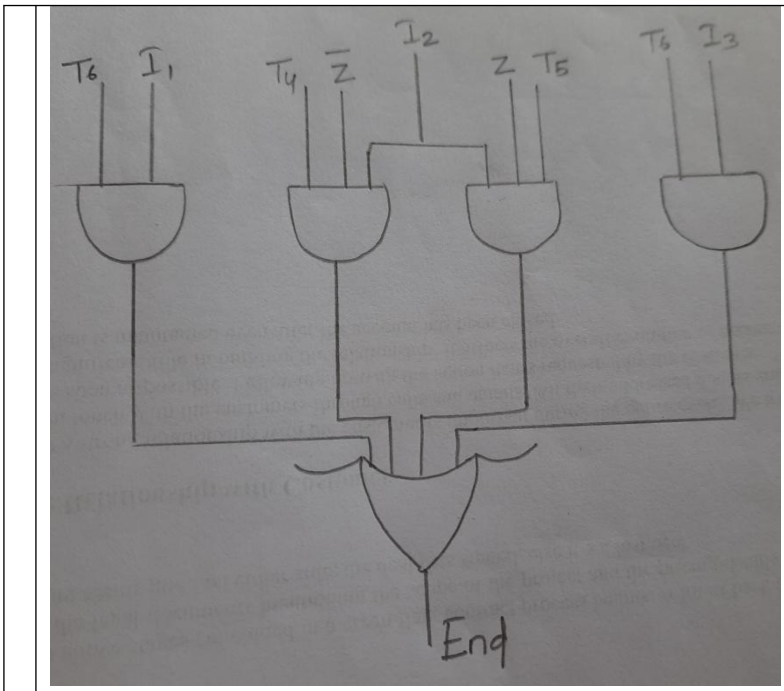
Logic function :

$End= T6.I1 \overline{+} (T4 . Z + T5 . Z) I2 + T7.I3$

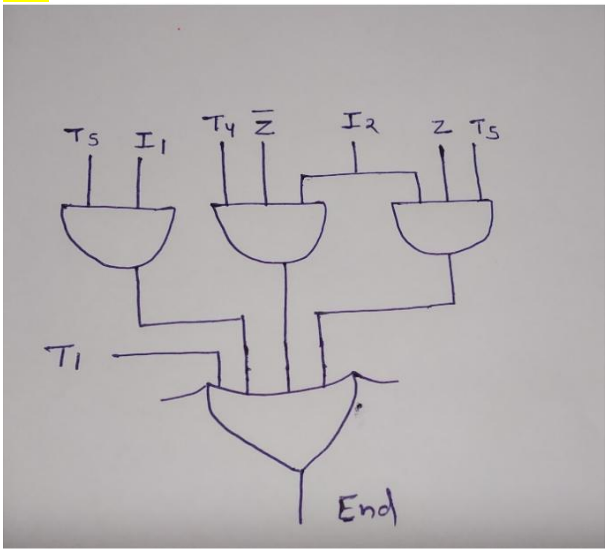
$Zin= T1 + T\overline{5}.I1+I2(T4 . Z + T5 . Z)$

Circuit diagram:

End



Zin



Q.6. A.Write the sequence of control steps for the given instructions and design the logic function for control signal with reference to given instructions. Using Single-Bus CPU Organization. [Assume the length of each instruction is 1 word, 1word= 4bytes, machine is byte addressable. Assume $2^{nd}$ operand is the destination.

i) ADD 25(R2), R1
ii) LOAD (R2), R1
iii) MUL –(R1), R2

B. “Hardwired control unit is faster compared to microprogrammed control unit” - Justify the statement. Explain the working principle of microprogrammed control unit design with proper block diagram.

a)

I1: ADD 25(R2), R1

Ans:

1. $PC_{out}$, $MAR_{in}$, Read, Select 4, Add, $Z_{in}$
2. $Z_{out}$, $PC_{in,}$ $Y_{in}$, WMFC
3. $MDR_{out}$, $IR_{in}$
4. Offset field of $IR_{out}$, $Y_{in}$
5. $R_{2out}$, Select Y, Add, $Z_{in}$
6. $Z_{out}$, $MAR_{in}$, Read
7. $R_{1out}$, $Y_{in}$, WMFC
8. $MDR_{out}$, Select Y, Add, $Z_{in}$
9. $Z_{out}$, $R_{1in}$, end

I2: LOAD (R2), R1

Ans:

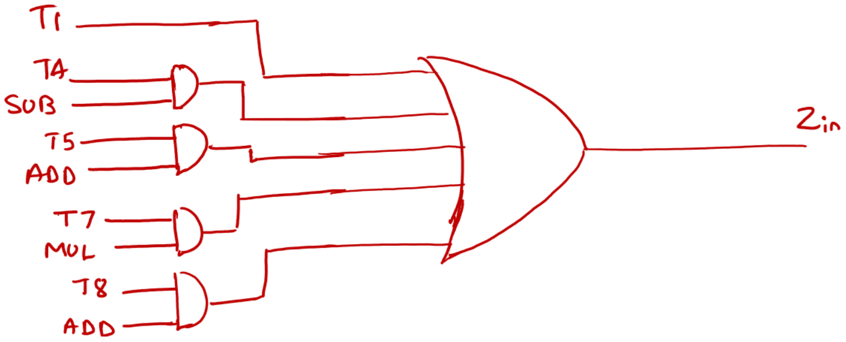
1. $PC_{out}$, $MAR_{in}$, Read, Select 4, Add, $Z_{in}$
2. $Z_{out}$, $PC_{in,}$ $Y_{in}$, WMFC
3. $MDR_{out}$, $IR_{in}$
4. $R_{2out}$, $MAR_{in}$, Read
5. WMFC
6. $MDR_{out}$, $R_{1in}$

I3: MUL -(R1), R2

Ans:

1. $PC_{out}$, $MAR_{in}$, Read, Select 4, Add, $Z_{in}$
2. $Z_{out}$, $PC_{in}$, $Y_{in}$, WMFC
3. $MDR_{out}$, $IR_{in}$
4. $R_{1out}$, Select 4, SUB, $Z_{in}$
5. $Z_{out}$, $R_{1in}$, $MAR_{in}$, Read
6. $R_{2out}$, $Y_{in}$, WMFC
7. $MDR_{out}$, Select Y, MUL, $Z_{in}$
8. $Z_{out}$, $R_{2in}$, end

$Z_{in}$= T1+Add*T5+ADD*T8 + MUL*T4+MUL*T7



b)

In Hardwired control, the control signals are generated by hardware like combinational circuits which give faster control signals than the program to generate the same control signals.

**Answer:**

Refer page no.431-32 of CO Text Book by Carl Hammacher, 5th ed.

Q.7. A. "Hardwired control unit is faster compared to microprogrammed control unit" - Justify the statement. Explain the working principle of hardwired control unit design with proper block diagram.

B. Write the control sequence for the following instructions in a Multiple Bus CPU Organization. Assume R3 is the destination operand.

ADD 50(R1), R2, R3

.

**A. "Hardwired control unit is faster compared to microprogrammed control unit" - Justify the statement. Explain the working principle of hardwired control unit design with proper block diagram.**

**Answer:**

Refer page no.426-327 of CO Text Book by Carl Hammacher, 5th ed.

In Hardwired control, the control signals are generated by hardware like combinational circuits which give faster control signals than the program to generate the same control signals.

**B. Write the control sequence for the following instructions in a Multiple Bus CPU Organization. Assume R3 is the destination operand.**

**ADD 50(R1), R2, R3**

**Ans ::**

1. PCout, MARin, R=B, Read, InPC
2. MDRin, WMFC
3. MDRout, R=B, IRin
4. Offset_field_of_IRoutA, SelectA, R1outB, Add, MARin, Read
5. MDR$_{\text{inE}}$, WMFC
6. R2outA, MDRoutB, Select A, Add, R3in, End

**Controller of Examinations**