SCHOOL OF COMPUTER ENGINEERING

KIIT, DEEMED TO BE UNIVERSITY

COMPUTER ORGANIZATION & ARCHITECTURE(COA) QUESTION BANK

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(4TH SEMESTER IT-6 STUDENTS)

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Module-1 Basic Structure of Computer

1.	Define Computer architecture and computer organization. Justify whether a common instruction set supports different architecture.
2.	Discuss different functional units of a digital computer system with its block diagram
3.	Von-Neumann Architecture v/s Harvard Architecture.
4.	Compare Von-Neumann architecture with Havard architecture.
5.	Justify whether present day computers are the combination of both Havard and Von-neumann concept or not.
6.	PC does the same function as MAR, and then justify your answer by keeping two registers instead of one.
7.	A processor is connected to a 128G X 32 memory module. What is the width of its MAR and MDR register?
8.	What is the function of following registers: MAR, IR, PC, Y.
9.	A processor is connected to 256G X 32 memory module. What is the size of MAR and MDR registers?
10.	At the end of a memory read operation, the MDR is loaded with a binary combination, how that combination is interpreted as an instruction or an operand to an instruction?
11.	An instruction is a 24 bit instruction. It is a byte addressable memory. The PC contains 300. Which one of the following is a legal PC value: (a) 400 (b) 500 (c) 600 (d) 700
12.	How the processor does execute an instruction? Explain with suitable example and neat diagram.
13.	Explain the basic operational concept involved in the execution of an instruction with an example
14.	An instruction takes 9 clock cycles to execute it on a 1.5GHz processor. How much time is taken by the instruction to complete its execution?
15.	One instruction requires 7 clock cycle to complete its execution. How much time is required for that instruction if the processor speed is 5 GHz?
16.	Discuss the factors that affect the performance of the computer. If a 8GHz computer takes 7 clock cycles for ALU instructions, 11 clock cycles for branch instructions and 6 clock cycles for data transfer instructions. Then Find the total time taken by the computer to execute the program that consists of 10 ALU instructions, 5 branch instructions and 5 data transfer instructions
17.	Let a processor operates by a frequency 10MHtz and it executes a typical program in which 50% are register referenced instruction,30% are memory reference instructions and 20% are branch instructions. Register referenced instruction , memory reference instructions and branch instructions take 4, 8 and 6 clock cycles respectively. then find out the total time taken by the processor to execute the program.

Module-2 Machine Instructions & Program

18.	Differentiate between the little endian and the big endian address assignment schemes.
19.	Differentiate between byte addressable and word addressable.
20.	Consider a computer that has a byte addressable memory organized in 32 bit words according to big endian scheme. A program reads ASCII characters entered at a keyboard and stores them in successive byte locations, starting at location 1000. Show the content of two memory words at location 1000 and 1004 after the name "Johnson" has been entered.
21.	Suggest the layout of an instruction. And thus write different types of instruction according to the appearance of number of address, with the advantages , disadvantages and one example.
	Write a program to evaluate the arithmetic statement: X = (A-B+C*(D*E-F)) / (G+H*K) i) Using a stack organized computer with zero-address operation instructions. ii) Using an accumulator type computer with one address instructions. iii) Using a general register computer with two address instructions
22.	Write the assembly code to evaluate the following arithmetic expression: Z = (A - B + C) * (D / E * F) / G i) Using an accumulator type computer with one address instructions. ii) Using a stack organized computer with zero-address operation instructions. iii) Using RISC computer instruction format.
23.	Write a program that can evaluate the following expression in single accumulator processor and stack based computer.(A*B)+(C*D).
24.	Describe briefly about three, two and one address instruction format. Evaluate the explain E = (A+B) * C/E using the above three format.
25.	Write a program to evaluate the given arithmetic expression :- Z = (R + P) * E + K * B - L / G - S i) Using a general register computer with two address and three address instructions. ii) Using an accumulator type computer with one address instructions. iii) Using a stack organized computer with zero-address operation instructions. iv) Using RISC computer instruction format.
26.	Differentiate between byte addressable and word addressable.

27.	Write the equivalent instructions for Zero Address Organization and One Address Organization of the following instructions:
	MOV P, R_1
	SUB Q, R_1
	DIV R, R_1
	MUL S, R_1
	MOV R_1, X

28.	Write the assembly language code segment to evaluate the following arithmetic expression X= (A+B)*C)/(D—E*F+G) Using Stack based organization, RISC organization
29.	Write down the sequence of instructions for the execution of the following statement: X = (A-B)*(C+D) Using a. Zero addresses instruction b. One address instructions c. Two address instructions d. Three address instructions
30.	Find the length of the ALU instructions, if one addressing mode, 70 operation codes and 1K memory and 3-address instructions is used in an ISA
31.	A computer has 64-bit instructions and 12 bit addresses. If there are 352 three-address instructions, and 2256 no of two-address instructions then how many one-address instructions can be formulated?
32.	A computer has 64 bit instruction and 12 bit address. If there are 250 three address instruction and 525 two address instruction, how many one address instructions are possible?
33.	A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. How many bits are there in the operation code, the register code part, and the address part?
34.	A general purpose register organization computer has a 16 bit instruction consisting of opcode, source register and a destination register. It supports 7 no of arithmetic operations and 6 no of logical operations. Find the total number of maximum registers present in the system.
35.	A two-word instruction is stored in memory at an address designated by the symbol P. The address field of the instruction (stored at P+1) is designated by the symbol Q. The operand used during the execution of the instruction is stored at an address symbolized by EA. An index register contains the value X. State how EA is calculated from the other addresses if the addressing mode of the instruction is direct, indirect, relative, and indexed.
36.	A machine has a 32-bit architecture, with 1-word long instructions. It has 60 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, what is the maximum value of the immediate operand?
37.	What is A two-word instruction is stored in a location A. The operand part of instruction holds B. If the addressing mode is relative, the operand is available in which location?

38.	An instruction is stored at location 1000 with its address field at location 1001; the address field has value 500. A processor register R1 contains the number 100. Evaluate the effective address of following addressing modes I. Register Indirect Addressing Mode II. Relative Addressing mode III. Index (R1 as index register) Addressing Mode
39.	Register R_1 and R_2 of a computer contain the decimal value 1540 and 1290.What is the effective address of the memory operand in each of the following instructions? 1. LOAD 18(R_1),R_5 2. STORE R_5,25(R_1,R_2) 3. ADD -(R_1),R_3 4. SUB (R_2)+,R_5 5. MOV #1235,R_3
40.	Write the number of memory references required for executing the following instructions: i) ADD R1,(R2)+ ii) SUB #10,R2 iii) MOV R1, 20(R3,R4) iv) AND R1,R2 v) Increment A
41.	How many memory references are required for fetching and executing the following instructions: 1.MUL #100,80(R_1) 2.ADD(R_2)+,R_1
42.	Registers R_1 and R_2 of a computer contains the decimal value 1100 and 500. What is the effective address of the memory operand in each of the following instruction? i) Load 20(R_1),R_5 ii) Move 300,R_5 iii) Store R_5, 50(R_1,R_2) iv) Subtract (R_i) +, R_5

43.	An instruction is stored at location 600 with its address field at location 601. The address field has the value 200. A processor register R1 contains the number 300. Evaluate the effective address if the addressing mode of the instruction is direct, immediate, relative, register indirect, and index with R1 as the index register.
44.	The memory unit of a computer has 256K words of 32bits each. The computer has an instruction with four fields: an operation code field, a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the number of bits in each field, if an instruction is stored in one memory word.
45.	An instruction is stored at location 500 with its address field at location 501. The address field contains the value 80. The contents of a processor register R1 and an Index Register XR are 501 and 321 respectively. Determine the effective address and data operand (if any), if the addressing mode of the instruction is☹i) Direct (ii) Immediate (iii) Register indirect(iv)Relative (v) Index
46.	Match each of the high level language statements given on the left hand side with the most natural addressing mode from those listed on the right hand side. 1. A[1] = B[J]; a) Indirect addressing 2. while [*A++]; b) Indexed, addressing 3. int temp = *x; c) Autoincrement
47.	Match columns: A — B Indirect — Relocatable code Index — Passing array as a parameter Base Register — Array Auto increment — while (*A++)
48.	How many memory references are required for fetching and executing each of the following instructions? [Here the 2nd operand is the destination.](a) ADD NUM, R2 (b) SUB –(RI), R2
49.	How many memory references are required for fetching and executing each of the following instructions? **(a)** ADD 50(R1),R**2** (b) SUB (R1)+R2
50.	A relative mode branch type instruction is stored in memory at an address 750. The branch is made to an address 500. What should be the value of the relative address field of the instruction?
51.	A program is required for the task C[]=A[]x B[]] Write a program for this task on a computer that supports one address instructions. Assume that C,A[i]and B[i] are located in main memory and the value n is stored in main memory location **N.**
52.	Explain the following addressing mode with suitable example. Relative Auto increment and decrement Register indirect Index addressing mode

53.	Write the use of indexed and relative addressing mode.
54.	Define how index addressing mode is different from base addressing mode
55.	How many memory references are required to execute the following instruction? (i)ADD (R1),R2, R3 where R3 is the destination (ii)SUB 600, R5where R5 is destination
56.	What are addressing modes? Explain different types of addressing modes with suitable example**.**
57.	Suggest different data references to be used in an instruction. And hence write the advantages of each with example.
58.	Discuss different types of instructions with examples. Find out the length of data transfer instructions where operation codes are LOAD and STORE data is temporarily staying in the accumulator and the memory
59.	Both of the following statements cause the value 150 to be stored in location 2000 ORIGIN 2000 DATAWORD 150 And Move #150,2000 Explain the difference.
60.	Consider the following program segment. Here R1, R2 and R3 are the general purpose registers. Instruction — Operation MOV R1, (3000) — R1←M[3000] LOOP: MOV R2, (R3) — R2←M[R3] ADD R2, R1 — R2←R1+R2 MOV (R3), R2 — M[R3] ←R2 INC R3 — R3←R3+1 DEC R1 — R1←R1-1 BNZ LOOP — Branch on not zero HALT — Stop Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal. Assume that the memory is word addressable. How many number of memory references for accessing the data in executing the program completely?
61.	Explain the significant of carry and overflow flag
62.	Write short notes on Condition Codes

63.	The content of register R1is 11010101. What will be the decimal value after execution of AshiftR #2, R1. [Assume the number is represented in 2's complement format]
64.	The content of register R1is 11010110. What will be the decimal value after execution of RotateL #2, R1. [Assume the number is represented in 2's complement format]
65.	The content of a register R_1 is10001010.What will be the decimal value in R_1 after the execution of ASHR #1,R_1 (Assume the numbers are written in 2's complement form)
66.	Execute the following instruction where Ro is of 8 bit and its content is 11001011. i) Lshift L #2, Ro ii) Ashift R #1, Ro
67.	Perform the logical left shift operation by 2 bit on the following data. R1= 1000110000110011 R2= 1000100001110011
68.	Explain the following instructions with example. XOR, Rotate, Compare, and Shift
69.	Explain the following instructions with example AND, AshiftR, Compare, Negate, and Branch.
70.	Give two examples from each of the following type of computer instructions, explaining their functions :- [i] Data Transfer Operation [ii] Logical Shift Operation [iii] Program Control Operation
71.	The content of the top of memory stack is 2452.The content of SP is 1258.A two byte call subroutine instruction is located in memory address 1456 followed by address field of 5490 at location 1457.What are the content of PC , SP and top of stack; 1.Before call instruction execution 2.After call instruction execution 3.After return from subroutine
72.	The content of the top of the memory stack is 5000. The content of the stack pointer SP is 3000. Assume you want to organize a nested subroutine calls on a computer as follows: the routine Main calls a subroutine SUB1 by executing a two-word call subroutine instruction located in memory at address 1000 followed by the address field of 6000 at location 1001.Again subroutine SUB1 calls another subroutine SUB2 by executing a two-word call subroutine instruction located in memory at address 6050 followed by the address field of 8000 at location 6051 . What are the content of PC, SP, and the top of the stack? i) After the subroutine call instruction is executed in the main routine? ii) After the subroutine call instruction is executed in the subroutine SUB1? iii) After the return from SUB2 subroutine?

73.	How many times a subroutine should be called so that the stack becomes full, Assume that the stack address space ranges from 2000 to 1600 and each stack word consumes 4 bytes and machine is byte addressable.[Note: No parameter, return value, registers, local variables are stored in the stack due to subroutine call]
74.	Given the following program fragment Main Program First Subroutine SUB1 Second Subroutine SUB2 2000 ADD R1, R2 3000 MOV R1,R2 4000 SUB R6, R1 2004 XOR R3, R4 3004 ADD R5, R1 4008 XOR R1, R5 2008 CALL SUB1 3008 CALL SUB2 4012 RETURN 1012 SUB R4, R5 3012 RETURN Initially the stack pointer SP contains 5000. What are the content of PC, SP, and the top of the stack? i) After the subroutine call instruction is executed in the main program? ii) After the subroutine call instruction is executed in the subroutine SUB1? iii) After the return from SUB2 subroutine?
75.	Which of the following IA-32 instructions would cause the assembler to issue a syntax error message and why? i. ADD EAX, EAX ii. SUB EAX, [EBX+ESI*10] iii. SUB EAX, [EBX+ESI*4+20] **iv.** MOV EAX,[EBP+ESP*4]
76.	Explain the following addressing modes of IA-32 with example I. Index with displacement mode II. Base with index mode **III.** Base with index and displacement mode
77.	What do you mean by Instruction set completeness?
78.	. RISC v/s CISC
79.	Discuss the register organization of IA-32.
80.	Discuss all addressing modes of IA-32.
81.	Discuss different types of instructions with respect to the operations performed.

Module-3 Basic Processing Unit

82.	Draw the schematic diagram of the architecture of a single bus CPU, clearly showing the general purpose, Special purpose registers and the data path. Explain the function of each component.
83.	Write the sequence of control steps required for single bus CPU organization of the following instruction ADD R1, NUM Write the sequence of control steps required for three bus CPU organizations for the above instruction Design the logic function for WMFC control signal using single bus CPU organization**.**
84.	Write micro routine for single bus 10rganization to execute thefollowing instructions: i) ADD (R1)+, R2 ii)SUB RI, 40
85.	Write the sequence of control steps for the following instructions for single bus CPU organization. Assume second operand is the destination operand MUL R1, (R2)
86.	Write the Micro routine for the instruction ADD mem1, R1, R2 where the content of R1 and R2 will be added and stored in mem1 in the above CPU
87.	Write the sequence of control steps for the following instructions for single bus CPU organization. Assume second operand is the destination operand. a) MUL #12, (R1) b)DIV -(R1), R2
88.	Write the sequence of control steps for the following instruction for multi bus CPU organization ADD (R1), R2 // R2←[R1]+R2
89.	Explain the 3-bus architecture inside CPU with suitable example. Write the control sgnals for the following instructions. MUL(R1),#15
90.	Write whether the CPU single bus connectivity supports pipelining or not.
91.	Write the sequence of control steps for the following instructions for single bus CPU organization Add (R3), R1.The processor is driven by a continuously running clock, such that each control step is 2 ns in duration. How long will the processor have to wait in step2 and 5, assuming that a memory read operation takes 16ns to complete? What percentage of time is the processor idle during execution of this instruction?
92.	Draw the CPU 3-bus 10rganization and explain the diagram with it's advantage and disadvantage.
93.	Why constant 4 in MUX is still present in three bus architecture though incrementor is there?
94.	Discuss multi bus organization of a data path inside a processor with the help of a block diagram. Write down the control sequence of the instruction ADD (R1), R.7, R3 in three-bus organization, where (R1), R, are used as source operand and R3 is used as destination operand.

95. Explain multibus organization inside CPU with its advantages over single bus organization and write the control signal for the following instruction execution in multibus organization. MUL 3 0(R_1), R_2 where R_2 is the destination

96. Write the advantage and limitation of Hard wired based control unit.

97. Explain the working principle of Hardwired control unit design along with neat diagram. Explain its advantages and disadvantages

98. A hardwired CPU uses 10 control signals S1 to S10, in various time steps T1 to T5, to implement 4 instructions I1to I4 as shown below:

	T1	T2	T3	T4	T5
I1	S1, S3, S5	S2, S4, S6	S1, S7	S10	S3,S8
I2	S1, S3, S5	S8,S9, S10	S5, S6, S7	S6	S10
I3	S1, S3, S5	S7, S8,S10	S2, S6, S9	S10	S1, S3
I4	S1, S3, S5	S2, S6, S7	S5, S10	S6, S9	S10

Write the expressions to represent the circuit for generating control signals S5 and S10respectively? What will be the specification of step decoder and instruction decoder in the hardwired control unit?

99. Write the micro routine for the following instruction:
ADD (R1)+ , R2

100. A computer has 58 instructions; each instruction requires at most 15 steps to complete its execution. What will be the specification of instruction and step counter decoder used in hardware control unit design?

101. A Computer has 70 instructions. For executing each instruction maximum steps required are 18. What will be the specification of instruction and step counter decoder used in hardwired control unit design?

102. Explain the 3-bus architecture inside CPU with suitable example. Write the control signals for the following instructions. MUL30(R,),R5.

103. Draw and explain the 3-bus CPU organization.Write the sequence of control signals to execute the following instruction using the same organization.
ADD (R5),R1,R2

104. A CPU has only three instructions I1, I2 and I3, which use the following signals in time steps T1-T5:

I1:	I2:	I3:
T1:A_{in},B_{out},Cin	T1:C_{in},B_{out},D_{in}	T1:D_{in},A_{out}
T2:PC_{out},B_{in}	T2:A_{out},B_{in}	T2:A_{in},B_{out}
T3:Z_{out},A_{in}	T3:Z_{out},A_{in}	T3:Z_{out},A_{in}
T4:B_{in},C_{out}	T4:B_{in},C_{out}	T4:D_{out},A_{in}
T5:End	T5:End	T5:End

Write the logic function for generating the signal A_{in}?

105.	Hardwired Control Unit is relatively inflexible"-Justify the statement
106.	Specify the importance of RUN and END control signal in hardwired control unit.
107.	Write the sequence of control steps for the following instructions for single bus CPU organization I. I1: ADD 10(R3), R4 II. I2: Branch<0 L1 III. I3: MUL -(R5), R5 **IV.** Design the logic function for WMFC control signal with reference to the above instructions i.e. I1 to I3.
108.	Justify whether control signal flows through the same bus where the data, address, instruction flow or not.
109.	Differentiate between micro program counter and program counter.
110.	Draw and explain the working principle of microprogrammed control unit.
111.	Write the function of control unit. Explain the following terms related to micro-programmed control unit design: (i) Micro program counter (ii) Micro Routine (iii) Micro Instruction (iv) Control Store
112.	Describe the operational principle of Hardware control unit and micro-programmed control unit with the help of proper diagram. What are the advantage and disadvantage of both the control unit?
113.	Explain the working principle of micro-programmed control [4 unit with suitable diagram. Explain how is it different from hardwired control unit
114.	Differentiate between horizontal and vertical micro instruction with example.

Module-4 Arithmetic & Logic Unit

115.	Why 2's complement number representation is better than **1** 's complement?
116.	How overflow condition is detected during binary addition?
117.	Discuss the following types of adders : n bit ripple carry adder and cascade of k n-bit ripple carry adder.
118.	Explain a binary addition subtraction logic network.
119.	Write the limitation of general multiplication process over Booth's.
120.	Write the steps for multiplication according to Booth and explain with the example to multiply 9 with -*4*.
121.	Multiply (15 X —7) using Booth Algorithm.
122.	Divide 11 ÷ 3 using restoring and non-restoring division algorithm. Give the flow table of division.
123.	Divide the following using Non-restoring division algorithm. 14 ÷ 5
124.	Multiply the -7×-3 using booth's multiplication algorithm.
125.	Divide the following using restoring and non-restoring method. 13 ÷ 4
126.	How the floating point numbers are normalized using IEEE standard
127.	Write the floating point presentation in memory according to IEEE standard with diagram
128.	Write the IEEE 754 format for representing floating point numbers in single precision and double precision format. Represent the decimal number 10.25 using IEEE 754 single precision floating point format.
129.	Represent 9.25 in IEEE single precision format.
130.	Express the decimal value 10.25 as IEEE single precision formal

Module-5 Memory Organization

131.	Differentiate between DRAM and SRAM
132.	Explain the working principle of DRAM chip
133.	Write down the working principle of SRAM cell.
134.	Design a 4M X 32 bits memory using 512X8 bits memory chip.
135.	How many external connections are required to design 32mX32 memory chip?
136.	A computer employs RAM chips of 256X **8** and ROM chips of 1024X8. The computer system needs 2K bytes of RAM and 4K bytes of ROM. DesigN the memory module of above configuration and interface with CPU.
137.	What is the difference between memory access time and memory cycle time?
138.	How many 64 X 8 RAM chips are needed to provide a memory capacity of 2048 bytes
139.	A computer uses RAM chips of 256X4 capacity. Design a memory capacity of 1KB by using available chip.
140.	How many separate address and data lines are needed in a 8Kx 16 memory?
141.	How many 128X8 RAM chips are needed to provide a memory capacity of 2048 bytes? Give the specifications with suitable diagram.
142.	Discuss Memory Hierarchy and Locality-of-reference
143.	What is the need of locality of reference? Explain about the different types of locality of references
144.	Write different mapping techniques in cache with their merits and demerits.
145.	A cache consists of a total of 128 blocks. The main memory contains 2K blocks, each consisting of 32 words. (I)How many bits are there in each of the TAG, BLOCK and WORD field in case of direct mapping? (ii)How many bits are there in each of the TAG, SET, and WORD field in case of 4-way set-associative mapping?
146.	Define the role of cache memory in memory organisation. Why we use the mapping function? Specify the different mapping function name.
147.	Specify the use of tag bit in memory mapping function

148.	A two-way set associative cache memory uses block of 4 words. The cache can have a total of 2048 words from main memory. The main memory size is 128K X 32. i)Draw the format of main memory address. ii)What is the size of cache with tag bits
149.	Explain the importance of valid bit associated with cache memory
150.	Differentiate between the valid bit and the dirty bit.
151.	What is difference between write-through and write-back protocol?
152.	Justify whether write through approach is better than write back approach.
153.	Differentiate between load through and load back policy
154.	Calculate the number of hits and misses in a 4-blocked cache for the LRU and FIFO policy if the sequence of block reference by CPU is given like; 2, 2, 3, **4,** 2, 5, 6, 4, 7, 5.
155.	Implement the LRU algorithm on the following data. Assume cache size is 3 block. 1,1,2,3,3,4,5,1,2,5
156.	Find out the number of page fault in the following strings of pages used by CPU using the page replacement algorithm LRU and LIFO [taking 3 page frames] 1,1,3,5,3,4,2,2,2,1,8
157.	Find the avg. cache access time if the hit ratio is 60%, one cache access time is 2ns and miss penalty is 10ns
158.	Can it be possible to have 100% hit in a cache, justify your answer
159.	What are the write policies of cache memory? Explain. In a cache organization if the cache memory has an access time of 8nsec and hit rate as 0.98, then find out Average Memory Access time (AMAT) for the whole arrangement. Assume the access time for the main memory is 1 .0 msec.
160.	What is the hit ratio of a cache memory if cache memory access time is 30ns, main memory access time is 150ns and average access time is 42ns.
161.	What is the hit ratio of a cache memory if cache memory access time is 30ns and main memory access time is 15ns and average access time is 42ns?
162.	Define different types of memory interleaving technique and its use.
163.	Find the block transfer time of one interleaved memory where the modules are divided to accommodate even and odd numbered wods of blocks, each block contains 4 words, the address transfer time is 2ns, 1st word access time is 4ns, consecutive word access time is 3ns and data transfer time is 1ns. Explain the answer with the diagram of the above interleaved memory

164.	Explain the technique of memory interleaving. Consider a memory of 8 words per block. If 2 clock cycle are required to transfer address from CPU to main memory and 6 clock cycle to access the 1st word and 3 clock cycle each for consecutive words and 2 clock cycle for transferring the word from memory to cache. Then calculate the total clock cycle required to transfer the block with inter leaving and without interleaving ifthe number of module is four
165.	Why is memory interleaving technique used? Consider a -memory of 8 words per block. If two clock cycle are required to transfer address from CPU to main memory, six clock cycle to access the first word, three clock cycles each for the word from memory to cache. Then calculate the total clock cycles required to transfer the block with interleaving and without interleaving if number of modules are four.
166.	What is virtual memory ? Discuss the virtual memory organization.
167.	Illustrate the address translation mechanism in virtual memory. Explain the role of TLB.
168.	The size of virtual memory is 256G Bytes and the physical memory is 4G Bytes. The page size is 8M Bytes. What would be the size of page table assuming 6 bits are used as control bits in the page table

Module-6 I/O Organization

169.	List the function of I/O interface
170.	Memory mapped I/O VS I/O mapped I/O
171.	State how isolated I/O is different from memory mapped I/O.
172.	Explain Program-Controlled I/O technique. Why interrupt driven I/o is more advantageous over it?
173.	How does the processor resolvs among simultaneous interrupt requests?
174.	What is the vectored interrupt technique of performing I/O operation?
175.	Write different types of I/O data transfer with it's advantage and disadvantage
176.	Explain Direct Memory Access method with it's requirement
177.	Distinguish between cycle stealing and burst mode data transfer in DMA
178.	State and explain the Flynn's classification of computer with proper diagram.

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