| Instruction | Opcode (Binary) | Funct3 | Funct7 |
| --- | --- | --- | --- |
| addi | 0010011 | 000 | XXXXXXX |
| add | 0110011 | 000 | 0000000 |
| and | 0110011 | 111 | 0000000 |
| andi | 0010011 | 111 | XXXXXXX |
| lui | 0110111 | XXX | XXXXXXX |
| lw | 0000011 | 010 | XXXXXXX |
| xor | 0110011 | 100 | 0000000 |
| xori | 0010011 | 100 | XXXXXXX |
| or | 0110011 | 110 | 0000000 |
| ori | 0010011 | 110 | XXXXXXX |
| slt | 0110011 | 010 | 0000000 |
| slti | 0010011 | 010 | XXXXXXX |
| sltiu | 0010011 | 011 | XXXXXXX |
| sll | 0110011 | 001 | 0000000 |
| srl | 0110011 | 101 | 0000000 |
| sra | 0110011 | 101 | 0100000 |
| sw | 0100011 | 010 | XXXXXXX |
| sub | 0110011 | 000 | 0100000 |
| beq | 1100011 | 000 | XXXXXXX |
| bne | 1100011 | 001 | XXXXXXX |
| blt | 1100011 | 100 | XXXXXXX |
| bge | 1100011 | 101 | XXXXXXX |
| bltu | 1100011 | 100 | XXXXXXX |
| bgeu | 1100011 | 111 | XXXXXXX |
| jal | 1101111 | XXX | XXXXXXX |
| jalr | 1100111 | 000 | XXXXXXX |
| lb | 0000011 | 000 | XXXXXXX |
| lh | 0000011 | 001 | XXXXXXX |
| lbu | 0000011 | 100 | XXXXXXX |
| lhu | 0000011 | 101 | XXXXXXX |
| slli | 0110011 | 001 | 0000000 |
| srli | 0010011 | 101 | 0000000 |
| srai | 0010011 | 101 | 0100000 |
| auipc | 0010111 | XXX | XXXXXXX |
| wfi | | 000 | 0000000 |

ALUSrc (1 bit)

1
0
0
1
1
1
1
1
1
1
0
1
1
0
0
0
1
0
0
0
0
0
0
0
X
1
1
1
1
1
1
1
1
X
0

| ALUControl (4 bit) |
| --- |
| 0011 |
| 0011 |
| 0000 |
| 0000 |
| 1000 |
| 0011 |
| 0010 |
| 0010 |
| 0001 |
| 0001 |
| 0100 |
| 0100 |
| 0100 |
| 0111 |
| 0101 |
| 0110 |
| 0011 |
| 0100 |
| 0100 |
| 0100 |
| 0100 |
| 0100 |
| 0100 |
| 0100 |
| XXXX |
| 0011 |
| 0011 |
| 0011 |
| 0011 |
| 0011 |
| 0111 |
| 0101 |
| 0110 |
| XXXX |
| 0000 |

| ImmType (2 bit) |
| --- |
| 01 |
| XX |
| XX |
| 01 |
| 11 |
| 01 |
| XX |
| 01 |
| XX |
| 01 |
| XX |
| 01 |
| 00 |
| XX |
| XX |
| XX |
| 01 |
| XX |
| 01 |
| 01 |
| 01 |
| 01 |
| 00 |
| 00 |
| 11 |
| 01 |
| 01 |
| 01 |
| 01 |
| 01 |
| 00 |
| 00 |
| 00 |
| 11 |
| 00 |

| Control Signals | |
| AndLink (2 bit) | MemWrite (1 bit) |
| --- | --- |
| 00 | 0 |
| 00 | 0 |
| 00 | 0 |
| 00 | 0 |
| 00 | 0 |
| XX | 0 |
| 00 | 0 |
| 00 | 0 |
| 00 | 0 |
| 00 | 0 |
| 10 | 0 |
| 10 | 0 |
| 11 | 0 |
| 00 | 0 |
| 00 | 0 |
| 00 | 0 |
| XX | 1 |
| 00 | 0 |
| XX | 0 |
| XX? | 0 |
| XX | 0 |
| XX | 0 |
| XX | 0 |
| XX | 0 |
| 01 | 0 |
| 01 | 0 |
| XX | 0 |
| XX | 0 |
| XX | 0 |
| XX | 0 |
| 00 | 0 |
| 00 | 0 |
| 00 | 0 |
| XX | 0 |
| 00 | 0 |

| RegWrite (1 bit) | MemToReg (2 bit) | MemRead (1 bit) | Branch (1 bit) |
| --- | --- | --- | --- |
| 1 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 01 | 1 | 0 |
| 1 | 01 | 1 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 0 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 0 | 00 | 0 | 1 |
| 0 | 00 | 0 | 1 |
| 0 | XX | 0 | 1 |
| 0 | XX | 0 | 1 |
| 0 | XX | 0 | 1 |
| 0 | XX | 0 | 1 |
| 1 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 01 | 1 | 0 |
| 1 | 01 | 1 | 0 |
| 1 | 01 | 1 | 0 |
| 1 | 01 | 1 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 00 | 0 | 0 |
| 1 | 10 | 0 | 0 |
| 0 | 00 | 0 | 0 |

| Jump (1 bit) | ALU_Or_Imm_Jump (1 bit) | Flag_Mux (2 bits) | Flag_Or_Nflag |
|---|---|---|---|
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 0 | 00 | X |
| 0 | 0 | 00 | X |
| 0 | 0 | 10 | X |
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 1 | 11 | 0 |
| 0 | 1 | 11 | 1 |
| 0 | 1 | 00 | 0 |
| 0 | 1 | 00 | 1 |
| 0 | 1 | 00 | 0 |
| 0 | 1 | 00 | 1 |
| 1 | 1 | XX | X |
| 1 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | 0 | XX | X |
| 0 | X | XX | X |
| 0 | X | XX | X |
| 0 | X | XX | X |
| 0 | 1 | XX | X |
| 0 | 0 | 00 | 0 |