

# CprE 3810: Computer Organization and Assembly Level Programming

## Team Contract – Project Part 2

Project Teams Group #: B3

Team Members: Anthon Worsham

Drew Swanson

*Discuss the following aspects of teamwork with your team – make sure to get input from each member. Write down your team's consensus for each of the bolded headings. Italicized text contains instructions and examples and should be deleted once you've read it. Please see the example contract for rough length expectations.*

**Course Goals:** List and acknowledge the goals of your individual team members.

*Examples may include:*

- *learn everything about computer architecture*
- *know enough to understand security risks posed by hardware primitives*
- *get an A/B/C/Pass in the course*
- *minimize the number of lost points*
- *prepare myself for a career in hardware design*
- *prepare myself to be able to do research involving FPGAs*
- *be able to explain the workings of a stored-program computer from gates to C*

**Team Goals:**

- Complete the projects
- Worse case get a C, shoot for B+
- Know security risks for cybersecurity
- Be sufficient in VHDL
- Know inner workings of computer processor

**Team Expectations:**

- **Conduct:** *What are the expectations for personal conduct of group members?*
- **Communication:** *What is the best mode of communication for the group? How often should communication occur? How fast should a response be expected?*
- **Group conventions:** *Naming conventions? Compilation and simulation methodology? Testbench strategies? Do file usage? Version control strategies? Commenting standards?*

- **Meetings:** Given the significant portion of the course that the lab covers, it is expected that your team will spend more time working on the labs than in your scheduled lab sections. How will your group expect to handle this? Please include at least two additional times outside of lab that your team can meet (preferably in-person). Examples of other issues to consider include:

- Work together in-person outside of lab sections?
- Work together online outside of lab sections?
- Work separately on responsibilities?

- **Peer Evaluation Criteria:** Now that you have experience working on a 381 lab with a team, please create a brief criteria for how effort and contribution are defined. Note that teams with vastly divergent scores may require a meeting with course instructor and result in different grades for different group members. Teams with reasonably equitable scores will receive the same grade.

**Team Expectations:**

- Only crash out at ourselves and our code, never partner

Communicate clearly and often

All variables should continue with same conventions

USE COMMENTS

Simple testbenches

Meet Friday at 10, Tuesday at 11, weekends work

Effort is trying our best

Be completed with the project by the due date

**Role Responsibilities:** Complete the following planning table. Each lab part should be the responsibility of one team member. Also make sure that no one team member is the lead on both the design and test aspects of a single lab part. These guidelines aid in all students having a complete view of the lab. Note that the non-lead is encouraged to participate and support the lead wherever possible, increasing both the quality of the lab part and each team member's knowledge.

| Lab Part                    |                          | Estimated Time | Design  |          | Test    |          |
|-----------------------------|--------------------------|----------------|---------|----------|---------|----------|
|                             |                          |                | Lead    | Deadline | Lead    | Deadline |
| Software-Scheduled Pipeline | Control Signals          | 0.5 hr         | Drew    | 1 Weeks  | Drew    | 1 Weeks  |
|                             | Datapath                 | 3 hr           | Antho n | 1 Weeks  | Anth on | 1 Weeks  |
|                             | Testing                  | 3 hr           | Drew    | 1 Weeks  | Drew    | 1 Weeks  |
|                             | Synthesis (human effort) | 0.5 hr         | Antho n | 1 Weeks  | Anth on | 1 Weeks  |
| Hardware                    | Pipeline Register Update | 1 hr           | Drew    | 2 Weeks  | Drew    | 2 Weeks  |
|                             | Data Hazard Avoidance    | 4 hr           | Antho n | 2 Weeks  | Anth on | 2 Weeks  |

|                    |  |                            |         |         |         |         |
|--------------------|--|----------------------------|---------|---------|---------|---------|
| Scheduled Pipeline | Control Hazard Avoidance                 | 2-6 hr based on group size | Drew    | 2 Weeks | Drew    | 2 Weeks |
|                    | Integration (Hardware-Schedule Pipeline) | 3 hr                       | Both    | 3 Weeks | Both    | 3 Weeks |
|                    | Testing                                  | 3 hr                       | Both    | 3 Weeks | Both    | 3 Weeks |
|                    | Synthesis                                | 0.5 hr                     | Antho n | 4 Weeks | Anth on | 4 Weeks |

*Estimated Time is given as a **very rough** guide for even distribution of tasks assuming you've already read through the lab document and have the prerequisite knowledge.*

*Please note that to be done properly, the test programs will require significant time investment, but will result in a much stronger final design.*

**Integrity of Work:** *Do not delete the following.* We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

**Student Signature** \_\_\_\_\_ Drew Swanson \_\_\_\_\_ **Date** \_\_\_\_\_ 11/3/25 \_\_\_\_\_

**Student Signature** \_\_\_\_\_ Anthon Worsham \_\_\_\_\_ **Date** \_\_\_\_\_ 11/3/25 \_\_\_\_\_

**Student Signature** \_\_\_\_\_ **Date** \_\_\_\_\_