

## SSD1306 Datasheet by DFRobot

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**SEMICONDUCTOR TECHNICAL DATA**

OLED 2864 DISPLAY  
[TOY0007](#)

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# SSD1306

## *Advance Information*

**128 x 64 Dot Matrix**  
**OLED/PLED Segment/Common Driver with Controller**

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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## 1 GENERAL DESCRIPTION

SSD1306 is a single-chip CMOS OLED/PLED driver with controller for organic / polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 64 commons. This IC is designed for Common Cathode type OLED panel.

The SSD1306 embeds with contrast control, display RAM and oscillator, which reduces the number of external components and power consumption. It has 256-step brightness control. Data/Commands are sent from general MCU through the hardware selectable 6800/8000 series compatible Parallel Interface, I<sup>2</sup>C interface or Serial Peripheral Interface. It is suitable for many compact portable applications, such as mobile phone sub-display, MP3 player and calculator, etc.

## 2 FEATURES

- Resolution: 128 x 64 dot matrix panel
- Power supply
  - V<sub>DD</sub> = 1.65V to 3.3V for IC logic
  - V<sub>CC</sub> = 7V to 15V for Panel driving
- For matrix display
  - OLED driving output voltage, 15V maximum
  - Segment maximum source current: 100uA
  - Common maximum sink current: 15mA
  - 256 step contrast brightness current control
- Embedded 128 x 64 bit SRAM display buffer
- Pin selectable MCU Interfaces:
  - 8-bit 6800/8080-series parallel interface
  - 3 / 4 wire Serial Peripheral Interface
  - I<sup>2</sup>C Interface
- Screen saving continuous scrolling function in both horizontal and vertical direction
- RAM write synchronization signal
- Programmable Frame Rate and Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- On-Chip Oscillator
- Chip layout for COG & COF
- Wide range of operating temperature: -40°C to 85°C

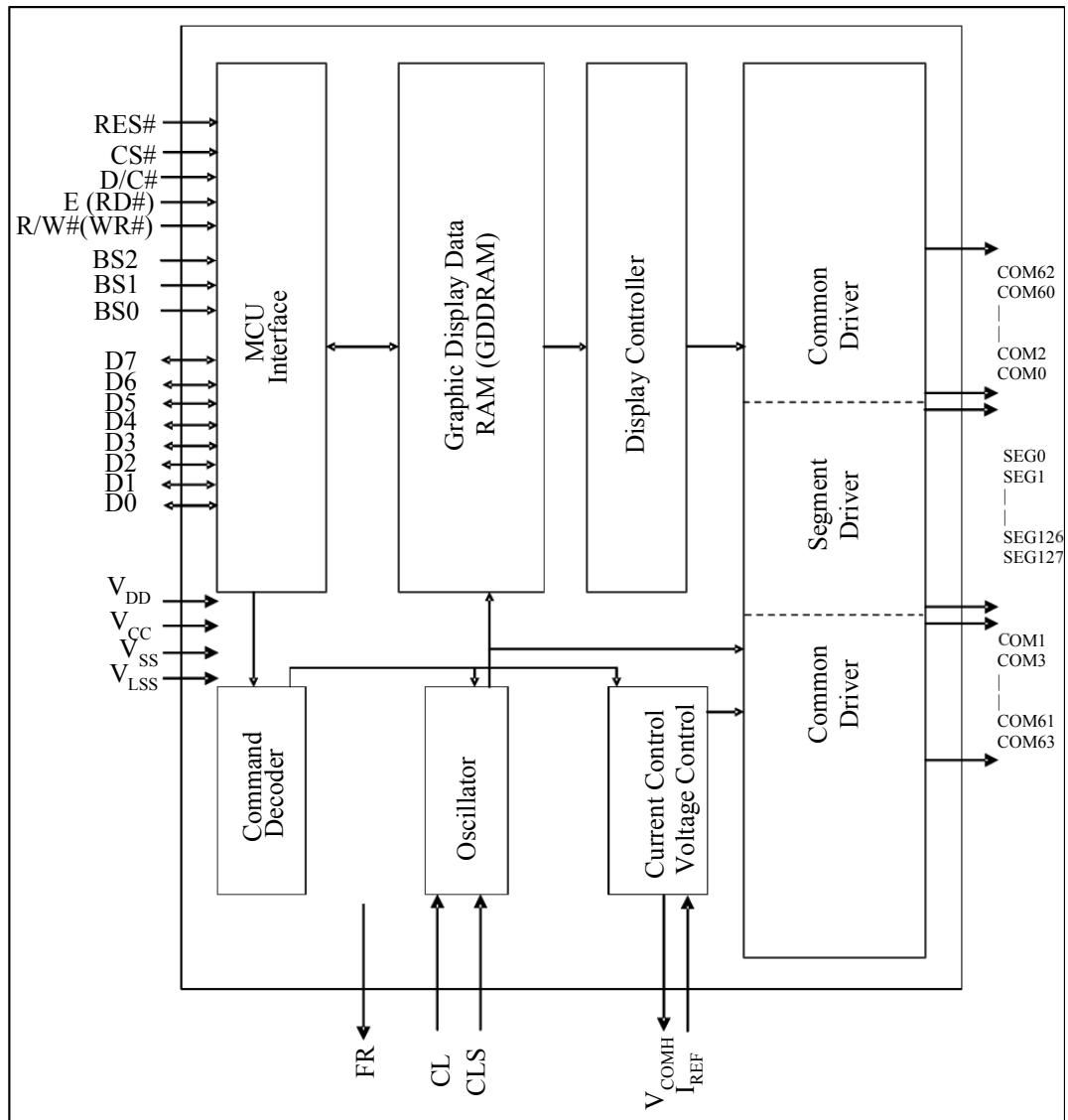
## 3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1306Z	128	64	COG	8	<ul style="list-style-type: none"><li>◦ Min SEG pad pitch : 47um</li><li>◦ Min COM pad pitch : 40um</li><li>◦ Die thickness: 300 +/- 25um</li></ul>
SSD1306TR1	104	48	TAB	11, 56	<ul style="list-style-type: none"><li>◦ 35mm film, 4 sprocket hole, Folding TAB</li><li>◦ 8-bit 80 / 8-bit 68 / SPI / I<sup>2</sup>C interface</li><li>◦ SEG, COM lead pitch 0.1mm x 0.997 =0.0997mm</li><li>◦ Die thickness: 457 +/- 25um</li></ul>

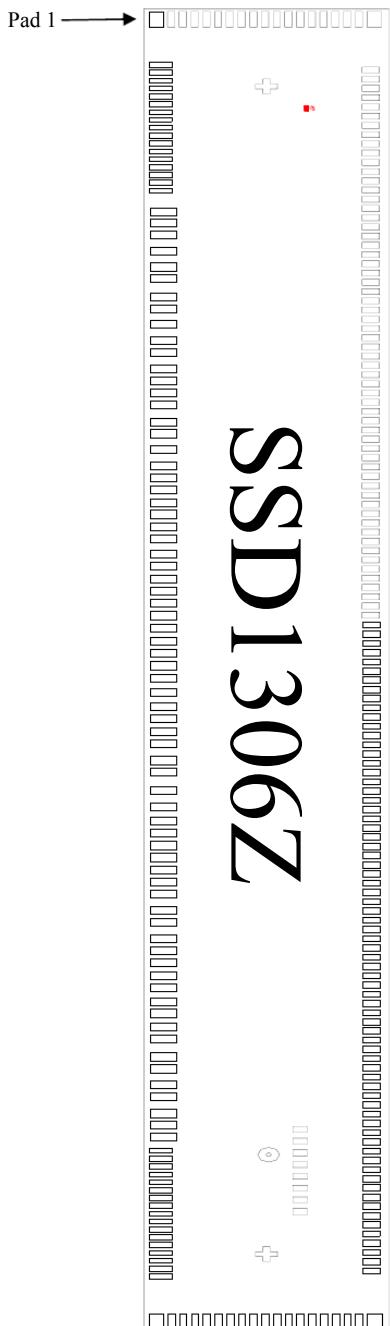
## 4 BLOCK DIAGRAM

Figure 4-1 SSD1306 Block Diagram



## 5 DIE PAD FLOOR PLAN

Figure 5-1 : SSD1306Z Die Drawing



Die size	6.76mm x 0.86mm
Die thickness	300 +/- 25um
Min I/O pad pitch	60um
Min SEG pad pitch	47um
Min COM pad pitch	40um
Bump height	Nominal 15um

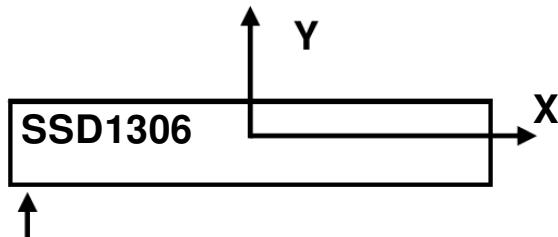
Bump size	
Pad 1, 106, 124, 256	80um x 50um
Pad 2-18, 89-105, 107-123, 257-273	25um x 80um
Pad 19-88	40um x 89um
Pad 125-255	31um x 59um
Pad 274-281 (TR pads)	30um x 50um

Alignment mark	Position	Size
+ shape	(-2973, 0)	75um x 75um
+ shape	(2973, 0)	75um x 75um
Circle	(2466.665, 7.575)	R37.5um, inner 18um
SSL Logo	(-2862.35, 144.82)	-

(For details dimension please see p.9 )

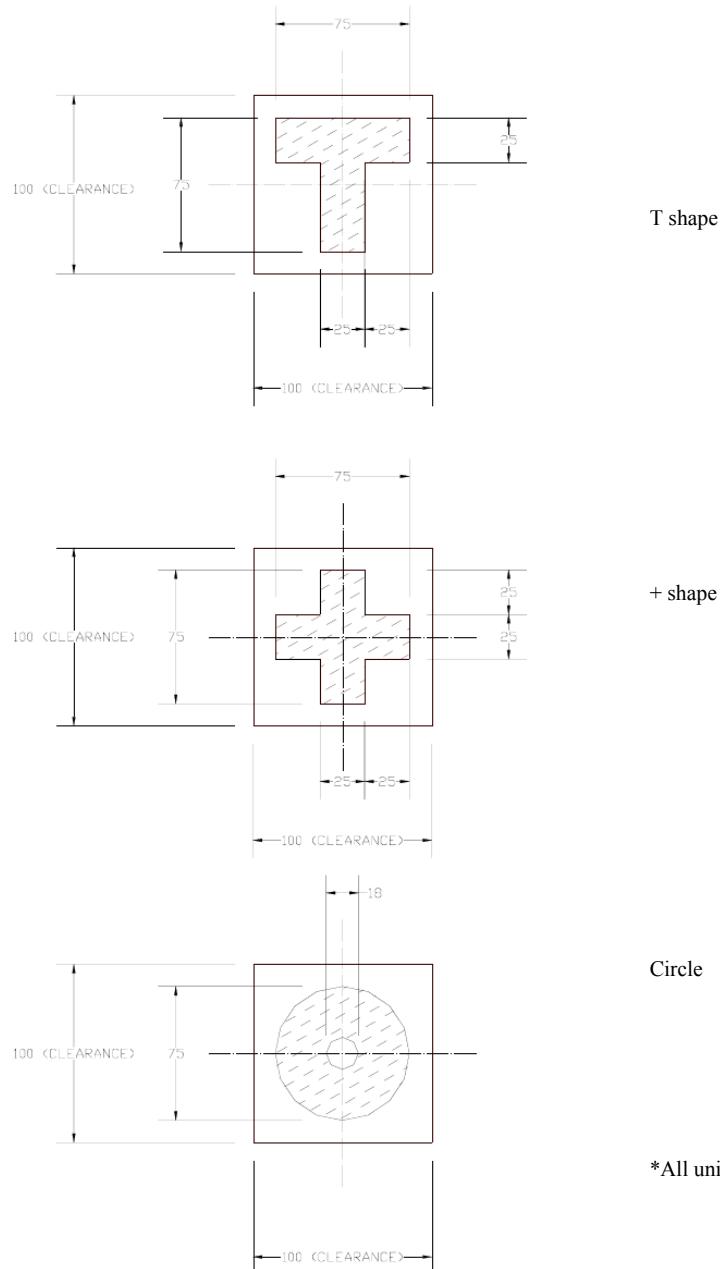
**Note**

- <sup>(1)</sup> Diagram showing the Gold bumps face up.
- <sup>(2)</sup> Coordinates are referenced to center of the chip.
- <sup>(3)</sup> Coordinate units and size of all alignment marks are in um.
- <sup>(4)</sup> All alignment keys do not contain gold



**Pad 1,2,3,...->281**  
Gold Bumps face up

**Figure 5-2 : SSD1306Z alignment mark dimensions**



\*All units are in um

**Table 5-1 : SSD1306Z Bump Die Pad Coordinates**

Pad no.	Pad Name	X-pos	Y-pos
1	NC	-3315	-377.5
2	VSS	-3084.77	-362.5
3	COM49	-3044.77	-362.5
4	COM50	-3004.77	-362.5
5	COM51	-2964.77	-362.5
6	COM52	-2924.77	-362.5
7	COM53	-2884.77	-362.5
8	COM54	-2844.77	-362.5
9	COM55	-2804.77	-362.5
10	COM56	-2764.77	-362.5
11	COM57	-2724.77	-362.5
12	COM58	-2684.77	-362.5
13	COM59	-2644.77	-362.5
14	COM60	-2604.77	-362.5
15	COM61	-2564.77	-362.5
16	COM62	-2524.77	-362.5
17	COM63	-2484.77	-362.5
18	VCOMH	-2444.77	-362.5
19	NC	-2334.965	-352.83
20	C2P	-2278.265	-352.83
21	C2P	-2218.265	-352.83
22	C2N	-2136.715	-352.83
23	C2N	-2055.465	-352.83
24	C1P	-1995.465	-352.83
25	C1P	-1904.115	-352.83
26	C1N	-1844.115	-352.83
27	C1N	-1762.865	-352.83
28	VBAT	-1679.31	-352.83
29	VBAT	-1619.31	-352.83
30	VBREF	-1537.51	-352.83
31	BGND	-1477.51	-352.83
32	VCC	-1416.01	-352.83
33	VCC	-1356.01	-352.83
34	VCOMH	-1266.955	-352.83
35	VCOMH	-1206.955	-352.83
36	VLSS	-1125.155	-352.83
37	VLSS	-1043.355	-352.83
38	VLSS	-983.355	-352.83
39	VSS	-920	-352.83
40	VSS	-856	-352.83
41	VSS	-796	-352.83
42	VDD	-732.645	-352.83
43	VDD	-672.645	-352.83
44	BS0	-595.655	-352.83
45	VSS	-531.955	-352.83
46	BS1	-467.655	-352.83
47	VDD	-403.155	-352.83
48	VDD	-342.555	-352.83
49	BS2	-279.705	-352.83
50	VSS	-215.705	-352.83
51	FR	-151.955	-352.83
52	CL	-89.815	-352.83
53	VSS	-25.665	-352.83
54	CS#	38.635	-352.83
55	RES#	109.835	-352.83
56	D/C#	182.425	-352.83
57	VSS	246.125	-352.83
58	R/W#	310.425	-352.83
59	E	373.125	-352.83
60	VDD	457.175	-352.83
61	VDD	517.175	-352.83
62	DO	609.275	-352.83
63	D1	692.475	-352.83
64	D2	765.675	-352.83
65	D3	828.875	-352.83
66	VSS	890.325	-352.83
67	D4	951.275	-352.83
68	D5	1013.315	-352.83
69	D6	1075.355	-352.83
70	D7	1137.395	-352.83
71	VSS	1220.735	-352.83
72	VSS	1280.735	-352.83
73	CLS	1362.585	-352.83
74	VDD	1425.285	-352.83
75	VDD	1485.885	-352.83
76	VDD	1553.185	-352.83
77	VDD	1613.185	-352.83
78	IREF	1684.585	-352.83
79	IREF	1744.585	-352.83
80	VCOMH	1815.585	-352.83

Pad no.	Pad Name	X-pos	Y-pos
81	VCOMH	1875.585	-352.83
82	VCC	1967.185	-352.83
83	VCC	2027.185	-352.83
84	VLSS	2109.185	-352.83
85	VLSS	2169.185	-352.83
86	VLSS	2254.185	-352.83
87	NC	2314.185	-352.83
88	NC	2374.185	-352.83
89	VSS	2444.77	-362.5
90	COM31	2484.77	-362.5
91	COM30	2524.77	-362.5
92	COM29	2564.77	-362.5
93	COM28	2604.77	-362.5
94	COM27	2644.77	-362.5
95	COM26	2684.77	-362.5
96	COM25	2724.77	-362.5
97	COM24	2764.77	-362.5
98	COM23	2804.77	-362.5
99	COM22	2844.77	-362.5
100	COM21	2884.77	-362.5
101	COM20	2924.77	-362.5
102	COM19	2964.77	-362.5
103	COM18	3004.77	-362.5
104	COM17	3044.77	-362.5
105	VSS	3084.77	-362.5
106	NC	3315	-377.5
107	COM16	3315	-325
108	COM15	3315	-285
109	COM14	3315	-245
110	COM13	3315	-205
111	COM12	3315	-165
112	COM11	3315	-125
113	COM10	3315	-85
114	COM9	3315	-45
115	COM8	3315	-5
116	COM7	3315	35
117	COM6	3315	75
118	COM5	3315	115
119	COM4	3315	155
120	COM3	3315	195
121	COM2	3315	235
122	COM1	3315	275
123	COM0	3315	315
124	NC	3315	367.5
125	NC	3055.5	356
126	SEQ0	3009.5	356
127	SEGI	2962.5	356
128	SEG2	2915.5	356
129	SEG3	2868.5	356
130	SEG4	2821.5	356
131	SEG5	2774.5	356
132	SEG6	2727.5	356
133	SEG7	2680.5	356
134	SEG8	2633.5	356
135	SEG9	2586.5	356
136	SEG10	2539.5	356
137	SEG11	2492.5	356
138	SEG12	2445.5	356
139	SEG13	2398.5	356
140	SEG14	2351.5	356
141	SEG15	2304.5	356
142	SEG16	2257.5	356
143	SEG17	2210.5	356
144	SEG18	2163.5	356
145	SEG19	2116.5	356
146	SEG20	2069.5	356
147	SEG21	2022.5	356
148	SEG22	1975.5	356
149	SEG23	1928.5	356
150	SEG24	1881.5	356
151	SEG25	1834.5	356
152	SEG26	1787.5	356
153	SEG27	1740.5	356
154	SEG28	1693.5	356
155	SEG29	1646.5	356
156	SEG30	1599.5	356
157	SEG31	1552.5	356
158	SEG32	1505.5	356
159	SEG33	1458.5	356
160	SEG34	1411.5	356

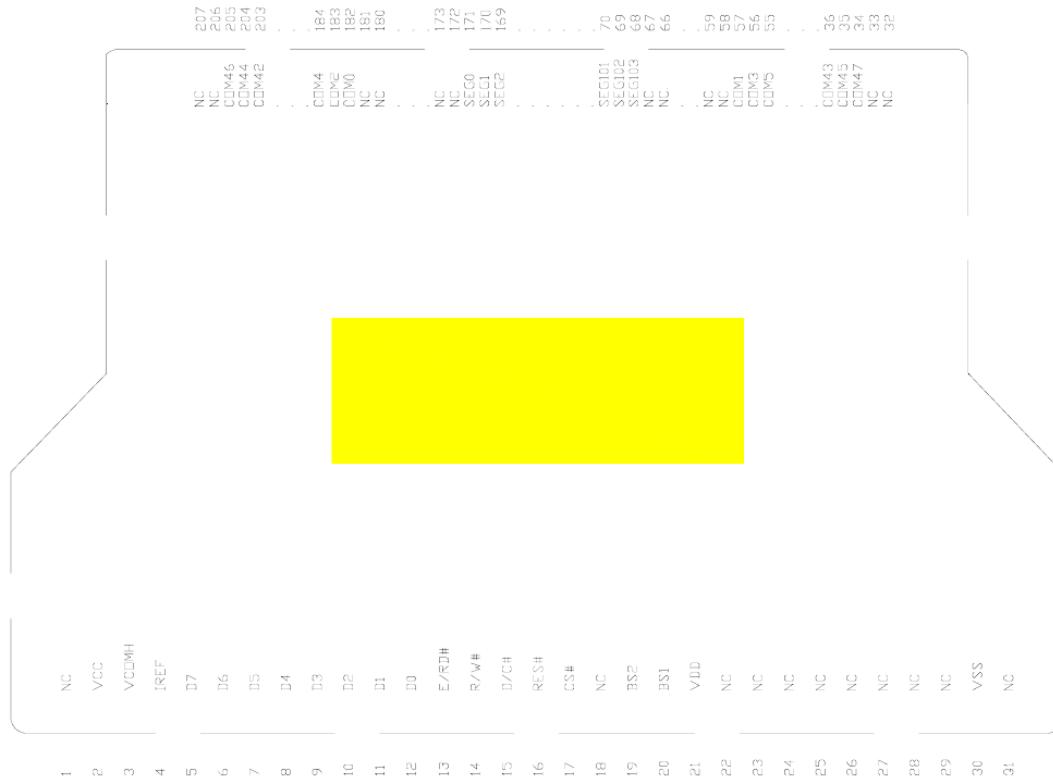
Pad no.	Pad Name	X-pos	Y-pos
161	SEG35	1364.5	356
162	SEG36	1317.5	356
163	SEG37	1270.5	356
164	SEG38	1223.5	356
165	SEG39	1176.5	356
166	SEG40	1129.5	356
167	SEG41	1082.5	356
168	SEG42	1035.5	356
169	SEG43	988.5	356
170	SEG44	941.5	356
171	SEG45	894.5	356
172	SEG46	847.5	356
173	SEG47	800.5	356
174	SEG48	753.5	356
175	SEG49	706.5	356
176	SEG50	659.5	356
177	SEG51	612.5	356
178	SEG52	565.5	356
179	SEG53	518.5	356
180	SEG54	471.5	356
181	SEG55	424.5	356
182	SEG56	377.5	356
183	SEG57	330.5	356
184	SEG58	283.5	356
185	SEG59	236.5	356
186	SEG60	189.5	356
187	SEG61	142.5	356
188	SEG62	95.5	356
189	SEG63	48.5	356
190	SEG64	1.5	356
191	SEG65	-45.5	356
192	SEG66	-92.5	356
193	SEG67	-139.5	356
194	SEG68	-186.5	356
195	SEG69	-233.5	356
196	SEG70	-280.5	356
197	SEG71	-327.5	356
198	SEG72	-374.5	356
199	SEG73	-421.5	356
200	SEG74	-468.5	356
201	SEG75	-515.5	356
202	SEG76	-562.5	356
203	SEG77	-609.5	356
204	SEG78	-656.5	356
205	SEG79	-703.5	356
206	SEG80	-750.5	356
207	SEG81	-797.5	356
208	SEG82	-844.5	356
209	SEG83	-891.5	356
210	NC	-940	356
211	SEG84	-988.5	356
212	SEG85	-1035.5	356
213	SEG86	-1082.5	356
214	SEG87	-1129.5	356
215	SEG88	-1176.5	356
216	SEG89	-1223.5	356
217	SEG90	-1270.5	356
218	SEG91	-1317.5	356
219	SEG92	-1364.5	356
220	SEG93	-1411.5	356
221	SEG94	-1458.5	356
222	SEG95	-1505.5	356
223	SEG96	-1552.5	356
224	SEG97	-1599.5	356
225	SEG98	-1646.5	356
226	SEG99	-1693.5	356
227	SEG100	-1740.5	356
228	SEG101	-1787.5	356
229	SEG102	-1834.5	356
230	SEG103	-1881.5	356
231	SEG104	-1928.5	356
232	SEG105	-1975.5	356
233	SEG106	-2022.5	356
234	SEG107	-2069.5	356
235	SEG108	-2116.5	356
236	SEG109	-2163.5	356
237	SEG110	-2210.5	356
238	SEG111	-2257.5	356
239	SEG112	-2304.5	356
240	SEG113	-2351.5	356

Pad no.	Pad Name	X-pos	Y-pos
Pin#	Pin name	X-dir	Y-dir
274	TR0	2757.05	114.8
275	TR1	2697.05	114.8
276	TR2	2637.05	114.8
277	TR3	2577.05	114.8
278	VSS	2517.05	114.8
279	TR4	2457.05	114.8
280	TR5	2397.05	114.8
281	TR6	2337.05	114.8

## 6 PIN ARRANGEMENT

### 6.1 SSD1306TR1 pin assignment

Figure 6-1 : SSD1306TR1 Pin Assignment



Note:

<sup>(1)</sup> COM sequence (Split) is under command setting: DAh, 12h

**Table 6-1 : SSD1306TR1 Pin Assignment Table**

Pin no.	Pin Name	Pin no.	Pin Name	Pin no.	Pin Name
1	NC	81	SEG90	161	SEG10
2	VCC	82	SEG89	162	SEG9
3	VCOMH	83	SEG88	163	SEG8
4	IREF	84	SEG87	164	SEG7
5	D7	85	SEG86	165	SEG6
6	D6	86	SEG85	166	SEG5
7	D5	87	SEG84	167	SEG4
8	D4	88	SEG83	168	SEG3
9	D3	89	SEG82	169	SEG2
10	D2	90	SEG81	170	SEG1
11	D1	91	SEG80	171	SEG0
12	D0	92	SEG79	172	NC
13	E/RD#	93	SEG78	173	NC
14	R/W#	94	SEG77	174	NC
15	DC#	95	SEG76	175	NC
16	RES#	96	SEG75	176	NC
17	CS#	97	SEG74	177	NC
18	NC	98	SEG73	178	NC
19	BS2	99	SEG72	179	NC
20	BS1	100	SEG71	180	NC
21	VDD	101	SEG70	181	NC
22	NC	102	SEG69	182	COM0
23	NC	103	SEG68	183	COM2
24	NC	104	SEG67	184	COM4
25	NC	105	SEG66	185	COM6
26	NC	106	SEG65	186	COM8
27	NC	107	SEG64	187	COM10
28	NC	108	SEG63	188	COM12
29	NC	109	SEG62	189	COM14
30	VSS	110	SEG61	190	COM16
31	NC	111	SEG60	191	COM18
32	NC	112	SEG59	192	COM20
33	NC	113	SEG58	193	COM22
34	COM47	114	SEG57	194	COM24
35	COM45	115	SEG56	195	COM26
36	COM43	116	SEG55	196	COM28
37	COM41	117	SEG54	197	COM30
38	COM39	118	SEG53	198	COM32
39	COM37	119	SEG52	199	COM34
40	COM35	120	SEG51	200	COM36
41	COM33	121	SEG50	201	COM38
42	COM31	122	SEG49	202	COM40
43	COM29	123	SEG48	203	COM42
44	COM27	124	SEG47	204	COM44
45	COM25	125	SEG46	205	COM46
46	COM23	126	SEG45	206	NC
47	COM21	127	SEG44	207	NC
48	COM19	128	SEG43		
49	COM17	129	SEG42		
50	COM15	130	SEG41		
51	COM13	131	SEG40		
52	COM11	132	SEG39		
53	COM9	133	SEG38		
54	COM7	134	SEG37		
55	COM5	135	SEG36		
56	COM3	136	SEG35		
57	COM1	137	SEG34		
58	NC	138	SEG33		
59	NC	139	SEG32		
60	NC	140	SEG31		
61	NC	141	SEG30		
62	NC	142	SEG29		
63	NC	143	SEG28		
64	NC	144	SEG27		
65	NC	145	SEG26		
66	NC	146	SEG25		
67	NC	147	SEG24		
68	SEG103	148	SEG23		
69	SEG102	149	SEG22		
70	SEG101	150	SEG21		
71	SEG100	151	SEG20		
72	SEG99	152	SEG19		
73	SEG98	153	SEG18		
74	SEG97	154	SEG17		
75	SEG96	155	SEG16		
76	SEG95	156	SEG15		
77	SEG94	157	SEG14		
78	SEG93	158	SEG13		
79	SEG92	159	SEG12		
80	SEG91	160	SEG11		

## 7 PIN DESCRIPTION

**Key:**

I = Input	NC = Not Connected
O = Output	Pull LOW= connect to Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V <sub>DD</sub>
P = Power pin	

Figure 7-1 Pin Description

Pin Name	Type	Description
V <sub>DD</sub>	P	Power supply pin for core logic operation.
V <sub>CC</sub>	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
V <sub>SS</sub>	P	This is a ground pin.
V <sub>LSS</sub>	P	This is an analog ground pin. It should be connected to V <sub>SS</sub> externally.
V <sub>COMH</sub>	O	The pin for COM signal deselected voltage level. A capacitor should be connected between this pin and V <sub>SS</sub> .
V <sub>BAT</sub>	P	Reserved pin. It should be connected to V <sub>DD</sub> .
BGGND	P	Reserved pin. It should be connected to ground.
C1P/C1N C2P/C2N	I	Reserved pin. It should be kept NC.
V <sub>BREF</sub>	P	Reserved pin. It should be kept NC.
BS[2:0]	I	MCU bus interface selection pins. Please refer to <b>Table 7-1</b> for the details of setting.
I <sub>REF</sub>	I	This is segment output current reference pin. A resistor should be connected between this pin and V <sub>SS</sub> to maintain the I <sub>REF</sub> current at 12.5 uA. Please refer to <b>Figure 8-15</b> for the details of resistor value.
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used. Please refer to Section 8.4 for details usage.
CL	I	This is external clock input pin. When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V <sub>SS</sub> . When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.
CLS	I	This is internal clock enable pin. When it is pulled HIGH (i.e. connect to V <sub>DD</sub> ), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.
RES#	I	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin HIGH (i.e. connect to V <sub>DD</sub> ) during normal operation.
CS#	I	This pin is the chip select input. (active LOW).

Pin Name	Type	Description
D/C#	I	This is Data/Command control pin. When it is pulled HIGH (i.e. connect to V <sub>DD</sub> ), the data at D[7:0] is treated as data. When it is pulled LOW, the data at D[7:0] will be transferred to the command register. In I <sup>2</sup> C mode, this pin acts as SA0 for slave address selection. When 3-wire serial interface is selected, this pin must be connected to V <sub>SS</sub> .  For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams: <b>Figure 13-1</b> to <b>Figure 13-5</b> .
E (RD#)	I	When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH (i.e. connect to V <sub>DD</sub> ) and the chip is selected. When connecting to an 8080-series microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I <sup>2</sup> C interface is selected, this pin must be connected to V <sub>SS</sub> .
R/W#(WR#)	I	This is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH (i.e. connect to V <sub>DD</sub> ) and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I <sup>2</sup> C interface is selected, this pin must be connected to V <sub>SS</sub> .
D[7:0]	IO	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I <sup>2</sup> C mode is selected, D2, D1 should be tied together and serve as SDA <sub>out</sub> , SDA <sub>in</sub> in application and D0 is the serial clock input, SCL.
TR0-TR6	-	Testing reserved pins. It should be kept NC.
SEG0 ~ SEG127	O	These pins provide Segment switch signals to OLED panel. These pins are V <sub>SS</sub> state when display is OFF.
COM0 ~ COM63	O	These pins provide Common switch signals to OLED panel. They are in high impedance state when display is OFF.
NC	-	This is dummy pin. Do not group or short NC pins together.

Table 7-1 : MCU Bus Interface Pin Selection

SSD1306 Pin Name	I <sup>2</sup> C Interface	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	4-wire Serial interface	3-wire Serial interface
BS0	0	0	0	0	1
BS1	1	0	1	0	0
BS2	0	1	1	0	0

**Note**

<sup>(1)</sup> 0 is connected to V<sub>SS</sub>

<sup>(2)</sup> 1 is connected to V<sub>DD</sub>

## 8 FUNCTIONAL BLOCK DESCRIPTIONS

### 8.1 MCU Interface selection

SSD1306 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 7-1 for BS[2:0] setting).

**Table 8-1 : MCU interface assignment under different bus interface mode**

Pin Name Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080						D[7:0]			RD#	WR#	CS#	D/C#	RES#
8-bit 6800						D[7:0]			E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW				NC	SDIN	SCLK		Tie LOW	CS#	Tie LOW	RES#	
4-wire SPI	Tie LOW				NC	SDIN	SCLK		Tie LOW	CS#	D/C#	RES#	
I <sup>2</sup> C	Tie LOW				SDA <sub>OUT</sub>	SDA <sub>IN</sub>	SCL		Tie LOW		SA0	RES#	

#### 8.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.

The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

**Table 8-2 : Control pins of 6800 interface**

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

#### Note

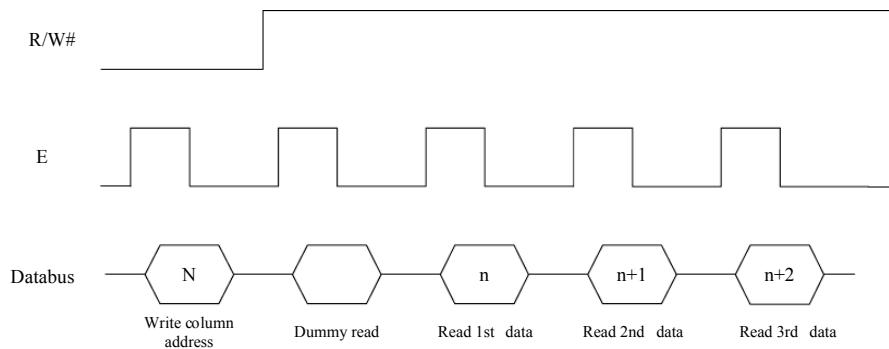
<sup>(1)</sup> ↓ stands for falling edge of signal

H stands for HIGH in signal

L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

**Figure 8-1 : Data read back procedure - insertion of dummy read**



### 8.1.2 MCU Parallel 8080-series Interface

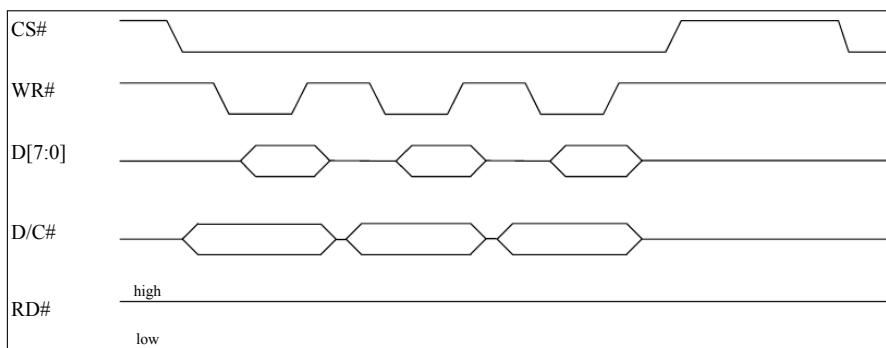
The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.

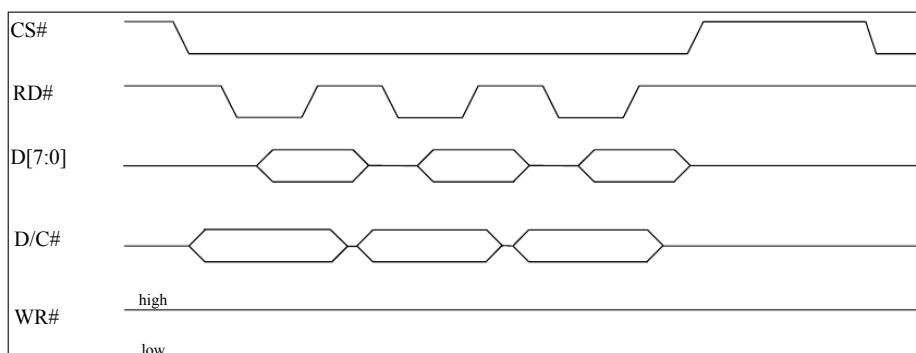
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.

A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

**Figure 8-2 : Example of Write procedure in 8080 parallel interface mode**



**Figure 8-3 : Example of Read procedure in 8080 parallel interface mode**



**Table 8-3 : Control pins of 8080 interface**

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

**Note**

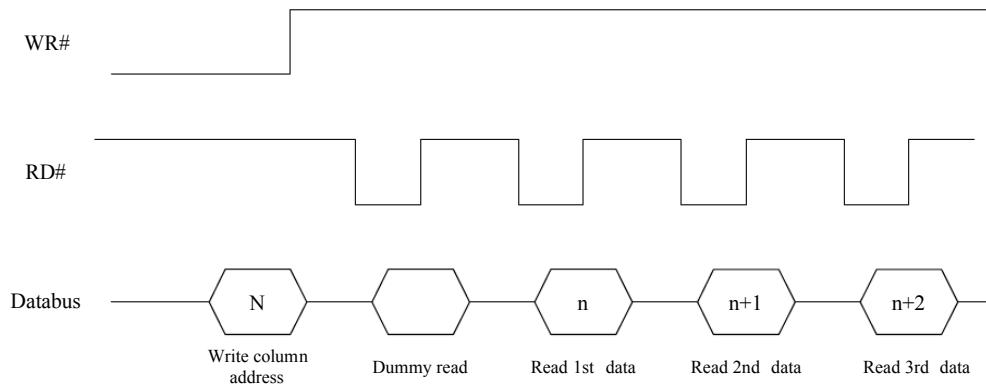
(<sup>1</sup>) ↑ stands for rising edge of signal

(<sup>2</sup>) H stands for HIGH in signal

(<sup>3</sup>) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-4.

**Figure 8-4 : Display data read back procedure - insertion of dummy read**



### 8.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# (WR#) can be connected to an external ground.

**Table 8-4 : Control pins of 4-wire Serial interface**

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

**Note**

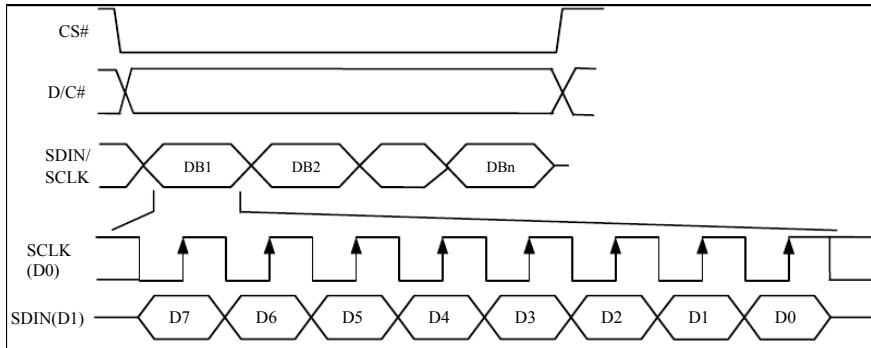
(<sup>1</sup>) H stands for HIGH in signal

(<sup>2</sup>) L stands for LOW in signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

**Figure 8-5 : Write procedure in 4-wire Serial interface mode**



#### 8.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.

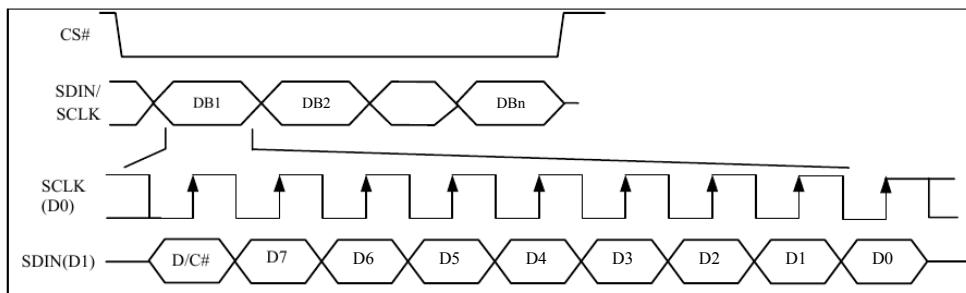
In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#) #, E and D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

**Table 8-5 : Control pins of 3-wire Serial interface**

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0	Note
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑	( <sup>1</sup> ) L stands for LOW in signal
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑	

**Figure 8-6 : Write procedure in 3-wire Serial interface mode**



### 8.1.5 MCU I<sup>2</sup>C Interface

The I<sup>2</sup>C communication interface consists of slave address bit SA0, I<sup>2</sup>C-bus data signal SDA (SDA<sub>OUT</sub>/D<sub>2</sub> for output and SDA<sub>IN</sub>/D<sub>1</sub> for input) and I<sup>2</sup>C-bus clock signal SCL (D<sub>0</sub>). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)

SSD1306 has to recognize the slave address before transmitting or receiving any information by the I<sup>2</sup>C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

b<sub>7</sub> b<sub>6</sub> b<sub>5</sub> b<sub>4</sub> b<sub>3</sub> b<sub>2</sub> b<sub>1</sub> b<sub>0</sub>  
0 1 1 1 1 0 SA0 R/W#

"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1306. D/C# pin acts as SA0 for slave address selection.

"R/W#" bit is used to determine the operation mode of the I<sup>2</sup>C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I<sup>2</sup>C-bus data signal (SDA)

SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

"SDA<sub>IN</sub>" and "SDA<sub>OUT</sub>" are tied together and serve as SDA. The "SDA<sub>IN</sub>" pin must be connected to act as SDA. The "SDA<sub>OUT</sub>" pin may be disconnected. When "SDA<sub>OUT</sub>" pin is disconnected, the acknowledgement signal will be ignored in the I<sup>2</sup>C-bus.

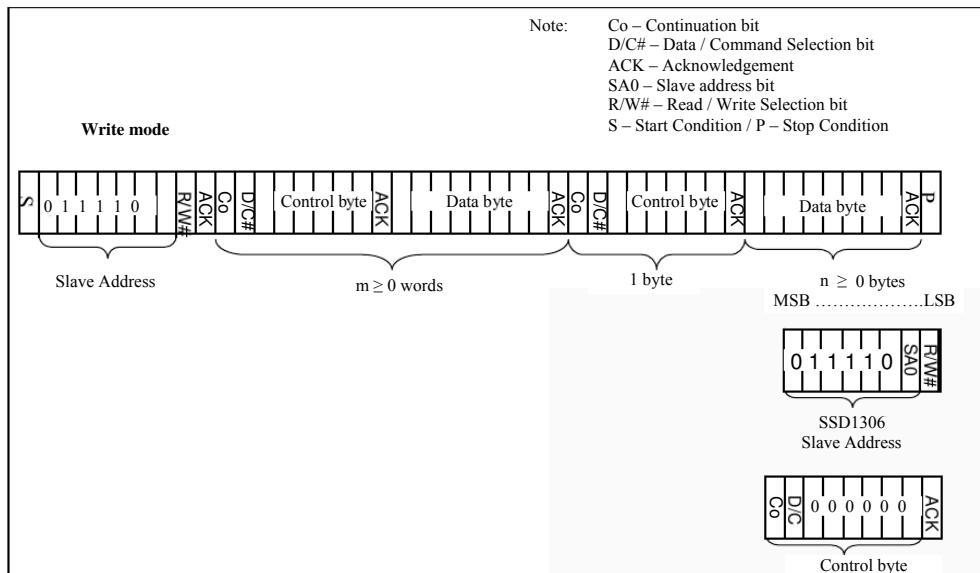
c) I<sup>2</sup>C-bus clock signal (SCL)

The transmission of information in the I<sup>2</sup>C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

### 8.1.5.1 I<sup>2</sup>C-bus Write data

The I<sup>2</sup>C-bus interface gives access to write data and command into the device. Please refer to Figure 8-7 for the write mode of I<sup>2</sup>C-bus in chronological order.

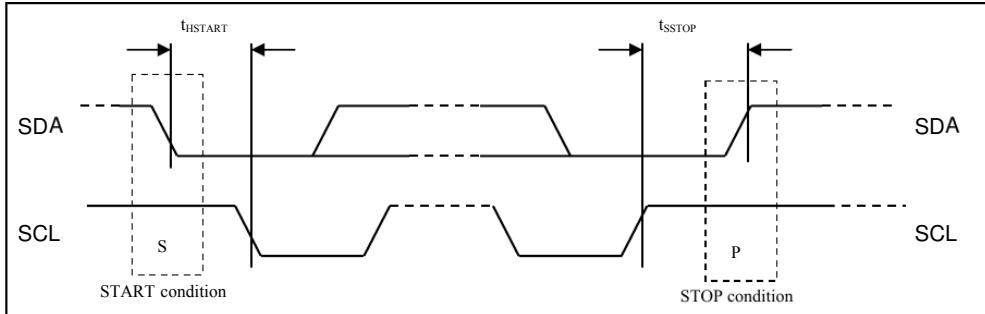
**Figure 8-7 : I<sup>2</sup>C-bus data format**



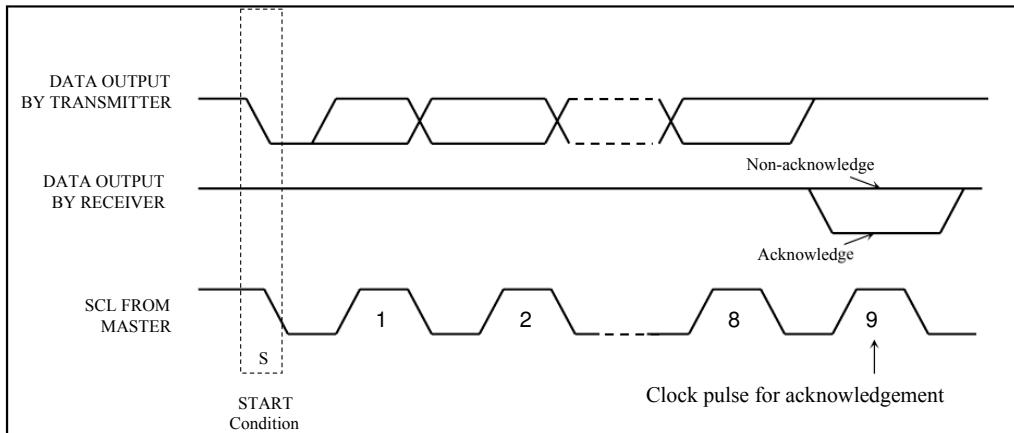
### 8.1.5.2 Write mode for I<sup>2</sup>C

- 1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 8-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
- 2) The slave address is following the start condition for recognition use. For the SSD1306, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
- 3) The write mode is established by setting the R/W# bit to logic “0”.
- 4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 8-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
- 5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0” ‘s.
  - a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
  - b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
- 6) Acknowledge bit will be generated after receiving each control byte or data byte.
- 7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 8-8. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

**Figure 8-8 : Definition of the Start and Stop Condition**



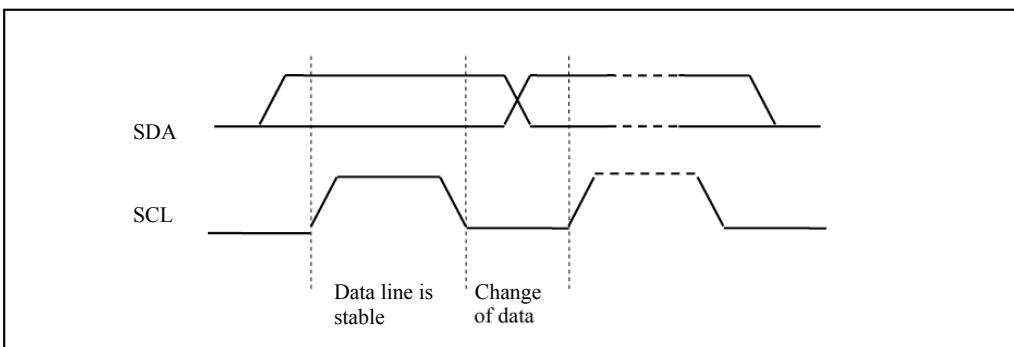
**Figure 8-9 : Definition of the acknowledgement condition**



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the “HIGH” period of the clock pulse. Please refer to the Figure 8-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

**Figure 8-10 : Definition of the data transfer condition**



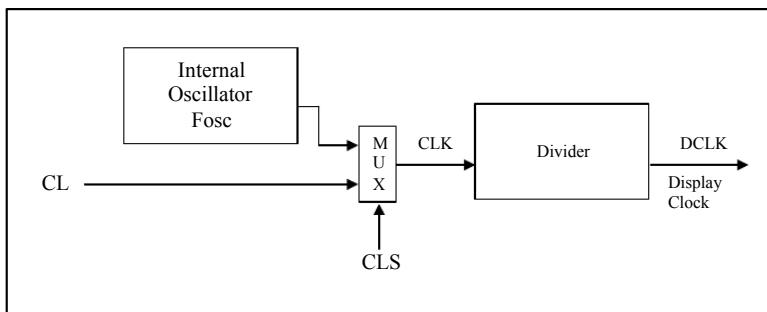
## 8.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

## 8.3 Oscillator Circuit and Display Time Generator

Figure 8-11 : Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be left open. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command D5h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor “D” can be programmed from 1 to 16 by command D5h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

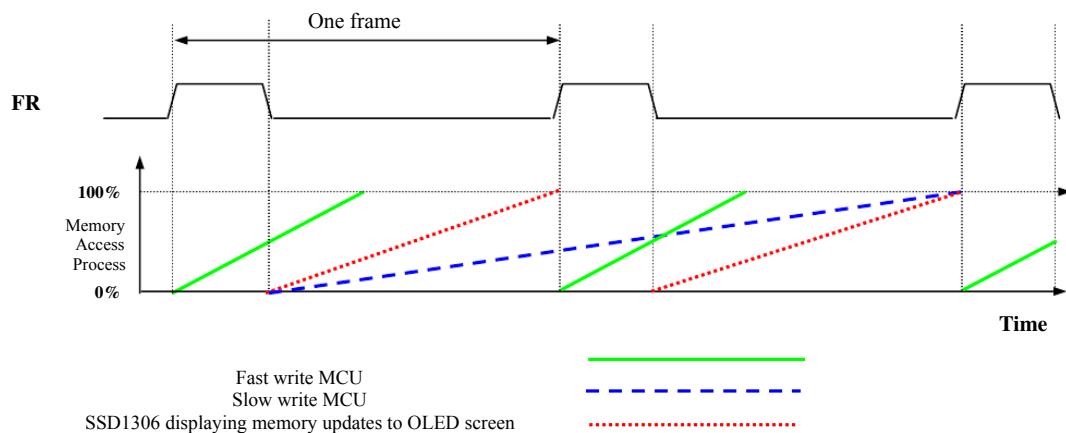
$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

- D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
$$\begin{aligned} K &= \text{Phase 1 period} + \text{Phase 2 period} + \text{BANK0 pulse width} \\ &= 2 + 2 + 50 = 54 \text{ at power on reset} \end{aligned}$$
(Please refer to Section 8.6 “Segment Drivers / Common Drivers” for the details of the “Phase”)
- Number of multiplex ratio is set by command A8h. The power on reset value is 63 (i.e. 64MUX).
- Fosc is the oscillator frequency. It can be changed by command D5h A[7:4]. The higher the register setting results in higher frequency.

## 8.4 FR synchronization

FR synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

**For fast write MCU:** MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

**For slow write MCU:** MCU should start to write new frame ram data after the falling edge of the 1<sup>st</sup> FR pulse and must be finished before the rising edge of the 3<sup>rd</sup> FR pulse.

## 8.5 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 64 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

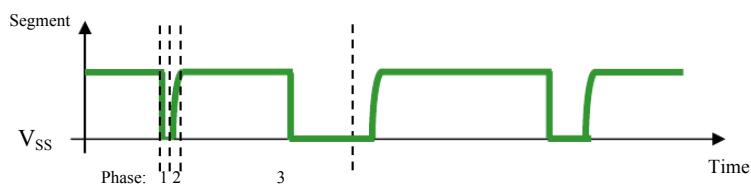
## 8.6 Segment Drivers / Common Drivers

Segment drivers deliver 128 current sources to drive the OLED panel. The driving current can be adjusted from 0 to 100uA with 256 steps. Common drivers generate voltage-scanning pulses.

The segment driving waveform is divided into three phases:

1. In phase 1, the OLED pixel charges of previous image are discharged in order to prepare for next image content display.
2. In phase 2, the OLED pixel is driven to the targeted voltage. The pixel is driven to attain the corresponding voltage level from  $V_{SS}$ . The period of phase 2 can be programmed in length from 1 to 15 DCLKs. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.
3. In phase 3, the OLED driver switches to use current source to drive the OLED pixels and this is the current drive stage.

**Figure 8-12 : Segment Output Waveform in three phases**



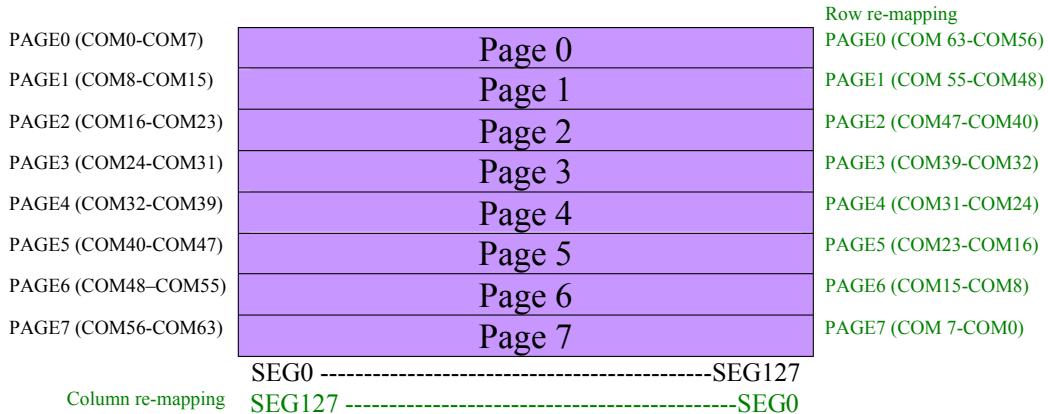
After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

In phase 3, if the length of current drive pulse width is set to 50, after finishing 50 DCLKs in current drive phase, the driver IC will go back to phase 1 for next row display.

## 8.7 Graphic Display Data RAM (GDDRAM)

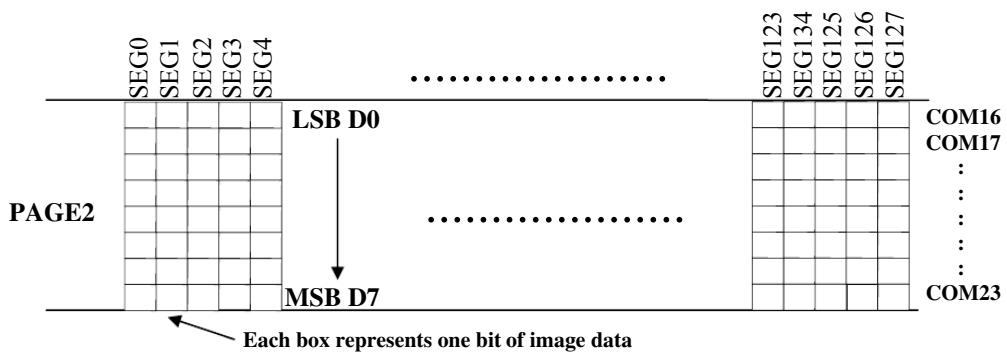
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in Figure 8-13.

**Figure 8-13 : GDDRAM pages structure of SSD1306**



When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in Figure 8-14.

**Figure 8-14 : Enlargement of GDDRAM (No row re-mapping and column-remapping)**



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software as shown in Figure 8-13.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

## 8.8 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- $V_{CC}$  is the most positive voltage supply.
- $V_{COMH}$  is the Common deselected level. It is internally regulated.
- $V_{LSS}$  is the ground path of the analog and panel current.
- $I_{REF}$  is a reference current source for segment current drivers  $I_{SEG}$ . The relationship between reference current and segment current of a color is:

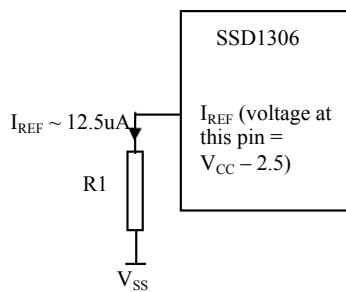
$$I_{SEG} = \text{Contrast} / 256 \times I_{REF} \times \text{scale factor}$$

in which

the contrast (0~255) is set by Set Contrast command 81h; and  
the scale factor is 8 by default.

The magnitude of  $I_{REF}$  is controlled by the value of resistor, which is connected between  $I_{REF}$  pin and  $V_{SS}$  as shown in Figure 8-15. It is recommended to set  $I_{REF}$  to  $12.5 \pm 2\mu A$  so as to achieve  $I_{SEG} = 100\mu A$  at maximum contrast 255.

**Figure 8-15 :  $I_{REF}$  Current Setting by Resistor Value**



Since the voltage at  $I_{REF}$  pin is  $V_{CC} - 2.5V$ , the value of resistor R1 can be found as below:

For  $I_{REF} = 12.5\mu A$ ,  $V_{CC} = 12V$ :

$$\begin{aligned} R1 &= (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF} \\ &= (12 - 2.5) / 12.5\mu A \\ &= 760K\Omega \end{aligned}$$

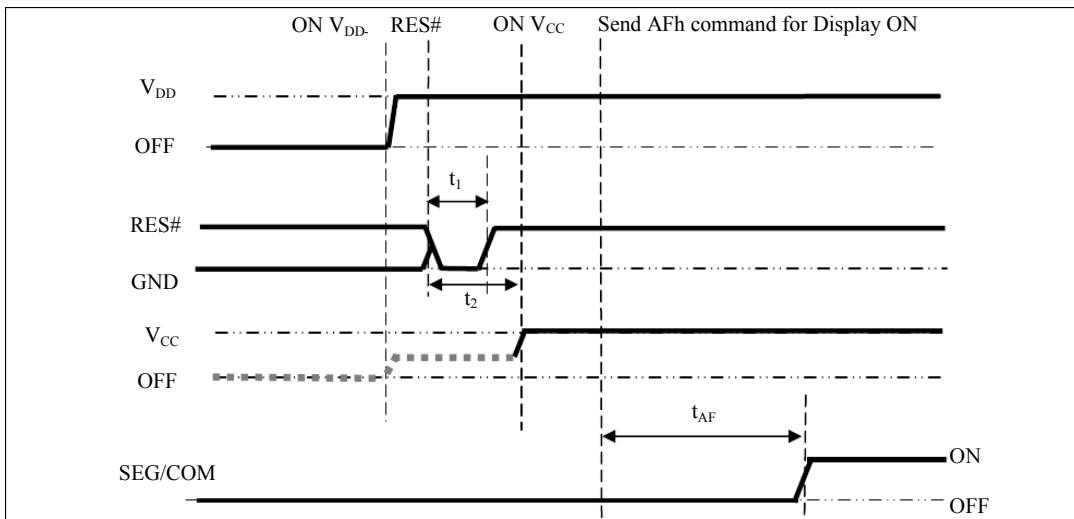
## 8.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1306

*Power ON sequence:*

1. Power ON  $V_{DD}$
2. After  $V_{DD}$  become stable, set RES# pin LOW (logic low) for at least 3us ( $t_1$ ) <sup>(4)</sup> and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us ( $t_2$ ). Then Power ON  $V_{CC}$ <sup>(1)</sup>
4. After  $V_{CC}$  become stable, send command AFh for display ON. SEG/COM will be ON after 100ms ( $t_{AF}$ ).

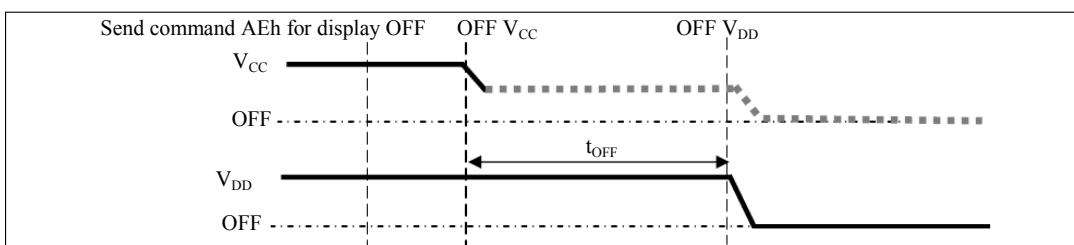
Figure 8-16 : The Power ON sequence



*Power OFF sequence:*

1. Send command AEh for display OFF.
2. Power OFF  $V_{CC}$ <sup>(1), (2), (3)</sup>
3. Power OFF  $V_{DD}$  after  $t_{OFF}$ . <sup>(5)</sup> (Typical  $t_{OFF}=100ms$ )

Figure 8-17 : The Power OFF sequence



### Note:

<sup>(1)</sup> Since an ESD protection circuit is connected between  $V_{DD}$  and  $V_{CC}$ ,  $V_{CC}$  becomes lower than  $V_{DD}$  whenever  $V_{DD}$  is ON and  $V_{CC}$  is OFF as shown in the dotted line of  $V_{CC}$  in Figure 8-16 and Figure 8-17.

<sup>(2)</sup>  $V_{CC}$  should be kept float (i.e. disable) when it is OFF.

<sup>(3)</sup> Power Pins ( $V_{DD}$ ,  $V_{CC}$ ) can never be pulled to ground under any circumstance.

<sup>(4)</sup> The register values are reset after  $t_1$ .

<sup>(5)</sup>  $V_{DD}$  should not be Power OFF before  $V_{CC}$  Power OFF.

## 9 COMMAND TABLE

**Table 9-1: Command Table**

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

### 1. Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	81 A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	0 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh )
0	A4/A5	1	0	1	0	0	1	0	X <sub>0</sub>	Entire Display ON	A4h, X <sub>0</sub> =0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X <sub>0</sub> =1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X <sub>0</sub>	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AE AF	1	0	1	0	1	1	1	X <sub>0</sub>	Set Display ON/OFF	AEh, X[0]=0b:Display OFF (sleep mode) (RESET) AFh X[0]=1b:Display ON in normal mode

### 2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	26/27	0	0	1	0	0	1	1	X <sub>0</sub>	Continuous Horizontal Scroll	26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll
0	A[7:0]	0	0	0	0	0	0	0	0	Horizontal Scroll (Horizontal scroll by 1 column)	(Horizontal scroll by 1 column)
0	B[2:0]	*	*	*	*	*	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	Setup	A[7:0] : Dummy byte (Set as 00h) B[2:0] : Define start page address
0	C[2:0]	*	*	*	*	*	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		000b – PAGE0   011b – PAGE3   110b – PAGE6 001b – PAGE1   100b – PAGE4   111b – PAGE7 010b – PAGE2   101b – PAGE5
0	D[2:0]	*	*	*	*	*	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 5 frames   100b – 3 frames 001b – 64 frames   101b – 4 frames 010b – 128 frames   110b – 25 frame 011b – 256 frames   111b – 2 frame
0	E[7:0]	0	0	0	0	0	0	0	0	D[2:0] : Define end page address	000b – PAGE0   011b – PAGE3   110b – PAGE6 001b – PAGE1   100b – PAGE4   111b – PAGE7 010b – PAGE2   101b – PAGE5
0	F[7:0]	1	1	1	1	1	1	1	1		The value of D[2:0] must be larger or equal to B[2:0] E[7:0] : Dummy byte (Set as 00h) F[7:0] : Dummy byte (Set as FFh)

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description									
0	29/2A	0	0	1	0	1	0	X <sub>1</sub>	X <sub>0</sub>	Continuous Vertical and Right Horizontal Scroll	29h, X <sub>1</sub> X <sub>0</sub> =01b : Vertical and Right Horizontal Scroll									
0	A[2:0]	0	0	0	0	0	0	0	0	Vertical and Horizontal Scroll	2Ah, X <sub>1</sub> X <sub>0</sub> =10b : Vertical and Left Horizontal Scroll									
0	B[2:0]	*	*	*	*	*	*	B <sub>2</sub>	B <sub>1</sub>	Horizontal Scroll (Horizontal scroll by 1 column)										
0	C[2:0]	*	*	*	*	*	*	C <sub>2</sub>	C <sub>1</sub>	Setup	A[7:0] : Dummy byte									
0	D[2:0]	*	*	*	*	*	*	D <sub>2</sub>	D <sub>1</sub>											
0	E[5:0]	*	*	E <sub>5</sub>	E <sub>4</sub>	E <sub>3</sub>	E <sub>2</sub>	E <sub>1</sub>	E <sub>0</sub>		B[2:0] : Define start page address									
											<table border="1"> <tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr> <tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr> <tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr> </table>	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5	
000b – PAGE0	011b – PAGE3	110b – PAGE6																		
001b – PAGE1	100b – PAGE4	111b – PAGE7																		
010b – PAGE2	101b – PAGE5																			
											C[2:0] : Set time interval between each scroll step in terms of frame frequency									
											<table border="1"> <tr><td>000b – 5 frames</td><td>100b – 3 frames</td></tr> <tr><td>001b – 64 frames</td><td>101b – 4 frames</td></tr> <tr><td>010b – 128 frames</td><td>110b – 25 frame</td></tr> <tr><td>011b – 256 frames</td><td>111b – 2 frame</td></tr> </table>	000b – 5 frames	100b – 3 frames	001b – 64 frames	101b – 4 frames	010b – 128 frames	110b – 25 frame	011b – 256 frames	111b – 2 frame	
000b – 5 frames	100b – 3 frames																			
001b – 64 frames	101b – 4 frames																			
010b – 128 frames	110b – 25 frame																			
011b – 256 frames	111b – 2 frame																			
											D[2:0] : Define end page address									
											<table border="1"> <tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr> <tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr> <tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr> </table>	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5	
000b – PAGE0	011b – PAGE3	110b – PAGE6																		
001b – PAGE1	100b – PAGE4	111b – PAGE7																		
010b – PAGE2	101b – PAGE5																			
											The value of D[2:0] must be larger or equal to B[2:0]									
											E[5:0] : Vertical scrolling offset e.g. E[5:0]=01h refer to offset =1 row E[5:0]=3Fh refer to offset =63 rows									
											<b>Note</b> <sup>(1)</sup> No continuous vertical scrolling is available.									
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	Stop scrolling that is configured by command 26h/27h/29h/2Ah.									
											<b>Note</b> <sup>(1)</sup> After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.									
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences:  Valid command sequence 1: 26h ;2Fh. Valid command sequence 2: 27h ;2Fh. Valid command sequence 3: 29h ;2Fh. Valid command sequence 4: 2Ah ;2Fh.  For example, if “26h; 2Ah; 2Fh.” commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.									

**2. Scrolling Command Table**

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0	A3 A[5:0] B[6:0]	1 * *	0 A <sub>5</sub> B <sub>6</sub>	1 A <sub>4</sub> B <sub>5</sub>	0 A <sub>3</sub> B <sub>4</sub>	0 A <sub>2</sub> B <sub>3</sub>	1 A <sub>1</sub> B <sub>2</sub>	1 A <sub>0</sub> B <sub>1</sub>	1 A <sub>0</sub> B <sub>0</sub>	Set Vertical Scroll Area	<p>A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0). [RESET = 0]</p> <p>B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64]</p> <p><b>Note</b></p> <p>(1) A[5:0]+B[6:0] &lt;= MUX ratio</p> <p>(2) B[6:0] &lt;= MUX ratio</p> <p>(3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) &lt; B[6:0]</p> <p>(3b) Set Display Start Line (X<sub>5</sub>X<sub>4</sub>X<sub>3</sub>X<sub>2</sub>X<sub>1</sub>X<sub>0</sub> of 40h~7Fh) &lt; B[6:0]</p> <p>(4) The last row of the scroll area shifts to the first row of the scroll area.</p> <p>(5) For 64d MUX display</p> <p>A[5:0] = 0, B[6:0]=64 : whole area scrolls</p> <p>A[5:0]=0, B[6:0] &lt; 64 : top area scrolls</p> <p>A[5:0] + B[6:0] &lt; 64 : central area scrolls</p> <p>A[5:0] + B[6:0] = 64 : bottom area scrolls</p>

**3. Addressing Setting Command Table**

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Lower Column Start Address for Page Addressing Mode	<p>Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.</p> <p><b>Note</b></p> <p>(1) This command is only for page addressing mode</p>
0	10~1F	0	0	0	1	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Higher Column Start Address for Page Addressing Mode	<p>Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.</p> <p><b>Note</b></p> <p>(1) This command is only for page addressing mode</p>
0 0	20 A[1:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 * *	0 A <sub>1</sub>	0 A <sub>0</sub>	Set Memory Addressing Mode	<p>A[1:0] = 00b, Horizontal Addressing Mode</p> <p>A[1:0] = 01b, Vertical Addressing Mode</p> <p>A[1:0] = 10b, Page Addressing Mode (RESET)</p> <p>A[1:0] = 11b, Invalid</p>
0 0 0	21 A[6:0] B[6:0]	0 * *	0 A <sub>6</sub> B <sub>6</sub>	1 A <sub>5</sub> B <sub>5</sub>	0 A <sub>4</sub> B <sub>4</sub>	0 A <sub>3</sub> B <sub>3</sub>	0 A <sub>2</sub> B <sub>2</sub>	0 A <sub>1</sub> B <sub>1</sub>	1 A <sub>0</sub> B <sub>0</sub>	Set Column Address	<p>Setup column start and end address</p> <p>A[6:0] : Column start address, range : 0-127d, (RESET=0d)</p> <p>B[6:0]: Column end address, range : 0-127d, (RESET=127d)</p> <p><b>Note</b></p> <p>(1) This command is only for horizontal or vertical addressing mode.</p>

### 3. Addressing Setting Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	22	0	0	1	0	0	0	1	0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d)
0	A[2:0]	*	*	*	*	*	*	A <sub>2</sub>	A <sub>1</sub>		
0	B[2:0]	*	*	*	*	*	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		
										<b>Note</b>	<sup>(1)</sup> This command is only for horizontal or vertical addressing mode.
0	B0~B7	1	0	1	1	0	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0].
										<b>Note</b>	<sup>(1)</sup> This command is only for page addressing mode

### 4. Hardware Configuration (Panel resolution & layout related) Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	40~7F	0	1	X <sub>5</sub>	X <sub>4</sub>	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Display Start Line	Set display RAM display start line register from 0-63 using X <sub>5</sub> X <sub>3</sub> X <sub>2</sub> X <sub>1</sub> X <sub>0</sub> . Display start line register is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X <sub>0</sub>	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0	A8	1	0	1	0	1	0	0	0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET=111111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry.
0	A[5:0]	*	*	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	C0/C8	1	1	0	0	X <sub>3</sub>	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N-1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0	D3	1	1	0	1	0	0	1	1	Set Display Offset	Set vertical shift by COM from 0d~63d The value is reset to 00h after RESET.
0	A[5:0]	*	*	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	DA	1	1	0	A <sub>5</sub>	1	1	0	1	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b(RESET), Alternative COM pin configuration
0	A[5:4]	0	0		A <sub>4</sub>	0	0	1	0		A[5]=0b(RESET), Disable COM Left/Right remap A[5]=1b, Enable COM Left/Right remap

### 5. Timing & Driving Scheme Setting Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	D5 A[7:0]	1 A <sub>7</sub>	1 A <sub>6</sub>	0 A <sub>5</sub>	1 A <sub>4</sub>	0 A <sub>3</sub>	1 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1)  A[7:4] : Set the Oscillator Frequency, Fosc. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1000b Range:0000b~1111b Frequency increases as setting value increases.
0	D9 A[7:0]	1 A <sub>7</sub>	1 A <sub>6</sub>	0 A <sub>5</sub>	1 A <sub>4</sub>	1 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h)  A[7:4] : Phase 2 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h)
0	DB A[6:4]	1 0	1 A <sub>6</sub>	0 A <sub>5</sub>	1 A <sub>4</sub>	1 0	0 0	1 0	1 0	Set V <sub>COMH</sub> Deselect Level	A[6:4] Hex V <sub>COMH</sub> deselect level code 000b 00h ~ 0.65 x V <sub>CC</sub> 010b 20h ~ 0.77 x V <sub>CC</sub> (RESET) 011b 30h ~ 0.83 x V <sub>CC</sub>
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation

#### Note

(1) “\*” stands for “Don’t care”.

**Table 9-2 : Read Command Table**

<b>Bit Pattern</b>	<b>Command</b>	<b>Description</b>
D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub> D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>	Status Register Read	D[7] : Reserved D[6] : “1” for display OFF / “0” for display ON D[5] : Reserved D[4] : Reserved D[3] : Reserved D[2] : Reserved D[1] : Reserved D[0] : Reserved

**Note**

<sup>(1)</sup>Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

**9.1 Data Read / Write**

To read data from the GDDRAM, select HIGH for both the R/W# (WR#) pin and the D/C# pin for 6800-series parallel mode and select LOW for the E (RD#) pin and HIGH for the D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.

In normal data read mode the GDDRAM column address pointer will be increased automatically by one after each data read.

Also, a dummy read is required before the first data read.

To write data to the GDDRAM, select LOW for the R/W# (WR#) pin and HIGH for the D/C# pin for both 6800-series parallel mode and 8080-series parallel mode. The serial interface mode is always in write mode. The GDDRAM column address pointer will be increased automatically by one after each data write.

**Table 9-3 : Address increment table (Automatic)**

<b>D/C#</b>	<b>R/W# (WR#)</b>	<b>Comment</b>	<b>Address Increment</b>
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

## 10 COMMAND DESCRIPTIONS

### 10.1 Fundamental Command

#### 10.1.1 Set Lower Column Start Address for Page Addressing Mode (00h~0Fh)

This command specifies the lower nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Section Table 9-1 and Section 10.1.3 for details.

#### 10.1.2 Set Higher Column Start Address for Page Addressing Mode (10h~1Fh)

This command specifies the higher nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Section Table 9-1 and Section 10.1.3 for details.

#### 10.1.3 Set Memory Addressing Mode (20h)

There are 3 different memory addressing mode in SSD1306: page addressing mode, horizontal addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above three modes. In there, “COL” means the graphic display data RAM column.

##### Page addressing mode (A[1:0]=10xb)

In page addressing mode, after the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is not changed. Users have to set the new page and column addresses in order to access the next page RAM content. The sequence of movement of the PAGE and column address point for page addressing mode is shown in Figure 10-1.

Figure 10-1 : Address Pointer Movement of Page addressing mode

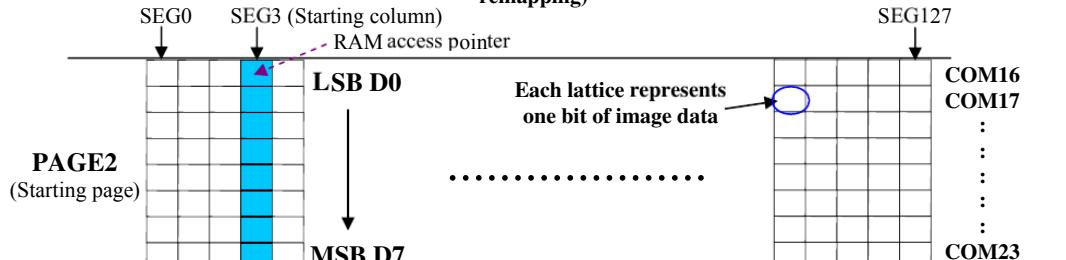
	COL0	COL 1	.....	COL 126	COL 127
PAGE0	→				
PAGE1	→				
:	:	:	:	:	:
PAGE6	→				
PAGE7	→				

In normal display data RAM read or write and page addressing mode, the following steps are required to define the starting RAM access pointer location:

- Set the page start address of the target display location by command B0h to B7h.
- Set the lower start column address of pointer by command 00h~0Fh.
- Set the upper start column address of pointer by command 10h~1Fh.

For example, if the page address is set to B2h, lower column address is 03h and upper column address is 10h, then that means the starting column is SEG3 of PAGE2. The RAM access pointer is located as shown in Figure 10-2. The input data byte will be written into RAM position of column 3.

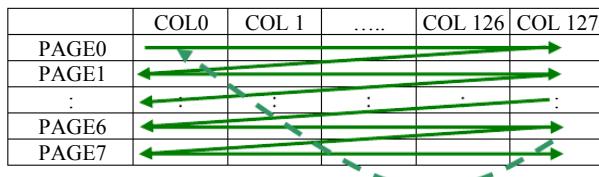
Figure 10-2 : Example of GDDRAM access pointer setting in Page Addressing Mode (No row and column-remapping)



#### Horizontal addressing mode (A[1:0]=00b)

In horizontal addressing mode, after the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is increased by 1. The sequence of movement of the page and column address point for horizontal addressing mode is shown in Figure 10-3. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 10-3.)

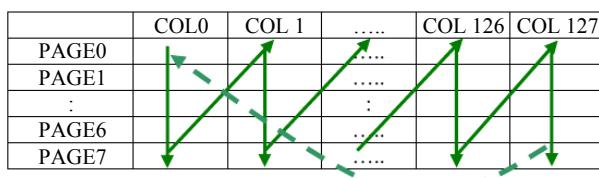
**Figure 10-3 : Address Pointer Movement of Horizontal addressing mode**



#### Vertical addressing mode: (A[1:0]=01b)

In vertical addressing mode, after the display RAM is read/written, the page address pointer is increased automatically by 1. If the page address pointer reaches the page end address, the page address pointer is reset to page start address and column address pointer is increased by 1. The sequence of movement of the page and column address point for vertical addressing mode is shown in Figure 10-4. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 10-4.)

**Figure 10-4 : Address Pointer Movement of Vertical addressing mode**



In normal display data RAM read or write and horizontal / vertical addressing mode, the following steps are required to define the RAM access pointer location:

- Set the column start and end address of the target display location by command 21h.
- Set the page start and end address of the target display location by command 22h.

Example is shown in Figure 10-5.

#### **10.1.4 Set Column Address (21h)**

This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command 20h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

### 10.1.5 Set Page Address (22h)

This triple byte command specifies page start address and end address of the display data RAM. This command also sets the page address pointer to page start address. This pointer is used to define the current read/write page address in graphic display data RAM. If vertical address increment mode is enabled by command 20h, after finishing read/write one page data, it is incremented automatically to the next page address. Whenever the page address pointer finishes accessing the end page address, it is reset back to start page address.

The figure below shows the way of column and page address pointer movement through the example: column start address is set to 2 and column end address is set to 125, page start address is set to 1 and page end address is set to 6; Horizontal address increment mode is enabled by command 20h. In this case, the graphic display data RAM column accessible range is from column 2 to column 125 and from page 1 to page 6 only. In addition, the column address pointer is set to 2 and page address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line* in *Figure 10-5*). Whenever the column address pointer finishes accessing the end column 125, it is reset back to column 2 and page address is automatically increased by 1 (*solid line* in *Figure 10-5*). While the end page 6 and end column 125 RAM location is accessed, the page address is reset back to 1 and the column address is reset back to 2 (*dotted line* in *Figure 10-5*).

**Figure 10-5 : Example of Column and Row Address Pointer Movement**

	Col 0	Col 1	Col 2	.....	.....	Col 125	Col 126	Col 127
PAGE0								
PAGE1								
:								
PAGE6								
PAGE7								

### 10.1.6 Set Display Start Line (40h~7Fh)

This command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 63. With value equal to 0, RAM row 0 is mapped to COM0. With value equal to 1, RAM row 1 is mapped to COM0 and so on.

Refer to Table 10-1 for more illustrations.

### 10.1.7 Set Contrast Control for BANK0 (81h)

This command sets the Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current increases as the contrast step value increases.

### 10.1.8 Set Segment Re-map (A0h/A1h)

This command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design. Please refer to Table 9-1.

This command only affects subsequent data input. Data already stored in GDDRAM will have no changes.

### **10.1.9 Entire Display ON (A4h/A5h)**

A4h command enable display outputs according to the GDDRAM contents.

If A5h command is issued, then by using A4h command, the display will resume to the GDDRAM contents.

In other words, A4h command resumes the display from entire display “ON” stage.

A5h command forces the entire display to be “ON”, regardless of the contents of the display data RAM.

### **10.1.10 Set Normal/Inverse Display (A6h/A7h)**

This command sets the display to be either normal or inverse. In normal display a RAM data of 1 indicates an “ON” pixel while in inverse display a RAM data of 0 indicates an “ON” pixel.

### **10.1.11 Set Multiplex Ratio (A8h)**

This command switches the default 63 multiplex mode to any multiplex ratio, ranging from 16 to 63. The output pads COM0~COM63 will be switched to the corresponding COM signal.

### **10.1.12 Set Display ON/OFF (AEh/AFh)**

These single byte commands are used to turn the OLED panel display ON or OFF.

When the display is ON, the selected circuits by Set Master Configuration command will be turned ON.

When the display is OFF, those circuits will be turned OFF and the segment and common output are in  $V_{SS}$  state and high impedance state, respectively. These commands set the display to one of the two states:

- AEh : Display OFF
- AFh : Display ON

**Figure 10-6 :Transition between different modes**



### **10.1.13 Set Page Start Address for Page Addressing Mode (B0h~B7h)**

This command positions the page start address from 0 to 7 in GDDRAM under Page Addressing Mode. Please refer to Table 9-1 and Section 10.1.3 for details.

### **10.1.14 Set COM Output Scan Direction (C0h/C8h)**

This command sets the scan direction of the COM output, allowing layout flexibility in the OLED module design. Additionally, the display will show once this command is issued. For example, if this command is sent during normal display then the graphic display will be vertically flipped immediately. Please refer to Table 10-3 for details.

### **10.1.15 Set Display Offset (D3h)**

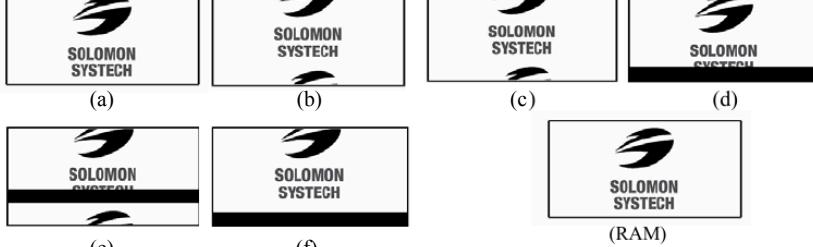
This is a double byte command. The second command specifies the mapping of the display start line to one of COM0~COM63 (assuming that COM0 is the display start line then the display start line register is equal to 0).

For example, to move the COM16 towards the COM0 direction by 16 lines the 6-bit data in the second byte should be given as 010000b. To move in the opposite direction by 16 lines the 6-bit data should be given by  $64 - 16$ , so the second byte would be 100000b. The following two tables (Table 10-1, Table 10-2) show the example of setting the command C0h/C8h and D3h.

**Table 10-1 : Example of Set Display Offset and Display Start Line with no Remap**

Hardware pin name	Output												Set MUX ratio(A8h) [COM Normal / Remapped (C0h / C8h)]	
	64		64		64		56		56		56			
	Normal													
0	0	8	0	8	0	8	0	8	0	8	0	8	Display offset (D3h)	
COM0	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row0	RAM0	Row8	RAM8	Row0	RAM8	Display start line (40h - 7Fh)	
COM1	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row1	RAM1	Row9	RAM9	Row1	RAM9		
COM2	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row2	RAM2	Row10	RAM10	Row2	RAM10		
COM3	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row3	RAM3	Row11	RAM11	Row3	RAM11		
COM4	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row4	RAM4	Row12	RAM12	Row4	RAM12		
COM5	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row5	RAM5	Row13	RAM13	Row5	RAM5		
COM6	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row6	RAM6	Row14	RAM14	Row6	RAM14		
COM7	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row7	RAM7	Row15	RAM15	Row7	RAM15		
COM8	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row8	RAM8	Row16	RAM16	Row8	RAM16		
COM9	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row9	RAM9	Row17	RAM17	Row9	RAM17		
COM10	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row10	RAM10	Row18	RAM18	Row10	RAM18		
COM11	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row11	RAM11	Row19	RAM19	Row11	RAM19		
COM12	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row12	RAM12	Row20	RAM20	Row12	RAM20		
COM13	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row13	RAM13	Row21	RAM21	Row13	RAM21		
COM14	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row14	RAM14	Row22	RAM22	Row14	RAM22		
COM15	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row15	RAM15	Row23	RAM23	Row15	RAM23		
COM16	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row16	RAM16	Row24	RAM24	Row16	RAM24		
COM17	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row17	RAM17	Row25	RAM25	Row17	RAM25		
COM18	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row18	RAM18	Row26	RAM26	Row18	RAM26		
COM19	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row19	RAM19	Row27	RAM27	Row19	RAM27		
COM20	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row20	RAM20	Row28	RAM28	Row20	RAM28		
COM21	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row21	RAM21	Row29	RAM29	Row21	RAM29		
COM22	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row22	RAM22	Row30	RAM30	Row22	RAM30		
COM23	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row23	RAM23	Row31	RAM31	Row23	RAM31		
COM24	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row24	RAM24	Row32	RAM32	Row24	RAM32		
COM25	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row25	RAM25	Row33	RAM33	Row25	RAM33		
COM26	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row26	RAM26	Row34	RAM34	Row26	RAM34		
COM27	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row27	RAM27	Row35	RAM35	Row27	RAM35		
COM28	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row28	RAM28	Row36	RAM36	Row28	RAM36		
COM29	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row29	RAM29	Row37	RAM37	Row29	RAM37		
COM30	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row30	RAM30	Row38	RAM38	Row30	RAM38		
COM31	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row31	RAM31	Row39	RAM39	Row31	RAM39		
COM32	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row32	RAM32	Row40	RAM40	Row32	RAM40		
COM33	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row33	RAM33	Row41	RAM41	Row33	RAM41		
COM34	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row34	RAM34	Row42	RAM42	Row34	RAM42		
COM35	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row35	RAM35	Row43	RAM43	Row35	RAM43		
COM36	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row36	RAM36	Row44	RAM44	Row36	RAM44		
COM37	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row37	RAM37	Row45	RAM45	Row37	RAM45		
COM38	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row38	RAM46	Row46	RAM46	Row38	RAM46		
COM39	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row39	RAM39	Row47	RAM47	Row39	RAM47		
COM40	Row40	RAM40	Row48	RAM48	Row40	RAM48	Row40	RAM40	Row48	RAM48	Row40	RAM48		
COM41	Row41	RAM41	Row49	RAM49	Row41	RAM49	Row41	RAM41	Row49	RAM49	Row41	RAM49		
COM42	Row42	RAM42	Row50	RAM50	Row42	RAM50	Row42	RAM42	Row50	RAM50	Row42	RAM50		
COM43	Row43	RAM43	Row51	RAM51	Row43	RAM51	Row43	RAM43	Row51	RAM51	Row43	RAM51		
COM44	Row44	RAM44	Row52	RAM52	Row44	RAM52	Row44	RAM44	Row52	RAM52	Row44	RAM52		
COM45	Row45	RAM45	Row53	RAM53	Row45	RAM53	Row45	RAM45	Row53	RAM53	Row45	RAM53		
COM46	Row46	RAM46	Row54	RAM54	Row46	RAM54	Row46	RAM46	Row54	RAM54	Row46	RAM54		
COM47	Row47	RAM47	Row55	RAM55	Row47	RAM55	Row47	RAM47	Row55	RAM55	Row47	RAM55		
COM48	Row48	RAM48	Row56	RAM56	Row48	RAM56	Row48	RAM48	-	-	Row48	RAM56		
COM49	Row49	RAM49	Row57	RAM57	Row49	RAM57	Row49	RAM49	-	-	Row49	RAM57		
COM50	Row50	RAM50	Row58	RAM58	Row50	RAM58	Row50	RAM50	-	-	Row50	RAM58		
COM51	Row51	RAM51	Row59	RAM59	Row51	RAM59	Row51	RAM51	-	-	Row51	RAM59		
COM52	Row52	RAM52	Row60	RAM60	Row52	RAM60	Row52	RAM52	-	-	Row52	RAM60		
COM53	Row53	RAM53	Row61	RAM61	Row53	RAM61	Row53	RAM53	-	-	Row53	RAM61		
COM54	Row54	RAM54	Row62	RAM62	Row54	RAM62	Row54	RAM54	-	-	Row54	RAM62		
COM55	Row55	RAM55	Row63	RAM63	Row55	RAM63	Row55	RAM55	-	-	Row55	RAM63		
COM56	Row56	RAM56	Row64	RAM64	Row56	RAM64	Row56	RAM56	-	-	Row56	RAM64		
COM57	Row57	RAM57	Row65	RAM65	Row57	RAM65	Row57	RAM57	-	-	Row57	RAM65		
COM58	Row58	RAM58	Row66	RAM66	Row58	RAM66	Row58	RAM58	-	-	Row58	RAM66		
COM59	Row59	RAM59	Row67	RAM67	Row59	RAM67	Row59	RAM59	-	-	Row59	RAM67		
COM60	Row60	RAM60	Row68	RAM68	Row60	RAM68	Row60	RAM60	-	-	Row60	RAM68		
COM61	Row61	RAM61	Row69	RAM69	Row61	RAM69	Row61	RAM61	-	-	Row61	RAM69		
COM62	Row62	RAM62	Row70	RAM70	Row62	RAM70	Row62	RAM62	-	-	Row62	RAM70		
COM63	Row63	RAM63	Row71	RAM71	Row63	RAM71	Row63	RAM63	-	-	Row63	RAM71		

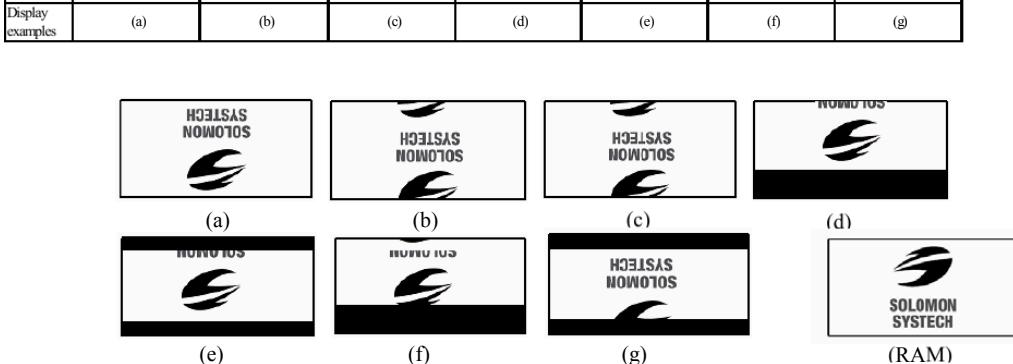
Display examples (a) (b) (c) (d) (e) (f)



(RAM)

**Table 10-2 :Example of Set Display Offset and Display Start Line with Remap**

Hardware pin name	Output								Set MUX ratio(A8h) COM Normal / Remapped (C0h / C8h)	
	64		64		48		48			
	Remap	Remap	Remap	Remap	Remap	Remap	Remap	Remap		
	0	8	0	0	8	0	8	16	Display offset (D3h) Display start line (40h - 7Fh)	
COM0	Row63	HAM63	Row7	HAM7	Row63	HAM7	Row47	HAM47	-	
COM1	Row62	HAM62	Row6	HAM6	Row62	HAM6	Row46	HAM46	-	
COM2	Row61	HAM61	Row5	HAM5	Row61	HAM5	Row45	HAM45	-	
COM3	Row60	HAM60	Row4	HAM4	Row60	HAM4	Row44	HAM44	-	
COM4	Row59	HAM59	Row3	HAM3	Row59	HAM3	Row43	HAM51	-	
COM5	Row58	HAM58	Row2	HAM2	Row58	HAM2	Row42	HAM50	-	
COM6	Row57	HAM57	Row1	HAM1	Row57	HAM1	Row41	HAM49	-	
COM7	Row56	HAM56	Row0	HAM0	Row56	HAM0	Row40	HAM48	-	
COM8	Row55	HAM55	Row63	HAM63	Row55	HAM59	Row47	HAM47	Row53 / HAM63	
COM9	Row54	HAM54	Row62	HAM62	Row54	HAM58	Row46	HAM46	Row52 / HAM62	
COM10	Row53	HAM53	Row61	HAM61	Row53	HAM57	Row45	HAM45	Row51 / HAM61	
COM11	Row52	HAM52	Row60	HAM60	Row52	HAM56	Row44	HAM44	Row50 / HAM60	
COM12	Row51	HAM51	Row59	HAM59	Row51	HAM55	Row43	HAM43	Row49 / HAM59	
COM13	Row50	HAM50	Row58	HAM58	Row50	HAM54	Row42	HAM42	Row48 / HAM58	
COM14	Row49	HAM49	Row57	HAM57	Row49	HAM57	Row41	HAM41	Row47 / HAM57	
COM15	Row48	HAM48	Row56	HAM56	Row48	HAM56	Row40	HAM40	Row46 / HAM56	
COM16	Row47	HAM47	Row55	HAM55	Row47	HAM52	Row39	HAM39	Row45 / HAM55	
COM17	Row46	HAM46	Row54	HAM54	Row46	HAM50	Row38	HAM38	Row44 / HAM54	
COM18	Row45	HAM45	Row53	HAM53	Row45	HAM49	Row37	HAM37	Row43 / HAM53	
COM19	Row44	HAM44	Row52	HAM52	Row44	HAM48	Row36	HAM36	Row42 / HAM52	
COM20	Row43	HAM43	Row51	HAM51	Row43	HAM47	Row35	HAM35	Row41 / HAM51	
COM21	Row42	HAM42	Row50	HAM50	Row42	HAM46	Row34	HAM34	Row39 / HAM50	
COM22	Row41	HAM41	Row49	HAM49	Row41	HAM49	Row33	HAM33	Row38 / HAM49	
COM23	Row40	HAM40	Row48	HAM48	Row40	HAM48	Row32	HAM32	Row37 / HAM48	
COM24	Row39	HAM39	Row47	HAM47	Row39	HAM47	Row31	HAM31	Row36 / HAM47	
COM25	Row38	HAM38	Row46	HAM46	Row38	HAM46	Row30	HAM30	Row35 / HAM46	
COM26	Row37	HAM37	Row45	HAM45	Row37	HAM45	Row29	HAM29	Row34 / HAM45	
COM27	Row36	HAM36	Row44	HAM44	Row36	HAM44	Row28	HAM28	Row33 / HAM44	
COM28	Row35	HAM35	Row43	HAM43	Row35	HAM43	Row27	HAM27	Row32 / HAM43	
COM29	Row34	HAM34	Row42	HAM42	Row34	HAM42	Row26	HAM26	Row31 / HAM42	
COM30	Row33	HAM33	Row41	HAM41	Row33	HAM41	Row25	HAM25	Row30 / HAM41	
COM31	Row32	HAM32	Row40	HAM40	Row32	HAM40	Row16	HAM16	Row24 / HAM40	
COM32	Row31	HAM31	Row39	HAM39	Row31	HAM39	Row15	HAM15	Row23 / HAM39	
COM33	Row30	HAM30	Row38	HAM38	Row30	HAM38	Row14	HAM14	Row22 / HAM38	
COM34	Row29	HAM29	Row37	HAM37	Row29	HAM37	Row13	HAM13	Row21 / HAM37	
COM35	Row28	HAM28	Row36	HAM36	Row28	HAM36	Row12	HAM12	Row20 / HAM36	
COM36	Row27	HAM27	Row26	HAM26	Row27	HAM26	Row11	HAM11	Row19 / HAM26	
COM37	Row26	HAM26	Row25	HAM25	Row26	HAM25	Row10	HAM10	Row18 / HAM25	
COM38	Row25	HAM25	Row23	HAM23	Row25	HAM23	Row7	HAM7	Row17 / HAM23	
COM39	Row24	HAM24	Row22	HAM22	Row24	HAM22	Row6	HAM6	Row16 / HAM22	
COM40	Row23	HAM23	Row21	HAM21	Row23	HAM21	Row5	HAM5	Row15 / HAM21	
COM41	Row22	HAM22	Row20	HAM20	Row22	HAM20	Row4	HAM4	Row14 / HAM20	
COM42	Row21	HAM21	Row19	HAM19	Row21	HAM19	Row3	HAM3	Row13 / HAM19	
COM43	Row20	HAM20	Row18	HAM18	Row20	HAM18	Row2	HAM2	Row12 / HAM18	
COM44	Row19	HAM19	Row17	HAM17	Row19	HAM17	Row1	HAM1	Row11 / HAM17	
COM45	Row18	HAM18	Row16	HAM16	Row18	HAM16	Row0	HAM0	Row10 / HAM16	
COM46	Row17	HAM17	Row15	HAM15	Row17	HAM15				
COM47	Row16	HAM16	Row14	HAM14	Row16	HAM14				
COM48	Row15	HAM15	Row13	HAM13	Row15	HAM13				
COM49	Row14	HAM14	Row12	HAM12	Row14	HAM12				
COM50	Row13	HAM13	Row11	HAM11	Row13	HAM11				
COM51	Row12	HAM12	Row10	HAM10	Row12	HAM10				
COM52	Row11	HAM11	Row9	HAM9	Row11	HAM9				
COM53	Row10	HAM10	Row8	HAM8	Row10	HAM8				
COM54	Row9	HAM9	Row7	HAM7	Row9	HAM7				
COM55	Row8	HAM8	Row6	HAM6	Row8	HAM6				
COM56	Row7	HAM7	Row5	HAM5	Row7	HAM5				
COM57	Row6	HAM6	Row4	HAM4	Row6	HAM4				
COM58	Row5	HAM5	Row3	HAM3	Row5	HAM3				
COM59	Row4	HAM4	Row2	HAM2	Row4	HAM2				
COM60	Row3	HAM3	Row1	HAM1	Row3	HAM1				
COM61	Row2	HAM2	Row0	HAM0	Row2	HAM0				
COM62	Row1	HAM1	Row9	HAM9	Row1	HAM9				
COM63	Row0	HAM0	Row8	HAM8	Row0	HAM8				



### 10.1.16 Set Display Clock Divide Ratio/ Oscillator Frequency (D5h)

This command consists of two functions:

- Display Clock Divide Ratio (D)(A[3:0])

Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 1. Please refer to section 8.3 for the details relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])

Program the oscillator frequency Fosc that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings available as shown below. The default setting is 1000b.

### 10.1.17 Set Pre-charge Period (D9h)

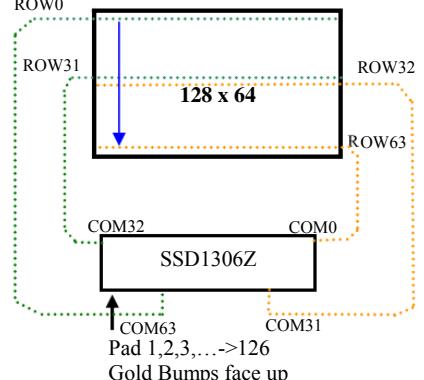
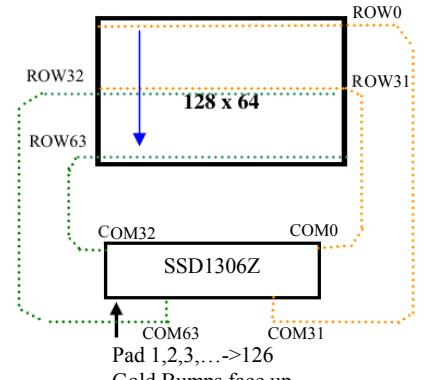
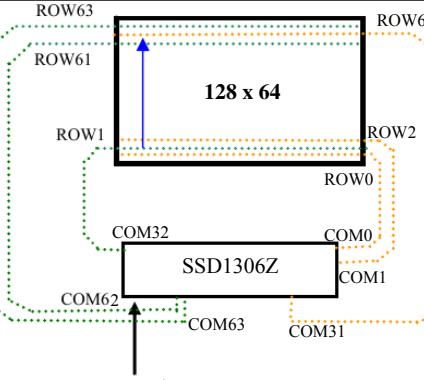
This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK, where RESET equals 2 DCLKs.

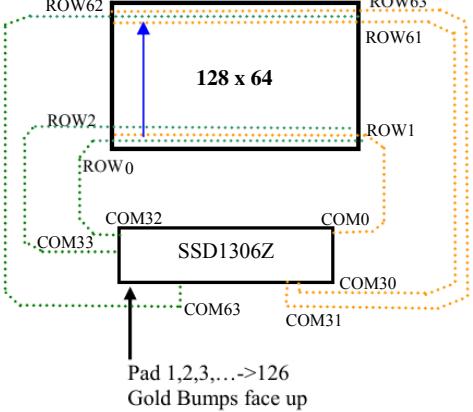
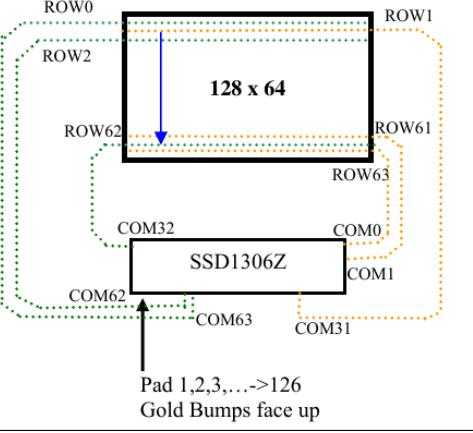
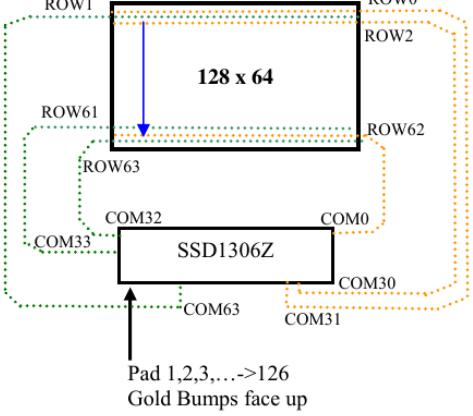
### 10.1.18 Set COM Pins Hardware Configuration (DAh)

This command sets the COM signals pin configuration to match the OLED panel hardware layout. The table below shows the COM pin configuration under different conditions (for MUX ratio =64):

Table 10-3 : COM Pins Hardware Configuration

Conditions	COM pins Configurations
1 Sequential COM pin configuration (DAh A[4]=0) COM output Scan direction: from COM0 to COM63 (C0h) Disable COM Left/Right remap (DAh A[5]=0)	
2 Sequential COM pin configuration (DAh A[4]=0) COM output Scan direction: from COM0 to COM63 (C0h) Enable COM Left/Right remap (DAh A[5]=1)	

Conditions	COM pins Configurations
3 Sequential COM pin configuration (DAh A[4] =0) COM output Scan direction: from COM63 to COM0 (C8h) Disable COM Left/Right remap (DAh A[5] =0)	 <p>128 x 64</p> <p>ROW0 ROW1 ROW2 ROW3 ROW4 ROW5 ROW6 ROW7 ROW8 ROW9 ROW10 ROW11 ROW12 ROW13 ROW14 ROW15 ROW16 ROW17 ROW18 ROW19 ROW20 ROW21 ROW22 ROW23 ROW24 ROW25 ROW26 ROW27 ROW28 ROW29 ROW30 ROW31</p> <p>ROW32 ROW33 ROW34 ROW35 ROW36 ROW37 ROW38 ROW39 ROW40 ROW41 ROW42 ROW43 ROW44 ROW45 ROW46 ROW47 ROW48 ROW49 ROW50 ROW51 ROW52 ROW53 ROW54 ROW55 ROW56 ROW57 ROW58 ROW59 ROW60 ROW61 ROW62 ROW63</p> <p>COM32 COM0</p> <p>SSD1306Z</p> <p>COM63 Pad 1,2,3,...&gt;126 Gold Bumps face up</p>
4 Sequential COM pin configuration (DAh A[4] =0) COM output Scan direction: from COM63 to COM0 (C8h) Enable COM Left/Right remap (DAh A[5] =1)	 <p>128 x 64</p> <p>ROW0 ROW1 ROW2 ROW3 ROW4 ROW5 ROW6 ROW7 ROW8 ROW9 ROW10 ROW11 ROW12 ROW13 ROW14 ROW15 ROW16 ROW17 ROW18 ROW19 ROW20 ROW21 ROW22 ROW23 ROW24 ROW25 ROW26 ROW27 ROW28 ROW29 ROW30 ROW31</p> <p>ROW32 ROW33 ROW34 ROW35 ROW36 ROW37 ROW38 ROW39 ROW40 ROW41 ROW42 ROW43 ROW44 ROW45 ROW46 ROW47 ROW48 ROW49 ROW50 ROW51 ROW52 ROW53 ROW54 ROW55 ROW56 ROW57 ROW58 ROW59 ROW60 ROW61 ROW62 ROW63</p> <p>COM32 COM0</p> <p>SSD1306Z</p> <p>COM63 Pad 1,2,3,...&gt;126 Gold Bumps face up</p>
5 Alternative COM pin configuration (DAh A[4] =1) COM output Scan direction: from COM0 to COM63 (C0h) Disable COM Left/Right remap (DAh A[5] =0)	 <p>128 x 64</p> <p>ROW63 ROW62 ROW61 ROW60 ROW59 ROW58 ROW57 ROW56 ROW55 ROW54 ROW53 ROW52 ROW51 ROW50 ROW49 ROW48 ROW47 ROW46 ROW45 ROW44 ROW43 ROW42 ROW41 ROW40 ROW39 ROW38 ROW37 ROW36 ROW35 ROW34 ROW33 ROW32 ROW31 ROW30 ROW29 ROW28 ROW27 ROW26 ROW25 ROW24 ROW23 ROW22 ROW21 ROW20 ROW19 ROW18 ROW17 ROW16 ROW15 ROW14 ROW13 ROW12 ROW11 ROW10 ROW9 ROW8 ROW7 ROW6 ROW5 ROW4 ROW3 ROW2 ROW1 ROW0</p> <p>COM32 COM62 COM0 COM1</p> <p>SSD1306Z</p> <p>COM63 Pad 1,2,3,...&gt;126 Gold Bumps face up</p>

Conditions	COM pins Configurations
6 Alternative COM pin configuration (DAh A[4] =1) COM output Scan direction: from COM0 to COM63 (C0h) Enable COM Left/Right remap (DAh A[5] =1)	
7 Alternative COM pin configuration (DAh A[4] =1) COM output Scan direction: from COM63 to COM0(C8h) Disable COM Left/Right remap (DAh A[5] =0)	
8 Alternative COM pin configuration (DAh A[4] =1) COM output Scan direction: from COM63 to COM0(C8h) Enable COM Left/Right remap (DAh A[5] =1)	

### **10.1.19 Set V<sub>COMH</sub> Deselect Level (DBh)**

This command adjusts the V<sub>COMH</sub> regulator output.

### **10.1.20 NOP (E3h)**

No Operation Command

### **10.1.21 Status register Read**

This command is issued by setting D/C# ON LOW during a data read (See Figure 13-1 to Figure 13-2 for parallel interface waveform). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

## 10.2 Graphic Acceleration Command

### 10.2.1 Horizontal Scroll Setup (26h/27h)

This command consists of consecutive bytes to set up the horizontal scroll parameters and determines the scrolling start page, end page and scrolling speed.

Before issuing this command the horizontal scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted.

The SSD1306 horizontal scroll is designed for 128 columns scrolling. The following two figures (Figure 10-7, Figure 10-8, Figure 10-9) show the examples of using the horizontal scroll:

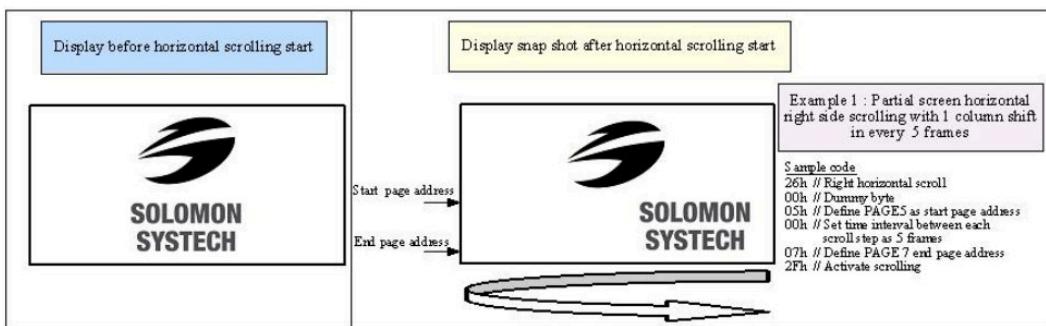
**Figure 10-7 : Horizontal scroll example: Scroll RIGHT by 1 column**

Original Setting	SEG0															
After one scroll step	SEG127															

**Figure 10-8 : Horizontal scroll example: Scroll LEFT by 1 column**

Original Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15
After one scroll step	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16

**Figure 10-9 : Horizontal scrolling setup example**



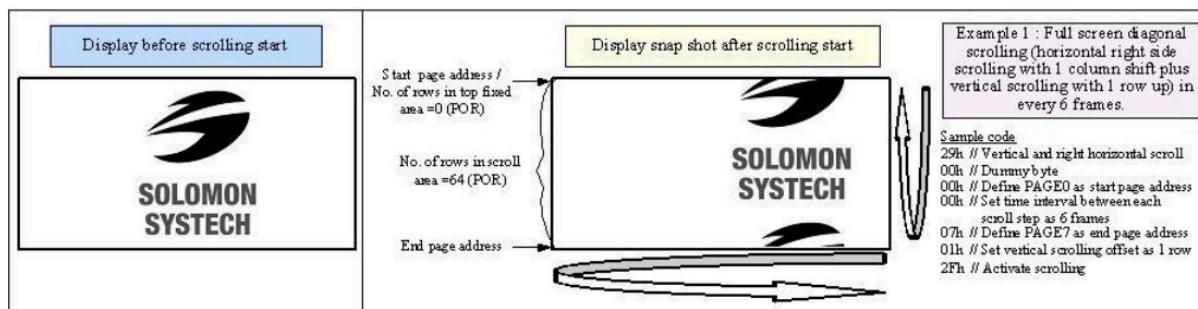
### 10.2.2 Continuous Vertical and Horizontal Scroll Setup (29h/2Ah)

This command consists of 6 consecutive bytes to set up the continuous vertical scroll parameters and determines the scrolling start page, end page, scrolling speed and vertical scrolling offset.

The bytes B[2:0], C[2:0] and D[2:0] of command 29h/2Ah are for the setting of the continuous horizontal scrolling. The byte E[5:0] is for the setting of the continuous vertical scrolling offset. All these bytes together are for the setting of continuous diagonal (horizontal + vertical) scrolling. If the vertical scrolling offset byte E[5:0] is set to zero, then only horizontal scrolling is performed (like command 26/27h).

Before issuing this command the scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted. The following figure (Figure 10-10 ) show the example of using the continuous vertical and horizontal scroll:

Figure 10-10 : Continuous Vertical and Horizontal scrolling setup example



### **10.2.3 Deactivate Scroll (2Eh)**

This command stops the motion of scrolling. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

### **10.2.4 Activate Scroll (2Fh)**

This command starts the motion of scrolling and should only be issued after the scroll setup parameters have been defined by the scrolling setup commands :26h/27h/29h/2Ah . The setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.

The following actions are prohibited after the scrolling is activated

1. RAM access (Data write or read)
2. Changing the horizontal scroll setup parameters

### **10.2.5 Set Vertical Scroll Area(A3h)**

This command consists of 3 consecutive bytes to set up the vertical scroll area. For the continuous vertical scroll function (command 29/2Ah), the number of rows that in vertical scrolling can be set smaller or equal to the MUX ratio.

## 11 MAXIMUM RATINGS

Table 11-1 : Maximum Ratings (Voltage Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	Supply Voltage	-0.3 to +4	V
V <sub>CC</sub>		0 to 16	V
V <sub>SEG</sub>	SEG output voltage	0 to V <sub>CC</sub>	V
V <sub>COM</sub>	COM output voltage	0 to 0.9*V <sub>CC</sub>	V
V <sub>in</sub>	Input voltage	V <sub>SS</sub> -0.3 to V <sub>DD</sub> +0.3	V
T <sub>A</sub>	Operating Temperature	-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

## 12 DC CHARACTERISTICS

### Condition (Unless otherwise specified):

Voltage referenced to V<sub>SS</sub>

V<sub>DD</sub> = 1.65 to 3.3V

T<sub>A</sub> = 25°C

**Table 12-1 : DC Characteristics**

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V <sub>CC</sub>	Operating Voltage	-	7	-	15	V
V <sub>DD</sub>	Logic Supply Voltage	-	1.65	-	3.3	V
V <sub>OH</sub>	High Logic Output Level	I <sub>OUT</sub> = 100uA, 3.3MHz	0.9 x V <sub>DD</sub>	-	-	V
V <sub>OL</sub>	Low Logic Output Level	I <sub>OUT</sub> = 100uA, 3.3MHz	-	-	0.1 x V <sub>DD</sub>	V
V <sub>IH</sub>	High Logic Input Level	-	0.8 x V <sub>DD</sub>	-	-	V
V <sub>IL</sub>	Low Logic Input Level	-	-	-	0.2 x V <sub>DD</sub>	V
I <sub>CC, SLEEP</sub>	I <sub>CC</sub> , Sleep mode Current	V <sub>DD</sub> = 1.65V~3.3V, V <sub>CC</sub> = 7V~15V Display OFF, No panel attached	-	-	10	uA
I <sub>DD, SLEEP</sub>	I <sub>DD</sub> , Sleep mode Current	V <sub>DD</sub> = 1.65V~3.3V, V <sub>CC</sub> = 7V~15V Display OFF, No panel attached	-	-	10	uA
I <sub>CC</sub>	V <sub>CC</sub> Supply Current V <sub>DD</sub> = 2.8V, V <sub>CC</sub> = 12V, I <sub>REF</sub> = 12.5uA No loading, Display ON, All ON	Contrast = FFh	-	430	780	uA
I <sub>DD</sub>	V <sub>DD</sub> Supply Current V <sub>DD</sub> = 2.8V, V <sub>CC</sub> = 12V, I <sub>REF</sub> = 12.5uA No loading, Display ON, All ON		-	50	150	uA
I <sub>SEG</sub>	Segment Output Current V <sub>DD</sub> =2.8V, V <sub>CC</sub> =12V, I <sub>REF</sub> =12.5uA, Display ON.	Contrast=FFh Contrast=AFh Contrast=3Fh	-	100 69 25	-	uA
Dev	Segment output current uniformity	Dev = (I <sub>SEG</sub> - I <sub>MID</sub> ) / I <sub>MID</sub> I <sub>MID</sub> = (I <sub>MAX</sub> + I <sub>MIN</sub> ) / 2 I <sub>SEG[0:131]</sub> = Segment current at contrast = FFh	-3	-	+3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n] - I[n+1]) / (I[n] + I[n+1])	-2	-	+2	%

## 13 AC CHARACTERISTICS

### Conditions:

Voltage referenced to V<sub>SS</sub>  
V<sub>DD</sub>=1.65 to 3.3V  
T<sub>A</sub> = 25°C

Table 13-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
FOSC <sup>(1)</sup>	Oscillation Frequency of Display Timing Generator	V <sub>DD</sub> = 2.8V	333	370	407	kHz
FFRM	Frame Frequency for 64 MUX Mode	128x64 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F <sub>Osc</sub> x 1/(DxKx64) <sup>(2)</sup>	-	Hz
RES#	Reset low pulse width		3	-	-	us

### Note

<sup>(1)</sup> Fosc stands for the frequency value of the internal oscillator and the value is measured when command D5h A[7:4] is in default value.

<sup>(2)</sup> D: divide ratio (default value = 1)

K: number of display clocks (default value = 54)

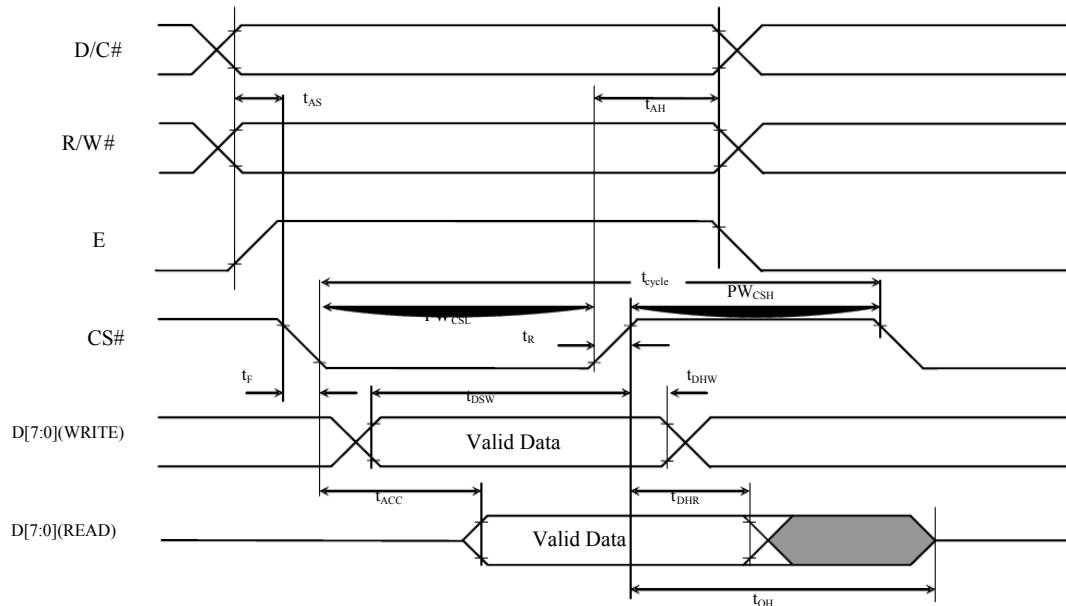
Please refer to Table 9-1 (Set Display Clock Divide Ratio/Oscillator Frequency, D5h) for detailed description

**Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics**

( $V_{DD} - V_{SS} = 1.65V$  to  $3.3V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	0	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	7	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$PW_{CSL}$	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60	-	-	
$PW_{CSH}$	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	
$t_R$	Rise Time	-	-	40	ns
$t_F$	Fall Time	-	-	40	ns

**Figure 13-1 : 6800-series MCU parallel interface characteristics**

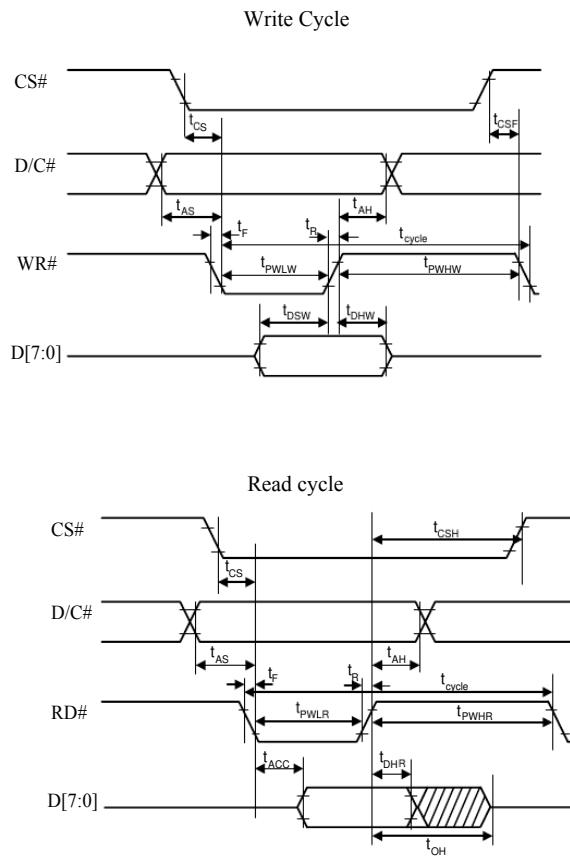


**Table 13-3 : 8080-Series MCU Parallel Interface Timing Characteristics**

( $V_{DD} - V_{SS} = 1.65V$  to  $3.3V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	10	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	7	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$t_{PWLR}$	Read Low Time	120	-	-	ns
$t_{PWLW}$	Write Low Time	60	-	-	ns
$t_{PWHR}$	Read High Time	60	-	-	ns
$t_{PWHW}$	Write High Time	60	-	-	ns
$t_R$	Rise Time	-	-	40	ns
$t_F$	Fall Time	-	-	40	ns
$t_{CS}$	Chip select setup time	0	-	-	ns
$t_{CSH}$	Chip select hold time to read signal	0	-	-	ns
$t_{CSF}$	Chip select hold time	20	-	-	ns

**Figure 13-2 : 8080-series parallel interface characteristics**

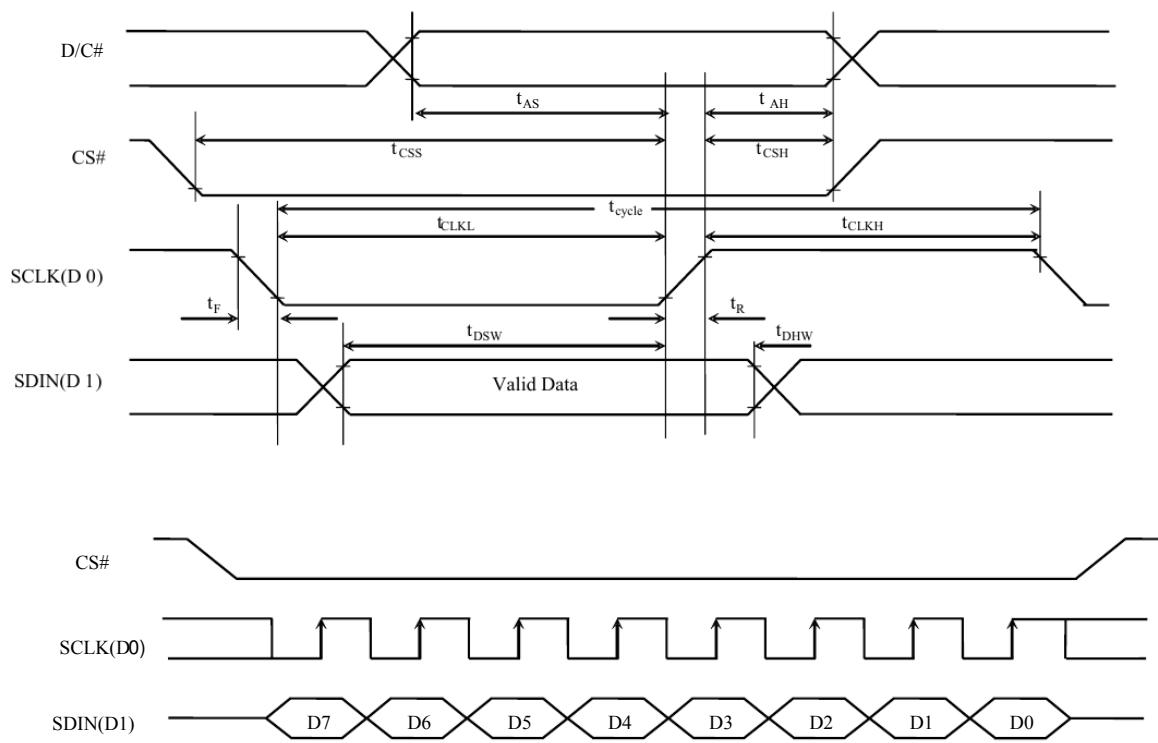


**Table 13-4 : 4-wire Serial Interface Timing Characteristics**

( $V_{DD} - V_{SS} = 1.65V$  to  $3.3V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	100	-	-	ns
$t_{AS}$	Address Setup Time	15	-	-	ns
$t_{AH}$	Address Hold Time	15	-	-	ns
$t_{CSS}$	Chip Select Setup Time	20	-	-	ns
$t_{CSH}$	Chip Select Hold Time	10	-	-	ns
$t_{DSW}$	Write Data Setup Time	15	-	-	ns
$t_{DHW}$	Write Data Hold Time	15	-	-	ns
$t_{CLKL}$	Clock Low Time	20	-	-	ns
$t_{CLKH}$	Clock High Time	20	-	-	ns
$t_R$	Rise Time	-	-	40	ns
$t_F$	Fall Time	-	-	40	ns

**Figure 13-3 : 4-wire Serial interface characteristics**

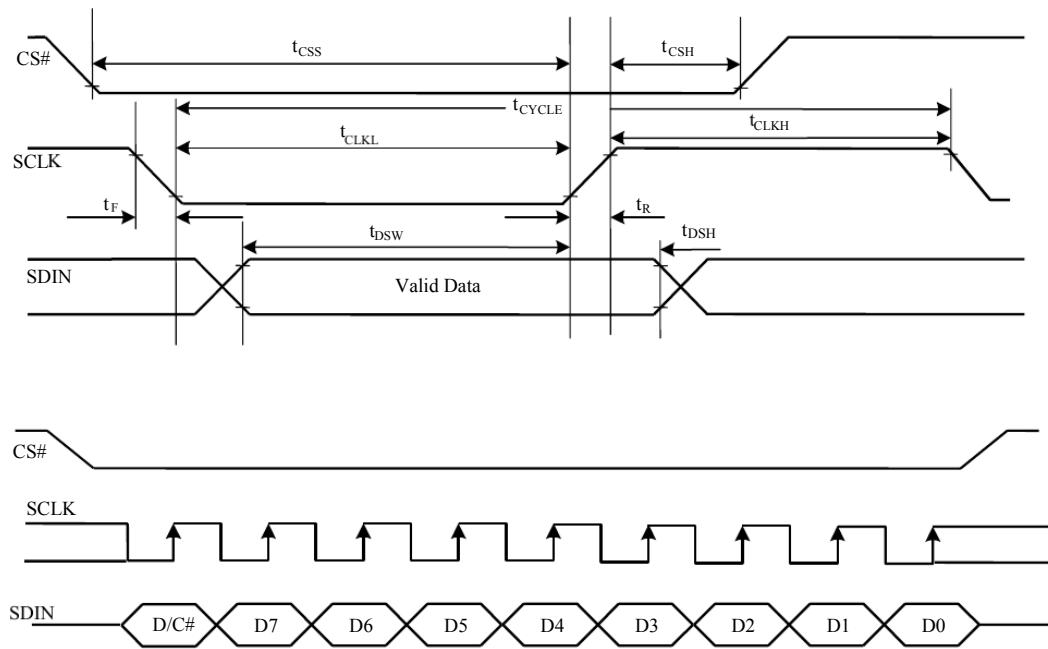


**Table 13-5 : 3-wire Serial Interface Timing Characteristics**

( $V_{DD} - V_{SS} = 1.65V$  to  $3.3V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	100	-	-	ns
$t_{CSS}$	Chip Select Setup Time	20	-	-	ns
$t_{CSH}$	Chip Select Hold Time	10	-	-	ns
$t_{DSW}$	Write Data Setup Time	15	-	-	ns
$t_{DHW}$	Write Data Hold Time	15	-	-	ns
$t_{CLKL}$	Clock Low Time	20	-	-	ns
$t_{CLKH}$	Clock High Time	20	-	-	ns
$t_R$	Rise Time	-	-	40	ns
$t_F$	Fall Time	-	-	40	ns

**Figure 13-4 : 3-wire Serial interface characteristics**

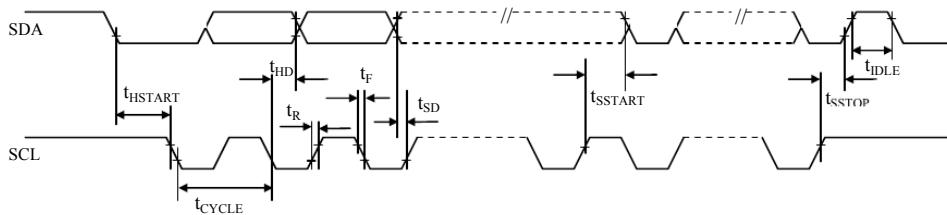


**Conditions:**

$V_{DD} - V_{SS} = V_{DD} - V_{SS} = 1.65V$  to  $3.3V$   
 $T_A = 25^\circ C$

**Table 13-6 :I<sup>2</sup>C Interface Timing Characteristics**

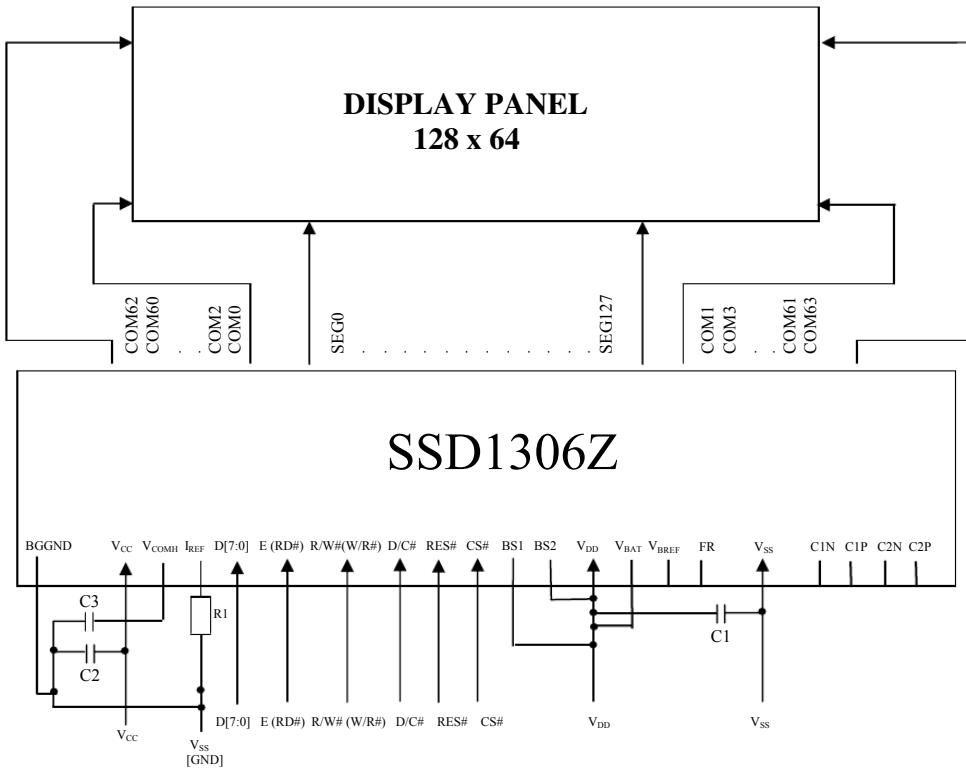
Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	2.5	-	-	us
$t_{HSTART}$	Start condition Hold Time	0.6	-	-	us
$t_{HD}$	Data Hold Time (for "SDA <sub>OUT</sub> " pin)	0	-	-	ns
	Data Hold Time (for "SDA <sub>IN</sub> " pin)	300	-	-	ns
$t_{SD}$	Data Setup Time	100	-	-	ns
$t_{SSTART}$	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
$t_{STOP}$	Stop condition Setup Time	0.6	-	-	us
$t_R$	Rise Time for data and clock pin	-	-	300	ns
$t_F$	Fall Time for data and clock pin	-	-	300	ns
$t_{IDLE}$	Idle Time before a new transmission can start	1.3	-	-	us

**Figure 13-5 : I<sup>2</sup>C interface Timing characteristics**

## 14 Application Example

Figure 14-1 : Application Example of SSD1306Z

The configuration for 8080-parallel interface mode is shown in the following diagram:  
 $(V_{DD}=2.8V, V_{CC}=12V, I_{REF}=12.5\mu A)$



Pin connected to MCU interface: D[7:0], E, R/W#, D/C#, CS#, RES#

Pin internally connected to V<sub>SS</sub>: BS0, CL

Pin internally connected to V<sub>DD</sub>: CLS

C2P, C2N, C1P, C1N, V<sub>BREF</sub>, FB should be left open.

C1: 1.0uF <sup>(1)</sup>

C2: 2.2uF <sup>(1)</sup>

C3: 2.2uF <sup>(1)</sup>

Voltage at I<sub>REF</sub> = V<sub>CC</sub> - 2.5V. For V<sub>CC</sub> = 12V, I<sub>REF</sub> = 12.5uA:

$$\begin{aligned} R1 &= (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF} \\ &= (12 - 2.5) / 12.5\mu A \\ &= 760K\Omega \end{aligned}$$

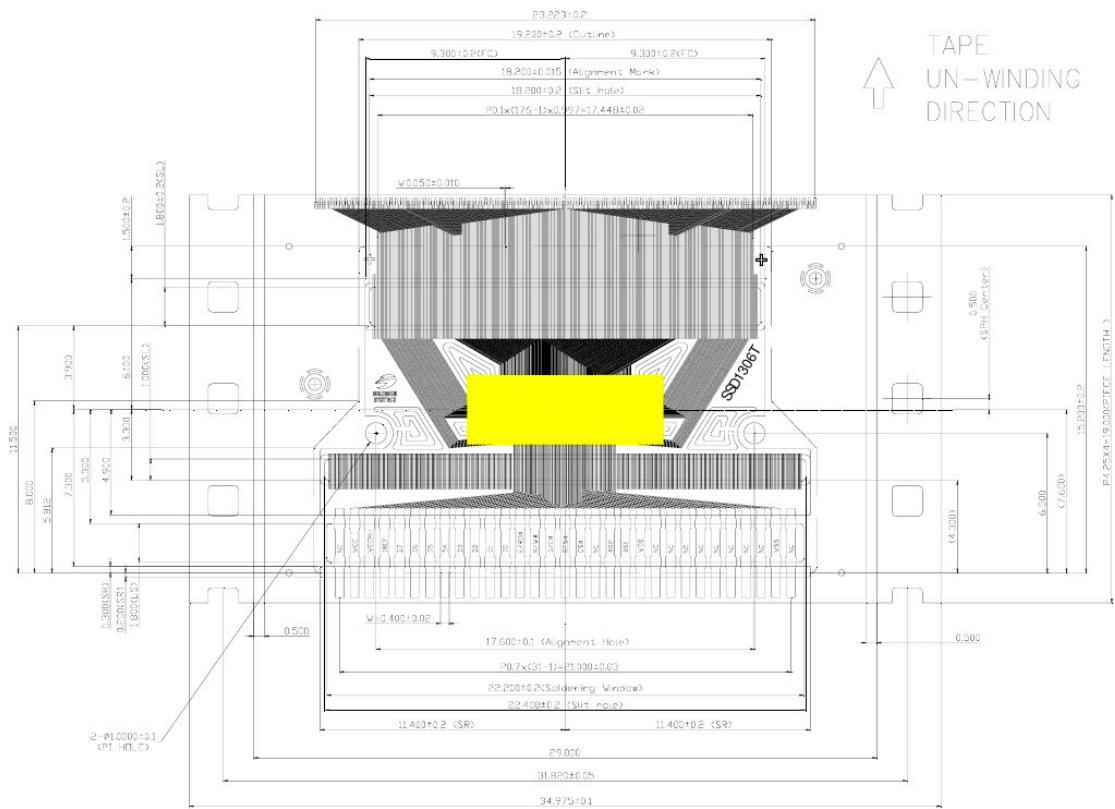
### Note

<sup>(1)</sup> The capacitor value is recommended value. Select appropriate value against module application.

## 15 PACKAGE INFORMATION

## 15.1 SSD1306TR1 Detail Dimension

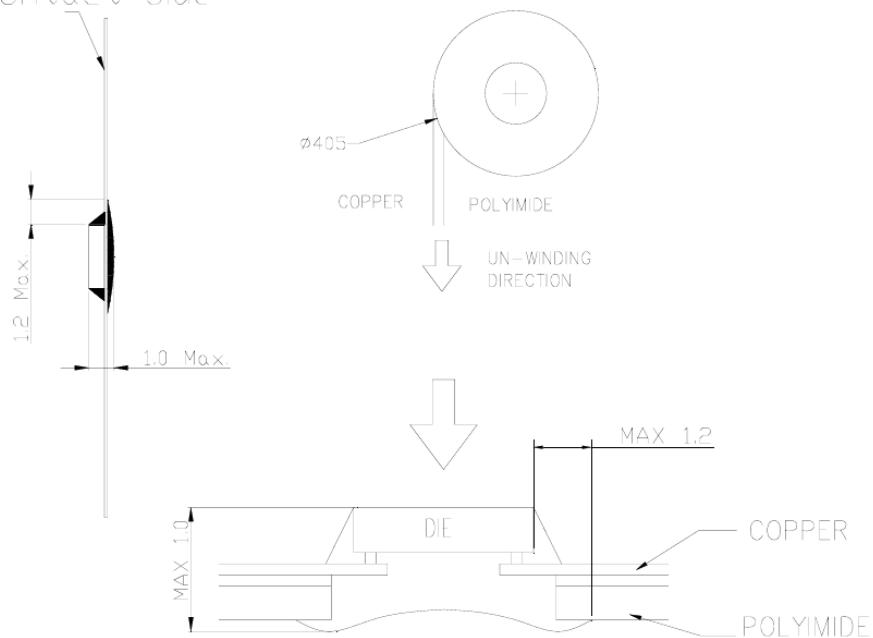
**Figure 15-1 SSD1306TR1 Detail Dimension**



## Specification:

1. GENERAL TOLERANCE:  $\pm 0.05$  mm
  2. MATERIAL
    - PI:  $75 \pm 8$  um
    - CU:  $15 \pm 3$  um
    - ADHESIVE:  $12 \pm 3$  um
    - SR:  $26 \pm 14$  um
  3. Plating : Sn  $0.20 \pm 0.05$  um
  4. TAPESITE: 4 SPH, 19 mm

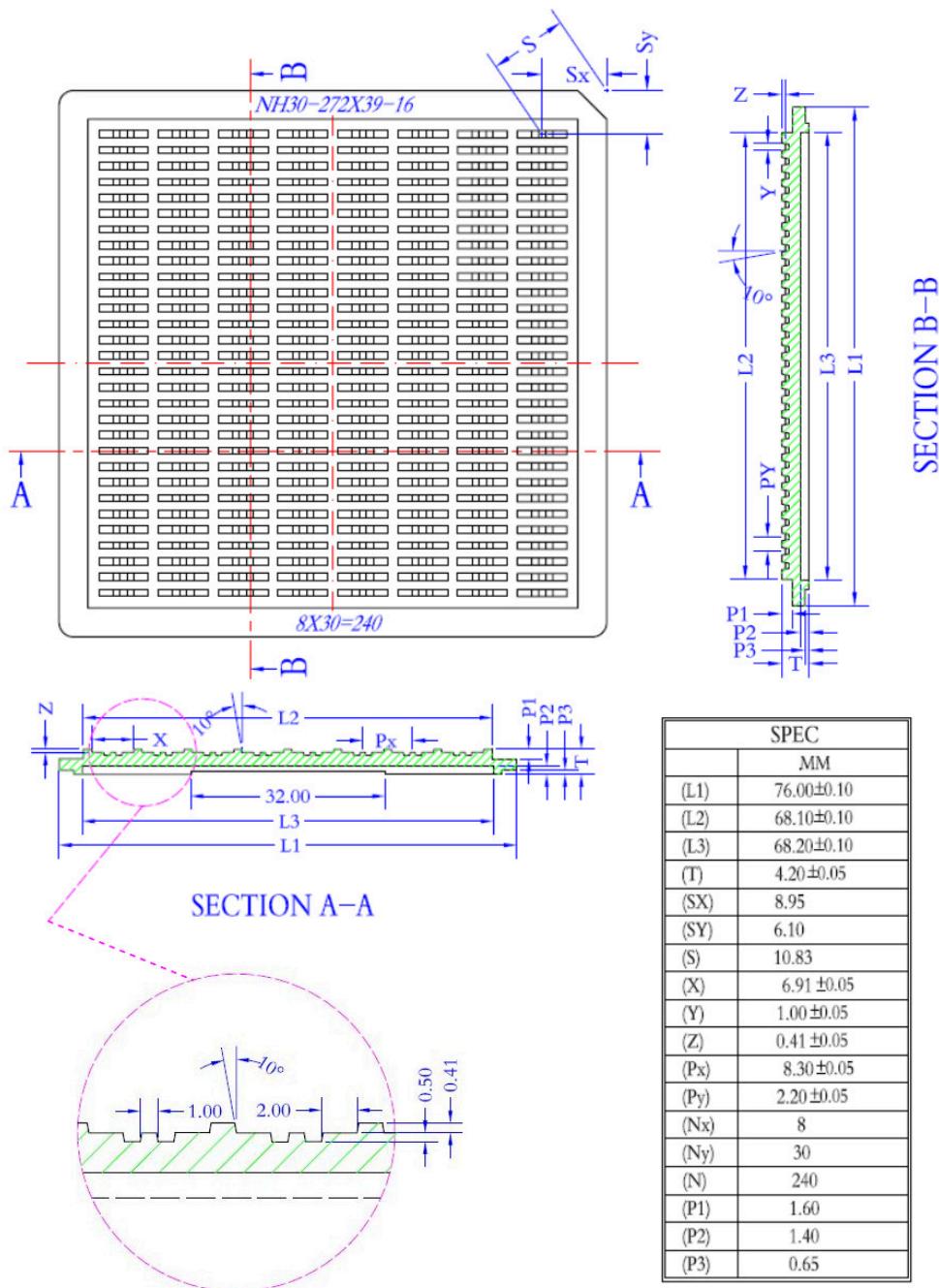
Contact Side



## MIRROR DESIGN

## 15.2 SSD1306Z Die Tray Information

Figure 15-2 : SSD1306Z die tray information



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# **SSD1306**

## ***Application Note***

**128 x 64 Dot Matrix  
OLED/PLED Segment/Common Driver with Controller**

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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## 1 Introduction

This application note of SSD1306 is written to explain the charge pump regulator function of SSD1306. SSD1306 is a single-chip CMOS OLED/PLED driver with controller for organic / polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 64 commons. This IC is designed for Common Cathode type OLED panel.

For the detailed characteristics of the driver IC, please refer to SSD1306 datasheet.

## 2 Charge Pump Regulator

The internal regulator circuit in SSD1306 accompanying only 2 external capacitors can generate a 7.5V voltage supply,  $V_{CC}$ , from a low voltage supply input,  $V_{BAT}$ . The  $V_{CC}$  is the voltage supply to the OLED driver block. This is a switching capacitor regulator circuit, designed for handheld applications. This regulator can be turned on/off by software command setting.

- Power supply
  - $V_{DD} = 1.65V$  to  $3.3V < V_{BAT}$  for IC logic
  - $V_{BAT} = 3.3V$  to  $4.2V$  for charge pump regulator circuit
- Pins description for related pins of the charge pump regulator
  - $V_{BAT}$  – Power supply for charge pump regulator circuit.

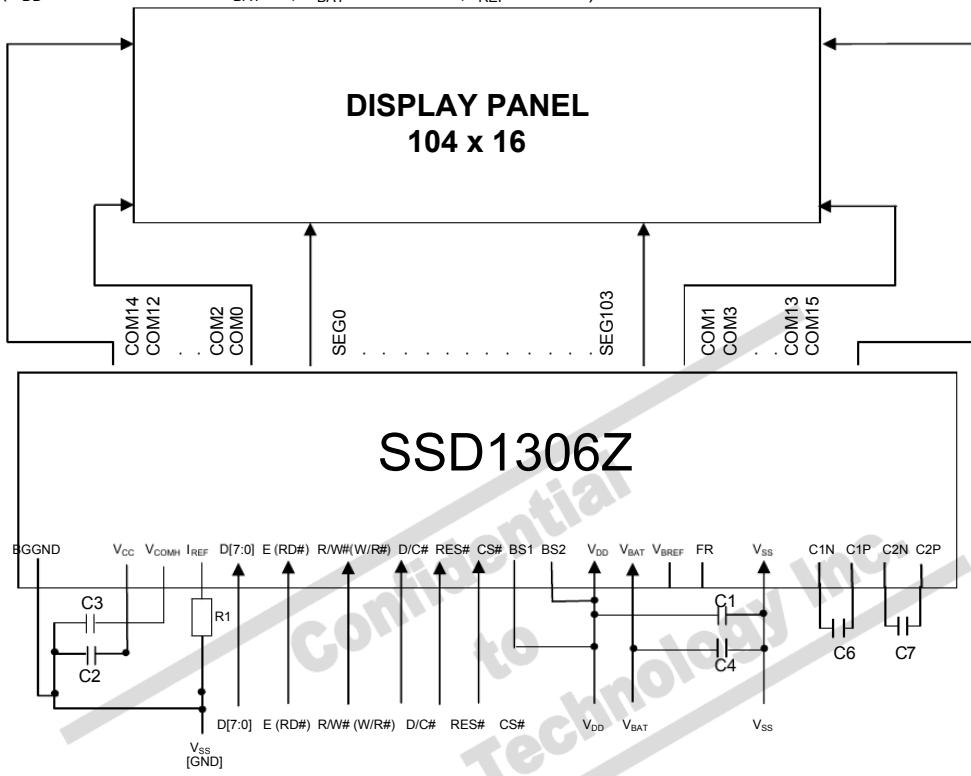
Status	$V_{BAT}$	$V_{DD}$	$V_{CC}$
Enable charge pump	Connect to external $V_{BAT}$ source	Connect to external $V_{DD}$ source	A capacitor should be connected between this pin and $V_{SS}$
Disable charge pump pin	Connect with $V_{DD}$	Connect to external $V_{DD}$ source	Connect to external $V_{CC}$ source
  - C1P/C1N – Pin for charge pump capacitor; Connect to each other with a capacitor
  - C2P/C2N – Pin for charge pump capacitor; Connect to each other with a capacitor

### 2.1 Command Table for Charge Pump Setting

1. Charge Pump Command Table										
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command Description
0	8D	1	0	0	0	1	1	0	1	Charge Pump Setting
0	A[7:0]	*	*	0	1	0	A <sub>2</sub>	0	0	A[2] = 0b, Disable charge pump(RESET) A[2] = 1b, Enable charge pump during display on  <b>Note</b> <sup>(1)</sup> The Charge Pump must be enabled by the following command: 8Dh ; Charge Pump Setting 14h ; Enable Charge Pump AFh; Display ON

**Figure 1 : Application Example of SSD1306Z with charge bump**

The configuration for 8080-parallel interface mode is shown in the following diagram:  
 $(V_{DD} = 1.65V \sim 3.3V, < V_{BAT}, V_{BAT} = 3.3V \sim 4.2V, I_{REF} = 12.5\mu A)$



Pin connected to MCU interface: D[7:0], E, R/W#, D/C#, CS#, RES#

Pin internally connected to V<sub>SS</sub>: BS0, CL

Pin internally connected to V<sub>DD</sub>: CLS

V<sub>BREF</sub>, FR should be left open.

C1, C4, C6, C7: 1.0 $\mu$ F <sup>(1)</sup>  
 C2, C3: 2.2 $\mu$ F <sup>(1)</sup>

Voltage at I<sub>REF</sub> = V<sub>CC</sub> - 2.5V. For V<sub>CC</sub> = 7.5V, I<sub>REF</sub> = 12.5 $\mu$ A:

$$\begin{aligned} R1 &= (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF} \\ &= (7.5 - 2.5) / 12.5\mu A \\ &= 400K\Omega \end{aligned}$$

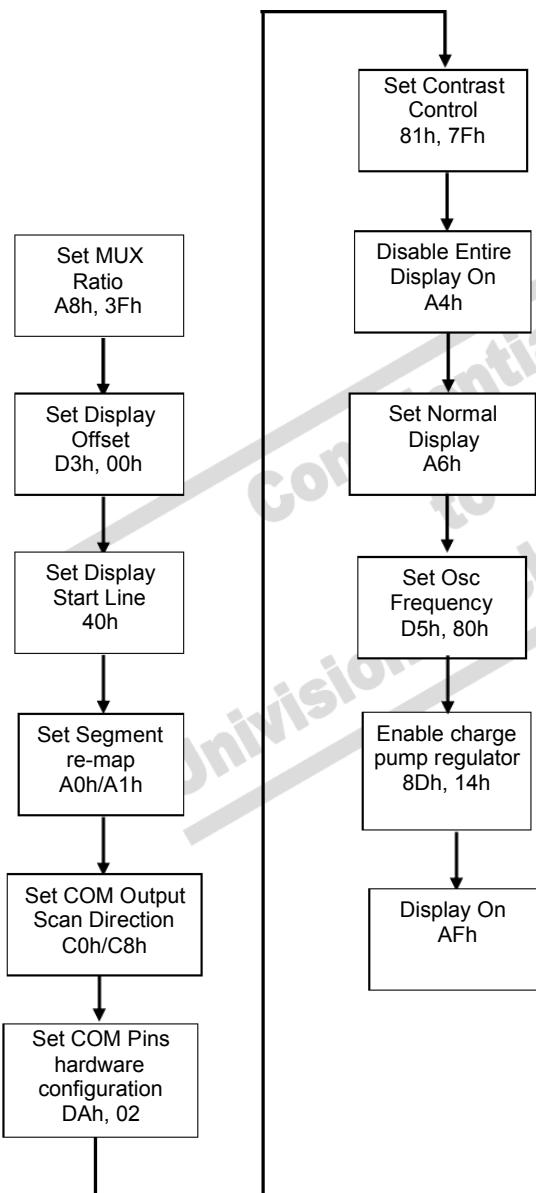
#### Note

<sup>(1)</sup> The capacitor value is recommended value. Select appropriate value against module application.

### 3 Software Configuration

SSD1306 has internal command registers that are used to configure the operations of the driver IC. After reset, the registers should be set with appropriate values in order to function well. The registers can be accessed by MPU interface in either 6800, 8080, SPI type with D/C# pin pull low or using I<sup>2</sup>C interface. Below is an example of initialization flow of SSD1306. The values of registers depend on different condition and application.

Figure 2 : Software Initialization Flow Chart



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