Automated Alphanumeric Sequencer: A 555-Timer Driven D-Flip-Flop and NAND-Gate Decoder for ‘C2-F9d4’ on a Seven-Segment Display

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Abstract—This project focuses on building a digital circuit that counts through a specific 3-bit binary sequence and displays each value on a seven-segment display. It uses only basic components such as NAND gates, D flip-flops, and a NE555 timer to generate clock pulses for counting. The output is shown on a common-cathode seven-segment display. The circuit follows the sequence: 111, 010, 100, 101, 011, 000, 110, 001, and then resets to repeat the cycle. After the initial reset, the display shows the characters “–9dFC42” in order, and the sequence restarts automatically after completing the cycle. This setup demonstrates how digital circuits can operate using simple logic components, without relying on any microcontroller.

Keywords—Digital Logic, D Flip-Flop, Karnaugh Map, Seven-Segment Display, State Machine.

I. Introduction

A. Background and Motivation

Digital electronics play a vital role in everyday devices like calculators, digital clocks, and embedded systems. A key concept in this field is the binary counter, which moves through binary numbers in response to clock pulses and is often used with decoders to provide visual output. This project focuses on building such a circuit using only basic logic components—D flip-flops (74HC74), NAND gates (74HC00/74HC10), and a NE555 timer—to avoid the need for any programmable device or microcontroller.

B. Problem Statement

Standard binary counters progress through natural binary order (000 to 111), but real-world applications often require custom sequences. In this project, we aim to design a counter that follows a predefined 3-bit sequence—111, 010, 100, 101, 011, 000, 110, 001—and loops continuously. Each state corresponds to a specific character to be displayed on a common-cathode seven-segment display, forming the pattern ‘–9dFC42’.

C. Scope and Objectives

The main goal of this project is to create a fully automatic digital system that cycles through the desired 3-bit binary sequence and displays the corresponding characters using a seven-segment display. The circuit is built using only fundamental ICs like D flip-flops for state storage and NAND gates for combinational decoding, while a 555 timer generates regular clock pulses to drive the sequence. The system is tested through both simulation and real hardware implementation to ensure that it performs as expected. This helps reinforce core digital logic concepts such as truth tables, flip-flop operation, combinational design, timing circuits, and display interfacing.

II. Work Plan and Human Resources

A. Work Plan

The project followed a structured work plan beginning with the preparation of the proposal, which outlined the objectives and overall approach. We first carried out an initial simulation using AND & OR gates to verify the K-map expressions for the seven-segment display. Once the logic was confirmed, the expressions were converted to NAND-only form, and the final simulation was completed.

After validating the design, we ordered the necessary components, including D flip-flops, NAND gate ICs, and the seven-segment display. The combinational logic circuit was built first and tested thoroughly to ensure that each binary input produced the correct segment output. This part of the project was demonstrated using manual inputs before moving on to the sequential logic.

Next, we simulated the 3-bit binary counter using D flip-flops and a clock source. Once verified, the circuit was implemented on a breadboard using 74HC74 flip-flops and a NE555 timer configured as a pulse generator. After confirming the counter transitioned through all states correctly, it was connected to the combinational circuit to complete the full system.

Final testing ensured that the complete circuit worked smoothly and displayed the correct character for each binary state in the sequence.

B. Human Resources

The project was executed collaboratively by a three-member team. Sadia Akter was responsible for the initial derivation of the K-map expressions for segments a, b, c, d, e, f, and g, ensuring that the number of required logic gates was minimized. She also contributed by drafting the Human Resources, Proposed Budget, and Conclusion sections of this report.