Crimson UHD Server API

This API utilizes UDP as the transport layer. Please code your respective software according to your machine's network sockets to enable UDP interactions.
It is important to note that properties take time to update, if too many subsequent commands are sent in a short time, there will be dropped UDP packets.

UDP Transaction (CSV in string format)				
Transmit	Sequence Number	Operation	Property	[Data]
Receive	Sequence Number	Status	[Data]	

Setting Properties			
Step 1	Transmit	Command	1,set,rx_a/rf/gain/val,65
Step 2	Receive	Acknowledge	1,0

Reading Properties			
Step 1	Transmit	Command	78,get,rx_a/rf/gain/val
Step 2	Receive	Acknowledge	78,0,65

Command Description	
Sequence	uint32_t value to reference on acknowledge steps just in case commands were executed out of order.
Operation	“get” or “set”
Property	Path of the property, refer to table below and concatenate with '/' between directories under “Property Path”
Data	String representation of data, refer to table below under “Function”
Status	0 is no error, 1 is error

Property Path				Permissons	Double Cycle	Function
TX	PWR			RW		Power of DSP and RF chain (1) on, (0) off, Power On resets all settings**
	RF	DAC	NCO	RW		DAC clock frequency (Mhz)
			TEMP	RO	Y	Temperature of the DAC IC (Celcius)
		FREQ	VAL	RW		Tune the RF chain to desired frequency (Hz)
			BAND	RW		RF band that was chosen after tuning (1) High, (0) Low
			I_BIAS	RW		Adjust I-bias (in 100mV's)
			Q_BIAS	RW		Adjust Q-bias (in 100mV's)
		GAIN	VAL	RW		Set RF chain gain (dB)
		BOARD	STATUS	RW	Y	Not implemented Yet
			DUMP	WO		Dump all of the registers of the device into /tmp/dump.txt
			TEST	WO		Not implemented Yet
			TEMP	RW	Y	Temperature of the RF board (Celcius)
			LED	WO		Number of times to toggle the LED
	DSP	GAIN		RW		Not implemented Yet
		RATE		RW		Sample Rate (SPS)
		NCO_ADJ		RW		Frequency Mixing (Hz)
		RSTREQ		WO		Request a reset to the DSP chain
	ABOUT	ID		RW		ID of the TX board
		SERIAL		RO		Serial Number of the TX Board
		FW_VER		RO		Compilation Date of UHD Server
		HW_VER		RO		Compilation Date of UHD Server
		SW_VER		RO		Compilation Date of UHD Server
	LINK	VITA_EN		RW		Enable VITA headers (1) or disable (0)
		IFACE		RW		Not implemented Yet (Refer to user manual for defaults)
		PORT		RW		UDP port to receive from (port for host to send output packets to)
RX	PWR			RW		Power of the DSP and RF chain (1) on, (0) off, Power On resets all settings
	RF	FREQ	VAL	RW		Tune the RF chain to desired frequency (Hz)
			BAND	RW		RF band that was chosen after tuning (1) High, (0) Low
			LNA	RW		Bypass the LNA (1) Bypass, (0) LNA
		GAIN	VAL	RW		Set RF chain gain (dB)
		BOARD	STATUS	RW	Y	Not implemented Yet
			DUMP	WO		Dump all of the registers of the device into /tmp/dump.txt
			TEST	WO		Not implemented Yet
			TEMP	RW	Y	Temperature of the RF board (Celcius)
			LED	WO		Number of times to toggle the LED
	DSP	SIGNED		RW		DSP output to be signed (1) or unsigned (0)
		GAIN		RW		Not implemented Yet
		RATE		RW		Sample Rate (SPS)
		NCO_ADJ		RW		Frequency Mixing (Hz)
		RSTREQ		WO		Request a reset to the DSP chain
	ABOUT	ID		RW		ID of the TX board
		SERIAL		RO		Serial Number of the TX Board
		FW_VER		RO		Compilation Date of UHD Server
		HW_VER		RO		Compilation Date of UHD Server
		SW_VER		RO		Compilation Date of UHD Server
	LINK	VITA_EN		RW		Enable VITA headers (1) or disable (0)
		IFACE		RW		Not implemented Yet (Refer to user manual for defaults)
		PORT		RW		UDP port to transmit to (port for host to listen to)
		IP_DEST		RW		IP address to transmit to (address of host)
		MAC_DEST		RW		MAC address to transmit to (address of host)
TIME	CLK	PPS		RW		Not implemented Yet
		CUR_TIME		RW	Y	Current time of Crimson
	SOURCE	VCO		RW		VCO clock source (internal/external)
		SYNC		RW		Sync clock source (internal/external)
		REF		RW		Ref clock source (internal/external)
	BOARD	STATUS		RW	Y	Not implemented Yet
		DUMP		WO		Dump all of the registers of the device into /tmp/dump.txt
		TEST		WO		Not implemented Yet
		TEMP		RW	Y	Temperature of the RF board (Celcius)
		LED		WO		Number of times to toggle the LED
	ABOUT	ID		RW		ID of the TX board
		SERIAL		RO		Serial Number of the TX Board
		FW_VER		RO		Compilation Date of UHD Server
		HW_VER		RO		Compilation Date of UHD Server
		SW_VER		RO		Compilation Date of UHD Server
	BOARD	STATUS		RW	Y	Not implemented Yet
		DUMP		WO		Dump all of the registers of the device into /tmp/dump.txt
		TEST		WO		Not implemented Yet
		TEMP		RW	Y	Temperature of the RF board (Celcius)

FPGA	BOARD		LED	WO		Number of times to toggle the LED
			RSTREQ	WO		Request a reset to the FPGA
			JESD_RSTREQ	WO		Request a reset to the JESD link
			SYS_RSTREQ	WO		Request a reset to entire Crimson
	ABOUT		ID	RW		ID of the FPGA board
			SERIAL	RO		Serial Number of the FPGA Board
			FW_VER	RO		FW Version on the FPGA DSP chain
			HW_VER	RO		HW version of the FPGA Board
			SW_VER	RO		SW version of the FPGA Board
	LINK		RATE	RW		Not implemented Yet
		SFPA	IP_ADDR	RW		IP Address of SFPA port (address for host to send output packets to)
			MAC_ADDR	RW		MAC Address of SFPA port (address for host to send output packets to)
			VER	RW		IP protocol version (1) IPV6 (0) IPV4
			PAY_LEN	RW		Payload Len (bytes)
		SFPB	IP_ADDR	RW		IP Address of SFPA port (address for host to send output packets to)
			MAC_ADDR	RW		MAC Address of SFPB port (address for host to send output packets to)
			VER	RW		IP protocol version (1) IPV6 (0) IPV4
			PAY_LEN	RW		Payload Len (bytes)
		NET	DHCP_EN	RW		Not implemented Yet
			HOSTNAME	RW		Name of Crimson
			IP_ADDR	RW		IP Address of Management Port