Crimson UDP API

UDP Transaction (CSV)				
Transmit	Sequence Number	Operation	Property	[Data]
Receive	Sequence Number	Status	[Data]	

Property Path				Permissons	Poll Update	Function
TX	RF	DAC	MIXER	RW	N	Enable the DAC mixer. (1) Enable (0) Disable
			NCO	RW	N	DAC clock Frequency (Mhz)
			PAP	RW	N	Power amplification circuit (1) Enable, (0) Disable
			INTERP	RW	N	DAC interpolation (factor)
			TEMP	RO	Y	Temperature of the DAC IC (Celcius)
			IQERR_GAIN	RW	N	IQ error gain adjust
			IQERR_PHASE	RW	N	IQ error phase adjust
		FREQ	VAL	RW	N	Tune the RF chain to desired frequency (Mhz)
			BAND	RO	Y	RF band that was chosen after tuning (1) High, (0) Low
			LNA	RW	N	Enable the LNA (1) Enable, (0) Disable
			I_BIAS	RW	N	Adjust I-bias
			Q_BIAS	RW	N	Adjust Q-bias
		GAIN	VAL	RW	N	Set RF chain gain (dB)
		BOARD	STATUS	RO	Y	Status of the board (string)
			DUMP	WO	N	Dump all of the registers of the device into /tmp/dump.txt
			TEST	WO	N	Execute test vectors for the IC's
			TEMP	RO	Y	Temperature of the RF board (Celcius)
			LED	WO	N	Number of times to toggle the LED
	DSP	FREQ		RW	N	Tune the DSP chain to desired frequency (Mhz)
		GAIN		RW	N	Set DSP chain gain (dB)
		INTERP		RW	N	DSP Interpolation factor (2-256)
		RATE		RO	N	Effective sample rate after interpolation (MSPS)
		NCO_ADJ		RW	N	Mixing frequency adjust (Hz)
		IQERR_GAIN		RW	N	IQ error gain adjust
		IQERR_PHASE		RW	N	IQ error phase adjust
		RSTREQ		WO	N	Request a reset to the DSP chain
	ABOUT	ID		RW	N	ID of the TX board
		SERIAL		RO	N	Serial Number of the TX Board
		FW_VER		RO	N	FW Version on the TX DSP chain
		HW_VER		RO	N	HW version of the TX Board
		SW_VER		RO	N	SW version of the TX Board
	LINK	LOOPBACK		RW	N	Configure the link in loopback mode (1) enable, (0) disable
		IFACE		RW	N	Streaming interface (10G) 10 Gigabit link, (1G) management port
		PORT		RW	N	UDP port to transmit to
		IP_SRC		RW	N	IP address of Crimson
		IP_DEST		RW	N	IP address to transmit to
		MAC_SRC		RW	N	MAC address of Crimson
		MAC_DEST		RW	N	MAC address to transmit to
		PAY_LEN		RW	N	Streaming payload size (64-bit width)
		VER		RW	N	IP protocol version (1) IPV6 (0) IPV4
	PWR			RW	N	Power of the DSP and RF chain (1) on, (0) off
RX	RF	VGA	FREQ	RW	N	Set the corner frequency of the VGA (Mhz)
			BYPASS	RW	N	Bypass the low pass filter on the VGA (1) bypass, (0) no bypass
			GAIN1	RW	N	Set gain stage 1 (dB)
			GAIN2	RW	N	Set gain stage 2 (dB)
			GAIN3	RW	N	Set gain stage 3 (dB)
			PGAIN	RW	N	Set post amp gain (dB)
			ATTEN1	RW	N	Set attenuation stage 1 (dB)
			ATTEN2	RW	N	Set attenuation stage 2 (dB)
			ATTEN3	RW	N	Set attenuation stage 3 (dB)
		FREQ	VAL	RW	N	Tune the RF chain to desired frequency (Mhz)
			BAND	RO	Y	RF band that was chosen after tuning (1) High, (0) Low
			LNA	RW	N	Enable the LNA (1) Enable, (0) Disable
			VARAC	RW	N	Adjust IQ phase (clk cycles)
		GAIN	VAL	RW	N	Set RF chain gain (dB)
		BOARD	STATUS	RO	Y	Status of the board (string)
			DUMP	WO	N	Dump all of the registers of the device into /tmp/dump.txt
			TEST	WO	N	Execute test vectors for the IC's
			TEMP	RO	Y	Temperature of the RF board (Celcius)
			LED	WO	N	Number of times to toggle the LED
	DSP	FREQ		RW	N	Tune the DSP chain to desired frequency (Mhz)
		GAIN		RW	N	Set DSP chain gain (dB)
		INTERP		RW	N	DSP Interpolation factor (2-256)
		RATE		RO	Y	Effective sample rate after interpolation (MSPS)
		NCO_ADJ		RW	N	Mixing frequency adjust (Hz)
		IQERR_GAIN		RW	N	IQ error gain adjust
		IQERR_PHASE		RW	N	IQ error phase adjust
		RSTREQ		WO	N	Request a reset to the DSP chain
	ABOUT	ID		RW	N	ID of the TX board
		SERIAL		RO	N	Serial Number of the TX Board
		FW_VER		RO	N	FW Version on the TX DSP chain
		HW_VER		RO	N	HW version of the TX Board
		SW_VER		RO	N	SW version of the TX Board
	LINK	LOOPBACK		RW	N	Configure the link in loopback mode (1) enable, (0) disable
		IFACE		RW	N	Streaming interface (10G) 10 Gigabit link, (1G) management port
		PORT		RW	N	UDP port to transmit to
		IP_SRC		RW	N	IP address of Crimson
		IP_DEST		RW	N	IP address to transmit to
		MAC_SRC		RW	N	MAC address of Crimson
		MAC_DEST		RW	N	MAC address to transmit to
		PAY_LEN		RW	N	Streaming payload size (64-bit width)
		VER		RW	N	IP protocol version (1) IPV6 (0) IPV4
	PWR			RW	N	Power of the DSP and RF chain (1) on, (0) off
	CLK	RATE		RW	N	Clock rate of the sample clock (Mhz)
		PPS		RW	N	Pulse per second, used for clock syncing
		CUR_TIME		RW	N	Current time of Crimson
		VCO		RW	N	VCO clock source (internal/external)

TIME	SOURCE	SYNC	RW	N	Sync clock source (internal/external)
		REF	RW	N	Ref clock source (internal/external)
	BOARD	STATUS	RO	Y	Status of the board (string)
		DUMP	WO	N	Dump all of the registers of the device into /tmp/dump.txt
		TEST	WO	N	Execute test vectors for the IC's
		TEMP	RO	Y	Temperature of the RF board (Celcius)
		LED	WO	N	Number of times to toggle the LED
	ABOUT	ID	RW	N	ID of the TX board
		SERIAL	RO	N	Serial Number of the TX Board
		FW_VER	RO	N	FW Version on the TX DSP chain
		HW_VER	RO	N	HW version of the TX Board
		SW_VER	RO	N	SW version of the TX Board
FPGA	BOARD	STATUS	RO	Y	Status of the board (string)
		DUMP	WO	N	Dump all of the registers of the device into /tmp/dump.txt
		TEST	WO	N	Execute test vectors for the IC's
		TEMP	RO	Y	Temperature of the RF board (Celcius)
		LED	WO	N	Number of times to toggle the LED
		RSTREQ	WO	N	Request a reset to the FPGA
		JESD_RSTREQ	WO	N	Request a reset to the JESD link
	ABOUT	ID	RW	N	ID of the TX board
		SERIAL	RO	N	Serial Number of the TX Board
		FW_VER	RO	N	FW Version on the TX DSP chain
		HW_VER	RO	N	HW version of the TX Board
		SW_VER	RO	N	SW version of the TX Board
	LINK	PORT	RW	N	UDP port to transmit to
		IP_DEST	RW	N	IP address to transmit to
		MAC_DEST	RW	N	MAC address to transmit to
		VER	RW	N	IP protocol version (1) IPV6 (0) IPV4
		RATE	RW	N	(10000) 10G, (1000) 1G (100) 1G