Crimson UDP API UDP Transaction (CSV) Sequence Number Transmit Property [Data] Operation Receive Sequence Number Status [Data] Poll Update Function **Property Path** Permissons Enable the DAC mixer. (1) Enable (0) Disable DAC clock Frequency (Mhz) Power amplification circuit (1) Enable, (0) Disable MIXER RW NCO ΡΔΡ RW INTERF DAC DAC interpolation (factor) RW N Temperature of the DAC IC (Celcius) TEMP RO IQERR_GAIN IQERR_PHASE RW N IQ error gain adjust IQ error phase adjust Tune the RF chain to desired frequency (Mhz) \/Δ1 RW N RF band that was chosen after tuning (1) High, (0) Low BAND RO RF RW Enable the LNA (1) Enable, (0) Disable FREO I_BIAS Q_BIAS VAL RW N Adjust I-bias RW Adjust Q-bias Set RF chain gain (dB) Status of the board (string) Dump all of the registers of the device into /tmp/dump.txt GAIN RW N STATUS RO DUMP WO **BOARD** TEST WO N Execute test vectors for the IC's TEMP Temperature of the RF board (Celcius) RC LED WO Number of times to toggle the LED FREQ Tune the DSP chain to desired frequency (Mhz) RW N RW Set DSP chain gain (dB) GAIN DSP Interpolation factor (2-256) TX INTERP RW Ν Effective sample rate after interpolation (MSPS) RATE RO DSP NCO_ADJ RW Mixing frequency adjust (Hz) IQERR_GAIN IQERR_PHASE RW N IQ error gain adjust RW IQ error phase adjust RSTREQ WO N Request a reset to the DSP chain ID RW N ID of the TX board SERIAL Serial Number of the TX Board RO ABOUT FW_VER RO N FW Version on the TX DSP chain RC HW version of the TX Board HW VER RO SW version of the TX Board N Configure the link in loopback mode (1) enable, (0) disable LOOPBACK RW N Streaming interface (10G) 10 Gigabit link, (1G) management port IFACE RW PORT RW N UDP port to transmit to IP SRO RW N IP address of Crimson IP_DEST LINK IP address to transmit to MAC_SRC MAC_DEST RW N MAC address of Crimson RW MAC address to transmit to PAY_LEN RW N Streaming payload size (64-bit width) VFR RW N IP protocol version (1) IPV6 (0) IPV4 PWR Power of the DSP and RF chain (1) on, (0) off RW Set the corner frequency of the VGA (Mhz) Bypass the low pass filter on the VGA (1) bypass, (0) no bypass FREQ RW N BYPASS RW GAIN1 RW Set gain stage 2 (dB) GAIN2 RW N VGA GAIN3 Set gain stage 3 (dB) RW PGAIN RW N Set post amp gain (dB) ATTEN1 RW Set attenuation stage 1 (dB ATTEN2 Set attenuation stage 2 (dB) Set attenuation stage 3 (dB) Tune the RF chain to desired frequency (Mhz) **ATTFN3** RW N RF RW N VAL RF band that was chosen after tuning (1) High, (0) Low Enable the LNA (1) Enable, (0) Disable BAND RΩ FREQ LNA RW N VARAC Adjust IQ phase (clk cycles) GAIN VAI RW N Set RF chain gain (dB) STATUS Status of the board (string) RO DUMP WO Dump all of the registers of the device into /tmp/dump.txt BOARD TEST WO N Execute test vectors for the IC's TEMP RO Temperature of the RF board (Celcius) LED WO N Number of times to toggle the LED Tune the DSP chain to desired frequency (Mhz) FREO RW RW Set DSP chain gain (dB RX DSP Interpolation factor (2-256) INTERP RW N RO Effective sample rate after interpolation (MSPS) RATE DSP NCO_ADJ RW N Mixing frequency adjust (Hz) IQERR_GAIN IQERR_PHASE IQ error gain adjust IQ error phase adjust RW RW Request a reset to the DSP chain ID of the TX board RSTREQ WO N RW ID SERIAL RO N erial Number of the TX Board ABOUT FW_VER HW_VER RO FW Version on the TX DSP chain HW version of the TX Board SW VFR RO N SW version of the TX Board Configure the link in loopback mode (1) enable, (0) disable LOOPBACK RW N IFACE RW Streaming interface (10G) 10 Gigabit link, (1G) management port UDP port to transmit to IP address of Crimson PORT RW N IP SRC RW LINK IP_DEST RW N IP address to transmit to MAC_SRC MAC_DEST RW N MAC address of Crimson MAC address to transmit to Streaming payload size (64-bit width) IP protocol version (1) IPV6 (0) IPV4 PAY_LEN RW N RW VER PWR RW N Power of the DSP and RF chain (1) on, (0) off RATE RW N Clock rate of the sample clock (Mhz) CLK Pulse per second, used for clock syncing CUR_TIME RW Current time of Crimson VCO clock source (internal/external)

Ν

VCO

RW

Sheet1

| TIME | SOURCE | SYNC | RW | N | Sync clock source (internal/external) |
|------|--------|-------------|----|---|--|
| | | REF | RW | N | Ref clock source (internal/external) |
| | BOARD | STATUS | RO | Y | Status of the board (string) |
| | | DUMP | WO | N | Dump all of the registers of the device into /tmp/dump.txt |
| | | TEST | WO | N | Execute test vectors for the IC's |
| | | TEMP | RO | Y | Temperature of the RF board (Celcius) |
| | | LED | WO | N | Number of times to toggle the LED |
| | ABOUT | ID | RW | N | ID of the TX board |
| | | SERIAL | RO | N | Serial Number of the TX Board |
| | | FW_VER | RO | N | FW Version on the TX DSP chain |
| | | HW_VER | RO | N | HW version of the TX Board |
| | | SW_VER | RO | N | SW version of the TX Board |
| FPGA | BOARD | STATUS | RO | Y | Status of the board (string) |
| | | DUMP | WO | N | Dump all of the registers of the device into /tmp/dump.txt |
| | | TEST | WO | N | Execute test vectors for the IC's |
| | | TEMP | RO | Y | Temperature of the RF board (Celcius) |
| | | LED | WO | N | Number of times to toggle the LED |
| | | RSTREQ | WO | N | Request a reset to the FPGA |
| | | JESD_RSTREQ | WO | N | Request a reset to the JESD link |
| | ABOUT | ID | RW | N | ID of the TX board |
| | | SERIAL | RO | N | Serial Number of the TX Board |
| | | FW_VER | RO | N | FW Version on the TX DSP chain |
| | | HW_VER | RO | N | HW version of the TX Board |
| | | SW_VER | RO | N | SW version of the TX Board |
| | LINK | PORT | RW | N | UDP port to transmit to |
| | | IP_DEST | RW | N | IP address to transmit to |
| | | MAC_DEST | RW | N | MAC address to transmit to |
| | | VER | RW | N | IP protocol version (1) IPV6 (0) IPV4 |
| | | RATE | RW | N | (10000) 10G, (1000) 1G (100) 1G |