Sheet1 Crimson UDP API UDP Transaction (CSV) Sequence Number Transmit Operation Property [Data] Sequence Number Receive Status [Data] Poll Update Function **Property Path** Permissons Enable the DAC mixer. (1) Enable (0) Disable DAC clock frequency (Hz) Power amplification protection circuit (1) Enable, (0) Disable MIXER RW NCO ΡΔΡ RW INTERP DAC RW DAC interpolation (factor) 0-15 N Temperature of the DAC IC (Celcius) TEMP RO IQERR_GAIN IQERR_PHASE RW N IQ error gain adjust IQ error phase adjust Tune the RF chain to desired frequency (Khz) RF band that was chosen after tuning (1) High, (0) Low \/Δ1 RW N BAND RO RF RW Bypass the LNA (1) Bypass, (0) LNA FREO I_BIAS Q_BIAS VAL RW N Adjust I-bias RW Adjust Q-bias Set RF chain gain (dB) Status of the board (string) Dump all of the registers of the device into /tmp/dump.txt GAIN RW N STATUS RO DUMP WO **BOARD** TEST WO N Execute test vectors for the IC's TEMP Temperature of the RF board (Celcius) Number of times to toggle the LED RC TX LED WO FREQ Tune the DSP chain to desired frequency (Khz) RW N RW Set DSP chain gain (dB) GAIN RATE RO N Effective sample rate after interpolation (MSPS) DSP Mixing frequency adjust (Hz) IQ error gain adjust NCO ADI RW IQERR_GAIN RW IQERR PHASE RW N IQ error phase adjust WO Request a reset to the DSP chain **RSTREQ** ID RW N ID of the TX board SERIAL Serial Number of the TX Board RO N FW Version on the TX DSP chain ABOUT FW_VER RO HW version of the TX Board SW version of the TX Board HW_VER RO N RC SW_VER IFACE RW N Streaming interface (10G) 10 Gigabit link, (1G) management port UDP port to transmit to Streaming payload size (64-bit width) LINK PORT RW N PAY LEN RW Power of the DSP and RF chain (1) on, (0) off PWR RW N FREQ RW Set the corner frequency of the VGA (Mhz) N BYPASS Bypass the low pass filter on the VGA (1) bypass, (0) no bypass Set gain stage 1 (dB) Set gain stage 2 (dB) GAIN1 RW N GAIN2 RW VGA GAIN3 RW N Set gain stage 3 (dB) **PGAIN** RW N Set post amp gain (dB) ATTEN1 RW Set attenuation stage 1 (dB Set attenuation stage 2 (dB) Set attenuation stage 3 (dB) ΔTTFN2 RW N ATTEN3 RW RW Tune the RF chain to desired frequency (Khz) RF BAND RO RF band that was chosen after tuning (1) High, (0) Low FREQ RW Bypass the LNA (1) Bypass, (0) LNA LNA VARAC RW N Adjust IQ phase (clk cycles) GAIN Set RF chain gain (dB) RW VAL Ν STATUS RO Status of the board (string) Dump all of the registers of the device into /tmp/dump.txt DUMP WO N BOARD TEST Execute test vectors for the IC's WO N TEMP RΩ Temperature of the RF board (Celcius) Number of times to toggle the LED Tune the DSP chain to desired frequency (Khz) RX LED WO N FREQ GAIN RW N Set DSP chain gain (dB) Effective sample rate after interpolation (MSPS) RATE RO DSP NCO_ADJ RW N Mixing frequency adjust (Hz) IOERR GAIN RW N IQ error gain adjust IQERR_PHASE RW IQ error phase adjust Request a reset to the DSP chain ID of the RX board RSTREQ WO N ID RW N SERIAL RO Serial Number of the RX Board FW_VER HW_VER AROUT RO N FW Version on the RX DSP chain RO HW version of the RX Board SW_VER RO N SW version of the RX Board Streaming interface (10G) 10 Gigabit link, (1G) management port UDP port to transmit to IFACE RW N RW IP_DEST MAC_DEST PAY_LEN LINK RW N IP address to transmit to RW MAC address to transmit to RW N Streaming payload size (64-bit width) **PWR** RW Power of the DSP and RF chain (1) on, (0) off RATE RW Clock rate of the sample clock (Mhz) CLK PPS RW N Pulse per second, used for clock syncing CUR_TIME RW N Current time of Crimson VCO VCO clock source (internal/external) Sync clock source (internal/external) Ref clock source (internal/external) SOURCE SYNC RW N RW REF Status of the board (string) STATUS RO Dump all of the registers of the device into /tmp/dump.txt DUMP TEST WO N TIME Execute test vectors for the IC's BOARD WO Temperature of the RF board (Celcius) Number of times to toggle the LED TEMP RO WO LED RW N ID of the TIME board

Serial Number of the TIME Board FW Version on the TIME DSP chain

HW version of the TIME Board SW version of the TIME Board

N

N

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SERIAL

FW_VER HW_VER

SW VER

ABOUT

RO

RΩ

RO

Sheet1

		STATUS		RO	Y	Status of the board (string)
FPGA		DUMP		WO	N	Dump all of the registers of the device into /tmp/dump.txt
		TEST		WO	N	Execute test vectors for the IC's
	BOARD	TEMP		RO	Y	Temperature of the RF board (Celcius)
		LED		WO	N	Number of times to toggle the LED
		RSTREQ		WO	N	Request a reset to the FPGA
		JESD_RSTREQ		WO	N	Request a reset to the JESD link
	ABOUT	ID		RW	N	ID of the FPGA board
		SERIAL		RO	N	Serial Number of the FPGA Board
		FW_VER		RO	N	FW Version on the FPGA DSP chain
		HW_VER		RO	N	HW version of the FPGA Board
		SW_VER		RO	N	SW version of the FPGA Board
	LINK	RATE		RW	N	(10000) 10G, (1000) 1G / Management Port
		LOOPBACK		RW	N	Enable Loopback mode (1) enable
		SFPA	IP_ADDR	RW	N	IP Address of Crimson's SFPA port (255.255.255.255)/(FFFF:FFFF:FFFF)
			MAC_ADDR	RW	N	MAC Address of Crimson's SFPA port
			VER	RW	N	IP protocol version (1) IPV6 (0) IPV4
		SFPB	IP_ADDR	RW	N	IP Address of Crimson's SFPA port (255.255.255.255)/(FFFF:FFFF:FFFF)
			MAC_ADDR	RW	N	MAC Address of Crimson's SFPB port
			VER	RW	N	IP protocol version (1) IPV6 (0) IPV4