Crimson UDP API

UDP Transaction (CSV)			
Transmit	Sequence Number	Operation	Property [Data]
Receive	Sequence Number	Status	[Data]

Property Path				Permissons	Poll Update	Function
TX	RF	DAC	MIXER	RW	N	Enable the DAC mixer. (1) Enable (0) Disable
			NCO	RW	N	DAC clock frequency (Mhz)
			PAP	RW	N	Power amplification protection circuit (1) Enable, (0) Disable
			INTERP	RW	N	DAC interpolation (factor) 0-15
			TEMP	RO	Y	Temperature of the DAC IC (Celcius)
			IQERR_GAIN	RW	N	IQ error gain adjust
			IQERR_PHASE	RW	N	IQ error phase adjust
		FREQ	VAL	RW	N	Tune the RF chain to desired frequency (Khz)
			BAND	RO	Y	RF band that was chosen after tuning (1) High, (0) Low
			LNA	RW	N	Bypass the LNA (1) Bypass, (0) LNA
			I_BIAS	RW	N	Adjust I-bias
			Q_BIAS	RW	N	Adjust Q-bias
		GAIN	VAL	RW	N	Set RF chain gain (dB)
		BOARD	STATUS	RO	Y	Status of the board (string)
			DUMP	WO	N	Dump all of the registers of the device into /tmp/dump.txt
			TEST	WO	N	Execute test vectors for the IC's
			TEMP	RO	Y	Temperature of the RF board (Celcius)
			LED	WO	N	Number of times to toggle the LED
	DSP	FREQ		RW	N	Tune the DSP chain to desired frequency (Khz)
		GAIN		RW	N	Set DSP chain gain (dB)
		RATE		RO	N	Effective sample rate after interpolation (SPS)
		NCO_ADJ		RW	N	Mixing frequency adjust (Hz)
		IQERR_GAIN		RW	N	IQ error gain adjust
		IQERR_PHASE		RW	N	IQ error phase adjust
		RSTREQ		WO	N	Request a reset to the DSP chain
	ABOUT	ID		RW	N	ID of the TX board
		SERIAL		RO	N	Serial Number of the TX Board
		FW_VER		RO	N	FW Version on the TX DSP chain
		HW_VER		RO	N	HW version of the TX Board
		SW_VER		RO	N	SW version of the TX Board
	LINK	ENABLE		RW	N	Enable streaming (1), (0) to disable
		VITA_EN		RW	N	Enable VITA headers
		IFACE		RW	N	sfpa / sfpb / management
		PORT		RW	N	UDP port to transmit to
	PWR			RW	N	Power of the DSP and RF chain (1) on, (0) off, Power On resets all settings
RX	RF	VGA	FREQ	RW	N	Set the corner frequency of the VGA (Mhz)
			BYPASS	RW	N	Bypass the low pass filter on the VGA (1) bypass, (0) no bypass
			GAIN1	RW	N	Set gain stage 1 (dB)
			GAIN2	RW	N	Set gain stage 2 (dB)
			GAIN3	RW	N	Set gain stage 3 (dB)
			PGAIN	RW	N	Set post amp gain (dB)
			ATTEN1	RW	N	Set attenuation stage 1 (dB)
			ATTEN2	RW	N	Set attenuation stage 2 (dB)
			ATTEN3	RW	N	Set attenuation stage 3 (dB)
		FREQ	VAL	RW	N	Tune the RF chain to desired frequency (Khz)
			BAND	RO	Y	RF band that was chosen after tuning (1) High, (0) Low
			LNA	RW	N	Bypass the LNA (1) Bypass, (0) LNA
			VARAC	RW	N	Adjust IQ phase (clk cycles)
		GAIN	VAL	RW	N	Set RF chain gain (dB)
		BOARD	STATUS	RO	Y	Status of the board (string)
			DUMP	WO	N	Dump all of the registers of the device into /tmp/dump.txt
			TEST	WO	N	Execute test vectors for the IC's
			TEMP	RO	Y	Temperature of the RF board (Celcius)
			LED	WO	N	Number of times to toggle the LED
	DSP	FREQ		RW	N	Tune the DSP chain to desired frequency (Khz)
		GAIN		RW	N	Set DSP chain gain (dB)
		RATE		RO	Y	Effective sample rate after interpolation (SPS)
		NCO_ADJ		RW	N	Mixing frequency adjust (Hz)
		IQERR_GAIN		RW	N	IQ error gain adjust
		IQERR_PHASE		RW	N	IQ error phase adjust
		RSTREQ		WO	N	Request a reset to the DSP chain
	ABOUT	ID		RW	N	ID of the RX board
		SERIAL		RO	N	Serial Number of the RX Board
		FW_VER		RO	N	FW Version on the RX DSP chain
		HW_VER		RO	N	HW version of the RX Board
		SW_VER		RO	N	SW version of the RX Board
	LINK	ENABLE		RW	N	Enable streaming (1), (0) to disable
		VITA_EN		RW	N	Enable VITA headers
		IFACE		RW	N	sfpa / sfpb / management
		PORT		RW	N	UDP port to transmit to
		IP_DEST		RW	N	IP address to transmit to
		MAC_DEST		RW	N	MAC address to transmit to
	PWR			RW	N	Power of the DSP and RF chain (1) on, (0) off, Power On resets all settings
TIME	CLK	PPS		RW	N	Pulse per second, used for clock syncing
		CUR_TIME		RW	N	Current time of Crimson
	SOURCE	VCO		RW	N	VCO clock source (internal/external)
		SYNC		RW	N	Sync clock source (internal/external)
		REF		RW	N	Ref clock source (internal/external)
	BOARD	STATUS		RO	Y	Status of the board (string)
		DUMP		WO	N	Dump all of the registers of the device into /tmp/dump.txt
		TEST		WO	N	Execute test vectors for the IC's
		TEMP		RO	Y	Temperature of the RF board (Celcius)
		LED		WO	N	Number of times to toggle the LED
	ABOUT	ID		RW	N	ID of the TIME board
		SERIAL		RO	N	Serial Number of the TIME Board
		FW_VER		RO	N	FW Version on the TIME DSP chain
		HW_VER		RO	N	HW version of the TIME Board

		SW_VER		RO	N	SW version of the TIME Board
FPGA	BOARD	STATUS		RO	Y	Status of the board (string)
		DUMP		WO	N	Dump all of the registers of the device into /tmp/dump.txt
		TEST		WO	N	Execute test vectors for the IC's
		TEMP		RO	Y	Temperature of the RF board (Celcius)
		LED		WO	N	Number of times to toggle the LED
		RSTREQ		WO	N	Request a reset to the FPGA
		JESD_RSTREQ		WO	N	Request a reset to the JESD link
	ABOUT	ID		RW	N	ID of the FPGA board
		SERIAL		RO	N	Serial Number of the FPGA Board
		FW_VER		RO	N	FW Version on the FPGA DSP chain
		HW_VER		RO	N	HW version of the FPGA Board
		SW_VER		RO	N	SW version of the FPGA Board
	LINK	RATE		RW	N	(10000) 10G, (1000) 1G / Management Port
		LOOPBACK		RW	N	Enable Loopback mode (1) enable
		SFPA	IP_ADDR	RW	N	IP Address of Crimson's SFPA port (255.255.255.255)/(FFFF:FFFF:FFFF:FFFF)
			MAC_ADDR	RW	N	MAC Address of Crimson's SFPA port
			VER	RW	N	IP protocol version (1) IPV6 (0) IPV4
			PAY_LEN	RW	N	Payload Len (max 1472, to min 4) multiple of 4. Keep same as SFPB*
		SFPB	IP_ADDR	RW	N	IP Address of Crimson's SFPA port (255.255.255.255)/(FFFF:FFFF:FFFF:FFFF)
			MAC_ADDR	RW	N	MAC Address of Crimson's SFPB port
			VER	RW	N	IP protocol version (1) IPV6 (0) IPV4
			PAY_LEN	RW	N	Payload Len (max 1472, to min 4) multiple of 4. Keep same as SFPA*