SYD8821: Ultra Low Power Bluetooth Low Energy 5.0 SoC

1.1 General Description

The SYD8821 is a low power and high performance Bluetooth Low Energy SoC. This SoC integrates all the essentials of a Bluetooth smart device which includes 32-bit ARM Cortex-M0 with Flash memory, digital interface support and high performance 2.4GHz RF transceiver. A high efficiency DCDC converter is integrated to provide a complete low power SoC solution for stand-alone applications such as wearable and IoT.

1.2 Key Features

- Fully qualified Bluetooth Low Energy 5.0
- 2.4mA RX radio current, 4.3mA TX radio current
- Cortex M0 32-bit MCU with max 64MHz clock rate, much more user-friendly than RSIC MCU
- Support Cache mode and DMA mode
- Ultra low power 2.4GHz transceiver with built-in balun and excellent performance
- Integrate 512kB Flash and 160kB SRAM
- Integrate 32MHz and 32.768kHz crystal oscillator
- Built in 64MHz and 32.768kHz RCOSC
- Communication interface options
  - I^2C-Master x2 + I^2C-Slave x1
  - SPI-Master x2 + SPI-Slave x1
  - UART x3
  - ISO-7816-3 x1
  - IRx1
- Digital peripherals
  - RTC x1
  - Quadrature Decoder x1
  - PWM/LED x6
  - FastPWM x4
  - KeyScan 8x18
  - PDM x1
- Analog peripherals
  - 10bit ADC x10
  - AMIC x1
- Serial Wire (SWD) debug supported

1.3 Applications

- Health and Fitness wearable device
- Interactive entertainment device
- Home and industrial automation
- HID peripherals
- Security/Proximity applications

1.4 Key Parameters

Parameter	Value
Max. TX Power	+4 dBm
RX Sensitivity	-94dBm
TX Current @0dBm*	4.3 mA
RX Current @-94dBm*	2.4 mA
Sleep Mode Current	3μA
Deep Sleep Mode Current	<1 μA
Flash	512 kB
Data RAM	160 kB
Supply Voltage	1.8~4.3V (VBAT) 1.8~3.6 V (VDDIO)
GPIO	31/19 (QFN48/32)
Operating Temperature, Tj	-40~+85 °C
Package Size –QFN48 –QFN32	6.0 x 6.0 x 1.0 mm 4.0 x 4.0 x 1.0 mm

*Condition: VBAT=3V, DCDC enable.

For any additional inquiries, please contact us at:

http://www.sydtek.com

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2.0 Introduction

2.1 Overview

The SYD8821 chip is highly integrated with ARM® Cortex®-M0 processor, Bluetooth Low Energy v5.0 baseband control core, ROM, Flash, Bluetooth Modem, Radio Transceiver, on-chip Balun and digital interfaces for the BLE application. The Cortex M0 can operate at 64MHz clock rate for heavy thread computing application, and can also operate at lower clock rate for simple data communication purpose. A DCDC built-in converter is integrated to provide full-solution SoC for stand-alone applications such as IoT, wearable and health devices.

Figure 1 shows the architecture block diagram of the chip. Refer to the subsequent chapters for detailed information on the functionality of the different interface blocks.

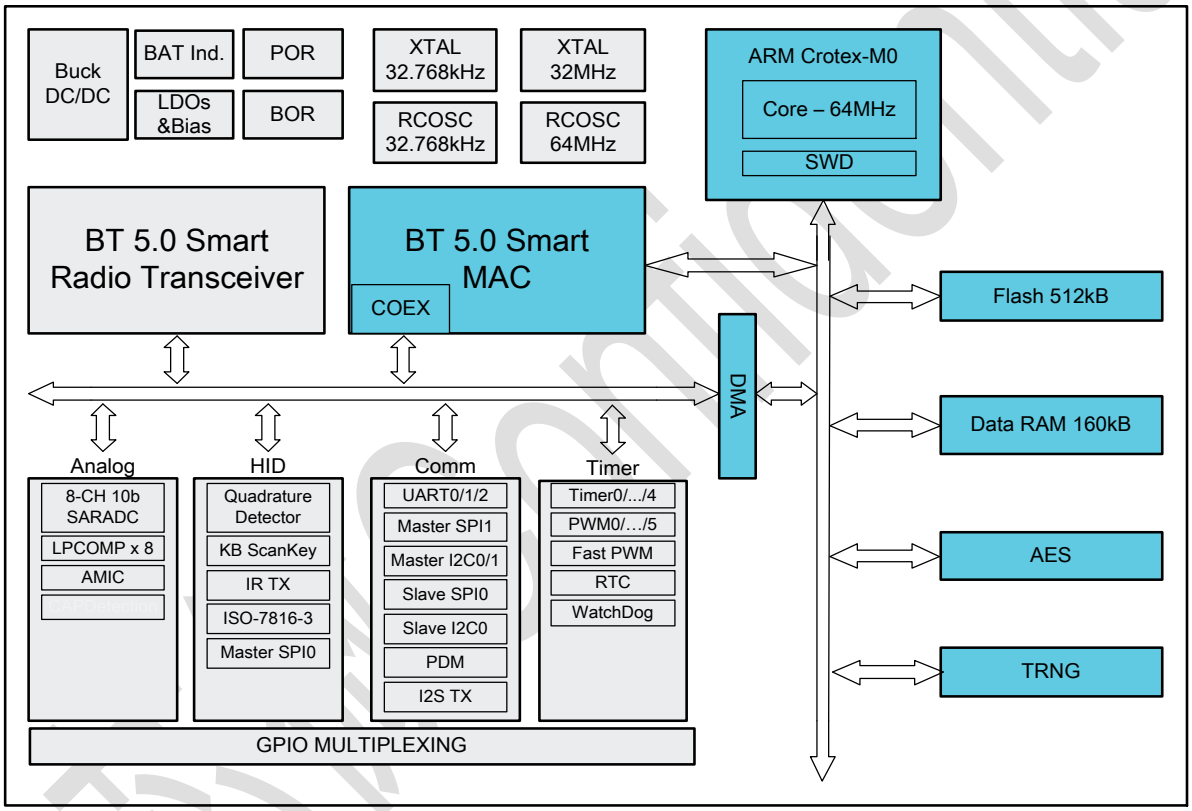


Figure 1. Functional Block Diagram

2.2 Terminology

Term	Description
GND	Ground
BiDir	Bi-Directional
PWM	Pulse Width Modulation
HID	Human Interface Device
GPIO	General Purpose Input / Output

2.3 Pin Assignment and Signal Description

2.3.1 QFN48 Pin Assignment and Signal Description

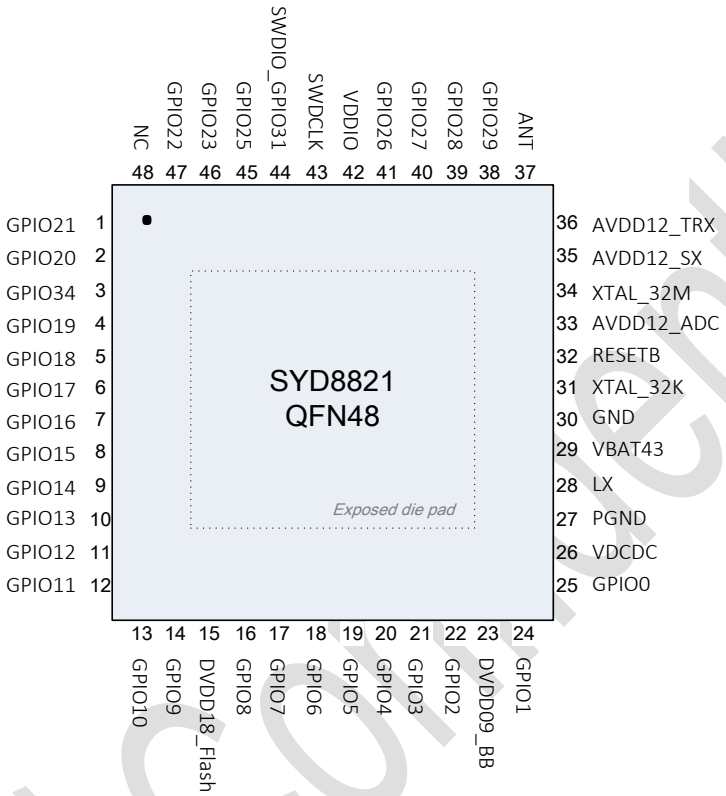


Figure 2. QFN48 pin assignments, top view (6mm*6mm)

Table 1a. QFN48 pin assignments

Pin	Name	Type	Description
Left side of chip			
1	GPIO21	Digital I/O	General purpose I/O
2	GPIO20	Digital I/O	General purpose I/O
3	GPIO34	Digital I/O	General purpose I/O
4	GPIO19	Digital I/O	General purpose I/O
5	GPIO18	Digital I/O	General purpose I/O
6	GPIO17	Digital I/O	General purpose I/O
	CAPDET_7	Analog input	Capacitive touch
7	GPIO16	Digital I/O	General purpose I/O
	CAPDET_6	Analog input	Capacitive touch

Pin	Name	Type	Description
8	GPIO15 CAPDET_5	Digital I/O Analog input	General purpose I/O Capacitive touch
9	GPIO14 CAPDET_4	Digital I/O Analog input	General purpose I/O Capacitive touch
10	GPIO13 CAPDET_3	Digital I/O Analog input	General purpose I/O Capacitive touch
11	GPIO12 CAPDET_2	Digital I/O Analog input	General purpose I/O Capacitive touch
12	GPIO11 CAPDET_1	Digital I/O Analog input	General purpose I/O Capacitive touch
Lower side of chip			
13	GPIO10 CAPDET_0	Digital I/O Analog input	General purpose I/O Capacitive touch
14	GPIO9 AIN9	Digital I/O Analog input	General purpose I/O SAADC input
15	DVDD18_Flash	Power	1.8V flash supply decoupling
16	GPIO8 AIN8	Digital I/O Analog input	General purpose I/O SAADC input
17	GPIO7 AIN7	Digital I/O Analog input	General purpose I/O SAADC input LPCOMP input
18	GPIO6 AIN6	Digital I/O Analog input	General purpose I/O SAADC input LPCOMP input
19	GPIO5 AIN5	Digital I/O Analog input	General purpose I/O SAADC input LPCOMP input
20	GPIO4 AIN4	Digital I/O Analog input	General purpose I/O SAADC input LPCOMP input

Pin	Name	Type	Description
21	GPIO3 AIN3	Digital I/O Analog input	General purpose I/O SAADC input LPCOMP input
22	GPIO2 AIN2	Digital I/O Analog input	General purpose I/O SAADC input LPCOMP input
23	DVDD09_BB	Power	0.9 V regulator digital supply decoupling
24	GPIO1 AIN1	Digital I/O Analog input	General purpose I/O SAADC input LPCOMP input
Right side of chip			
25	GPIO0 AIN0	Digital I/O Analog input	General purpose I/O SAADC input LPCOMP input
26	VDCDC	Power	DCDC output for internal LDOs
27	PGND	Power	DCDC Dirty Ground
28	LX	Power	Switch Node with connecting to inductor. Keep PCB trace as short and wide as possible
29	VBAT43	Power	Battery Power supply
30	GND	Power	Ground
31	XTAL_32K	Analog input	Connection for 32.768kHz crystal
32	RESETB		System reset, low effective
33	AVDD12_ADC	Power	Internal LDO input for ADC, recommend to place a 0.1uF capacitor close to Pin45
34	XTAL_32M	Analog input	Connection for 32 MHz crystal
35	AVDD12_SX	Power	Internal LDO input for PLL, recommend to place a 0.1uF capacitor close to Pin47
36	AVDD12_TRX	Power	Internal LDO input for TRX, recommend to place a 0.1uF capacitor close to Pin48
Upper side of chip			
37	ANT	RF	Single-ended radio antenna connection
38	GPIO29	Digital I/O	General purpose I/O

Pin	Name	Type	Description
	AMIC_INP	Analog input	AMIC input +
39	GPIO28 AMIC_INN	Digital I/O Analog input	General purpose I/O AMIC input -
40	GPIO27 AMIC_BIAS	Digital I/O Analog input	General purpose I/O AMIC_BIAS
41	GPIO26 AMIC_VREF	Digital I/O Analog input	General purpose I/O AMIC_VREF
42	VDDIO	Power	GPIO Power supply
43	SWDCLK	Digital input	Serial wire debug clock input for debug and programming
44	SWDIO GPIO31	Digital I/O	Serial wire debug I/O for debug and Programming General purpose I/O
45	GPIO25	Digital I/O	General purpose I/O
46	GPIO23	Digital I/O	General purpose I/O
47	GPIO22	Digital I/O	General purpose I/O
48	NC	NC	No connection
Bottom of chip			
Die pad	VSS	Power Ground pad	Exposed die pad must be connected to ground (VSS)

2.3.2 QFN32 Pin Assignment and Signal Description

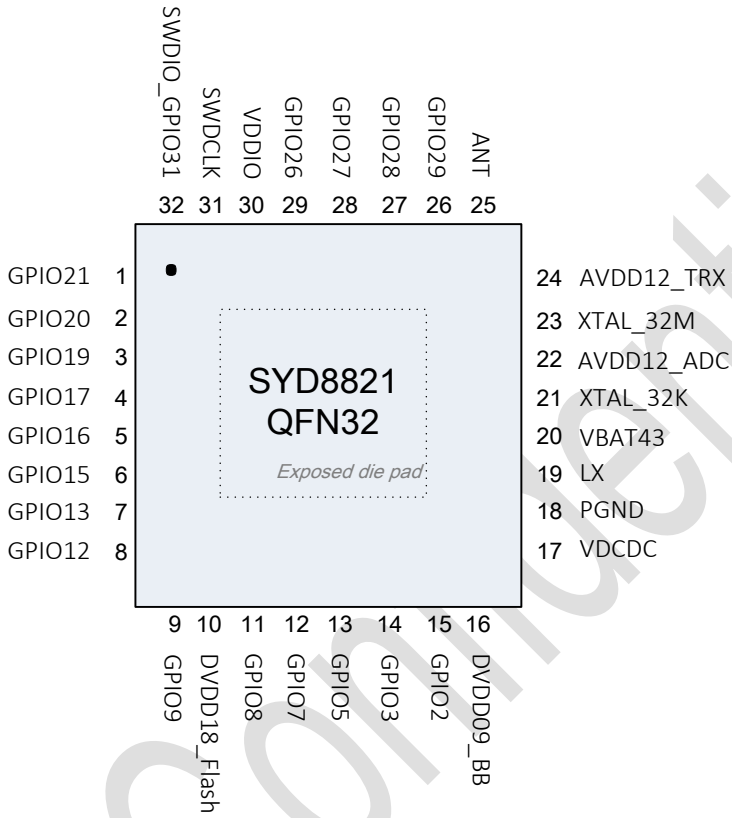


Figure 3. QFN32 pin assignments, top view (4mm*4mm)

Table 2b. QFN32pin assignments

Pin	Name	Type	Description
Left side of chip			
1	GPIO21	Digital I/O	General purpose I/O
2	GPIO20	Digital I/O	General purpose I/O
3	GPIO19	Digital I/O	General purpose I/O
4	GPIO17	Digital I/O	General purpose I/O
	CAPDET_7	Analog input	Capacitive touch
5	GPIO16	Digital I/O	General purpose I/O
	CAPDET_6	Analog input	Capacitive touch
6	GPIO15	Digital I/O	General purpose I/O
	CAPDET_5	Analog input	Capacitive touch

Pin	Name	Type	Description
7	GPIO13 CAPDET_3	Digital I/O Analog input	General purpose I/O Capacitive touch
8	GPIO12 CAPDET_2	Digital I/O Analog input	General purpose I/O Capacitive touch
Lower side of chip			
9	GPIO9 AIN9	Digital I/O Analog input	General purpose I/O SAADC input
10	DVDD18_Flash	Power	1.8V flash supply decoupling
11	GPIO8 AIN8	Digital I/O Analog input	General purpose I/O SAADC input
12	GPIO7 AIN7	Digital I/O Analog input	General purpose I/O SAADC input LPCOMP input
15	GPIO5 AIN5	Digital I/O Analog input	General purpose I/O SAADC input LPCOMP input
16	GPIO3 AIN3	Digital I/O Analog input	General purpose I/O SAADC input LPCOMP input
Right side of chip			
17	VDCDC	Power	DCDC output for internal LDOs
18	PGND	Power	DCDC Dirty Ground
19	LX	Power	Switch Node with connecting to inductor. Keep PCB trace as short and wide as possible
20	VBAT43	Power	Battery Power supply
21	XTAL_32K	Analog input	Connection for 32.768kHz crystal
22	AVDD12_ADC	Power	Internal LDO input for ADC, recommend to place a 0.1uF capacitor close to Pin45
23	XTAL_32M	Analog input	Connection for 32 MHz crystal
24	AVDD12_TRX	Power	Internal LDO input for TRX, recommend to place a 0.1uF capacitor close to Pin48
Upper side of chip			

Pin	Name	Type	Description
25	ANT	RF	Single-ended radio antenna connection
26	GPIO29 AMIC_INP	Digital I/O Analog input	General purpose I/O AMIC input +
27	GPIO28 AMIC_INN	Digital I/O Analog input	General purpose I/O AMIC input -
28	GPIO27 AMIC_BIAS	Digital I/O Analog input	General purpose I/O AMIC_BIAS
29	GPIO26 AMIC_VREF	Digital I/O Analog input	General purpose I/O AMIC_VREF
30	VDDIO	Power	GPIO Power supply
31	SWDCLK	Digital input	Serial wire debug clock input for debug and programming
32	SWDIO GPIO31	Digital I/O	Serial wire debug I/O for debug and Programming General purpose I/O
Bottom of chip			
Die pad	VSS	Power Ground pad	Exposed die pad must be connected to ground (VSS)

Table 3. IO Mode Selection –Part1

GPIO_#	0	1	2	3	4	5
GPIO0	GPIO0	Analog Input_9				Key_Out_0
GPIO1	GPIO1	Analog Input_8				Key_Out_1
GPIO2	GPIO2	Analog Input_7			S_SCLK	Key_Out_2
GPIO3	GPIO3	Analog Input_6			S_MOSI	Key_Out_3
GPIO4	GPIO4	Analog Input_5			S_CSN	Key_Out_4
GPIO5	GPIO5	Analog Input_4			S_MISO	Key_Out_5
GPIO6	GPIO6	Analog Input_3	MOTION_Wake_UP			Key_Out_6
GPIO7	GPIO7	Analog Input_2	Mouse Key (BL)			Key_Out_7
GPIO8	GPIO8	Analog Input_1	Mouse Key (BR)			Key_In_0
GPIO9	GPIO9	Analog Input_0	Mouse Key (BM)			Key_In_1
GPIO10	GPIO10	CAPDET_0	Mouse Key (CPI)	M_SCLK_1		Key_In_2
GPIO11	GPIO11	CAPDET_1	Mouse Key (B4)	M_MISO_1		Key_In_3
GPIO12	GPIO12	CAPDET_2	Mouse Key (B5)	M_CSN_1		Key_In_4

GPIO13	GPIO13	CAPDET_3	MOTION_Wake_UP	M_MOSI_1		Key_In_5
GPIO14	GPIO14	CAPDET_4				Key_In_6
GPIO15	GPIO15	CAPDET_5	Mouse Key (Z1)	M_SCLK_1		Key_In_7
GPIO16	GPIO16	CAPDET_6	Mouse Key (Z2)	M_MISO_1		Key_Out_8
GPIO17	GPIO17	CAPDET_7		M_CSN_1		Key_Out_9
GPIO18	GPIO18	CAPDET_8		M_MOSI_1		Key_Out_10
GPIO19	GPIO19	CAPDET_9		M_SCLK_1		Key_Out_11
GPIO20	GPIO20	CAPDET_10		M_MISO_1		Key_Out_6
GPIO21	GPIO21	CAPDET_11		M_MOSI_1		Key_Out_10
GPIO22	GPIO22	CAPDET_12	Mouse Key (T1)	M_SCLK_1	S_SCLK	Key_Out_12
GPIO23	GPIO23	CAPDET_13	Mouse Key (T2)	M_MISO_1	S_MOSI	Key_Out_13
GPIO34	GPIO34					
GPIO25	GPIO25	CAPDET_15		M_MOSI_1	S_MISO	Key_Out_15
GPIO26	GPIO26			M_SCLK_0	M_SCLK_0	Key_Out_16
GPIO27	GPIO27			M_SDI_0	M_SDIO_0	Key_Out_17
GPIO28	GPIO28			M_CSN_0	M_CSN_0	Key_Out_18
GPIO29	GPIO29		Mouse Key (BL)	M_SDO_0		Key_Out_19
ICE_DATA	GPIO31	ICE_DATA	Mouse Key (BR)			Key_Out_0

Table 4. IO Mode Selection –Part2

GPIO_#	6	7	8	9	10	11
GPIO0	M_I2C_SCL_0	UART_RXD_1			PWM/LED_0	7816_DET
GPIO1	M_I2C_SDA_0	UART_TXD_1			PWM/LED_1	7816_CLK
GPIO2	M_I2C_SCL_1	UART_RXD_0		PDM_CLK	PWM/LED_2	7816_DATA
GPIO3	M_I2C_SDA_1	UART_TXD_0		PDM_DATA	PWM/LED_3	7816_RST
GPIO4	S_I2C_SCL	UART_RXD_1			PWM/LED_4	7816_VCCCTL
GPIO5	S_I2C_SDA	UART_TXD_1			PWM/LED_5	IR_TX
GPIO6		UART_RXD_0			PWM/LED_0	
GPIO7		UART_TXD_0	FastPWM_0	M_I2S_MCLK	PWM/LED_1	
GPIO8	M_I2C_SCL_1	UART_CTS_0	FastPWM_1	M_I2S_SCLK	PWM/LED_2	
GPIO9	M_I2C_SDA_1	UART_RTS_0	FastPWM_2	M_I2S_LRCLK	PWM/LED_3	
GPIO10			FastPWM_3	M_I2S_SDO	PWM/LED_4	
GPIO11				M_I2S_SDI	PWM/LED_5	
GPIO12	M_I2C_SCL_0	UART_RXD_0			PWM/LED_0	
GPIO13	M_I2C_SDA_0	UART_TXD_0			PWM/LED_1	
GPIO14	M_I2C_SCL_1	UART_CTS_2			PWM/LED_2	

GPIO15	M_I2C_SDA_1	UART_RTS_2			PWM/LED_3	IR_TX
GPIO16	S_I2C_SCL	UART_RXD_2			PWM/LED_4	
GPIO17	S_I2C_SDA	UART_TXD_2			PWM/LED_5	
GPIO18		UART_CTS_0			PWM/LED_0	
GPIO19		UART_RTS_0	FastPWM_0		PWM/LED_1	
GPIO20	M_I2C_SCL_1	UART_RXD_0	FastPWM_1	PDM_CLK	PWM/LED_2	
GPIO21	M_I2C_SDA_1	UART_TXD_0	FastPWM_2	PDM_DATA	PWM/LED_3	
GPIO22	M_I2C_SCL_0		FastPWM_3		PWM/LED_4	
GPIO23	M_I2C_SDA_0				PWM/LED_5	IR_TX
GPIO34						
GPIO25					PWM/LED_1	7816_VCCCTL
GPIO26	M_I2C_SCL_1	UART_RXD_2	FastPWM_0	AMIC_VREF	PWM/LED_2	7816_DET
GPIO27	M_I2C_SDA_1	UART_TXD_2	FastPWM_1	AMIC_BIAS	PWM/LED_3	7816_CLK
GPIO28		UART_CTS_2	FastPWM_2	AMIC_INN	PWM/LED_4	7816_DATA
GPIO29		UART_RTS_2	FastPWM_3	AMIC_INP	PWM/LED_5	7816_RST
ICE_DATA					PWM/LED_1	

3.0 Operating Specifications

3.1 Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
VBAT4V3 Voltage	V_{BAT3V}	-0.4	V_{BAT4V3}+0.1	V	
I/O Voltage	V_{DDIO}	-0.4	V_{DDIO}+0.3	V	
Relative Humidity	RH	0	50	%	Non-condensing, Non-biased
ESD	ESD_{HBM}		2	kV	Class 2 on all pins, as per human body model. JESD22-A114E with 15 sec zap interval.

Notes:

1. At room temperature.
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability.
4. Functional operation under absolute maximum-rated conditions is not implied and should be restricted to the Recommended Operating Conditions.

3.2 Recommended Operating Conditions

Table 6. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature	T_A	-40	25	85	°C	
Operating Junction Temperature	T_J	-40	-	85	°C	
Power Supply Voltage for Buck DCDC converter	V_{BAT4V3}	1.7	3.0	4.3	V	Buck DCDC Power input supply. Includes ripples
I/O Supply Voltage	V_{DDIO}	1.7	3.0	3.6	V	
Power Regulator Output Voltage	V_{DVDD09_BB}	0.9	1.1	1.35	V	Power for internal digital circuit
	V_{DVDD18_Flash}	1.7	1.8	2.1	V	Power for internal flash
Serial Clock Frequency	SPI_CLK	-	16	-	MHz	
	I2C_SCL	-	400[1]	1000	KHz	

Note: SYDTEK does not guarantee the performance if the operating temperature is beyond the specified limit.

3.3 Thermal Specifications

Table 7. Thermal Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T_S	-20	-	125	°C	
Lead-free Solder Temperature	T_P	-	-	245	°C	Refer to Package Handling Information document

3.4 DC Characteristics

Table 8. DC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
DCDC Converter Input Voltage	V_{BAT3V}	1.7	4.2	4.3	V	
DCDC Converter Output Voltage	V_{Buck_OUT}	0.9	1.1	-	V	
DCDC Converter Output Current	I_{Buck_Out}	-	-	40	mA	Max current w/i keep setting output voltage
DCDC Converter Output Ripple	R_{Buck}	-	30	-	mV	Max. Ripple on DCDC converter output (Peak to Peak)
Power Consumption[2]						
TX RF Current @ Pout=0dBm			4.3		mA	@V_{BAT4V3} = 3V with DCDC Buck enable
RX RF Current @ -94dBm sense.			2.4		mA	@V_{BAT4V3} = 3V with DCDC Buck enable
Supply Current @ Sleep	I_{SLEEP}	-	6	-	µA	@V_{BAT4V3} = 3V with DCDC Buck enable
Supply Current @ Power Down	I_{PD}	-	<1	-	µA	@V_{BAT4V3} = 3V with DCDC Buck enable

Notes:

1. Electrical Characteristics are defined under recommended operating conditions.
2. All the parameters are tested under operating conditions: V_{BAT4V3} = 3 V, DCDC Buck bypass mode at T_A = 25°C

3.5 AC and Timing Characteristics

3.5.1 Power-On Sequence

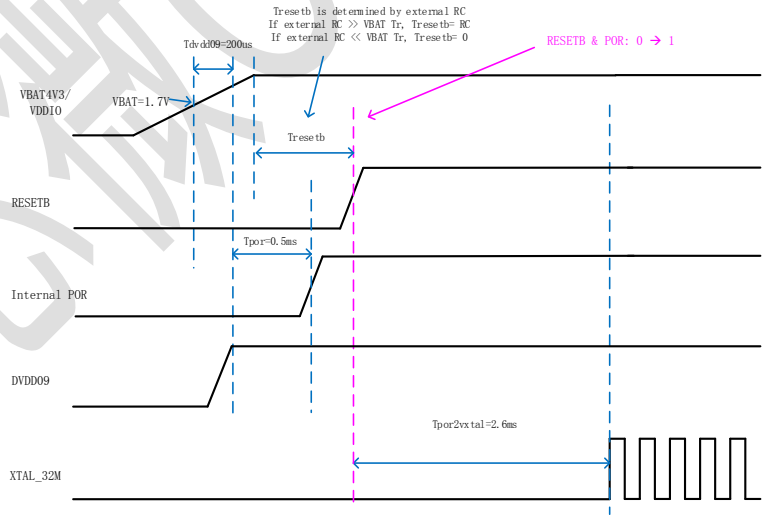


Figure 4. Power-On Sequence

3.5.2 32MHz Crystal Oscillator

The 32MHz crystal oscillator is designed for low power consumption and high stability. The 32MHz oscillator can be trimmed without external capacitors. A group of digital controlled trimming loading capacitors are integrated and optimally designed for 9pF XTAL with 50ohm ESR max. Digital controlled capacitors could ease and speed up tuning procedure of XTAL frequency accuracy. The simplified schematic of the 32MHz crystal is shown in Figure 5.

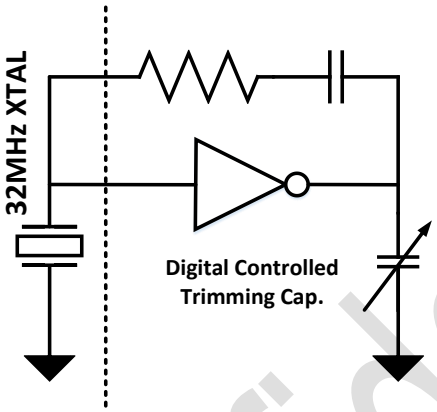


Figure 5. 32MHz Crystal Oscillator Circuit

Table 9. 32MHz Crystal Oscillator Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Crystal Oscillator Frequency	F_{X32M}	-	32		MHz	
Crystal Oscillator Frequency tolerance	F_{X32M_TOL}	-	±10	±20	ppm	Frequency tolerance depends on XTAL Spec.
Equivalent series Resistor	ESR_{X32M}		30	60	Ω	
Loading Capacitor	C_{L_X32M}		9.0		pF	Built in digital controlled trimming loading cap, no external cap needed.
XTAL Drive Power	P_{DRIVE_X32M}			100	uW	
XTAL Start Up Time	T_{START_X32M}		0.4	1	ms	

Notes: Electrical Characteristics are defined under recommended operating conditions

Carrier Drift and Drift Rate are major test items in RF BQB verification, XTAL would have influence on modulation performance and connection stability. Here are several XTALs verified by SYDTEK and listed below:

Hosonic Electronic Co., Ltd.
a. 32MHz, 3225 , 9pF, ESR 50ohm max, -40~+85, +/-10ppm, P/N: E3SB32E003800E
b. 32MHz, 2520, 9pF, ESR 50ohm max, -40~+85, +/-10ppm, P/N: E2SB32E003800E
c. 32MHz, 2016, 9pF, ESR 60ohm max, -40~+85, +/-10ppm, P/N: E1SB32E003800E

HARMONY ELECTRONICS Co., Ltd.
a. 32MHz, 2520 , 9pF, ESR 50ohm max, -40~+85, +/-7ppm, P/N: X2B032000M91H-HT
b. 32MHz, 2016, 9pF, ESR 50ohm max, -40~+85, +/-7ppm, P/N: X2C032000M91H-HT

3.5.3 32.768kHz Crystal Oscillator

The 32.768 kHz oscillator is designed optimally for XTAL with C-Load =12.5pF , and no internal trimming capabilities and 32.768kHz clock is used as the clock source in the Sleep or Power Down modes.

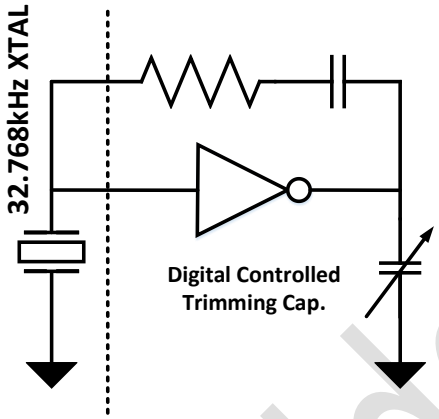


Figure 6. 32.768kHz Crystal Oscillator Circuit

Table 10. 32.768kHz Crystal Oscillator Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Crystal Oscillator Frequency	F_{X32k}		32.768		kHz	
Crystal Oscillator Frequency tolerance	F_{X32k_TOL}		±20		ppm	Frequency tolerance depends on XTAL Spec.
Equivalent series Resistor	ESR_{X32k}		50	80	kΩ	
Load Capacitor	C_{L_X32k}		12.5		pF	Built internal fixed load cap for 12.5pF XTAL
XTAL Drive Power	P_{DRIVE_X32k}			1	uW	
XTAL Start Up Time	T_{START_X32k}		0.3	1	s	

3.5.4 64MHz RC Oscillator

The 64MHz RC oscillator is designed for high speed wake up and high computing power application. Due to characteristic of RC oscillator, calibration process is needed before switching to 64MHz RC oscillator mode.

Table 11. 64MHz RC Oscillator Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
RC Oscillator Frequency	F_{RC64M}		64		MHz	
RC Oscillator Frequency tolerance	F_{RC32M_TOL}		±1	±5	%	Calibration needed before switching to RC oscillator mode
Oscillator Start Up Time	T_{ST_RC64M}		2.5		us	

Notes: Electrical Characteristics are defined under recommended operating conditions

3.5.5 32.768kHz RC Oscillator

The 32.768kHz RC oscillator is designed for low cost applications without additional 32.768kHz XTAL. Due to characteristic of RC oscillator, calibration process is needed before switching to 32.768kHz RC oscillator mode.

Table 12. 32.768kHz RC Oscillator Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
RC Oscillator Frequency	F_{RC32k}		32.768		kHz	
RC Oscillator Frequency tolerance	F_{RC32k_TOL}		±2		%	
RC Oscillator Frequency tolerance, Calibrated	F_{RC32k_TOL}		±250	±500	ppm	Calibration needed before switching to RC oscillator mode
Start Up Time	T_{START_32k}		100	1	us	

Notes: Electrical Characteristics are defined under recommended operating conditions

3.6 RF Specifications

3.6.1 Transmitter RF Specification

Table 13. Transmitter Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Frequency Range	FR_{TX}	2402	-	2480	MHz	
Max. Output Power	$P_{O,MAX}$	-		4	dBm	
Default Output Power	$P_{O,DEF}$		0		dBm	
Output Power Adjust Range	$P_{O,ADJ}$	-30		4	dBm	
Output Power Variation	$P_{O,VAR}$		2.0		dBm	All channels TX power variation
TX 20dB Bandwidth	BW_{20dB}			1150	kHz	
1st Adjacent Channel Power	P_{AJC1}			-20	dBc	
2nd Adjacent Channel Power	P_{AJC2}			-40	dBc	
Delta F1 Frequency Deviation	$\Delta f1_{AVG}$	225		275	kHz	
Delta F2 Frequency Deviation	$\Delta f2_{AVG}$	185			kHz	
AVG Delta F2/ Delta F1	Δf_{AVG}	0.8				Δf2AVG/Δf1AVG
Frequency Offset	F_{OFFSET}	-150		150	kHz	
Carrier Frequency Drift	CF_{DRIFT}			50	kHz	
Carrier Frequency Drift rate	CF_{DRIFT_Rate}			20	kHz/50μs	
2nd Harmonics Power Level	Har_{2nd}			-40	dBm	@Pout = 0dBm
3rd Harmonics Power Level	Har_{3rd}			-45	dBm	@Pout = 0dBm

Notes: Electrical Characteristics are measured under BLE specification and recommended operating conditions

3.6.2 Receiver RF Specification

Table 14. Receiver Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Frequency Range	FR_{RX}	2402		2480	MHz	
Maximum Input Power	RX_{MAX}		0	4	dBm	
Ideal Signal Sensitivity	SEN_{IDEAL}	-95	-94.5	-93	dBm	
Dirty Signal Sensitivity	SEN_{DIRTY}		-94		dBm	
C/I and Selectivity						
C/I Co-Channel	C/I_{CO}		9		dB	
C/I Adjacent +1MHz	C/I_{1M}		-1		dB	
C/I Adjacent +2MHz	C/I_{2M}		-35		dB	
C/I Adjacent≧ +3MHz	C/I_{3M}	-40	-48		dB	
C/I Image Channel	C/I_{IMG}		-25		dB	
C/I Image+1M Channel	C/I_{IMG+1M}		-35		dB	
Inter-Modulation Performance						
IMD performance	IMD		-24		dBm	3rd, 4th and 5th offset channel
Blocking Performance						
Blocking 30~2000MHz	$P_{BLK\_30\sim2000MHz}$	-10	TBD		dBm	
Blocking 2003~2399MHz	$P_{BLK\_2003\sim2399MHz}$	-30	TBD		dBm	
Blocking 2484~2997MHz	$P_{BLK\_2484\sim29}$	-30	TBD		dBm	

Blocking 3000MHz~12.75GHz	$P_{BLK\_3\sim12.75GHz}^{97MHz}$	-10	TBD	dBm

Notes: Electrical Characteristics are measured under BLE specification and recommended operating conditions

4.0 Design References

4.1 Application Schematics

SYD8821 integrates one DCDC buck converter and one 4.7uH needed.

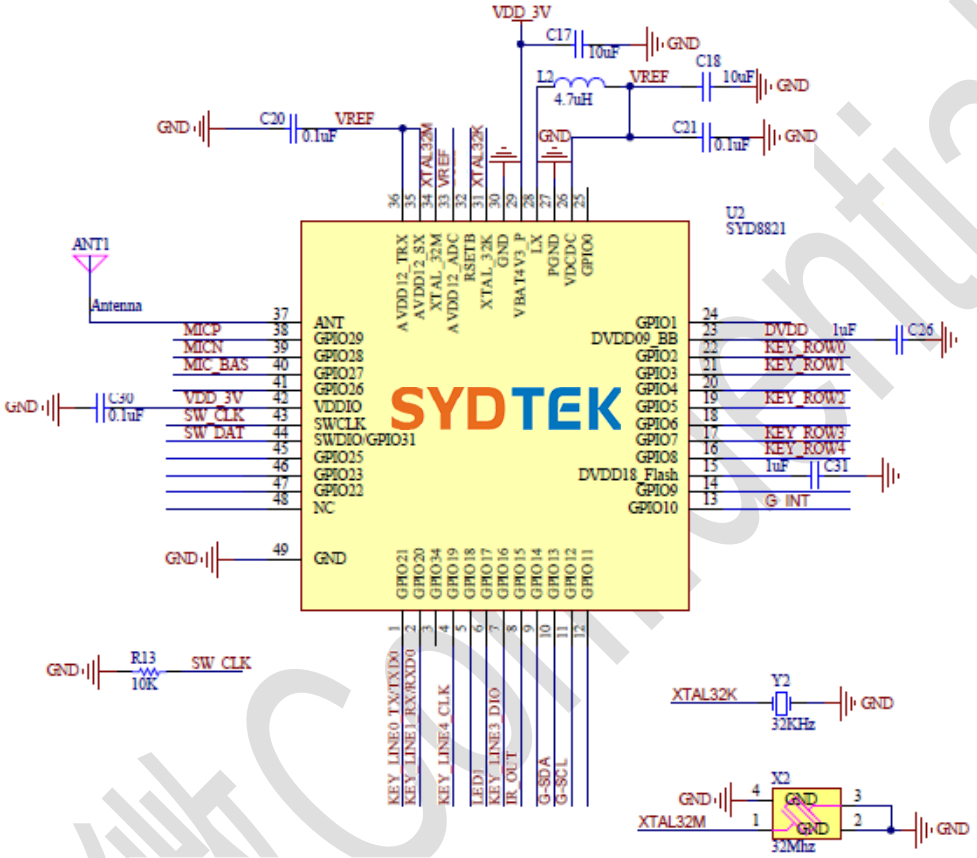


Figure 7. Buck Mode Reference Application Circuit (32k xtal is optional)

Table 15. BOM of SYD8821

Designator	Value	Description	Footprint
C20, C21, C30	100 nF	Capacitor, X5R, ±20%	0402
C26, C31	1 µF	Capacitor, X5R, ±20%	0402
C17, C18	10 µF	Capacitor, X5R, ±20%	0603
L2	4.7 µH	Inductor, IDC,min = 30 mA, ±20%	0603 0806
U1	SYD8821	ULP Bluetooth low energy SoC	QFN-48
X1	32 MHz	32 MHz, CL = 10 pF, Tol: ±10ppm	3225
X2 (optional)	32.768 kHz	32.768 kHz, CL = 12.5 pF, Tol: ±20 ppm	3215

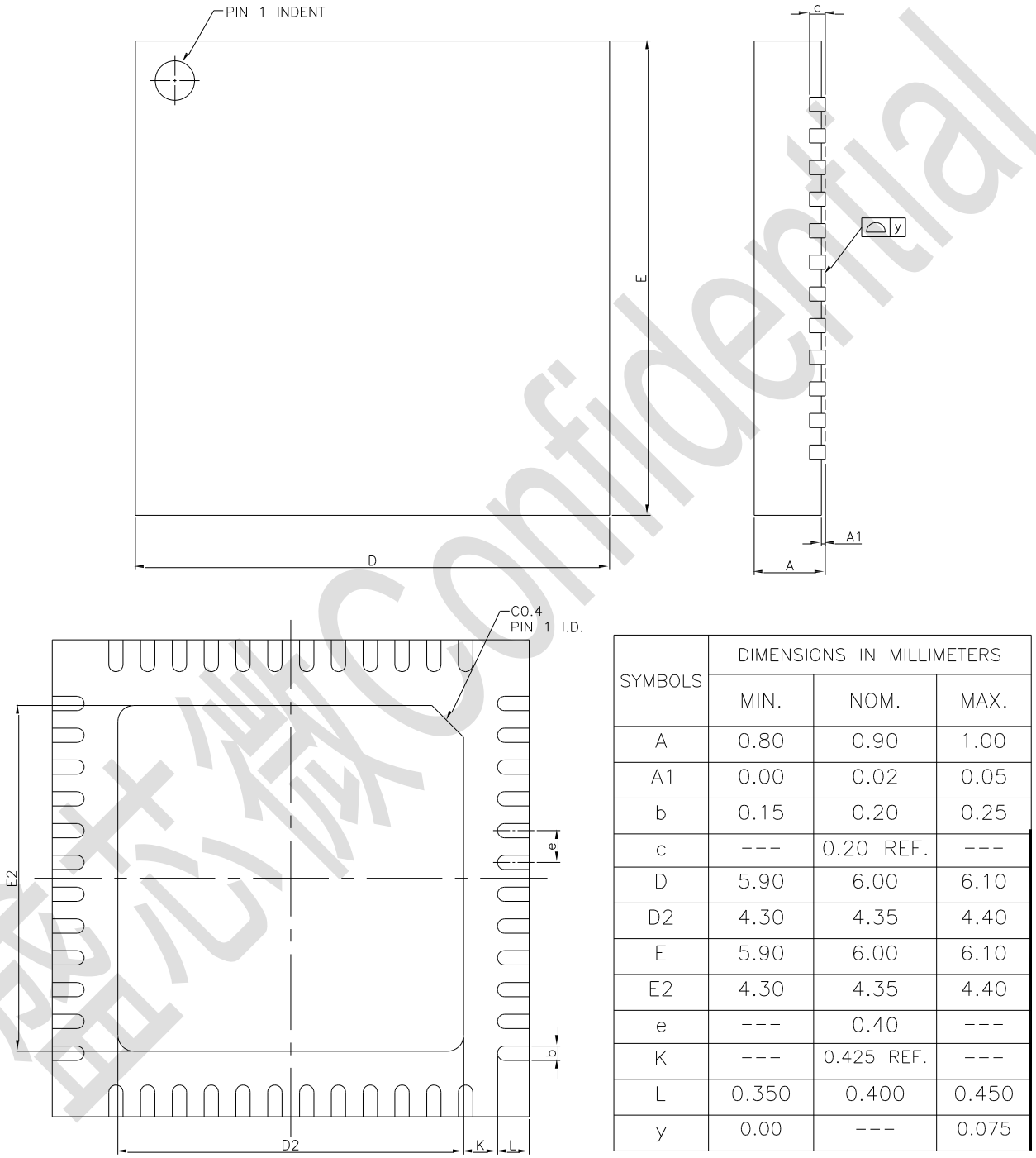
4.2 Layout Design Guidelines

Precaution: PCB layout is extremely important to minimize parasitical capacitance and line inductance.
The following layout guidelines are recommended to achieve optimum performance.

1. Make sure RF 50-ohm trace is with GND continuation.
2. Place the DCDC inductor close to the LX pin. Keep the traces short and wide.
3. Place ceramic bypass capacitors near the input/output pins.
4. All feedback signals must go through the regulator capacitors first.
5. Place the crystal and its components close to the oscillator side and near the oscillator pins.
6. Ensure that the ground plane under the oscillator and its components are in good quality.
7. Avoid long connections to the crystal and also to the load capacitor which may create a large loop on the PCB.
8. Do not route any digital-signal lines on the opposite side of the PCB under the RF trace and crystal area.
9. Keep other digital signal lines, especially clock lines and frequently switching signal lines, as far away from crystal/analog/RF connections as possible.
10. Place at least 9 ground vias directly under IC thermal PAD for good grounding and thermal dissipation.

5.0 Mechanical Specifications

5.1 Mechanical Dimension



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	---	0.20 REF.	---
D	5.90	6.00	6.10
D2	4.30	4.35	4.40
E	5.90	6.00	6.10
E2	4.30	4.35	4.40
e	---	0.40	---
K	---	0.425 REF.	---
L	0.350	0.400	0.450
y	0.00	---	0.075

Figure 8. Package Outline Diagram and Dimension

5.2 Package Marking

Refer to Figure 9 for the code marking location on the device package.

Figure 9. Package Marking

Table 16. Code Identification

Marking	Description
LYWWXXXXXXX	SYD Date Code Y: Assembly year e.g. (Yearly 2018) -> 8 WW: Assembly week e.g. (Weekly 16) -> 16 XXXXX: NO. e.g. 433CE12

6.0 Power States & Sequence

6.1 Operation Mode

State	Functional Description
Power Down	All power supplies are off except I/O for pin wake-up. All clocks are gated. System can be woken up by configured external pin. When it happens, SYD8821 resets from boot-up state.
Sleep	Active clocks (RCOSC 64MHz) are off, and the sleep clock (32.768kHz) remain working. Certain engines' power are off. Two types of sleep modes are provided in SYD8821. When CPU uses 32MHz crystal clock together with Bluetooth, it follows Bluetooth sleep mode aligning to connection interval. When CPU uses internal 64MHz RC clock, it can set CPU sleep mode independently and woken up by timer or Bluetooth interrupts.
Standby	This is the default state after power-up. All clocks are working but the RF is inactive.
TX	This mode is entered when Bluetooth link-layer determines to send transmission packets.
RX	This mode is entered when Bluetooth link-layer determines to receive an incoming packet.

7.0 System Description

7.1 ARM Cortex M0

The ARM® Cortex®-M0 processor is the smallest ARM processor available. It provides low power consumption and minimal code of the processor to enable developers to achieve 32-bit performance. With its friendly architecture, users can develop applications easily and fast.

SYD8821 supports dynamic clock technology for various applications ranging from 8MHz to 64MHz. The CPU clock can be configured to use internal 64MHz RCOSC clock or external 32MHz crystal clock. When using RC clock, MCU can run independently with Bluetooth link-layer and switch on and off at users' discretion. When using 32MHz crystal clock, it should follow the working period of Bluetooth. However, the Bluetooth working period can be determined by MCU.

SWD (Serial-Wire Debug) is supported for powerful debug and trace features with two connection pins.

SYD8821 has 128kB ROM for boot-up and BLE protocol stack, 512kB flash for profile/application, and total 160kB internal SRAM for programing and data usage.

7.2 Memory

Cache Mode: Partial FW code operates in Cache RAM and cache engine would re-load corresponding FW from flash automatically.

Cache Mode

Address	Description	Size
0x00000000	Flash Header & Protocol Setting	4k Byte
0x00001000	Bond Manager (Master)	4k Byte
0x00002000	Bond Manager (Slave)	4k Byte
0x00003000	Profile Paratemers	68k Byte
0x00014000	FW Code 0	216k Byte
0x0004A000	FW Code 1	216k Byte

Figure 10. Data RAM Address Mapping

7.3 Bluetooth Low Energy Core

The Bluetooth Low Energy Core is SIG Qualified. It is fully compliant with Bluetooth Smart v5.0 slave-role controller and provides qualified features as below:

- Bluetooth low energy stack: All layers up to GATT including (PHY, LL, HCI, L2CAP, GAP, SM, ATT/GATT)
- Slave-Role Link layer
  - Slave-required PDU types
  - Encryption/Decryption
- L2CAP
  - Slave connection update
  - Attribute channel
  - Security channel
- GAP/ATT/GATT: Mandatory protocols
- Security Management
  - Key generation and passing
  - Automatic security engine
- DTM: For RF qualification
- Profile configuration
  - Initialization
  - Flexibility and testability

7.4 Cache Mode

SYD8821 supports both cache mode and mirror mode.

In cache mode, the code is executed in 16kB cache RAM, the maximum code size is 490kB, and the maximum available data RAM is 160kB.

- 4-way set associative
- Cacheable range up to 512kB
- Cache Ram size: 16 kB, Tag Ram size: 4 kB

In mirror mode, the code is loaded from flash to SRAM, and the code is executed in SRAM, and hence the maximum code size is 128kB, while the maximum data RAM is 48kB.

The power consumption in mirror mode is about 20% lower than that in mirror mode.

7.5 Radio Transceiver

The SYD8821 integrates high performance 2.4GHz radio transceiver for Bluetooth radio specification. With the built-in on-chip balun, SYD8821 does not need external balun circuit to minimize BOM. The integrated high efficiency PA can transmit up to +4dBm RF power for class 2 operation, while the integrated low-IF receiver can provide excellent sensitivity up to -93dBm and outstanding interference rejection capability.

7.6 DMA

SYD8821 supports DMA, 32byte FIFO is for SPI, and 960byte FIFO is for voice remote controller.

7.7 General Purpose ADC (SAADC)

The SYD8821 integrates a low power 10-bit general purpose Analog-to-Digital Converter (GPADC) with 1MHz sampling rate. For each one shot measurement, it takes 3us for data acquisition. It can operate as a 10-channel ADC by switching the GPADC input. One dedicated channel is for internal Battery Voltage detection (V_{BAT4V3}), while the other ten channels are configured to monitor GPIO0~GPIO9. For better accuracy, internal reference voltage calibration is preferred. Sensing applications as battery monitoring, temperature resister, analog signal sampling could be applied with this GPADC.

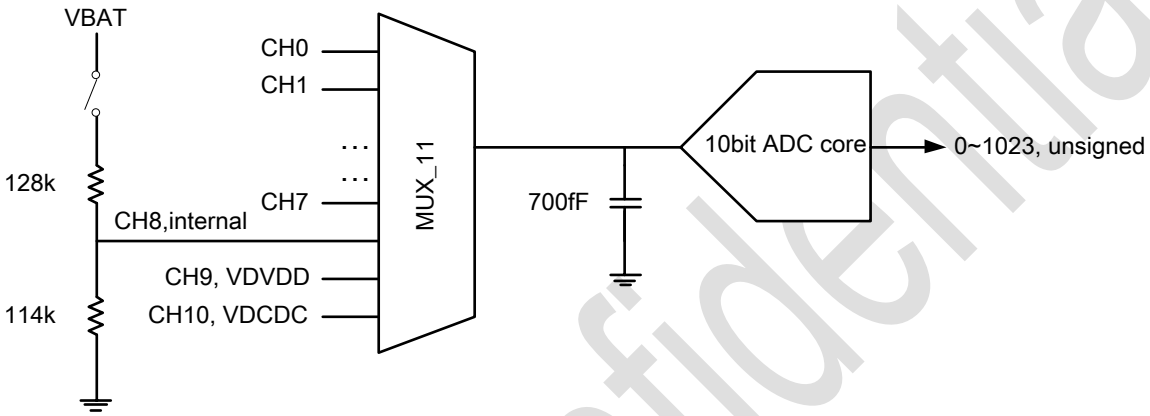


Figure 11. GPADC Internal Channel MUX and Resister Divider Configuration

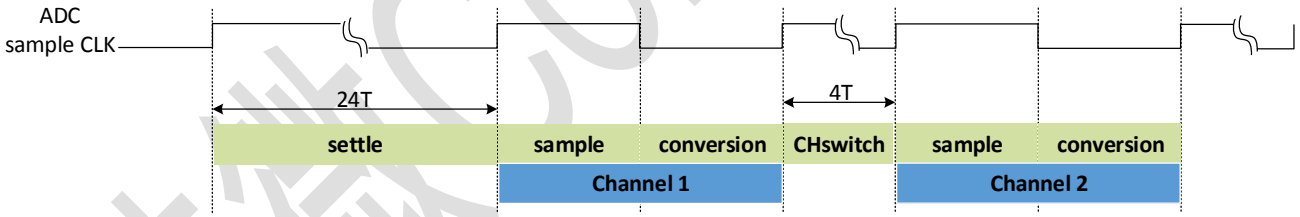


Figure 12. GPADC Conversion Timing

7.8 Power Management

The SYD8821 integrates an power management unit for handheld or wearable devices with buck DC/DC converter. No external Schottky diode is needed for minimal layout area. The DC/DC converter transforms battery voltage to a lower internal voltage with minimal power loss. The DC/DC converter could provide excellent power efficiency with adaptive loading current setting. It can provide power solution for one-cell Lithium-Ion, or two serial alkaline battery applications, 1.8V~4.2V.

7.8.1 Buck Converter

Higher performance DC/DC Buck converter would bring up better battery life time. To ensure longest battery life, Buck converter has an NAP mode under light load current. The reduction in supply voltage level from a high voltage to

a low voltage reduces the peak power drain from the battery. For better conversion efficiency, DC resistance (R_{DC}) of Inductor should be less than 0.25ohm.

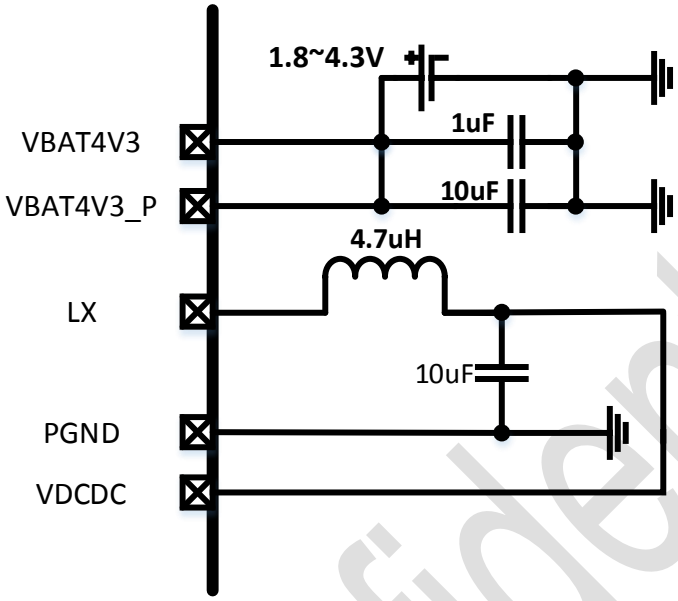


Figure 13. DC/DC Buck Converter Configuration

Table 17. Buck Converter Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Voltage	$V_{In,Buck}$	1.8	3.0	4.3	V	
Output Voltage	$V_{DCDC,Buck}$	0.9	1.1	1.2	V	
Converting Efficiency	Eff_{Buck}		88		%	@20mA Loading current
Maximum Load Current	$I_{Load,Buck}$			40	mA	
Output Ripple Voltage	$V_{RIPPLE,Buck}$		30		mV	

7.9 GPIO

SYD8821 offer 31 GPIOs. GPIO could be set with internal Pulled-up(GPIO0~ GPIO31). Max driving current of each GPIO is 2mA (4mA optional).

7.10 Timer

SYD8821 provide 5 timers(timer0~timer3 are with 16-bit width, timer4 is with 24-bit width, running with 32.768kHz clock from 32.768kHz XTAL or LPO), timer interrupt can wakeup CPU from sleep or power down mode. Timer0 is reserved for Rom Code.

7.11 Watch Dog Timer (WDT)

SYD8821 offer one 32-bit CRV(Counter reload value) countdown watchdog timer for supervisor purpose. It also runs at 32.768kHz clock for maximum 131072sec supervisor time to execute system reset due to a hardware fault or program error.

The watchdog's timeout period is given by: Timeout [s] = (CRV + 1) / 32768

7.11.1 Reload criteria

The watchdog has eight separate reload request registers, which shall be used to request the watchdog to reload its counter with the value specified in the CRV register. To reload the watchdog counter, the special value 0x5F763214 needs to be written to all enabled reload registers. One or more RR registers can be individually enabled through the RREN register.

7.11.2 Watchdog reset

A TIMEOUT event will automatically lead to a watchdog reset equivalent to a system reset. Once the TIMEOUT event has been generated, the impending watchdog reset system.

7.12 Real Time Clock (RTC)

SYD8821 provides one RTC timer for real time clock application. Clock source would be from 32.768kHz XTAL or internal 32.768kHz RC clock. SYD8821 RTC includes two alarms with two interrupt outputs. Calendar supports seconds, minutes, hours and days (up to 7days).

8.0 Peripheral

8.1 Hardware Keyscan

SYD8821 provides an 8x20 keyscan decoder for maximum 8 rows and 20 columns. The row and column could be assigned in specified IO for flexible configuration and layout.

When key is pressed, the keyscan circuit would auto scan the defined matrix and report to firmware in FIFOs.

8.2 Quadrature Decoder

SYD8821 provides a quadrature decoder for HID application. It could detect quadrature encoder signals and report to firmware in FIFOs. Also can support sleep wakeup.

8.3 Low Power Comparator

SYD8821 provides 8 channels Low Power Comparator with 15 steps and selectable reference voltage. In System ON, the LPCOMP can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the selected reference. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog system wakeup source. The comparator threshold can be programmed to a range of fractions of the supply voltage.

Main features of LPCOMP:

- 0 - VDDIO input range
- Eight input options (Analog Input_0 to Analog Input_7)
  - Reference voltage options: 15-level internal reference ladder (VDDIO/16)
  - Two external analog reference inputs (Analog Input_0 and Analog Input_1)
- Wakeup source from OFF mode

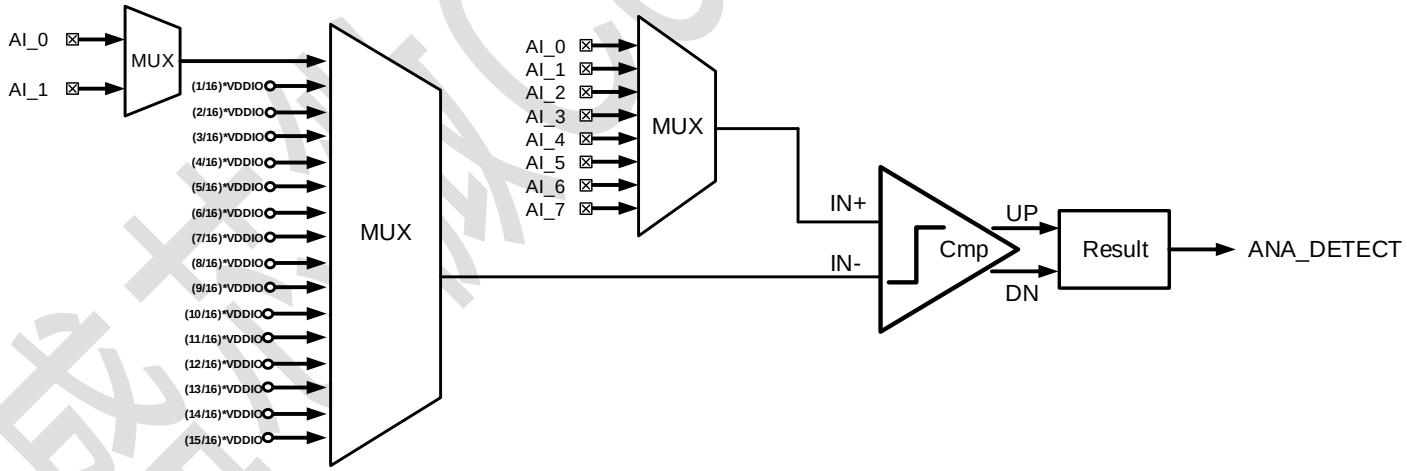


Figure 14. Low power comparator

Table 18. LPCOMP Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Reference Power of LPCOMP	P_{LPCOMP}	1.8		3.6	V	Refer to VDDIO
Input offset error*	V_{IOE}	-20		+20	%	

Notes: Depend on actual IO current loading

8.4 PWM

SYD8821 integrates four channel low speed PWM and six channel high speed PWM.

8.4.1 High speed PWM

SYD8821 provides one FastPWM module which implements an up or up & down counter with four PWM channels. A built-in decoder and DMA make SYD8821 can control PWM duty cycle without CPU intervention. Multiple duty-cycle arrays (Sequence0 & sequence1) are defined in data RAM and data RAM sequences could be repeated or loop mode.

8.4.1.1 Wave Counter

SYD8821 FastPWM provides two type counter (Up or Up&Down) for generating pulse with different duty-cycle. Which depends on the compare values.SYD8821 offers 15bits REG for counter top value. All four channels will share the same period (PWM clock), but can have individual duty-cycle and polarity. Register table has setting description details.

8.4.1.2 Up mode

PWM period: TPWM(Up) = TPWM_CLK * COUNTERTOP

Step: Tsteps = TPWM_CLK

Compare period: Tcompare=TPWM_CLK*Compare

Duty cycle=[(TPWM(Up)-Tcompare)/TPWM(Up)]*100%

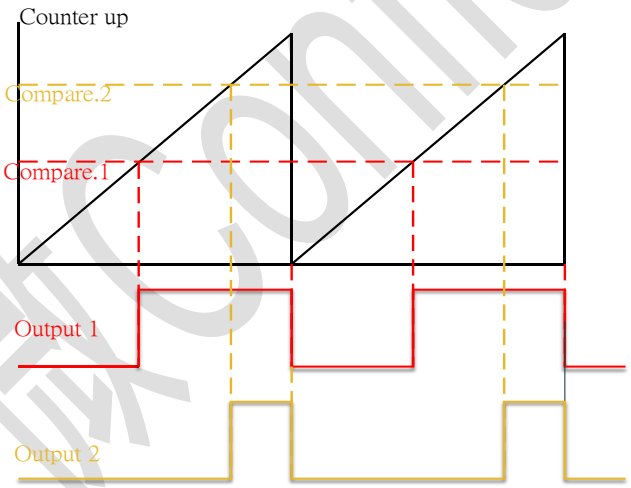


Figure 15. FastPWM Timing – Up Mode

8.4.1.3 Up & Down mode

PWM period: TPWM(Up&Down) = TPWM_CLK *2* COUNTERTOP

Step: Tsteps = TPWM_CLK*2

Compare period: Tcompare=TPWM_CLK*Compare*2

Duty cycle=[(TPWM(Up&Down)-Tcompare)/TPWM(Up&Down)]*100%

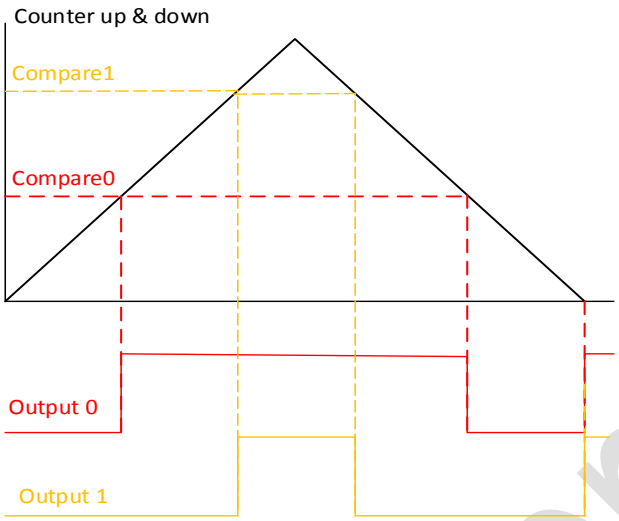


Figure 16. FastPWM Timing – Up & Down Mode

8.4.1.4 Decoder

The DECODER uses DMA to controls how the RAM content is interpreted and loaded to the internal compare registers. The load data can be configured which are stored in RAM and routed to the various compare channels in the different modes (Common / grouped /individual /waveform). For more details, register table has setting description details.

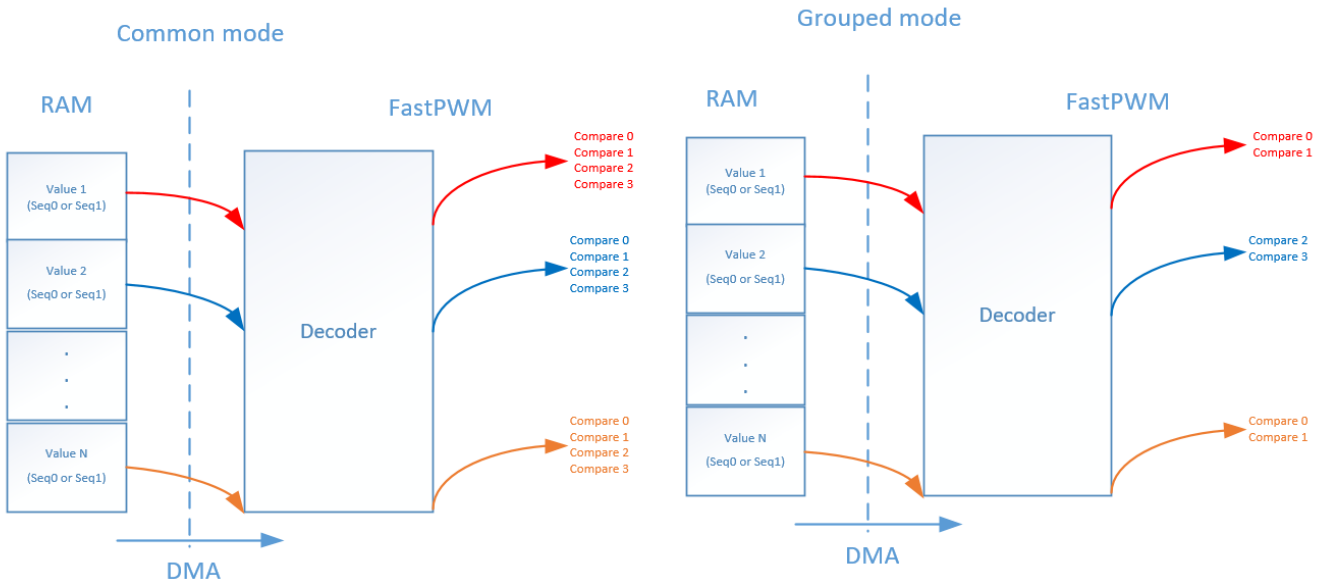


Figure 17. FastPWM Timing –Common & Grouped mode Mode

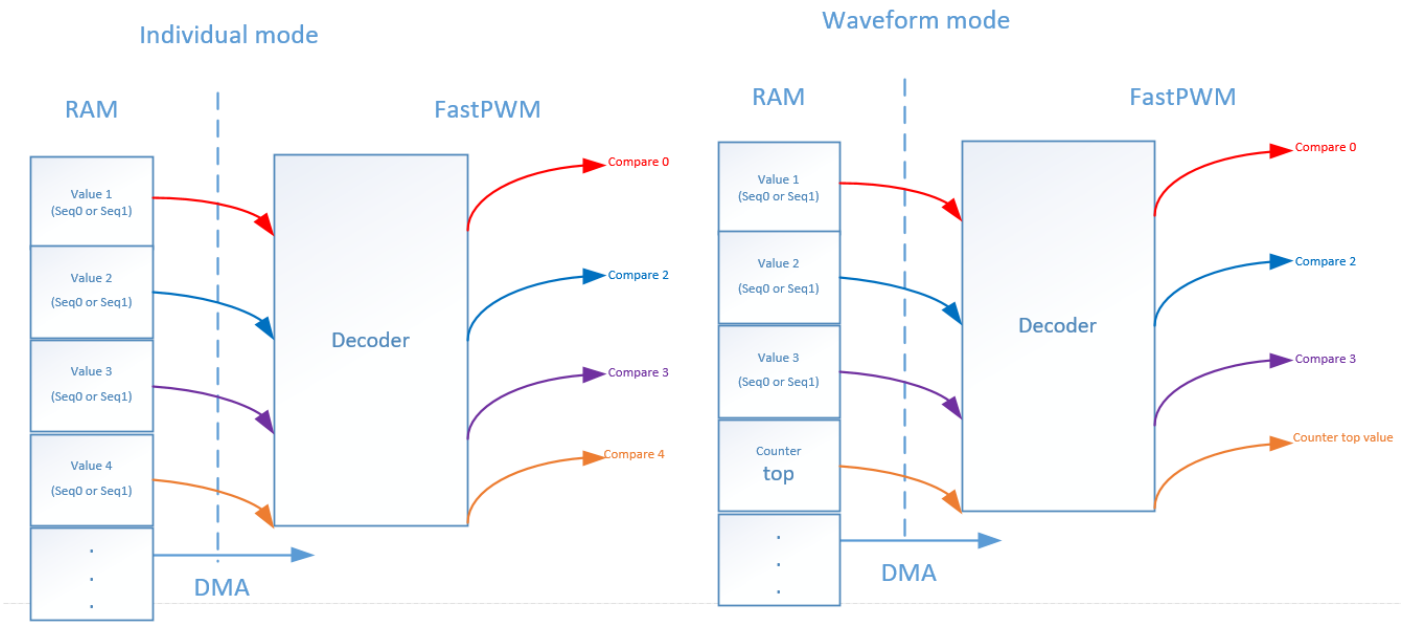


Figure 18. FastPWM Timing –Individual & Waveform mode Mode

8.4.2 Low speed PWM (LED Controller)

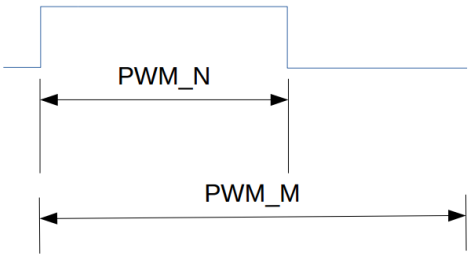


Figure 19. Low speed PWM Timing Setting Diagram

SYD8821 integrates four adjustable PWM generators which are controlled by individual register and could be mux out at three different GPIOs. The minimum positive or negative width of PWM is 1/32ms and flexible setting ranges from 1 to 255 steps. Buzzer or LED diming could be controlled by PWM signal with pre-defined PWM duty.

SYD8821 integrate LED controller which provide general On-OFF mode and Breathing light mode. The minimum LED on width is 1/32s with max 255 steps. LED ON-OFF repetition times could be configured as continuous or 1~127 times. Register table has setting description details. T1, T2, T3 are 8-bit width control register with minimum step 31.25ms.

For Breathing light mode, min, max, T4 are 8-bit width control register with minimum step 0.5ms. The sp is defined as breath mode speed with 4-bit width control resister with minimum step, 31.25us.

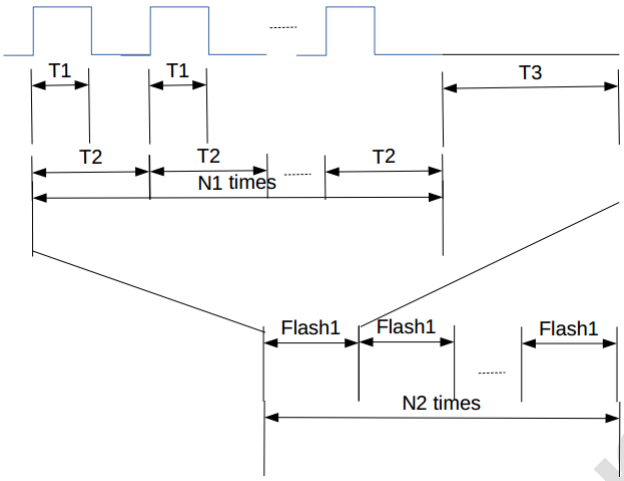


Figure 20. LED ON-OFF Setting Diagram

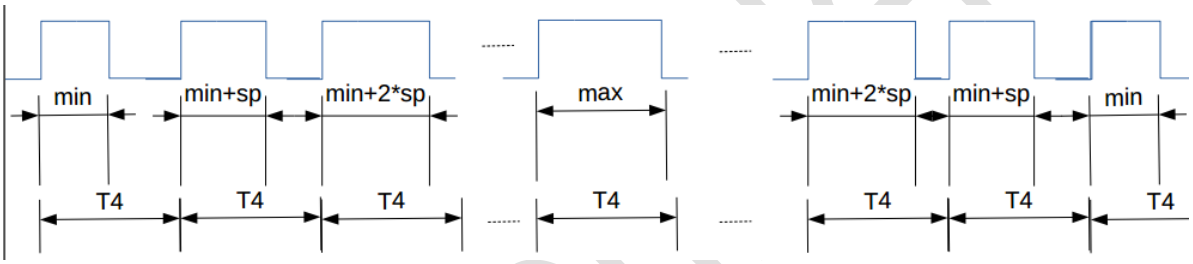


Figure 21. LED Breathing Light Setting Diagram

9.0 Interfaces

9.1 UART

The SYD8821 has three sets of UART interface (UART0, UART1 & UART2) for serial asynchronous communication between devices.

9.1.1 UART0 & 1

UART 0&1 supports following features. 8bit data length, parity check and 1bit stop bit format. Integrates 8bytes T/RX FIFO. UART 0 also supports CTS/RTS HW flow control for options.

9.1.2 UART2

UART 2 supports following features. 7 or 8bit data length, parity check and 1 or 2bit stop bit format. Integrates 16bytes T/RX FIFO. UART2 supports CTS/RTS HW flow control for options, and it has selectable receiver FIFO threshold values (1byte, 1/4 full FIFO size, 1/2 full FIFO size, 2bytes less than full FIFO size).

Figure 22. UART Data Frame

Table 19. UART Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Baud Rate	BR	1200		921600	bps	
Baud Rate Accuracy	BR_{ACCU}			3.0	%	

9.2 I2C

The SYD8821 has two sets of I2C Master(I2C_0, I2C_1) & 1 I2C salve (I2C_S) for 2-wire bi-directional communication. The I2C supports wide range of data rate up to 400kHz in register controls. Multiple Read modes are supported as current read, random read, and sequential read. Write mode also support byte write and page write (Up to 256bytes).

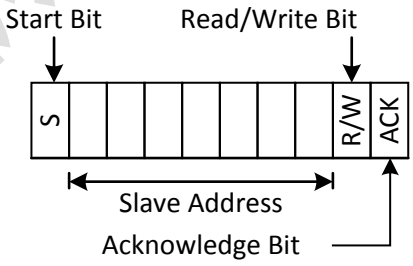


Figure 23. I2C Control Byte Format

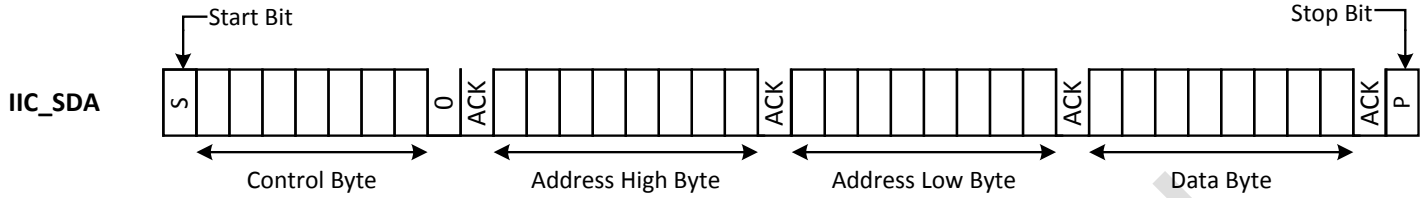


Figure 24. I2C Byte Write Format

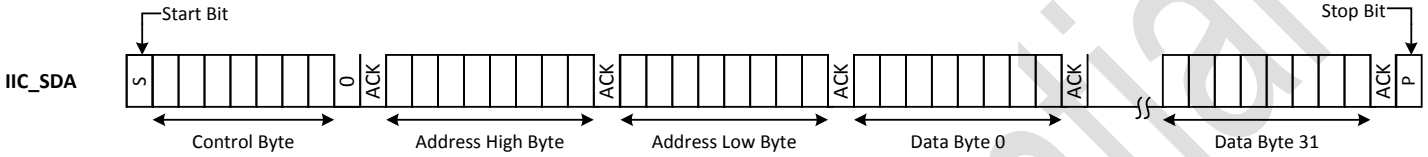


Figure 25. I2C Page Write Format

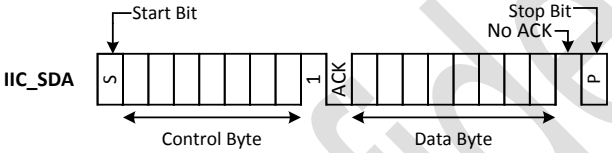


Figure 26. I2C Current Read Format

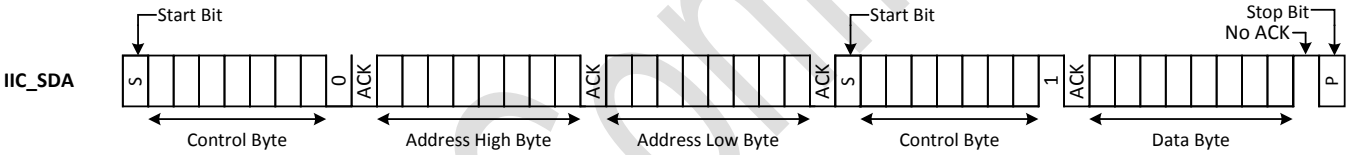


Figure 27. I2C Random Read Format

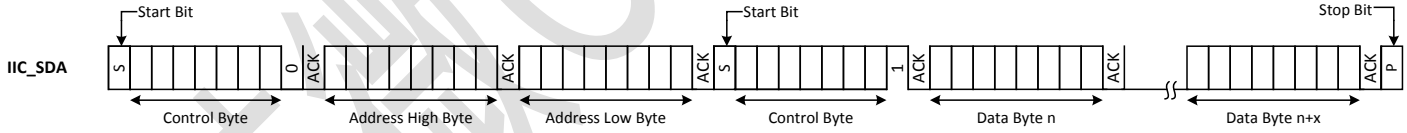


Figure 28. I2C Sequential Read Format

9.3 SPI

The SYD8821 provides two configurations of SPI interfaces. One is four wire SPI, as CSN (chip select), SCLK (clock), SDI (MOSI data) and SDO (MISO data)and the other is two or three wire SPI interface as CSN (chip select) – optional, SCLK (clock), SDIO (bi-directional Data). These two configurations are for master operation only, slave mode is not supported.

9.3.1 Packet Formats

The transmission protocol consists of the two operation modes:

- Write Operation.
- Read Operation.

Both of the two operation modes consist of two bytes. The first byte contains the address (seven bits) and has bit-7 as its MSB to indicate data direction. The second byte contains the data.

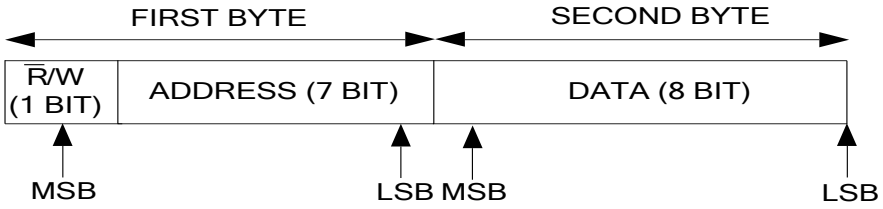


Figure 29. Four-wire or Three/Two-wire SPI Transmission Protocol

9.3.2 Write Operation

A write operation is always initiated by theSYD8821 and consists of two bytes, which the data is going from the host controller to the device. The first byte contains the 7 bits address and has a “1” as its MSB to indicate data direction. The second byte contains the full 8 bits data. The communication is synchronized by SCLK. TheSYD8821 changes SDIO or SDI on the falling edges of SCLK and the device reads SDIO or SDI on the rising edges of SCLK.

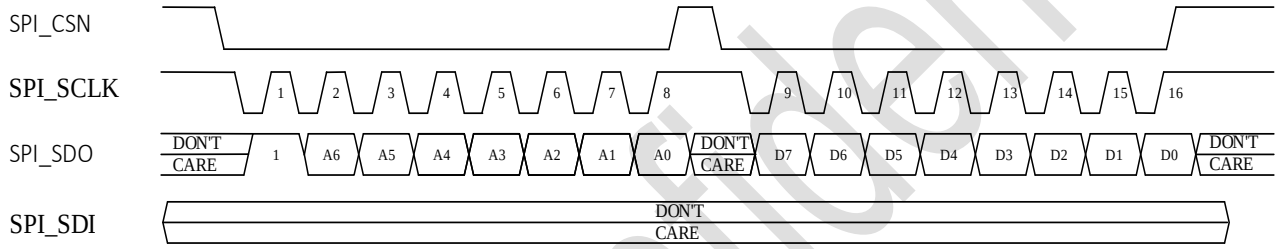


Figure 30. Four-wire SPI Write Operation

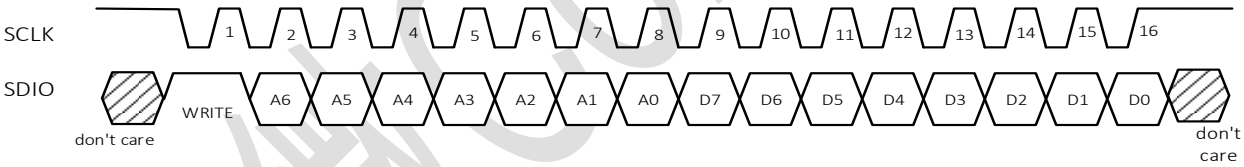


Figure 31. Three/Two-wire SPI Write Operation

9.3.3 Read Operation

A read operation is initiated by the host controller and consists of two bytes. The first byte contains 7-bit address specified by SYD8821 and has a “0” as its MSB to indicate data direction. The second byte contains the full 8 bits data and is driven by the slave device. This communication is synchronized by SPI_SCLK. For three/two-wire SPI, SDIO is changed on the falling edges of SCLK and is read on every rising edge of SCLK. SYD8821 release SDIO bus and handover the control of SDIO bus to the device on the falling edge of last address bit.

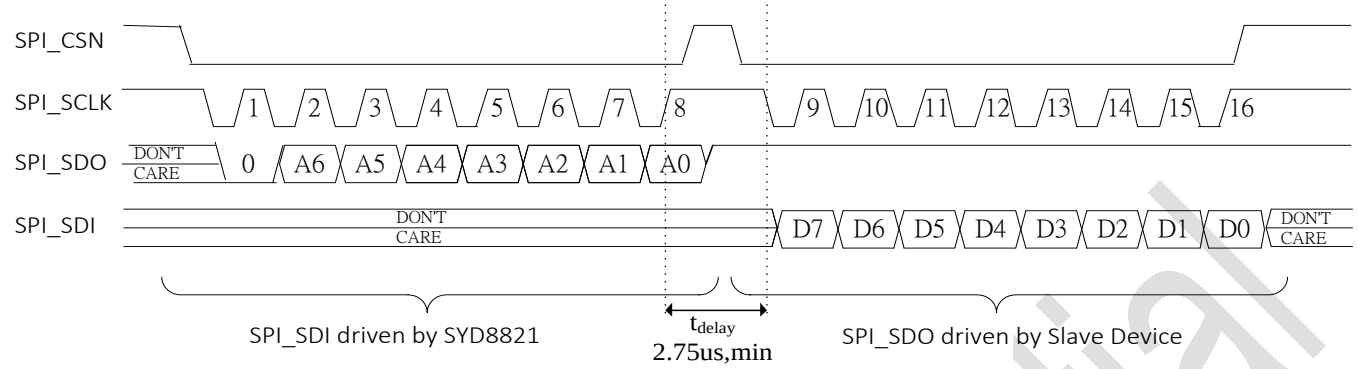


Figure 32. Four-wire SPI Read Operation

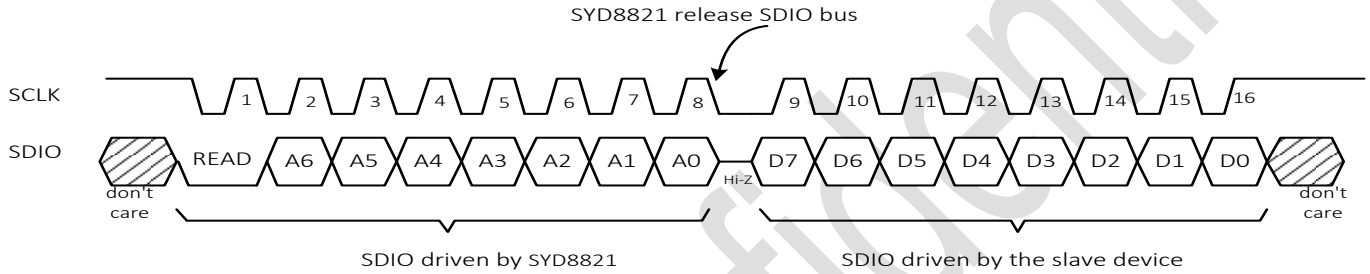


Figure 33. Three/Two-wire SPI Read Operation

9.4 ISO-7816-3

SYD8821 integrate one Smart Card Controller supports asynchronous 3V smartcards. The device is controlled by an ISO 7816-3 interface and is capable of card activation, deactivation, cold/warm reset, ATR parsing and data exchange.

- Compliant to ISO/IEC 7816-3: 1997
- Supports FIFO 8 bytes
- Interrupt report
- Flexible clock frequency and baud rate
- Parity/error check and resend
- T=0 protocol
- Wait time configuration
  - ATR wait time
  - Reset time
  - Guard time

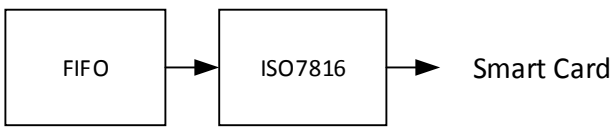


Figure 34. Function block of ISO7816

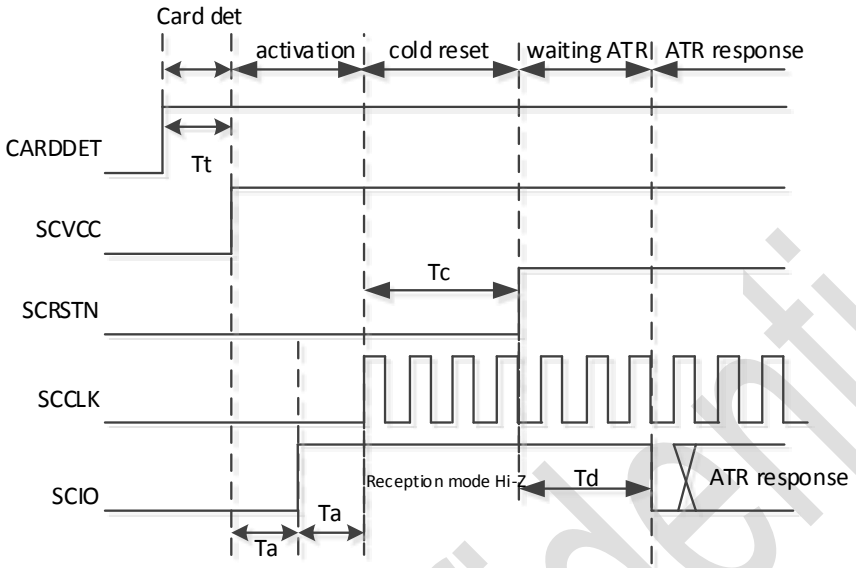


Figure 35. Activation, Cold Reset and ATR

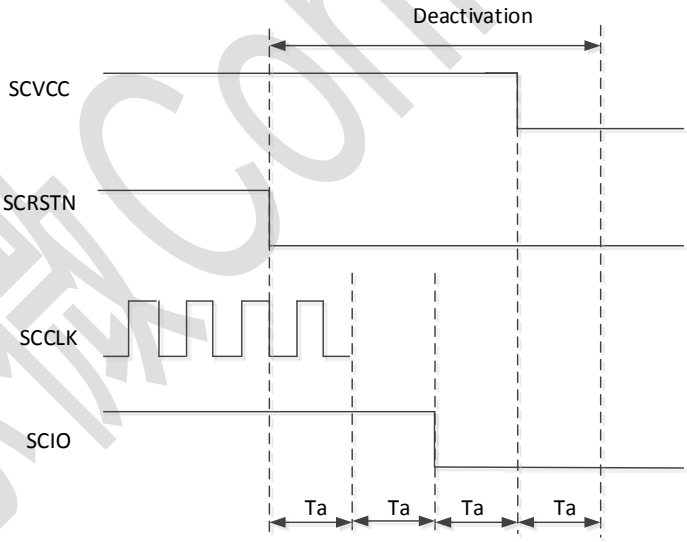


Figure 36. Deactivation Sequence

9.5 IR Transmitter

The Infrared generator provides a flexible way of transmitting any IR code used in remote controls. It has an efficient message queue where users can describe the waveform of a specific IR command in just a few bytes independently from the protocol.

- Flexible carrier frequency and duty cycle.

- Flexible MARK and SPACE.
- Any IR remote control protocol.
- Supported 8 commands message queue in the FIFO.
- Interrupt report

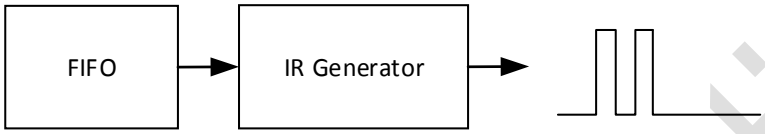


Figure 37. Function block of IR Generator

NEC code:

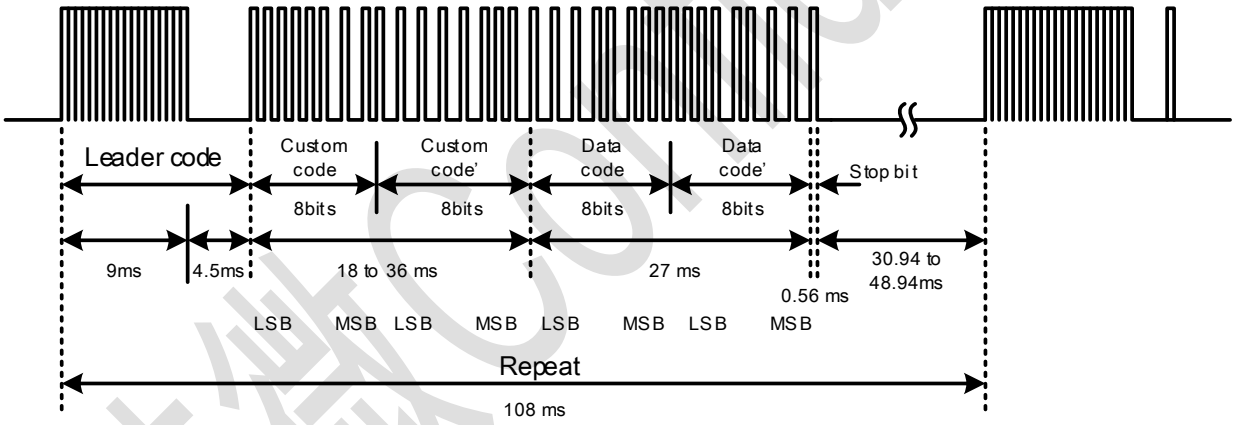


Figure 38. Waveform format of NEC code

RC5 code:

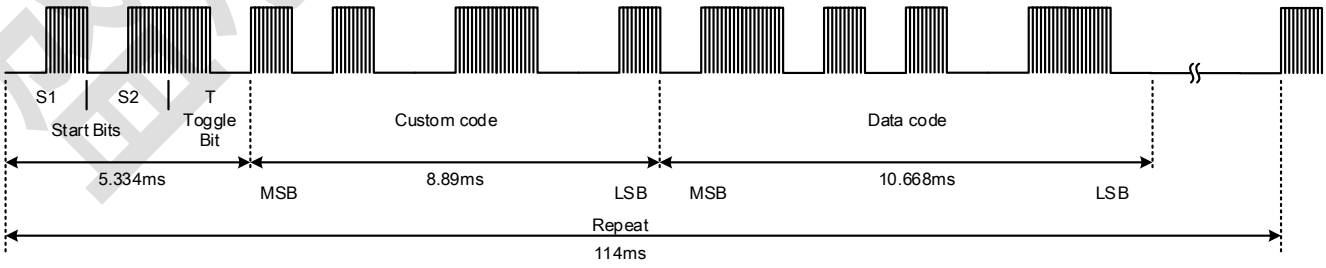


Figure 39. Waveform format of RC5 code

9.6 Audio

SYD8821 supports both AMIC and DMIC(I2S, PDM) audio interfaces.

9.6.1 AMIC Interface

SYD8821 integrate a microphone interface for application of voice recorded. For voice recorded functionality. The SYD8821 includes a 12bits SAR ADC with 75dB SNR performance and with a programmable Gain amplifier capable of a maximum gain of 50dB. SYD8821 also provides MIC bias source with 4 steps (2.94V/2.5V/1.4V/1.25V).Illustrated the block diagram as below.

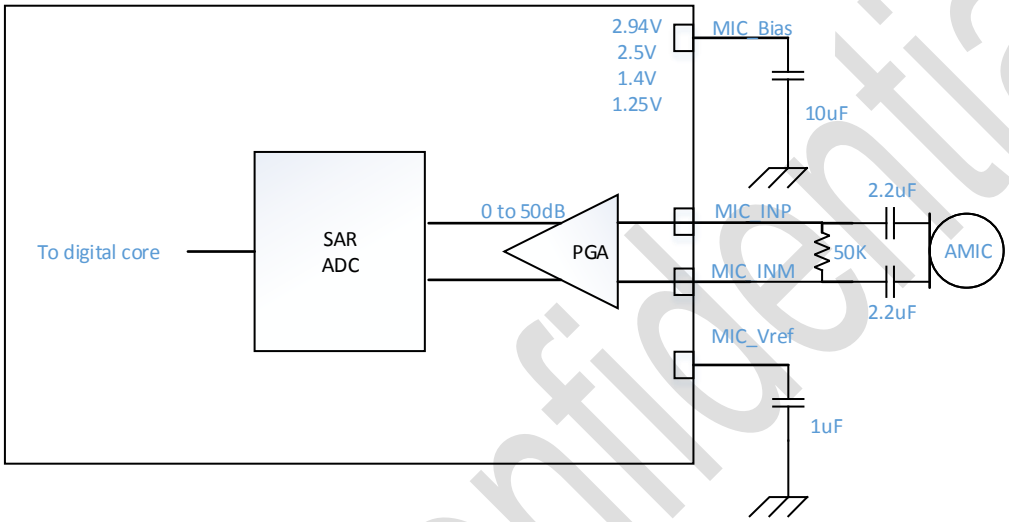


Figure 40. AMIC Reference Circuit

Table 20. AMIC Interface Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Microphone Input						
Signal to Noise Ratio	SNR		75		dB	PGAgain=24dB, 22Hz to 7.5KHz
Total Harmonic & Noise	THD+N		64		dB	PGAgain=24dB, 22Hz to 7.5KHz
Frequency response	FR	-1.5		1.5	dB	PGAgain=24dB, 22Hz to 4.0KHz
Programmable input PGA gain	$V_{RIPPLE,Buck}$	0		50	dB	
Input resistance	Rin		23.74		kΩ	PGA = 24 dB
			80.3		kΩ	PGA = 12 dB
			200		kΩ	PGA = 0 dB
Microphone Bias	Vbias		2.94		V	150Ω output series resistance
			2.5		V	150Ω output series resistance
			1.4		V	150Ω output series resistance
			1.25		V	150Ω output series resistance

9.6.2 DMIC Interface

SYD8821 supports both PDM and I2S audio interface.

The SYD8821 has PDM module for application of digital microphone with PDM output.

SYD8821 PDM module supports 16kHz output sample rate and 16bit format. It also implements DMA for sample buffering and HW decimation filters.

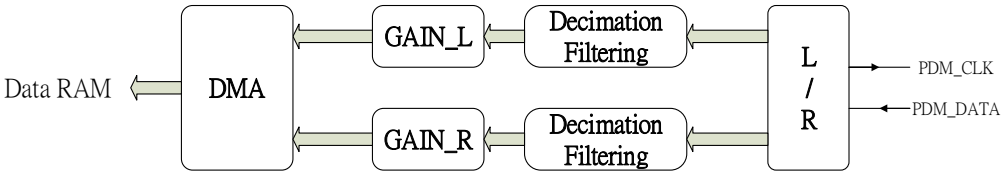


Figure 41. PDM Function Diagram

10.0 Ordering information

Part number	Package	Packing	Minimum Order Quantity
SYD8821QN48	QFN 6mmx6mm 48-Pin	Tape Reel	3K
SYD8821QN32	QFN 5mmx5mm 32-Pin	Tape Reel	3K

Document Revision History

Revision Number	Date	Description
0.1	26 Dec 2017	Preliminary version
1.0	10 Mar 2018	Add pin assignment and signal description
1.1	12 Mar 2018	Add QFN32 information
2.0	25 Apr 2018	Update the pin assignment in Figure2
2.1	08 May 2018	Update the current consumption information
3.0	08 Oct 2018	Update UART, ISO7816, IR transmitter, PDM/AMIC information

SYDTEK 盛芯微官方网站： http://www.sydtek.com