Sri Venkateswara College

(University of Delhi)

Basic VLSI Design

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Examination roll number: 23079558022

Course: B.Sc. (Hons.) Electronics

Semester: V

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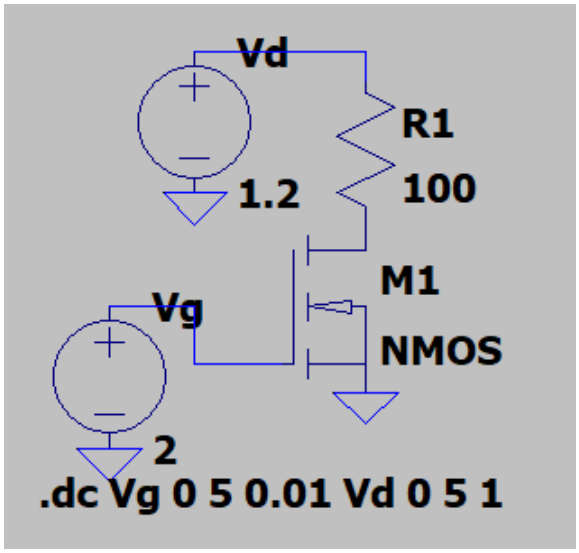
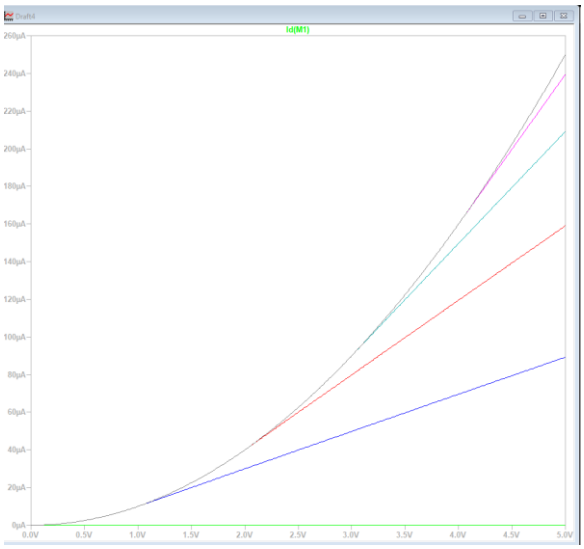
S. No.	Name of the Experiment
1.	To plot the (i) output characteristics Ids-Vds & (ii) transfer characteristics Ids-Vgs of an n-channel and p-channel MOSFET.
2.	To study the impact of change in physical/device parameters and scaling on the I-V characteristics of n-MOSFET. (using Level 1 MOS and BSIM models)
3.	To design and plot the static and dynamic characteristics of a digital CMOS inverter (VTC and transient) (i) Plot the butterfly diagram of the CMOS inverter (ii) Analyse the impact of load capacitance value on the propagation delay
4.	To design and plot the output characteristics of a 3-stage inverter ring oscillator.
5.	To design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS technology.
6.	To design half adder using CMOS technology.
7.	To design 2x1 digital MUX using transmission gate logic.
8.	To design and plot the characteristics of a 4x1 digital multiplexer using pass-transistor logic.
9.	To design and plot the characteristics of a positive and negative latch/master-slave edge triggered registers based on multiplexers.

Experiment 1

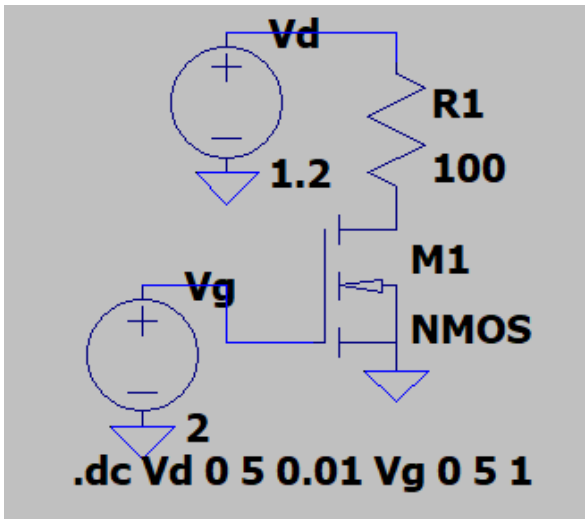
Aim: To plot the (i) output characteristics Ids-Vds & (ii) transfer characteristics Ids-Vgs of an n-channel and p-channel MOSFET.

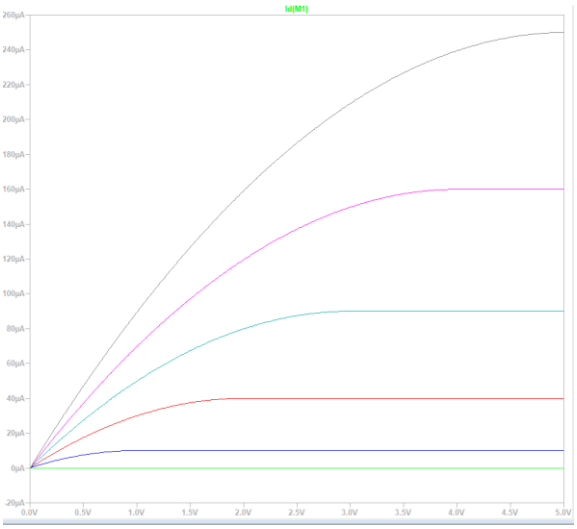
1. Transfer characteristics Ids-Vgs





2. Output characteristics Ids-Vds



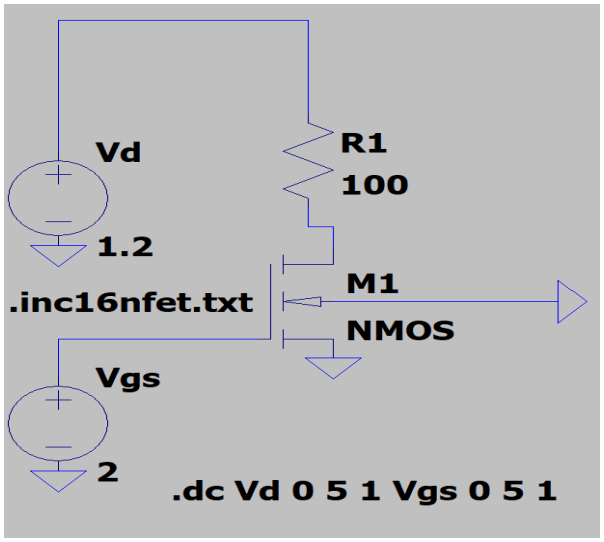


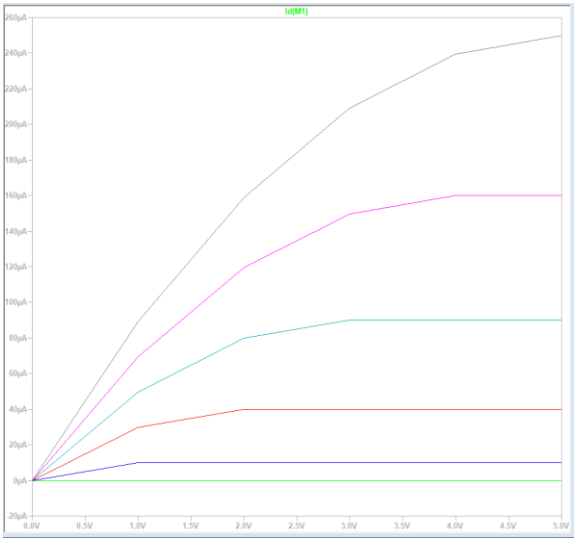
Experiment 2

Aim: To study the impact of change in physical/device parameters and scaling on the I-V characteristics of n-MOSFET. (using Level 1 MOS and BSIM models)

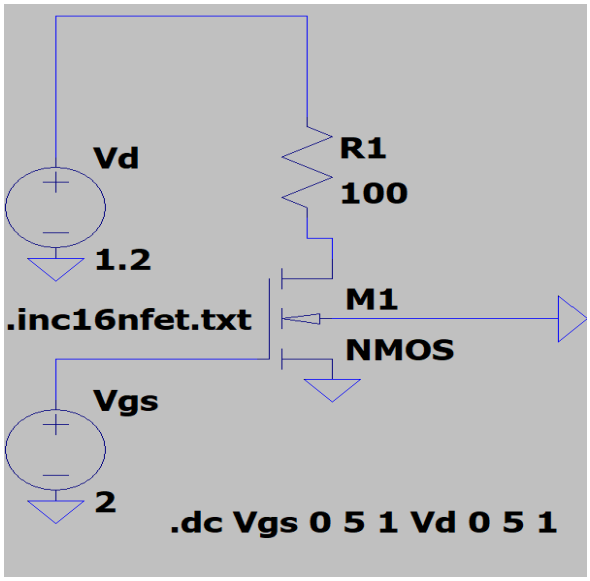
A) MOSFET imported from other website

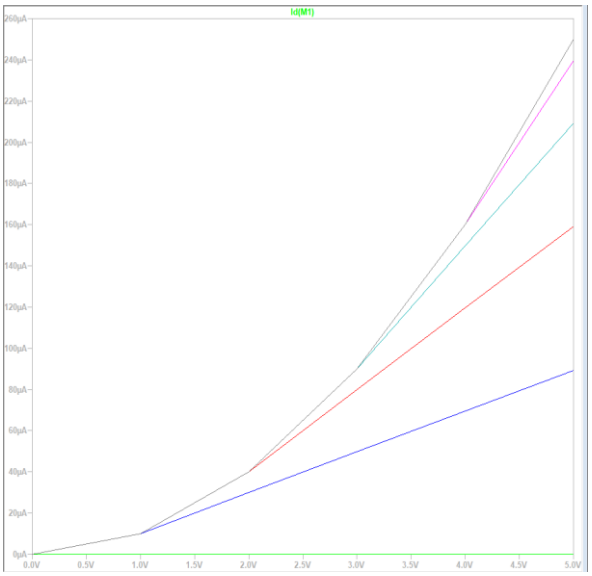
1. Output characteristics Ids-Vds





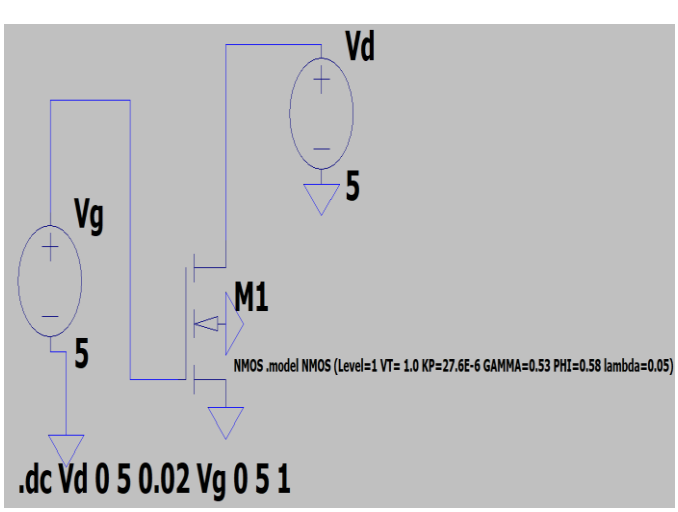
2. Transfer characteristics Ids-Vgs

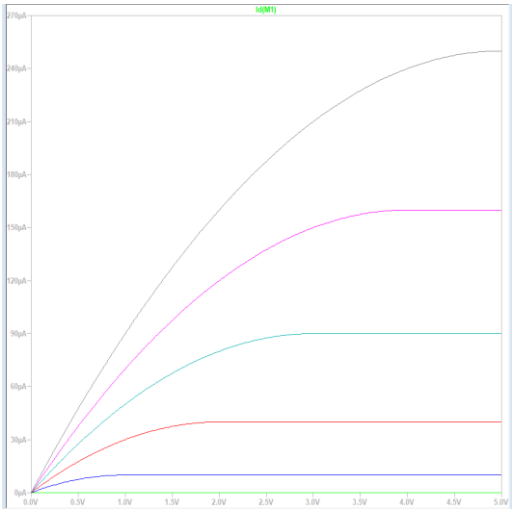




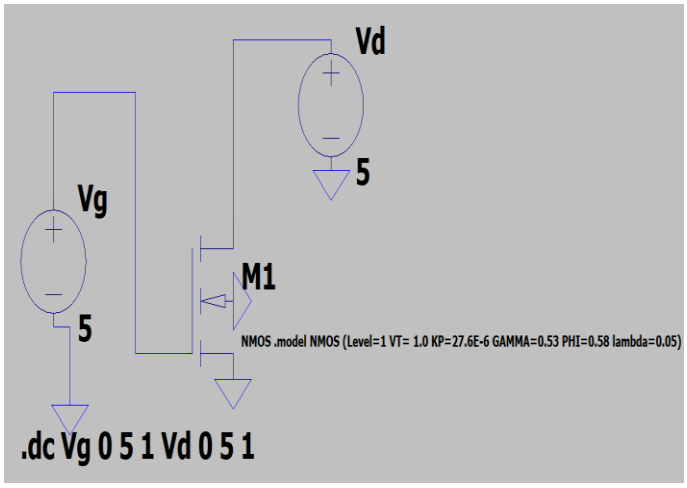
B) Defining device parameters

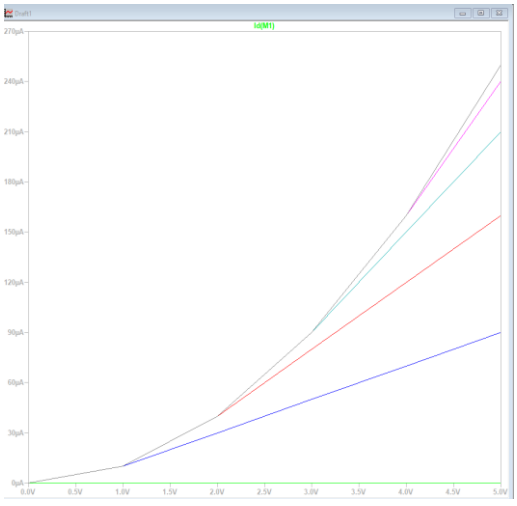
1. Output characteristics Ids-Vds





2. Transfer characteristics Ids-Vgs





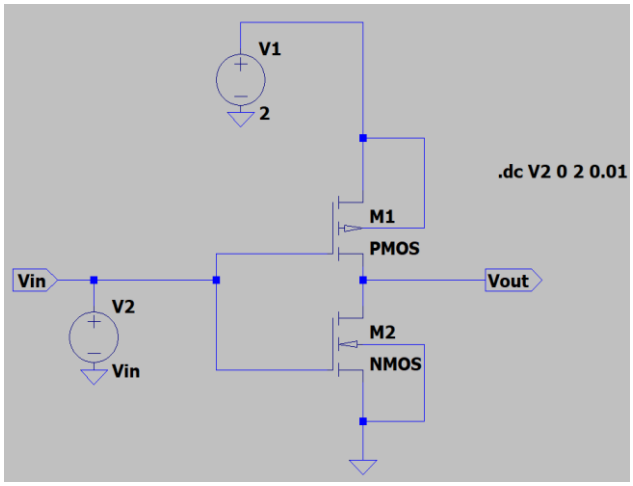
Experiment 3

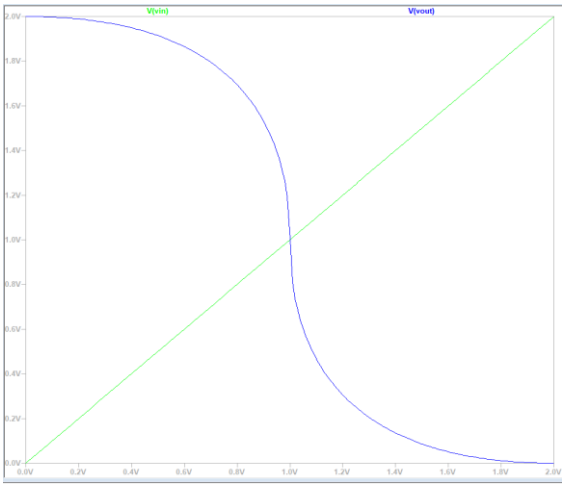
Aim: To design and plot the static and dynamic characteristics of a digital CMOS inverter (VTC and transient)

(i) Plot the butterfly diagram of the CMOS inverter

(ii) Analyse the impact of load capacitance value on the propagation delay

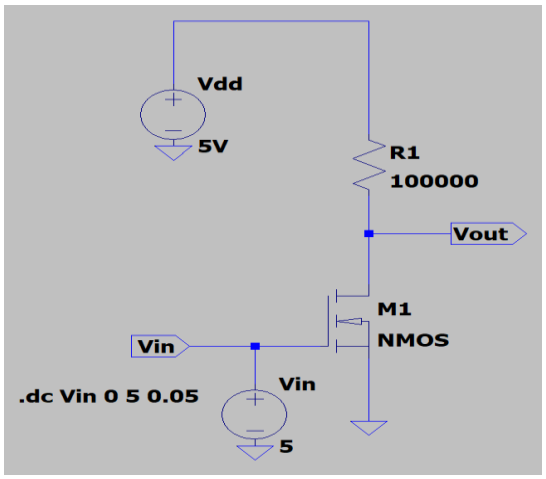
(i) Butterfly diagram of the CMOS inverter

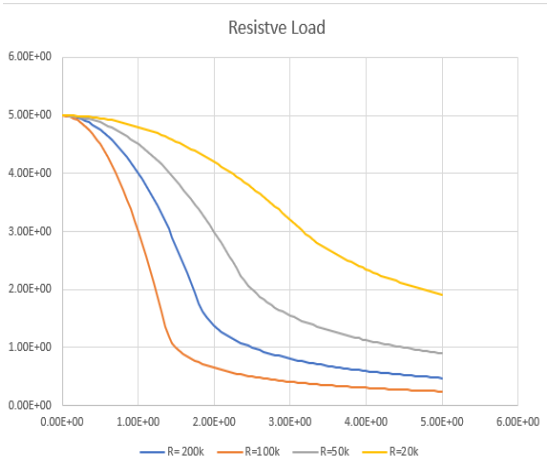




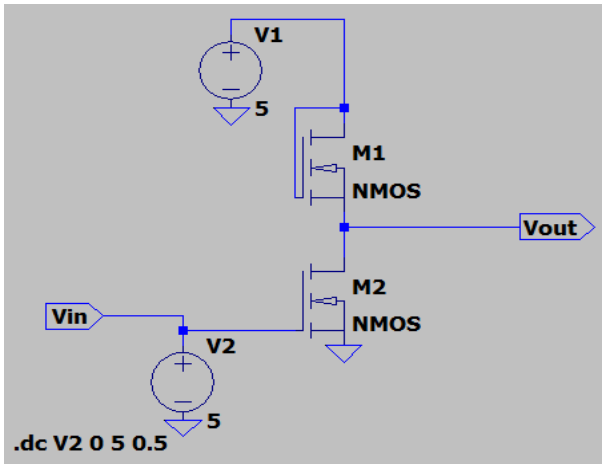
A) Nmos inverter with resistive load

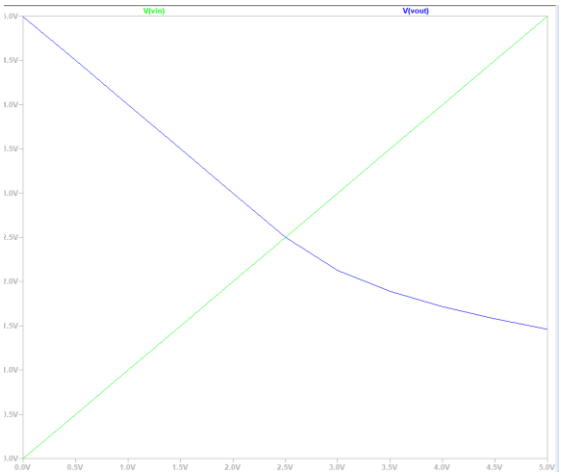
R= 20K ohm, 50k ohm, 100k ohm, 200k ohm





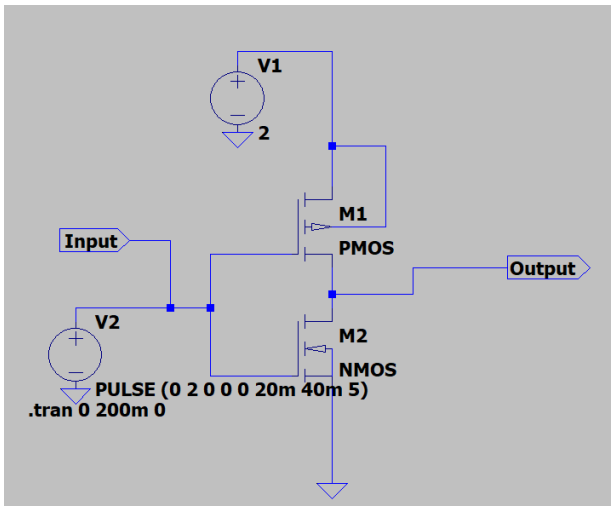
C) Nmos as a load

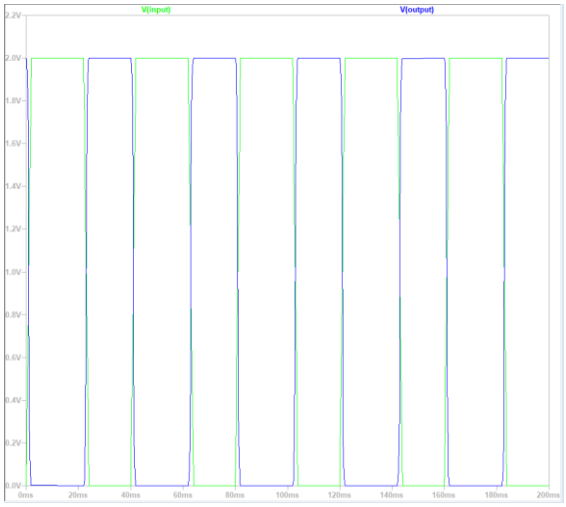




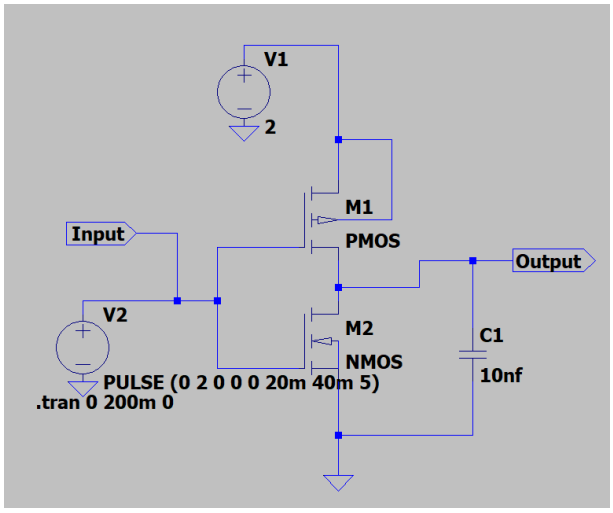
(ii) Analyse the impact of load capacitance value on the propagation delay

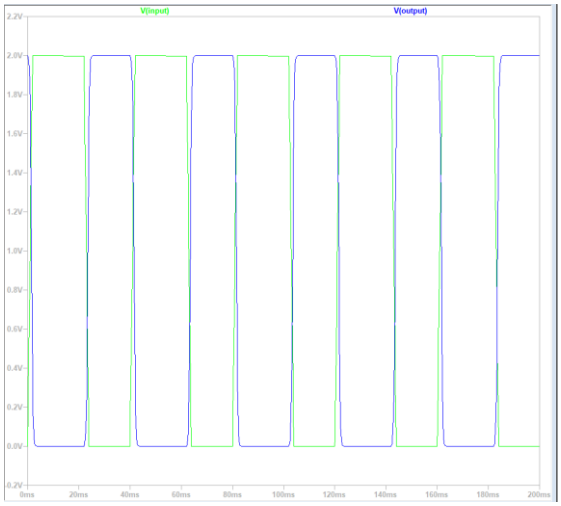
A) Without capacitor:



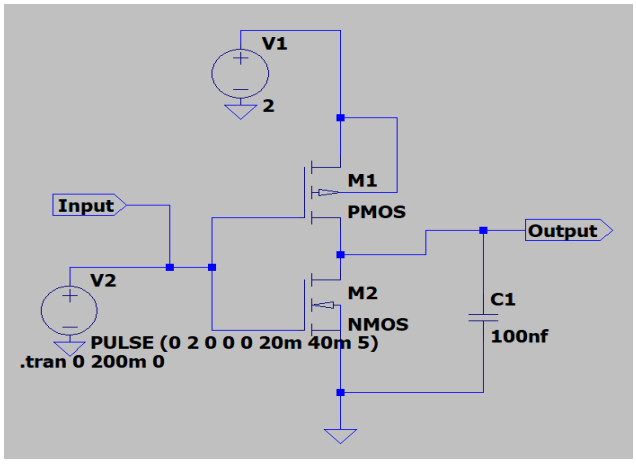


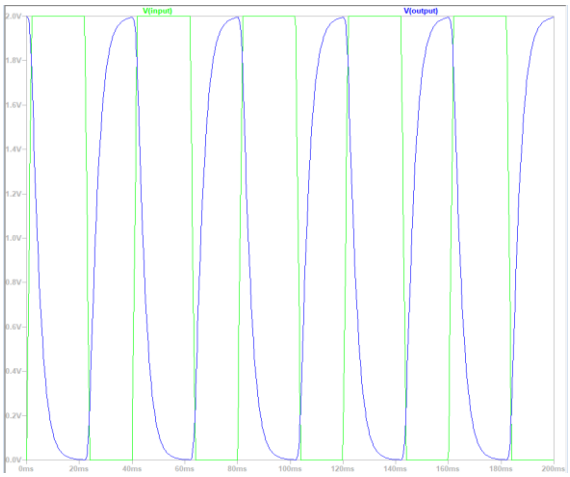
B) With capacitor C1= 10nf:





c) With capacitor C2= 100nf:

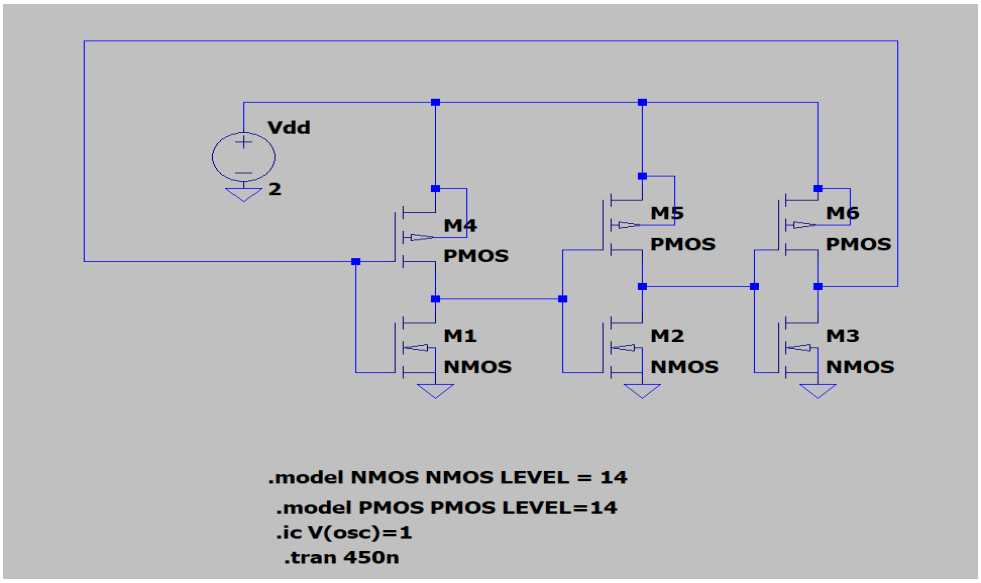




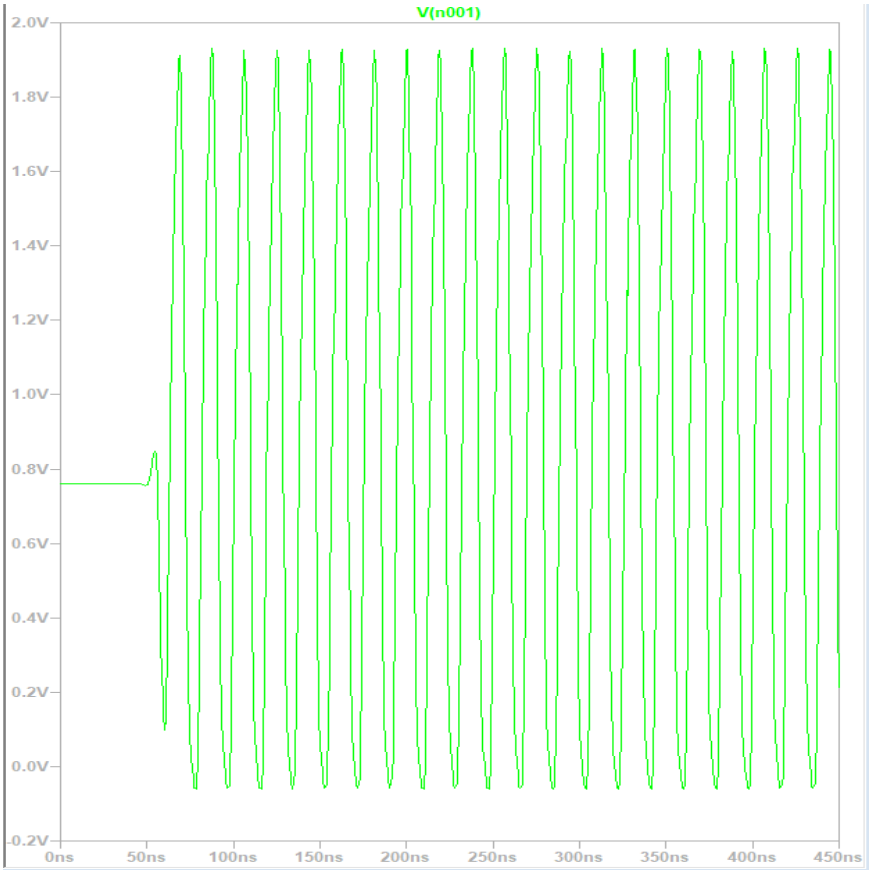
Experiment 4

Aim: To design and plot the output characteristics of a 3-stage inverter ring oscillator.

Circuit Diagram:



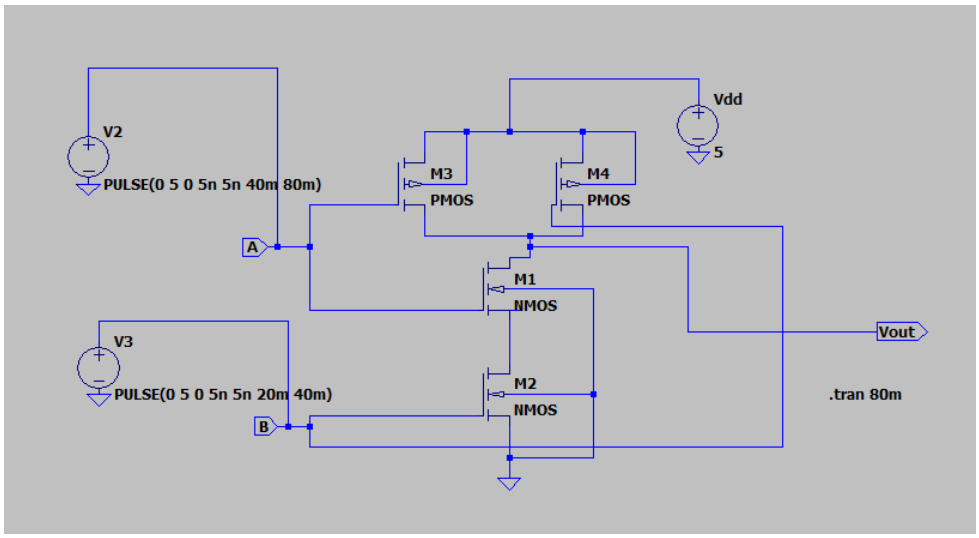
Output:

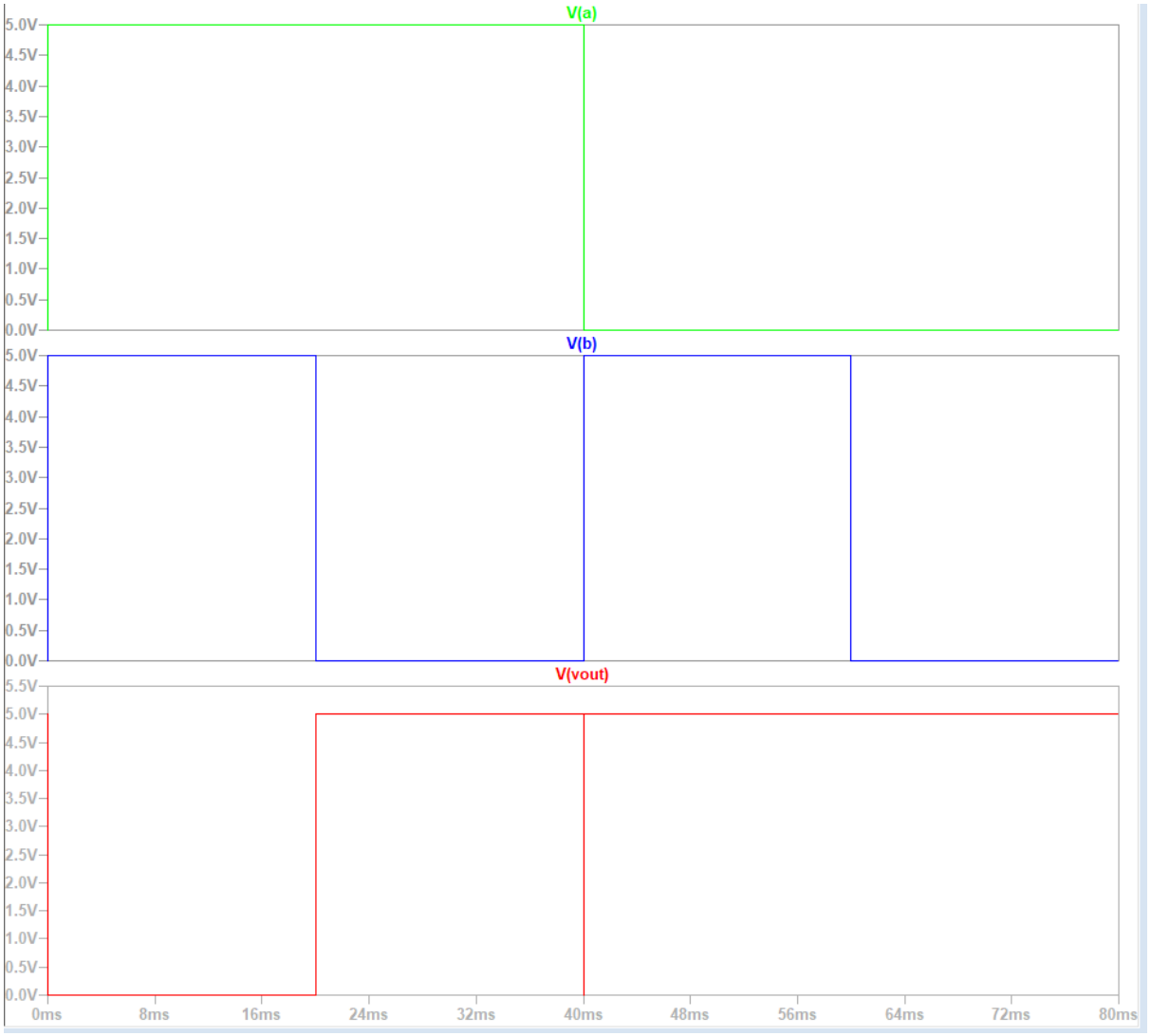


Experiment 5

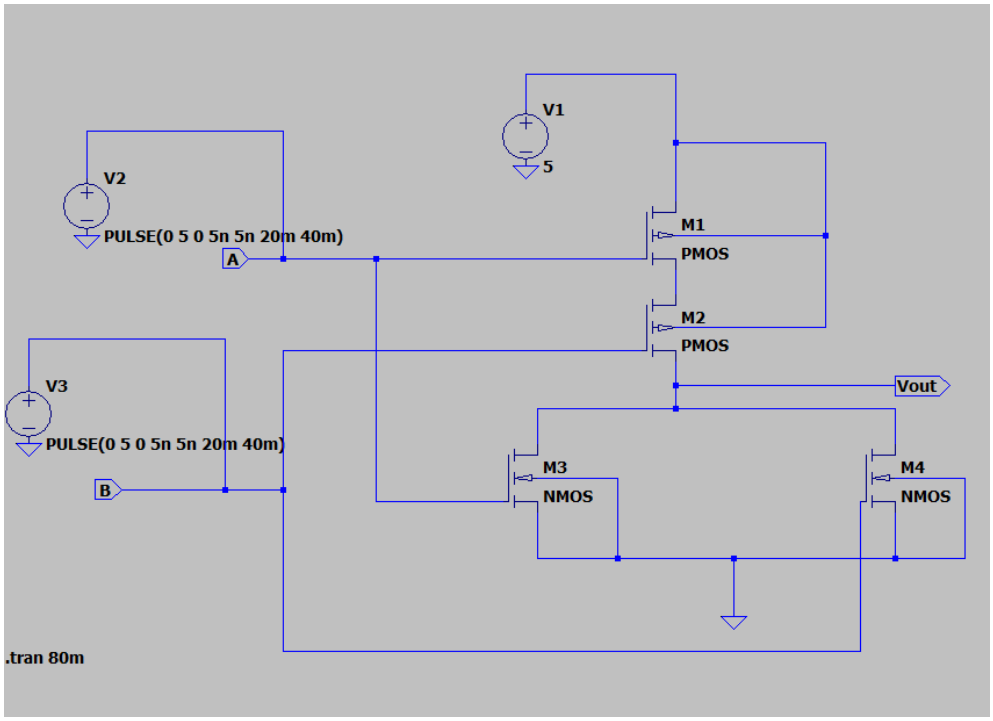
Aim: To design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS technology.

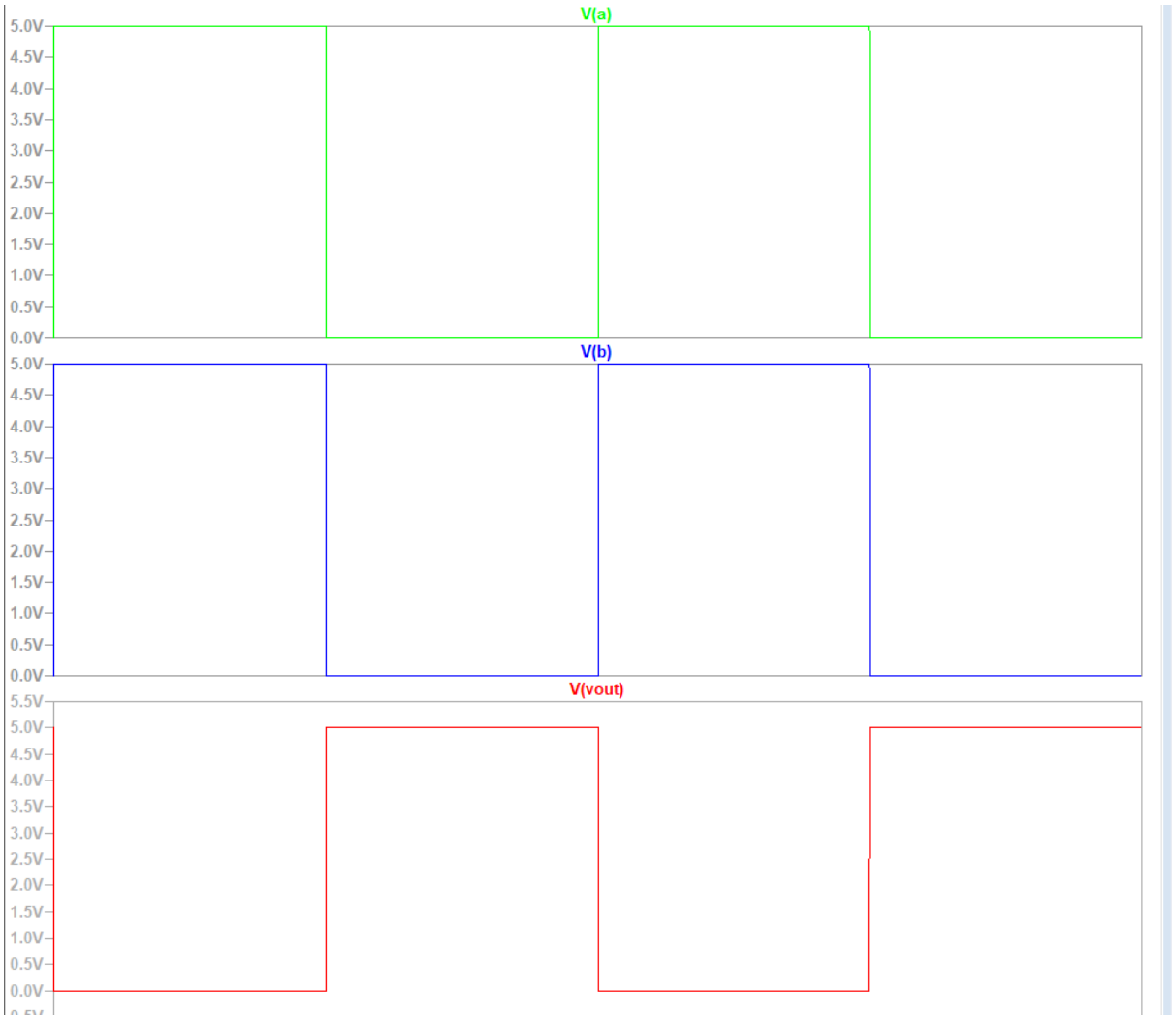
A) NAND gate using CMOS



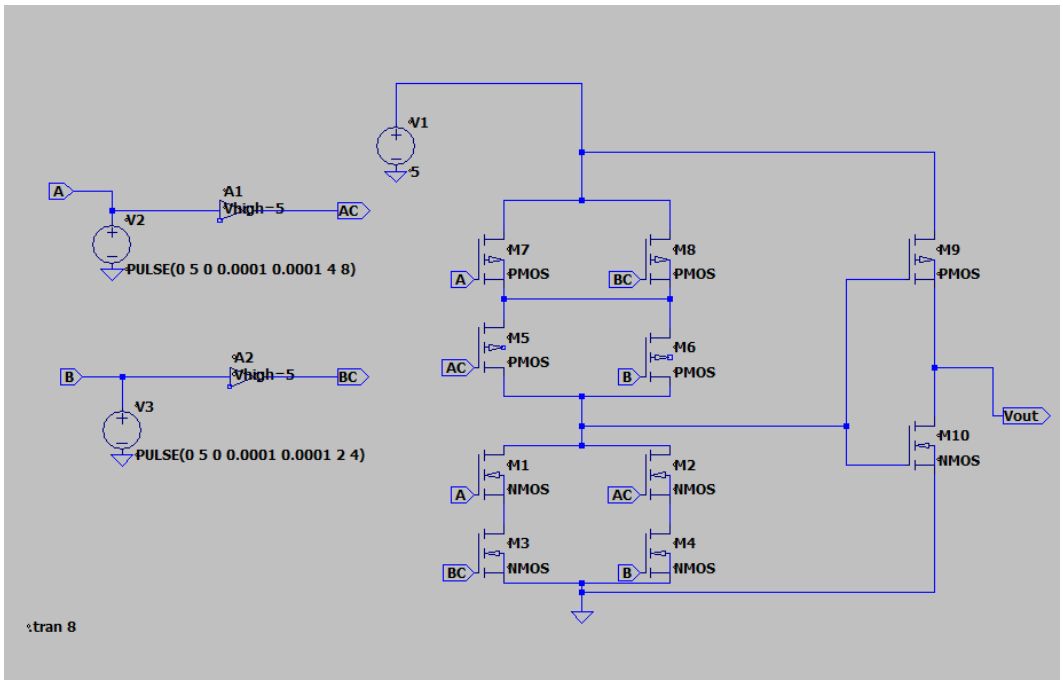


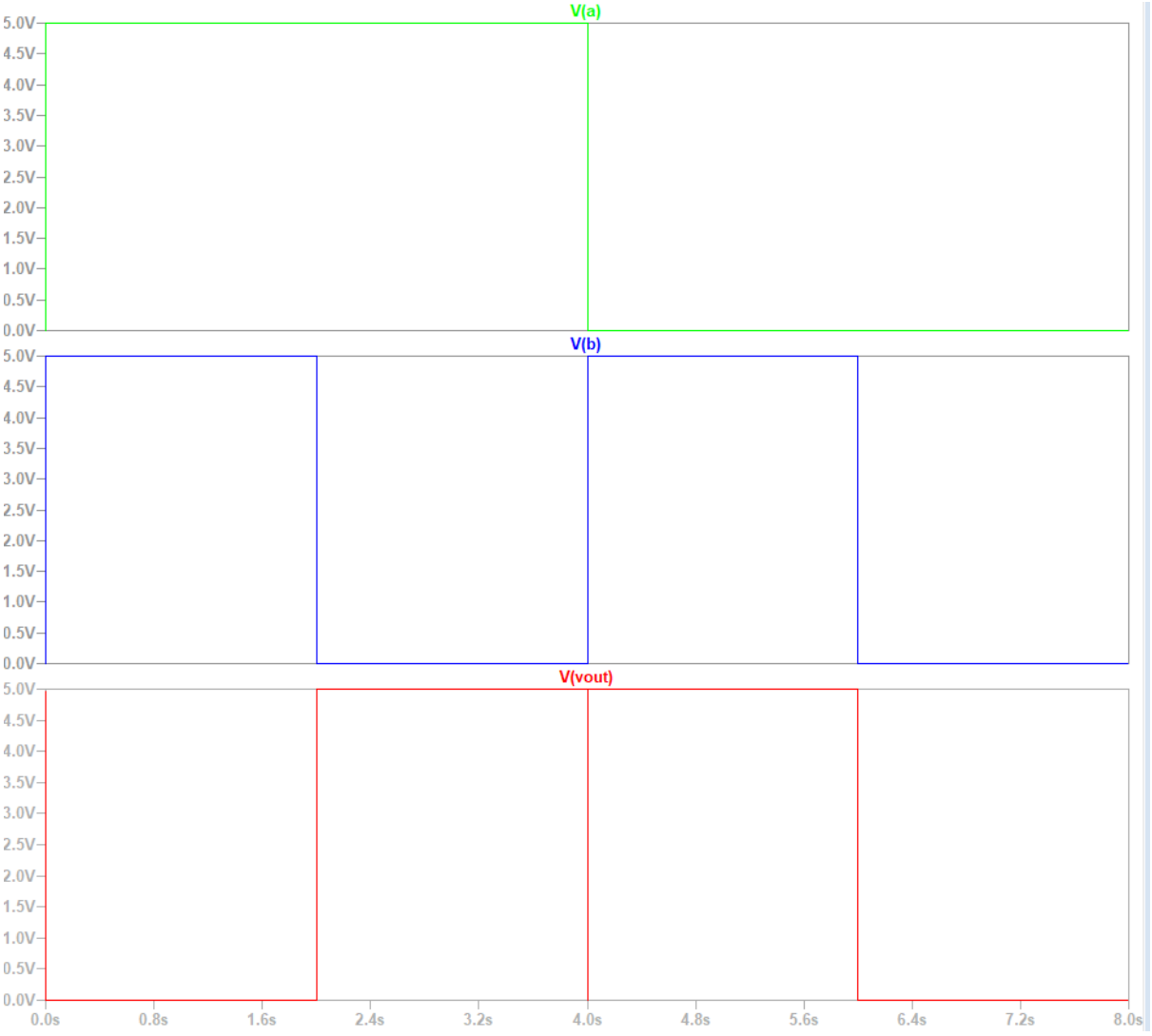
B) NOR Gate using CMOS





C) XOR using CMOS

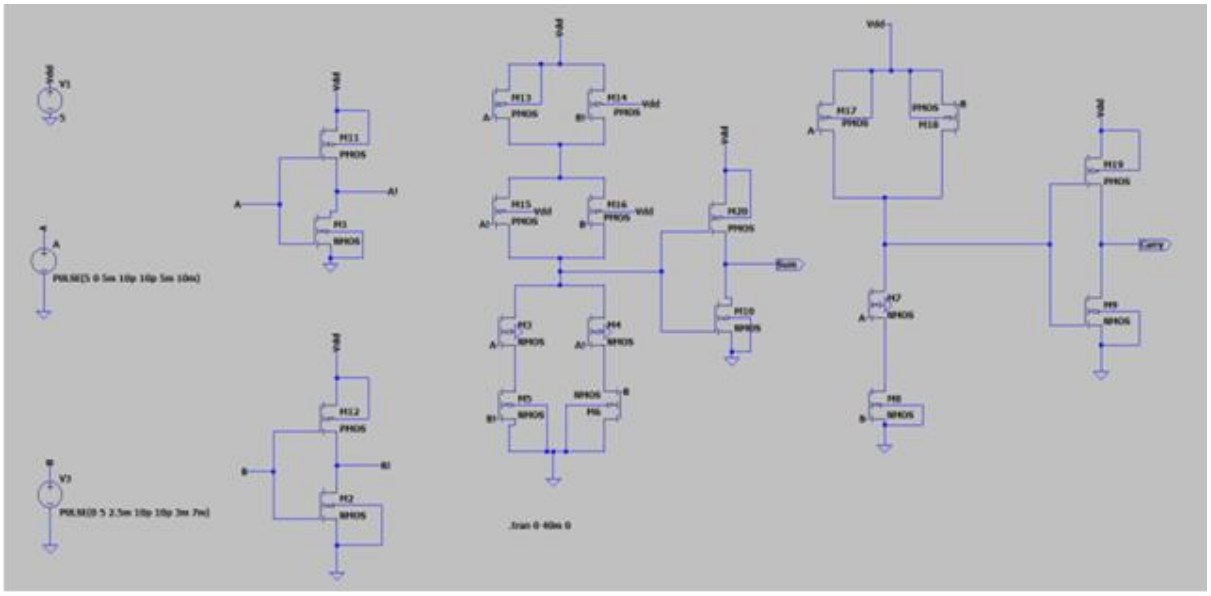




Experiment 6

Aim: To design half adder using CMOS technology.

Circuit Diagram:

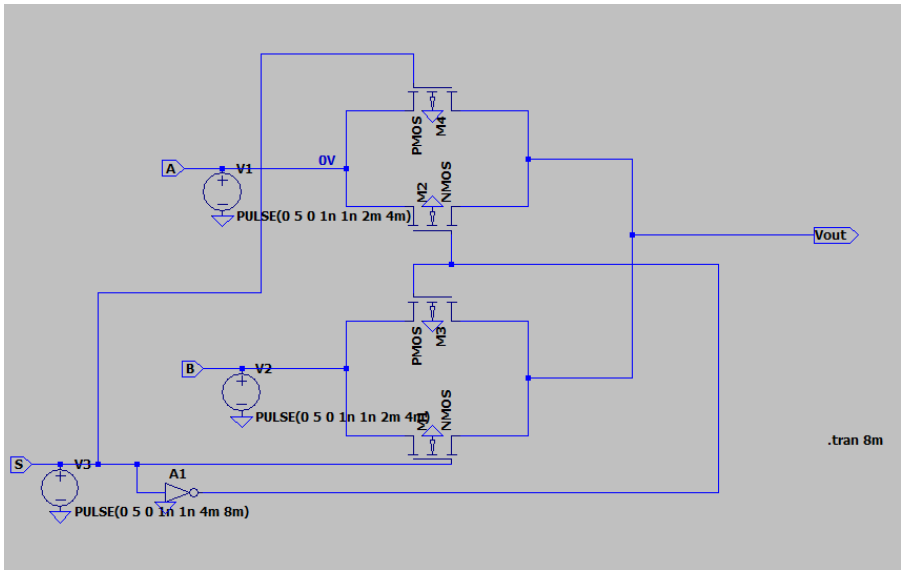


Output:

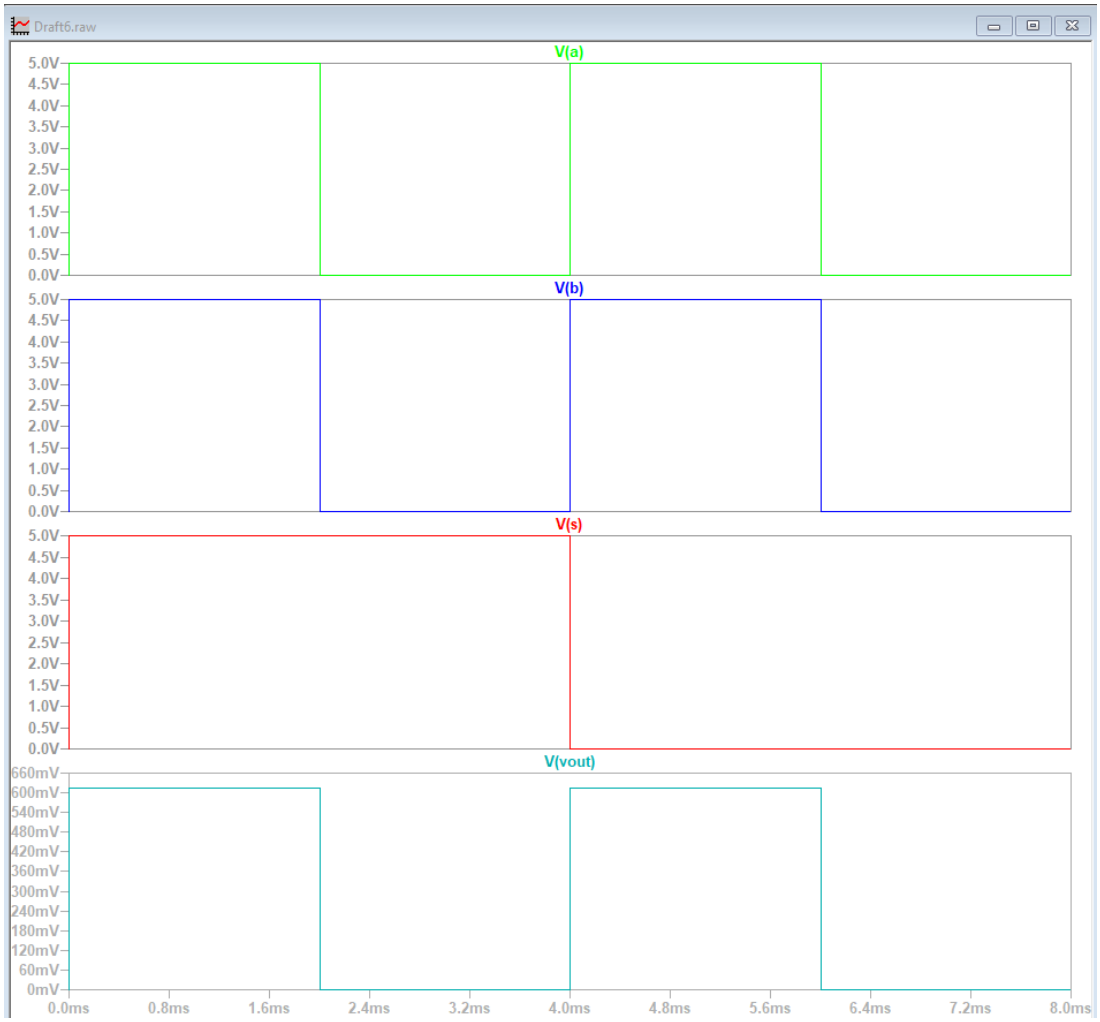
Experiment 7

Aim: To design 2x1 digital MUX using transmission gate logic.

Circuit Diagram:



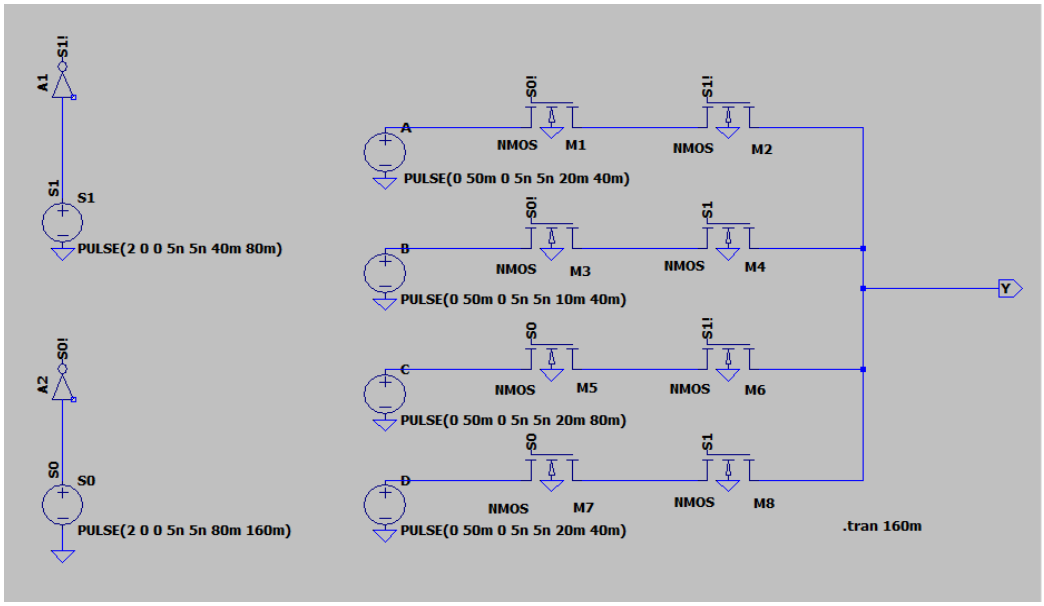
Output:



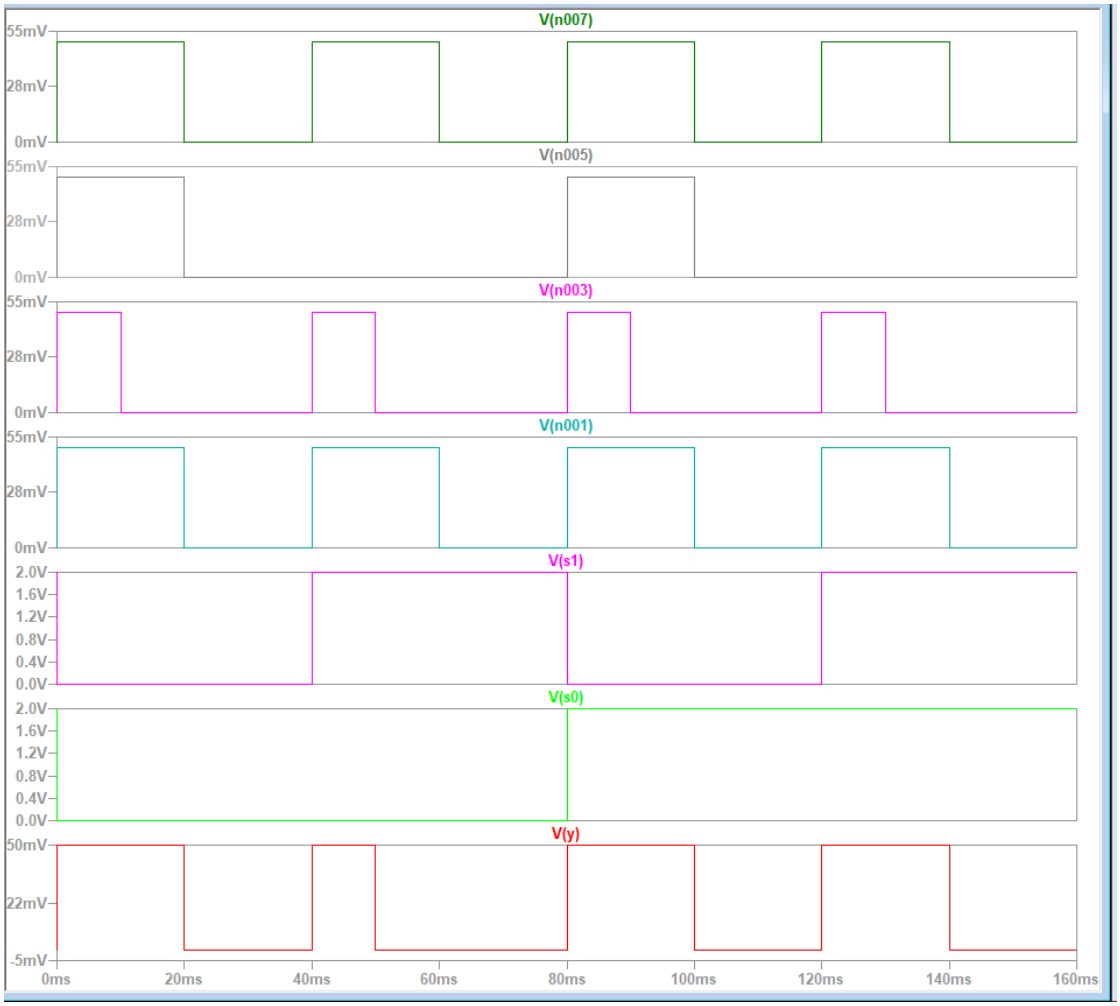
Experiment 8

Aim: To design and plot the characteristics of a 4x1 digital multiplexer using pass-transistor logic.

Circuit diagram:



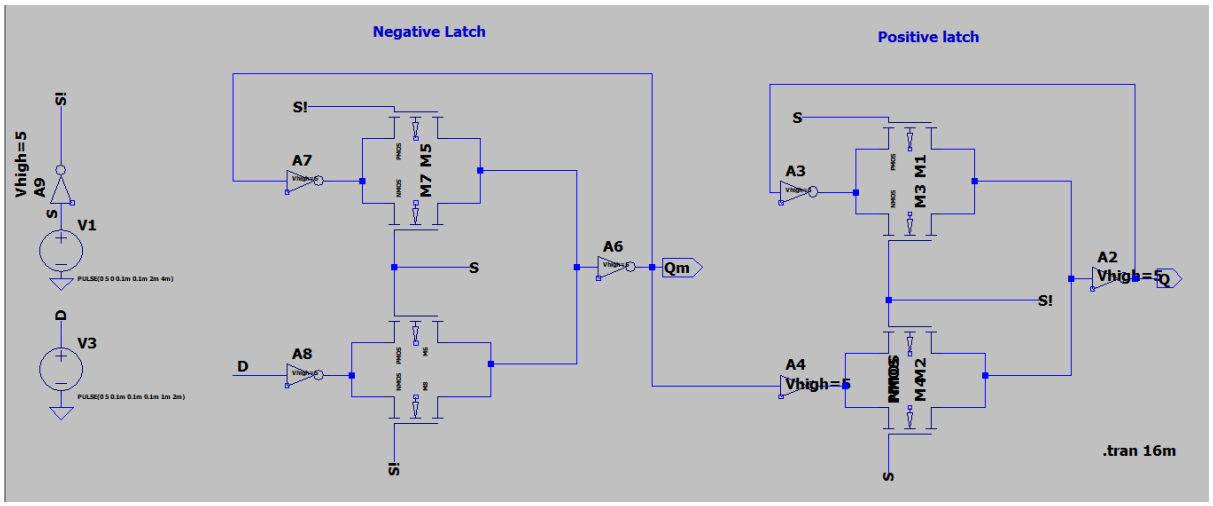
Output:



Experiment 9

Aim: To design and plot the characteristics of a positive and negative latch/master-slave edge triggered registers based on multiplexers.

Circuit Diagram:



Output: