VLSI DESIGN

PRACTICAL FILE

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COURSE: BSC. (H.) ELECTRONICS - III

SEMESTER - V

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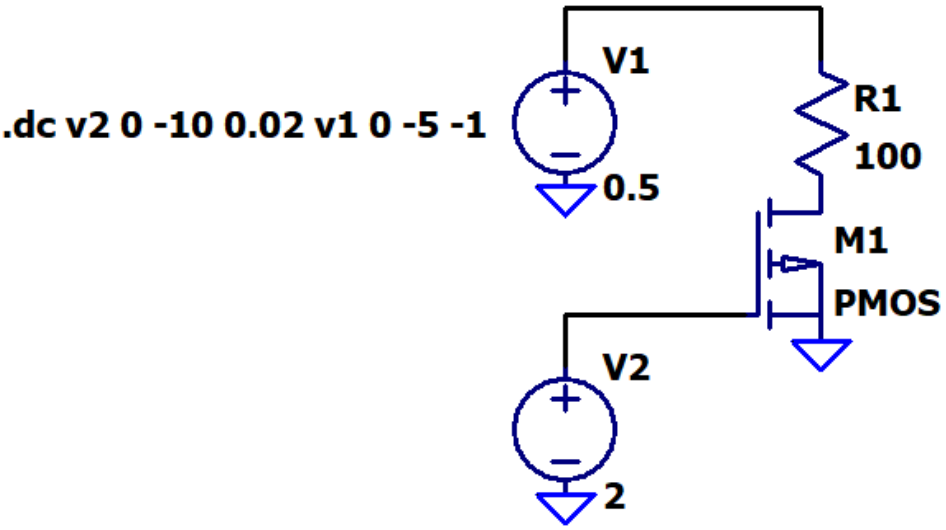
S.no.	Experiment	Signature
1	To plot the (i) output characteristics Ids-Vds & (ii) transfer characteristics Ids-Vgs of an n-channel and p-channel MOSFET.	
2	To design and plot the static and dynamic characteristics of a digital CMOS inverter (VTC and transient) (i) Plot the butterfly diagram of the CMOS inverter (ii) Analyse the impact of load capacitance value on the propagation delay	
3	To design and plot the output characteristics of a 3-stage inverter ring oscillator.	
4	To design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS technology.	
5	To design full adder using CMOS technology.	
6	To design 2x1 digital MUX using transmission gate logic	
7	To design and plot the characteristics of a 4x1 digital multiplexer using pass-transistor logic.	
8	To design and plot the characteristics of a positive and negative latch/master-slave edge triggered registers based on multiplexers.	

EXPERIMENT 1:

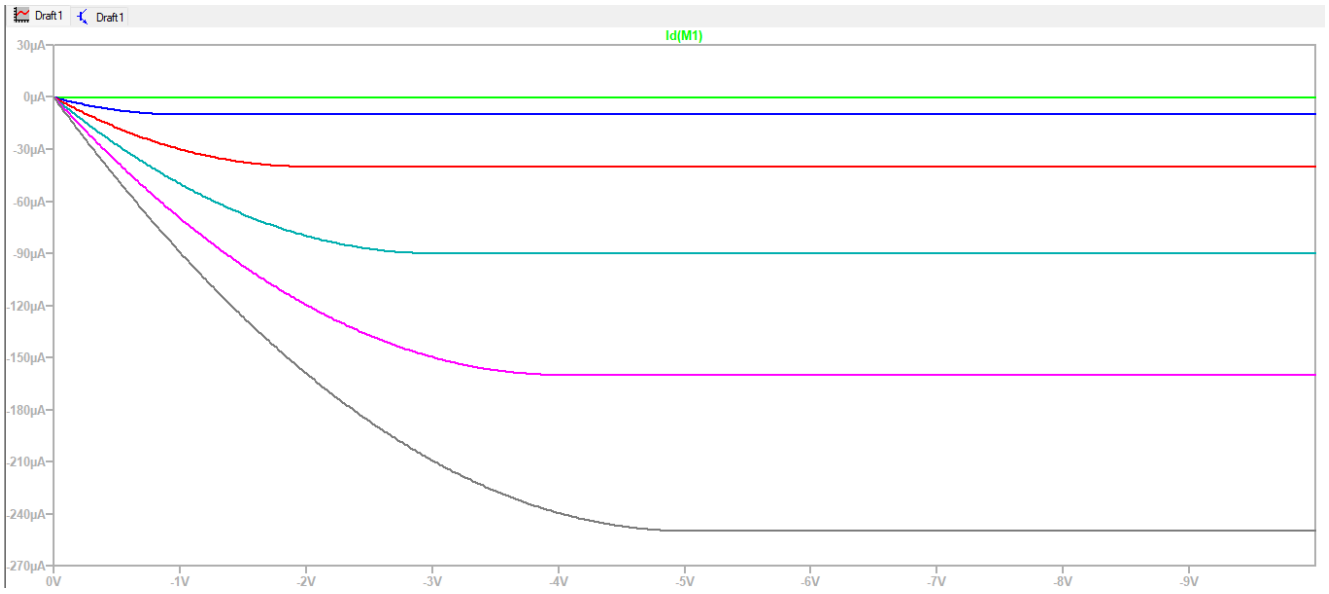
AIM : To plot the (i) output characteristics Ids-Vds & (ii) transfer characteristics Ids-Vgs of an n-channel and p-channel MOSFET.

Transfer and output characteristics of NMOS and PMOS

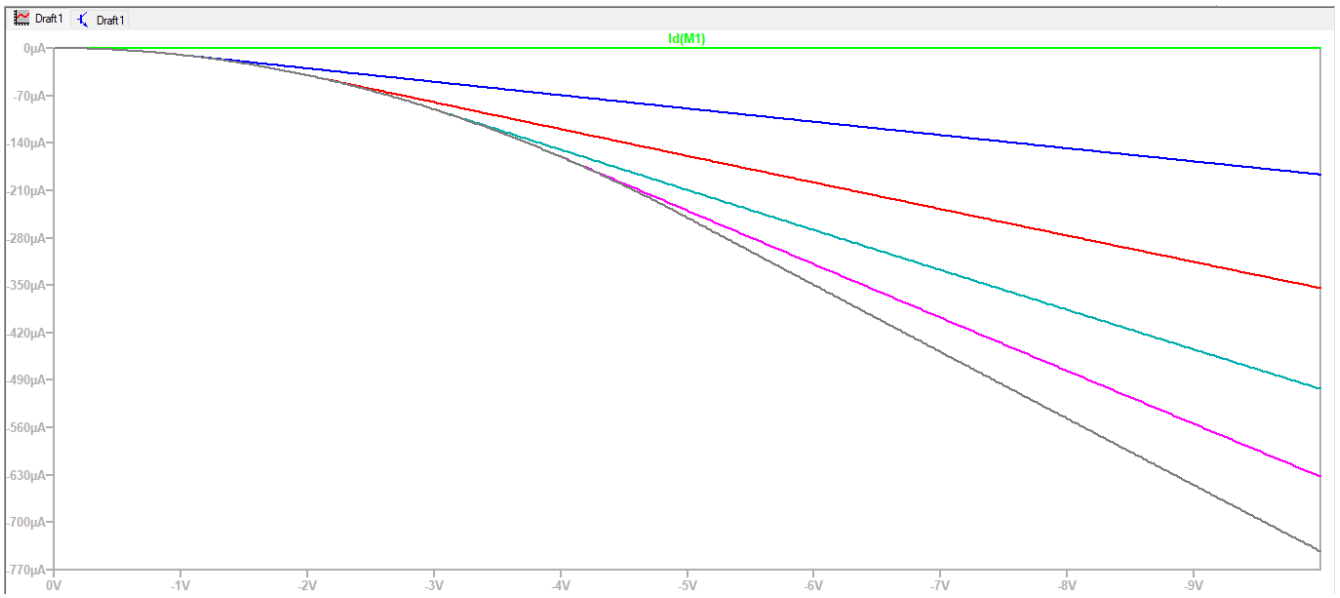
CIRCUIT:



Output Characteristics

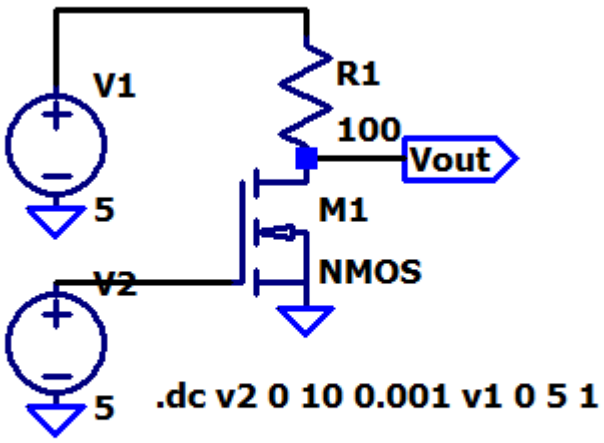


Transfer Characteristics

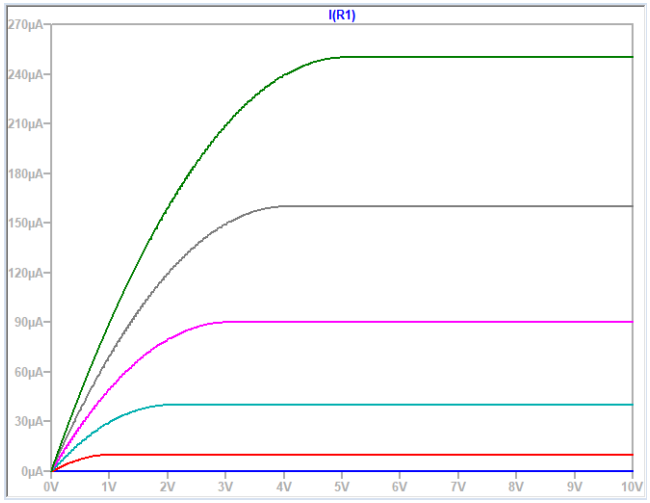


Output and transfer characteristics of NMOS:

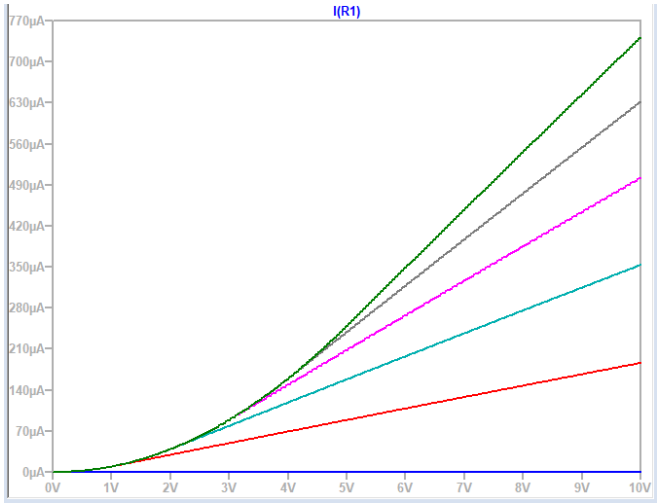
CIRCUIT:



Output:



Transfer:



EXPERIMENT 2:

DC and Transient analysis of CMOS inverter

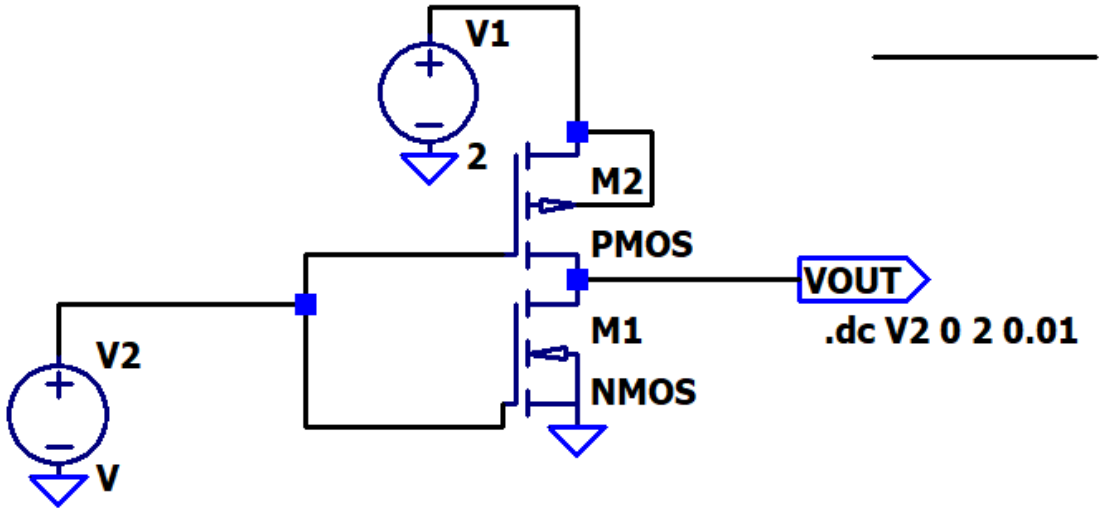
AIM: To design and plot the static and dynamic characteristics of a digital CMOS inverter (VTC and transient)

(i) Plot the butterfly diagram of the CMOS inverter

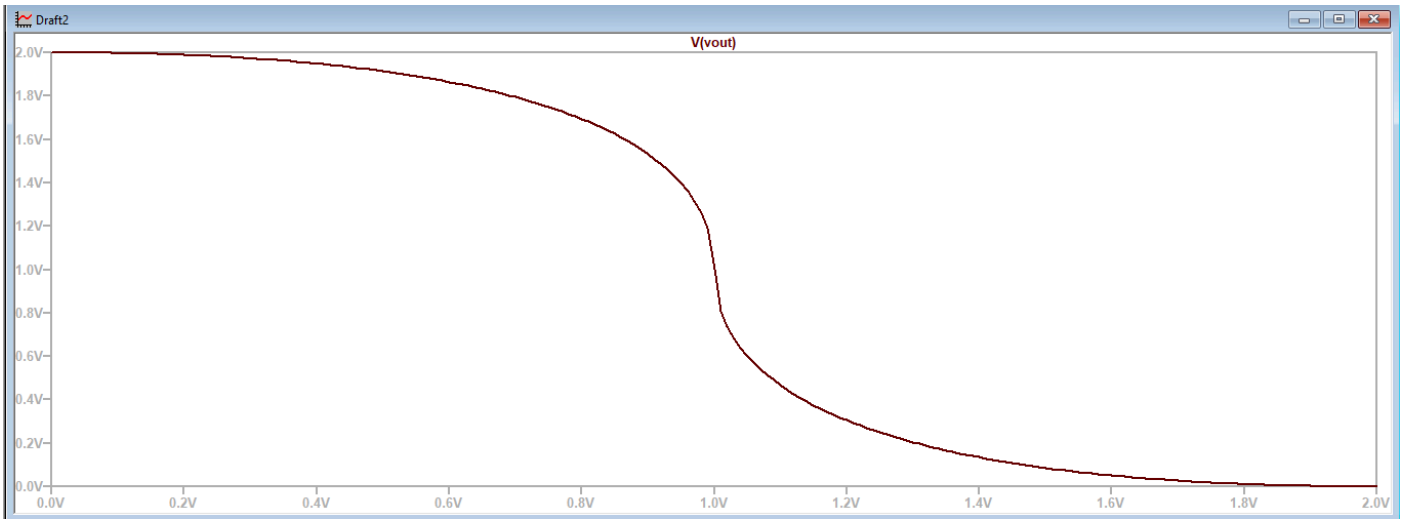
(ii) Analyse the impact of load capacitance value on the propagation delay

CIRCUIT:

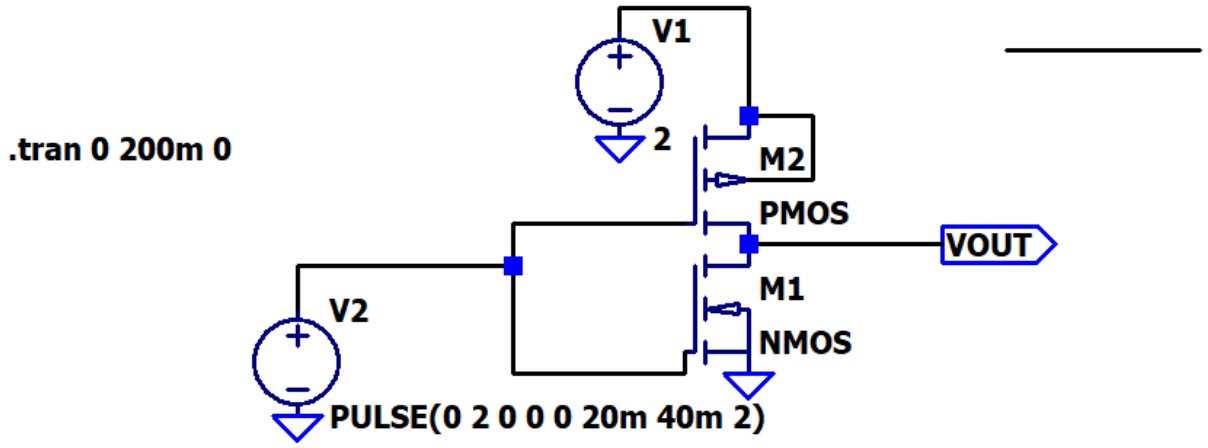
CMOS Inverter:

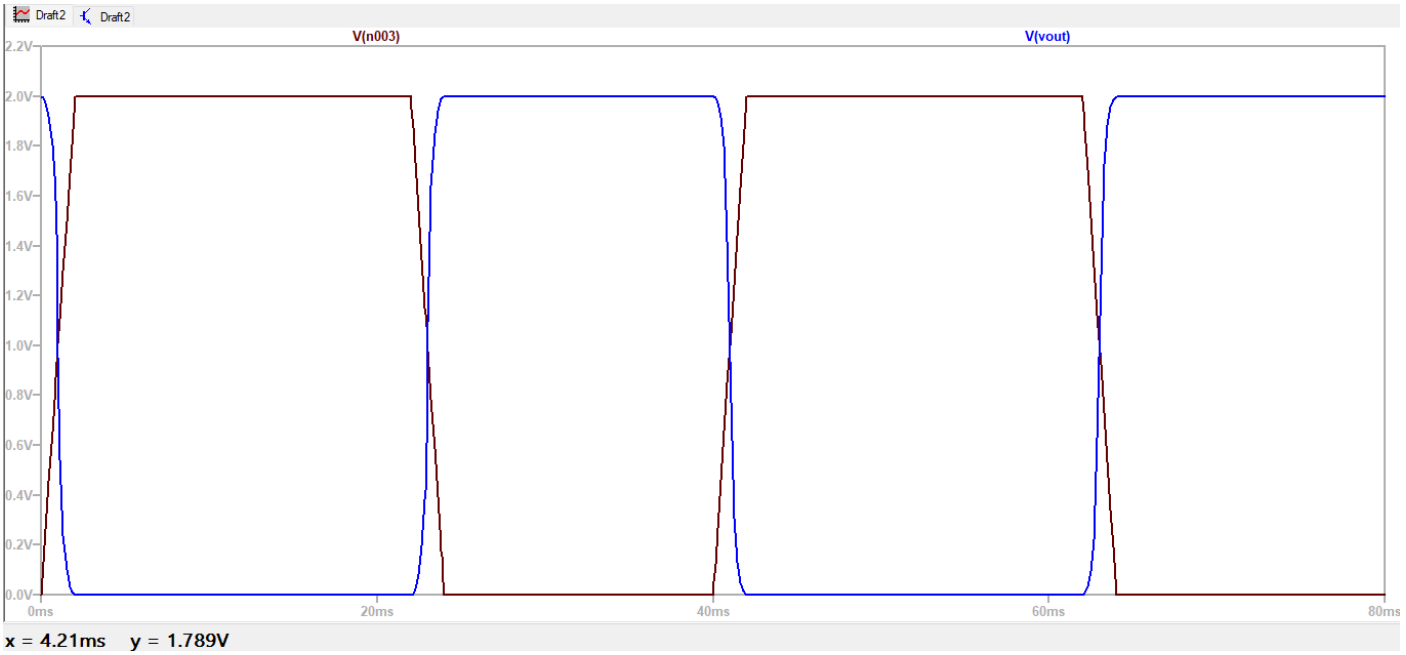


DC analysis:

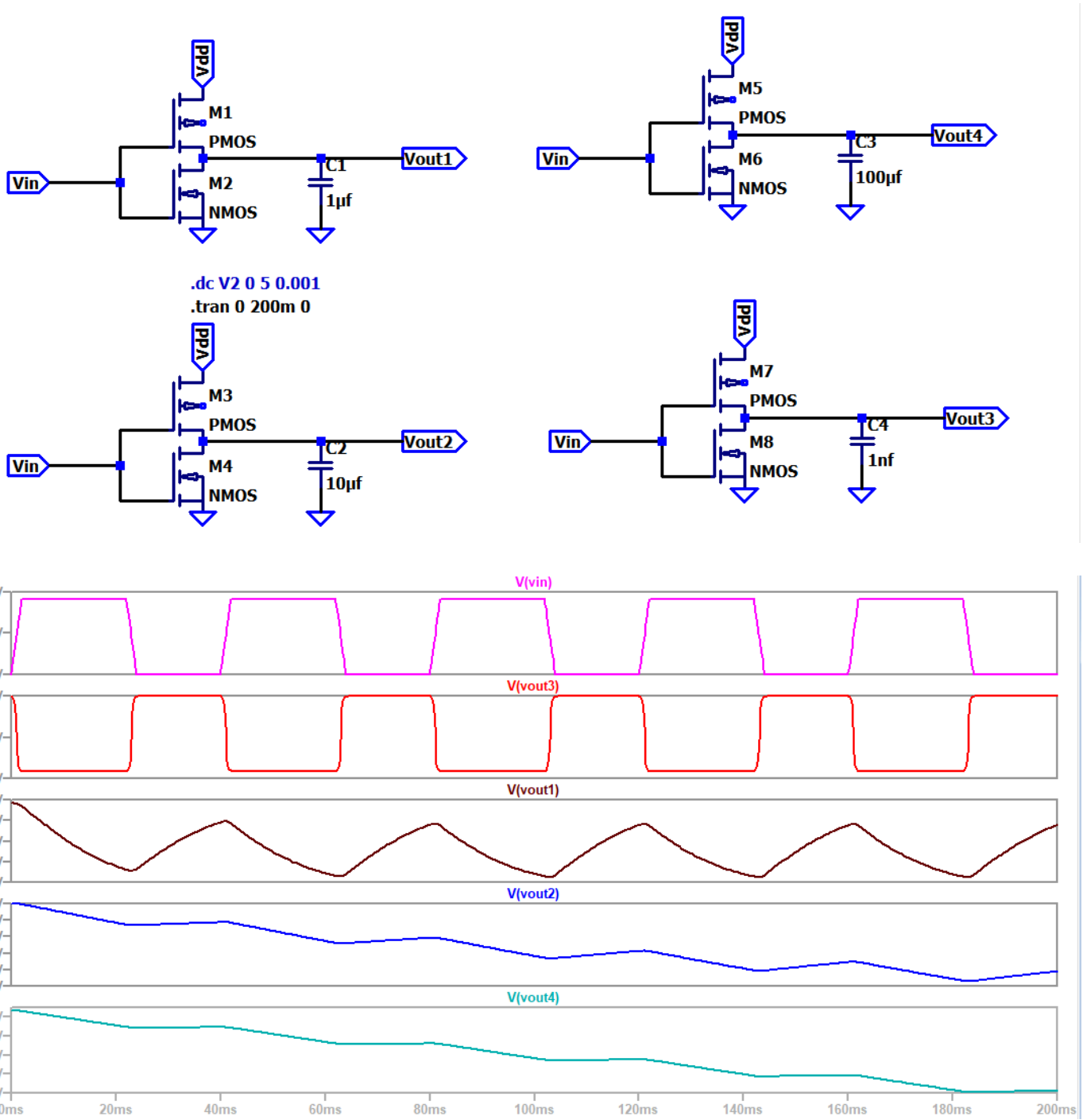


Transient Analysis:





Effect of C_{load} on Transient analysis:

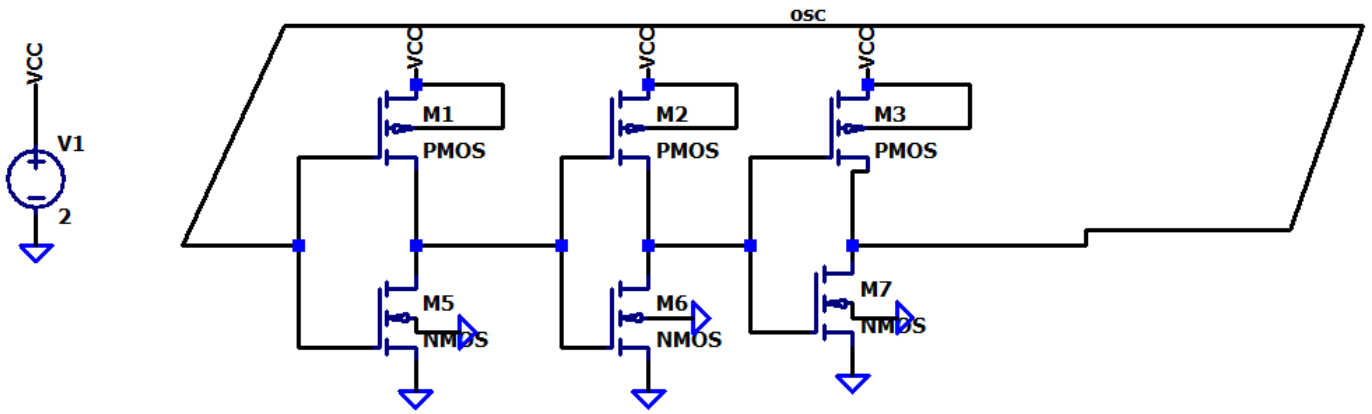


EXPERIMENT 3:

AIM: To design and plot the output characteristics of a 3 stage inverter ring oscillator.

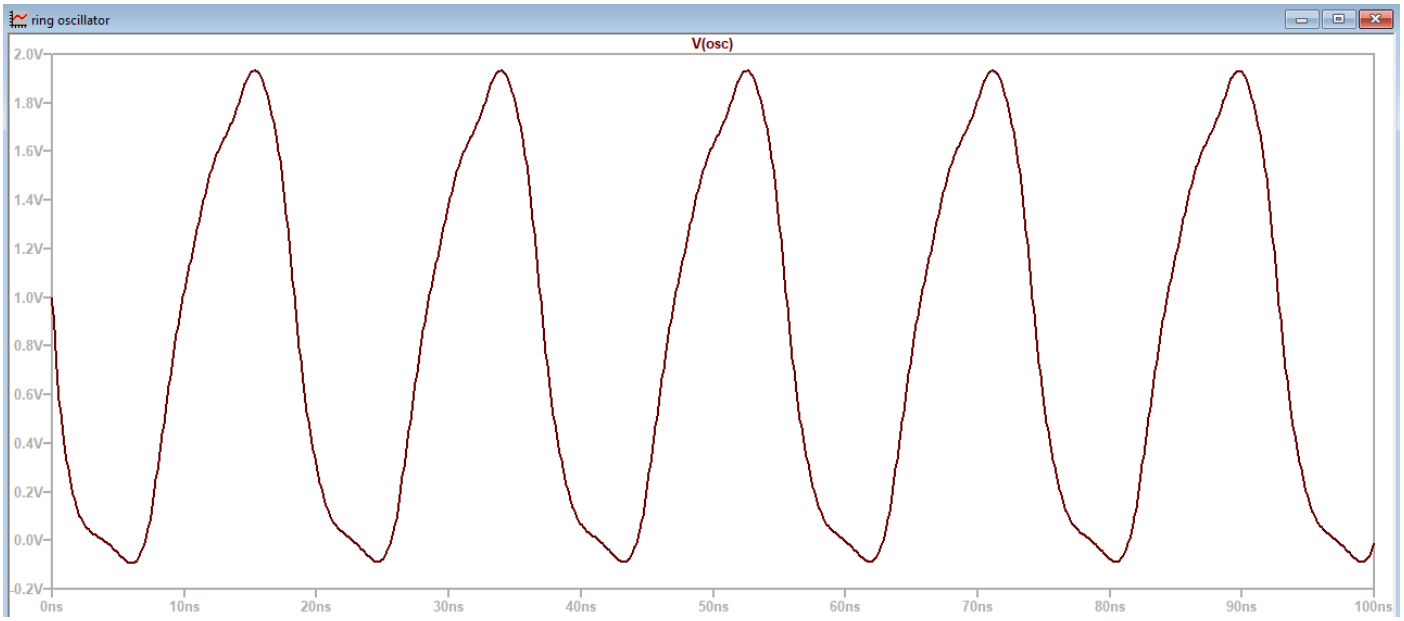
Ring Oscillator:

CIRCUIT:




```
.model NMOS NMOS LEVEL=14
.model PMOS PMOS LEVEL=14
.ic V(osc)=1
```

```
.tran 100n
```



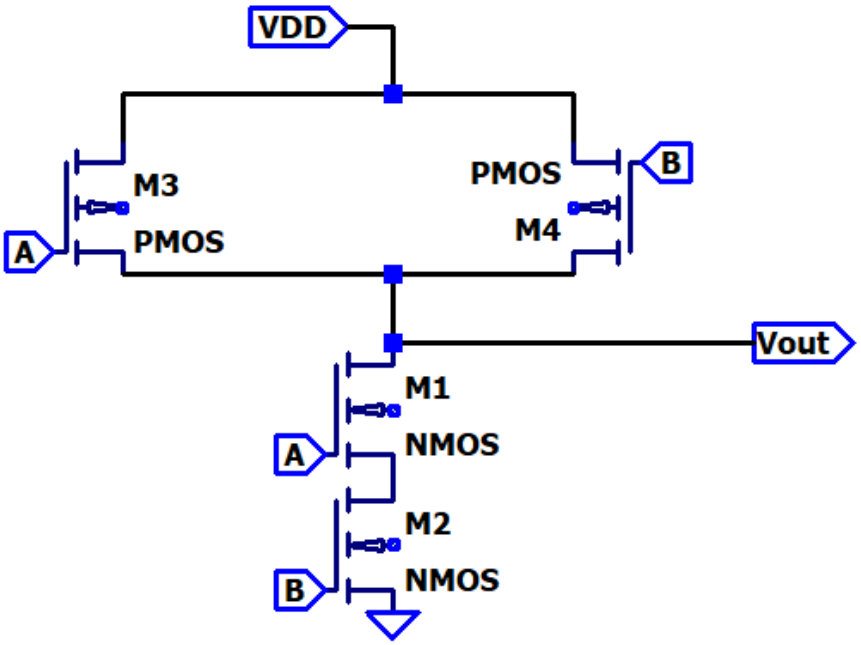
EXPERIMENT 4:

AIM: To design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS technology.

Various Logic Gate Using CMOS logic

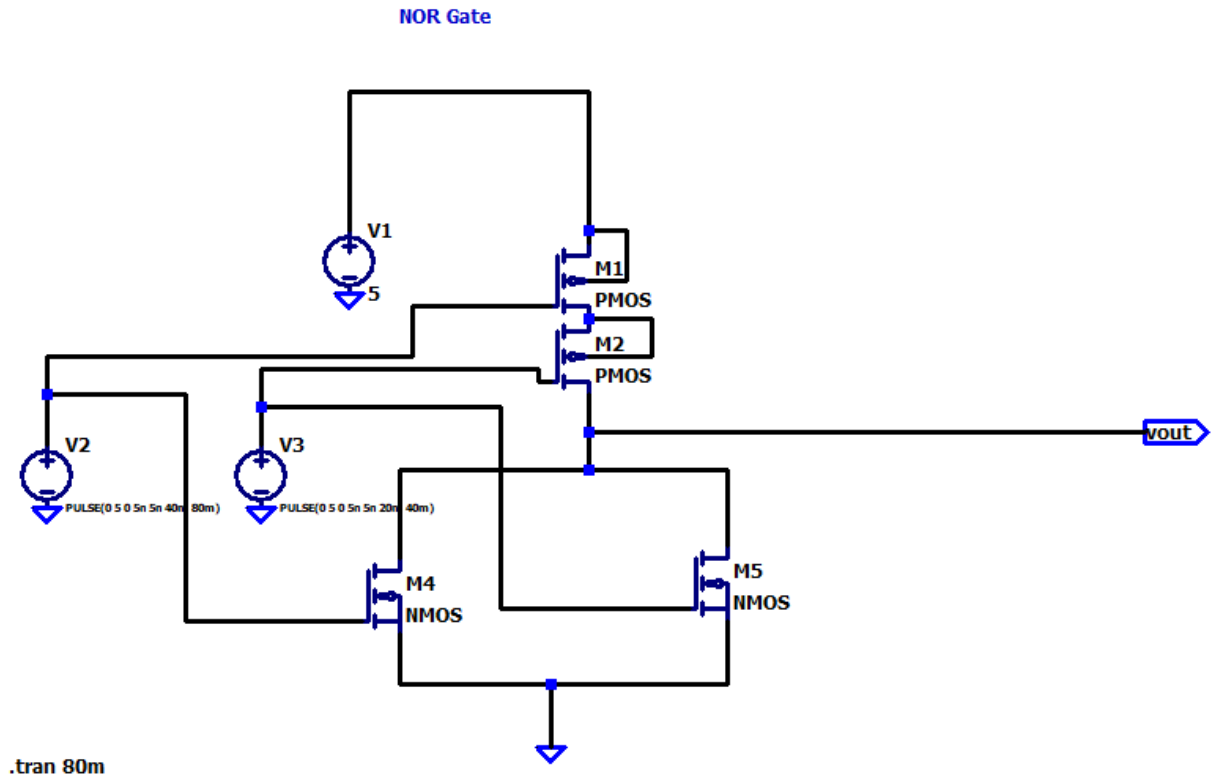
CIRCUIT:

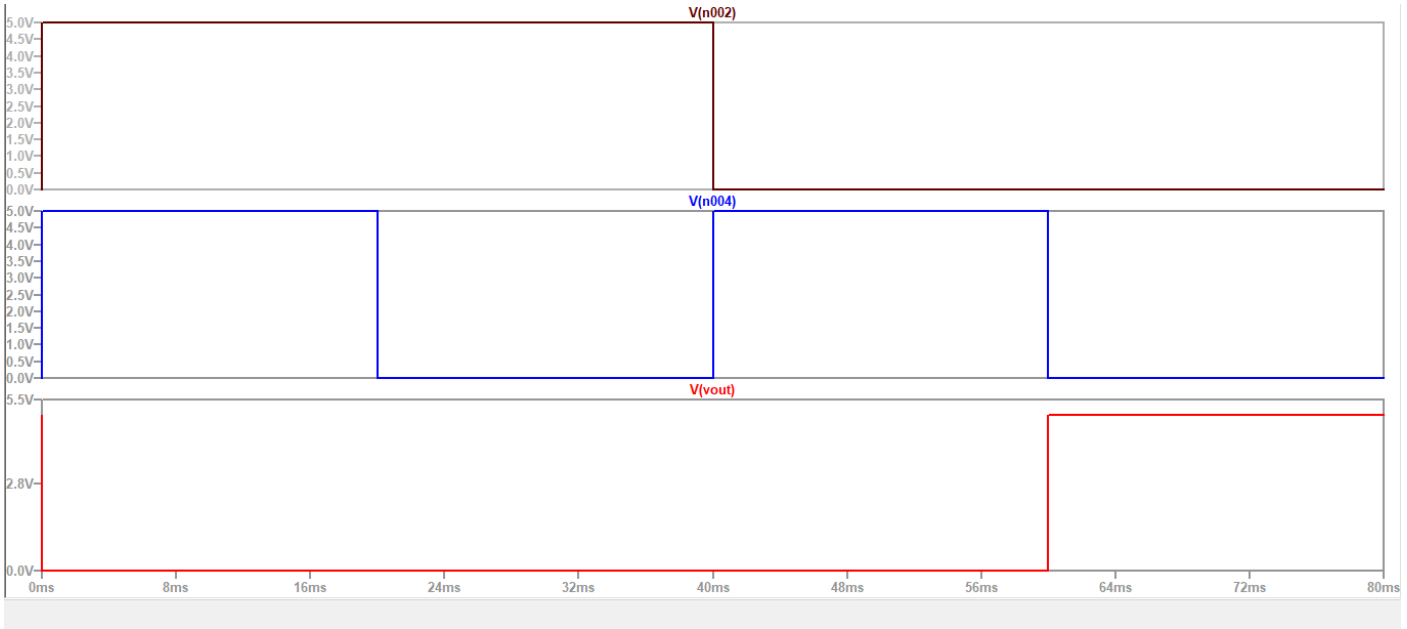
NAND Gate:



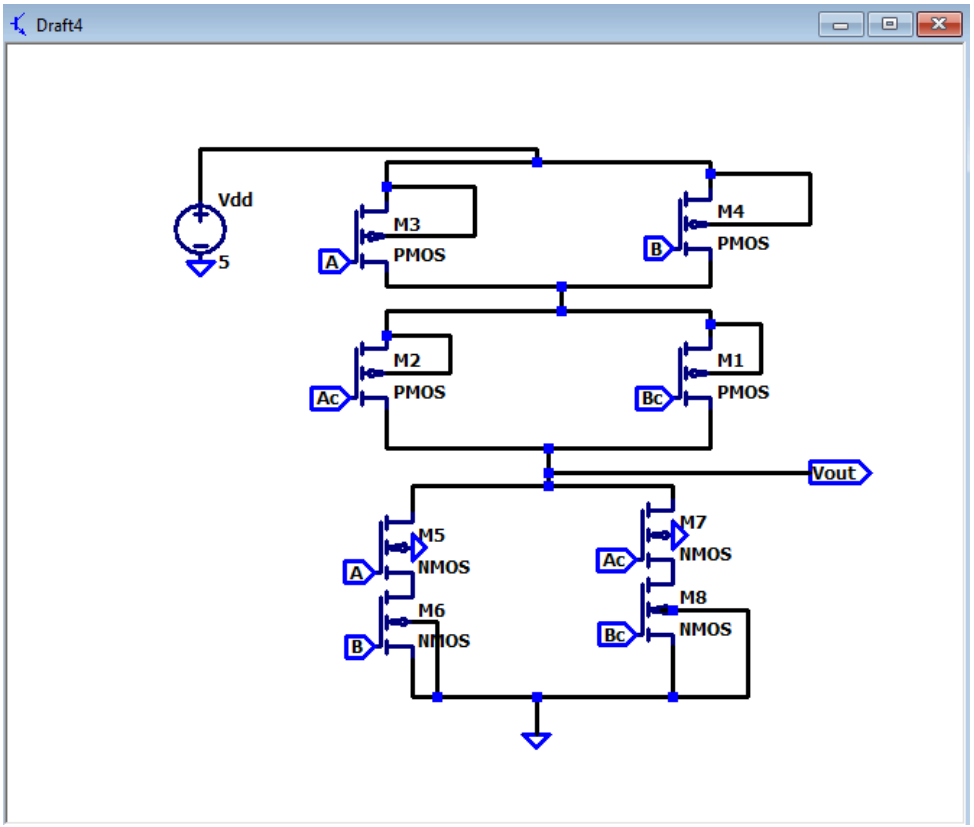

Draft6
V(a)
V(b)
V(vout)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0.0s
0.4s
0.8s
1.2s
1.6s
2.0s
2.4s
2.8s
3.2s
3.6s
4.0s

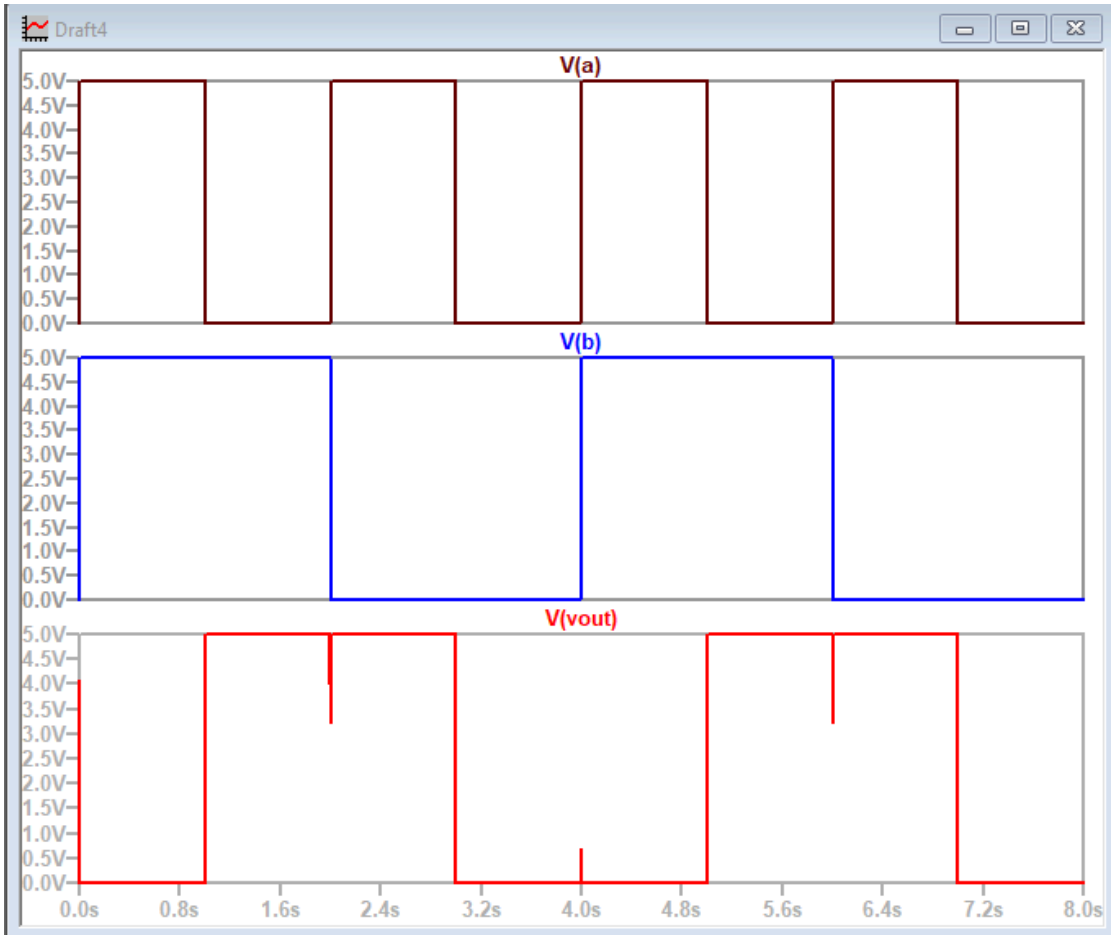
NOR gate:


NOR Gate
V1
5
M1
PMOS
M2
PMOS
V2
V3
vout
M4
NMOS
M5
NMOS
.tran 80m

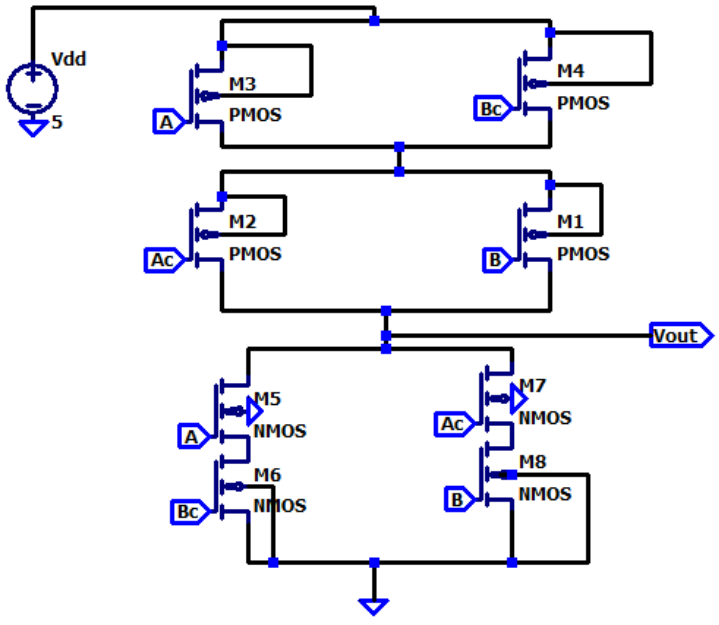

V(n002)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
V(n004)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
V(vout)
5.5V
2.8V
0.0V
0ms
8ms
16ms
24ms
32ms
40ms
48ms
56ms
64ms
72ms
80ms

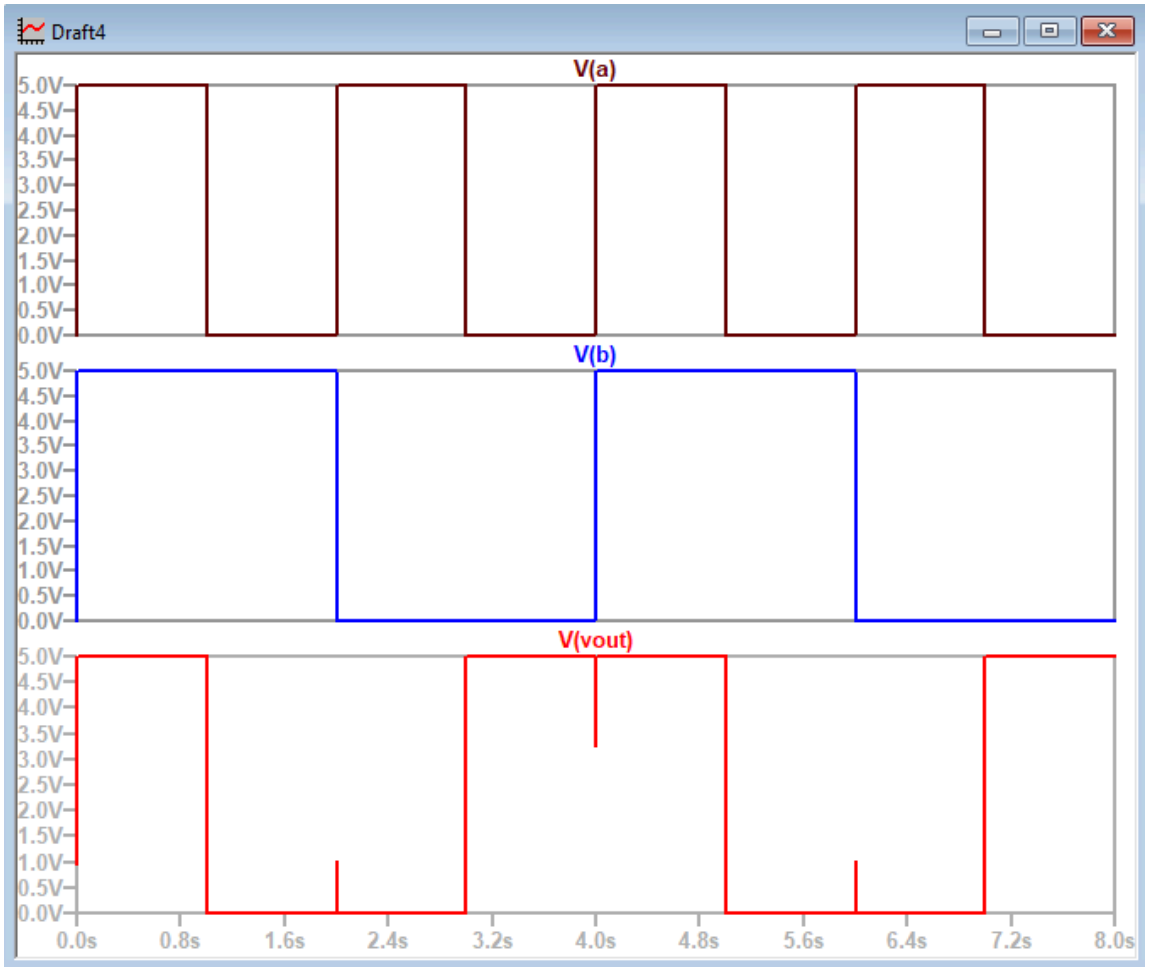
XOR Gate:


Draft4
Vdd
5
M3
PMOS
A
M4
PMOS
B
M2
PMOS
Ac
M1
PMOS
Bc
Vout
M5
NMOS
A
M6
NMOS
B
M7
NMOS
Ac
M8
NMOS
Bc


Draft4
V(a)
V(b)
V(vout)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0.0s
0.8s
1.6s
2.4s
3.2s
4.0s
4.8s
5.6s
6.4s
7.2s
8.0s

XNOR GATE:


Vdd
5
M3
PMOS
A
M4
PMOS
Bc
M2
PMOS
Ac
M1
PMOS
B
Vout
M5
NMOS
A
M6
NMOS
Bc
M7
NMOS
Ac
M8
NMOS
B

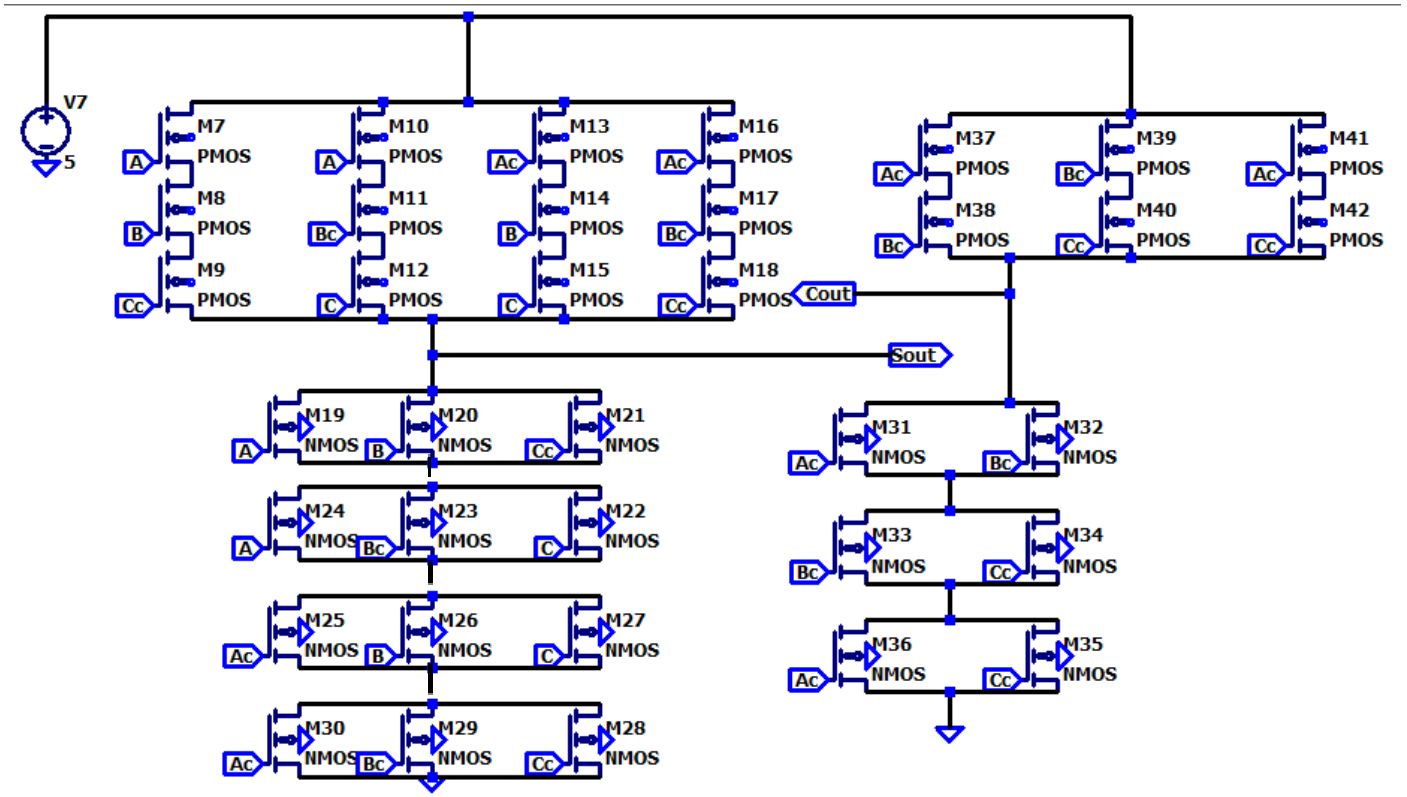

Draft4
V(a)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
V(b)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
V(vout)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0.0s
0.8s
1.6s
2.4s
3.2s
4.0s
4.8s
5.6s
6.4s
7.2s
8.0s

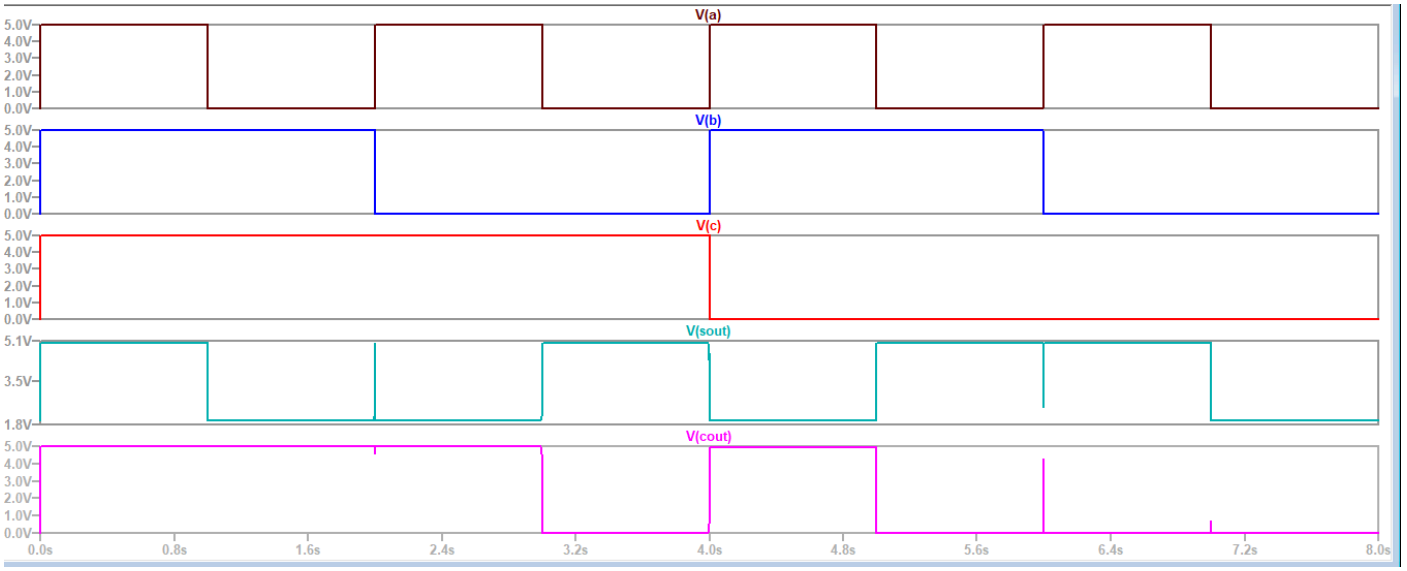
EXPERIMENT 5:

AIM: To design full adder using CMOS technology.

Full Adder:

CIRCUIT:





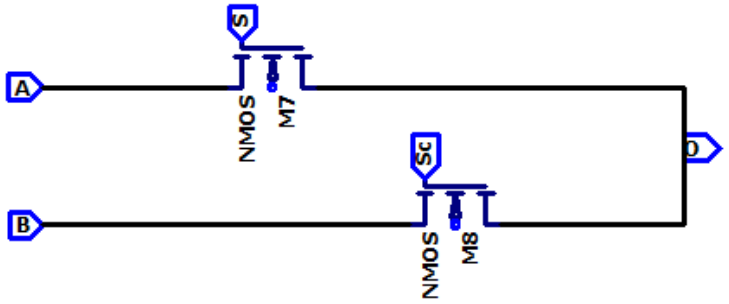
EXPERIMENT 6:

AIM: To design 2x1 digital MUX using transmission gate logic

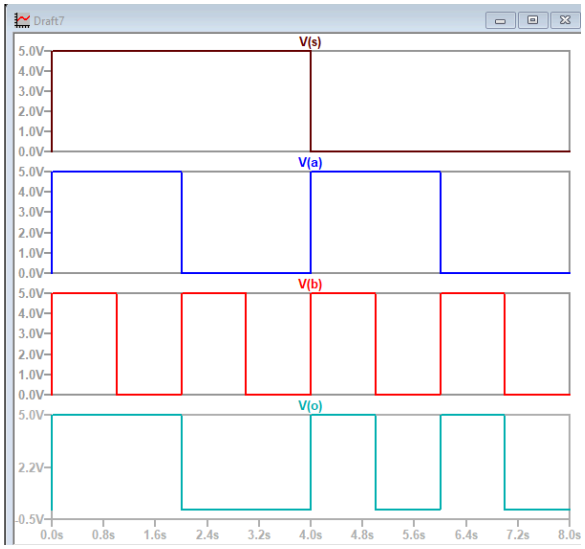
2x1 Multiplexer:

CIRCUIT:

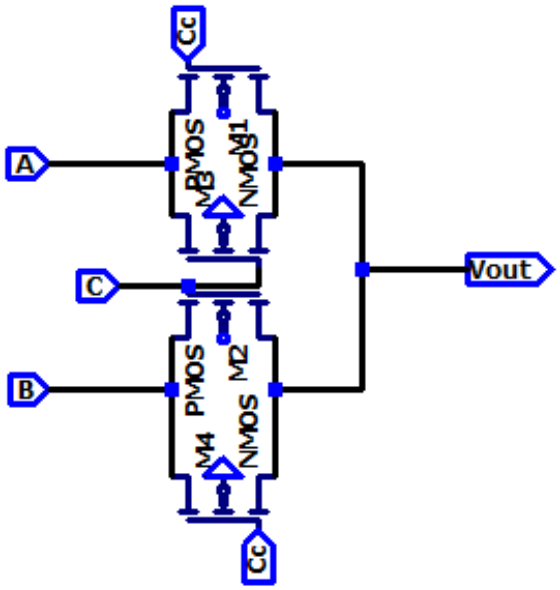
2x1 Using Pass Transistors :



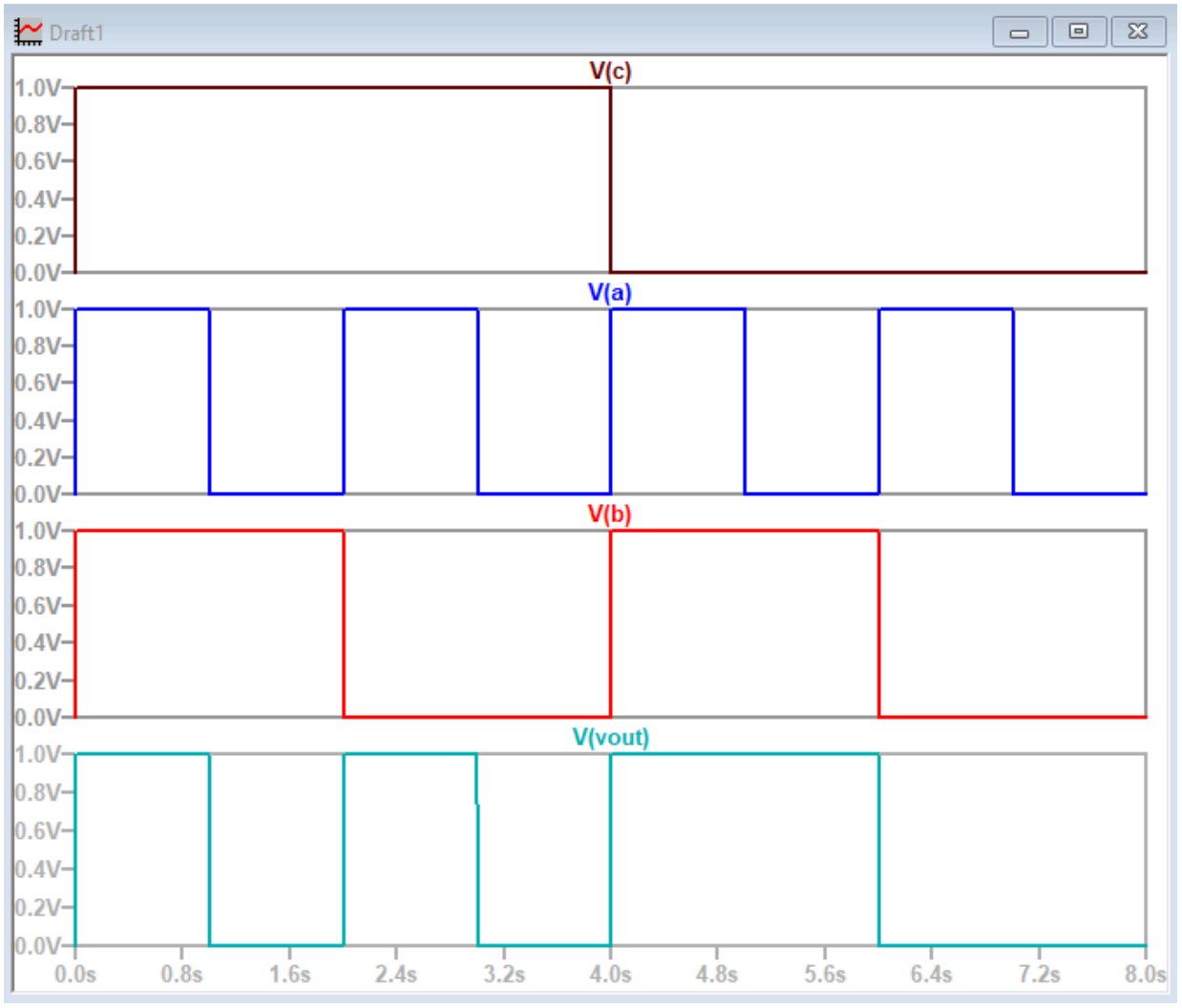
OUTPUT:



Using Transmission gate:



OUTPUT:

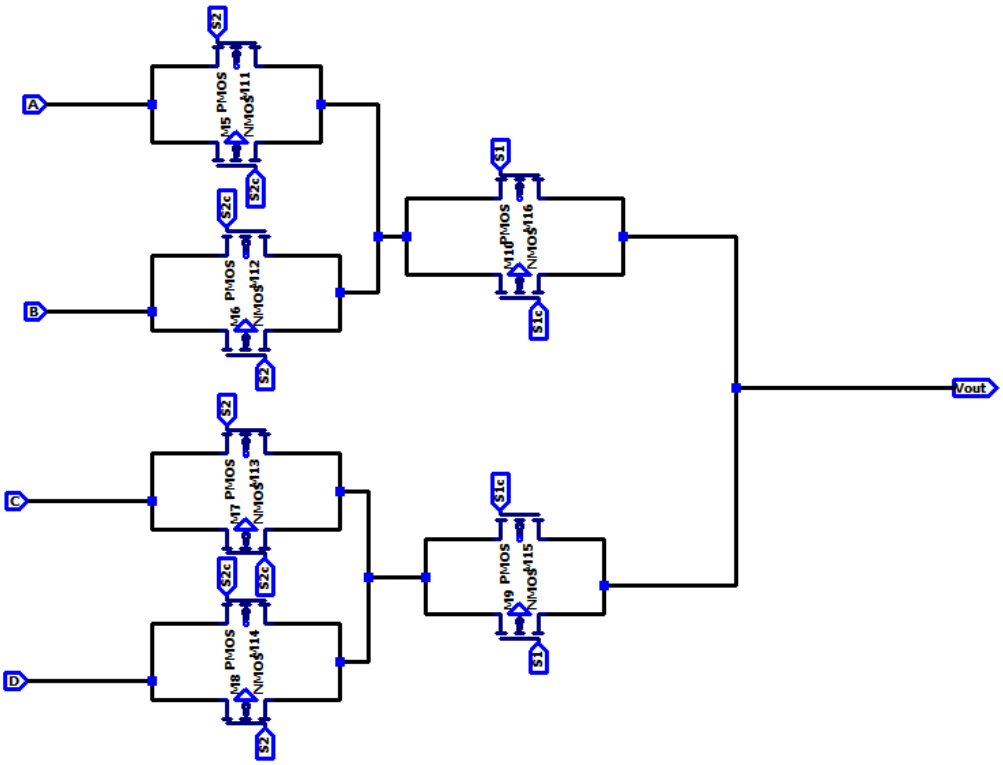


EXPERIMENT 7:

AIM: To design and plot the characteristics of a 4x1 digital multiplexer using pass-transistor logic.

4x1 Using Transmission Gate :

CIRCUIT:



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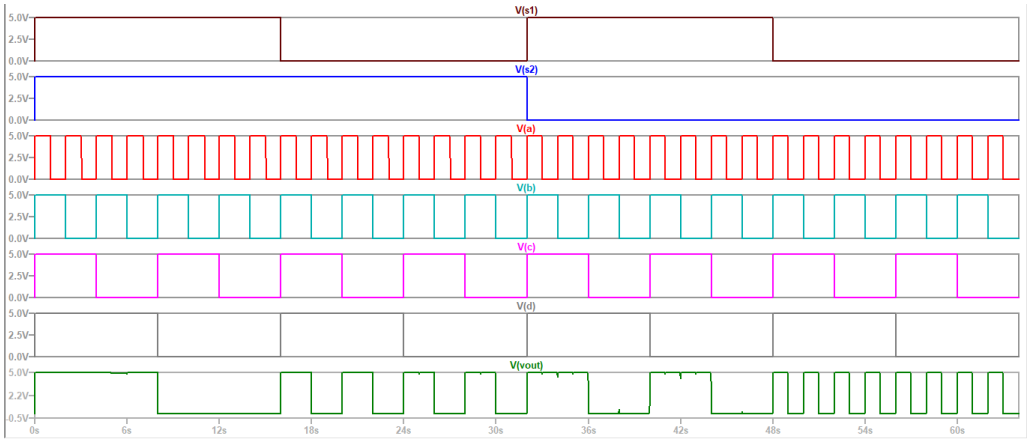
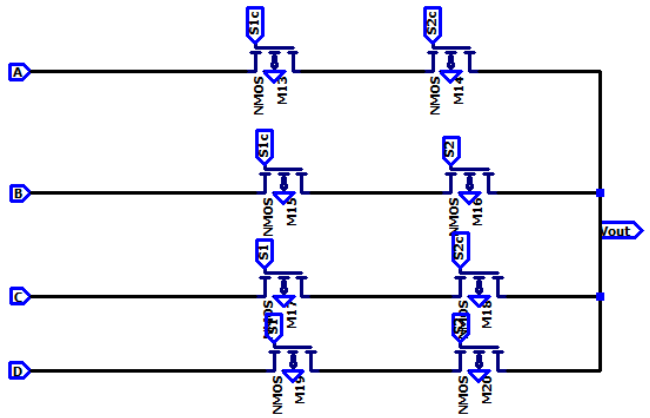


Using Pass transistor logic:



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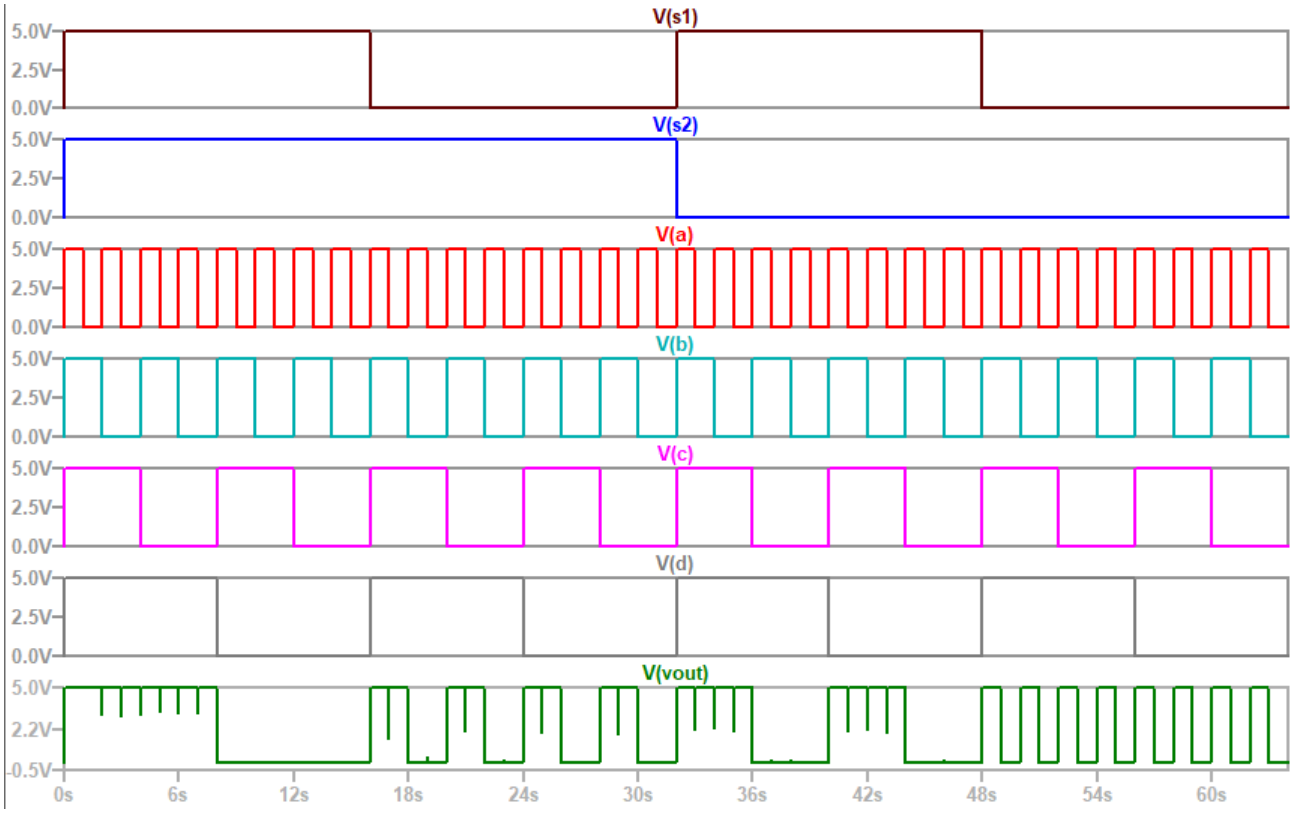
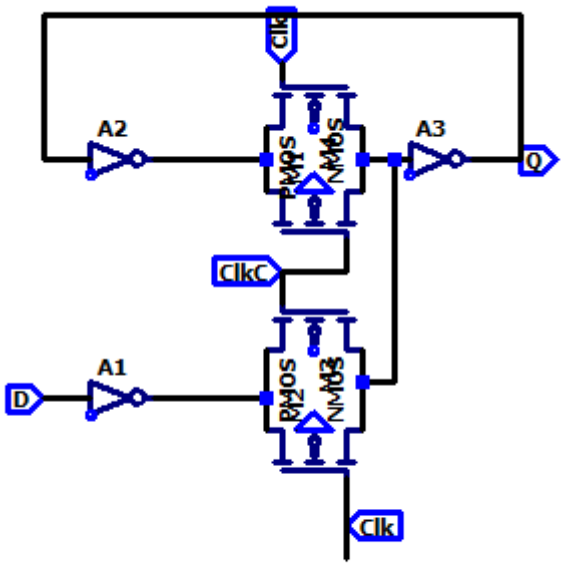


EXPERIMENT 8:

AIM: To design and plot the characteristics of a positive and negative latch/master-slave edge triggered registers based on multiplexers.

Positive Latch:

CIRCUIT:



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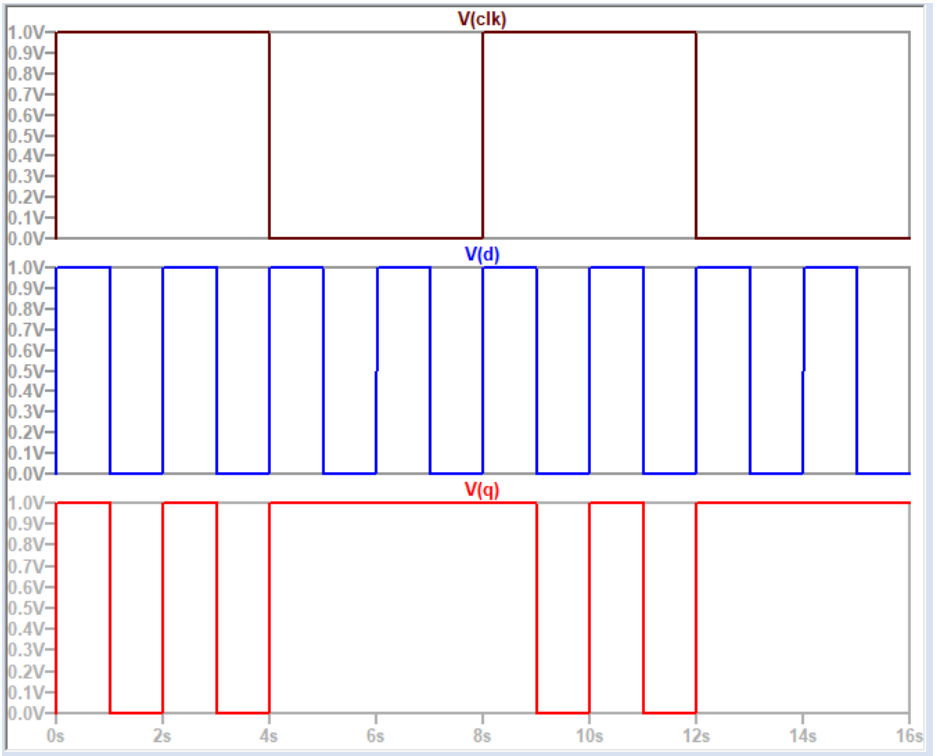
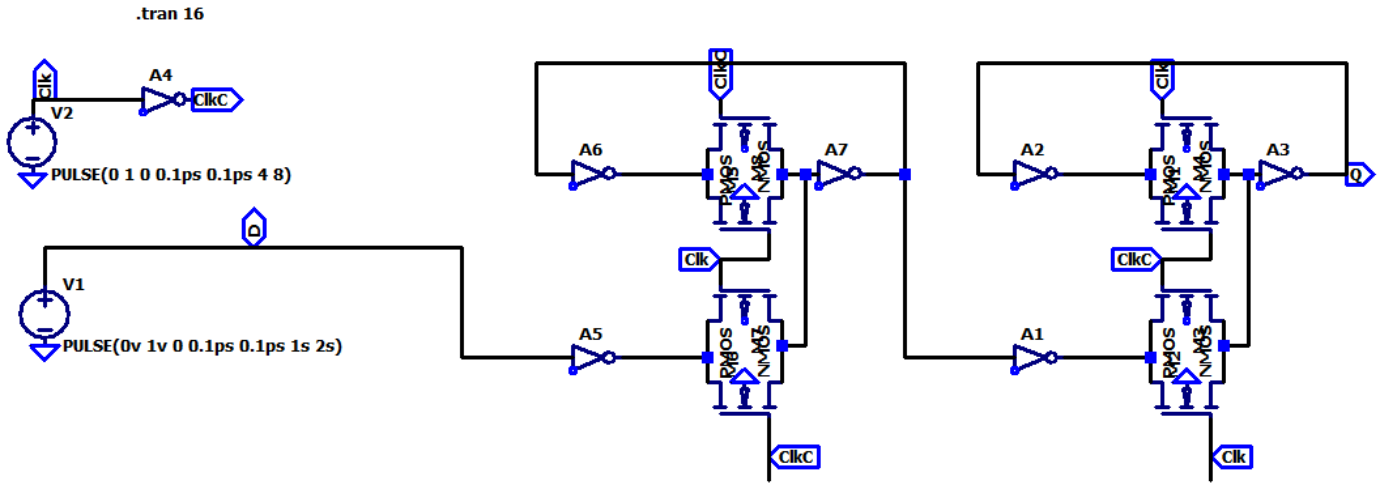
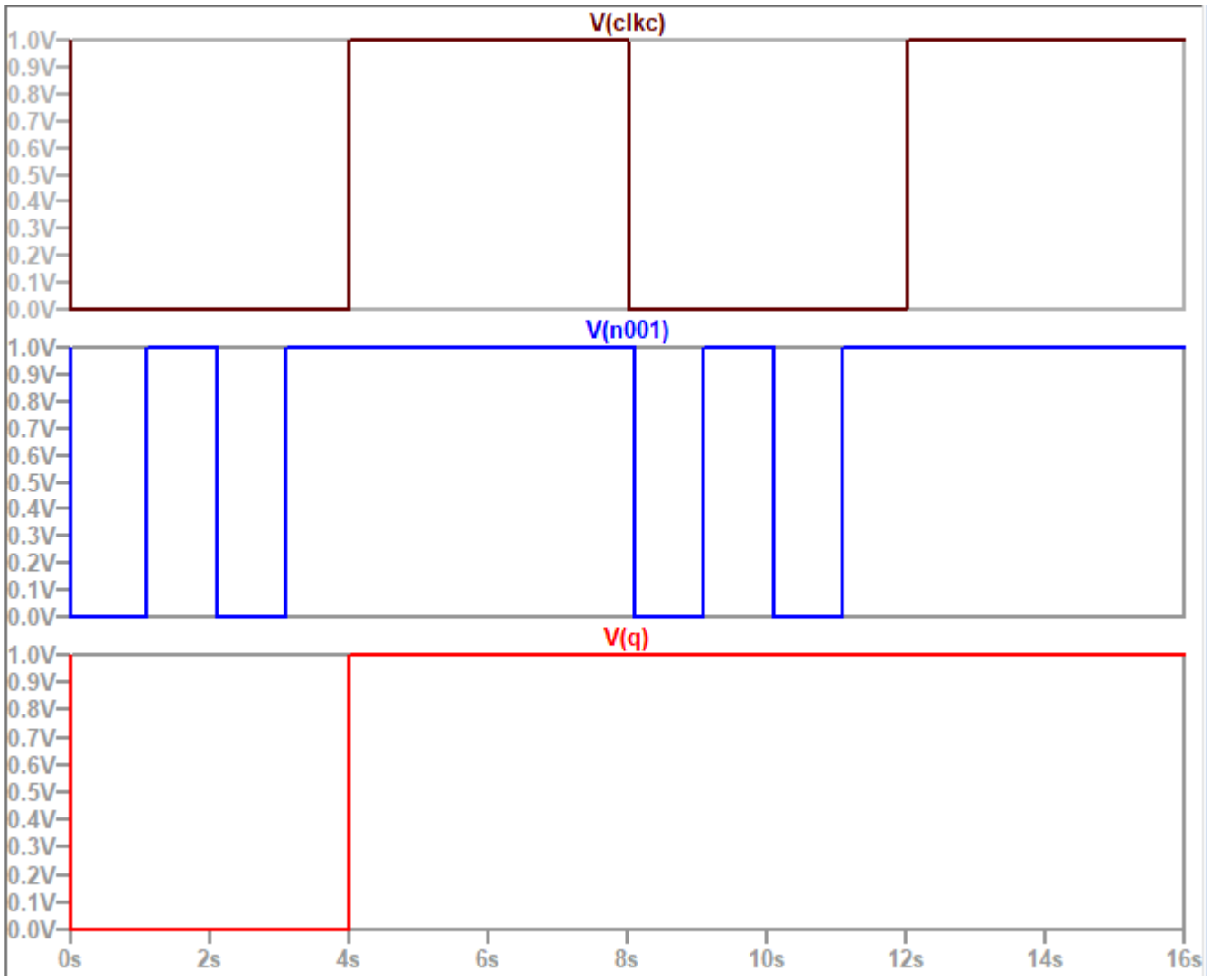


Register using Master slave Config:

CIRCUIT:



OUTPUT:



For negative edge triggering: