Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

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Instructor:	**Dr. Fei Yuan**

Assignment/Lab Number:	*Design Project*
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By: S.AbdulRahman

Date of Preparation April 3, 2024

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1. Introduction

The report for the final Design Project for ELE404, is presented herein. The project is centered on Bipolar Junction Transistors (BJT) and how one can design, simulate, analyze, implement, and test a single-supply, multistage, inverting, transistor amplifier which fulfills a set of specifications.

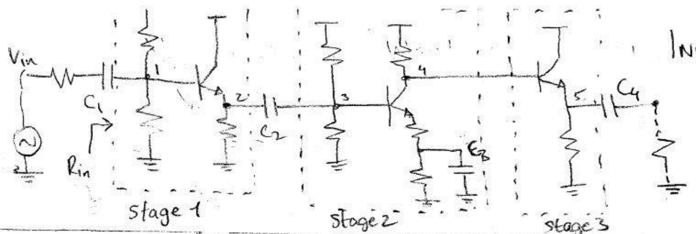
2. Objectives

The main objective of this project is to design an amplifier that fulfills the summarized specifications below

- Power supply: $+10V$ relative to the ground;
- Quiescent current drawn from the power supply: no larger than $10\ mA$;
- No-load voltage gain (at 1 kHz): $|Avo|$ = 50 (± 10%);
- Maximum no-load output voltage swing (at 1 kHz): no smaller than 8 V peak to peak;
- Loaded voltage gain (at 1 kHz and with RL = 1 $k\Omega$): no smaller than 90% of the no-load voltage gain;
- Maximum loaded output voltage swing (at 1 kHz and RL = 1 $k\Omega$): no smaller than 4 V peak to peak;
- Input resistance (at 1 kHz): no smaller than $20\ k\Omega$;
- Amplifier type: inverting or non-inverting;
- Frequency response: 20 Hz to 50 kHz ($-3dB$ response);
- Type of transistors: BJT;
- Number of transistors (stages): no more than 3;
- Resistances permitted: values smaller than $220\ k\Omega$ from the E24 series;
- Capacitors permitted: $0.1\ \mu F$, $1.0\ \mu F$, $2.2\ \mu F$, $4.7\ \mu F$, $10\ \mu F$, $47\ \mu F$, $100\ \mu F$, $220\ \mu F$;
- Other components (BJTs, diodes, Zener diodes, etc.): only from your ELE404 lab kit.

3. Initial Design and Calculations

DESIGN PROJECT
Syed AbdulRahman



INITAL DESIGN

Stage 1: Common Collector CC

- Take $I_C = 0.1mA$
- $A_V = \frac{V_o}{V_{in}}$ ← 8V, 50; taking V_o to be 8V to match specification of 8vpp. $V_o \approx 8V$

$\rightarrow V_{in} = 0.16V$

Gain for $CC \approx 1$

$1 = \frac{V_o}{0.16} \Rightarrow V_o = 0.16V$ (E)

$V_o = V_E$

$V_E = R_E I_E$

$R_E = \frac{0.16V}{0.1mA} \Rightarrow \boxed{R_E = 1.6k\Omega}$

$V_{BE} = 0.7$

$V_{BE} = V_B - V_E$ $\quad g_m = \frac{I_C}{V_T} = \frac{0.001}{0.026}$

$V_B = 0.86V$

$\frac{V_B}{V_{CC}} = \frac{R_2}{R_1 + R_2}$

$R_1 = \frac{0.914 R_2}{0.086} \approx R_1 = 10 R_2$

- Set $R_1 = R_2 = 50k\Omega$ → Better results when $R_1 = R_2$

$R_{in} = R_1 \| R_2 \| r_{\pi} + R_E(1+\beta)$

$= \frac{1}{\frac{1}{50} + \frac{1}{50} + \frac{1}{\frac{100}{0.001/0.026} + 1.6(101)}}$

$\boxed{R_{in} = 24.77K \geq 20K}$ ✓

Stage 2: Common Emmiter CE

- Take $I_C = 2mA$

$V_C = V_{o,max} = \frac{V_{CC} - V_{sat}}{2}$

$V_{sat} \approx 0.3V \quad V_{o,max} = 4.85V$

$V_C = \frac{1}{2}(V_{CC} + V_E) = 5.5V$

$V_C = V_{CC} - R_C I_C \Rightarrow \boxed{R_C = 2.25k \approx 2.4k}$

$I_E = I_C = 2mA$

$\boxed{V_E = \frac{1}{10} V_{CC} = 1V}$

Since CC Voltage Gain ≈ 1
so Gain Must come from CE

$50 = \frac{-g_m R_C}{1 + g_m R_{E_2}}$

$\Rightarrow R_{E_2} = 34\Omega \rightarrow \boxed{24\Omega}$

$V_E = I_E(R_{E_2} + R_{E_3})$

$\Rightarrow R_{E_3} = 466\Omega \rightarrow \boxed{510\Omega}$ ← better results by testing

$V_B = V_{CC}\left(\frac{R_3}{R_3 + R_4}\right) \quad V_B = 0.7 + 1$

$\frac{1.7}{10} = \frac{R_3}{R_3 + R_4} \quad V_B = 1.7V$

$R_3 = 5R_4$

$R_3 \approx 4R_4$ ← Better results

- Set $R_3 = 200K \quad R_4 = 50K$

Stage 3: Common Collector CC

Want $R_{E_4} \approx R_L$ due to loading effect

- Set $R_{E_4} = 1.5k\Omega$

$V_B = 8V \quad V_o = 8V = V_E$

$I_E = \frac{V_E}{R_E} = 5.33mA \approx I_C$

Total Qusient current: $0.1 + 2 + 5.33$

$\boxed{= 7.43mA \leq 10mA}$ ✓

Reason for CC at end is so that gain does not fluctuate when load is added.

Note: Emitter degeneration resistance is important in order to maintain the gain of the CE stage.

Large capacitance values are expected for C_2 & C_3. Set $C_2 = C_3 = 220 uF$

Since R_{in} value is high C_1 value is not requried to also be high

Large capacitance value for C_4 is also expected, so it blocks any DC current flowing into the load
Provides a low-resistance path from output of amplifier to load.

hence take $C_2 = C_3 = 220uF$
$C_4 = 100uF$
$C_1 = 10uF$

$A_V = \frac{V_4}{V_s} = \underbrace{\frac{V_5}{V_4}}_{=1} \times \frac{V_3}{V_3} \times \underbrace{\frac{V_2}{V_1}}_{=1} \times \underbrace{\frac{V_1}{V_s}}_{=1}$ ← Input stage (CC2, CE, CC1)

$= \frac{-g_{m1} R_C}{1 + g_{m1} R_{E_2}} = 50$ ✓

3. Circuit under Test

Figure 1 below shows the final design of the 3 stage BJT amplifier circuit. Thus, the circuit consists of 3 2N3904 transistors, 4 electrolytic capacitors and 10 resistors to create a CC-CE-CC amplifier.

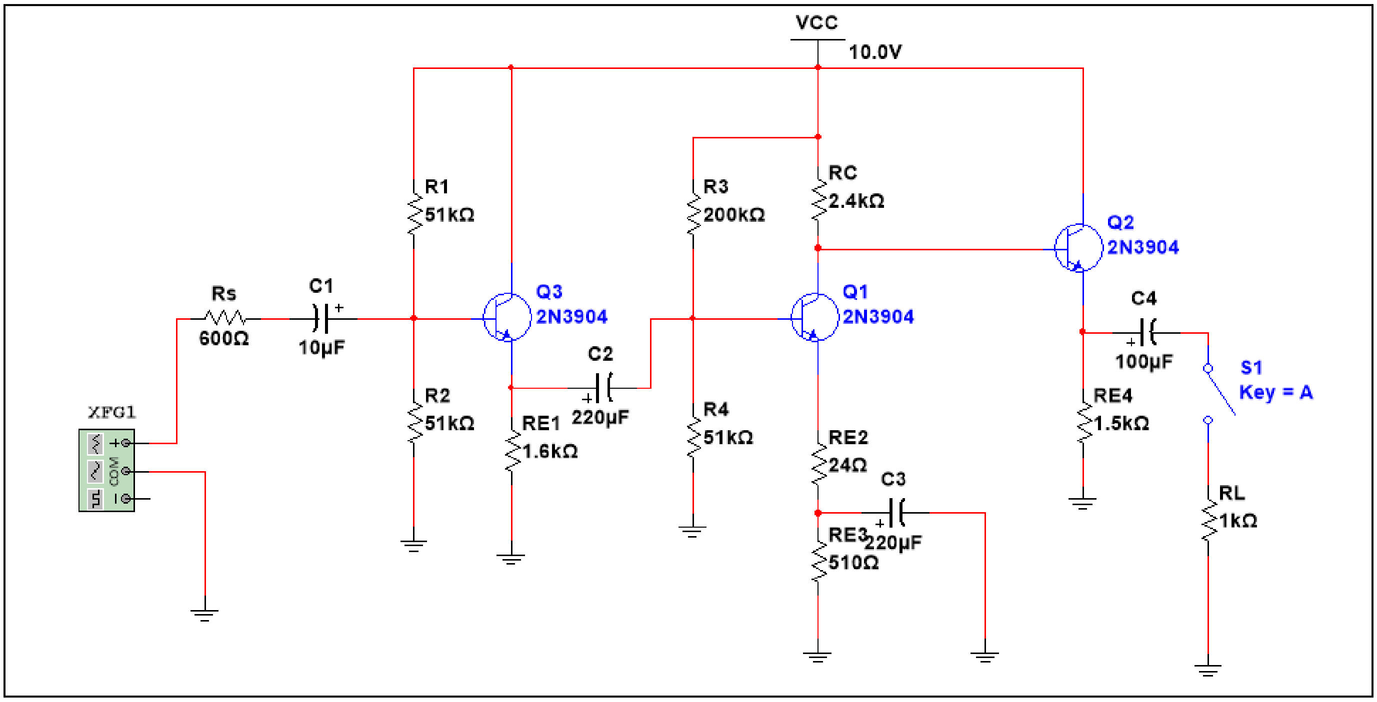


Figure 1: Final design of multistage amplifier using Multisim (CC-CE-CC)

Stage 1: Common Collector (CC)

Placing a Common Collector (CC) stage at the start of an amplifier ensures a high input resistance (Rin), minimizing signal loss from impedance mismatches. This is crucial when the source can't drive low-impedance loads, which is a common limitation of a Common Emitter (CE) stage placed first due to its lower Rin. The CC stage acts as a buffer, allowing subsequent stages to amplify a strong, undistorted signal.

Stage 2: Common Emitter (CE)

To satisfy the requirement for high voltage gain in an amplifier circuit, a Common Emitter (CE) stage is essential due to its high voltage gain characteristics. While a Common Collector (CC) stage at the input ensures a high input resistance, adding a CE stage between the CC input stage and the output provides the necessary amplification of the voltage. The CE stage's lower input impedance is less of an issue in this configuration, as the preceding CC stage effectively isolates it from the source. Thus, the CE stage can leverage its strength in voltage amplification without degrading the source signal, ensuring the amplifier meets its gain specifications.

Stage 3: Common Collector (CC)

Adding a Common Collector (CC) stage, also known as an emitter follower, at the end of an amplifier circuit acts as an effective buffer due to its high input and low output impedance. This buffering action helps maintain the overall voltage gain when a load is connected, as the CC stage minimizes the load's impact on the preceding amplification stages. With the CC stage's near unity voltage gain and power gain, it ensures stable amplifier performance, making the loaded voltage gain largely consistent with the no-load gain.

Resistance and Capacitance Values

For the first stage, the resistor RE was chosen based on the collector current IC=IE , ensuring proper biasing and stability. The resistors R1 and R2 were selected to be equal to satisfy the input resistance (Rin) requirement and provided better results than the calculated value of R1=10R2. The input voltage Vin of 0.16V was determined by considering the maximum peak-to-peak voltage of 8V and a gain of 50, ensuring the amplifier operates within its linear range and avoids clipping.

In the second stage, RC was calculated based on the chosen current to set the correct quiescent point. The emitter resistor RE2 and RE3 was solved using the transconductance *gm* and desired gain, emphasizing the importance of emitter degeneration in maintaining consistent gain. RE2 was added to reduce the clipping that was produced by RE3 with the isolating capacitor (emitter degeneration). R3 was selected to be four times R4 to achieve the required biasing and gain ratios.

For the third stage, RE4 was chosen to ensure it does not significantly affect the load resistance RL, maintaining the overall gain and output integrity of the amplifier. Should be noted that during simulation calculated values of some resistances need to be changed slightly in order to match the E24 series.

Regarding capacitance values, C2 and C3 needed to be large enough to maintain a gain of 50, serving as isolating capacitors that prevent DC interference while allowing AC signals to pass through effectively. C1 could be smaller as it handles the initial coupling, but C4 needed to be large, acting as an isolating capacitor to preserve signal integrity across stages and ensure stable gain throughout.

4. Experimental Results

This section presents a condensed analysis of the data and key findings.

Table 1: summary of elements and values in circuit

Circuit Elements and Values (Resistors from E24 series)			
R1	51kΩ	R2	51kΩ
R3	200kΩ	R4	51kΩ
RE1	1.6kΩ	RE2	24Ω
RE3	510Ω	RE4	1.5kΩ
C1	10uF	C2	220uF
C3	220uF	C4	100uF

Power Supply and Quiescent Current

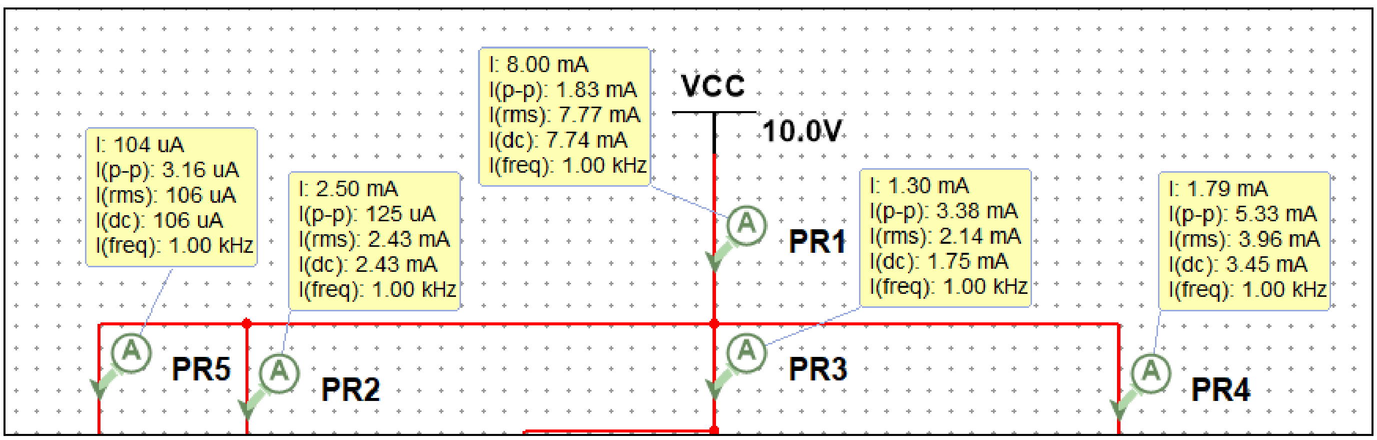


Figure 2: Power Supply Voltage and Quiescent current

The voltage is 10V and quiescent current drawn from the power supply is: 7.77mA $\leq$ 10mA.

Table 2: Tests for required specifications

Voltage Gain [V/V]	Vs Input Signal [mVpp]	Vo Output Signal [Vpp]	Voltage Gain [V/V]
Avo (without load)	83.996	4.49	53.45
Av (with load)	83.778	4.038	48.198

Waveforms

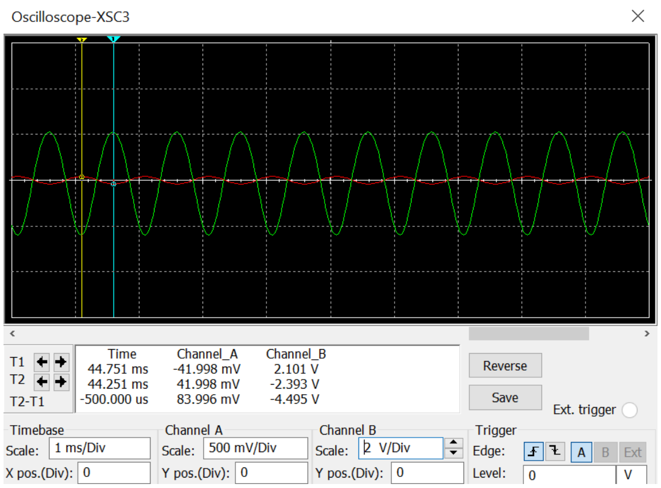


Figure 3: Without Load

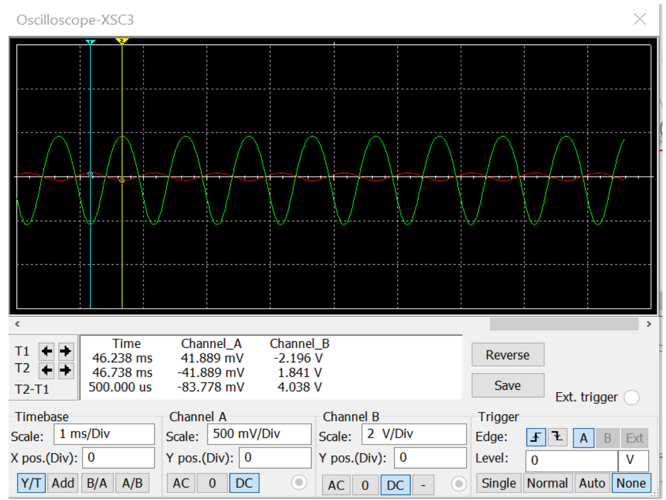


Figure 4 : With Load

The table presents measurements that align well with the given amplifier specifications. The measured values for both loaded and no-load conditions illustrate that the amplifier not only meets but slightly exceeds the stated specifications, demonstrating good performance characteristics suitable for the intended application.

No-Load Voltage Gain

In table 2, the no-load voltage gain Avo at 1 kHz is listed as 53.45 V/V, which sits comfortably within the ±10% tolerance of the specified 50 V/V, offering a slight but acceptable margin above the target value. This indicates that the amplifier is performing slightly better than the minimum specification when no external load is applied.

Loaded Voltage Gain

In figure 4, when the amplifier is loaded, with RL=1kΩ, the voltage gain Av drops to 48.198 V/V, which is more than 90% of the no-load voltage gain, fulfilling the requirement that the loaded voltage gain should not fall below this threshold. Specifically, 90% of 53.45 V/V is approximately 48.105 V/V, and the measured loaded gain of 48.198 V/V exceeds this, verifying that the amplifier maintains a high level of performance even under load.

Maximum loaded output voltage swing

Lastly, the loaded output voltage swing is observed to be 4.038 V peak-to-peak at 1 kHz as seen in figure 4, which is just slightly above the minimum requirement of 4 V peak-to-peak. This value confirms that the amplifier can drive a 1 kΩ load without a significant loss in signal amplitude, thereby meeting the design criteria for maximum loaded output voltage swing.

Amplifier type

As seen in figure 3 and 4 the amplifier is of inverting type

Table 2: Tests for required specifications

Vs Input Signal [mVpp]	Vo Output Signal [Vpp]	Voltage Gain [V/V]
165.628	8.101	48.9

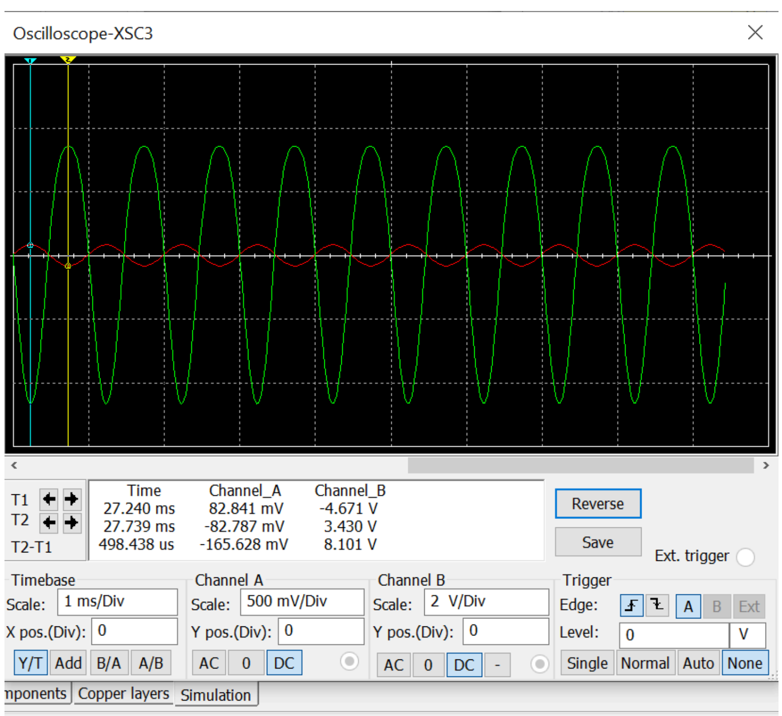


Figure 5: No load max swing 8Vpp

Maximum no-load output voltage swing

The data presented in table 2, accompanied by the oscilloscope trace in figure 5, shows that the amplifier's maximum no-load output voltage swing at 1 kHz is 8.101 Vpp, which exceeds the specified minimum of 8 Vpp. While also the no-load voltage gain, Avo, at 1 kHz is listed as 48.9 V/V, which is within the ±10% tolerance of the specified 50 V/V.

Input resistance

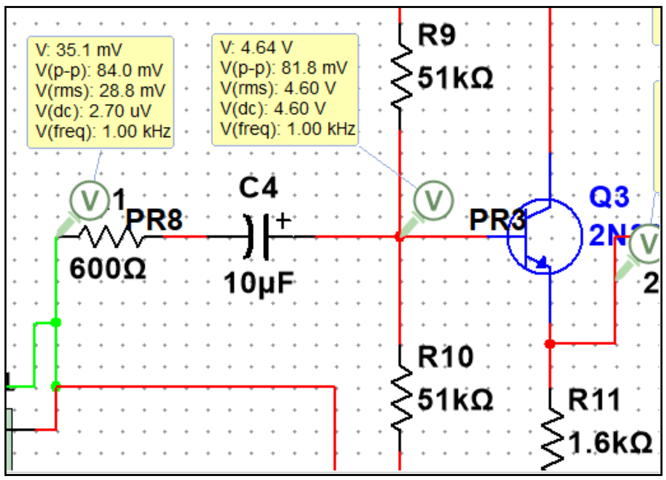


Figure 6: Voltage Division to find Rin

Calculations:

$VB = Vs\frac{Rin}{Rin+Rs}$

$Rin = \frac{VB \cdot Rs}{Vs - Vb}$

$Rin = \frac{81.8x10^{-3} \cdot 600}{84x10^{-3} - 81.8x10^{-3}}$

$Rin = 22309\Omega$

$22k\Omega \geq 20k\Omega$. The measured input resistance (Rin) of the amplifier is 22kΩ, which exceeds the specified requirement of at least 20kΩ, thereby satisfying the design criteria.

Frequency response:

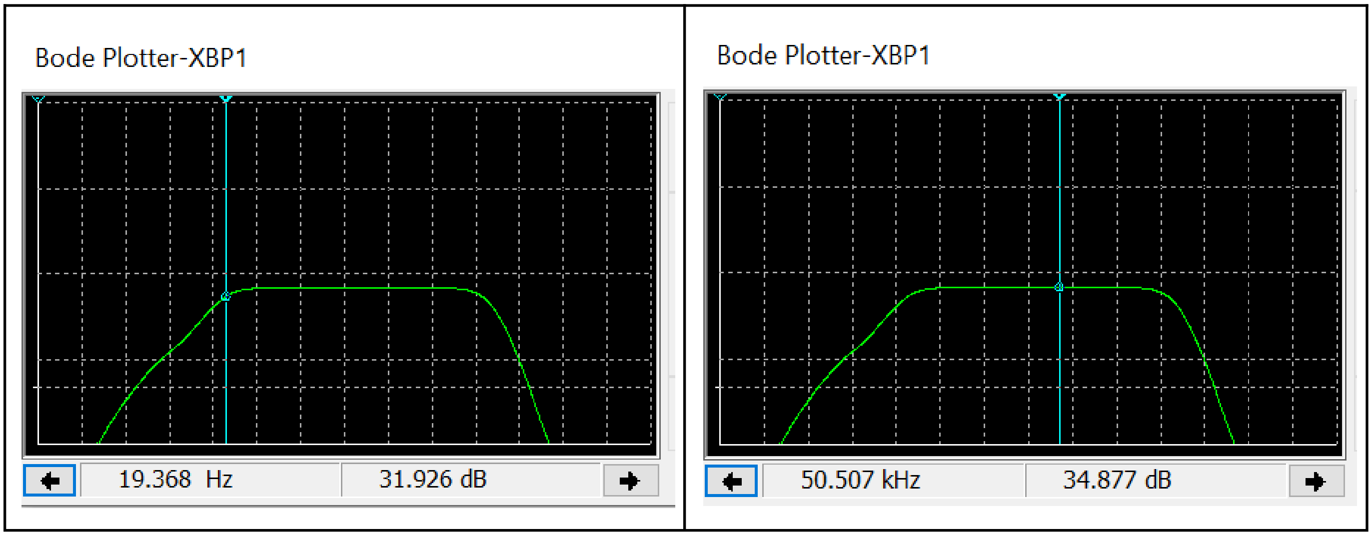


Figure 7: Frequency Response analyzer

A Bode Plotter was added and connected to the input and output ends of the circuit. The bode plots shown in the figure illustrate the frequency response of the amplifier circuit at both the input and output stages. Achieving a -3dB frequency response is a common way to define the bandwidth of an amplifier. On the left plot, the lower point is identified at approximately 19.368 Hz, which marks the lower boundary frequency range. Similarly, the right plot shows the upper point at around 50.507 kHz, which sets the upper boundary of the frequency response. resulting with -2.951dB which is effectively -3dB at around 1.6% error.

5. Conclusions and Remarks

The project has successfully demonstrated the versatility of Bipolar Junction Transistors (BJT) by designing, simulating, and calculating a transistor amplifier that meets all specified requirements.

Discrepancies

No significant discrepancies between the calculations and the results of the simulations. The DC node voltages, quiescent current, input resistance, and gain from the simulated circuits were consistent with the calculations. Slight differences are expected because theoretical calculations often employ idealized models and assumptions that simplify complex real-world phenomena, which can lead to significant discrepancies when compared with actual measurements obtained in simulation, laboratory or field conditions. Furthermore, the precision of these calculations can be further compromised by the use of varying resistance values, even within the same order of magnitude, for input and output resistance tests. This variance can influence the accuracy of the outcomes.

Real World Applications

BJT amplifiers are important to a wide array of practical applications. From amplifying delicate audio signals in consumer electronics to enhancing radio frequencies for clear communication transmissions, BJTs play a crucial role. They are key components in medical devices, magnifying bioelectric signals for diagnostics, and are essential in industrial controls for processing sensor data and driving actuators. In automotive systems, BJTs ensure smooth operation of audio and engine control units, while in computing, they are the building blocks of logic gates and memory. Their high-speed operation and power handling capabilities make BJTs indispensable in modern electronics for signal processing and amplification.

6. Appendix:

E24 Resistor Sizes

1.0 Ω	10 Ω	100 Ω	1.0 kΩ	10 kΩ	100 kΩ	1.0 MΩ
1.1 Ω	11 Ω	110 Ω	1.1 kΩ	11 kΩ	110 kΩ	1.1 MΩ
1.2 Ω	12 Ω	120 Ω	1.2 kΩ	12 kΩ	120 kΩ	1.2 MΩ
1.3 Ω	13 Ω	130 Ω	1.3 kΩ	13 kΩ	130 kΩ	1.3 MΩ
1.5 Ω	15 Ω	150 Ω	1.5 kΩ	15 kΩ	150 kΩ	1.5 MΩ
1.6 Ω	16 Ω	160 Ω	1.6 kΩ	16 kΩ	160 kΩ	1.6 MΩ
1.8 Ω	18 Ω	180 Ω	1.8 kΩ	18 kΩ	180 kΩ	1.8 MΩ
2.0 Ω	20 Ω	200 Ω	2.0 kΩ	20 kΩ	200 kΩ	2.0 MΩ
2.2 Ω	22 Ω	220 Ω	2.2 kΩ	22 kΩ	220 kΩ	2.2 MΩ
2.4 Ω	24 Ω	240 Ω	2.4 kΩ	24 kΩ	240 kΩ	2.4 MΩ
2.7 Ω	27 Ω	270 Ω	2.7 kΩ	27 kΩ	270 kΩ	2.7 MΩ
3.0 Ω	30 Ω	300 Ω	3.0 kΩ	30 kΩ	300 kΩ	3.0 MΩ
3.3 Ω	33 Ω	330 Ω	3.3 kΩ	33 kΩ	330 kΩ	3.3 MΩ
3.6 Ω	36 Ω	360 Ω	3.6 kΩ	36 kΩ	360 kΩ	3.6 MΩ
3.9 Ω	39 Ω	390 Ω	3.9 kΩ	39 kΩ	390 kΩ	3.9 MΩ
4.3 Ω	43 Ω	430 Ω	4.3 kΩ	43 kΩ	430 kΩ	4.3 MΩ
4.7 Ω	47 Ω	470 Ω	4.7 kΩ	47 kΩ	470 kΩ	4.7 MΩ
5.1 Ω	51 Ω	510 Ω	5.1 kΩ	51 kΩ	510 kΩ	5.1 MΩ
5.6 Ω	56 Ω	560 Ω	5.6 kΩ	56 kΩ	560 kΩ	5.6 MΩ
6.2 Ω	62 Ω	620 Ω	6.2 kΩ	62 kΩ	620 kΩ	6.2 MΩ
6.8 Ω	68 Ω	680 Ω	6.8 kΩ	68 kΩ	680 kΩ	6.8 MΩ
7.5 Ω	75 Ω	750 Ω	7.5 kΩ	75 kΩ	750 kΩ	7.5 MΩ
8.2 Ω	82 Ω	820 Ω	8.2 kΩ	82 kΩ	820 kΩ	8.2 MΩ
9.1 Ω	91 Ω	910 Ω	9.1 kΩ	91 kΩ	910 kΩ	9.1 MΩ