National University of Computer and Emerging Sciences, Lahore Campus				
	Course:	Computer Architecture	Course Code:	EE204
	Program:	BS(Computer Science)	Semester:	Fall 2019
	Due Date:	23-10-2019	Total Marks:	55
	Section:		Weight	3.33
	Exam:	Assignment 2	Page(s):	4
	Name:		Roll #:	

Submit hard-copy of the assignment by 23rd October 2019 during the class. Print these pages and solve questions on the printed sheet.

Question 1 **[3+4+3 marks]**

Suppose we want to design an embedded processor. We studied in our course that a processor can take different clock cycles for each instruction as is the case here. Load takes 7 cycles, store instruction take 10 and so on. The software that will be run on this processor is analyzed by using a monitoring program and following instruction mix is obtained:

Instruction	Frequency	Execution Cycles
Load	15%	10
Store	15%	7
Branch	5%	4
Add	55%	5
Divide	10%	7

a. Calculate the average CPI for the program on this processor.

You have 2 possible optimizations for this processor:

i. **Decrease Load instruction time to 5 clock cycles but this increases the clock cycle time by 10%.**
ii. **Decrease Add instruction time to 4 clock cycles but this increases the clock cycle time by 20%.**

b. Compute the new average CPI for both optimizations (I) and (II).

CPI doesn't tell the whole story in this case because clock cycle time is also changing.

c. Consider the increase in the clock cycle time and compare which of the optimizations gives better performance.

Question2: **[10 marks]**

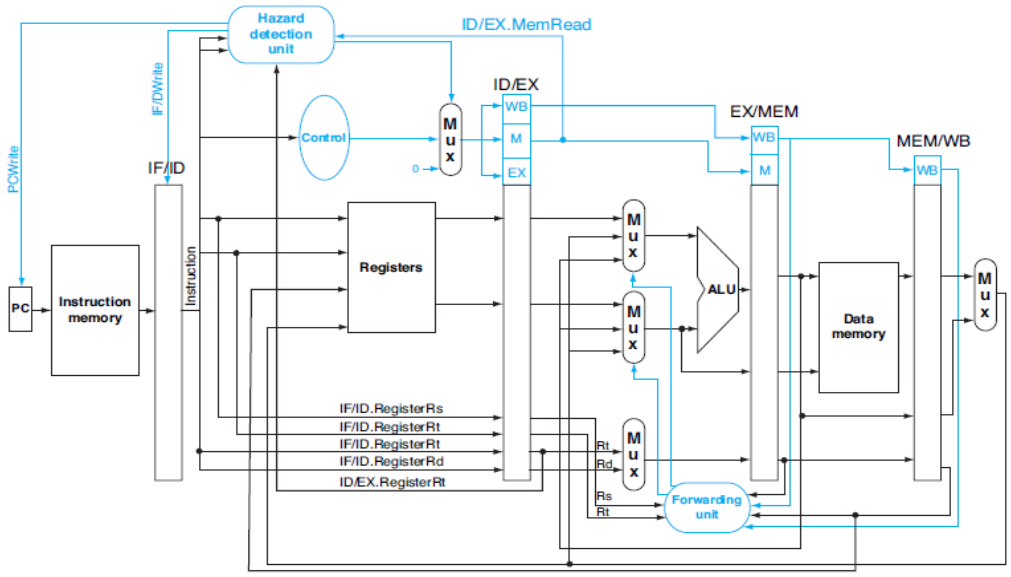
We have studied multi-cycle MIPS as shown below with datapath and control unit. Forwarding unit and Data-hazard detection unit is also implemented.

We know that if branch instruction is dependent on previous instruction then we need to add a stall even though we have EXE to EXE and MEM to EXE forwarding. Suppose a branch instruction is immediately after a load instruction as below:

Ld R1, R2, 20

beq R2, R1, 10

Analyze the situation and modify Hazard detection unit to detect this hazard and then how stall will be inserted between these two instructions. Moreover we may need to add another forwarding unit. Add this new unit and write code to perform forwarding.



Question3: **[15 marks]**

Consider the following MIPS assembly language loop. Assume that we run this code on the five stages pipelined data path.

1. **Loop: ld R1, 0(R7)**
2. **mul R1, R2, R1**
3. **ld R3, 0(R0)**
4. **add R4, R1, R3**
5. **sw R4, 0(R0)**
6. **sub R5, R5, 1**
7. **bne R5, 0, Loop**

a) Find all possible hazards in the above code. Fill the following table by writing lines and register in front of particular hazard. For example if a **WAR** hazard exist between instruction 1 and 2 due to register R0 then write **1 & 2** in column "Lines" and Register number **R0** in column "Register".

Without Forwarding			**With Forwarding**		
Hazard	**Lines**	**Register**	**Hazard**	**Lines**	**Register**
WAR					
WAW					
RAW					

b) Add stalls in the above code to remove all hazards

Without Forwarding	**With Forwarding**

Question4: **[20 marks]**

Consider the execution of the following code snippet on MIPS 5-stage pipelined processor with hazard detection and **forwarding fully implemented**. Static Branch prediction is applied which always assumes branch to be **taken**.

Instruction 1	Loop: ld R1, 20 (R2)
Instruction 2	addi R1, R1, 4
Instruction 3	add R4, R7, R3
Instruction 4	addi R5, R4, 8
Instruction 5	sw R5, 30 (R2)
Instruction 6	addi R2, R2, 4
Instruction 7	bne R2, R6, Loop

Initial values for all registers are equal to (2* register number). Register 2 contains 4, register 3 contains 6 etc. Value stored at each memory location is equal to (3* memory address).

a. Consider the execution of the above snippet in the 9^{th} Clock Cycle. Which instructions are executing at each of the pipeline stages? Fill in the following table to answer the question. Write instruction number and if a stall is at some stage then simply write **stall** for that stage**.**

Stage	Executing Instruction
IF	
ID	
EXE	
MEM	
WB	

b. In the **start** of the ***9^{th}Clock Cycle***, what will be the contents of each of the pipeline separation registers? Fill in the following tables to answer the question. You need to explicitly state names and values of ***ALL*** the variables in each register. For values that are not known to you, you can write them in terms of English phrases. For example, First entry of the IF/ID register has been filled as a guideline. You don't know the exact value of the Program Counter (PC) yet you can state that it is the value of the PC that points to instruction x plus 4 (Here you should replace "x" by the correct instruction number). All other variables, whose values can be determined, should state exact values. For example, if EXE/MEM register contains the result of the addition of instruction 5, you should state the Variable Name as "Result of ALU" and Value as "30"

IF/ID Register Contents

Variable Name	***Value***
PC	***(Program counter value of the instruction x) + 4***

EXE/MEM Register Contents

Variable Name	***Value***

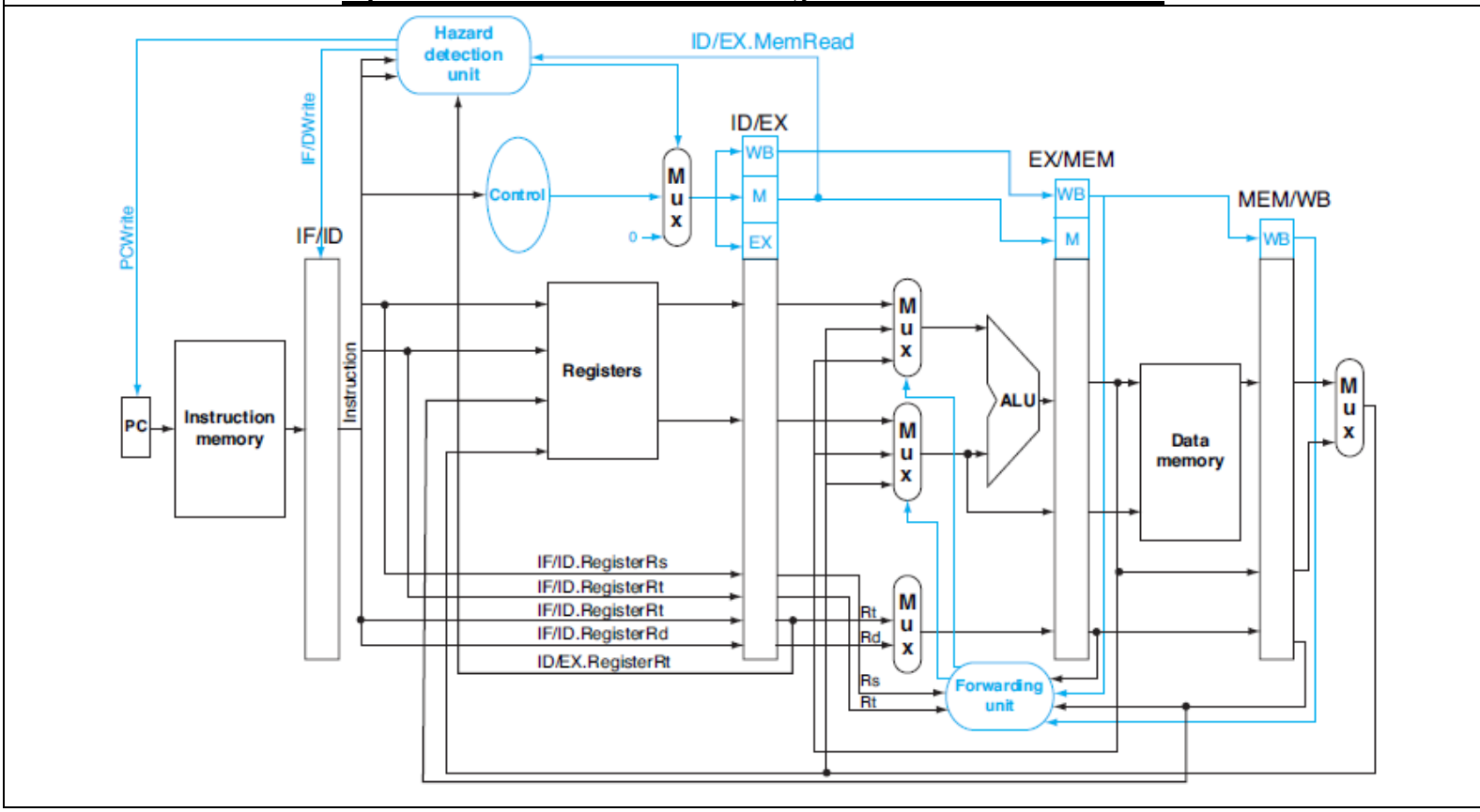
ID/EXE Register Contents

Variable Name	***Value***

MEM/WB Register Contents

Variable Name	***Value***

Pipelined Data Path with Forwarding and Hazard Detection Units



Information of control signals