	Course Name:	Computer Architecture	Course Code:	EE204
	Program:	BS(Computer Science)	Semester:	Fall 2019
	Section	All	Total Marks:	50
	Due Date:	11-09-2019	Weight	~2.5
	Exam Type:	Assignment 1	Page(s):	2

Student : Name:_____ Roll No._____ Section:_____

Question #1 [4 marks]

Prove the identity of the following Boolean equation, using algebraic manipulation:

Y + X'Z + XY' = X + Y + Z

Question #2 [8 marks]

(a) Use gates to implement following logic. (You have to show circuit diagram using symbolic representation of logic gates.)

$$X=A\overline{\overline{CD}}+\overline{E}F+\overline{AF}$$

(b) Implement the function F with a 4:1 MUX.

F = XY'Z + YZ'

Question #3 [4 marks]

Draw 4-to-16 Decoder using 3-to-8 Decoder. Draw a neat and clear block diagram.

Question #4 [8 marks]

Design a 2 - bit strange counter. This is a sequential circuit with two flip-flops and one input x. When x=0, state of the flip-flops does not change, when x=1 the state sequence is 11, 00,10,01 and repeat. Provide Excitation table and circuit diagram along with the state transition diagram for the sequential circuit.

Question #5 [8 marks]

Convert the following binary numbers to decimal:

(a) 10101001.11 (b) 11010010 (c) 1000101.101

Convert following decimal numbers to binary:

(a) 243 (b) 7685 (c) 451

Convert:

(a) 6532 to octal (b) 865 to hexadecimal

Question #6 [6 marks]

Design a circuit that has a 3-bit binary input and a single output (F) specified as follows:

- F = 0, when the input is less than $(5)_{10}$
- F = 1, otherwise

Question #7 [4 marks]

(a) Find $(35)_{10} - (72)_{10}$ using two's complement format with 8-bit numbers. Show your result in base 10.
(b) Find $(65)_{10} - (25)_{10}$ using one's complement format with 8-bit numbers. Show your result in base 10.

Question #8 [8 marks]

The outputs of four registers, R0,R1,R2 and R3 are connected through 4 to 1 line multiplexers to the input of a fifth register R5.Each register is eight bits long. The required transfers are dictated by four timing variables T0 through T3 as follows:

T0 : R5← R0

T1: R5← R1

T2: R5← R2

T3: R5← R3

The timing variables are mutually exclusive, which mean that only one variable is equal to 1 at any given time, while the other three are equal to 0. Draw a block diagram showing the hardware implementation of the register transfers. Include the connections necessary from the four timing variables to the selection inputs of the multiplexers and to the load input of register R5.