NATIONAL UNIVERSITY
of Computer & Emerging Sciences, Lahore

Department of Computer Science

EE204 – Computer Architecture

Fall 2019

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Office Location/Number: Liberty lab
Office Hours: Monday to Thursday10:00-11:00 AM

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Course Information

Program: BS **Credit Hours:** 3 **Type:** Core
Pre-requisites (if any): Digital Logic Design (EE227)
Class Meeting Time: Section C: Mon, Wed 12:30 – 1:50 PM Section D: Mon, Wed 3:30 – 4:50 PM
Section E: Tue, Thur 08:00 –09:20 AM
Class Venue: Section C, D CS-2, Section E CS-5

Course Description/Objectives/Goals:

- The main objective of this course is to provide a profound understanding of the architectural design and internal working of a microprocessor which will allow computer science students to appreciate concepts like optimization and hardware level performance issues.
- This course also introduces advanced concepts like pipelining and superscalar architecture and techniques like microprogramming.
- Multi-Core processors and issues related to multicore processors are introduced.

Course Textbook

1. M. Morris Mano, *Computer System Architecture* 3rd Edition, Prentice Hall
2. David A. Patterson, John L. Hennessy, *Computer Organization and Design: The hardware/software interface*, 4th Edition

Additional references and books related to the course:

1. Modern Processor Design: Fundamentals of Superscalar Processors by John Paul Shen and Mikko H. Lipasti

Tentative Weekly Schedule

Lect #	Topics to be covered	Readings	Assignments/ Projects?
1	Introduction to basic hardware components and devices a) Digital Logic Design Review i) Boolean Algebra ii) Combinational Circuits iii) Sequential Circuits	Text1 Chapter 1 (Excluding 1.4)	
2	Frequently used components in computers a) Adders b) Decoders c) Multiplexers d) Registers (Parallel load with shifts) e) Counters Number Systems and Binary Representations a) Integer Representations b) Floating point representation	Text1 Chapter 2 Text2 Chapter 2 (Section 2.4) Chapter 3 (Section 3.5)	
3	Logic Operations Shift Operations Combined Arithmetic, Logic and Shift Unit.	Text1 Chapter 4 (Section 4.5 – 4.7)	
4	Additional Arithmetic Operations: a) Integer Multiplication, Division b) Floating Point Operations (Addition)	Text2 Chapter 3 (Section 3.4 – 3.6)	
5	Complete ALU and FPU design Introduction to Machine Language Central processing unit in detail a) General register organization b) Addressing modes c) CISC Vs RISC	Text2 Chapter 3 (Section 3.6) Text2 Chapter 2	
6	Computer Instructions and instruction codes Introduction to the MIPS Assembly Language Instruction Types 1) Arithmetic Instructions 2) Memory Reference 3) Branch Instructions	Text2 Chapter 2 (Figure 2.32, 2.38)	Assignment 1
7	Design of a Single Cycle Machine 1) Register File 2) ALU 3) Instruction and Data Memory 4) Control Unit 5) Integration of Units	Text2 Chapter 4 (Section 4.1 – 4.4)	
8	Single Cycle Machine Design Continued Control Unit (As a hardwired combinational circuit) Exceptions and Interrupts	Text2 Chapter 4 (Section 4.1 – 4.4)	
9	Revision for Mid 1		
10	Multi-cycle implementation Motivation and Hardware Differences	Text2 Chapter 4	

		(Section 4.5)	
11	Enhancing Performance with Pipelining a) Introduction to pipelining b) A pipelined data-path c) Pipelined Control d) Shallow and deep pipelining	Text2 Chapter 4 (Section 4.5)	
12	Multi-cycle Continued Control Unit State for each instruction type Pipelined Machine: Hardware and Control Unit	Text2 Chapter 4 (Section 4.6)	
13	Multi-cycle Continued Control Unit State Machine combined Exception Handling in Multi-Cycle machine	Text2 Chapter 4 (4.6, 4.9)	
14	Data Hazards a) RAW (covered in detail) b) WAR c) WAW	Text2 Chapter 4 Section (4.7)	
15	Control Hazards a) Branch Prediction Performance of pipelined systems	Text2 Chapter 4 Section (4.8)	Assignment 2
16	Understanding Performance a) CPU Performance b) Benchmarks c) Evaluating Performance	Text2 Chapter 1 (Section 1.4)	
17	Superscalar Processors. Basic concepts of superscalar processors and instruction independence		
18	Step by step execution of instructions in superscalar processors.		
19	Code Rescheduling Loop Unrolling		
20	Revision for Mid 2		
21	Cache Design: Memory Hierarchy basic concepts Basics and Direct mapped caches	Text 2 Chapter 5 (Section 5.1, 5.2)	
22	Cache Design: Associative Caches and Miss Rates	Text 2 Chapter 5 (Section 5.2)	
23	Cache Design: Processor performance evaluation with cache / Multi-level Caches.	Text 2 Chapter 5 (Section 5.3)	
24	Virtual Memory	Text 2 Chapter 5	

		(Section 5.4)	
25	Multicores, Multiprocessors, and Clusters Multi-processor Systems basics. Multi-processor system types Parallel Processing Programs	Text 3 Chapter 7 Text 2 Chapter 7 (Section 7.1 & Section 7.2)	Assignment 3
26	Intro to memory sharing models and cache coherence problem Clusters and Other Message-Passing Multiprocessors	Text 2 Chapter 7 (Section 7.3 & 7.4)	
27	Hardware multithreading SISD,MIMD,SIMD,SPMD	Text 2 Chapter 7 (Section 7.5 & 7.6)	
28	GPUs	Text 2 Chapter 7 (Section 7.7)	
29	NVIDIA GPU architecture	Text 2 Chapter 7 (Section 7.7)	
30	Revision for Final		

(Tentative) Grading Criteria

1. 3-4 Assignments (10%)
2. 4-5 Quizzes (15%)
3. 2 Midterm Exam(s)(30%)
4. Final Exam (45%)

Course Policies

1. No makeup for missed quiz or assignment.
2. 80% attendance