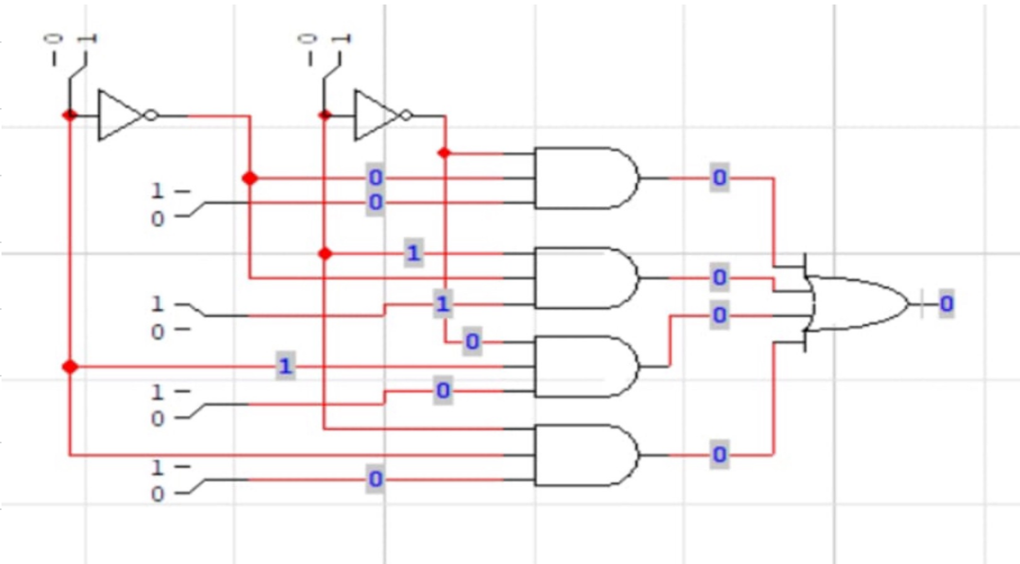
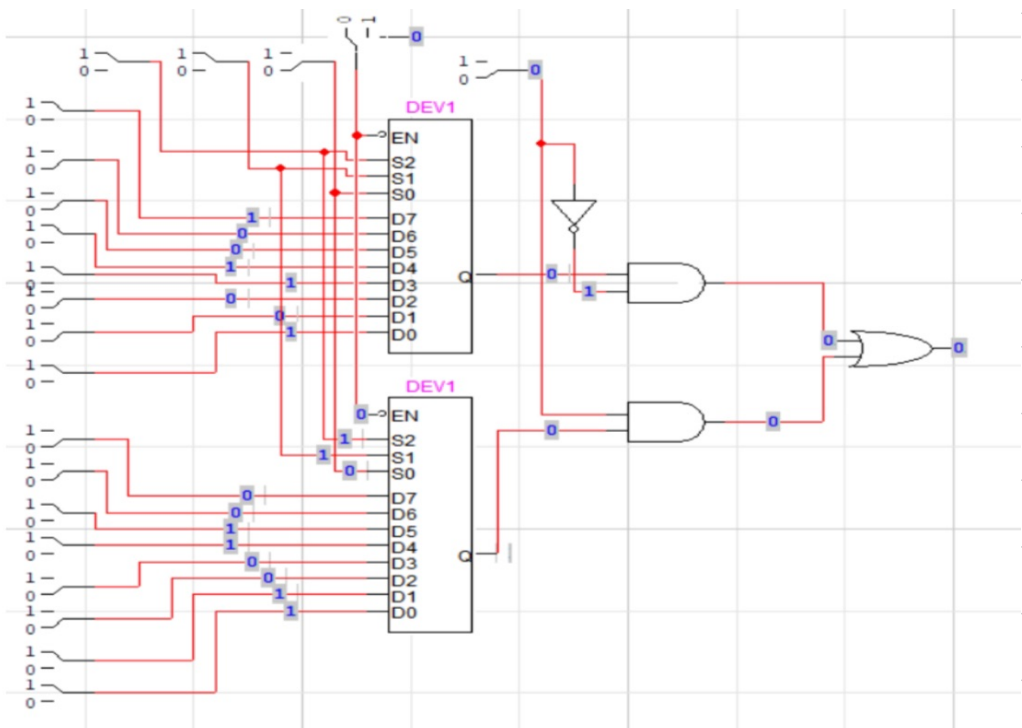
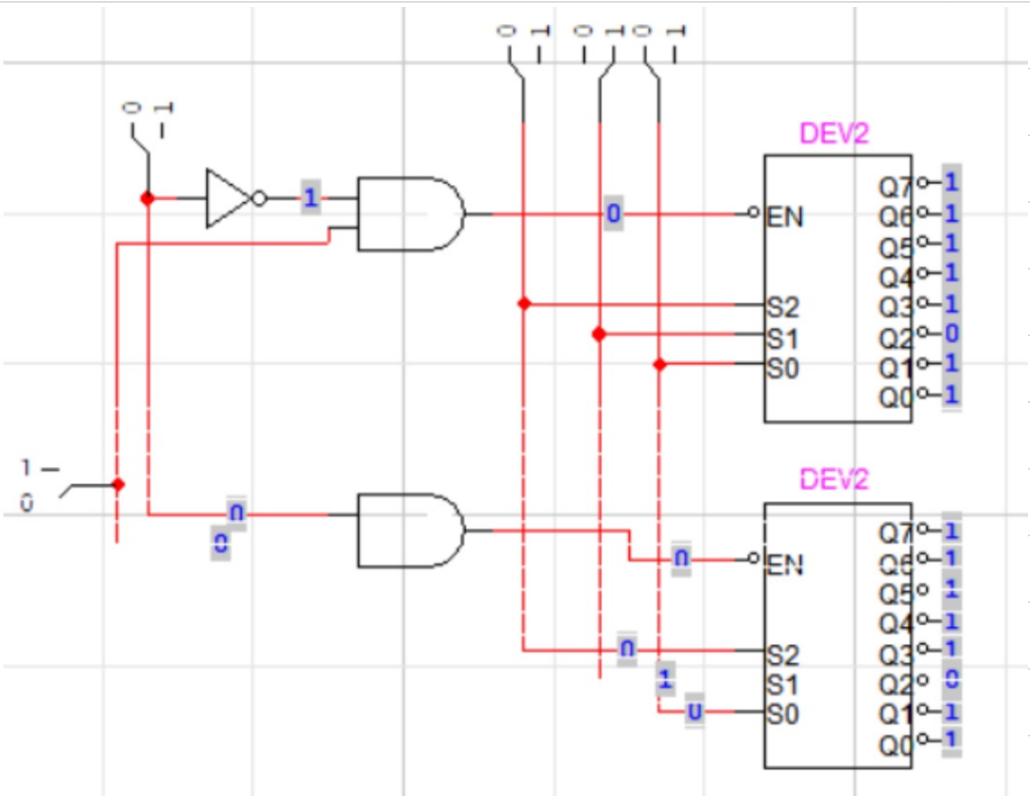
1. Design and simulate a 4:1 multiplexer using logic gates.
2. Design and simulate a 4:1 multiplexer using logic gates.



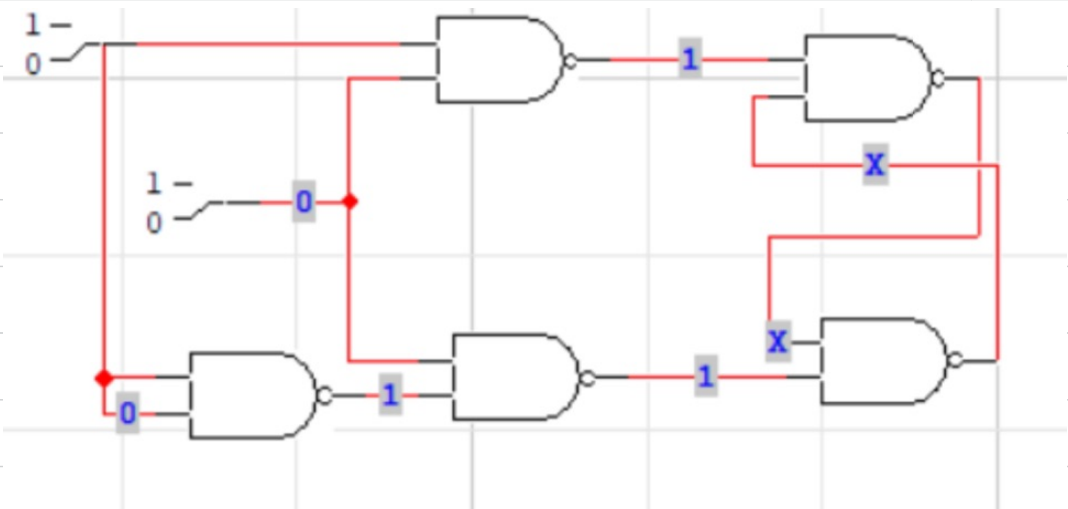
3. Create a 16-1 mux using 2 8-1 mux but one multiplexer should have a 2 bit input window while the other one should have a single bit input window. (Hint use splitters from logism)



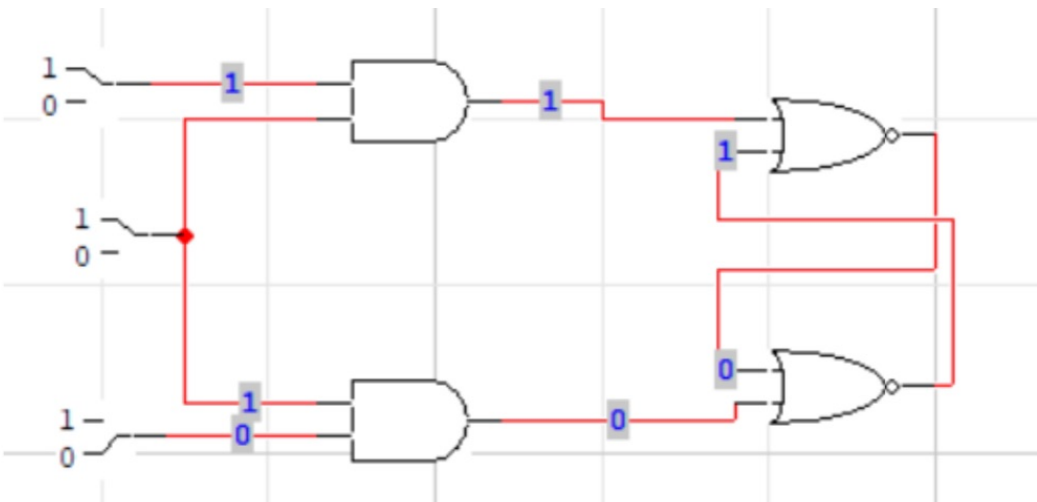
4. Create a Demux from the same Q3 circuit with 16 outputs.



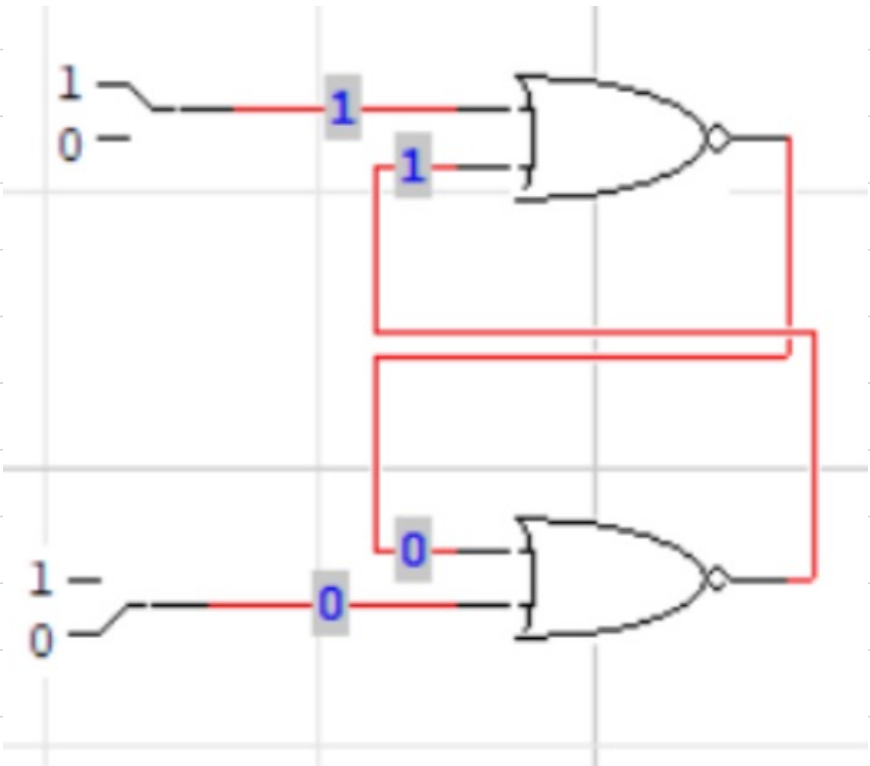
5. Design a D Latch Using NAND Gates Only



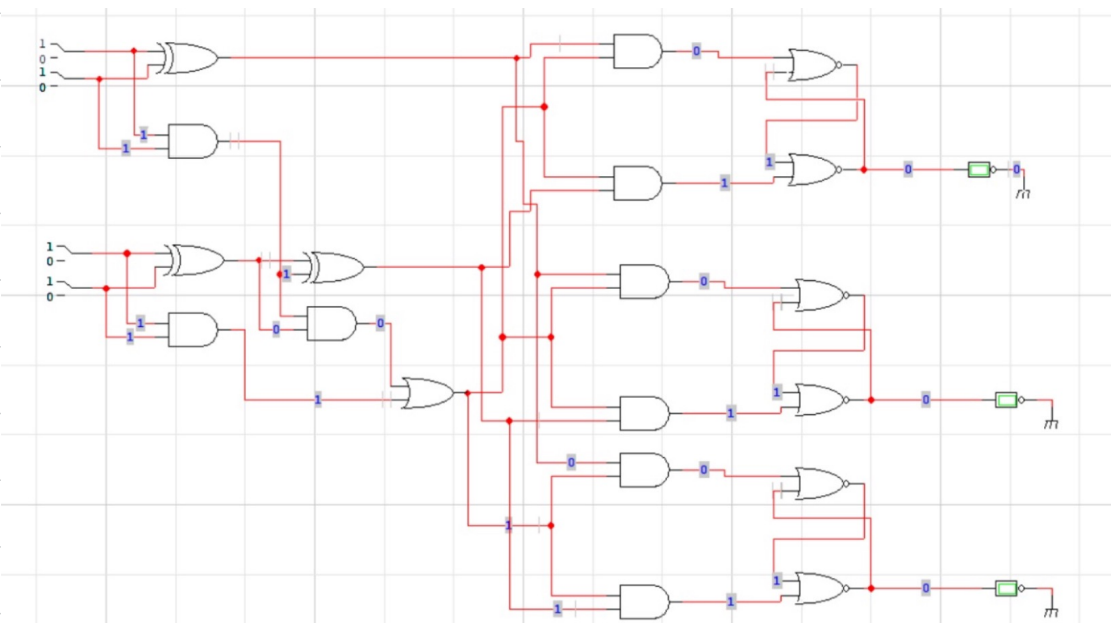
6. Design a Gated SR Latch



7. Design a SR Latch using NOR gate



8. Create a 3-bit memory using gated S-R Latches the inputs should be the output of a 2-bit adder



9. Create the same circuit with D-Latch but the output should be from a multiplier circuit