PIDELINING Pipelining is a phenomena or method using which, we will be able to run more than one instruction at the same time, on singe processor. Eik Instruction execute hore mein 5 dock cycles (yo 5 secs) leta hai ho agr do execute komi no to 10 lega. To isi cheez ko reduce terne R lije pipelining ku concept use tota hois Time taken for n instruction to = total no of phases * n x time of one clock pipeline with pipeline = [totalno.of phases + (n-1)] x fine of one dock How much the system is speedup: Speedup = (Time without pipline) / Time with piplere

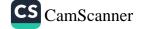
HAZARDS A hozard (conflict) is cosaled whenever there os a dependencé blu instr., 2 instr. are close enough mut overlop caused by pipliners operands involved in the dependence. Types of Hazards O Structural Hazards Data Hazards 3 Control Hazards LAWTRUCTURAL THAZARDS : , Allenpt to use same sesource (memory) from diff inst. simultaneously. - Agr do instr. same memory use bortic hai to ex instruction to subna posega q to eb wagt mein ek hi insk. memory we kr sakti hai. O: Why in MIPS Architeture there are no shuclosed Hazards ? In MIPS architecture, structural tregards

In MIPS architecture, structural hazards are minimized because the design enseurer that diff pasts of the processor don't need to use the same hasdware at the same time. Fisto. are avoided by ensuring that instruction in different stages of execution don't conflict with each other for same resources. 2) IL ATTA IT LAZARDS : Attempt to use a result before it's really. eg: Instr. depending on a sesult of a previous instr. 8 till in pipeline · Types of Skuctural Hazards: - RAW! Read After White (Flow / True dependency). RAW nazard occurs if an instruction

In tries to read on R2 before instruction Ic cosiles it. I, & R2 4 R, + R3 I 2 8 Ry 4 R2 + R3 Iz is trung to read Rz before it has been withen in memory by II.

WHAR: Write After Read (Anti Dala Dependency) This occurs when instr. Iz tries to write data before instruct I sead it. In 3 R2 = R1 + R3

In the R3 = R1 + R5 -> Ag8 ge phele execute high to R2 mein ghold value destifonyegi. MINOTEN: Write After While (Output Data Dependency). When Iz tries to write output before I, write it. I, & R2 - R, + R3 120 R2 = R4 + R5 Possible Solutions: 1 Compilation Technique: a) Insestion of nop "(no operation histo.) b) Instruct. sheduling to avoid that the corellating histraction are hos close. 5 Brein hum un instructions ko phete likholenje jinko Instruction I se kei selation this high



Sub \$2, \$1, \$3 -> nop nop nop and \$12,\$2;\$3 08 \$13; \$6,\$2 add \$14,82,82 Sw \$15, 100(BZ)

