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CHP# 9

A 5-bit conter have total 10 bit patter or 10 states.

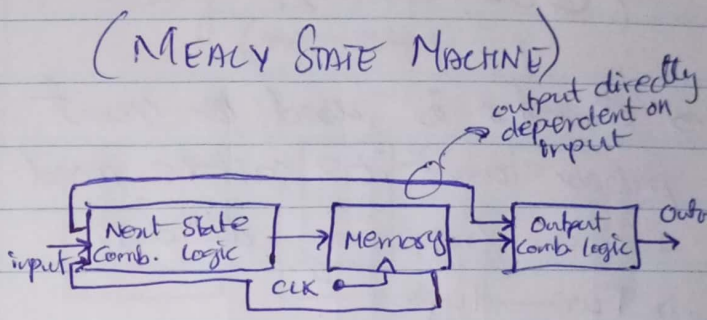
In general a Johnos Counter produce a modulus of 2n where n is the no. of stages in counter.

MEALY AND MOORE STATE MACHINES

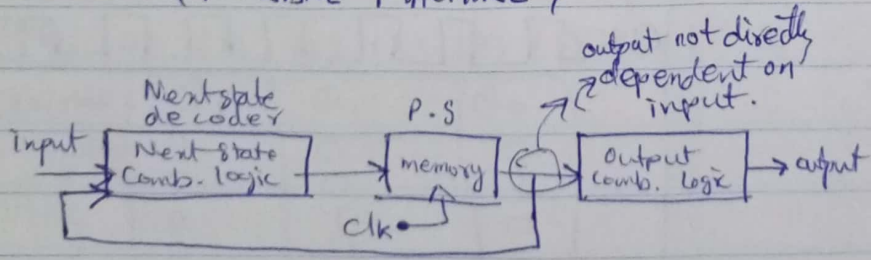
-> There are two models developed for representing synchronous sequential circuits.
- i) Moore Circuit / Moore State Machine → output function o present state only
- ii) Mealy " / Mealy State Machine → output funct. o P.S & input State

-> Difference in b/w them is in the way the output is generated.

(MEALY STATE MACHINE)



(MOORE MACHINE)



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(COUNTER)

→ Counter is used to count pulses and it can be used as a frequency divider

→ Two types
- Up Counter [Counts from 0, 1, ... N]
- Down Counter [from N, N-1, ..., 3, 2, 1, 0]

→ Classification of Counter

1) Synchronous Counter
   ↳ All memory elements (flipflop) are provided same CLK
2) Asynchronous Counter
   ↳ All memory elements (flipflop) have diff CLK pulse.

→ For n-bits counter, Max counts = 2^n
   ↳ starts from 0 to 2^n

for eg: for 3-bit counter

000
001
010
011
100
101
110
111

$2^3 = 8$ counts

• each output is representing a states

therefore there are total 8 states.

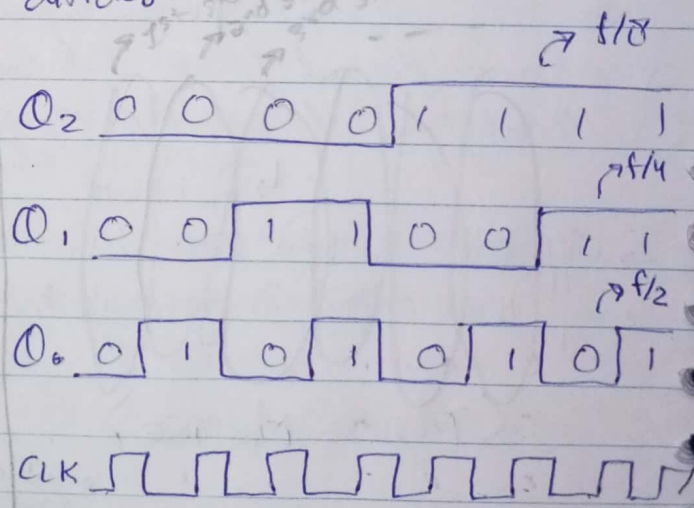
→ Up Counter will start its count from 000 — 111

→ Down " " " 111 — 000.

→ State will change in sequence

→ state " " w.r.t CLK

→ We use counter as frequency divider.



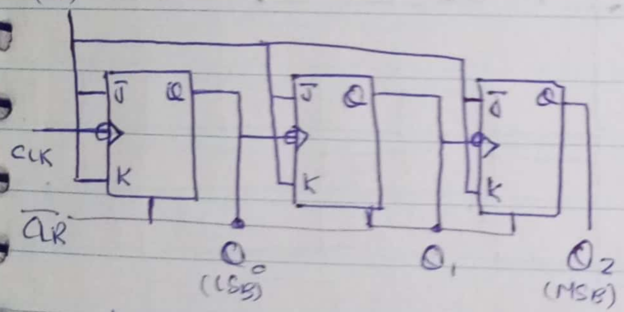
Asynchronous (Ripple) Up Counter

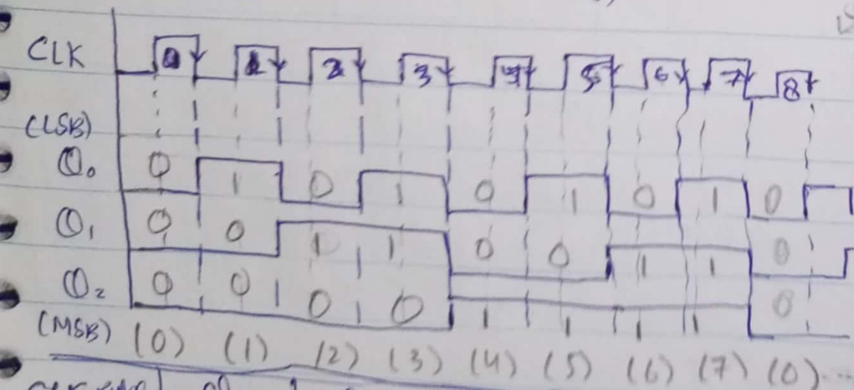
→ In asynchronous counters we donot provide same clock signal to all memory elements

(neg-edge)

— 3-bit Asynchronous —

(1) → toggle k liye sabko 1 diya hai [illegible]

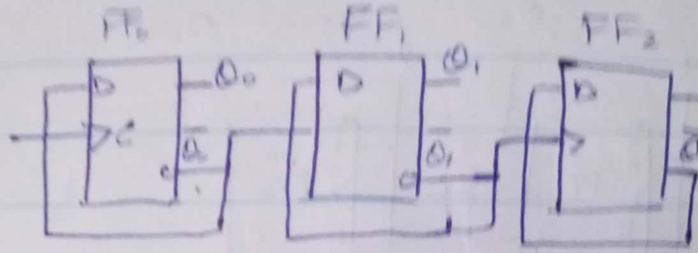


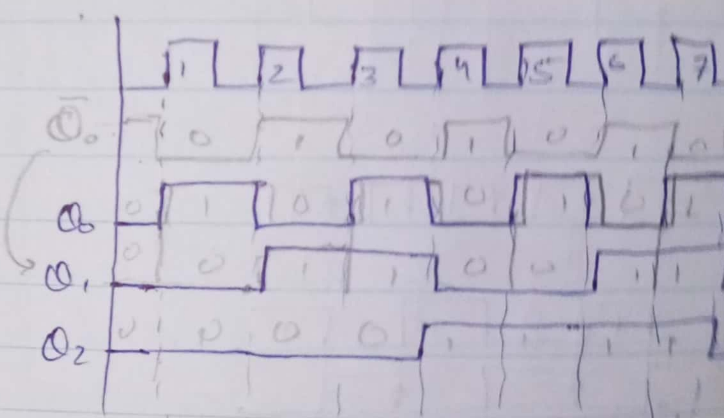


CLK pulse	Q_2	Q_1	Q_0
initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

Q_0, Q_1, Q_2 sabke output pichhle wali wave k neg-trigger par toggle krenge. [illegible]

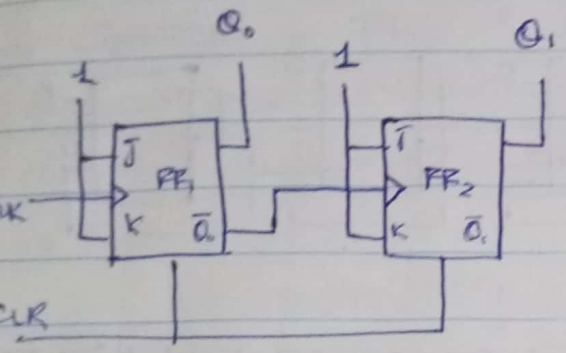
Using D-Flip Flop (+ve-edge)

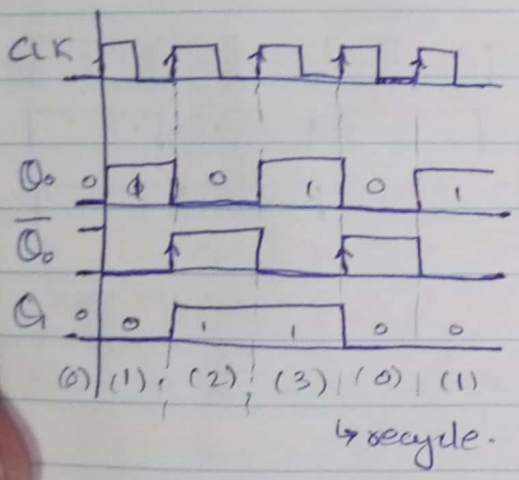




yaha par Q_0 CLK ko dekh kr toggle krega, Q_1 $\bar{Q}_0$ ko as CLK dekh kr toggle krega, Q_2 $\bar{Q}_1$ ko " " " toggle krega.

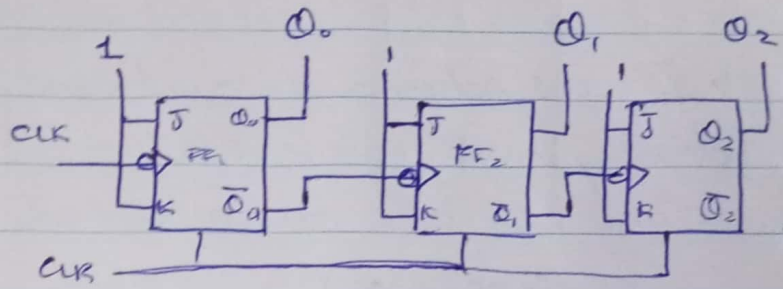
2-bit Counter (+ve edge)

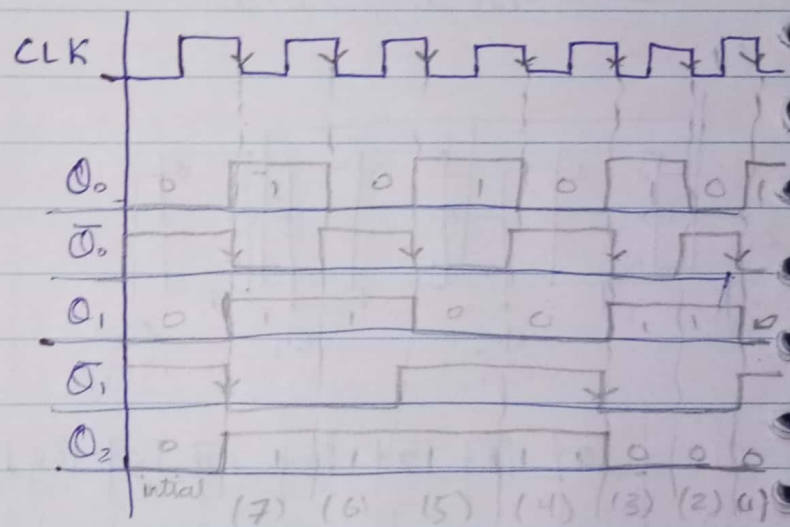




↳ recycle.

— Down Counter —
(−ve edge)





yaha par bhi Q_0 ka original CLK par toggle krega jabke Q_1 $\bar{Q}_0$ par toggle krega; or Q_2 $\bar{Q}_1$ par.

Triggering	Counter	CLK Connection
−ve	Up	Q
−ve	Down	Q'
+ve	Up	Q'
+ve	Down	Q

Syed Samooz Ali

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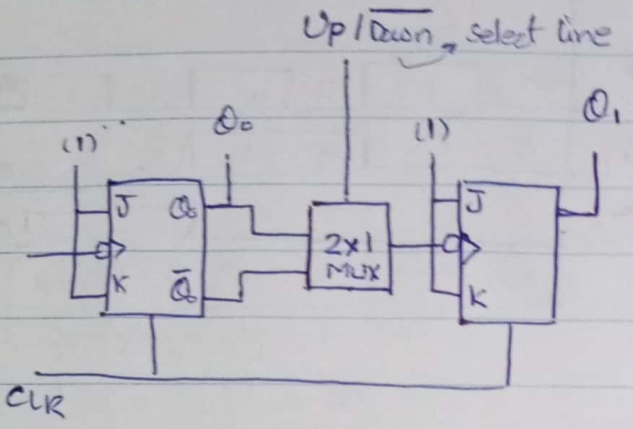
$16 \leq 10$

$2^5 > n \leq 2^n$

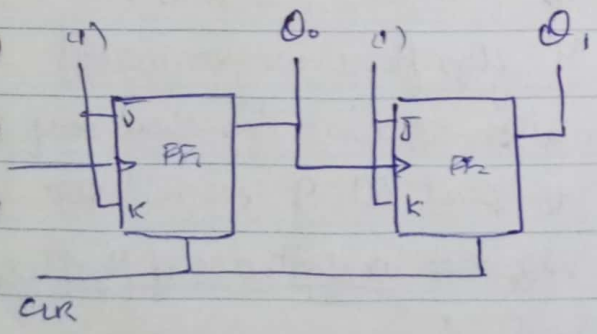
(negative edge)

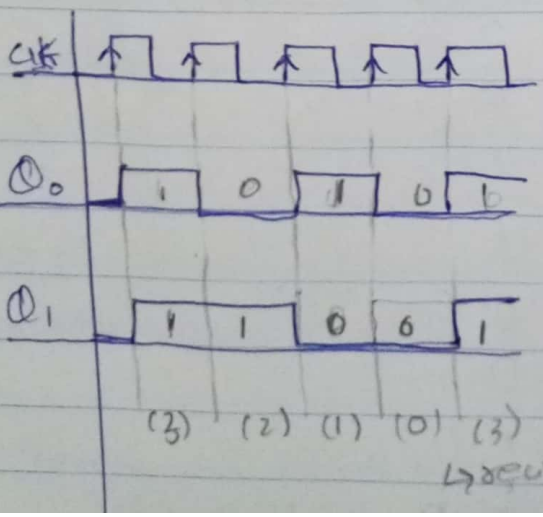
— 2 bit Up/down Counter —



agr select line 1 hoenge to UP counter agr 0 to down counter.

— 2-bit DownCounter —





→ Full modulus Counter are those which counts to it's maximum capacity. Jaise eg 2-bit counter mod will be $2^2 = 4$ → means it will count till 3.

for 4-bit → $2^4 = 16$ means it will count till 15.

Mod = 2^n.

→ We can also design a counter which counts ~~for~~ till specific number for eg MOD-10 counter which counts till 9.

— MODULO COUNTER —

→ By 2-bit counter, At max we can have MOD 4 counter

→ By 4-bit counter we have MOD 16 counter

For M-mod counter no. of flip flops required is,

$$2^n \geq M$$

n ↳ no. of flipflops; M ↳ Mod

As MOD-10 counter

$2^3 \geq 10$

$8 \geq 10$ ✗

$2^4 \geq 10$

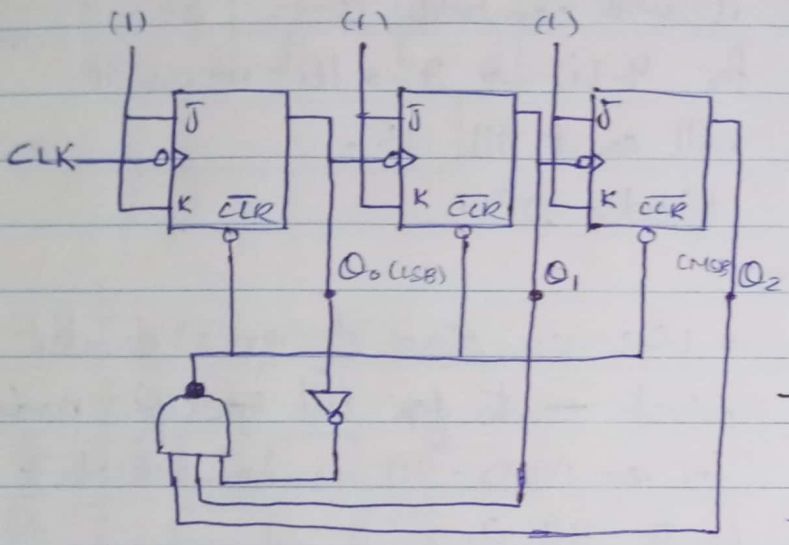
$16 > 10$ ✓

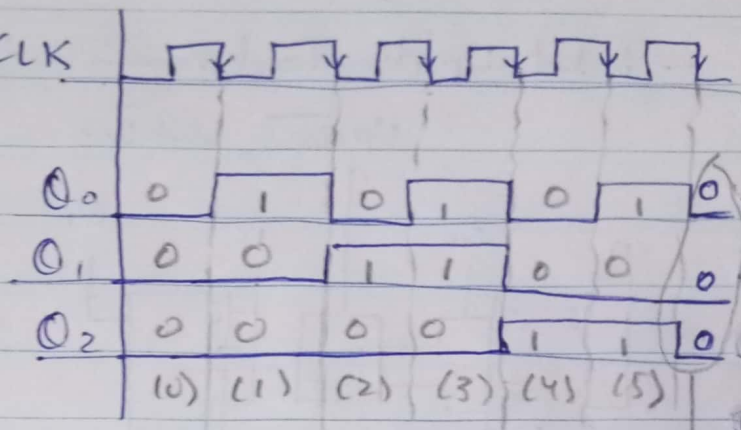
So 4 flip flops.

— MOD 6 Counter —

$2^n \geq 6$

$2^3 \geq 6$ ✓





	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0

We have to make MOD-6 Counter means from 0–5 so at 6 our counter should RESET flip flops when $Q_2=1, Q_1=1$ & $Q_0=0$ the NAND gate will give output ZERO which RESETS the counter using CLR.

— BCD / DECADE COUNTER —

→ It counts from 0 to 9

→ it means MOD-10 counter

$2^3 \geq 10$ ×, $2^4 \geq 10$ ✓

→ So 4 flip flops are required!

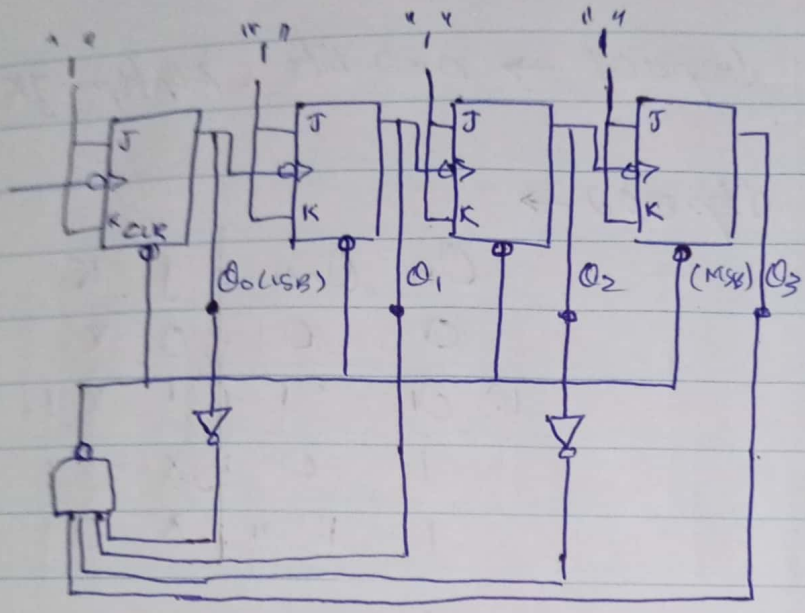
→ We can also calculate this thru no. of bits as to count till 9 we will req. 4-bits so no. of bits = no. of flip flops

	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0 ✗

recycles back to 0000.

SYNCHRONOUS COUNTERS

— 2-Bit SYNCHRONOUS — COUNTER (JK Flip flop)



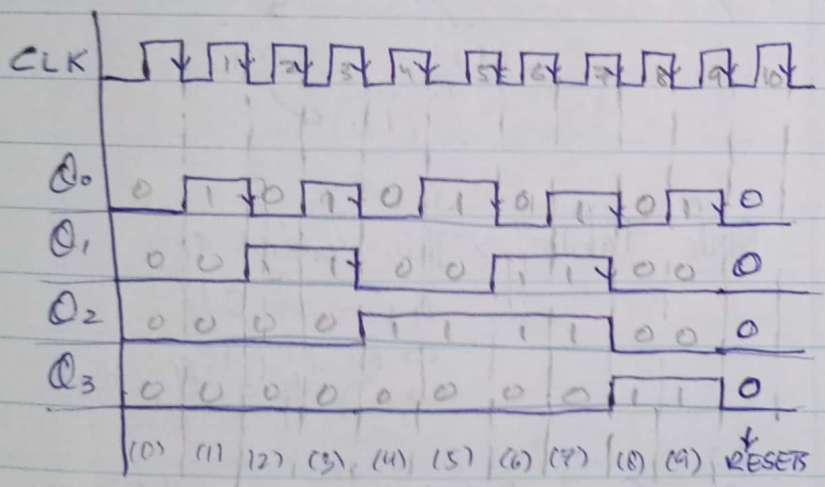
Step#01: Identify no of bits & flip flop

Step#02: Write excitation table of flip flop

Step#03: Make State diagram & state table

Step#04: Solve boolean expression

Step#5: Make Circuit



EXCITATION TABLE

[JK Flip Flop]

(Characteristic Table)

Q_n	J	K	Q_{n+1}	
0	0	0	0	
0	0	1	0	
0	1	0	1	
0	1	1	1	→ complement of Q_n as J=K=1
1	0	0	1	
1	0	1	0	
1	1	0	1	
1	1	1	0	

→ For n-bit counter maximum propagation delay is $n \times t_{pd}$

↳ no. of counters

→ Max Frequency of CLK = $1/n \times t_{pd}$

→ Max Frequency $\leq \frac{1}{n \times t_{pd}}$

[by using this condition we can still se decoding errors so we use a decoders and provide the CLK signal to enable of decoder to get correct

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using characteristic table.

Excitation Table:-

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

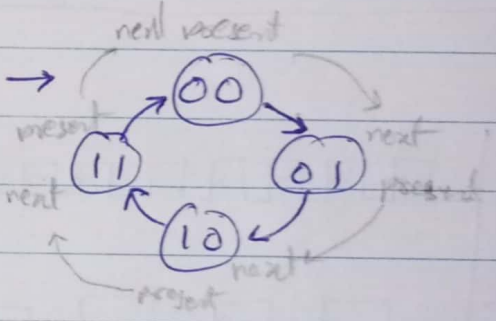
Q_n or Q_{n+1} 0 to zero
change to 1
J=0 and K par 1
depend which change so X → don't care.

Step#01 → n=2 bits, Flip flop = JK

Step#02 →

Q_n	Q_{n+1}	$\bar{J}$	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step#03 →



D - Flip Flop

Characteristic Table

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Excitation Table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

State Table → This consist of
↳ Present State
↳ Next State
↳ Inputs of flip flop
by using State diagram

Present Q_1	Present Q_0	next state Q_1^+	next state Q_0^+	$\bar{J}_1$	K_1	$\bar{J}_0$	K_0
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1

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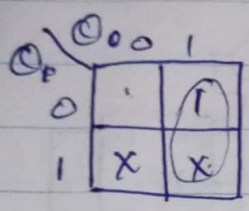
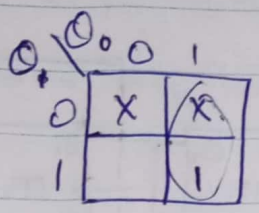
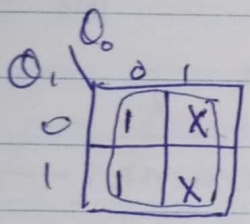
Step#04 → Boolean expression for J_1, K_1, J_0, K_0 — 3-bit Synchronous Counter



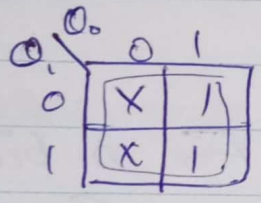
$J_1 = Q_1$



$K_1 = Q_0$



$J_0 = 1$

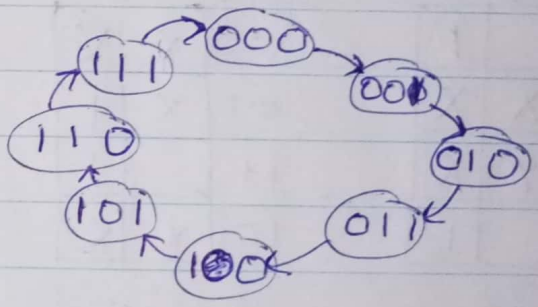


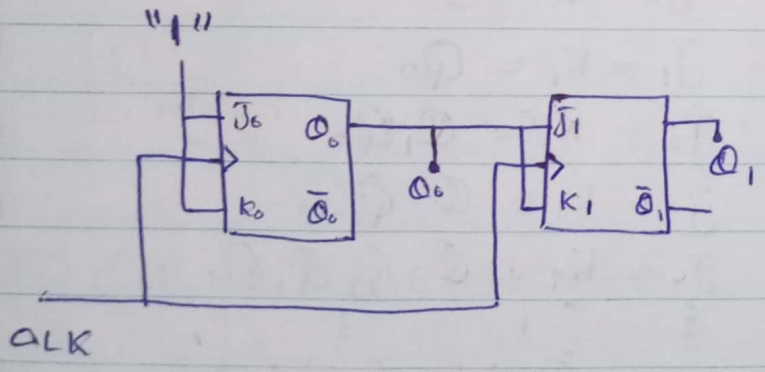
$K_0 = 1$

→ no. of flip flops = 3 (JK flip flops)

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

→





→ Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	J_2 K_2	J_1 K_1	J_0 K_0
0	0	0	0	0	1	0 X	0 X	1 X
0	0	1	0	1	0	0 X	1 X	X 1
0	1	0	0	1	1	0 X	X 0	1 X
0	1	1	1	0	0	1 X	X 1	X 1
1	0	0	1	0	1	X 0	0 X	1 X
1	0	1	1	1	0	X 0	1 X	X 1
1	1	0	1	1	1	X 0	X 0	1 X
1	1	1	0	0	0	X 1	X 1	X 1

For J_2:

Q_2Q_1 \ Q_0	0	1
00	0	
01		1
11	X	X
10	X	X

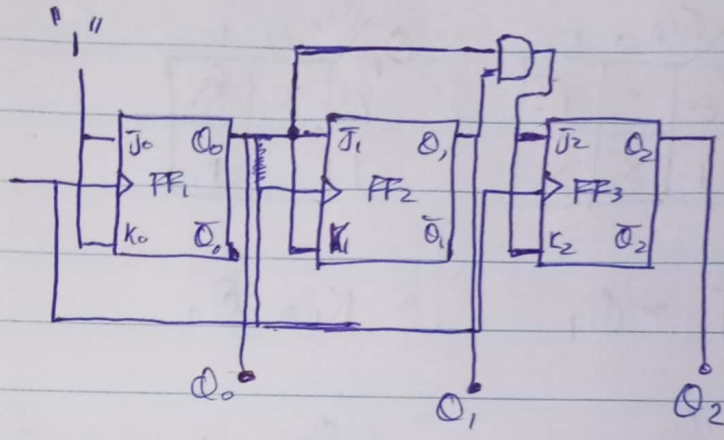
$J_2 = Q_1Q_0$

For K_2:

Q_2Q_1 \ Q_0	0	1
00	X	X
01	X	X
11		1
10		

$K_2 = Q_1Q_0$

→ Construction:



For J_1:

Q_2Q_1 \ Q_0	0	1
00		1
01	X	X
11	X	X
10		1

$J_1 = Q_0$

For K_1:

Q_2Q_1 \ Q_0	0	1
00	X	X
01	X	1
11		1
10	X	X

$K_1 = Q_0$

— For n-bit Synchronous Counter.

$J_0 = K_0 = 1$

$J_1 = K_1 = Q_0$

$J_2 = K_2 = Q_1Q_0$

$J_3 = K_3 = Q_2Q_1Q_0$

$J_4 = K_4 = Q_3Q_2Q_1Q_0$

For J_0:

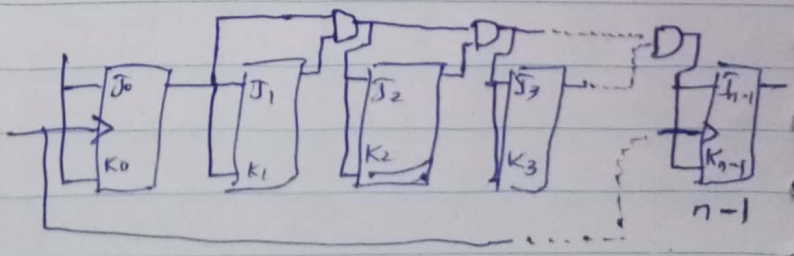
Q_2Q_1 \ Q_0	0	1
00	1	X
01	1	X
11	1	X
10	1	X

$J_0 = 1$

For K_0:

Q_2Q_1 \ Q_0	0	1
00	X	1
01	X	1
11	X	1
10	X	1

$K_0 = 1$



n-bit Synchronous Counter

→ Max propagation delay

$T_{pd}(FF) + (n-2)T_{pd}(AND\ gate)$

↳ n = no. of flip

Max CLK frequency = $\frac{1}{\text{Max } t_{pd}}$

For J_2:

Q_2Q_1 \ Q_0	0	1
00	1	
01	-	
11	X	X
10	X	X

$J_2 = \bar{Q}_1\bar{Q}_0$

For K_2

Q_2Q_1 \ Q_0	0	1
00	X	X
01	1	X
11		
10	1	

$K_2 = \bar{Q}_1\bar{Q}_0$

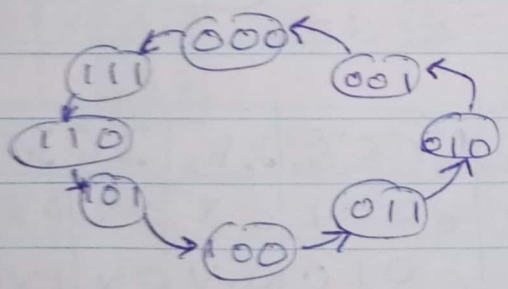
Baaqi bhi isi tarha nikal jayega K-map se

3bit

— Down Counter —

→ Excitation table previous one.

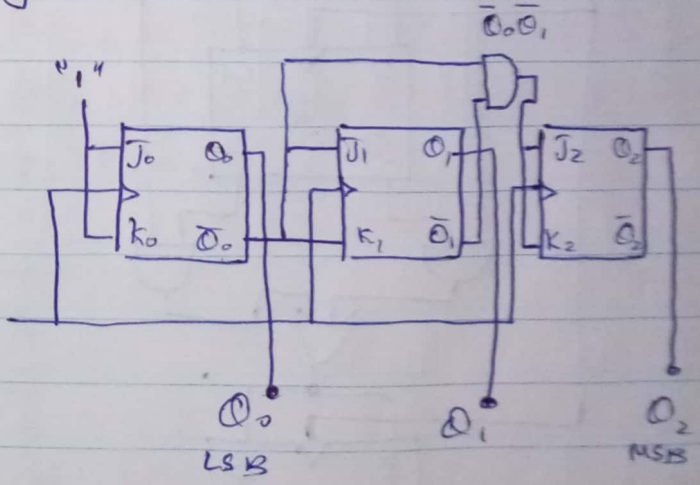
→



Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	$\bar{J}_2K_2$		$\bar{J}_1K_1$		$\bar{J}_0K_0$	
1	1	1	1	1	0	X	0	X	0	X	1
1	1	0	1	0	1	X	0	X	1	1	X
1	0	1	1	0	0	X	0	0	X	X	1
1	0	0	0	1	1	X	1	1	X	1	X
0	1	1	0	1	0	0	X	X	0	X	1
0	1	0	0	0	1	0	X	X	1	1	X
0	0	1	0	0	0	0	X	0	X	X	1
0	0	0	1	1	1	1	X	1	X	1	X

$\bar{J}_1 = K_1 = \bar{Q}_0$

$J_0 = K_0 = 1$



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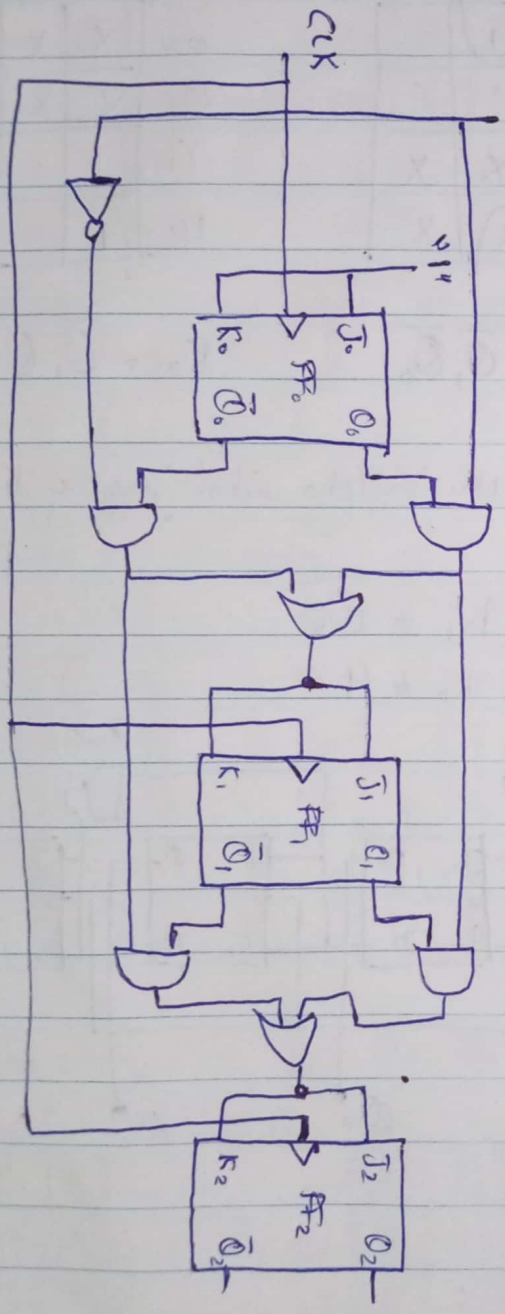
→ Bidirectional counter

3-bit Up/down Synchronous Counter



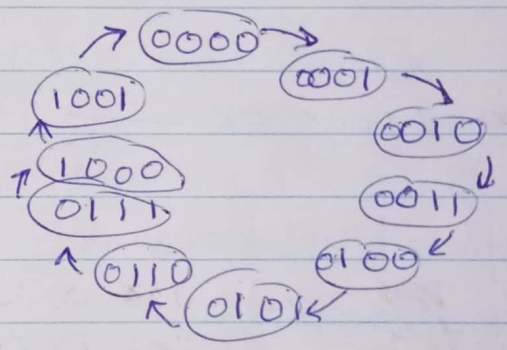
Job UP/down = 0 than reache every gates challenge.

Job UP/down = 1 than upper wale gates challenge

→ no. of flip flops = 4

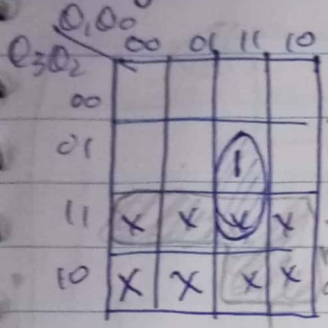
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

→

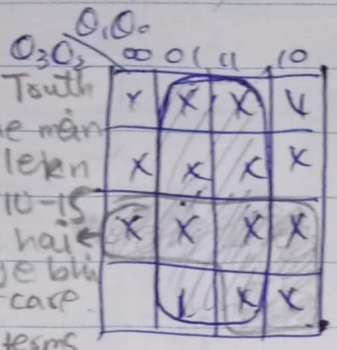


$Q_3 Q_2 Q_1 Q_0$	$Q_3^+ Q_2^+ Q_1^+ Q_0^+$	$J_3 K_3$	$J_2 K_2$	$J_1 K_1$	$J_0 K_0$
0 0 0 0	0 0 0 1	0 X	0 X	0 X	1 X
0 0 0 1	0 0 1 0	0 X	0 X	1 X	X 1
0 0 1 0	0 0 1 1	0 X	0 X	X 0	1 X
0 0 1 1	0 1 0 0	0 X	1 X	X 1	X 1
0 1 0 0	0 1 0 1	0 X	X 0	0 X	1 X
0 1 0 1	0 1 1 0	0 X	X 0	1 X	X 1
0 1 1 0	0 1 1 1	0 X	X 0	X 0	1 X
0 1 1 1	1 0 0 0	1 X	X 1	X 1	X 1
1 0 0 0	1 0 0 1	X 0	0 X	0 X	1 X
1 0 0 1	0 0 0 0	X 1	0 X	0 X	X 1

For J_3:



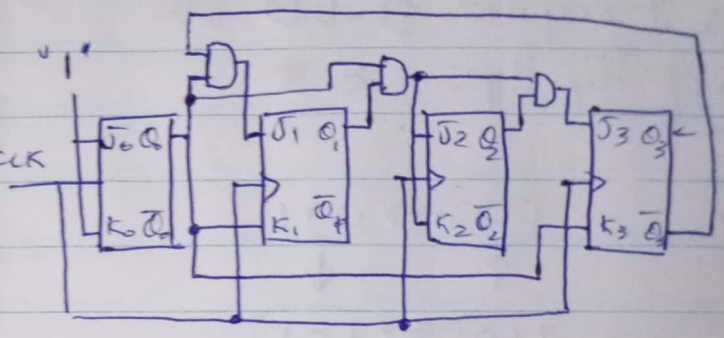
For K_3:



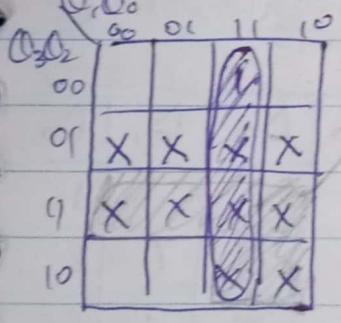
ye Truth table mein nhi leken ye 10-15 take hain is ye bhi don't care terms hain.

$J_3 = Q_2Q_1Q_0$ $K_3 = Q_0$

$J_0 = K_0 = 1$

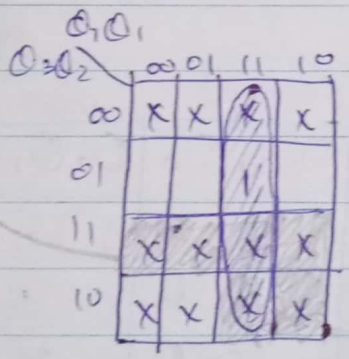


For J_2:



$J_2 = Q_1Q_0$

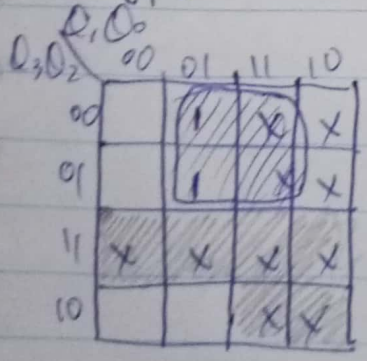
For K_2:



$K_2 = Q_1Q_0$

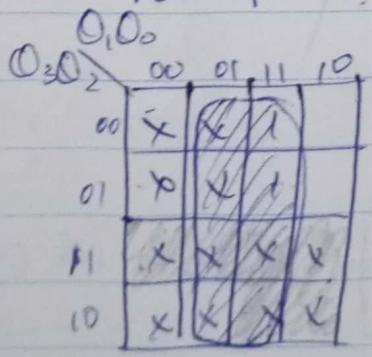
→ If counter is in one of the unused state & if it comes back to one of the valid states after one or more clocks then it is self correcting & no modification is required!

For J_1:



$J_1 = \bar{Q}_3 Q_0$

For K_1:



$K_1 = Q_0$

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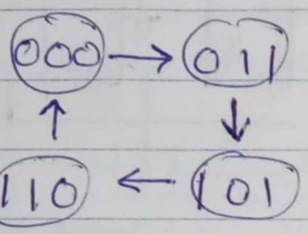
Sequence Counter

0, 3, 5, 6, 0

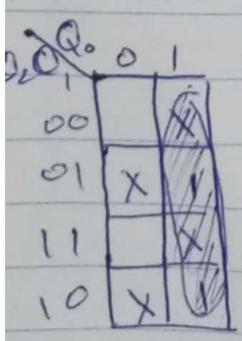
as it requires 3-bits so
no. of flip flops = 3

→


↳ remaining states will be don't care terms.

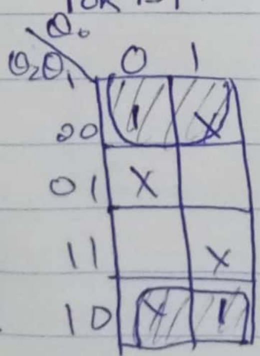
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	D_2	D_1	D_0
0	0	0	0	1	1	0	1	1
0	1	1	1	0	1	1	0	1
1	0	1	1	1	0	1	1	0
1	1	0	0	0	0	0	0	0

For D_2:



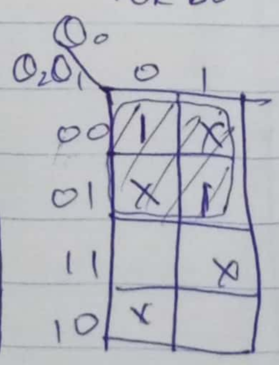
$D_2 = Q_0$

For D_1:



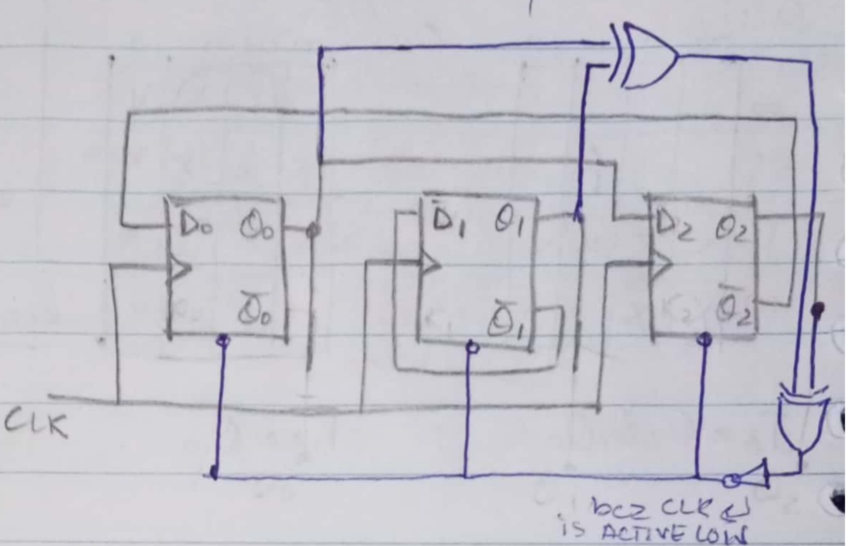
$D_1 = \overline{Q}_1$

For D_0:



$D_0 = \overline{Q}_2$

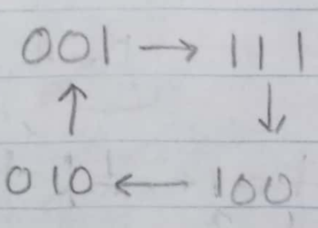
→ Construction:- after modification



Step#06: Check for lockout conditi

inki values hum apni eqn se dekh kr likhenge

present			next					
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	D_2	D_1	D_0
0	0	1	1	1	1	1	1	1
0	1	0	0	0	1	0	0	1
1	0	0	0	1	0	0	1	0
1	1	1	1	0	0	1	0	0



phele present state & D_2, D_1, D_0 likhenge phir unkei madad se next state.

It is not self correcting!

Step 2 & 3: Elimination of lockout each by

→ Generate the reset pulse when counter goes in "invalid State"

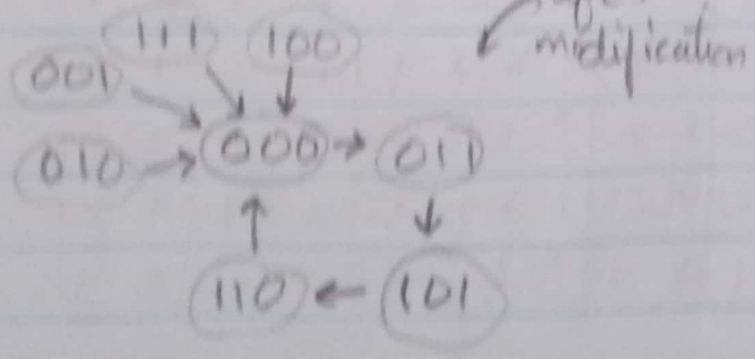
→ The RESET input should bring the counter in any one of the valid State.

Invalid states

Q_2	Q_1	Q_0	R → Reset
0	0	1	1
0	1	0	1
1	0	0	1
1	1	1	1

Q_2 \ Q_1Q_0	00	01	11	10
1		1		1
0	1		1	

$$\overline{R} = Q_2 \oplus Q_1 \odot Q_0$$



after modification

▲ State diagram!