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CHP#07

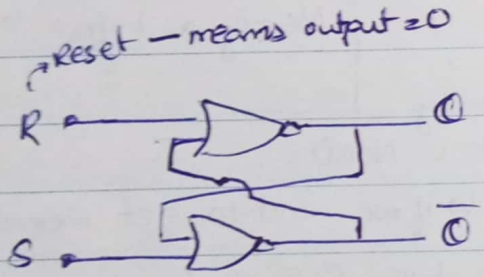
jaha input 1 hoga waha se start krenge

(SR LATCH)

→ in sequential circuits we have a memory element which is used to store previous output.

→ The basic storage element is called LATCH.

SR-LATCH can be two types
1. NOR 2. NAND



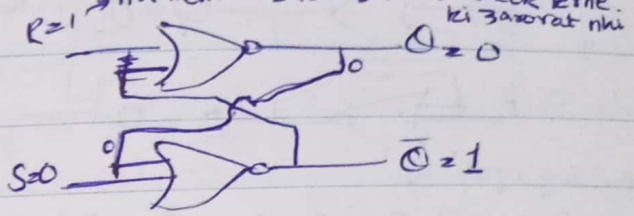
q/ S = 1 then output Q = 1
q/ R = 1 " " Q = 0

T.T for NOR gate

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

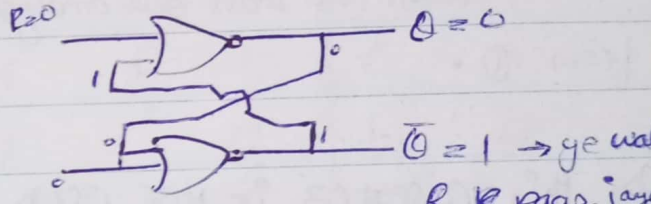
→ when A is 1 than X is always 0 no need to check B.

Case #01: S = 0 , R = 1 then Q = 0, $\bar{Q}$ = 1



R=1 → nor mein ek 1 hoi to doosra check krne ki zaroorat nhi

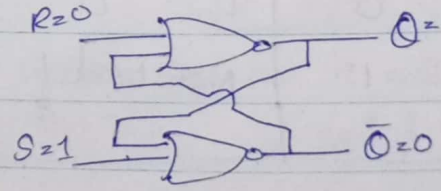
q/ we remove input than output will remain same
↳ i.e S=0 & R=0



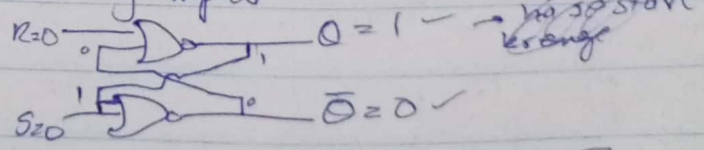
→ ye wala R k paas jayega to 0,1 = 0 or phir Q wala S k pass to 0,0 = 1 output remains same.

S=0, R=0, Q=0 & $\bar{Q}$ = 1
↳ Memory

Case #02: S = 1, R = 0, Q = & $\bar{Q}$ =



removing input.



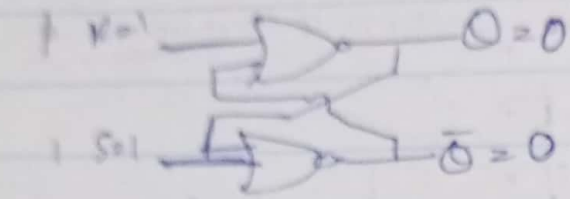
→ ha ye start krenge

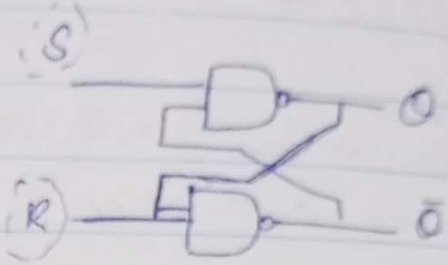
S=0, R=0, Q=1, $\bar{Q}$=0
↳ Memory

Case #03: S=1, R=1, Q=0, $\bar{Q}$=0 —(Using NAND)—

Q=$\bar{Q}$ (X)

Not True





remaining inputs ⇒

S=0, R=0, Q=0 & $\bar{Q}$=1

ye jab ayega jab $\bar{Q}$ se start karein

S=0, R=0, Q=1, & $\bar{Q}$=0

when we start our analysis from Q.

So this case #03 is NOT USED in SR LATCH! as it is not storing the previous values.

S	R	Q	$\bar{Q}$
0	0	Not Used!	
0	1	1	0
1	0	0	1
1	1	Memory as before	

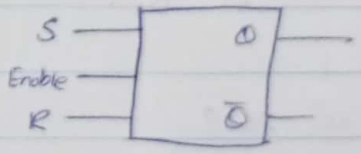
↳ memory state in NAND

↳ if we want to get memory we will set both S & R to 1.

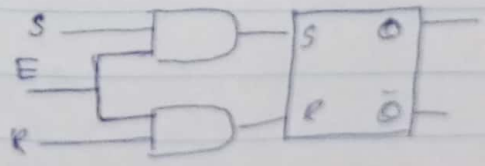
S	R	Q	$\bar{Q}$
0	0	Memory (as before)	
0	1	0	1
1	0	1	0
1	1	Not used!	

memory state in NOR

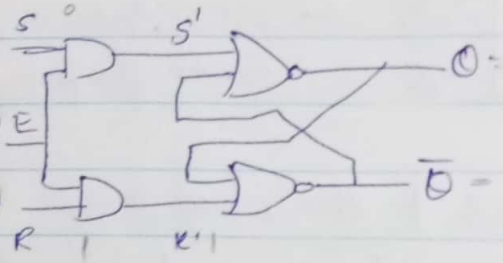
—(GATED SR-LATCH)—



or



The gate SR latch control the input states means when E=1 only then Q & $\bar{Q}$ are changed else if E=0 then S & R also bcms 0 & memory state is availed.

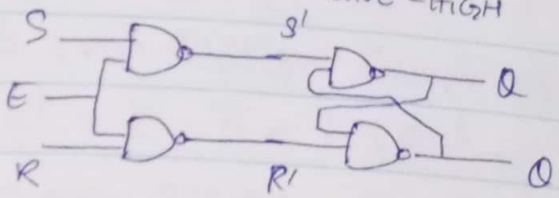


R' & S' are normal inputs to latch and S & R are external inputs which will be used to change the memory.

E	S	R	Q	$\bar{Q}$
0	X	X	Memory	
1	0	0	Memory	
1	0	1	0	1
1	1	0	1	0
1	1	1		

Using NAND Gates

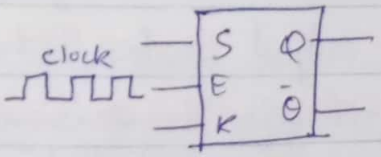
this is ACTIVE-HIGH



E	S	R	Q	Q'
0	X	X	Memory State	
1	0	0	Memory State	
1	0	1	0	1
1	1	0	1	0
1	1	1	0	0

→ Not Used!

We can provide clock to enable to control the output states. As SR latch immediatly responds to inputs so Q & $\bar{Q}$ are change therefore we use clock.



When clock is ~~High~~ low it will give memory. Clock is like a control input.

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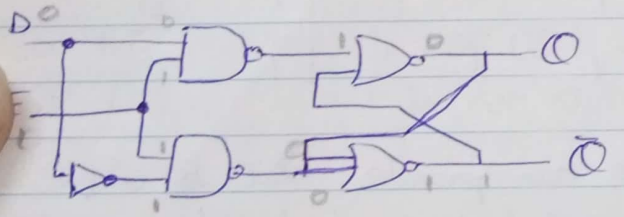
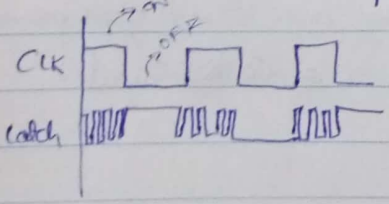
(GATED D-LATCH)

Only two inputs Enable (EN) & Data input (D).

D	EN	Q	$\bar{Q}$
0	0	Memory State	
0	1	0	1
1	0	1	0
1	1	Not used!	

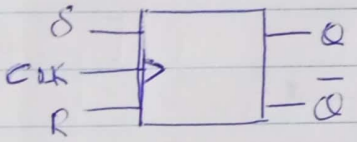


→ Gated SR-latch ka ye disadvantage hai k jab clock ON hogi to LATCH ki output States change hosakti hai. Therefor it is not preferred in sequential circuits



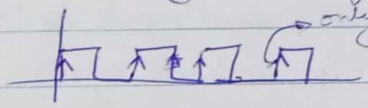
G-R FLIP-FLOP

It responds to input only on flip-flop transitions.



→ +ve edge triger flipflop

it will responds to the input only at the rising edge of the clock



CLK	S	R	Q_n present state	Q_{n+1} Next State	State
0	x	x	0	0	No change
			1	1	
↑	0	0	0	0	No change
			1	1	
↑	0	1	0	0	RESET
			1	0	
↑	1	0	0	1	SET
			1	1	
↑	1	1	0	x	Not used!
			1	x	

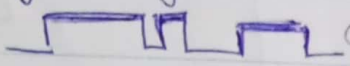
jab S=0, R=1 ho to irrespective of present state the next state will be 0 0.

0	0	Not used
0	1	1 0
1	0	0 1
1	1	Mem

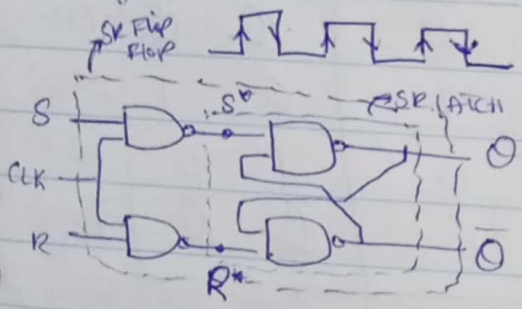
With NAND

Difference b/w Latch & Flip Flop

Latch mein ~~inputs~~ S & R ko control krne k liye enable input hota hai ~~jo~~ clock nhi hota.
S it is sensitive to level trigger.
means States are only changed when enable is high.



Jab enable ki jaga CLOCK use hoga or ye edge triggering k liye sensitive ho.



$S^* = (\overline{S \cdot CLK}) = \bar{S} + \overline{CLK}$

$R^* = (\overline{R \cdot CLK}) = \bar{R} + \overline{CLK}$

CLK	S	R	Q	$\bar{Q}$
0	X	X	Memory	
1	0	0	Memory	
1	0	1	0	1
1	1	0	1	0
1	1	1	Not used!	

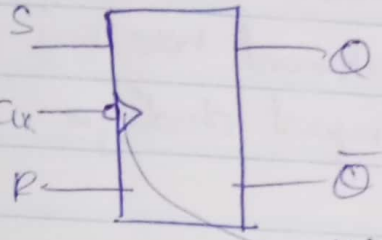
When CLK = 0

$S^* = \bar{S} + \bar{Q} = 1$

↳ iski value kuch bhi ho ans 1 hi ayega

$R^* = \bar{R} + \bar{Q} = 1$

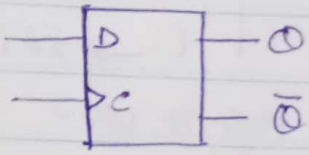
~~In NAND SR latch~~ we will get memory



→ ve edge triggered flip flop.

→ this is called dynamic input indicator

D - FLIP FLOP



The D input is a synchronous input bcz data on the input are transferred to the flip flop's output only on the triggering edge of the clock pulse.

→ The flip flop cannot change the state except on the triggering edge of a CLK pulse.

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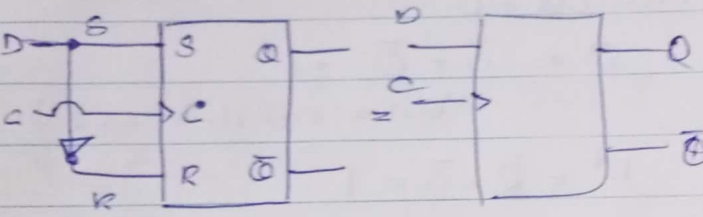
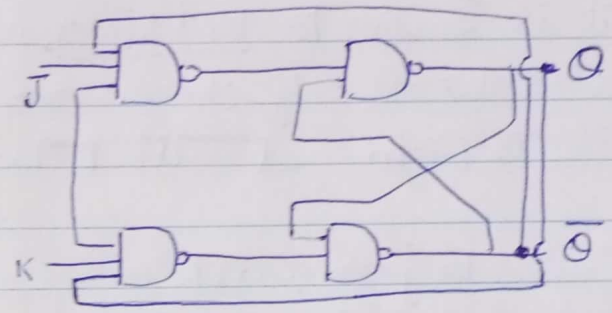
J-K Flip Flop



It can be used to get outputs on Not used states.

S $\bar{R}$ flip mein hamesha S or R ek doosre k complement hote hai to humne ek hi input dediya 2 k bajaye.



CLK	D	Q
1 or 0	X	Memory
↑	0	0 → RESET
↑	1	1 → SET

↑ means from High to Low

neg triggering k liye bhi same hi hoga.

CLK	J	K	Q	$\bar{Q}$	
↑	0	0	Q_0	$\bar{Q}_0$	Memory
↑	0	1	0	1	RESET
↑	1	0	1	0	SET
↑	1	1	$\bar{Q}_0$	$\bar{Q}$	Toggle

previous state ka complement

Q_0 = Output level prior to clock transition

neg edge triggering flip flop