

Programmable Interfacing Devices

General-Purpose Programmable Peripheral Devices

- PPI – Programmable Peripheral Interface
- It is an I/O port chip used for interfacing I/O devices with microprocessor.
- Very commonly used programmable devices from Intel family are:
 - The 8255A peripheral interface.
 - The 8254 Interval Timer.
 - The 8294A Interrupt Controller.
 - The 8237 DMA controller.

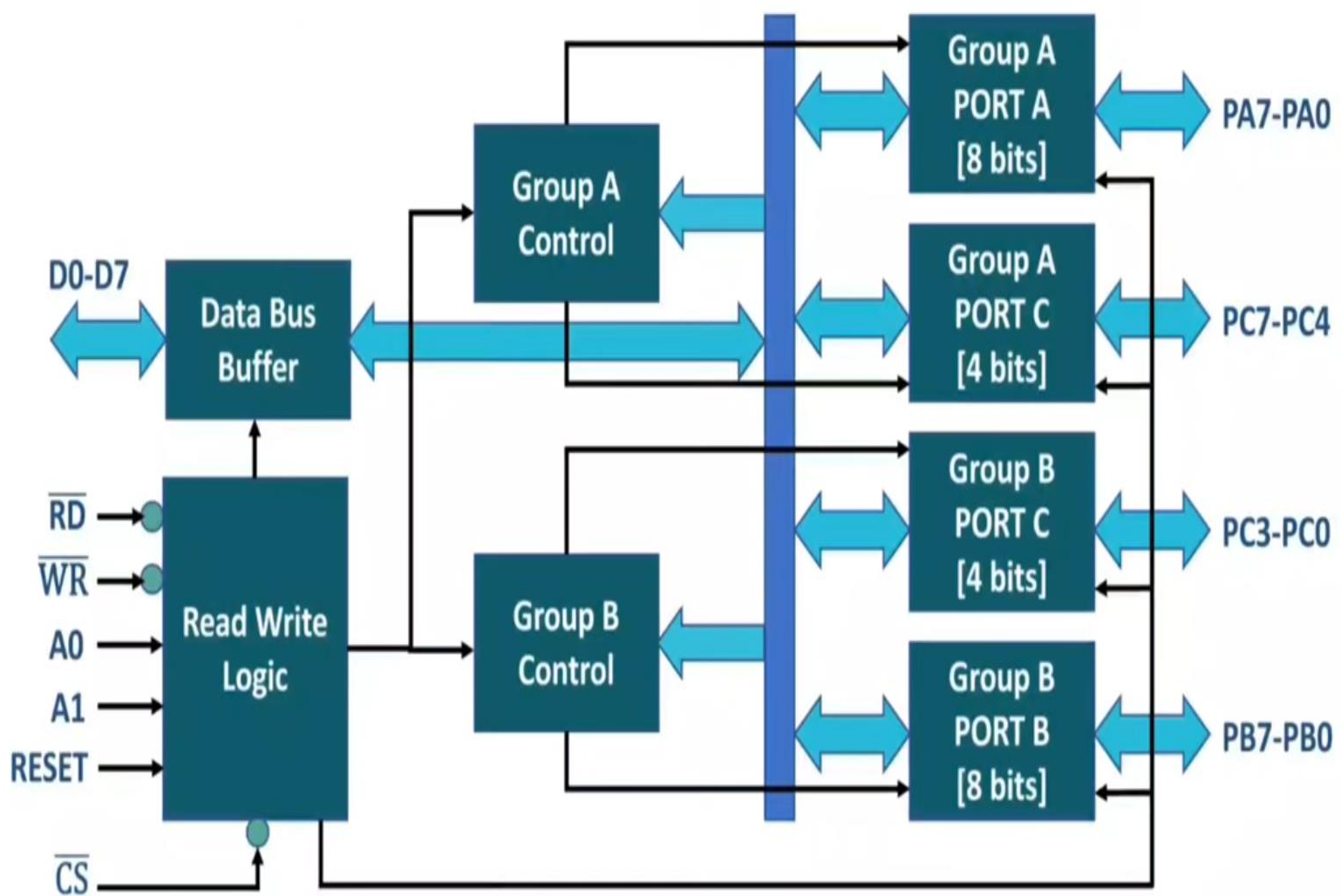
8255 Programmable Peripheral Interface

❖ Features of 8255 Programmable Peripheral Interface

- ❑ 8255 is designed to work with various microprocessors like 8085, 8086 etc.
- ❑ 8255 is designed to increase capacity of Input Output Interface.
- ❑ 8255 has three 8bits bidirectional IO ports.
- ❑ 8255 has three IO modes of transfer data:
 - Simple IO mode
 - Handshake IO mode
 - Bidirectional handshake IO mode
- ❑ 8255 has BSR mode to alter individual bits of port C.

8255A Programmable Peripheral Interface

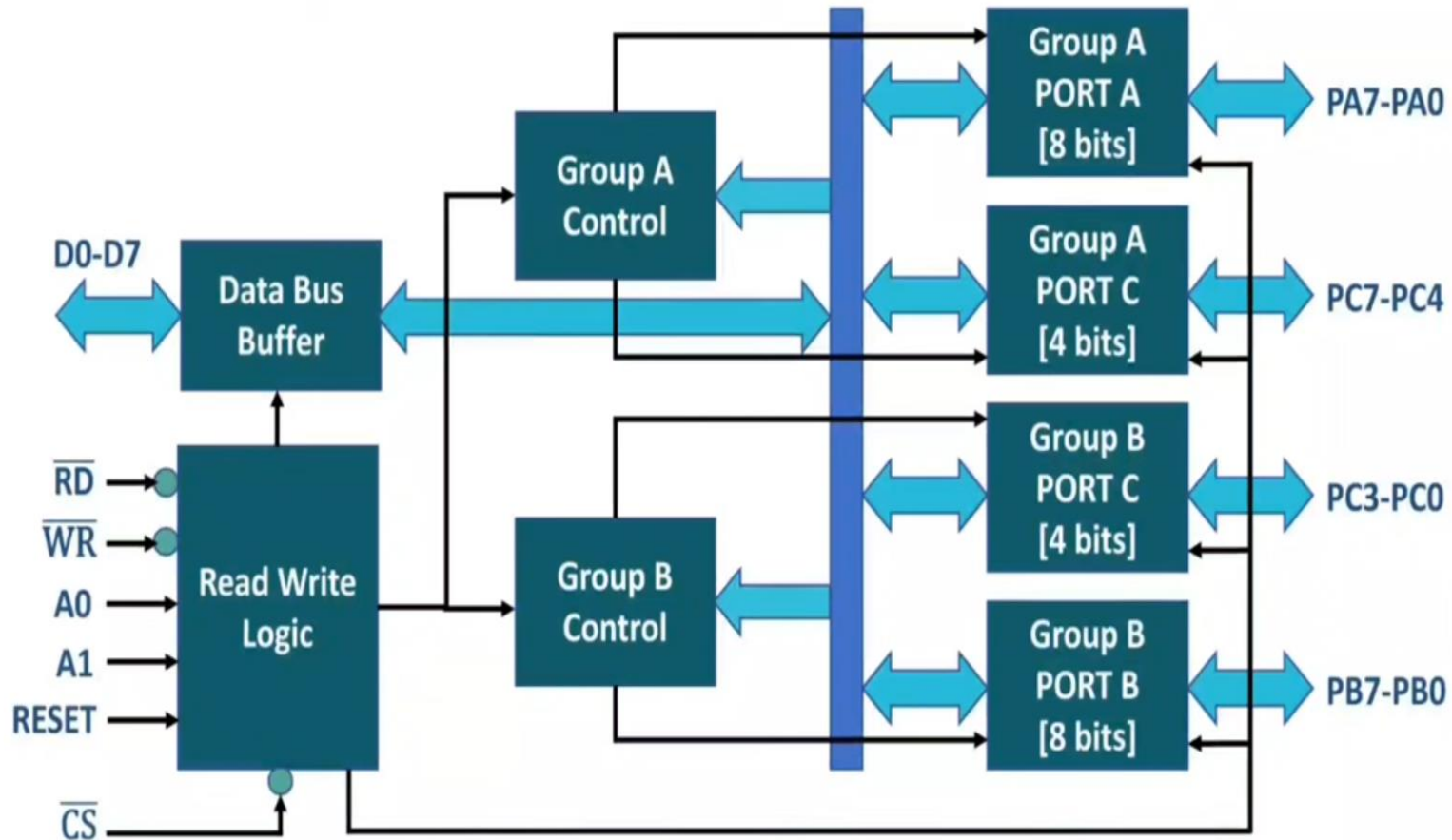
- The 8255A is a general purpose programmable I/O device designed to transfer the data from I/O to interrupt I/O under certain conditions as required. It can be used with almost any microprocessor.
- It consists of three 8-bit bidirectional I/O ports (24 I/O lines) which can be configured as per the requirement.



❖ Data Bus Buffer

- ❑ It has bidirectional data bus D0 – D7.
- ❑ D0 – D7 is interfaced with system data bus of Microprocessor.

Read Write Control Logic of 8255

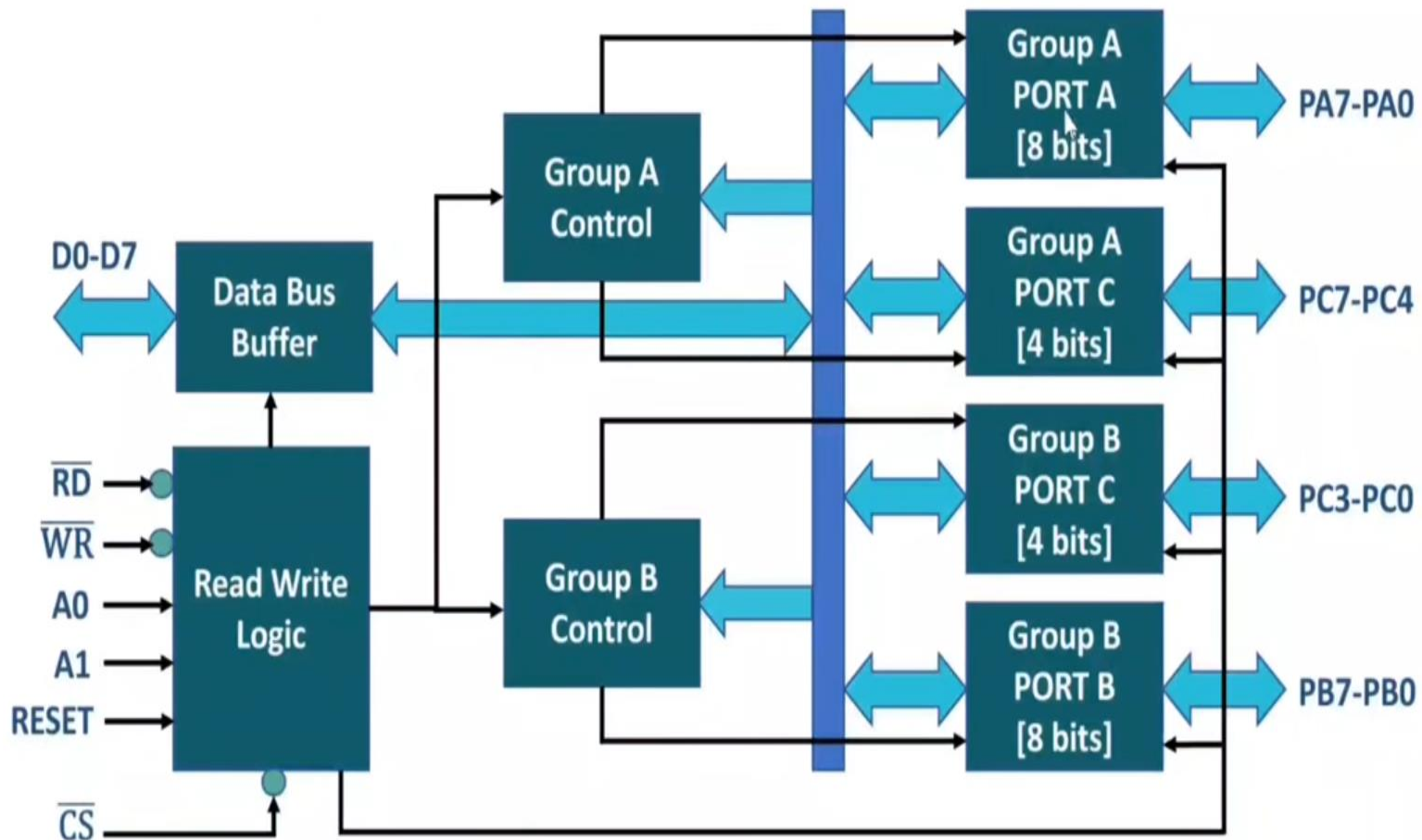


❖ Read Write Control Logic

- ❑ 8255 read and write data as per control signals \overline{RD} and \overline{WR} connected with microprocessor.
- ❑ \overline{RESET} will reset 8255.
- ❑ A_1 and A_0 used to select port and control word.
- ❑ \overline{CS} is used to select chip of 8255.

\overline{CS}	A_1	A_0	Selected	Sample Address
0	0	0	Port A	80H [1000 00 00]
0	0	1	Port B	81H [1000 00 01]
0	1	0	Port C	82H [1000 00 10]
0	1	1	Control Register	83H [1000 00 11]
1	X	X	8255 is not selected	

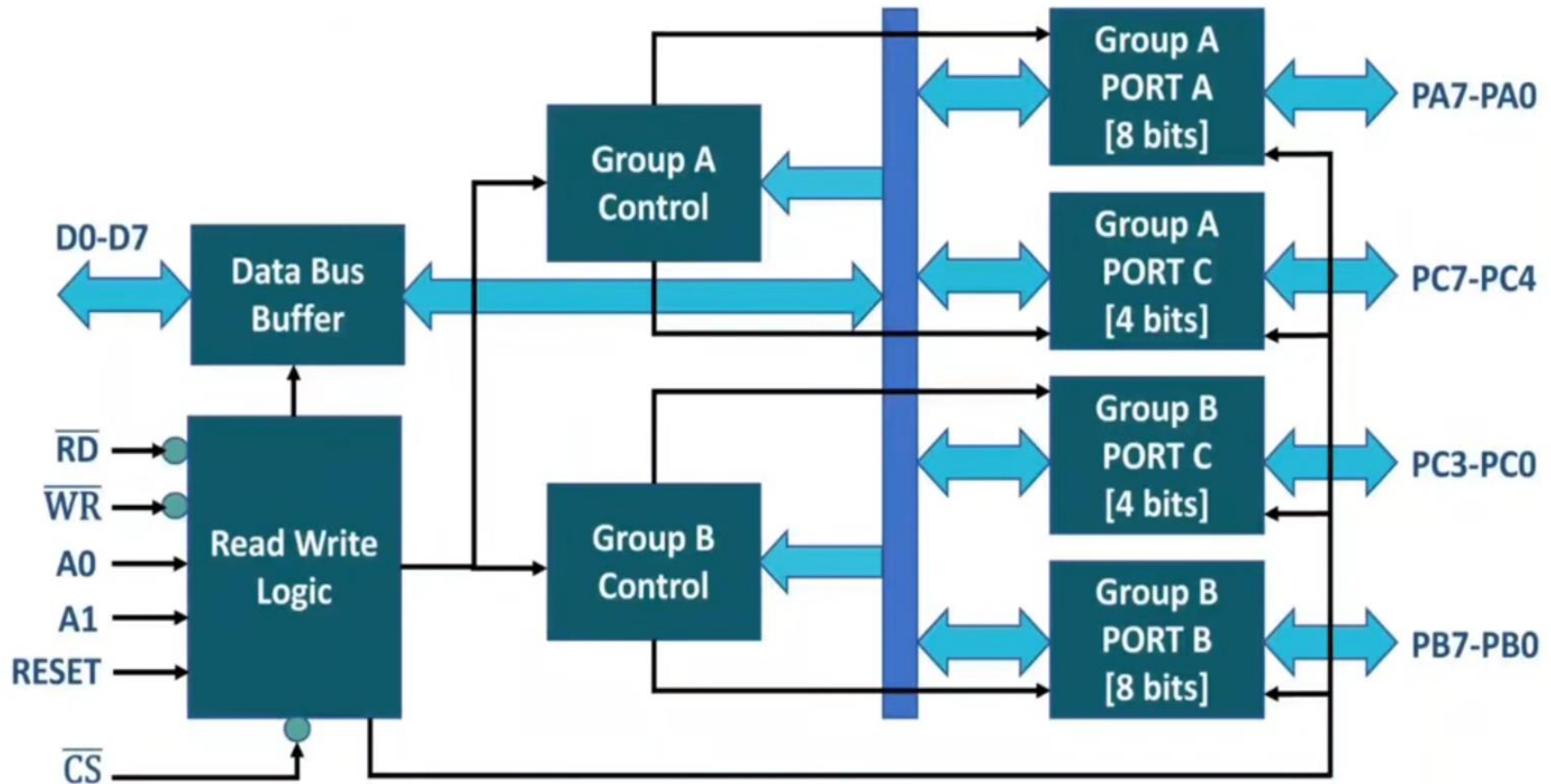
Group A & Group B Control of 8255



❖ Group A and Group B Control

- ❑ Group A control is used to control PORT A [PA7 – PA0] and UPPER PORT C [PC7 – PC4].
- ❑ Group B control is used to control PORT B [PB7 – PB0] and LOWER PORT C [PC3 – PC0].
- ❑ It takes control signals from control word and forwards it on respective ports.

Ports of 8255



❖ PORT A, PORT B and PORT C

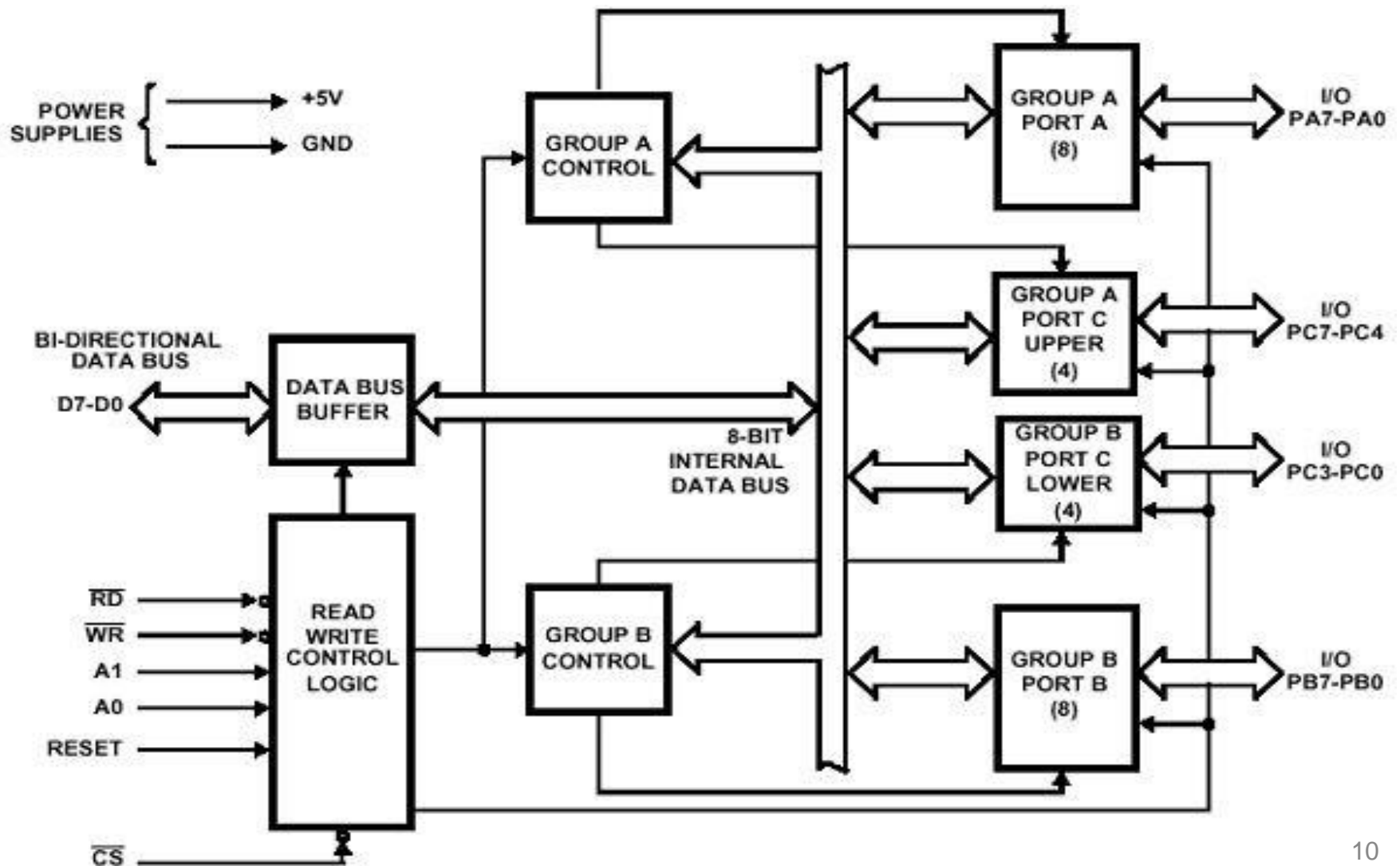
❑ These are 8 bits IO ports and works as follows:

Port	MODE 0	MODE 1	MODE 2	BSR MODE
PORT A	YES	YES	YES	NO
PORT B	YES	YES	NO	NO
PORT C	YES	NO [HS]	NO [HS]	YES

Ports of 8255A

- 8255A has three ports, i.e., PORT A, PORT B, and PORT C.
 - **Port A** contains one 8-bit output latch/buffer and one 8-bit input buffer.
 - **Port B** is similar to PORT A.
 - **Port C** can be split into two parts, i.e. PORT C lower (PC0-PC3) and PORT C upper (PC7-PC4) by the control word.
- These three ports are further divided into two groups, i.e. Group A includes PORT A and upper PORT C. Group B includes PORT B and lower PORT C. These two groups can be programmed in three different modes, i.e. the first mode is named as mode 0, the second mode is named as Mode 1 and the third mode is named as Mode 2.

Block diagram of 8255



Different Mode of Operation of 8255

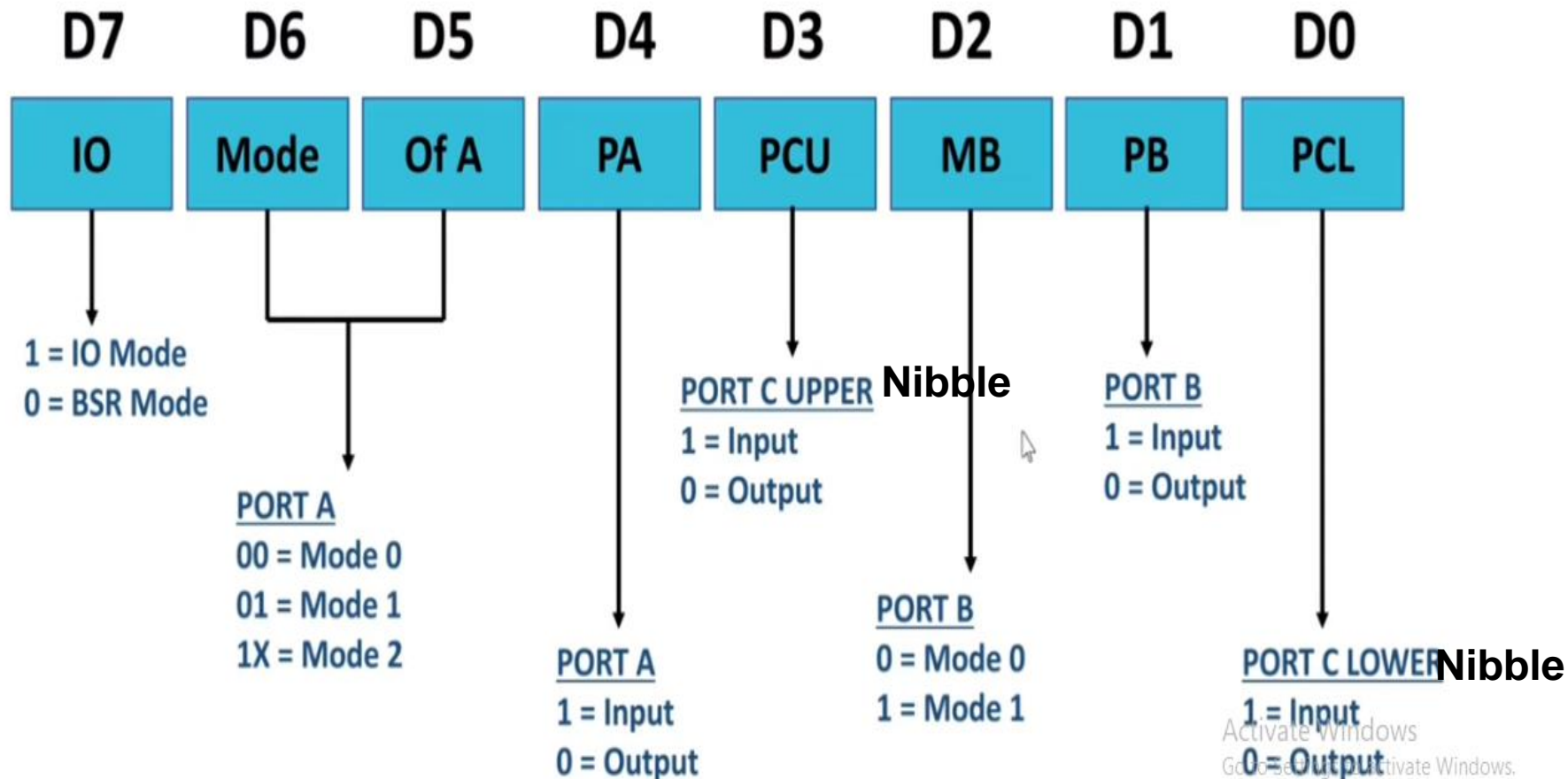
8255A has three different operating modes –

- **Mode 0** – In this mode, Port A and B is used as two 8-bit ports and Port C as two 4-bit ports. Each port can be programmed in either input mode or output mode where outputs are latched and inputs are not latched. Ports do not have interrupt capability.
- **Mode 1** – In this mode, Port A and B is used as 8-bit I/O ports. They can be configured as either input or output ports. Each port uses three lines from port C as **handshake** signals. Inputs and outputs are latched.
- **Mode 2** – In this mode, Port A can be configured as the bidirectional port and Port B either in Mode 0 or Mode 1. Port A uses five signals from Port C as **handshake** signals for data transfer. The remaining three signals from Port C can be used either as simple I/O or as handshake for port B.

Control Word and Modes of 8255

❖ Control Word

❑ 8255 has 8 bits of control word. It defines working of IO ports A, B and C.



Control Word and Modes of 8255

❖ BSR [Bit Set Reset] Mode of 8255

❑ BSR Mode only works with PORT C.



↓
1 = IO Mode
0 = BSR Mode

D1, D2, D3 Is used
to select individual
terminal of port-C

BIT Select			Bit
0	0	0	PC0
0	0	1	PC1
0	1	0	PC2
0	1	1	PC3
1	0	0	PC4
1	0	1	PC5
1	1	0	PC6
1	1	1	PC7

↓
1 = Set bit of Port C
0 = Reset bit of Port C

If the Terminal
(PC0-PC7)
values is 0/1 is
selected by D0

Activate Windows
Go to Settings to activate Windows.

Control Word and Modes of 8255

❖ Modes of 8255

- ❑ There are three 8 bits IO ports and works as follows:

Port	MODE 0	MODE 1	MODE 2	BSR MODE
PORT A	YES	YES	YES	NO
PORT B	YES	YES	NO	NO
PORT C	YES	NO [HS]	NO [HS]	YES

- ❑ Here, Mode 0 is simple IO mode.

- Output are latched and Input are not latched.
- Port Do not have Interrupt handling capacity.

Works in handshaking mode

- ❑ Here, Mode 1 is IO mode with handshake.

- Here each port uses three lines from port C as Handshake signals.
- Here, Input and Output are latched.
- Interrupt handling is supported.

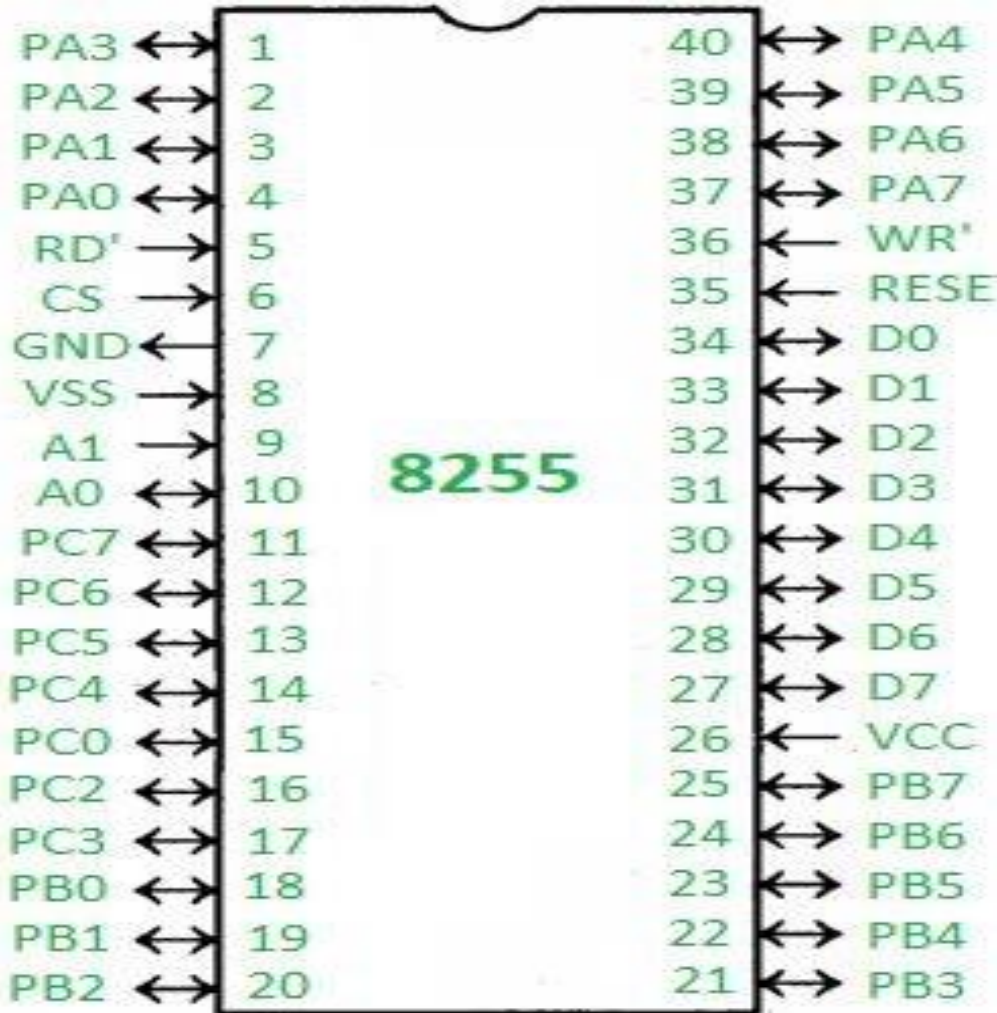
- ❑ Here, Mode 2 is Bidirectional IO mode with handshake.

- Here port A uses five lines from port C as Handshake signals.
- Interrupt handling is supported.

Activate Windows
Go to Settings to activate Windows.



Pin Diagram of 8255

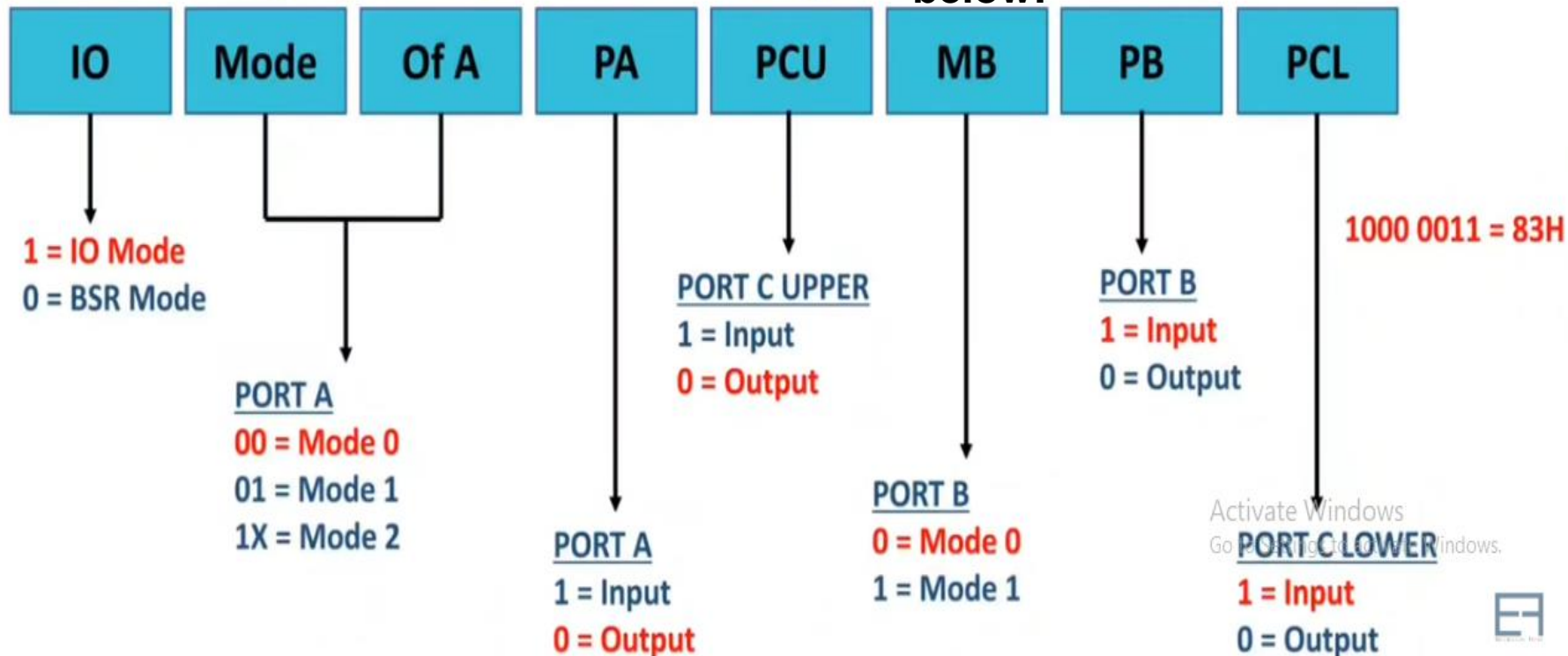


- **PA0 – PA7** – Pins of port A
- **PB0 – PB7** – Pins of port B
- **PC0 – PC7** – Pins of port C
- **D0 – D7** – Data pins for the transfer of data
- **RESET** – Reset input
- **RD'** – Read input
- **WR'** – Write input
- **CS'** – Chip select
- **A1 and A0** – Address pins

Programming of 8255

Problem

- ❖ Identify the port Address, Identify the Mode 0 control word to configure port A & Upper port C as output port and port B & Lower port C as Input port. Write a program to read DIP from Input and display it with LED on Output. Control word for the problem below:

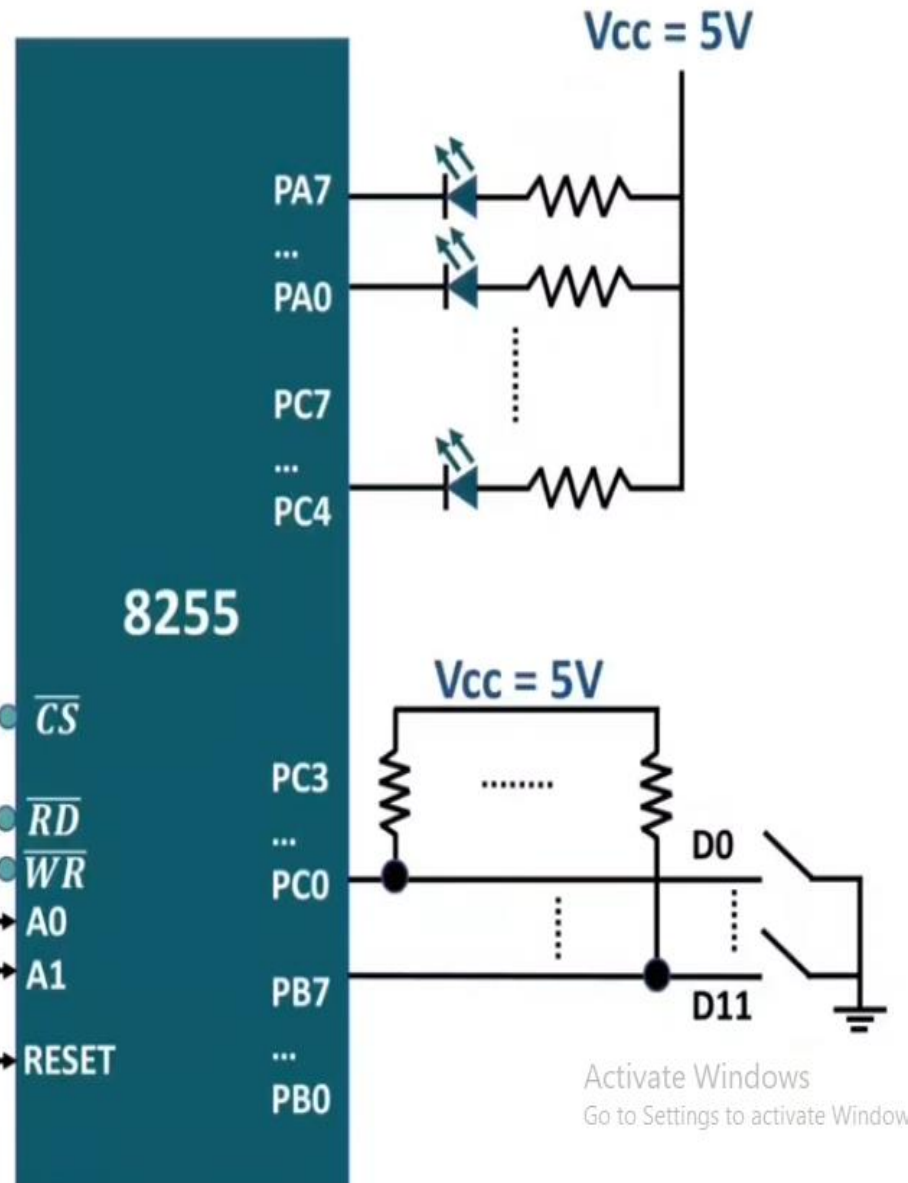
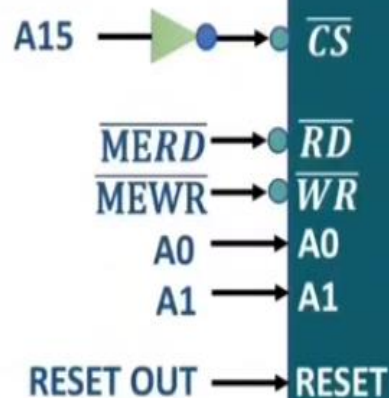


Interfacing, and Addressing Details

A15	A1	A0	Selected	Sample Address
1	0	0	Port A	8000H [1000 00 00]
1	0	1	Port B	8001H [1000 00 01]
1	1	0	Port C	8002H [1000 00 10]
1	1	1	Control Register	8003H [1000 00 11]
0	X	X	8255 is not selected	

```

XX:  MVI A,83H
      STA 8003H
      LDA 8001H
      STA 8000H
      LDA 8002H
      ANI 0FH
      RLC
      RLC
      RLC
      RLC
      STA 8002H
      JMP XX
  
```



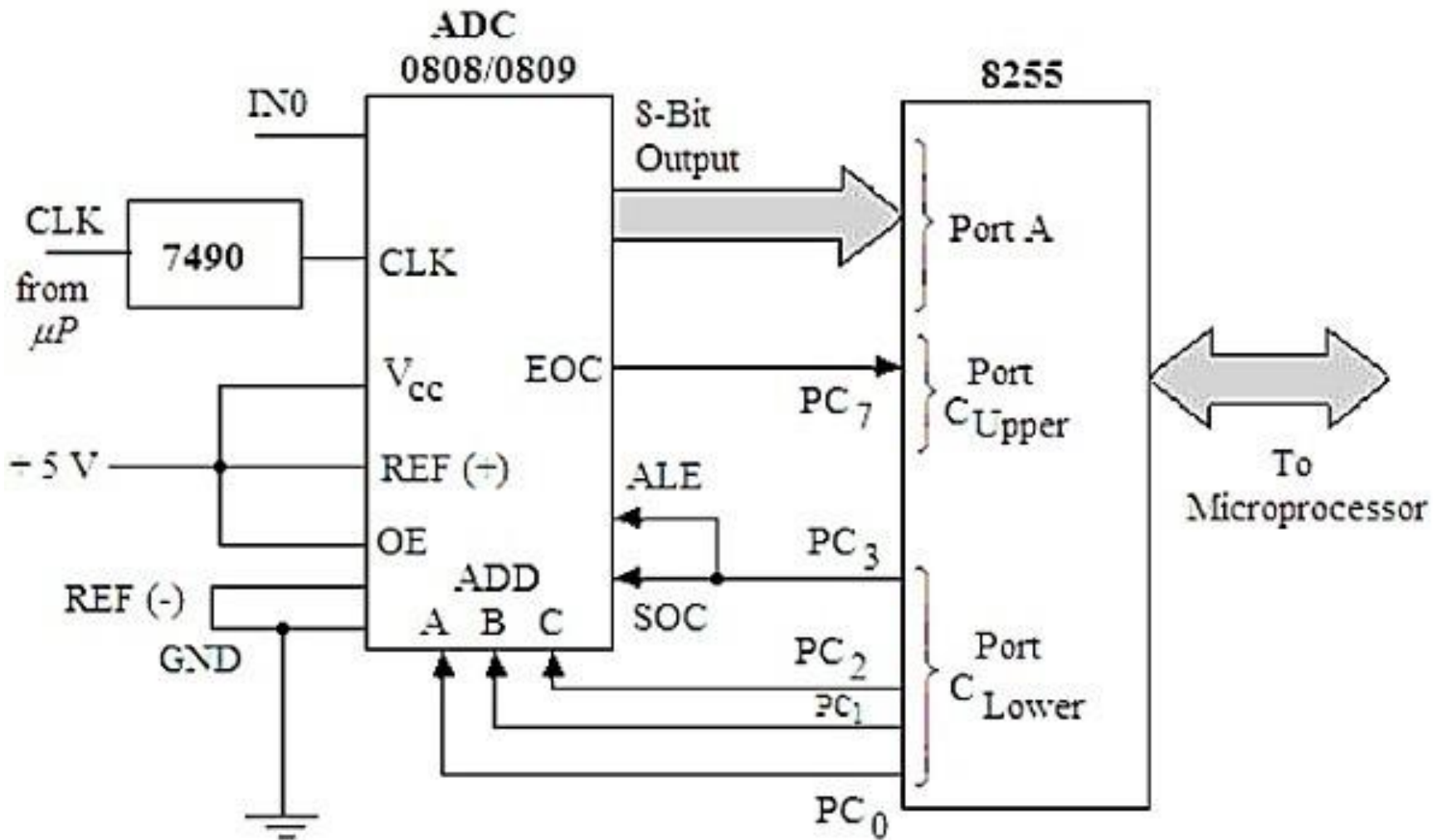
Activate Windows
Go to Settings to activate Window

MVI=Move immediately ANI=Immediate addressing RLC=Rotate Left through Carry (Convert lower to upper nibble)

Interfacing A/D converter using 8255

- To interface the ADC with 8085, we need 8255 Programmable Peripheral Interface chip with it.
- The Port A of 8255 chip is used as the input port. The PC_7 pin of Port C_{upper} is connected to the End of Conversion (EOC) Pin of the analog to digital converter. This port is also used as input port. The C_{lower} port is used as output port. The PC_{2-0} lines are connected to three address pins of this chip to select input channels. The PC_3 pin is connected to the Start of Conversion (SOC) pin and ALE pin of ADC 0808/0809.

Interfacing A/D converter using 8255 (Cont.)



8253 Programmable Interval Timer

- The Intel 8253 is Programmable Interval Timers (PTIs) designed for microprocessors to perform timing and counting functions using three 16-bit registers.
- Each counter has 2 input pins, i.e. Clock & Gate, and 1 pin for “OUT” output.
- To operate a counter, a 16-bit count is loaded in its register.
- On command, it begins to decrement the count until it reaches 0, then it generates a pulse that can be used to interrupt the CPU.

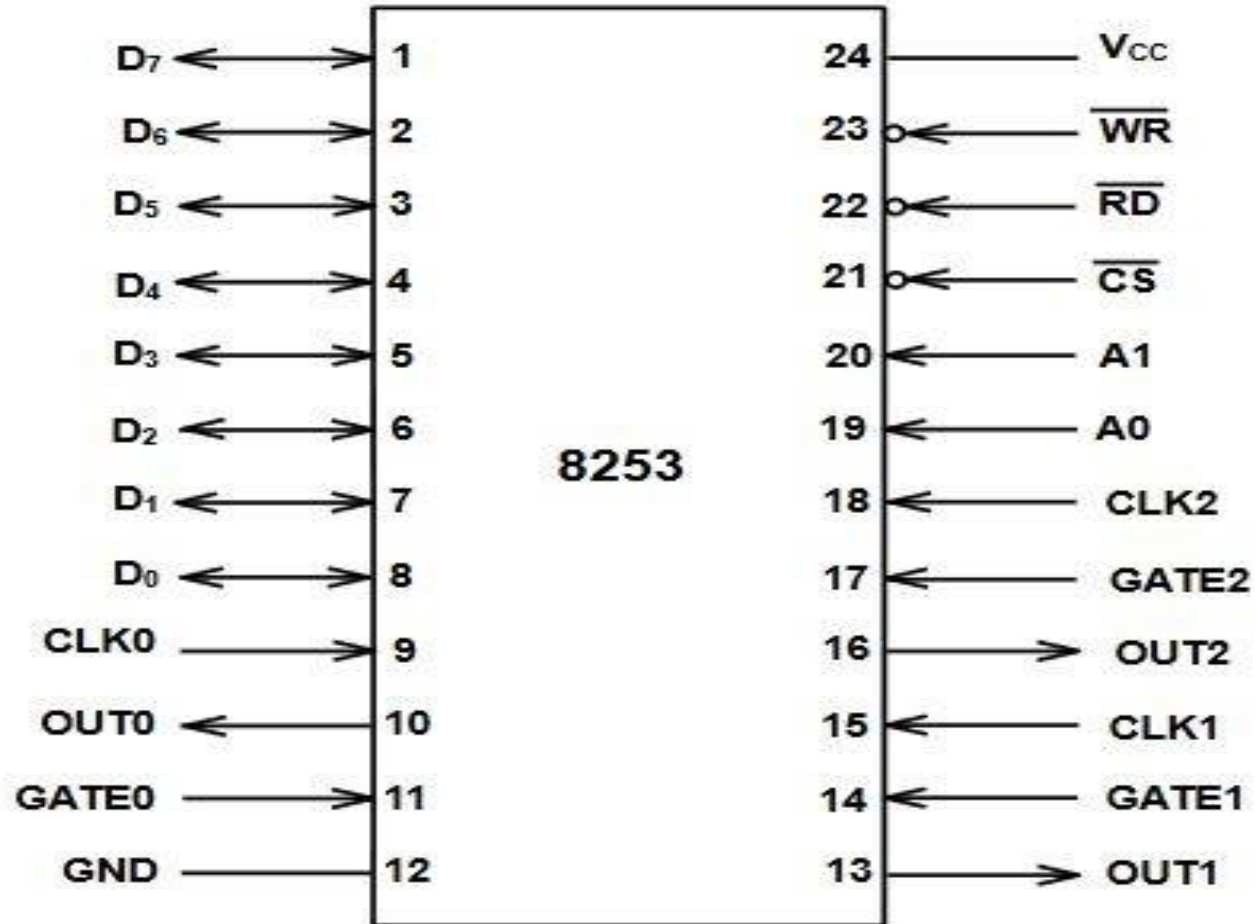


Fig.10.1 Pin Configuration of Intel 8253

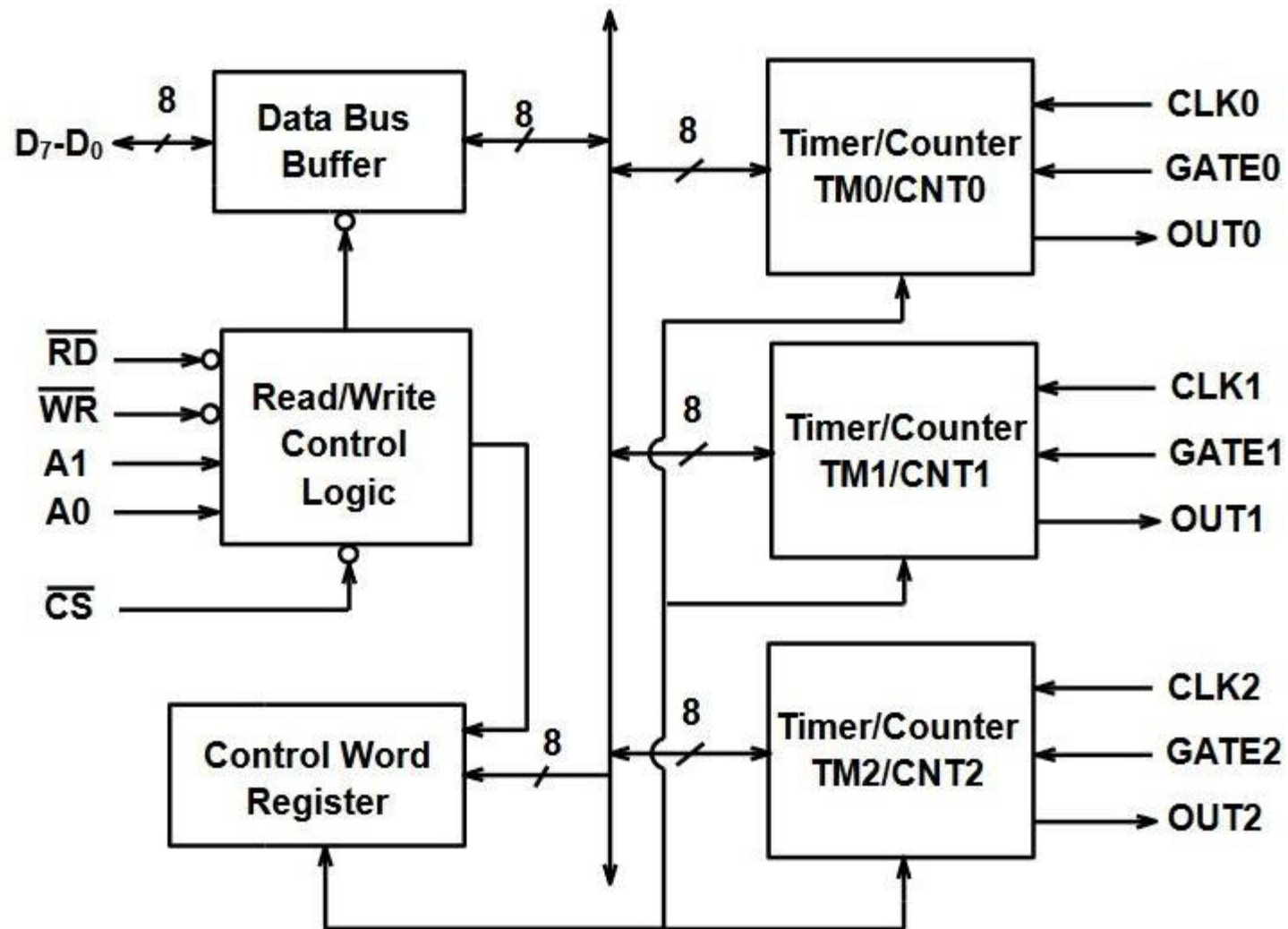


Fig.10.2 Functional Block Diagram of 8253

8259 Programmable Interrupt Controller

- The 8259A is a programmable interrupt controller specially designed to work with Intel microprocessor 8080, 8085A, 8086, 8088.

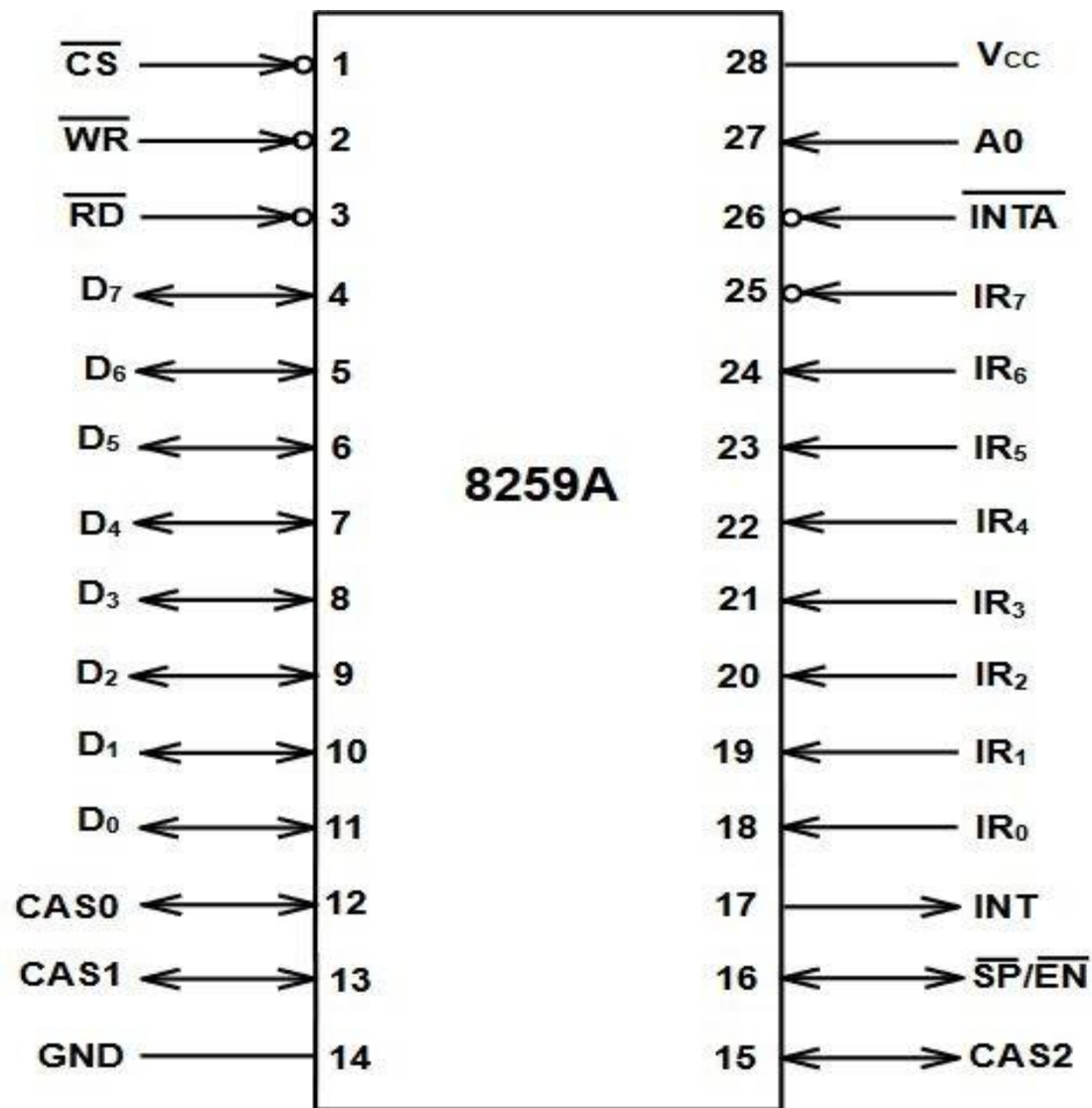


Fig.11.2 Pin Configuration of Intel 8259A

Modes of 8259A PIC

- Fully Nested mode
- Special Fully Nested mode
- Nonspecific Rotating
- Specific Rotating
- Special Mask
- Polling
- Fixed priority mode

- Fully nested mode:
 - This is a general purpose mode where all IR's are arranged in highest to lowest.
 - IR0 highest and IR7 lowest.
- Special Fully Nested Mode:
 - Used in more complicated systems.
 - Similar to, normal nested mode.
 - When an interrupt request from a certain slave is in service, this slave can further send requests to the master.
 - The master interrupts the CPU only.
- Automatic Rotation Mode:
 - In this mode a device after being serviced receives the lowest priority.

- Specific Rotation Mode:
 - In this user can select any IR for lowest priority thus fixing all priorities.
- Special Mask Mode
 - When a mask bit is set in OCW, it inhibits further interrupts at that level and enables interrupt from other levels, which are not mastered.
- Poll command
 - The INT output is neglected, though it functions normally by not connecting INT output or by masking INT input of the microprocessor.
 - This mode is entered by setting $p=1$ in OCW3.
 - A poll command may give more than 64 priority levels.

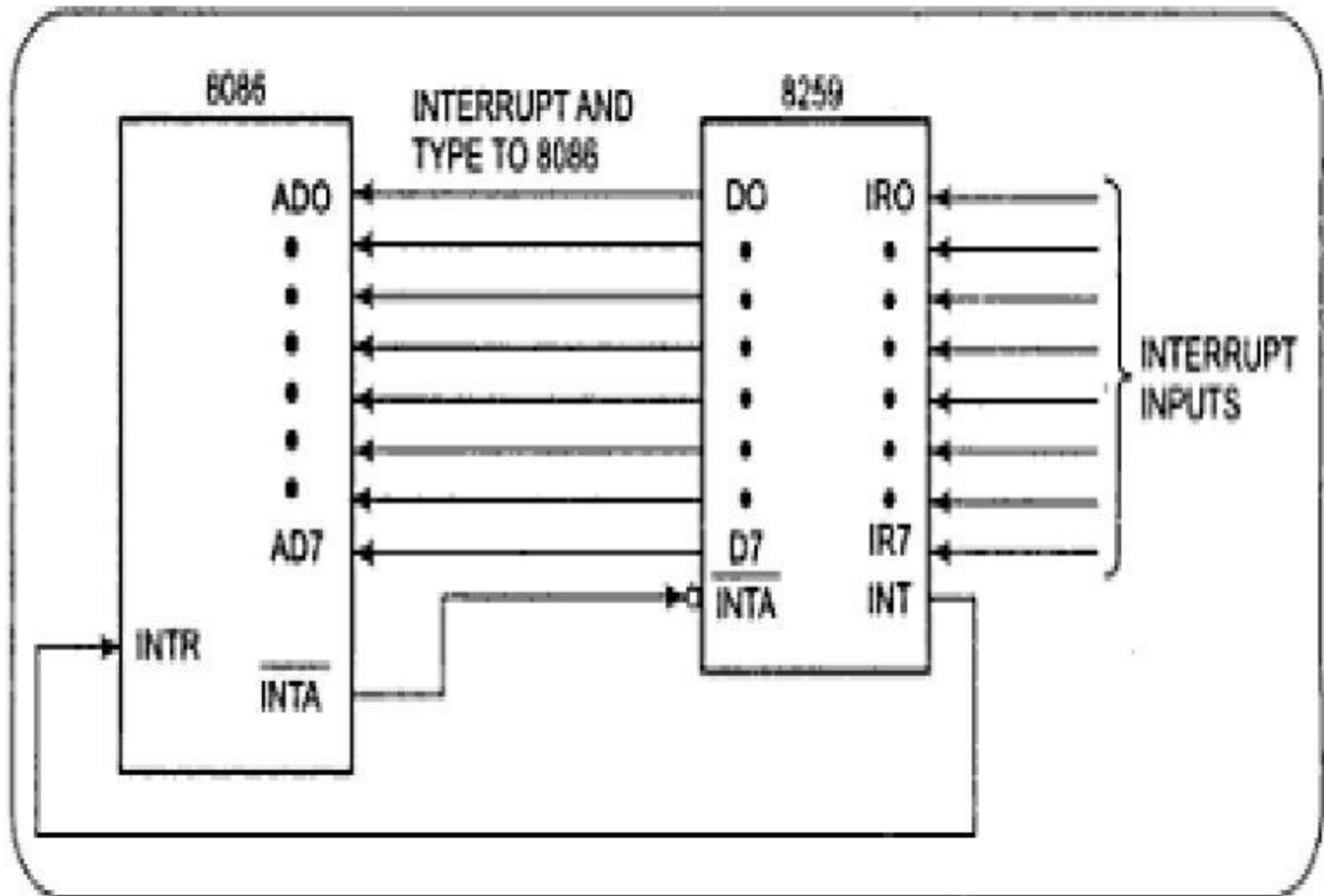


Fig:- Interface 8259 PIC with 8086 Microprocessor

8257 DMA Controller

- DMA stands for Direct Memory Access. It is designed by Intel to transfer data at the fastest rate. It allows the device to transfer the data directly to/from memory without any interference of the CPU.
- Using a DMA controller, the device requests the CPU to hold its data, address and control bus, so the device is free to transfer data directly to/from the memory. The DMA data transfer is initiated only after receiving HLDA signal from the CPU.

Features of 8257

- It has four channels which can be used over four I/O devices.
- Each channel has 16-bit address and 14-bit counter.
- Each channel can transfer data up to 64kb.
- Each channel can be programmed independently.
- Each channel can perform read transfer, write transfer and verify transfer operations.
- It generates MARK signal to the peripheral device that 128 bytes have been transferred.
- It requires a single phase clock.
- Its frequency ranges from 250Hz to 3MHz.
- It operates in 2 modes, i.e., **Master mode** and **Slave mode**.

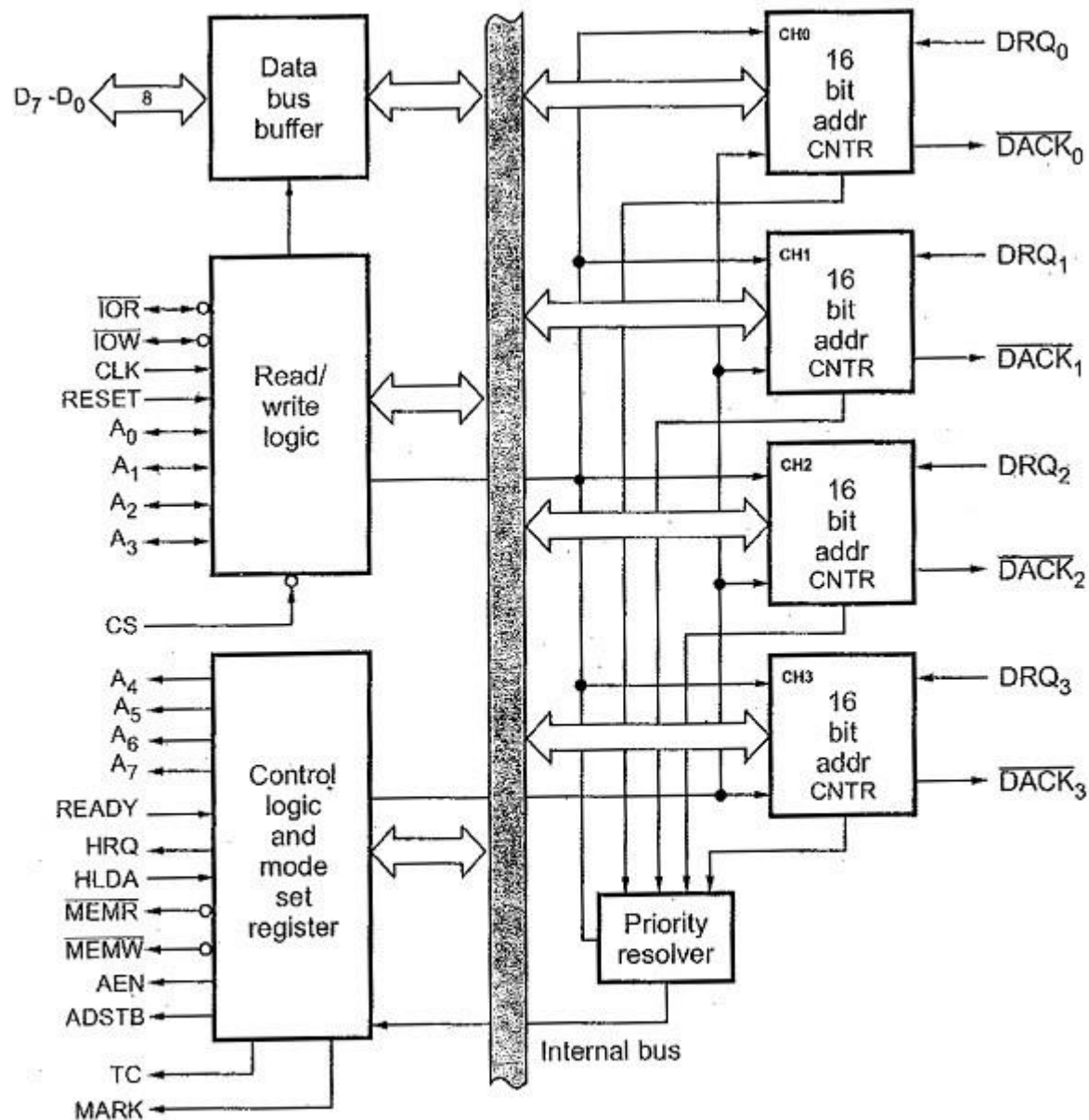


Fig. 14.62 Functional block diagram of 8257