MemtoReg\_WB

ALUout\_MEM

RegDst\_EX

rt\_EX

rd\_EX

RD2\_EX

**CLR**

**INS\_MEM**

**(ROM)**

pc

instruction

pc\_in

00

01

10

11

**+**

**R\_IF\_ID**

**PC**

pc\_out

PC\_EN

4

pc\_4

[1] 高位

**CLR**

**EN**

rs

rt

**Register\_File**

ra1

ra2

wa

wd

rd1

rd2

we

[0] 低位

op

RegWrite

**Control**

**Unit**

MemtoReg

MemWrite

ALUop

ALUSrc

RegDst

Branch

Jump

RD1

RD2

**=**

MemtoReg\_EX

MemWrite\_EX

ALUop\_EX

ALUSrc\_EX

RegWrite\_EX

**R\_ID\_EX**

RD1\_ID

RD2\_ID

rd

imm

**Sign\_EXT**

**NPC**

**<<2**

**+**

{Instruction[25:0],2’b00}

npc[31:26]

0

1

0

1

0

1

RD1\_EX

00

01

10

11

00

01

10

11

rt

rd

rs

0

1

**ALU**

ALU\_in1

ALU\_in2

WriteData\_EX

WriteReg\_EX

**R\_EX\_MEM**

ALUout\_EX

MemtoReg\_EX

MemtoReg\_WB

MemtoReg\_MEM

WriteData\_MEM

**Data**

**Memory**

addr

WriteData

ReadData

we

MemWrite\_MEM

MemtoReg\_MEM

RegWrite\_MEM

ReadData\_MEM

**R\_ MEM\_WB**

WriteReg\_MEM

RegWrite\_WB

ReadData\_WB

1

0

ALUout\_WB

WriteReg\_WB

**Hazard Unit**

**OR**

**Branch**

**R\_ID\_EX\_CLEAR**

**PC\_EN**

**R\_ID\_EX\_EN**

**SEL\_ALU1**

**SEL\_ALU2**

**SEL\_RD1**

**SEL\_RD2**

**RegWrite\_xxx**

**MemtoReg\_xxx**

sign\_ext\_imm

sign\_ext\_imm\_EX