INTRO. TO COMP. ENG. CHAPTER XI-1 DATAPATH ELEMENTS •CHAPTER XI

CHAPTER XI

DATAPATH ELEMENTS

READ DATAPATH ELEMENTS FREE-DOC ON COURSE WEBPAGE

INTRO. TO COMP. ENG. **CHAPTER XI-2 DATAPATH ELEMENTS**

DATAPATH ELEMENTS DATAPATH ELEMENTS

-INTRODUCTION

INTRODUCTION

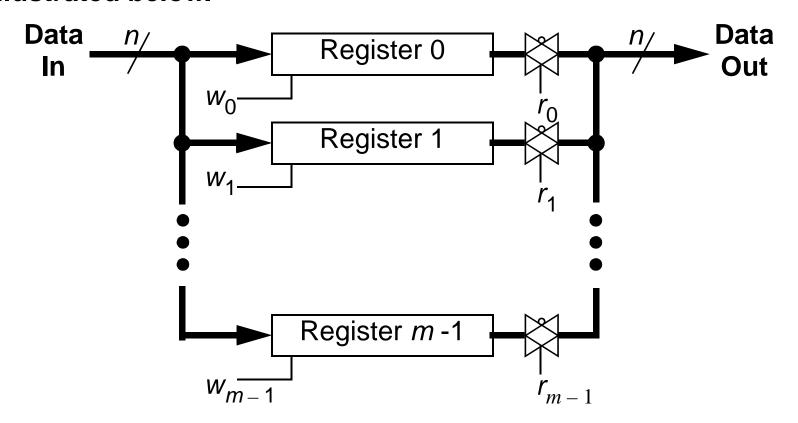
- So far we have discussed many small components and building blocks.
- One final step in our building blocks before we can start to piece together a microprocessor is various datapath elements.
 - We have already discussed portions of these datapath elements in terms of other components and building blocks.
 - We will now consider some of these components and building blocks in ways that will make the design of a microprocessor a little easier in the next chapter.

REGISTER FILES

REGISTER LAYOUT

•DATAPATH ELEMENTS
-INTRODUCTION

• A general $m \times n$ register file with m registers that are each n-bits wide is illustrated below.



• The r_k and w_j signals indicate which register to read/write, respectively.

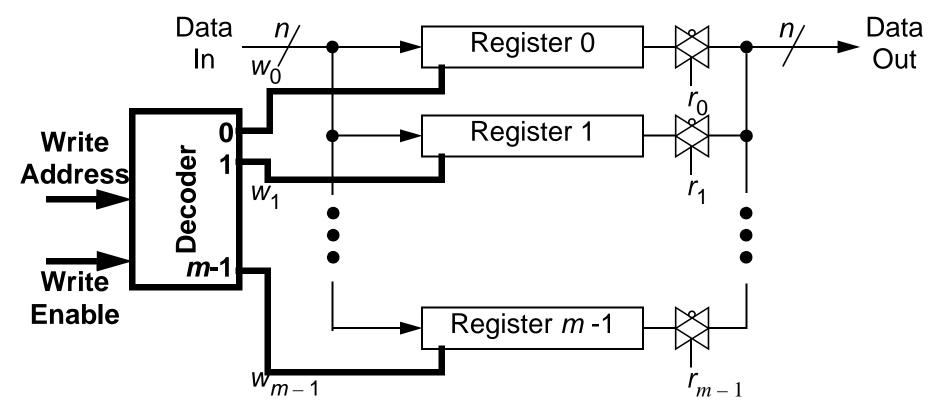
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REGISTER FILES

WRITE DECODER

•DATAPATH ELEMENTS
•REGISTER FILES
-REGISTER LAYOUT

For writing to a register, we include a write address with decoder.



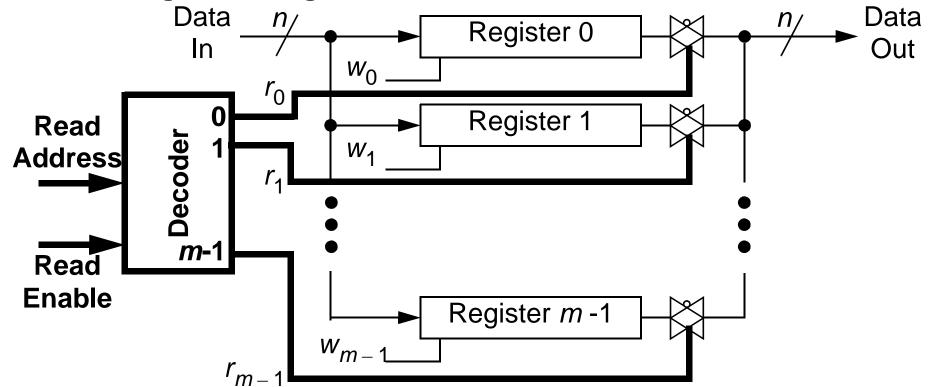
A given Write Address (with Write Enable = 1) selects which register, 0 through m - 1, to store the input from Data In.

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REGISTER FILES

READ DECODER

- •DATAPATH ELEMENTS
 •REGISTER FILES
 -REGISTER LAYOUT
 -WRITE DECODER
- For reading from a register, we include a read address with decoder.



- A given Read Address (with Read Enable = 1) selects which register, 0 through m 1, to read from and output to Data Out.
- Could have multiple data outputs with multiple read address decoders.

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DATAPATH ELEMENTS

REGISTER FILES

32-BIT WORD, 32 REGISTERS

•REGISTER FILES
-REGISTER LAYOUT
-WRITE DECODER

-READ DECODER

• For the upcoming datapath designs in the next chapter, we want to have a 32x32 register file with one write input and two read outputs.

X_{ra} - X read address

Y_{ra} - Y read address

Z_{wa} - Z write address

X_{do} - X data out

Y_{do} - Y data out

Z_{di} - Z data in

rwe - register write enable

Clk Z_{wa} Z_{wa} Z_{wa} Z_{wa} Z_{wa} Z_{wa} Z_{va} Z_{va}

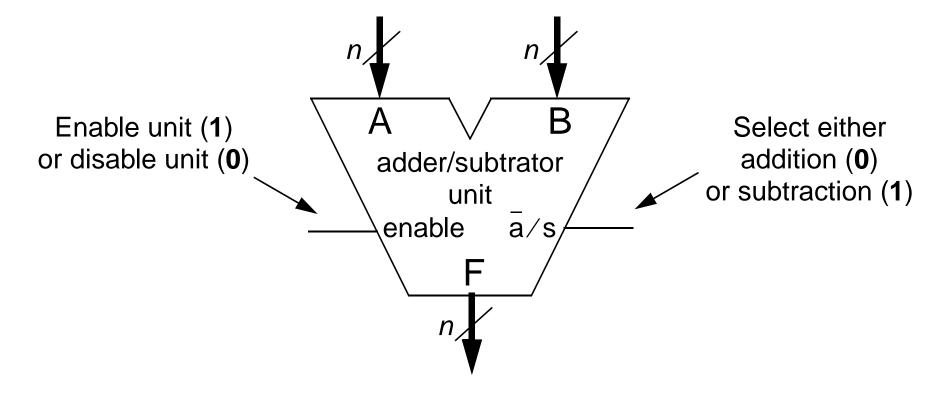
Note: Two data outputs implemented with two read address decoders.

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ADDER/SUBTRACTOR

GENERAL UNIT DIAGRAM

- •REGISTER FILES
 - -WRITE DECODER
 - -READ DECODER
 - -32X32 REGISTER FILE
- An n-bit adder/subtractor unit is often illustrated as follows.



This unit would have n full-adders internally.

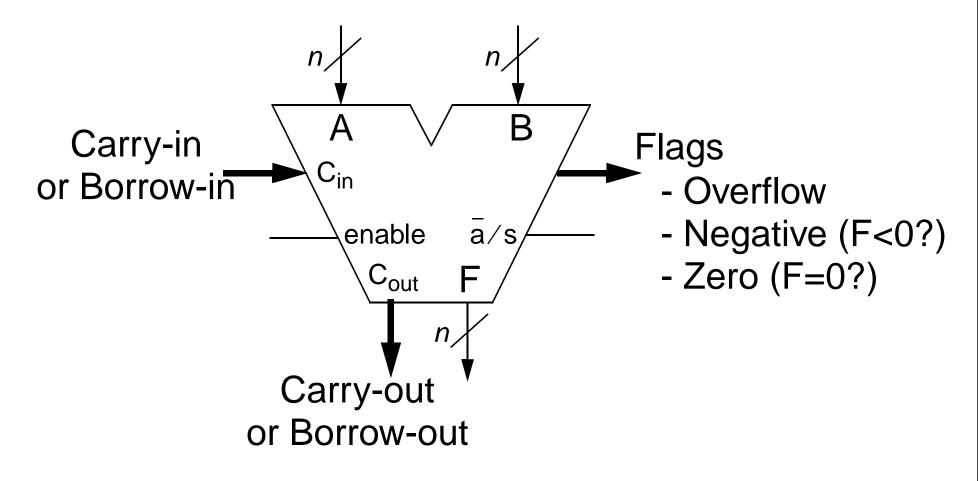
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ADDER/SUBTRACTOR

OTHER UNIT SIGNALS

•REGISTER FILES
•ADDER/SUBTRACTOR
-GENERAL UNIT DIAGRAM

 Other signals often included with an adder/subtractor are shown below.



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LOGICAL UNIT

INTRODUCTION

•REGISTER FILES
•ADDER/SUBTRACTOR
-GENERAL UNIT DIAGRAM
-OTHER UNIT SIGNALS

- A useful unit would be one that can take two n-bit inputs and perform some logical operation between each of the bits to get an n-bit output.
 - For example, given the 8-bit values **0001 1110** and **1001 1000**, we might want to find the **bit-wise logical OR**.

bit-wise 0001 1110 1001 1000 1001 1110

Or similarly, the bit-wise logical AND of the two 8-bit values.

bit-wise 0001 1110 1001 1000 0001 1000

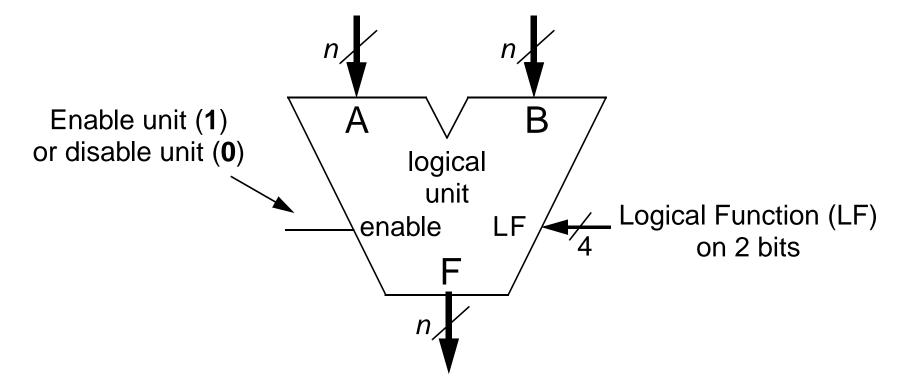
These types of operations are often used for masking and setting bits.

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LOGICAL UNIT

GENERAL UNIT DIAGRAM

- •REGISTER FILES
 •ADDER/SUBTRACTOR
 •LOGICAL UNIT
 -INTRODUCTION
- Below is a general unit diagram for an n-bit logical unit.



 Logical operations, such as AND/OR/NOT/NAND/NOR/etc., are done for each bit of A and B to form F. INTRO. TO COMP. ENG. CHAPTER XI-11 DATAPATH ELEMENTS

LOGICAL UNIT

4-BIT LOGICAL FUNCTIONS (LF)

•ADDER/SUBTRACTOR
•LOGICAL UNIT
-INTRODUCTION
-GENERAL UNIT DIAGRAM

- Recall the possible logic functions for two bits, A and B.
 - We can use the column \mathbf{F}_n as the 4-bit LF input for the logical unit.

A	В	F ₀	F ₁	F ₂	F_3	F ₄	F ₅	F ₆	F ₇	F ₈	F ₉	F ₁₀	F ₁₁	F ₁₂	F ₁₃	F ₁₄	F ₁₅
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
		0 Null	AB		 A		 B	l	 	_		 B		 A		AB	1 entity
	ITGII		 Inhibition			A ⊕ B A +				A ⊕ B B		 Implication				identity	

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LOGICAL UNIT

BIT SLICE IMPLEMENTATION

- •LOGICAL UNIT
 -INTRODUCTION
 - -GENERAL UNIT DIAGRAM
 - -4-BIT LOGICAL FUNCTIONS
- A number of internal implementations exist for the logical unit.
 - The easiest is to use a 4-to-1 multiplexer for each bit as follows

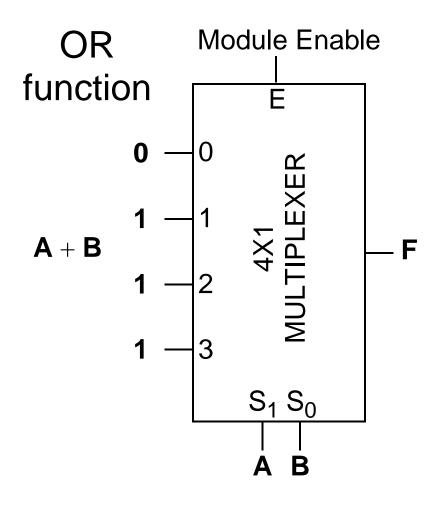
Module Enable Require *n* of these to form our *n*-bit logical unit. Take F_n column from previous slide as LF input Note: When you look at a design for each bit, it is known as a $S_1 S_0$ bit slice

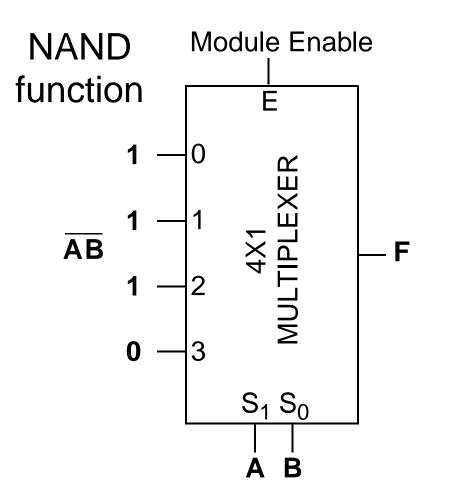
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LOGICAL UNIT

BIT SLICE IMPLEMENTATION

- •LOGICAL UNIT
 -GENERAL UNIT DIAGRAM
 -4-BIT LOGICAL FUNCTIONS
 -BIT SLICE IMPLEMENTAT.
- The following are example LF inputs for a logical unit bit slice.





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SHIFT UNIT INTRODUCTION

•LOGICAL UNIT
-GENERAL UNIT DIAGRAM
-4-BIT LOGICAL FUNCTIONS

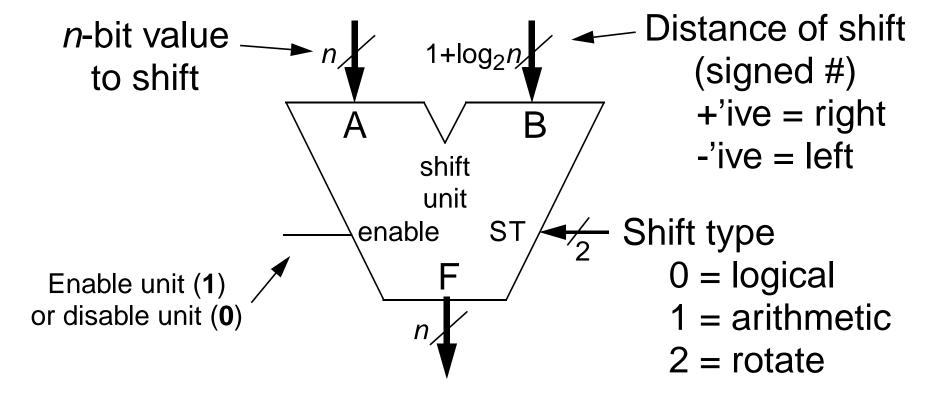
- -BIT SLICE IMPLEMENTAT.
- We have already discussed the bulk about shift units in previous chapters.
- As given in the Free-Doc, there are different types of shift units.
 - Logical shift
 - Arithmetic shift
 - Circular shift (this is just a rotate unit)
- We want to discuss an implementation, the barrel shifter, that will be useful in our single cycle datapath computer we will design next chapter.

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SHIFT UNIT

GENERAL UNIT DIAGRAM

- •LOGICAL UNIT
 •SHIFT UNIT
 -INTRODUCTION
- Below is a general unit diagram for an n-bit shift unit.

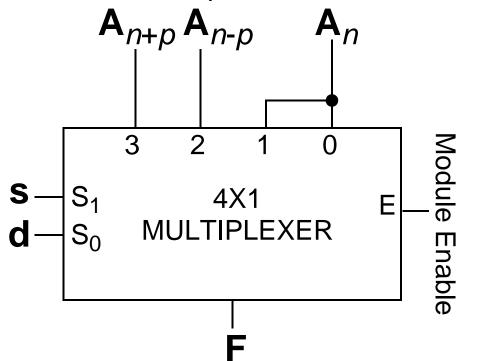


 Notice that the n-bit value A will be shifted according to the distance indicated with signed number B. INTRO. TO COMP. ENG. CHAPTER XI-16 DATAPATH ELEMENTS

SHIFT UNIT

P-SHIFTER BIT SLICE

- •LOGICAL UNIT
 •SHIFT UNIT
 -INTRODUCTION
 -GENERAL UNIT DIAGRAM
- Previously, we discussed the p-shifter but not its implementation.
 - A *p*-shifter shifts the value to the left or right by *p*-bits.
 - A bit slice view of a p-shifter for nth bit could be as follows.



Notice that this can ONLY shift by p-bits. It is hardwired to shift p-bits.

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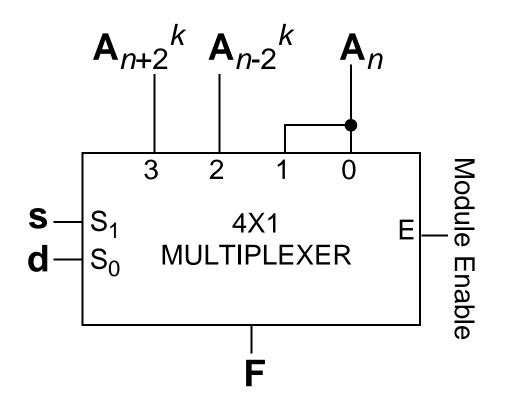
SHIFT UNIT

2^K-SHIFTER BIT SLICE

SHIFT UNIT

- -INTRODUCTION
- -GENERAL UNIT DIAGRAM
- -P-SHIFTER BIT SLICE

• A useful type of p-shifter is when $p = 2^k$ for some positive integer k.



• A 2^k-shifter allows use to build a barrel shifter.

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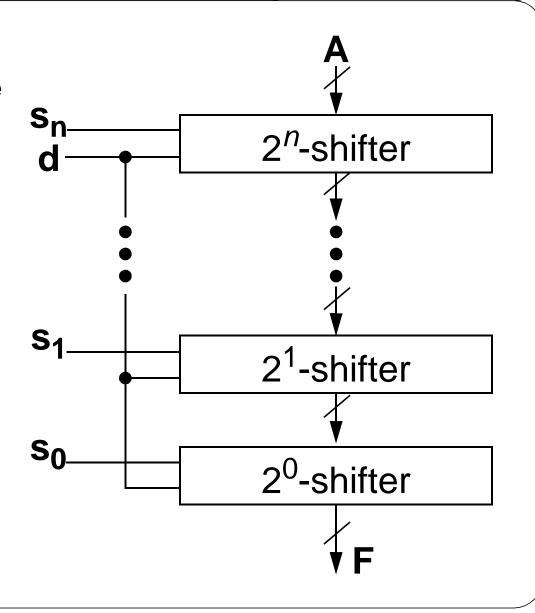
SHIFT UNIT

BARREL SHIFTER

SHIFT UNIT

- -GENERAL UNIT DIAGRAM
- -P-SHIFTER BIT SLICE
- -2^K-SHIFTER BIT SLICE

- We want to be able to shift a vector by an arbitrary distance instead of hardwired like the p-shifter and 2^k-shifter.
 - The top level can shift A by n bits, depending on s_n.
 - Subsequent levels can shift result by n/2 bits, depending on their input s_q.



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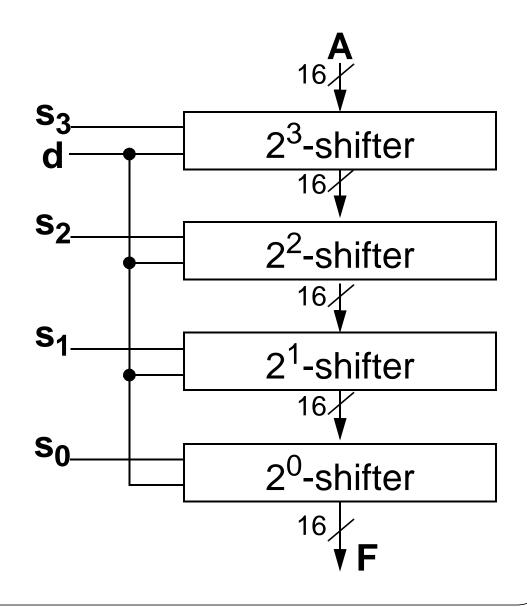
SHIFT UNIT

SAMPLE BARREL SHIFTER

•SHIFT UNIT

- -P-SHIFTER BIT SLICE
- -2K-SHIFTER BIT SLICE
- -BARREL SHIFTER

- We will do some examples
 with the following arbitrary
 n-shifter on a 16-bit input.
- Note that this barrel shifter can shift the input by 15 bits in either direction.



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SHIFT UNIT

BARREL SHIFTER: EXAMPLE #1

•SHIFT UNIT

- -2^K-SHIFTER BIT SLICE
- -BARREL SHIFTER
- -SAMPLE BARREL SHIFTER

For example, consider the input of

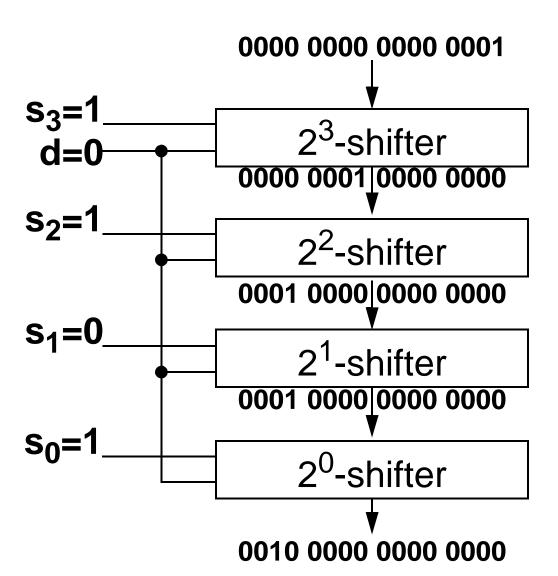
0000 0000 0000 0001

 If we want to shift this value to the left by 13, we need the input

$$d = 0$$

 $s = (s_3s_2s_1s_0) = 1101$

Note: This example is for a logical shift.



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SHIFT UNIT

BARREL SHIFTER: EXAMPLE #2

•SHIFT UNIT

- -BARREL SHIFTER
- -SAMPLE BARREL SHIFTER
- -BARREL SHIFTER EX. #1

- As another example,
 consider the input of
 1001 0100 1110 0001
 - If we want to shift this value to the **right** by **6**, we need the input

$$d = 1$$

 $s = (s_3s_2s_1s_0) = 0110$

Note: This example is for a logical shift.

