Metric Pitch BGA and Micro BGA Routing Solutions

By Tom Hausherr

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Overview:
The following paper provides Via Fanout and Trace Routing solutions for various metric pitch Ball Grid Array Packages.

Note: the "metric" dimensions are the ruling numbers.

To solve the metric pitch BGA dilemma, one should have a basic understanding of the metric feature sizes for:

- BGA Ball Sizes and BGA Land Pattern Pad Construction
- BGA Via Anatomy
- Trace/Space
- Trace and Via Routing Grid
- Differential Pairs
- HDI Hole Size/Annular Ring

Starting: The BGA Pad Size is determined by the Ball Size as seen below in Table 14-5 from IPC-7351A.

Table 14-5: Land Approximation (mm) for Collapsible Solder Balls

Nominal Ball Diameter	Reduction	Land Pattern Density Level	Nominal Land Diameter	Land Variation
0.75	25%	A	0.55	0.60 - 0.50
0.65	25%	A	0.50	0.55 - 0.45
0.60	25%	A	0.45	0.50 - 0.40
0.55	25%	A	0.40	0.45 - 0.35
0.50	20%	B	0.40	0.45 - 0.35
0.45	20%	B	0.35	0.40 - 0.30
0.40	20%	B	0.30	0.35 - 0.25
0.35	20%	B	0.30	0.35 - 0.25
0.30	20%	B	0.25	0.25 - 0.20
0.25	20%	B	0.20	0.20 - 0.17
0.20	15%	C	0.17	0.20 - 0.14
0.17	15%	C	0.15	0.18 - 0.12
0.15	15%	C	0.13	0.15 - 0.10

Note: The IPC-7351A LP Calculator Uses this chart for calculations

It is very important to note that IPC prefers the Maximum Material Condition for all BGA Land sizes; they do not use the Nominal Land Diameter, but do use the Maximum Land Variation Diameter.

IPC-7351A has a 3-Tier BGA formula for Placement Courtyards that uses the BGA ball size to calculate an adequate placement courtyard for BGA rework tools.

If the BGA has a large ball size, larger rework equipment is necessary to unsolder the large solder volume.

With a small ball size, the placement courtyard can be smaller as less heat is then required to unsolder the BGA component for rework. However, the end user may not plan to rework the BGA if it fails. In that case, there is no need to have a robust placement courtyard.

Table 3-18 below represents the 3-Tier scenario and the different placement courtyard sizes.

Table 3-18: Ball Grid Array Density Levels

Lead Part	Minimum (Least) Density Level C	Median (Nominal) Density Level B	Maximum (Most) Density Level A
Periphery Collapsing Ball	15% reduction below nominal ball diameter	20% reduction below nominal ball diameter	25% reduction below nominal ball diameter
Periphery Noncollapsing Ball or Column	5% increase above the nominal ball or column diameter	10% increase above the nominal ball or column diameter	15% increase above the nominal ball or column diameter
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.50	1.00	2.00
Ball Grid Array **(BGA)** Construction and land pattern development are described in 14.1 & 14.4			
Column Grid Array **(CGA)** Construction and land pattern development are described in 14.1.3 & 14.4			

The anatomy of the “Metric Via” is based on the 0.05mm universal grid for PCB design layout. The features of the metric via should always be sized in 0.05 increments –

- Pad Size
- Hole Size
- Solder Mask Size
- Plane Clearance (Anti-pad) Size
- Plane Thermal Relief ID and OD Size

The chart in Table 1 represents common via padstack feature sizes for various pitch BGA components.

Table 1: Common Via Padstacks

BGA Pin Pitch	VIA Name	Land Diameter	Finished Hole Dia	Plane Clearance	Solder Mask	Thermal ID	Thermal OD	Thermal Spoke Width
1.50 mm	VIA60-25-80	0.60	0.25	0.80	0.00	0.55	0.80	0.25 or None
1.50 mm	VIA55-25-75	0.55	0.25	0.75	0.00	0.55	0.75	0.25 or None
1.27 mm	VIA63-30-85	0.635	0.30	0.85	0.00	0.65	0.85	0.25 or None
1.00 mm	VIA55-25-75	0.55	0.25	0.75	0.00	0.55	0.75	0.25 or None
1.00 mm	VIA50-25-70	0.50	0.25	0.70	0.00	0.55	0.70	0.25 or None
0.80 mm	VIA45-20-65	0.45	0.20	0.65	0.00	0.50	0.65	0.20 or None
0.75 mm	VIA40-20-65	0.40	0.20	0.65	0.00	0.50	0.65	0.20 or None

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The IPC-7351A LP Calculator has a BGA via calculator that allows the user to input BGA Pitch and Trace/Space data. It automatically calculates the optimized via for any technology and the results are shown in Table 1.

Metric Trace/Space sizes are in 0.025 mm (1 mil) increments.

Common metric trace widths with the nearest Imperial unit in brackets (mils) –

- 0.075 mm (3 mils)
- 0.1 mm (4 mils)
- 0.125 mm (5 mils)
- 0.15 mm (6 mils)
- 0.2 mm (8 mils)

Today, finest pitch BGA in the industry today is 0.4. There are plans for 0.3 and even 0.25 pitch BGA components, but mainstream fabrication facilities must first find easy to manufacture routing solutions for the 0.4 mm pitch. 0.05 trace/space is not yet mainstream. See Figure 1 and Table 2 for the BGA technology chart that provides through-hole Via-in-Land information.

Figure 1: BGA Using Via-in-Land Technology

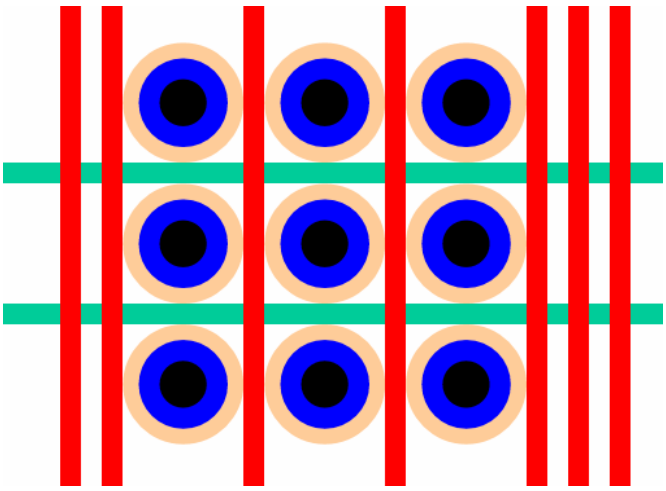

Table 2: BGA Technology Chart for 0.4, 0.5 and 0.65 pitch BGA parts

BGA Pin Pitch	BGA Ball Dia	BGA Land Size	Land Hole Size	Plane Clearance	Trace Width	Trace/ Trace Space	Trace/ Via Space	Trace/ Land Space	Route Grid	Part Place Grid
0.4	0.25	0.25	0.125	0.35	0.05	0.05	0.05	0.05	0.05	0.5
0.5	0.3	0.275	0.15	0.425	0.075	0.075	0.075	0.075	0.05	0.5
0.65	0.4	0.4	0.15	0.5	0.1	0.1	0.1	0.075	0.05	1
0.65	0.4	0.425	0.2	0.575	0.075	0.075	0.075	0.075	0.05	1

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For all via-in-land technology, a thermal relief on the voltage and ground plane connections must be used to prevent cold solder joints. A direct via-in-land connection to the plane will dissipate the heat required to melt the solder around the BGA ball and this will result in a cold or cracked solder joint.

If traces are routed between pins of the BGA land with 0.4, 0.5 and 0.65 pitch, the solder mask must be a 1:1 scale to create a “solder mask defined” BGA land. In this way, the traces between the lands will be protected from exposure and possible short circuiting.

The 0.4 pitch BGA via-in-land through the PCB is leading edge technology. When laser drills are capable of producing 0.125 hole sizes entirely through the board and PCB manufacturers can accurately fill the holes with conductive metal epoxy, this technology will become mainstream.

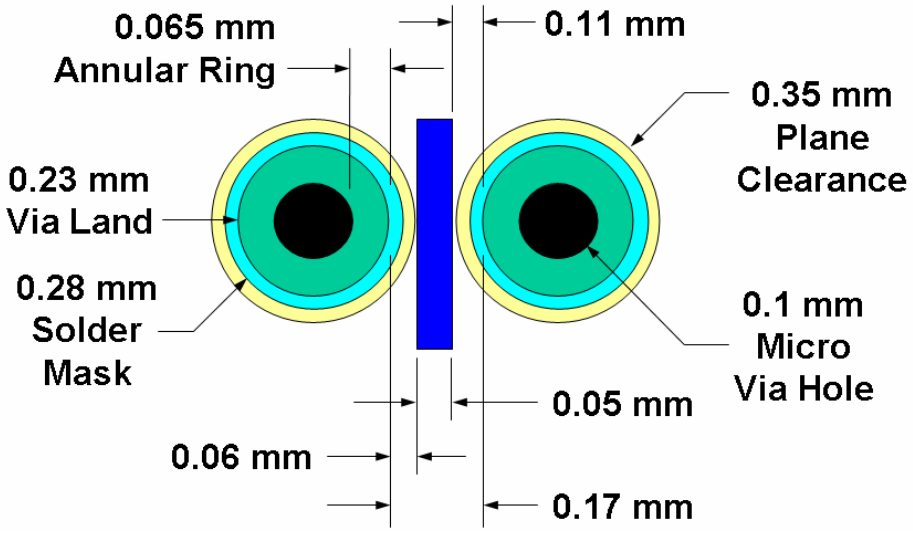
The 0.5 pitch BGA via-in-land through the PCB is also leading edge technology. Before it can become mainstream, laser drills must produce 0.15 hole sizes entirely through the board and PCB manufacturers must accurately fill the holes with conductive metal epoxy. However, this technology can be used when PCB thickness is 1.0 or less.

The 0.65 pitch BGA via-in-land through the PCB **is** mainstream technology. Mechanical 0.2 hole sizes entirely through the board are common and PCB manufacturers can accurately fill the holes with conductive metal epoxy. This technology can be used when PCB thickness is 1.57 or less.

Micro Via technology is the mainstream solution for 0.4 and 0.5 pitch BGA parts when a 0.1 – 0.15 laser hole is drilled one or two layers deep.

Figures 2, 3 and 4 illustrate routing solutions for “Micro Via” technology for a 0.4 pitch BGA.

Figure 2: 0.4 Pitch BGA using Micro Via Technology



Whenever traces are routed between 0.4, 0.5 and 0.65 pitch, the BGA pads on the outer layers, the solder mask size and the tolerance must be considered. It is best not to route any traces between BGA pads, but if necessary, the solder mask should be a 1:1 scale of the land size or a 0.025 minimum annular ring.

Figure 3: 0.4 Pitch BGA Solder Mask Clearance

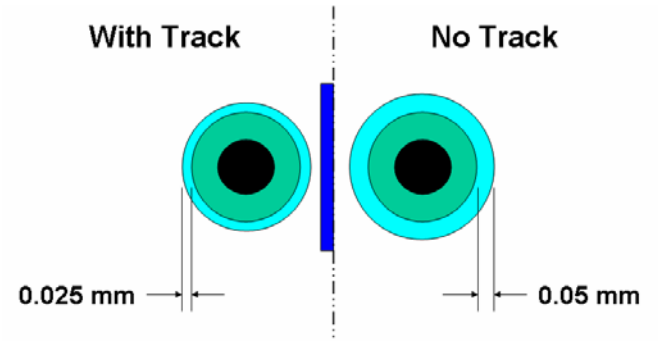
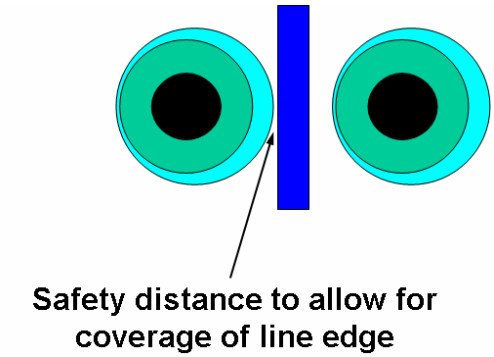


Figure 4: 0.4 Pitch BGA Solder Mask Maximum Offset



The four PCB cross sections below use three different via technologies –

- Through Via
- Blind Via
- Burried Via

There are “Staggered Micro Vias”, Figure 5 and “Stacked Micro Vias, Figures 6, 7, and 8. I prefer the stacked micro vias as PCB design layout is easier. In this case, there are fewer visible obstacles to manage when using the CAD tool.

Most PCB designers use blind stacked micro vias and buried vias as the routing solutions for the 0.5 pitch BGA. However, the through-hole via in land is actually a less expensive alternative as long as the PCB thickness is 1 mm or less to maintain a good aspect ratio.

Figure 5: Staggered Micro Vias

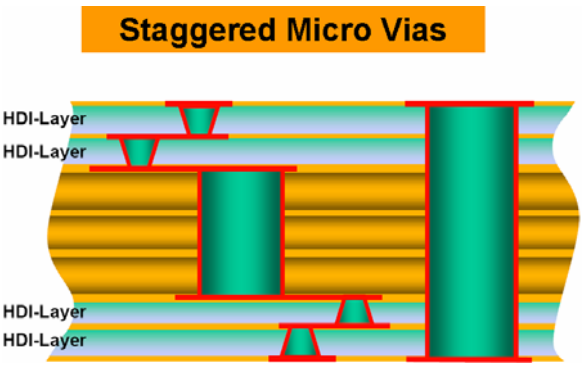
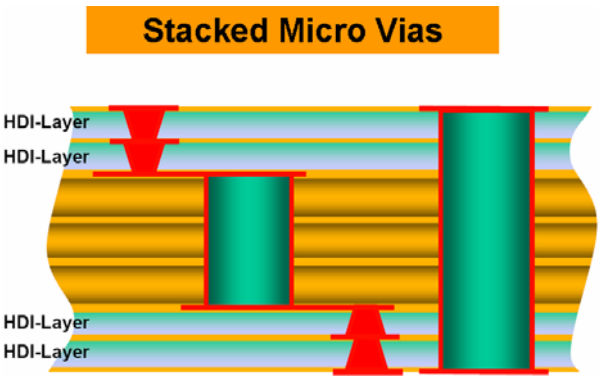


Figure 6: Stacked Micro Vias



“Double layer” blind via technology is preferred because layer to layer controlled impedance causes Layer 2 to act as the “Ground Plane” or “Reference Plane” to the Layer 1 signals. Layer 3 is typically where the signal must go. Layer 3 can then transition through the rest of the inner signal layers using blind via technology and the layer construction techniques below. This technology is for 0.4, 0.5 and 0.65 pitch BGA components.

Figure 7: Stacked Micro Vias

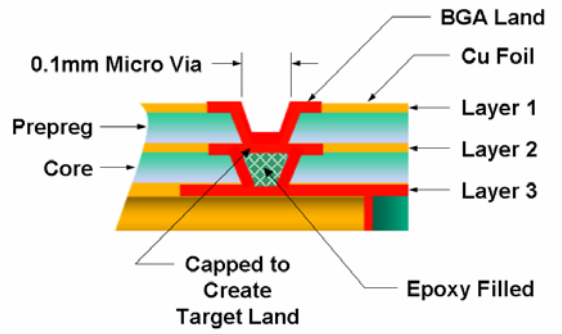
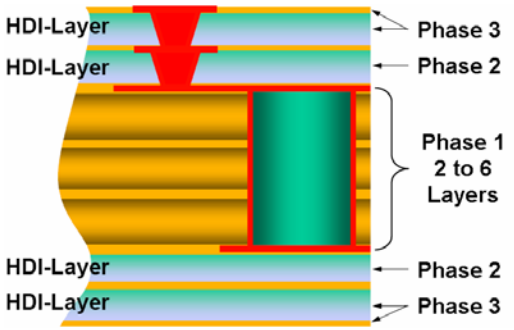


Figure 8: Stacked Micro Vias



Today, the second finest pitch BGA in the industry is 0.5. The 0.075 trace/space is not yet mainstream, but PCB fabrication companies are quickly getting up to speed on this technology.

The two outer rows of a 0.5 and 0.65 pitch BGA are routed to a via fanout on the external layer and blind vias or through vias are only used on the inner rows.\

"Non-collapsing" ball BGA components

Table 3 below is used for land size calculations for non-collapsing BGA balls.

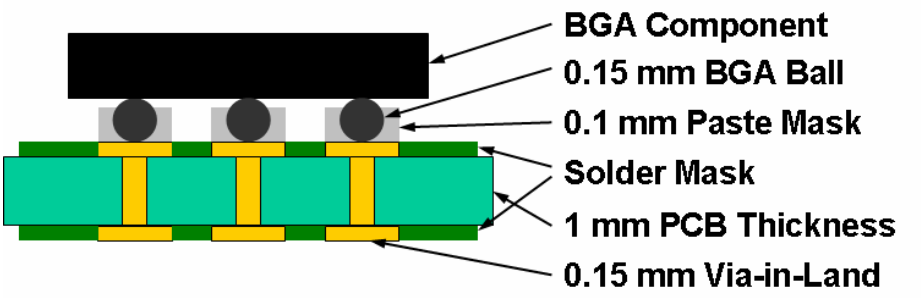
Table 3: Non-Collapsing BGA ball land calculations

Nominal Ball Diameter	Increase	Nominal Land Diameter	Land Variation
0.75	15%	0.85	0.90 - 0.80
0.65	15%	0.75	0.80 - 0.70
0.60	15%	0.70	0.75 - 0.65
0.55	15%	0.65	0.70 - 0.60
0.50	10%	0.55	0.60 - 0.50
0.45	10%	0.50	0.55 - 0.45
0.40	10%	0.45	0.50 - 0.40
0.35	10%	0.40	0.45 - 0.35
0.30	10%	0.35	0.40 - 0.30
0.25	10%	0.30	0.35 - 0.25
0.20	5%	0.21	0.26 - 0.16
0.17	5%	0.18	0.22 - 0.13
0.15	5%	0.16	0.21 - 0.11

It is very important to note that IPC prefers the Maximum Material Condition for all BGA Land Sizes, meaning that the Maximum Land Variation Diameter **is** used; the Nominal Land Diameter is not.

Figure 9 is a 0.5 pitch non-collapsing BGA ball. Instead of shrinking, the non-collapsing land size gets larger to handle the solder volume that creates the solder joint. This technology is new to the electronics industry and was created as a solution for lead free BGA balls.

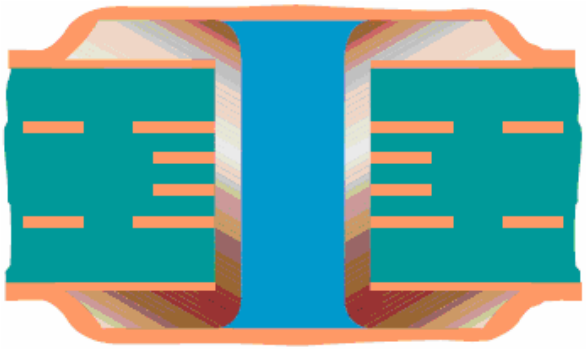
Figure 9: Non-Collapsing 0.5 mm pitch BGA



Via-in-Land Technology	Trace/Space & Grid Data
BGA Ball Size: 0.15	Trace Width: 0.075
BGA Land Dia: 0.275	Trace/Trace Space: 0.075
Hole Size: 0.15	Trace/Via Space: 0.075
Thermal Relief Required	Trace/BGA Land: 0.075
Plane Clearance: 0.425	Routing Grid: 0.05
Solder Mask: 1:1 scale	Part Place Grid: 1

Figure 10 is a **Filled and Capped Via (Type VII Via) - A Type V via with a secondary metallized coating covering the via.** The metallization is on both sides. This technique is designed for future Via-in-Land technology for 0.4 and 0.5 pitch and current 0.65 pitch BGA devices when a through-hole in BGA land is used.

Figure 10: Plated, Filled and Capped BGA Land



When using Via-in-Land technology, solder mask is defined 1:1 scale on the BGA side of the PCB and Tented or covered with solder mask on the opposite side to protect the routed trace. However you could use 1:1 scale solder mask on both sides if you need to use the bottom side for a test fixture.

Solder mask defined land is used for 0.4, 0.5 and 0.65 pitch BGA parts when trace routing is done on the same layer as the BGA land. The solder mask defined BGA land is only recommended when traces need to be protected from exposure and to avoid short circuiting with the BGA land. Also, if outer layer routing can be avoided, it's best to use the "non-solder mask defined" BGA technology to allow the BGA ball to collapse around the land. See Figures 11, 12 and 13 for the various solder lands for BGA components.

Figure 11: Solder Lands for BGA Components

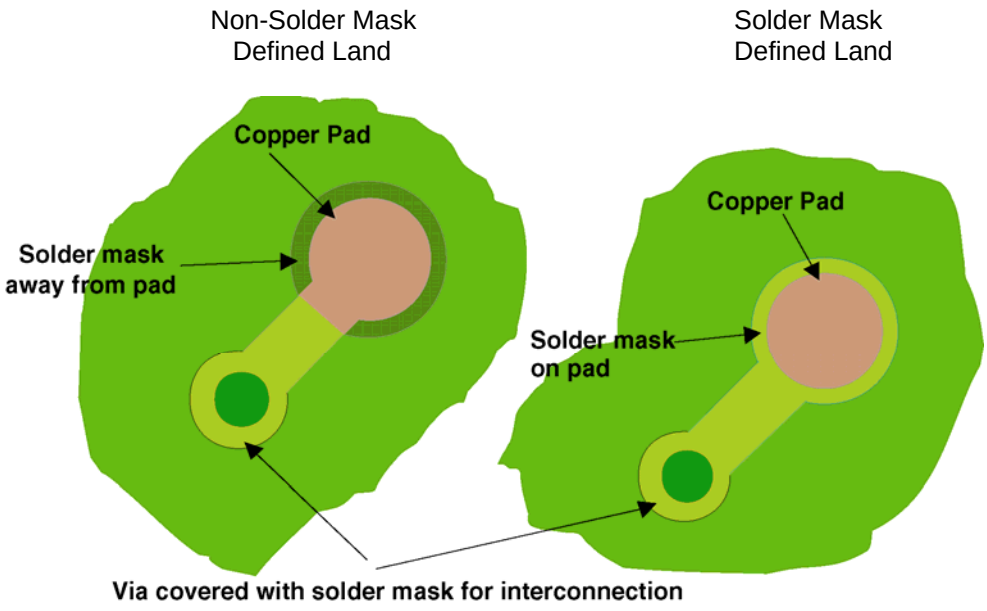


Figure 12: Top View of land illustrating increase of effective land diameter due to trace connections

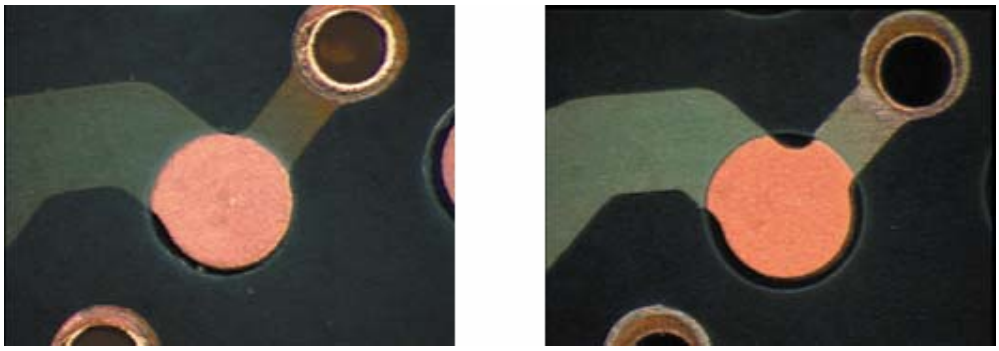
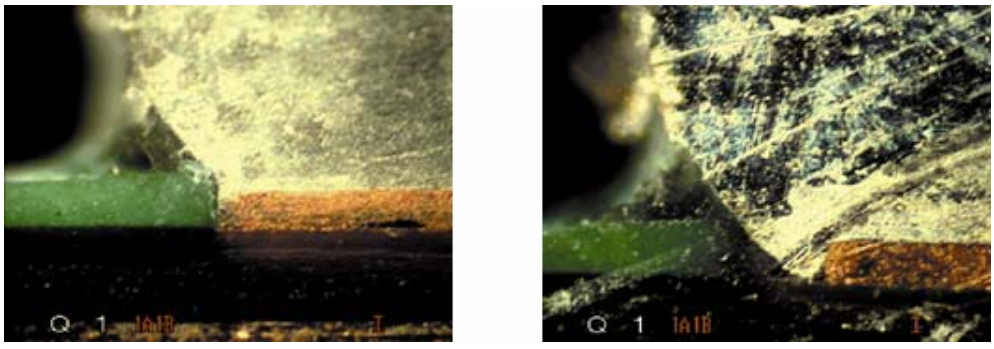


Figure 13: Cross-sectional view of land with solder ball joint illustrating the solder wetting down the edge of the land with solder mask relief away from the land edge



The next group of BGA components is 0.8 and 1.0 pitch. These components can fan out to a via placed between the BGA lands. This fanout is the “dog bone fanout” because it looks like a dog bone with nubs on each end. Table 4 lists the via size, hole size, trace width and routing grid for best routing results. Figures 14 and 15 illustrate one and two track technology between vias.

Table 4: BGA Technology Chart for 0.8 mm and 1 mm pitch BGA parts. All dimensions in millimeters.

BGA Pin Pitch	BGA Ball Dia	BGA Land Size	Via Pad Size	Via Hole Size	Plane Clearance	Trace Width	Trace/ Trace Space	Trace/ Via Space	Route Grid	Via Grid	Part Place Grid
0.8	0.5	0.45	0.5	0.25	0.7	0.1	0.1	0.125	0.1	0.2	1
0.8	0.5	0.45	0.45	0.2	0.65	0.125	0.125	0.1	0.05	0.2	1
1	0.6	0.5	0.5	0.25	0.7	0.1	0.1	0.1	0.1	0.5	0.5
1	0.6	0.5	0.55	0.25	0.75	0.125	0.125	0.16	0.05	0.5	0.5
1	0.6	0.5	0.375	0.175	0.625	0.125	0.125	0.125	0.05	0.5	0.5
1	0.6	0.5	0.55	0.25	0.75	0.15	0.15	0.15	0.05	0.5	0.5
1	0.6	0.5	0.5	0.25	0.7	0.2	0.2	0.15	0.1	0.5	0.5

Figure 14: Single Trace Between Vias

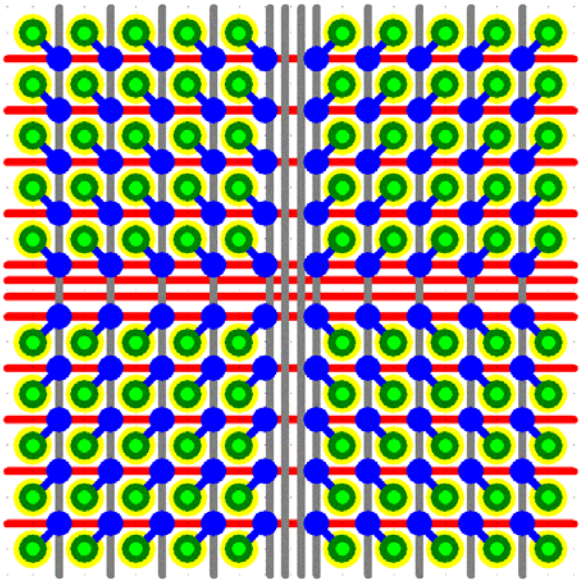
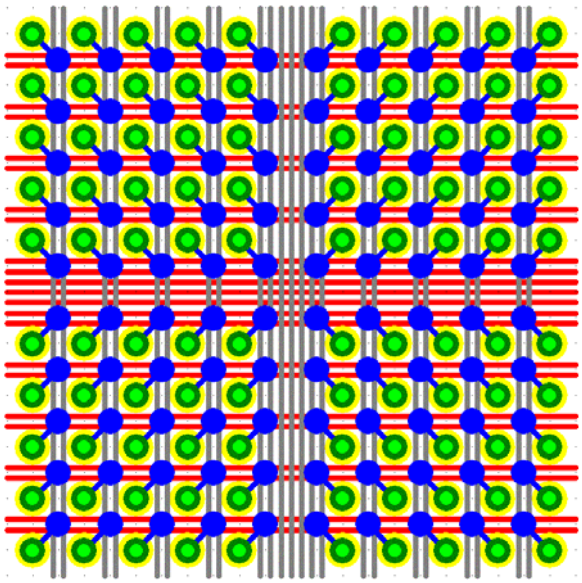


Figure 15: Double Trace Between Vias



The IPC-7351A LP Calculator has a BGA via calculator that helps PCB designers accurately calculate the trace width, trace space, via pad, hole size and plane clearance. The plane clearance is extremely important because it removes copper from ground planes. Ground planes are used for return paths for all transmission lines. If the plane clearance encroaches under a trace, the return path will find an alternate route to return to the source. Having clean reference plane return paths produces the fastest and quietest PC boards. By calculating the via hole plane clearance size, the minimum copper-to-hole annular ring can be determined and this value is derived by the PCB manufacturer. Fewer layers (4 to 6 layers) and thinner PCB material may have a smaller plane clearance than multi-layer (8 – 20 layers) thick boards.

High speed PCB layouts require layer-to-layer controlled impedance. Differential impedance is typically 100 ohms and Single Ended transmission line impedance is typically 50 – 60 ohms. The primary goal is to keep all the traces on a 0.05 routing grid and adjust the trace width accordingly for proper impedance values. Figures 16 and 17 illustrate the 0.2 trace pitch; 0.05 and 0.1 are perfect snap grid solutions for signal routing. You will achieve better routing results when the traces snap to a grid.

Figure 16: Controlled Impedance Differential Pairs for 1 mm pitch BGA

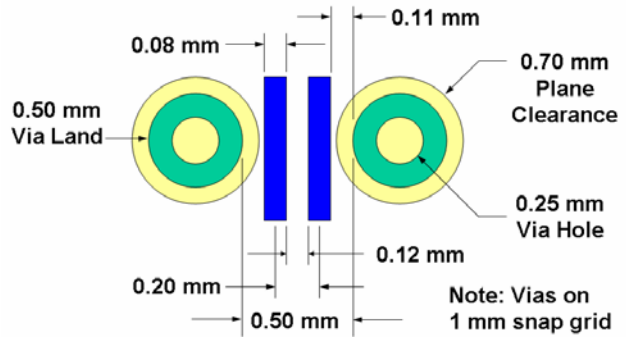
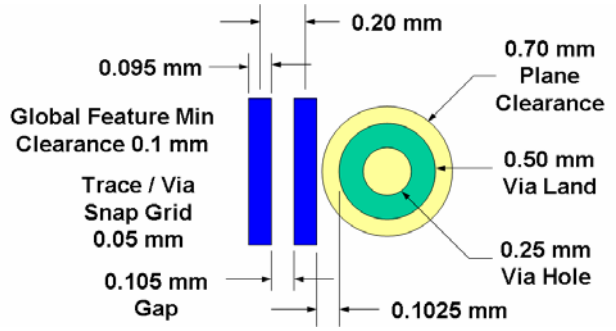


Figure 17: Controlled Impedance Single Ended Traces for 1 mm pitch BGA



Metric “snap grids” that produce the best part placement, via fanout and trace routing results should evenly divisible into 1 mm. Table 5 lists good and bad snap grids.

Table 5: Good and Bad Metric Snap Grids

Good Metric Snap Grids	Bad Metric Snap Grids
1 mm	0.9 mm
0.5 mm	0.8 mm
0.25 mm	0.7 mm
0.2 mm	0.6 mm
0.125 mm	0.4 mm
0.1 mm	0.3 mm
0.05 mm	0.15 mm

There are optimized via padstacks that go with certain trace / space technologies. Table 6 illustrates the optimum via padstack data for the 3 most popular trace widths – 0.1, 0.125 & 0.15 mm.

Table 6: Optimal Via Padstacks

0.1 Trace Width 0.1 Route Grid	0.125 Trace Width 0.05 Route Grid	0.15 Trace Width 0.05 Route Grid
Pad Size: 0.5	Pad Size: 0.65	Pad Size: 0.55
Hole Size: 0.25	Hole Size: 0.3	Hole Size: 0.25
Plane Clearance: 0.7	Plane Clearance: 0.8	Plane Clearance: 0.75

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Conclusion: Using a metric placement and routing grids and metric trace widths are far superior and easier to work with than Imperial unit dimensions. Also, working with a trace route snap grid is much easier to work with rather than using shape based "gridless" routing solutions. This is especially true when your CAD library uses 0.05 as the base units for all CAD library land size calculation round-offs. Clean use of metric unit technology throughout the CAD database environment renders the shape based theory obsolete. When PCB designers finally discover that working with metric unit's increases performance and overall quality they will be asking themselves "What took me so long to transition to the metric SI measurement system?"

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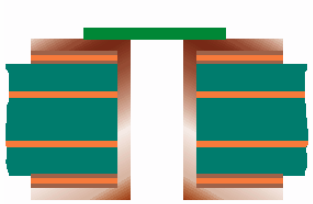
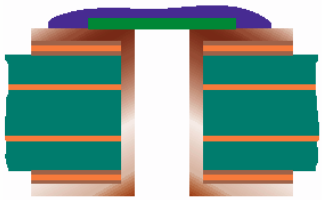
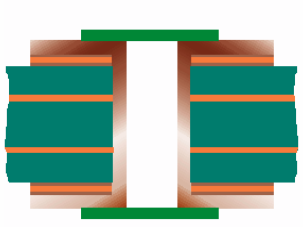
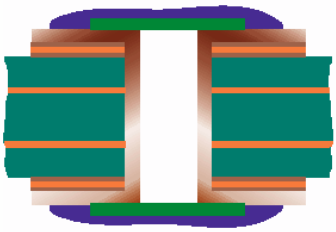
Optional Material:

Tented, Plugged, and Filled Vias

TYPE I – TENTED		TYPE II – TENTED AND COVERED	
Tented Via (Type 1 Via) - A via with a mask material (typically dry film) applied bridging over the via wherein no additional materials are in the hole. It may be applied to one side or both		Tented and Covered Via (Type II Via) - A Type I via with a secondary covering of mask material applied over the tented via.	
A via covered with dry film solder mask; the via is not filled. When tenting from both sides there may be issues with trapped air that expands during mass soldering.		A via covered with dry film and the LPI solder mask; the via is not filled. Just like Type 1 when tenting from both sides there may be issues with trapped air that expands during mass soldering.	

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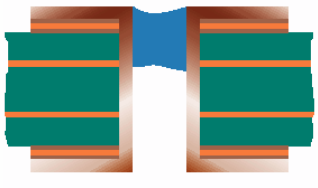
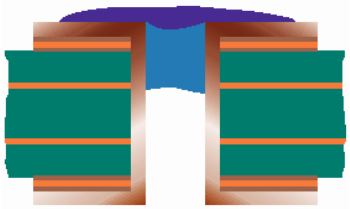
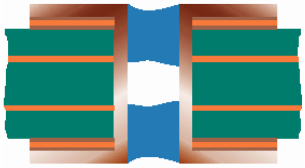
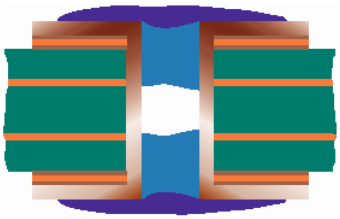
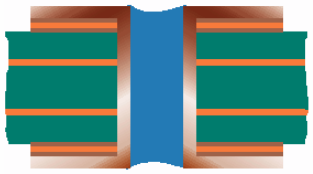
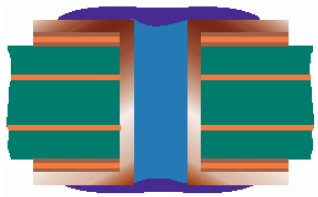
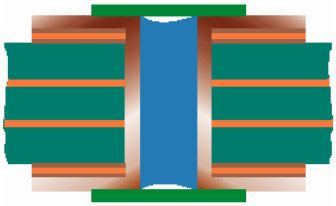
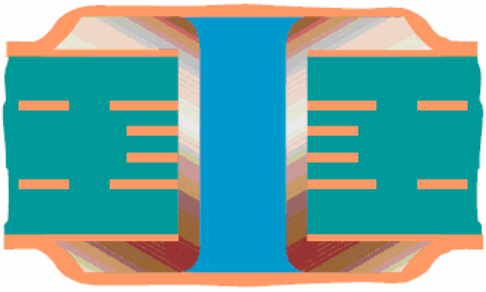
TYPE III – PLUGGED		TYPE IV – PLUGGED AND COVERED	
Plugged Via (Type III Via) - A via with material applied allowing partial penetration into the via. It may be applied from either side		Plugged and Covered Via (Type IV Via) - A Type III via with a secondary covering of material applied over the via.	
During solder mask application the via is flooded with solder mask. The via is partially filled. Chemical entrapment is a major concern.		An additional operation which is done independent of solder mask application on one or both sides of the via. The via is partially filled.	

TYPE V – FILLED		TYPE VI – FILLED AND COVERED	
Filled Via (Type V Via) - A via with material applied into the via targeting a full penetration and encapsulation of the hole An additional operation which is done independent of solder mask application. The via is filled with a non-conductive material.		Filled and Covered Via (Type VI Via) - A Type V via with a secondary covering of material (liquid or dry film solder mask) applied over the via. It may be applied from either one side or both sides.	 

Filled and Capped Vias

TYPE VII – FILLED AND CAPPED	
Filled and Capped Via (Type VII Via) - A Type V via with a secondary metallized coating covering the via. The metallization is on both sides. This technique is used for Via-in-pad technology for 0.8, 0.75, 0.65, 0.5 and 0.4 mm BGA pitch devices.	

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