



ON Semiconductor®

The Dark Side of Flyback Converters

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Course Agenda

- The Flyback Converter
- The Parasitic Elements
- How These Parasitics Affect your Design?
- Current-Mode is the Most Popular Scheme
- Fixed or Variable Frequency?
- More Power than Needed
- The Frequency Response
- Compensating With the TL431

What is the Subject?

- ❑ There has been numerous seminars on Flyback converters
- ❑ Seminars are usually highly theoretical – link to the market?
- ❑ Industrial requirements usually not covered: standby, over power...
- ❑ This 3-hour seminar will shed lights on less covered topics:
 - ❖ Why the converter delivers more power than expected? Solutions?
 - ❖ Books talk about compensation with op amps, I have a TL431!
 - ❖ The origin of the Right-Half Plane Zero, how do I deal with it?
 - ❖ Quasi-resonant converters presence increases, how do they work?
- In a 3-hour course, we are just scratching the surface...!

The Flyback, a Popular Structure

- ❑ The flyback converter is widely used in consumer products
- ✓ Ease of design, low-cost, well-known structure
- Poor EMI signature, bulky transformer, practical up to 150 W



DVD player
Set-top box

flyback $\approx 10 - 35$ W



Charger

flyback $\approx 3 - 5$ W



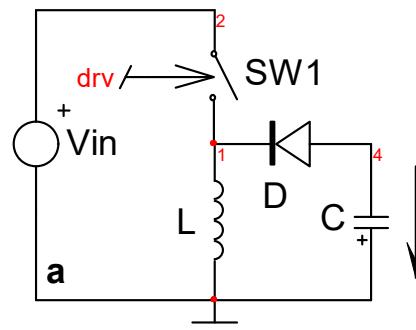
Notebook
Netbook

flyback $\approx 40 - 180$ W

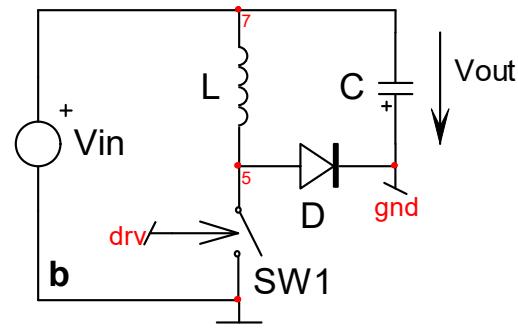


An Isolated Buck-Boost

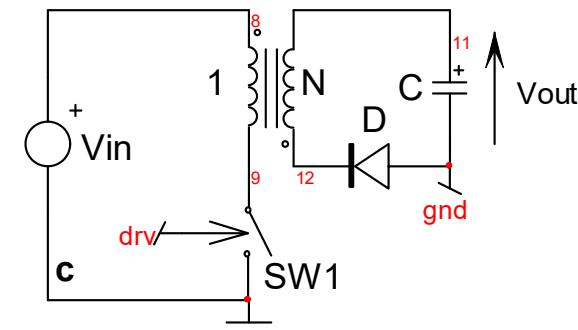
- The flyback converter is derived from the buck-boost cell



buck-boost
ground referenced

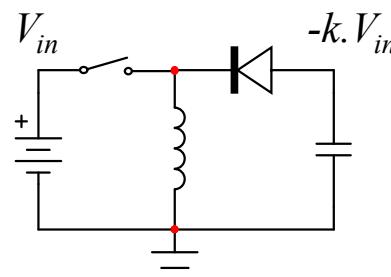


buck-boost
input referenced



flyback
isolated ground referenced

- The addition of a transformer brings:



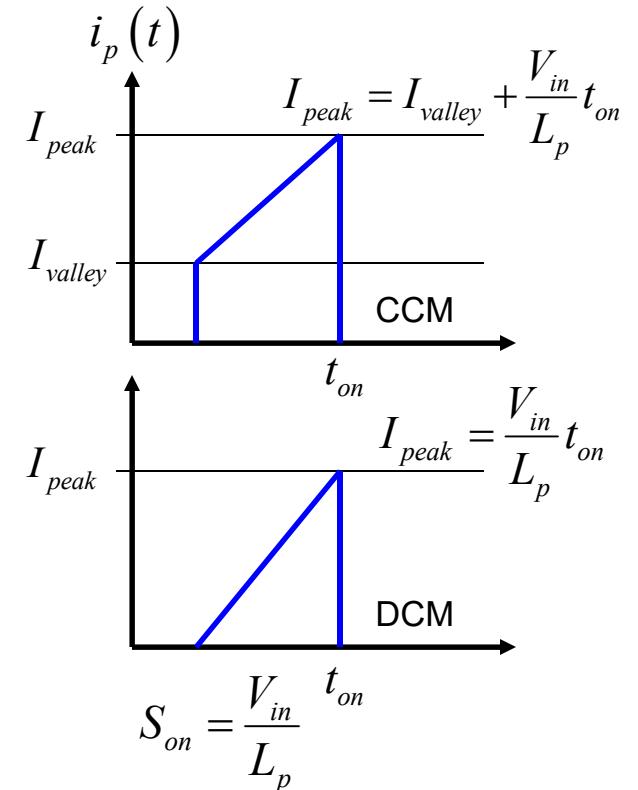
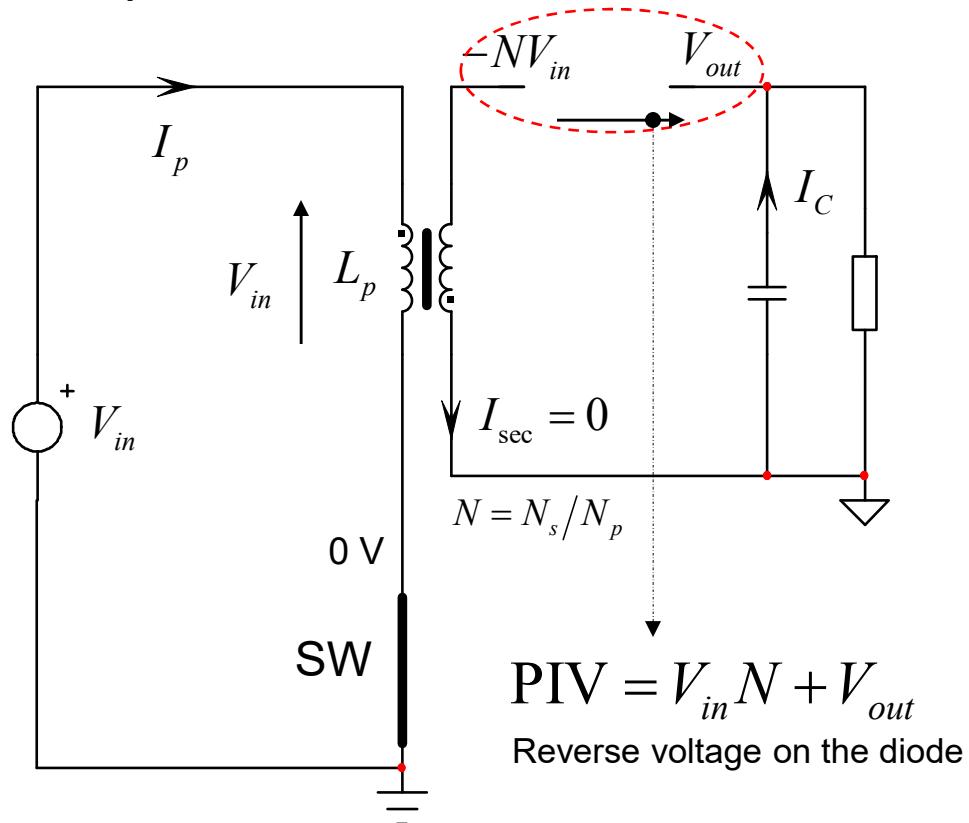
+



- Up or down scale V_{in}
- Isolation
- Polarity change
- More than 1 output

The Turn-on Event

- The power switch turns on: current ramps up in L_p , D is blocked

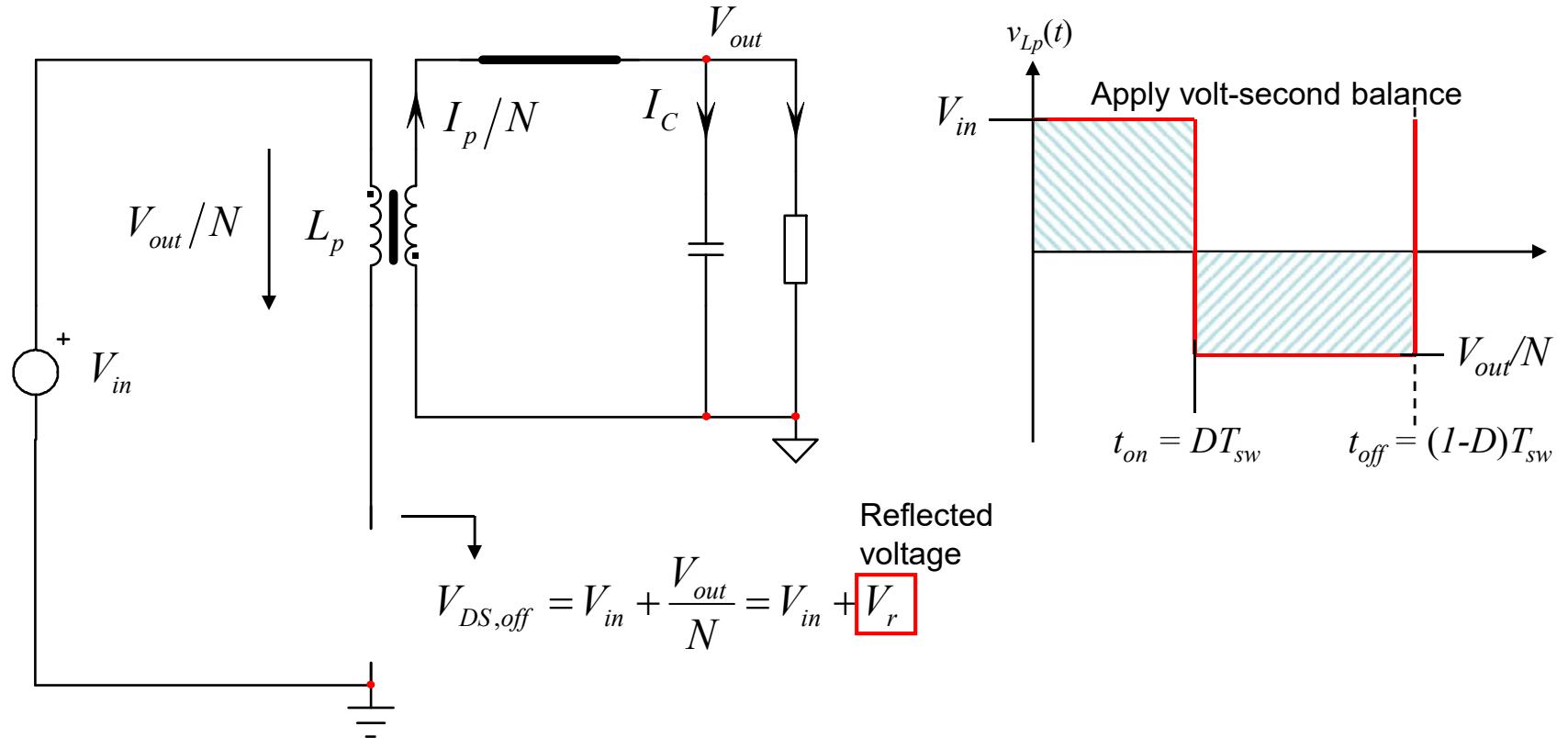


- The current increases in the inductor in relationship to V_{in} and L_p
- The output capacitor supplies the load on its own

Simplified, no leakage

Applying Volt-Second Balance, CCM

- The power switch turns off: D conducts, V_{out} "flies" back

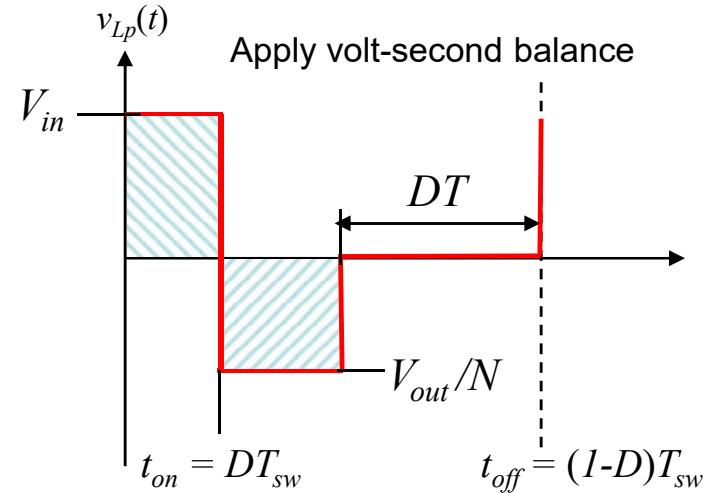
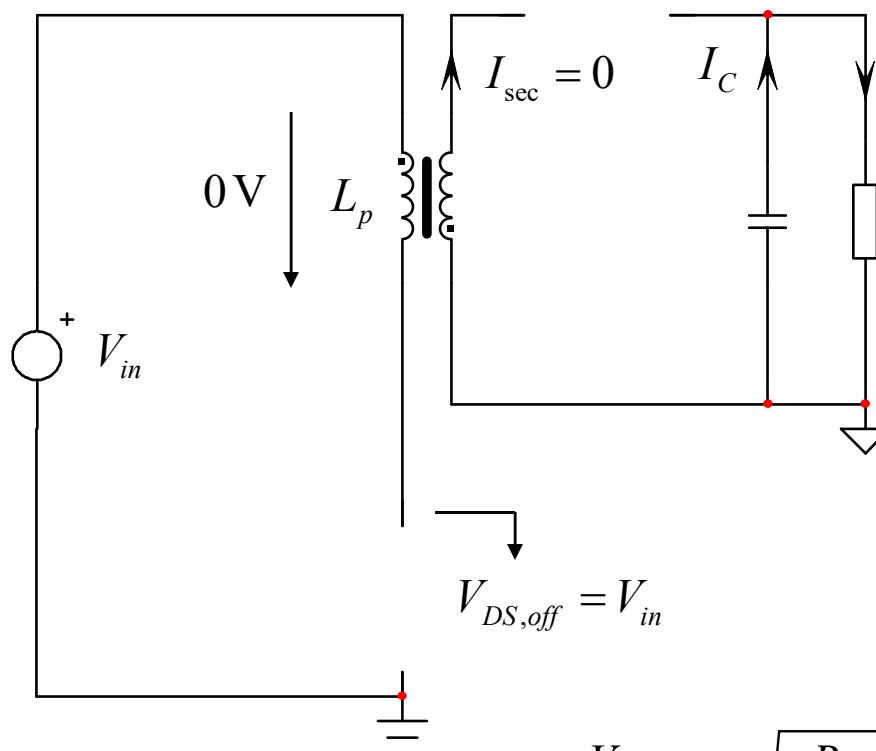


$$\frac{V_{out}}{V_{in}} = \frac{Nt_{on}}{t_{off}} = \frac{NDT_{sw}}{(1-D)T_{sw}} = \frac{ND}{1-D}$$

dc transfer function in CCM

Applying Volt-Second Balance, DCM

- In DCM, when L_p is fully depleted D opens: V_{out} reflection is lost



$$\frac{V_{out}}{V_{in}} = D \sqrt{\frac{R_{load}}{2L_p F_{sw}}}$$

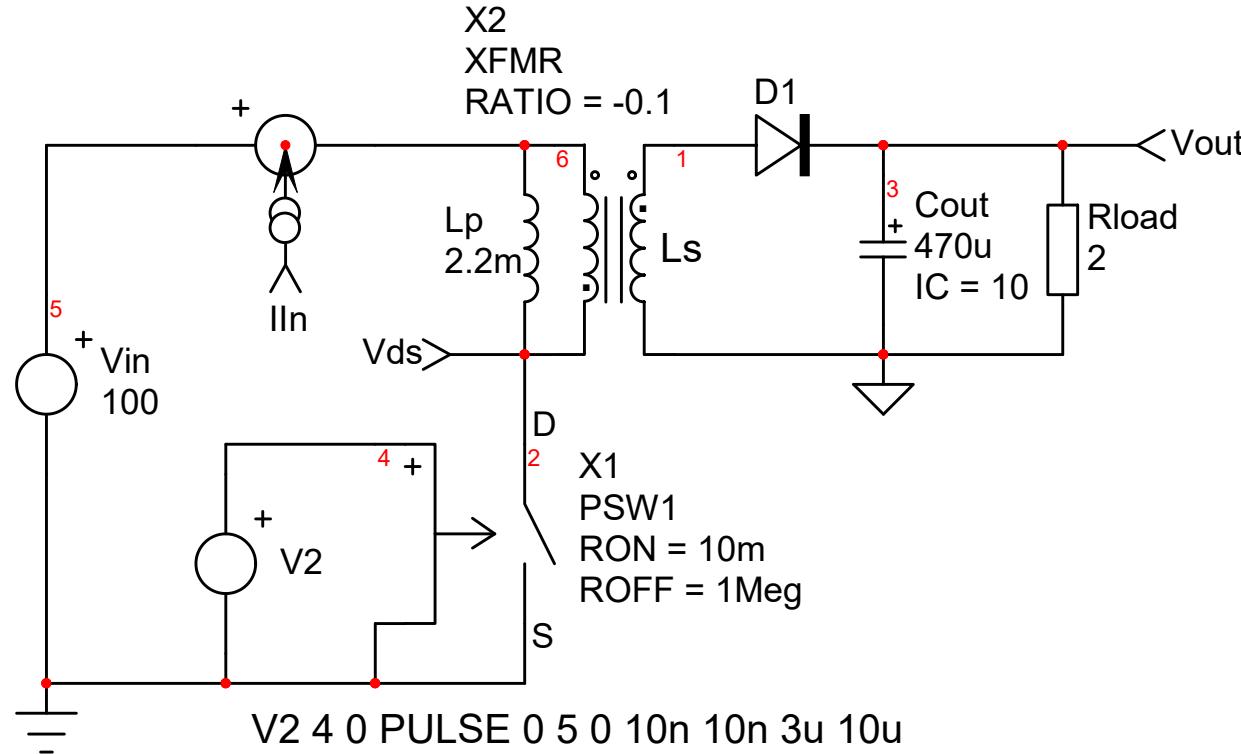
dc transfer function in DCM

From the buck-boost:

$$\frac{V_{out}}{NV_{in}} = D \sqrt{\frac{R_{load}}{2L_p N^2 F_{sw}}}$$

Flyback, Typical Waveforms

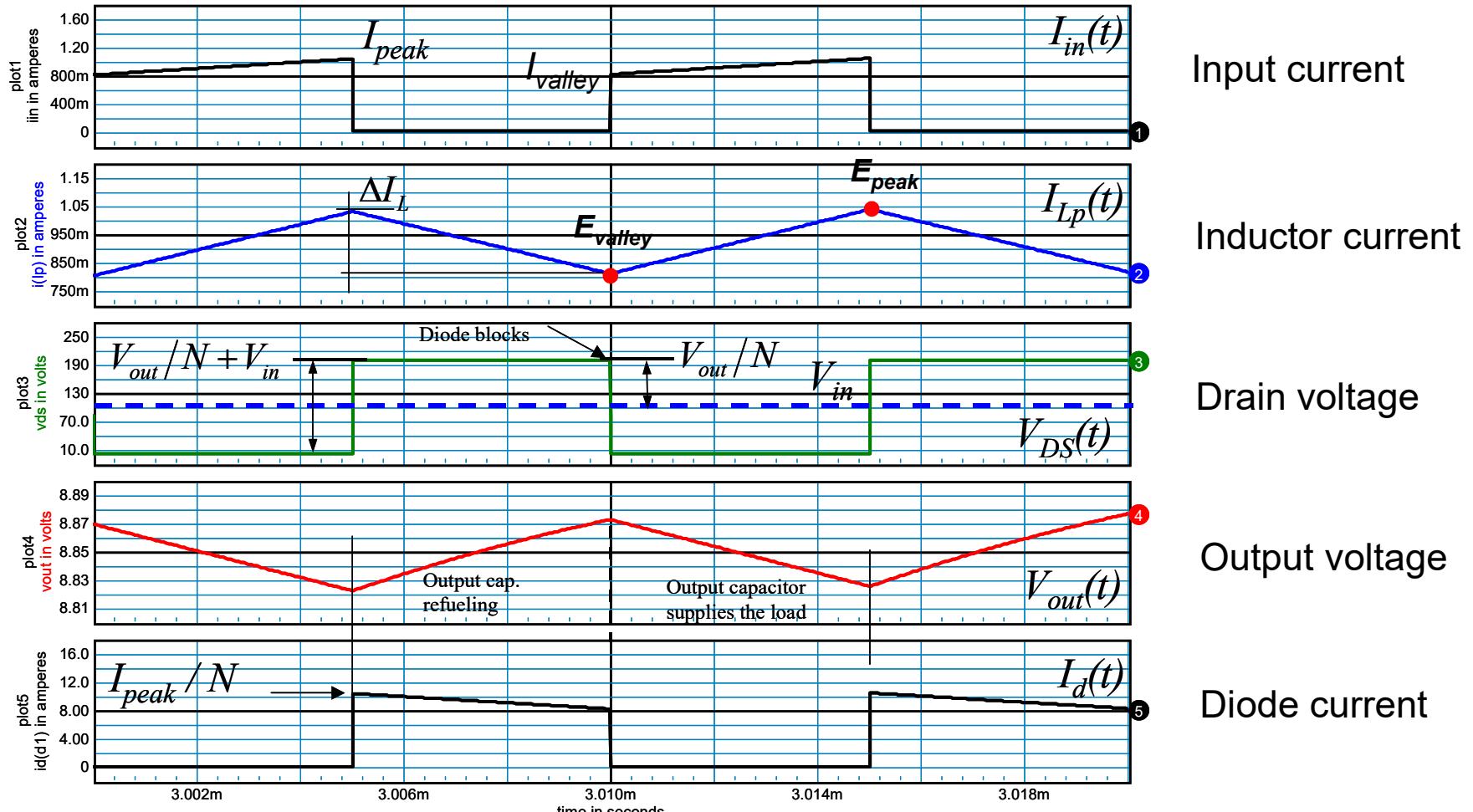
- Below is a simple flyback converter, without parasitics



- It will run open loop for simplicity, $V_{out} \approx 8 \text{ V}$

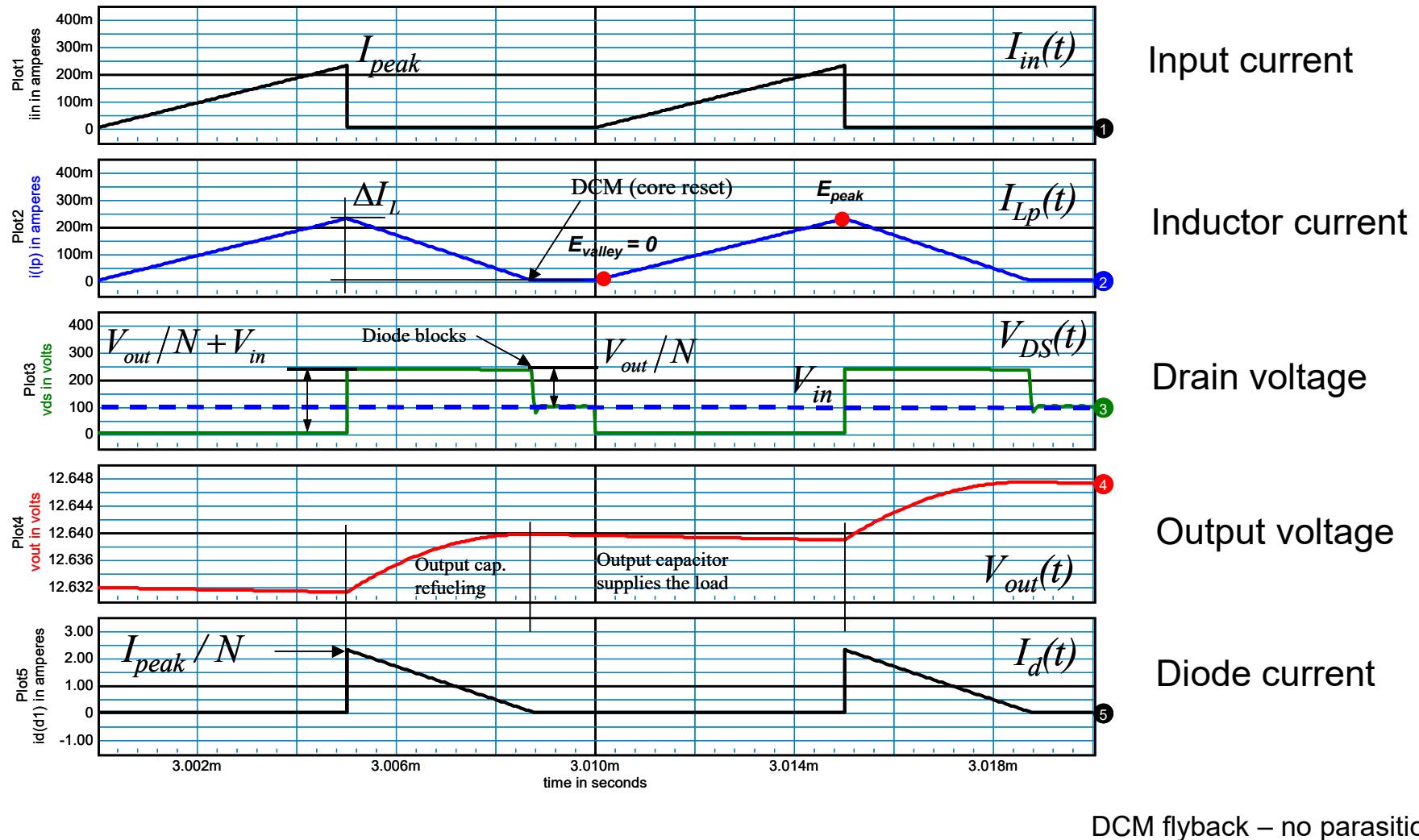
No parasitics

Flyback, Typical Waveforms, CCM



CCM flyback – no parasitics

Flyback, Typical Waveforms, DCM



Energy Transfer in CCM and DCM

- The primary inductance, L_p , stores and releases energy

$$E_{L_p, \text{valley}} = \frac{1}{2} L_p I_{\text{valley}}^2 \quad \text{Initially stored energy}$$

$$E_{L_p, \text{peak}} = \frac{1}{2} L_p I_{\text{peak}}^2 \quad \text{Stored energy at } t_{on}$$

$$E_{L_p, \text{accu}} = \frac{1}{2} L_p I_{\text{peak}}^2 - \frac{1}{2} L_p I_{\text{valley}}^2 = \frac{1}{2} L_p (I_{\text{peak}}^2 - I_{\text{valley}}^2) \quad \text{Accumulated energy at } T_{sw}$$

- Power (W) is energy (J) averaged over time (s):

$$P_{out} = \frac{1}{2} (I_{\text{peak}}^2 - I_{\text{valley}}^2) L_p F_{sw} \eta \quad \begin{matrix} \text{Eta, the efficiency} \\ \text{CCM} \end{matrix}$$

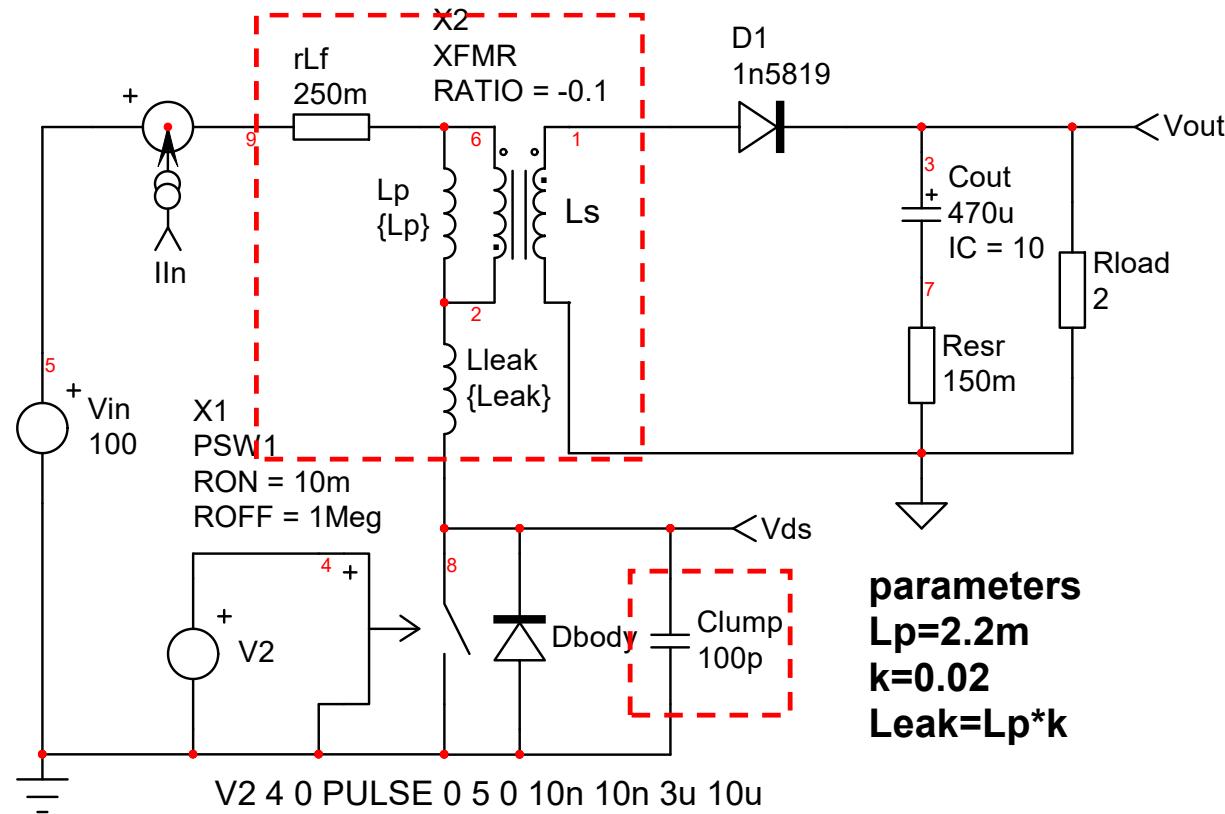
$$P_{out} = \frac{1}{2} I_{\text{peak}}^2 L_p F_{sw} \eta \quad \begin{matrix} \text{DCM, } I_{\text{valley}} = 0 \end{matrix}$$

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 - ❑ How These Parasitics Affect your Design?
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 - ❑ The Frequency Response
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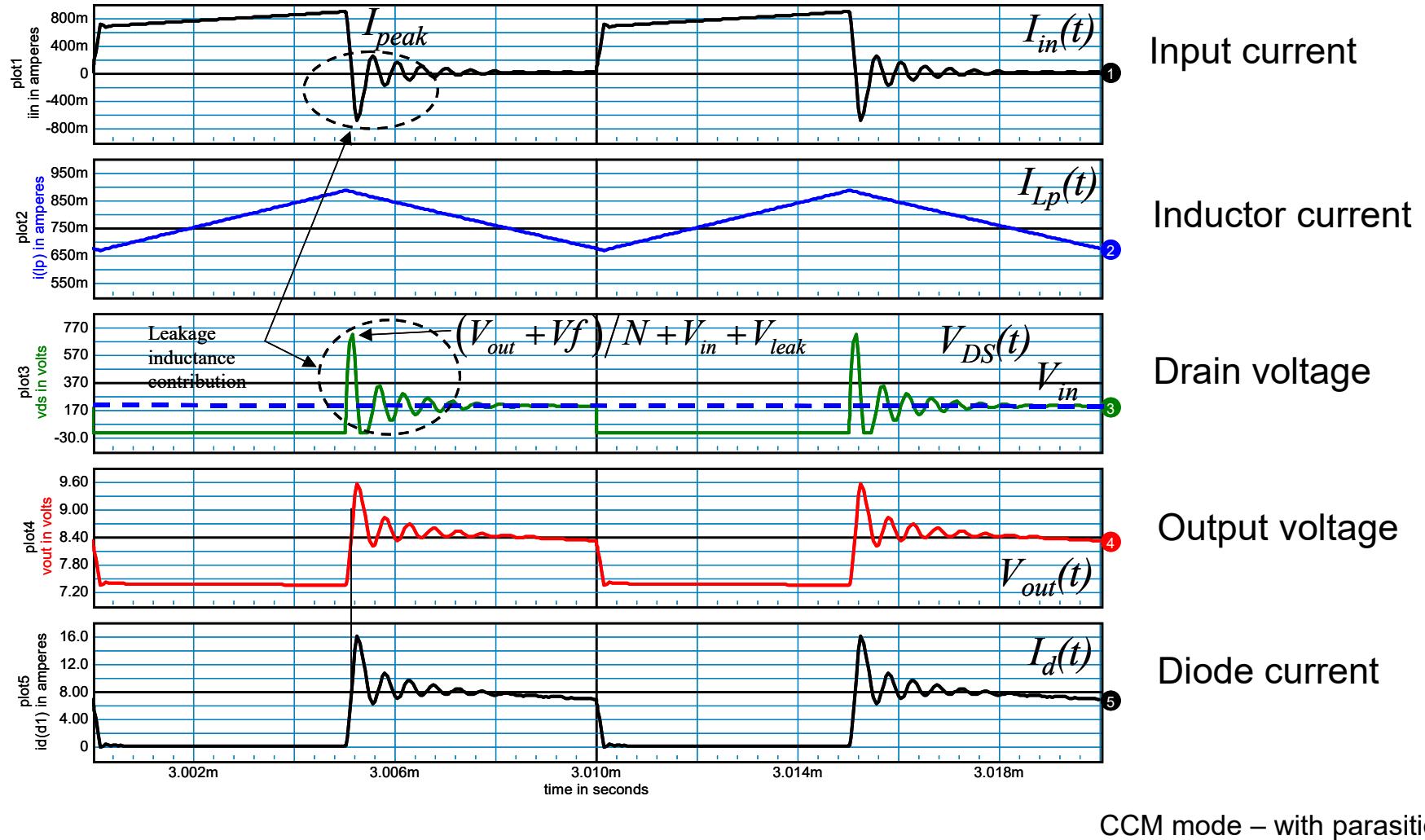
Considering Parasitic Elements

- The transformer and the MOSFET include parasitics

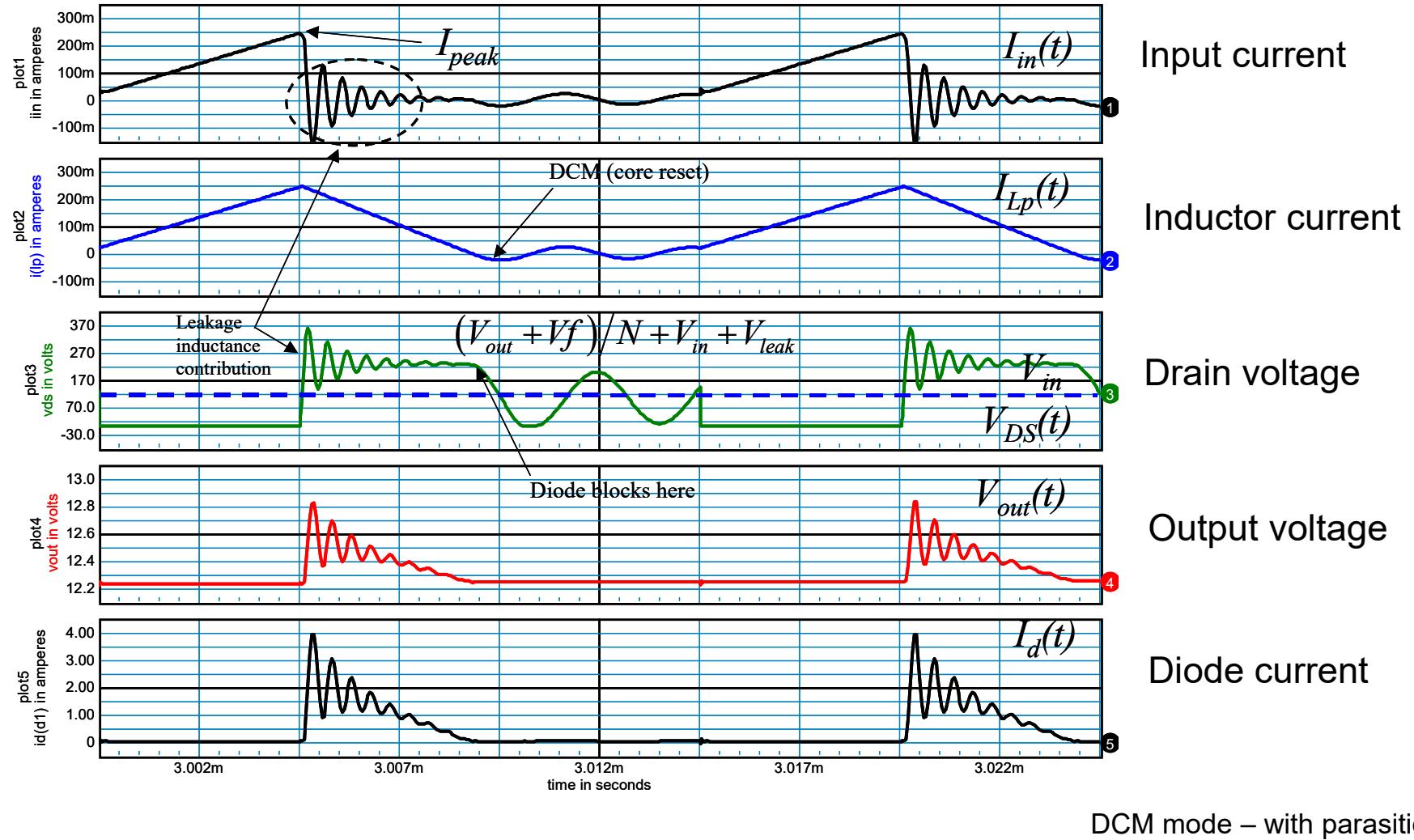


With parasitics

Considering Parasitic Elements, CCM

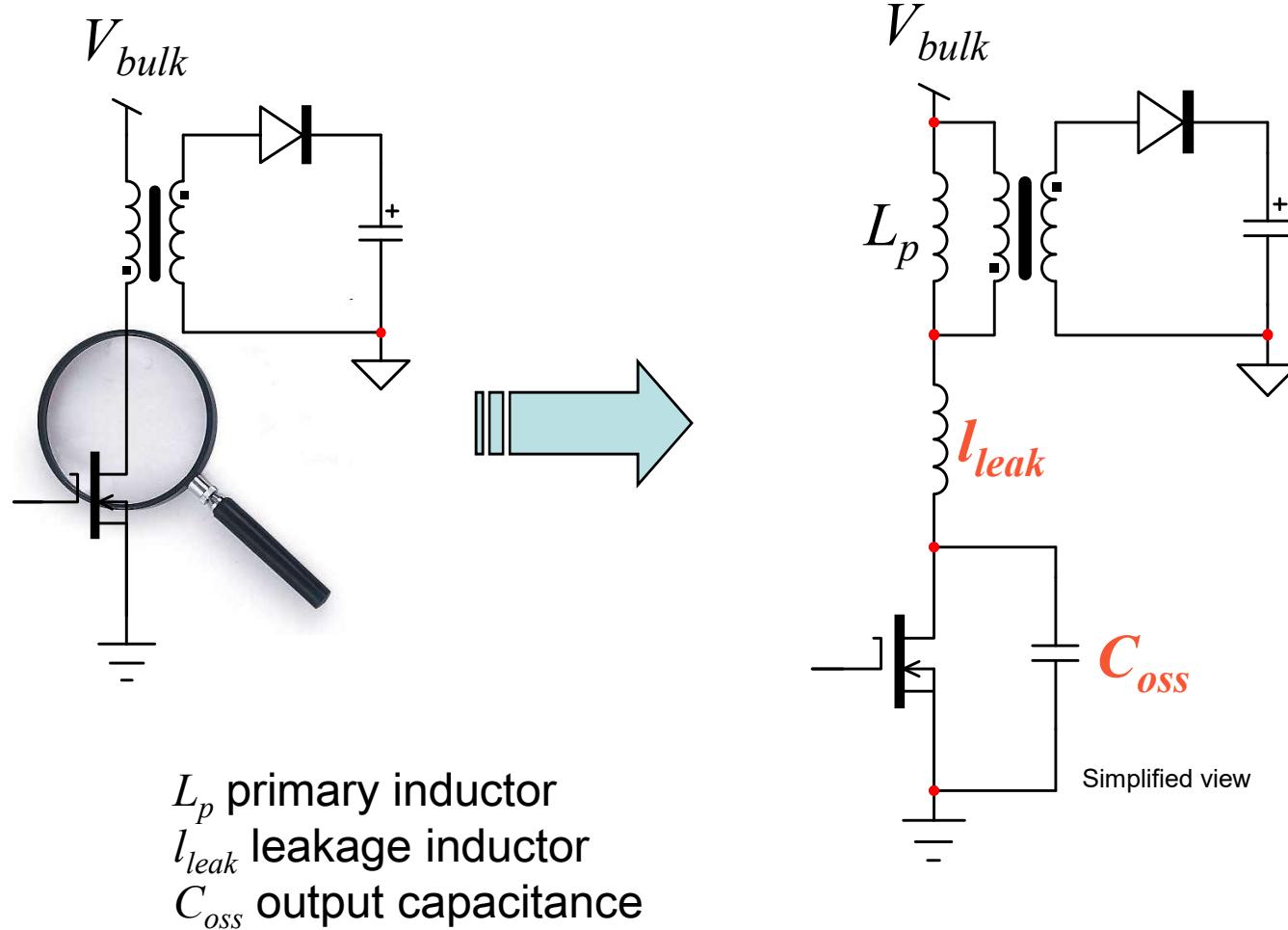


Considering Parasitic Elements, DCM



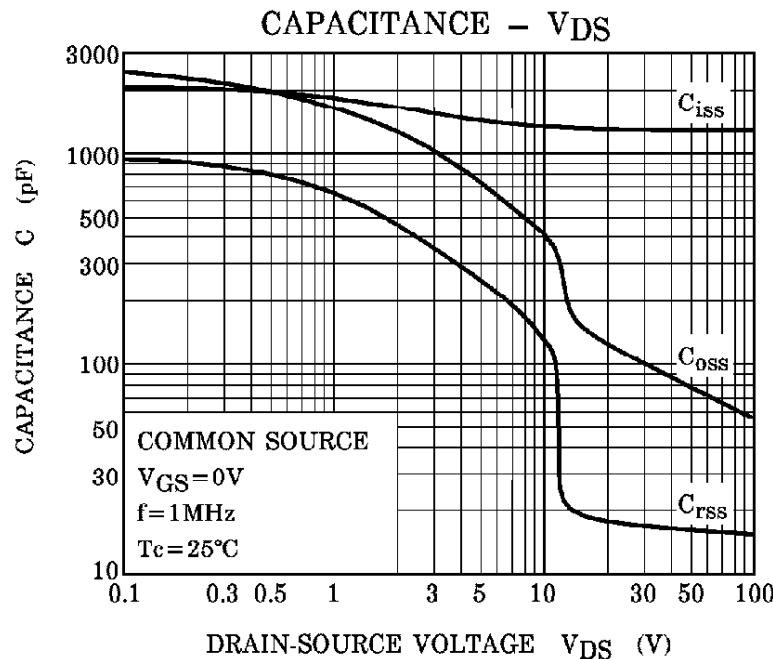
Who Are the Stray Elements?

- The study of the drain node reveals a *LC* network



The MOSFET C_{OSS} is a Non-Linear Device

- The capacitor value changes with its bias voltage



$$C_{OSS}(V_{DS}) = \frac{C_{D0}}{\sqrt{1 + \frac{V_{DS}}{V_0}}}$$

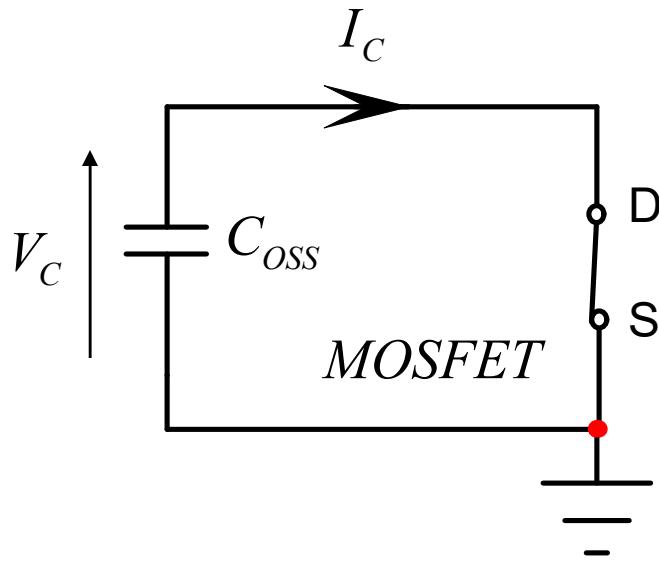
C_{D0} is the cap. for $V_{DS} = V_0$

- As bias affects the capacitor value:

$$W = \frac{1}{2} C_{OSS} V_{DS}^2$$

As the Voltage Decreases, C_{oss} Value Changes

- The brutal discharge generates switching losses



$$I_C(t) = C \frac{dV_C(t)}{dt} \quad W = \int_0^t I_C(t) V_C(t) \cdot dt$$

$$W = \int_0^t C \frac{dV_{DS}(t)}{dt} V_{DS}(t) \cdot dt = \int_0^{V_{DS}} C(V_{DS}) V_{DS} \cdot dV_{DS}$$

$$C_{oss}(V_{DS}) \approx \frac{C_{D0} \sqrt{V_0}}{\sqrt{V_{DS}}}$$

$$W = \frac{2}{3} V_{DS}^{3/2} C_{D0} \sqrt{V_0}$$

↑
At turn-off

- The energy lost is smaller with the non-linear variation!

Using the Raw C_{oss} is an ... Overkill

- Re-compute the capacitor from the MOSFET data-sheet

Input Capacitance	C_{iss}	—	1300	—	pF
Reverse Transfer Capacitance	C_{rss}	$V_{DS} = 10V, V_{GS} = 0V, f = 1MHz$	—	130	
Output Capacitance	C_{oss}	V_{D0}	—	400	

C_{D0}

- The classical equation gives:

$$W = \frac{1}{2} C_{oss} V_{DS}^2 = 0.5 \times 400 \text{ pF} \times 100^2 = 2 \mu\text{J} \quad \text{or } 200 \text{ mW @ 100 kHz}$$

- The updated equation gives:

$$W = \frac{2}{3} V_{DS}^{3/2} C_{D0} \sqrt{V_0} = \frac{2}{3} \times 100^{3/2} \times 400 \text{ pF} \times \sqrt{10} = 843 \text{ nJ}$$

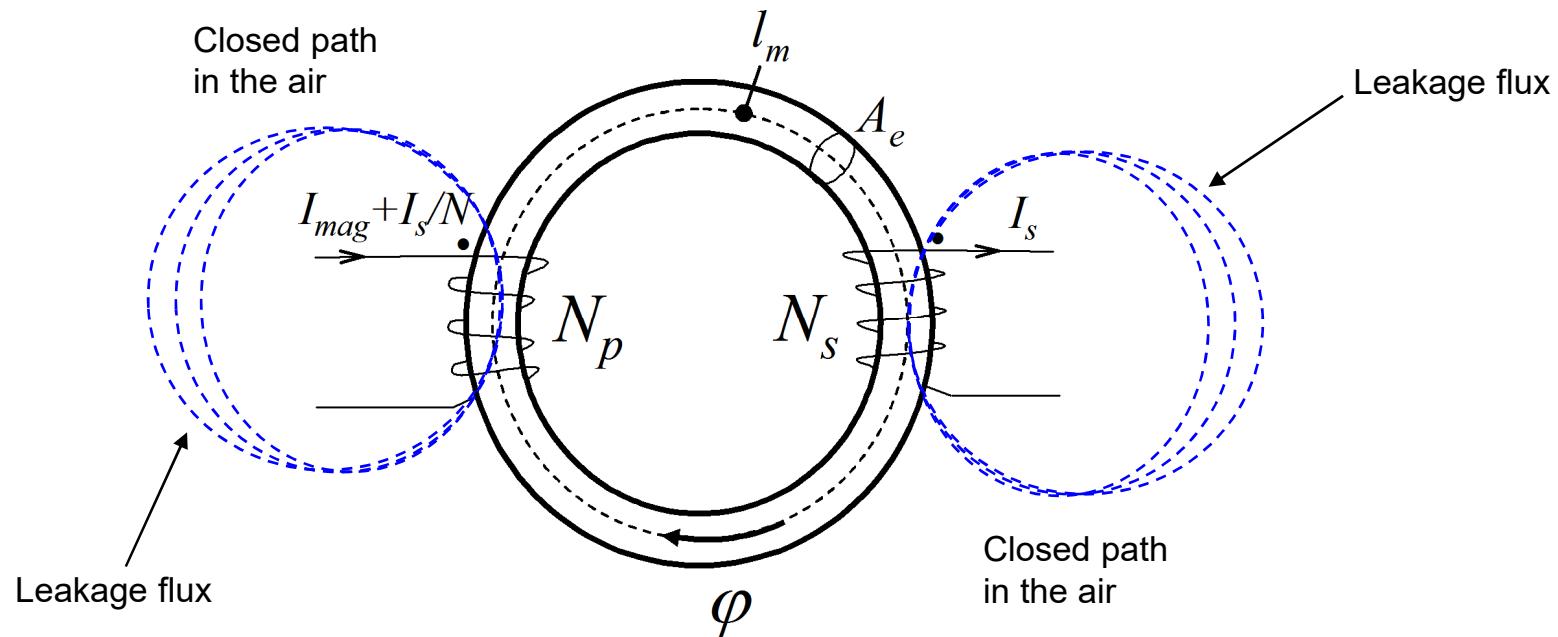
or 84 mW @ 100 kHz = 58% reduction

Overkill



The Leakage Inductance

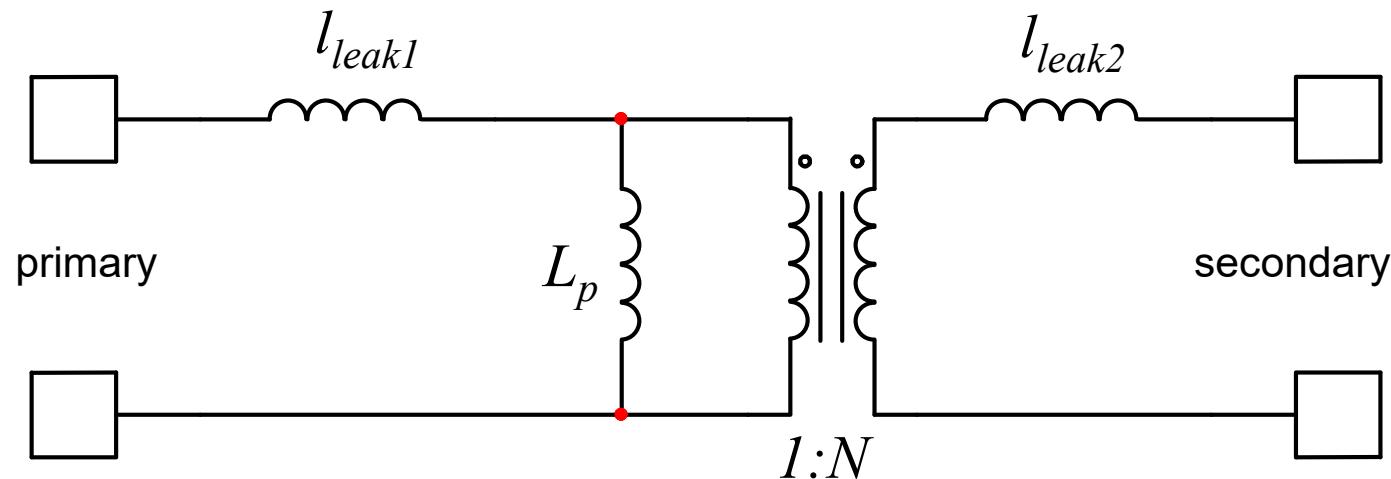
- The coupling in a transformer is not perfect



- Some induction lines couple in the air: leakage flux

An Equivalent Transformer Model

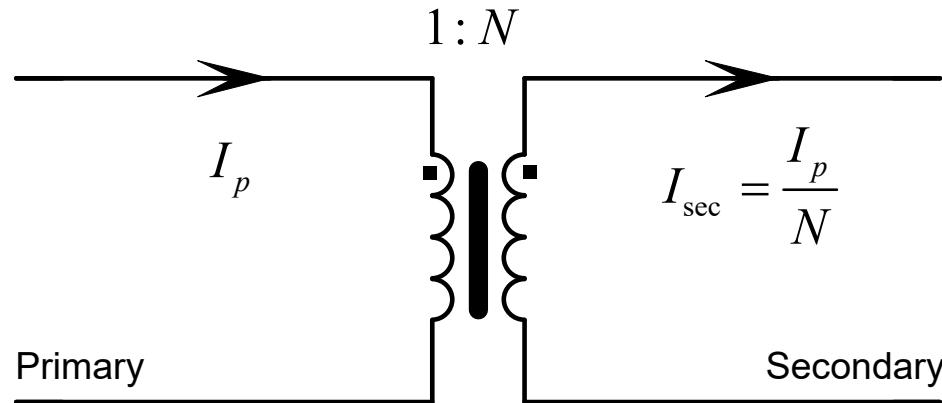
- For a two-winding transformer, the model is simple:
 - ✓ Two leakage inductors
 - ✓ One magnetizing inductor



- This is commonly known as the "PI" model

The Transformer Scales the Primary Current

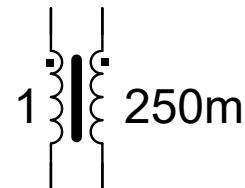
- In a perfect transformer, we have:



- The turns ratio is usually normalized to the primary

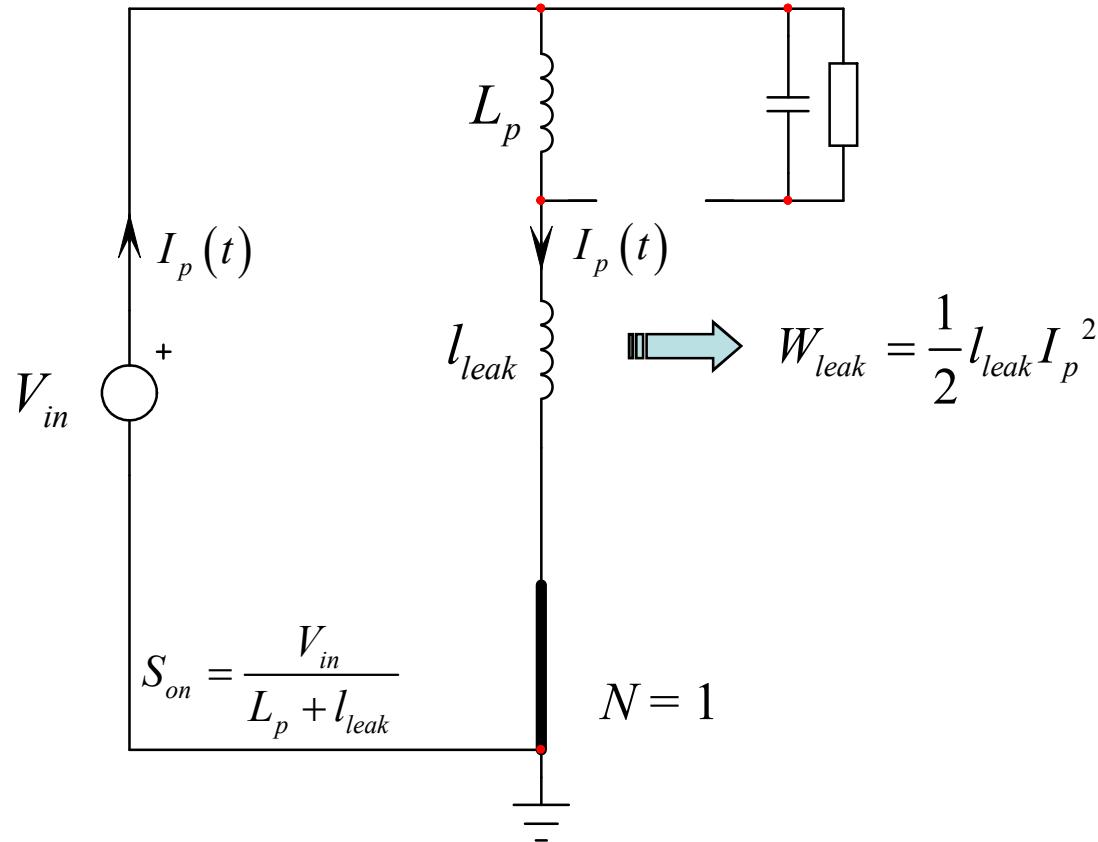
$$N_p : N_s \xrightarrow{\text{Divide by } N_p} \frac{N_p}{N_p} : \frac{N_s}{N_p} \longrightarrow 1:N$$

$$\left. \begin{array}{l} N_p = 100 \\ N_s = 25 \end{array} \right\} 1:0.25$$



The Leakage Term also Stores Energy

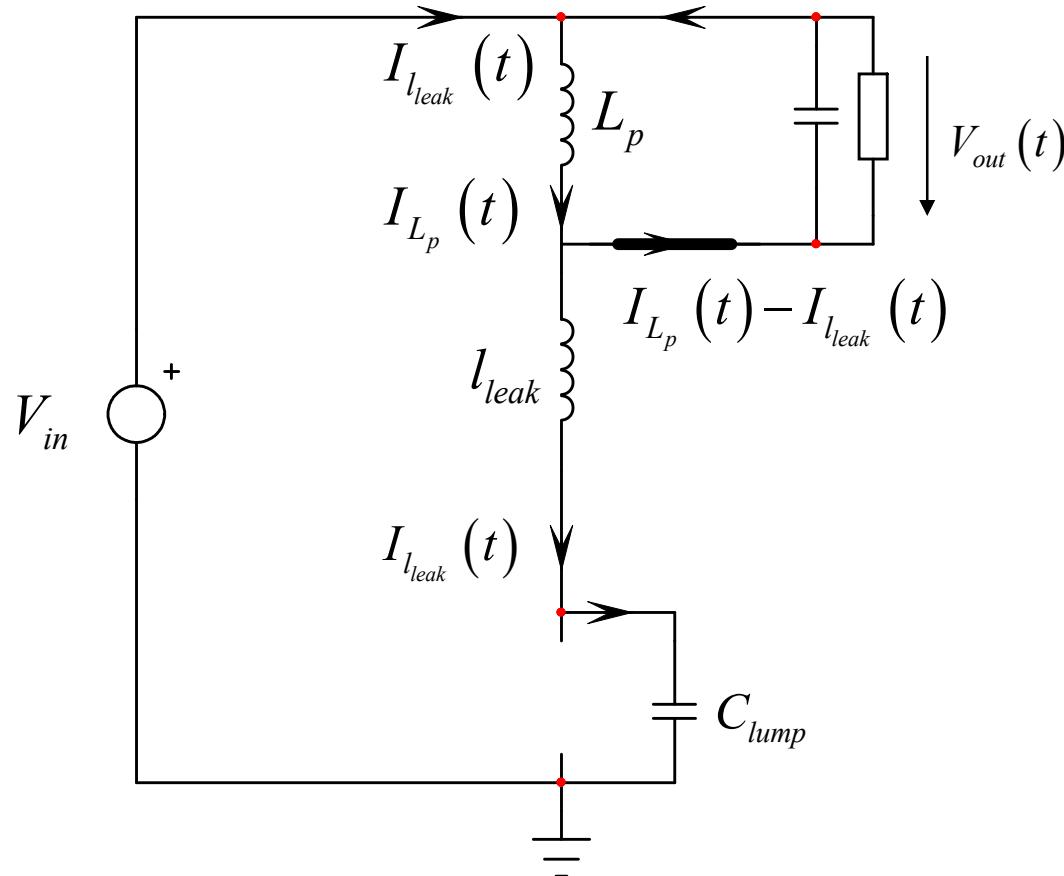
- At turn-on, the primary current flows in both l_{leak} and L_p



- During the on-time, both L_p and l_{leak} store energy

Where does the Current Flow?

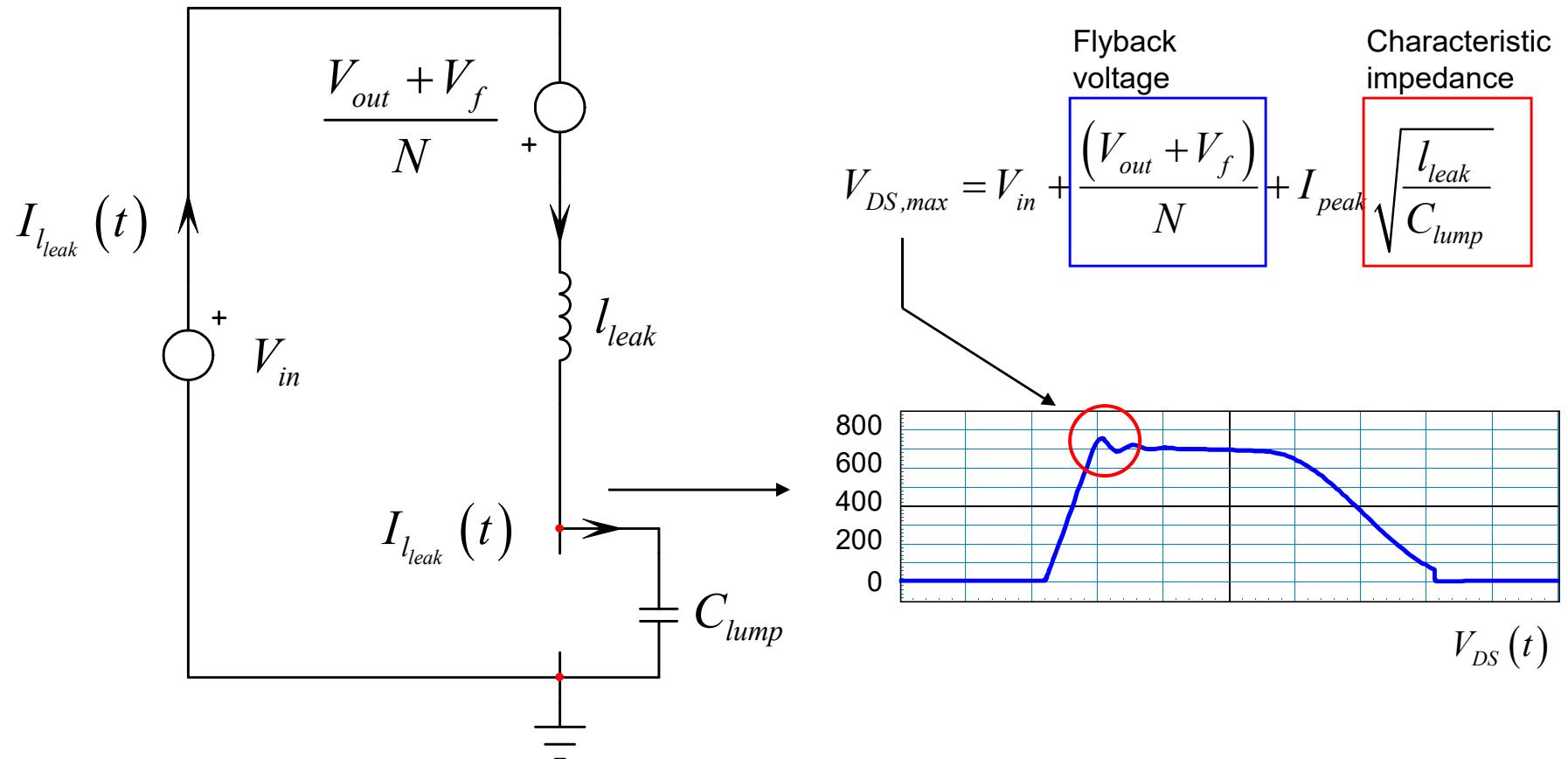
- At turn-off, the energy stored in L_p is dumped in the output cap.



- The leakage inductor current fills up the drain lump capacitor

Watch out for the Maximum Excursion!

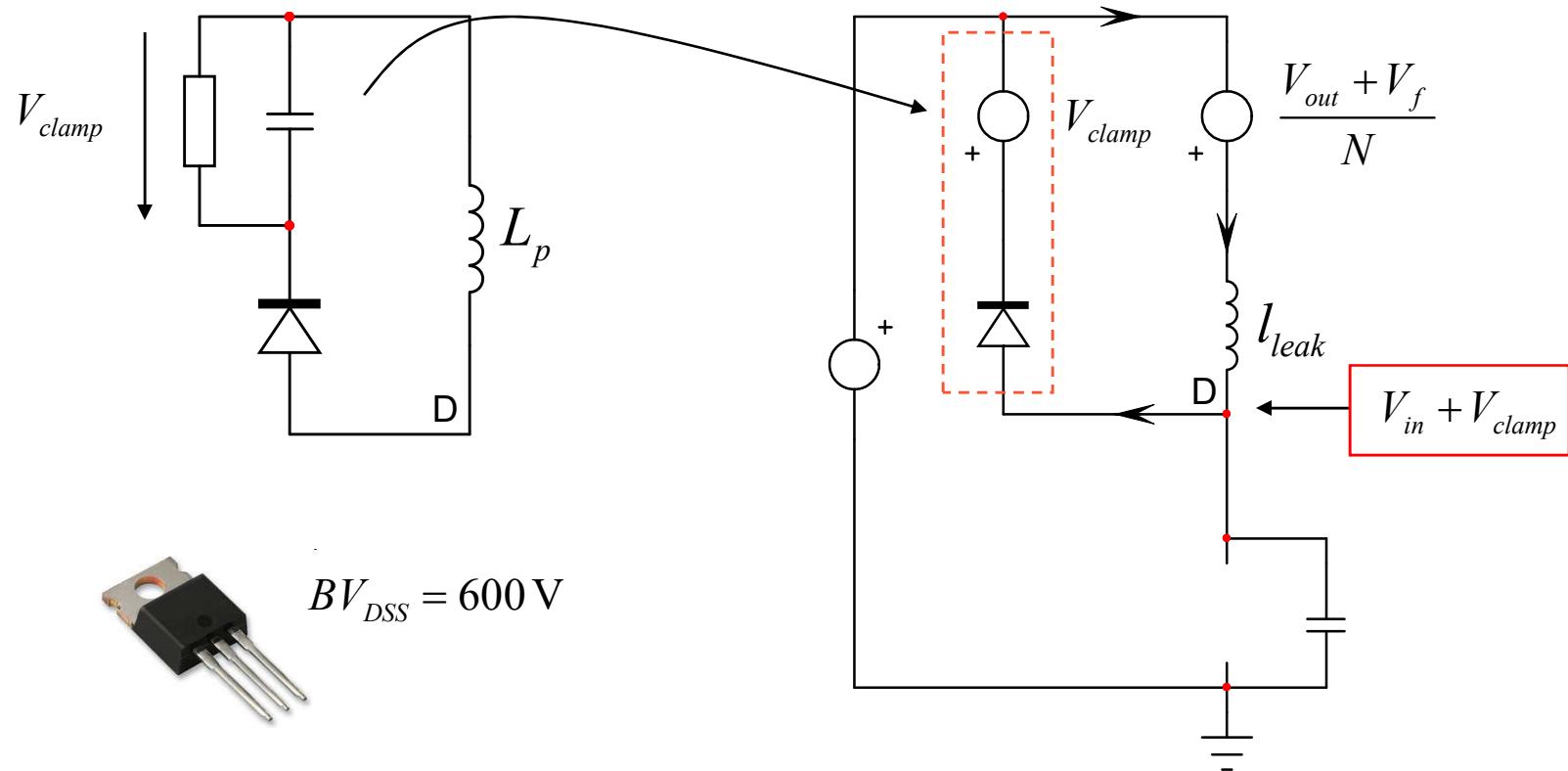
- As the diode conducts, V_{out} reflects over L_p



- The voltage on the drain increases dangerously!

We Need to Clamp that Voltage

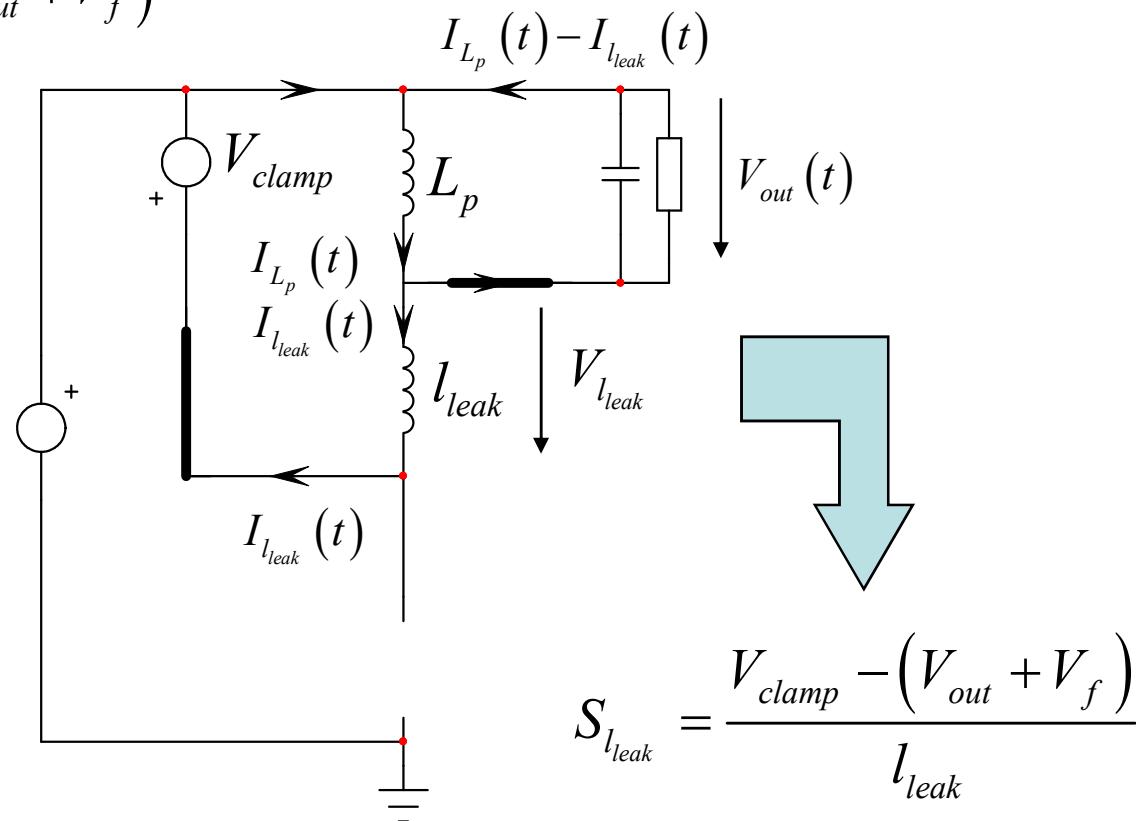
- MOSFETs have a voltage limit they can fly up to: BV_{DSS}
- A clamping circuit has been installed to respect a margin



Resetting the Leakage Inductance

- Because of the clamp action, a voltage appears across l_{leak}

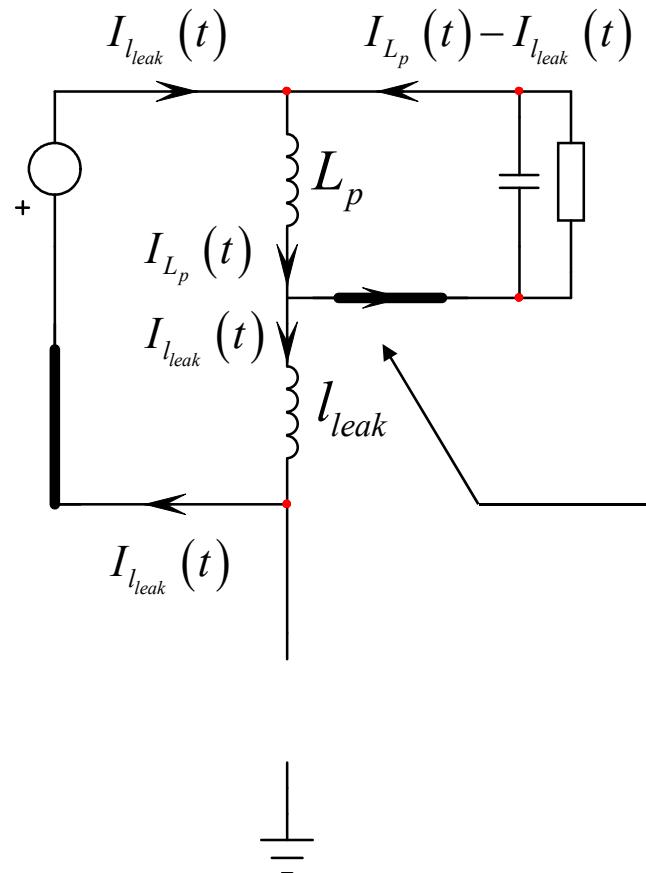
$$V_{l_{leak}} = V_{clamp} - (V_{out} + V_f)$$



- This voltage forces a reset of the leakage inductance

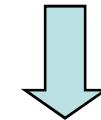
Do we Need a Quick Reset?

- When current flows in I_{leak} , it is diverted from the secondary



At the switch opening:

$$I_{L_p}(t) = I_{leak}(t)$$

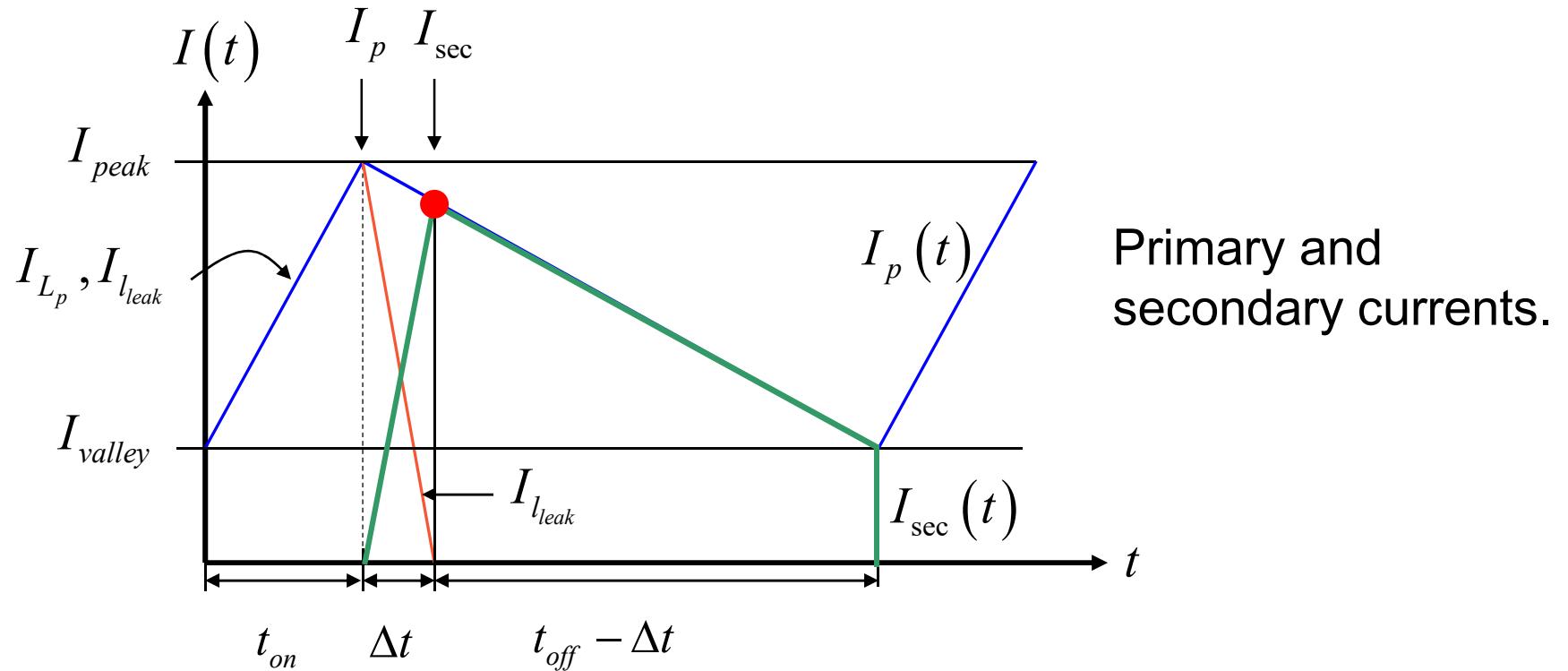


$$I_{sec}(t) = 0$$

- The leakage current delays the occurrence of the sec. current

I_{leak} Delays the Secondary Current

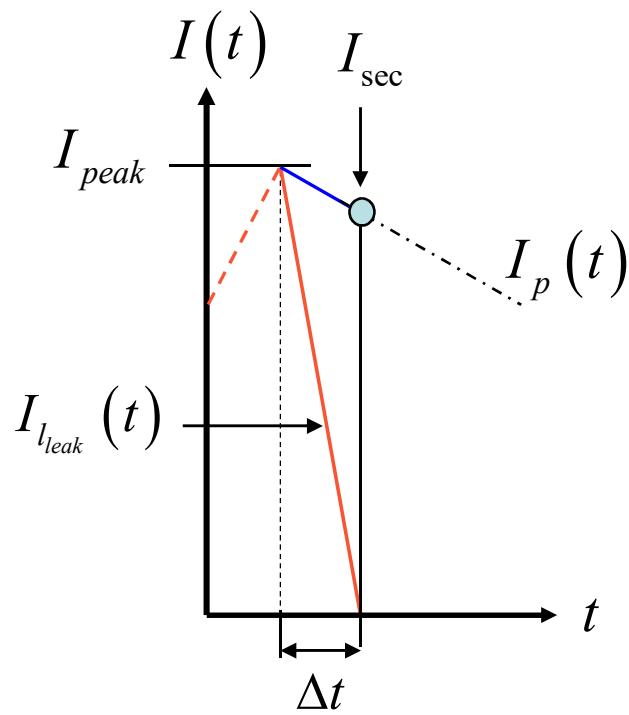
- The leakage inductor reduces the peak secondary current



- The "stolen" energy is dissipated as heat in the clamping network
- Less energy is transmitted to the secondary side

A Reduced Secondary-Side Current

- We can calculate the leakage inductor reset time Δt



$$\frac{l_{leak}}{L_p} = 1.8\%, \quad \frac{NV_{clamp}}{V_{out} + V_f} = 1.5$$



$$S_{leak} = \frac{V_{clamp} - (V_{out} + V_f)}{l_{leak}}$$

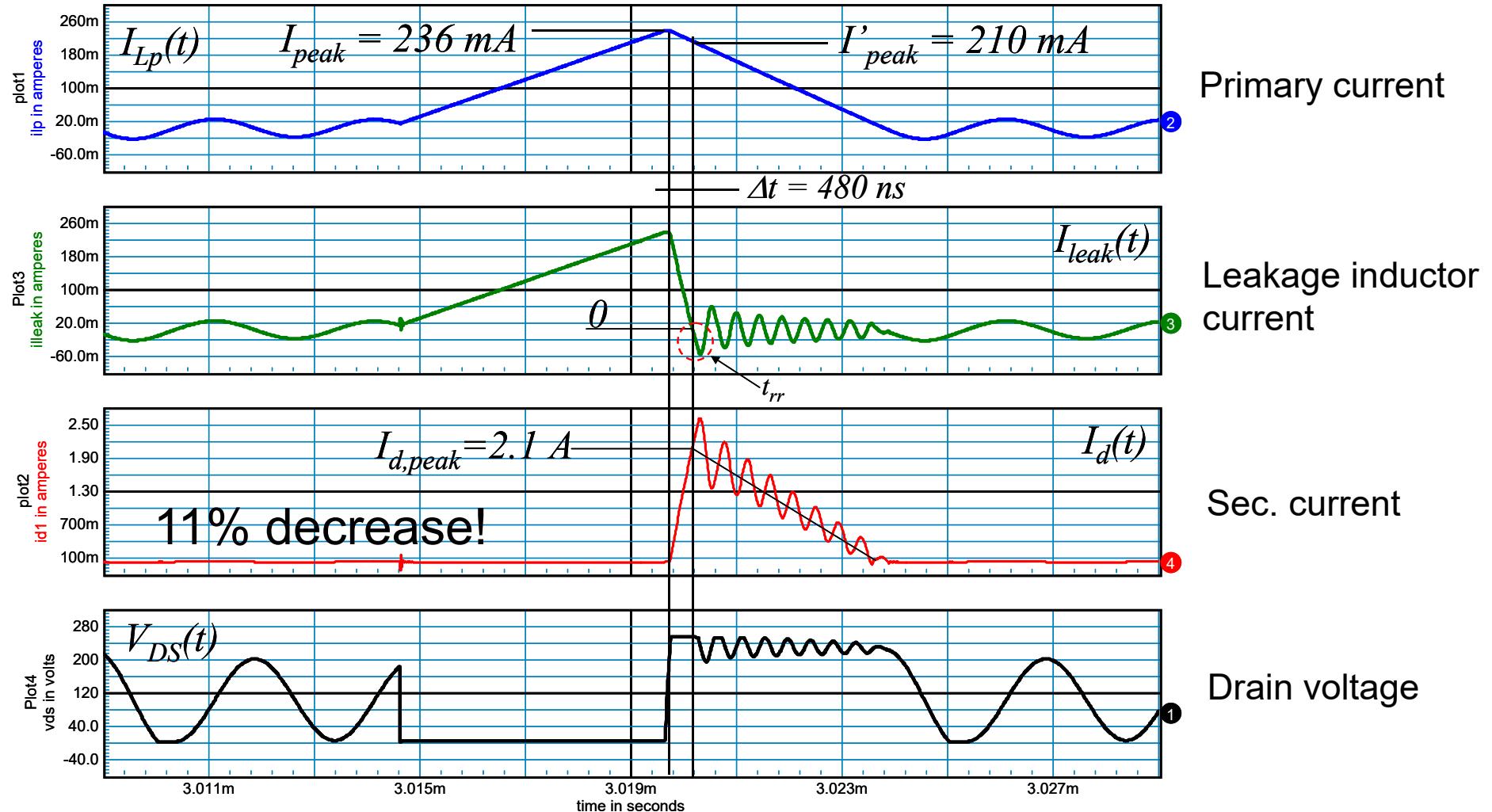
$$\Delta t = \frac{I_{peak}}{S_{leak}} = \frac{l_{leak} I_{peak}}{V_{clamp} - (V_{out} + V_f)}$$

$$\xrightarrow{N \neq 1} \Delta t = \frac{I_{peak}}{S_{leak}} = \frac{N l_{leak} I_{peak}}{N V_{clamp} - (V_{out} + V_f)}$$

$$I_{sec} = \frac{I_{peak}}{N} - S_{sec} \Delta t = \frac{I_{peak}}{N} \left(1 - \frac{l_{leak}}{L_p} \frac{1}{\frac{N V_{clamp}}{V_{out} + V_f} - 1} \right)$$

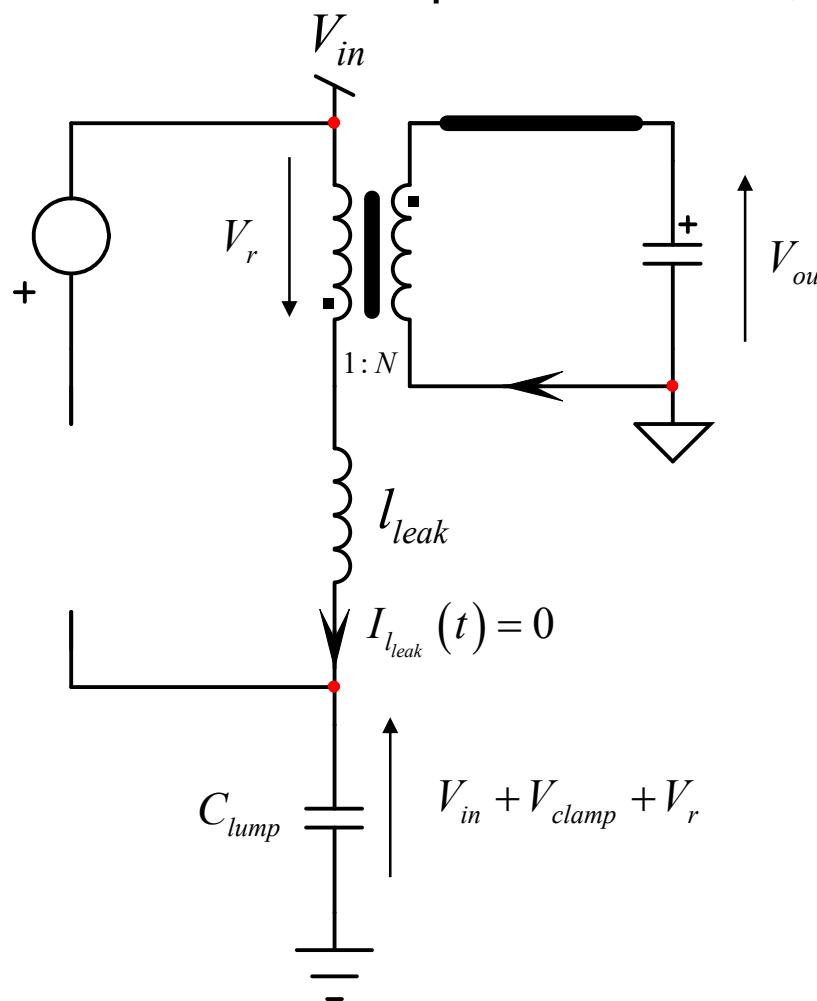
$$I_{sec} = \frac{I_{peak}}{N} - 3.6\%$$

Typical Example Simulation Results

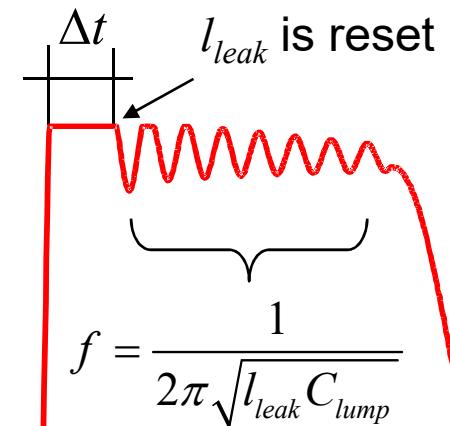


A Ringing Appears as the Diode Blocks

- As the clamp diode blocks, the drain returns to $V_{in} + \frac{V_{out} + V_f}{N}$

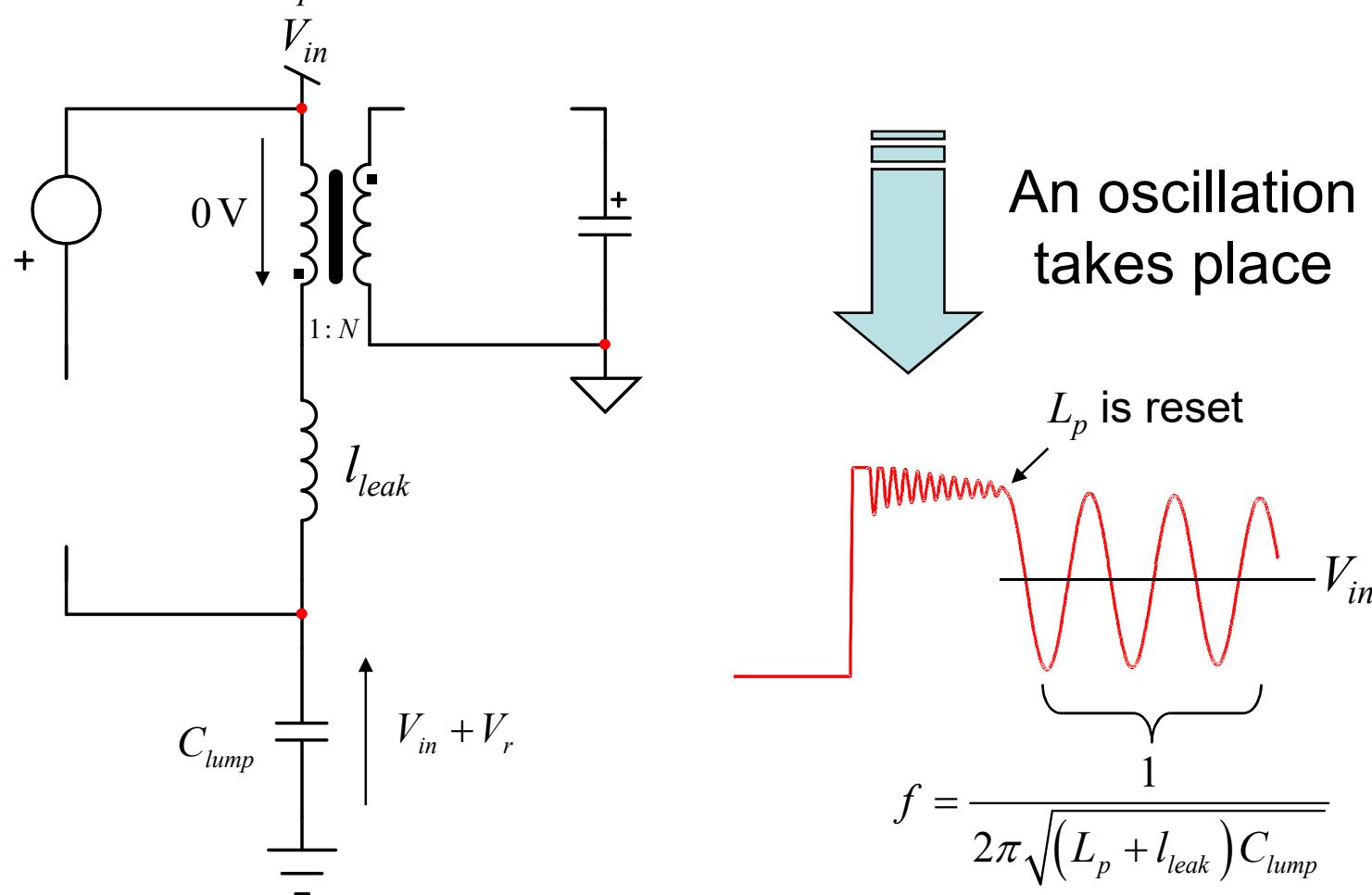


An oscillation takes place



The Primary Inductor also Rings in DCM

- When L_p is reset, the capacitor voltage returns to V_{in}

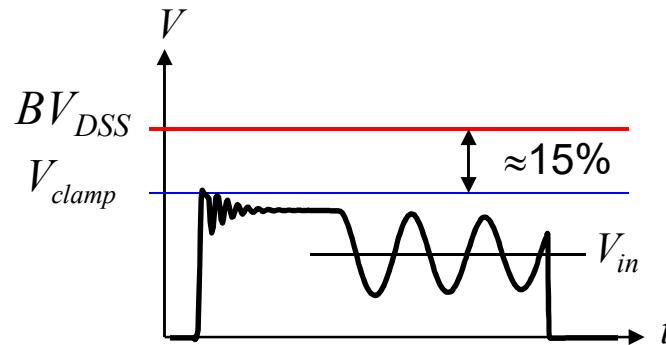


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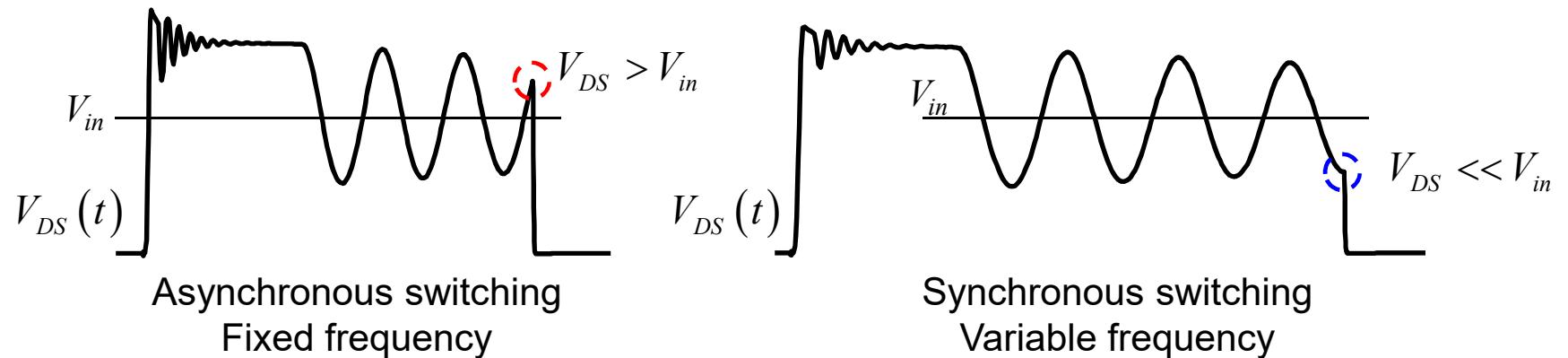
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How these Parasitics Affect your Design?

- The leakage inductor induces a large spike at turn-off
- This voltage excursion must be kept under control



- The lump capacitor on the drain brings switching losses
- Is there a way to switch on again when discharged?



Protecting the Power MOSFET

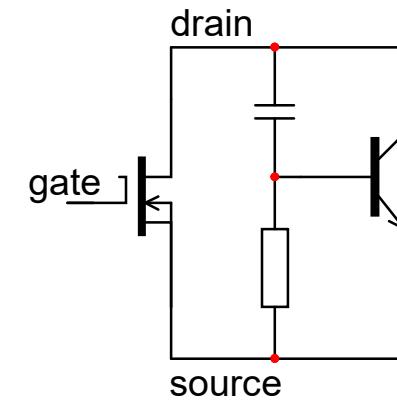
- A vertical MOSFET features a buried parasitic NPN transistor
 - The collector-base junction of this transistor forms the body-diode
 - This « diode » can accept to avalanche in certain conditions
 - Do NOT use this diode as a Transient Voltage Suppressor
-
- ✓ Adopt a safety coefficient k_D when choosing the maximum $V_{DS}(t)$
 - ✓ 15% derating is usually selected

$$k_D = 0.85$$

$$BV_{DSS} \times k_D = 600 \times 0.85 = 510 \text{ V}$$

$$V_{clamp} = BV_{DSS} \times k_D - V_{os} - V_{in} = \boxed{115 \text{ V}}$$

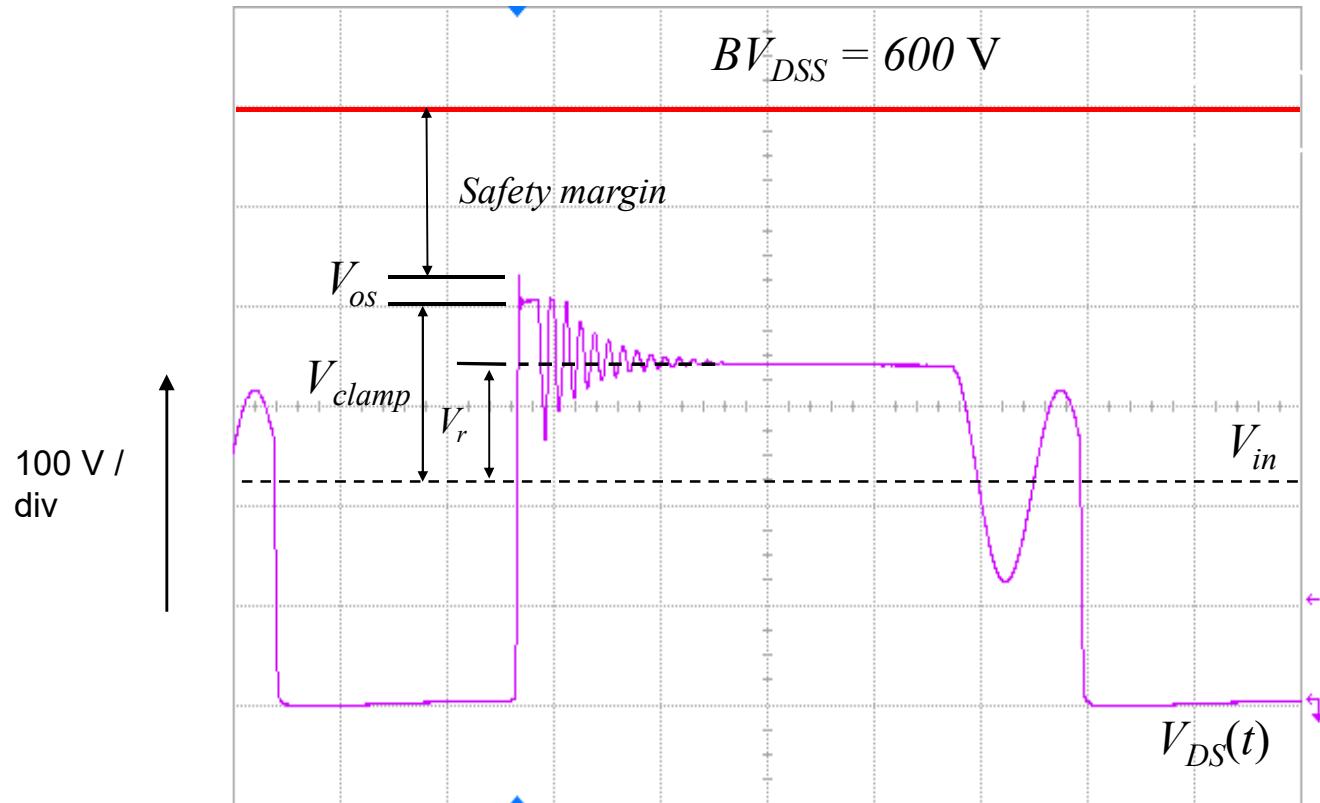
Take V_{os} around 15 – 20 V



RCD clamp
design entry

Inclusion of a Safety Margin

- The voltage on the drain swings up to V_{clamp}



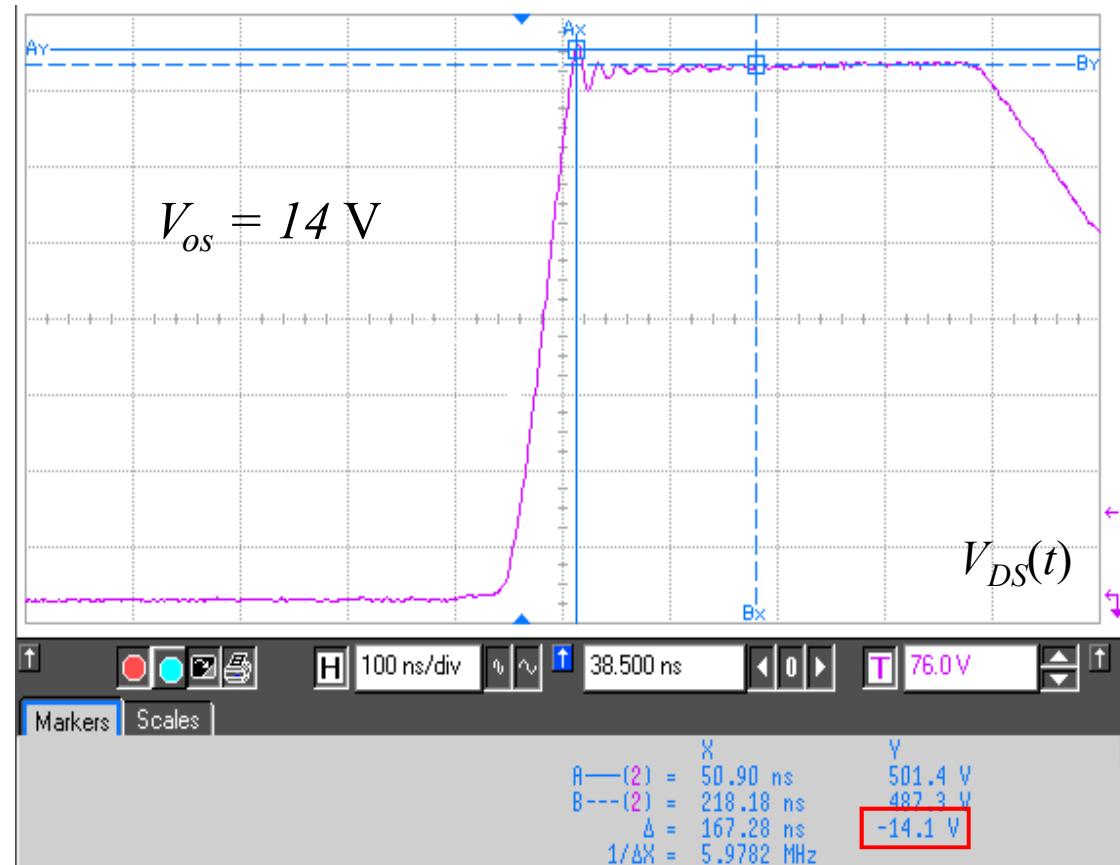
V_{out} = nominal
 I_{out} = max
 V_{in} = max

Test at start-up
and in short-circuit

- Capture this waveform in worst-case conditions

The Clamp Circuit Overshoots

- The clamp diode forward transit time delays the clamping action

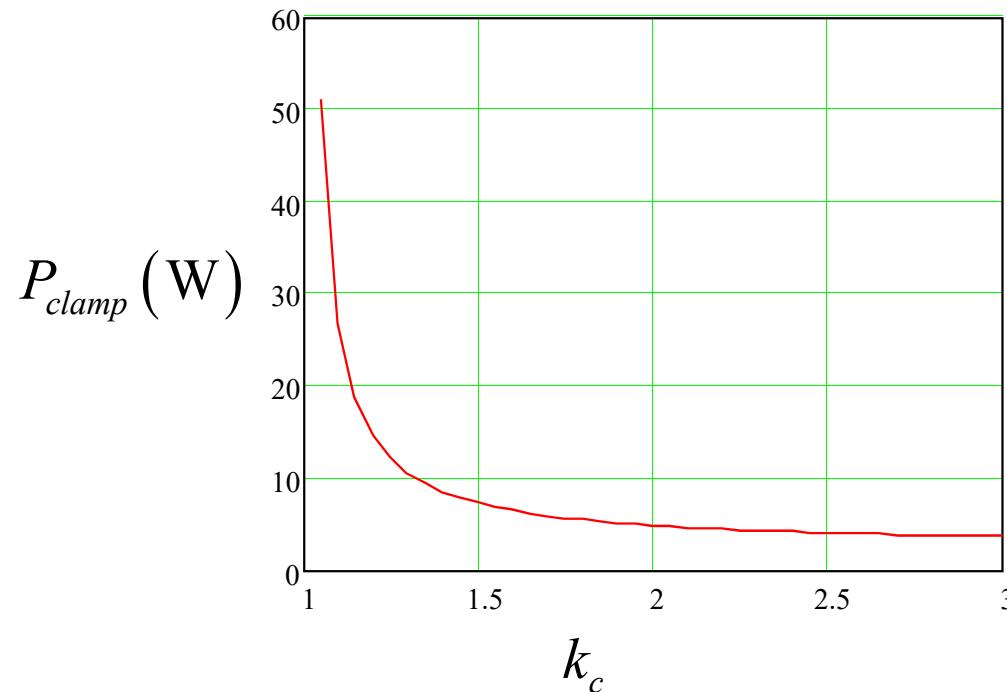


- This spike can be lethal to the power MOSFET

Do not Reflect too Much Voltage

- The reflected voltage affects the power dissipation in the clamp

$$P_{V_{clamp},avg} = \frac{1}{2} F_{sw} L_{leak} I_{peak}^2 \frac{k_c}{(k_c - 1)} \quad k_c = \frac{V_{clamp}}{V_r}$$



- If V_{clamp} is too close to V_r , dissipation occurs $\rightarrow k_c = 1.3$ to 2

Compute the Transformer Turns Ratio

- The turns ratio affects the reflected voltage...

$$V_{clamp} \geq k_c \frac{(V_{out} + V_f)}{N} \quad \Rightarrow \quad N \geq \frac{k_c (V_{out} + V_f)}{V_{clamp}}$$

- But also the Peak Inverse Voltage of the secondary diode

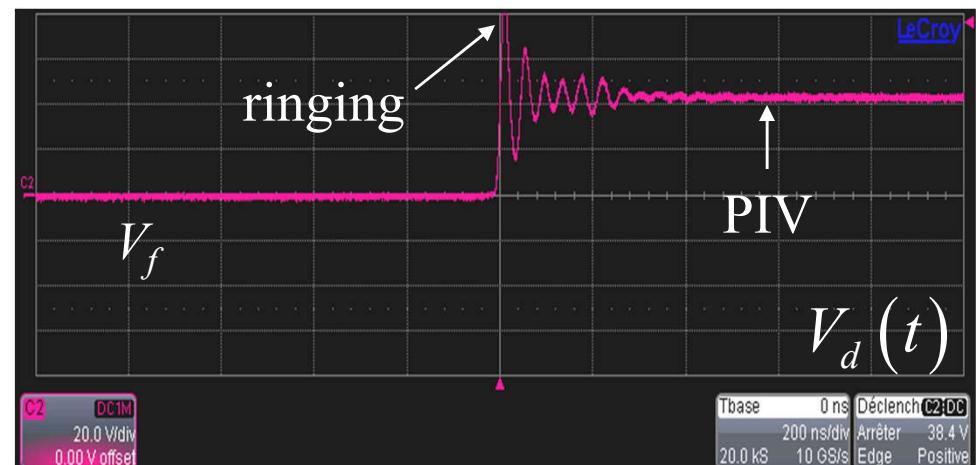
$$PIV = V_{in} N + V_{out}$$



Choose a 100% derating factor

If $PIV = 100 \text{ V}$

Then $BV = 200 \text{ V}$



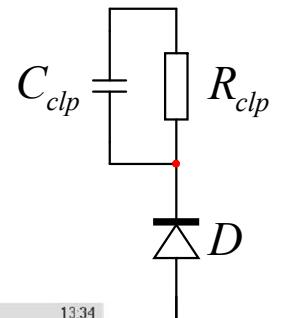
- Always check the margins are not violated in any operating modes

Select the Clamp Passive Elements

- The clamp resistor depends on the maximum peak current

$$R_{clp} = \frac{2V_{clamp} \left[V_{clamp} - \frac{(V_{out} + V_f)}{N} \right]}{F_{sw} l_{leak} I_{peak}^2}$$

$$C_{clp} = \frac{V_{clamp}}{R_{clp} F_{sw} \Delta V}$$



$$I_{peak,max} = \frac{V_{sense,max}}{R_{sense}} + \frac{V_{in,max}}{L_p} t_{prop}$$

Worst-case value

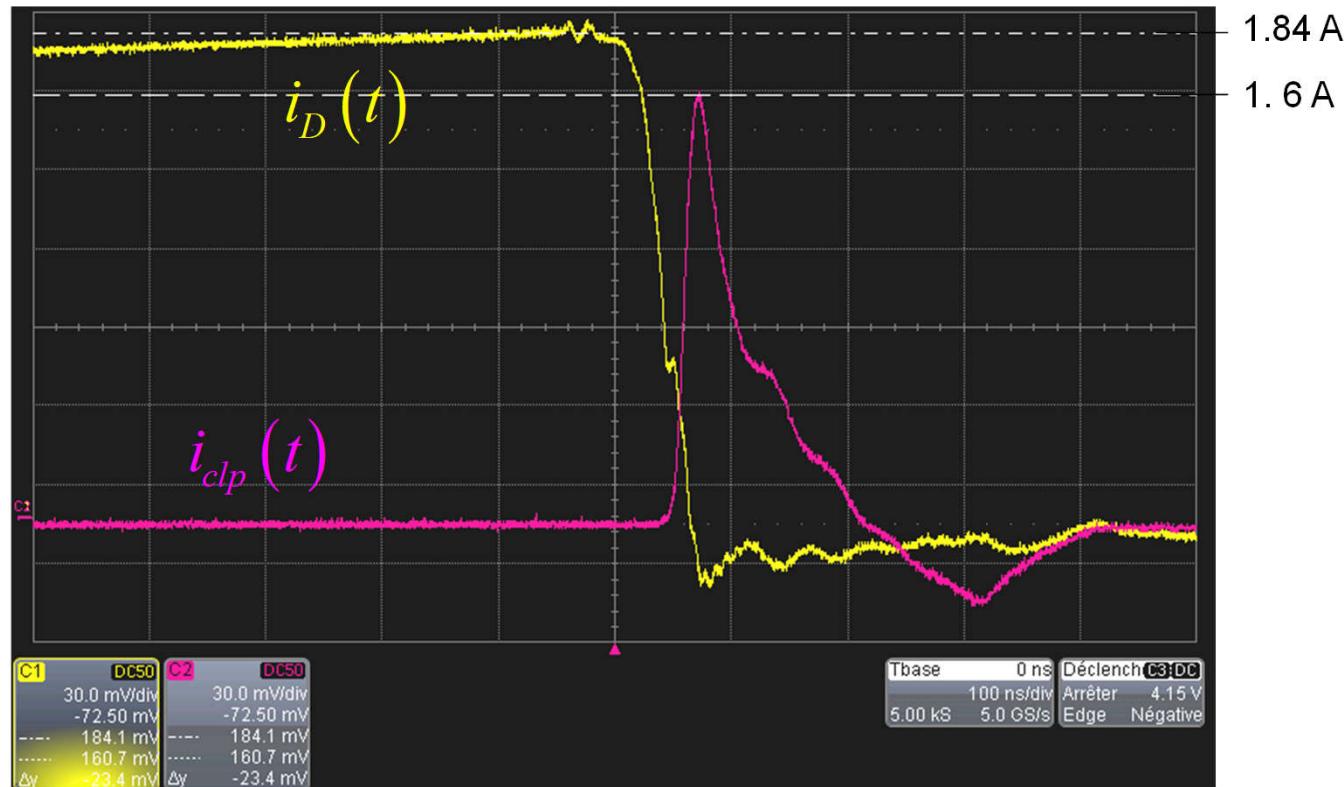


600 V

- Watch for the peak current overshoot in fault!

Clamp Current is Smaller

- Lump capacitance charge at turn off depletes the leakage energy



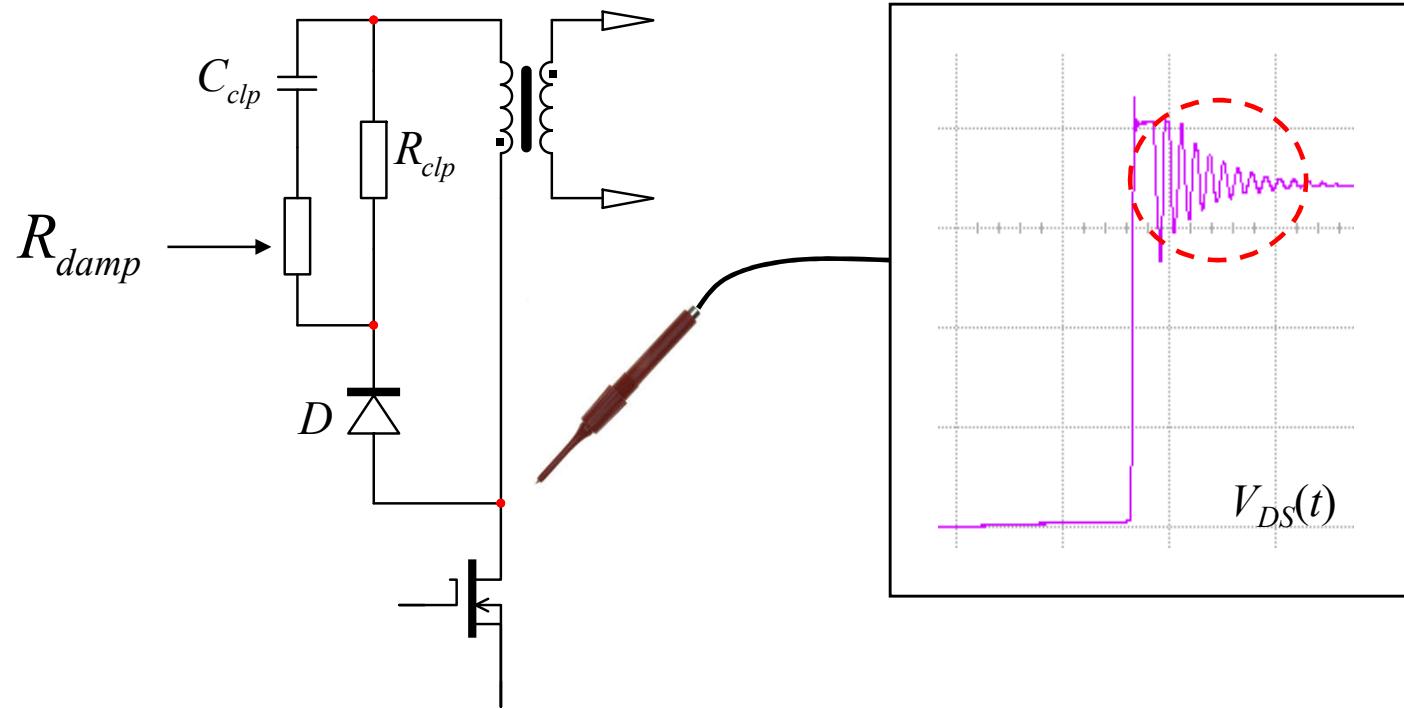
$$\Delta I = 234 \text{ mA}$$

$$1.13^2 = 1.28$$

$$(0.234/1.84) * 100 = 13\% \longrightarrow \text{Power is reduced by 28\%}$$

The Leakage Inductor Rings

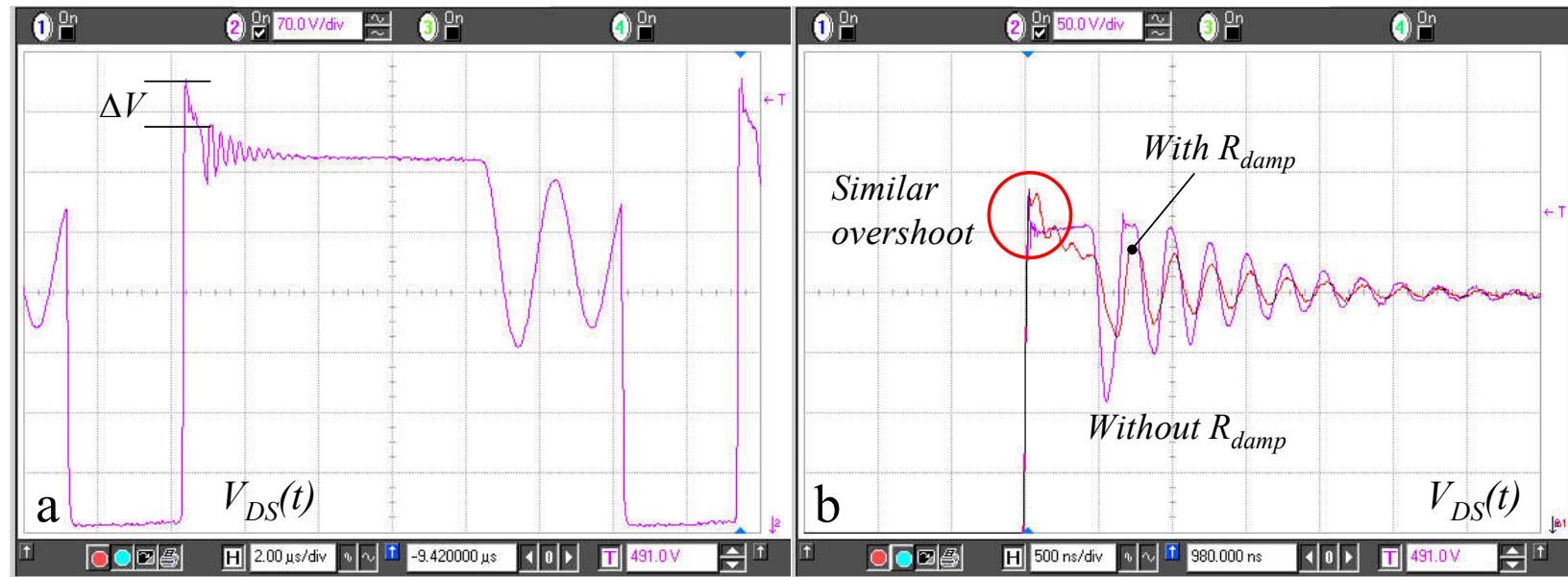
- This ringing can be of high frequency and is radiated-EMI rich



- It can also forward-bias the MOSFET body diode
- Damp it!

Fighting Parasitic Ringing – part I

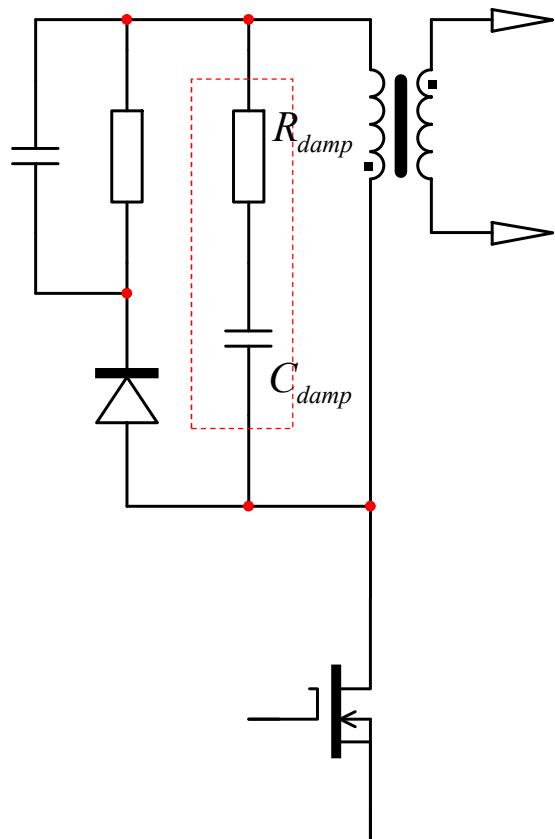
- The installed resistor reduces the ringing on the drain



$$Q = \frac{\omega_0 l_{leak}}{R_{damp}} = 1 \quad Z_{l_{leak}} @ f_0 = R_{damp}$$

Fighting Parasitic Ringing – part II

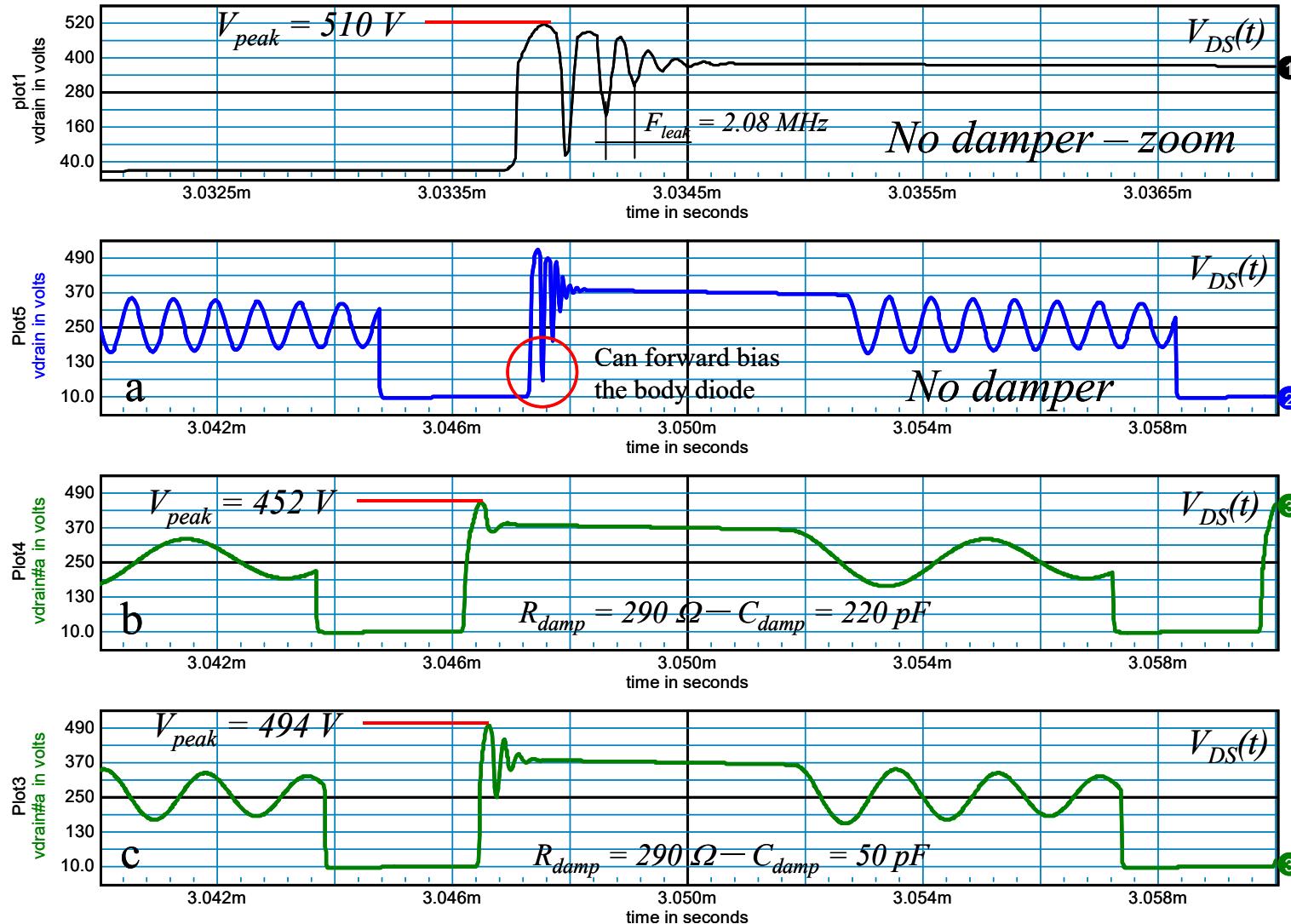
- If the series resistor is not enough, install a damper



1. Measure the ringing: f_0
2. Evaluate leakage impedance at f_0
$$Z_{l_{leak}} = 2\pi l_{leak} f_0$$
3. Make $R_{damp} = Z_{l_{leak}}$
4. Try $C_{damp} = \frac{1}{2\pi f_0 R}$
5. Tweak for power dissipation

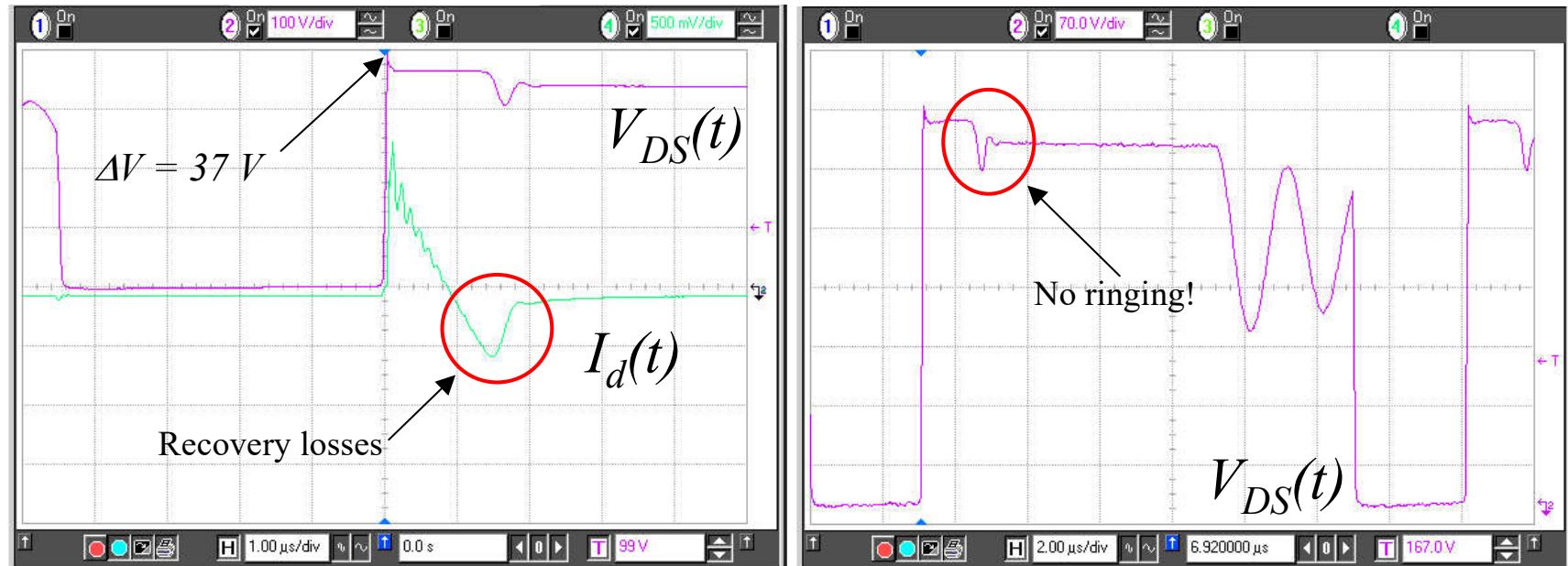
Ray Ridley – Snubber design procedure

Effects brought by clamping action



What Diode to Select for the Clamp?

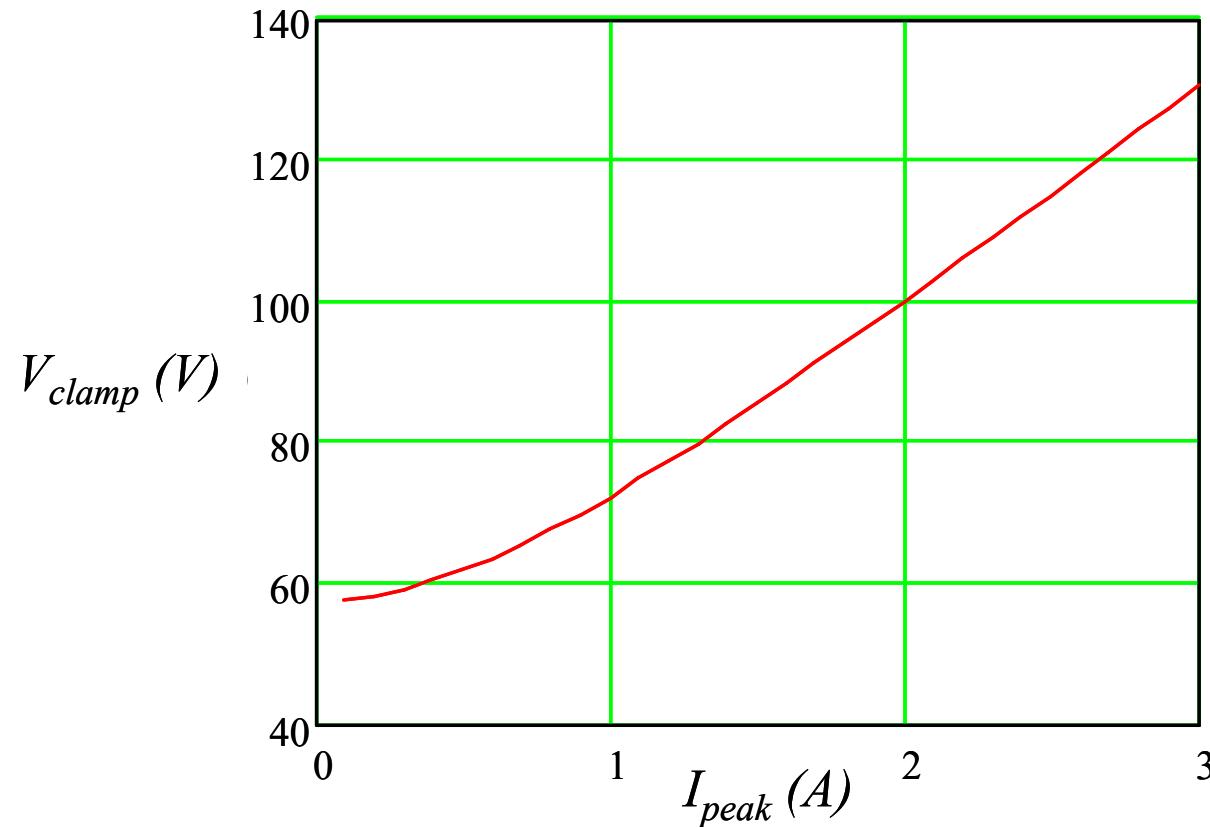
- A fast diode is a must: MUR160 is good fit



- Can a simple 1N4007 be used in a *RCD* clamping network?
- The answer is yes for low power applications (below 20 W)
- The long recovery time naturally damps the leakage inductor

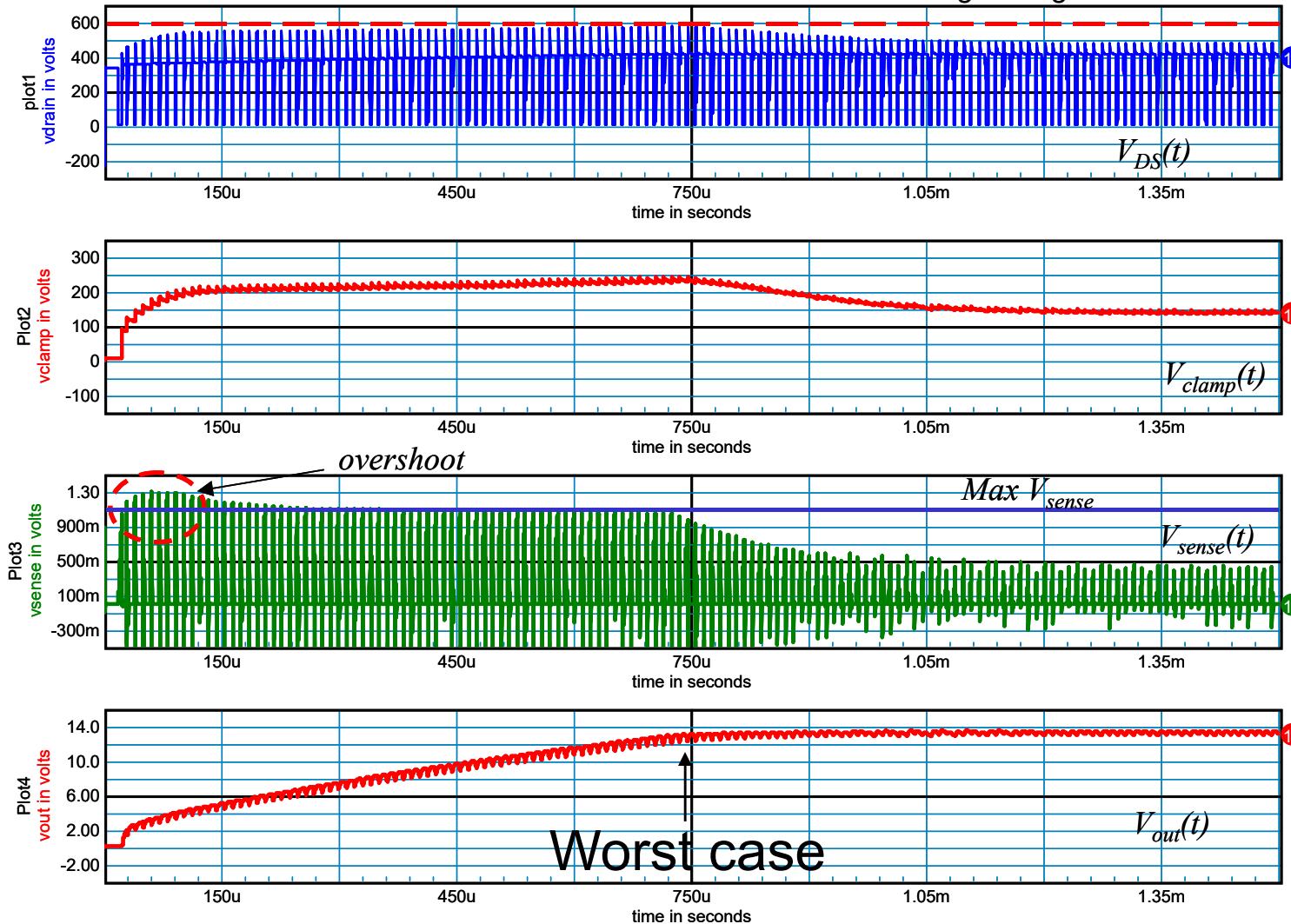
Be Sure the Clamp Level does not Runaway

- Watch-out for clamp voltage variations, at start-up or in short-circuit
- The main problem comes from the propagation delay!



Check the Clamp Voltage Variations

No design margin!



Drain
voltage

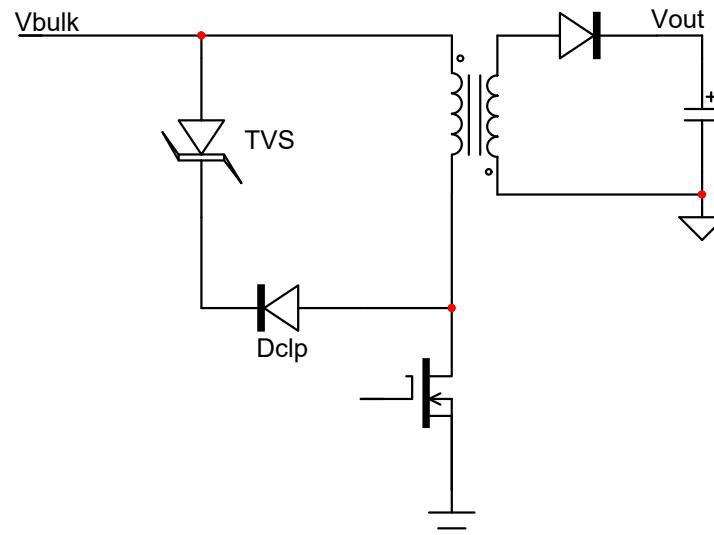
Clamp
voltage

Sense
voltage

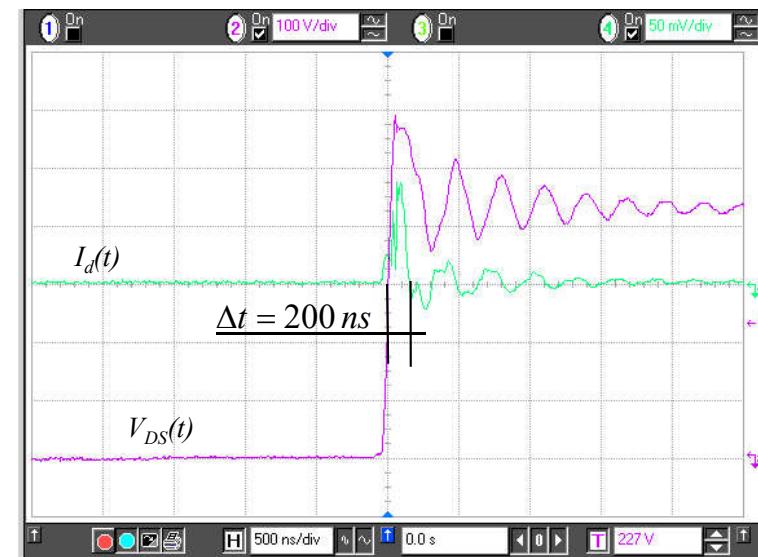
Output
voltage

A Zener or TVS to Hard Clamp the Voltage

- TVS do not suffer from voltage runaways in fault conditions



$$P_{TVS} = \frac{1}{2} F_{sw} l_{leak} I_{peak}^2 \frac{V_z}{V_z - \frac{(V_{out} + V_f)}{N}}$$



- The TVS improves the efficiency in standby but degrades EMI
- ❖ It costs around 5 cents...

Course Agenda

- The Flyback Converter
- The Parasitic Elements
- How These Parasitics Affect your Design?
- Current-Mode is the Most Popular Scheme**
- Fixed or Variable Frequency?
- More Power than Needed
- The Frequency Response
- Compensating With the TL431

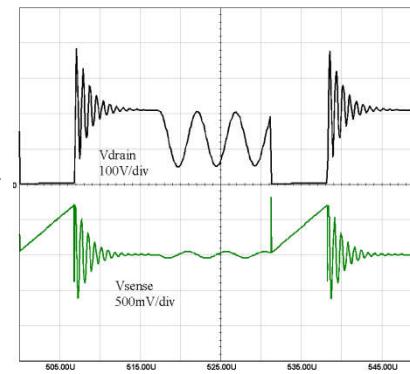
What Control Scheme?

- Two control scheme coexist, current-mode and voltage-mode



Voltage-mode?

Current-mode?

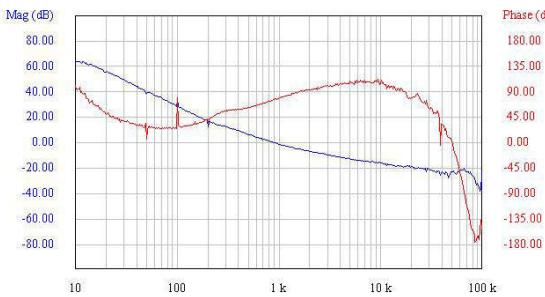


Operating waveforms
are identical



Voltage-mode?

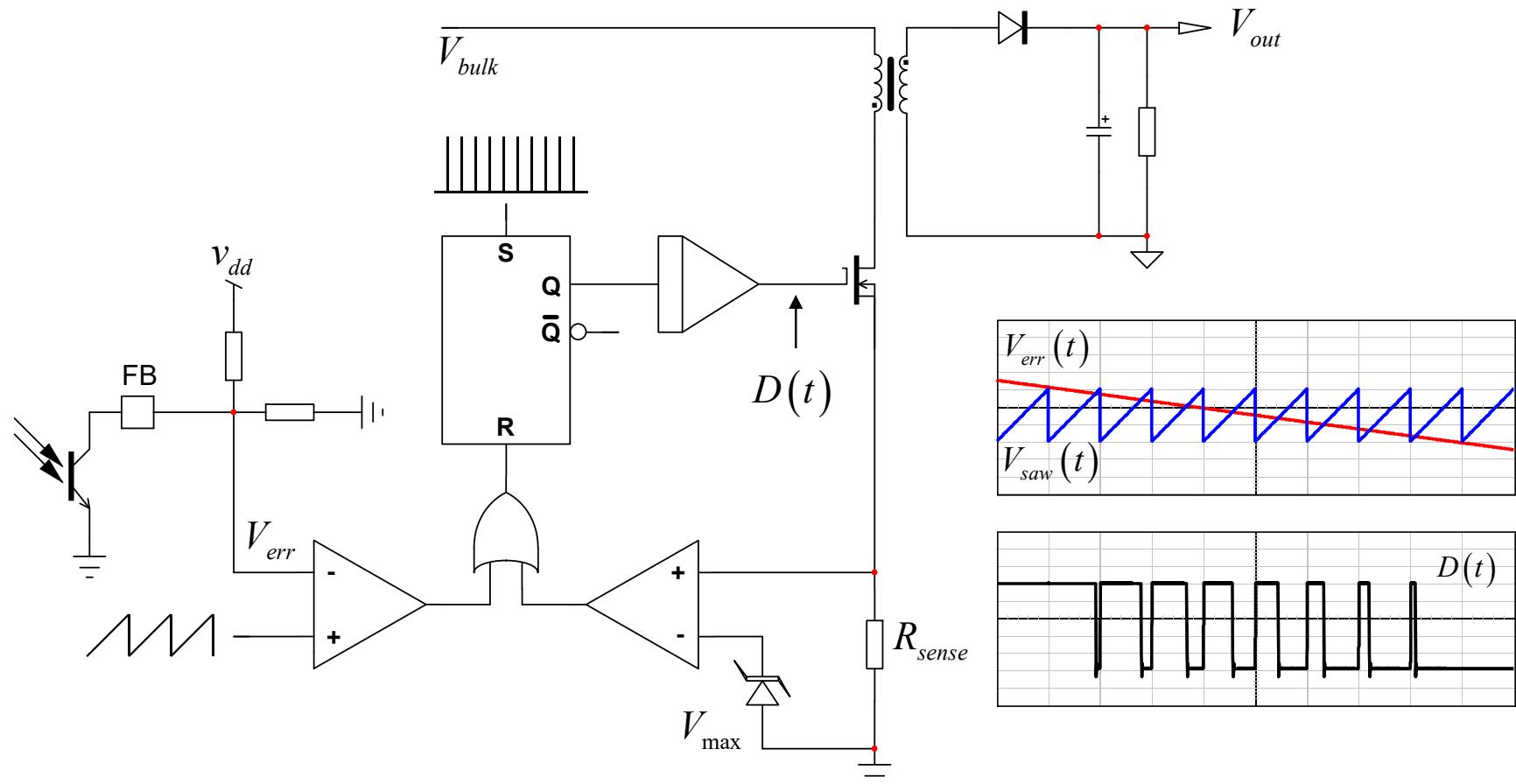
Current-mode?



Ac -transfer
functions
differ

Voltage-Mode Control

- Voltage mode uses a ramp to generate the duty-ratio
- The error voltage directly adjusts the duty-ratio



Voltage-Mode Control

PROs

- Does not need the inductor current information
 - Can go to very small duty-ratio
- CCM operation without sub-harmonic instabilities
 - No need for slope compensation, current limit unaffected

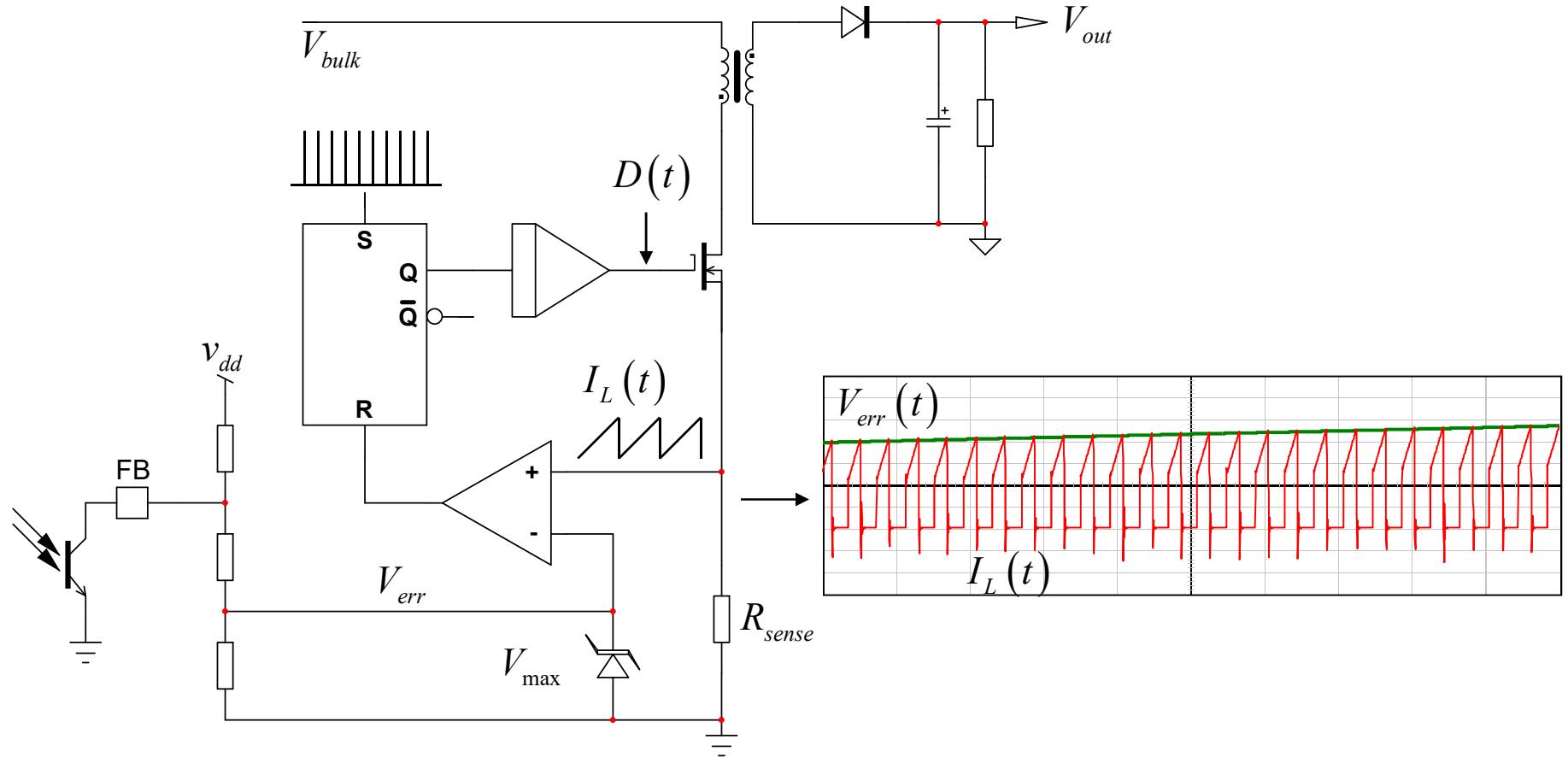
CONs

- No inherent input line feedforward (weak audio susceptibility)
 - Cannot use small bulk capacitor, bad ripple rejection
- 2nd-order system in CCM: mode transition can be a problem
- Limited integrated circuit offer



Peak-Current-Mode Control

- Current mode uses the inductor current information as a ramp
- The error voltage adjusts the inductor peak current
- The duty-ratio is indirectly controlled



Peak-Current-Mode Control

PROs

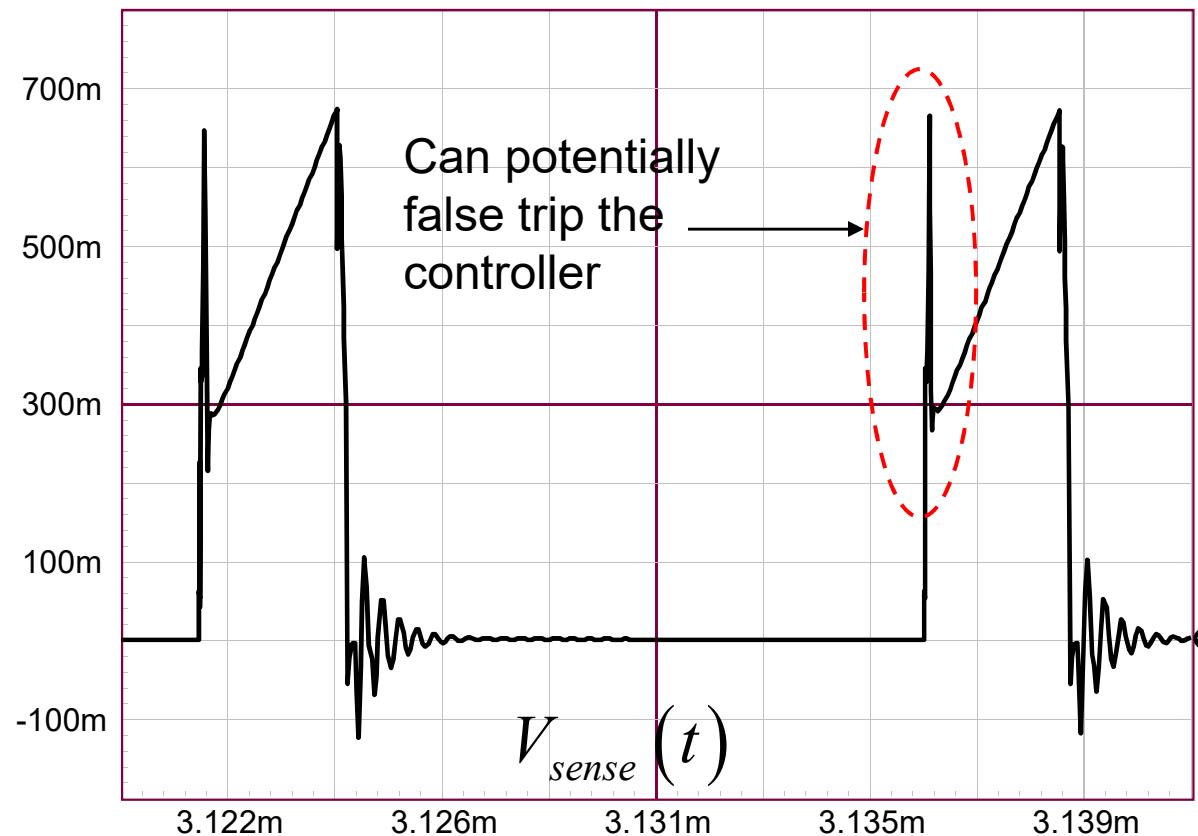
- Inherent pulse-by-pulse current limitation
- Natural input line rejection
- Mode transition DCM to CCM is easy
- Converter remains a 1st-order system at low frequency
- Widest offer on the market: a really popular technique!

CONs

- Leading Edge Blanking limits the minimum duty-ratio
- Requires slope compensation against sub-harmonic oscillations
- Additionnal ramp affects the available maximum peak current
- Current sense can sometimes be a problem (floating sense)

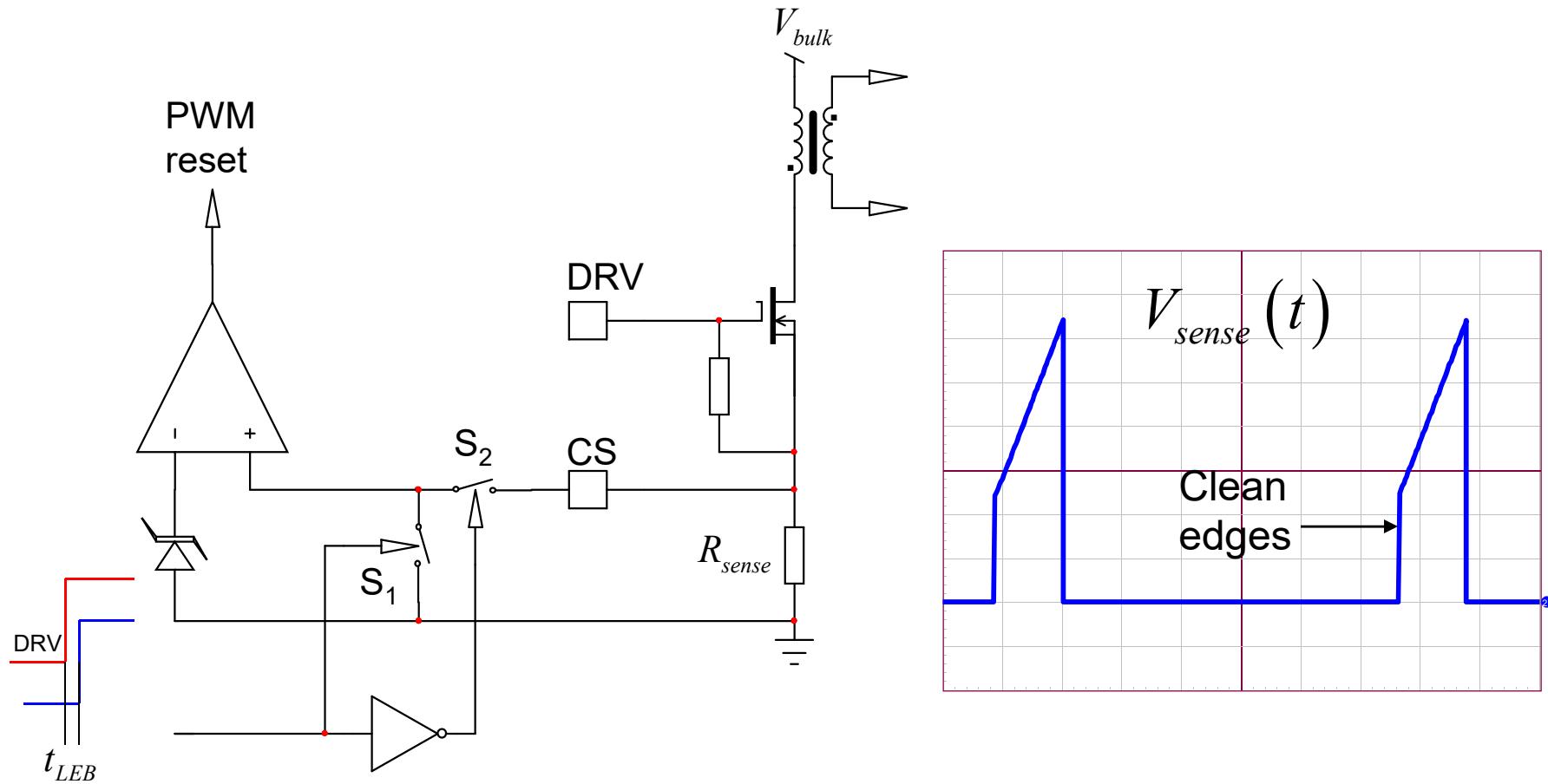
A Dirty Inductor Current Signal

- The inductor current is sensed with a resistor, a transformer...
- This information is affected by parasitics: false tripping possible!



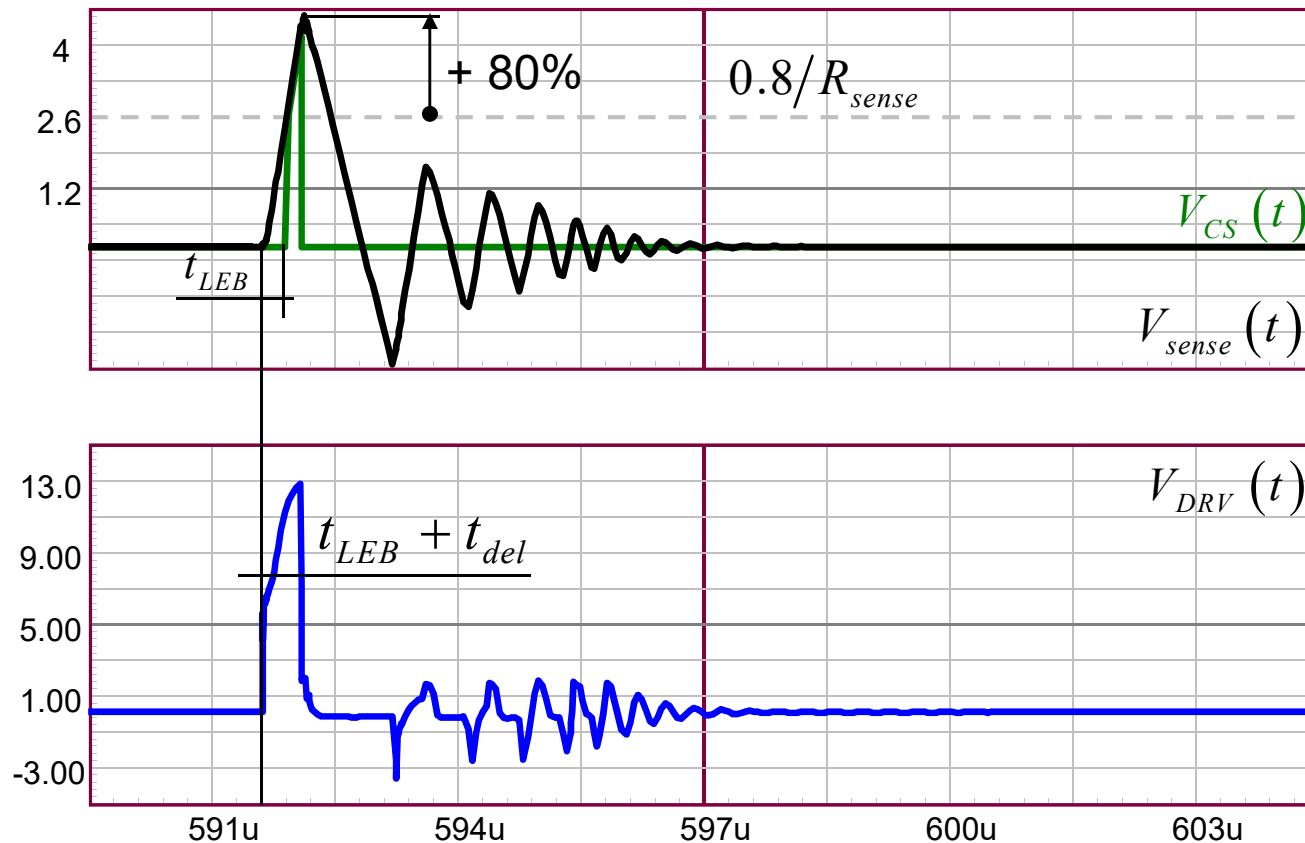
The LEB Cleanses the Signal

- A circuit blinds the controller at turn-on for a small time (≈ 250 ns)
- It conveys the signal afterwards: Leading Edge Blanking



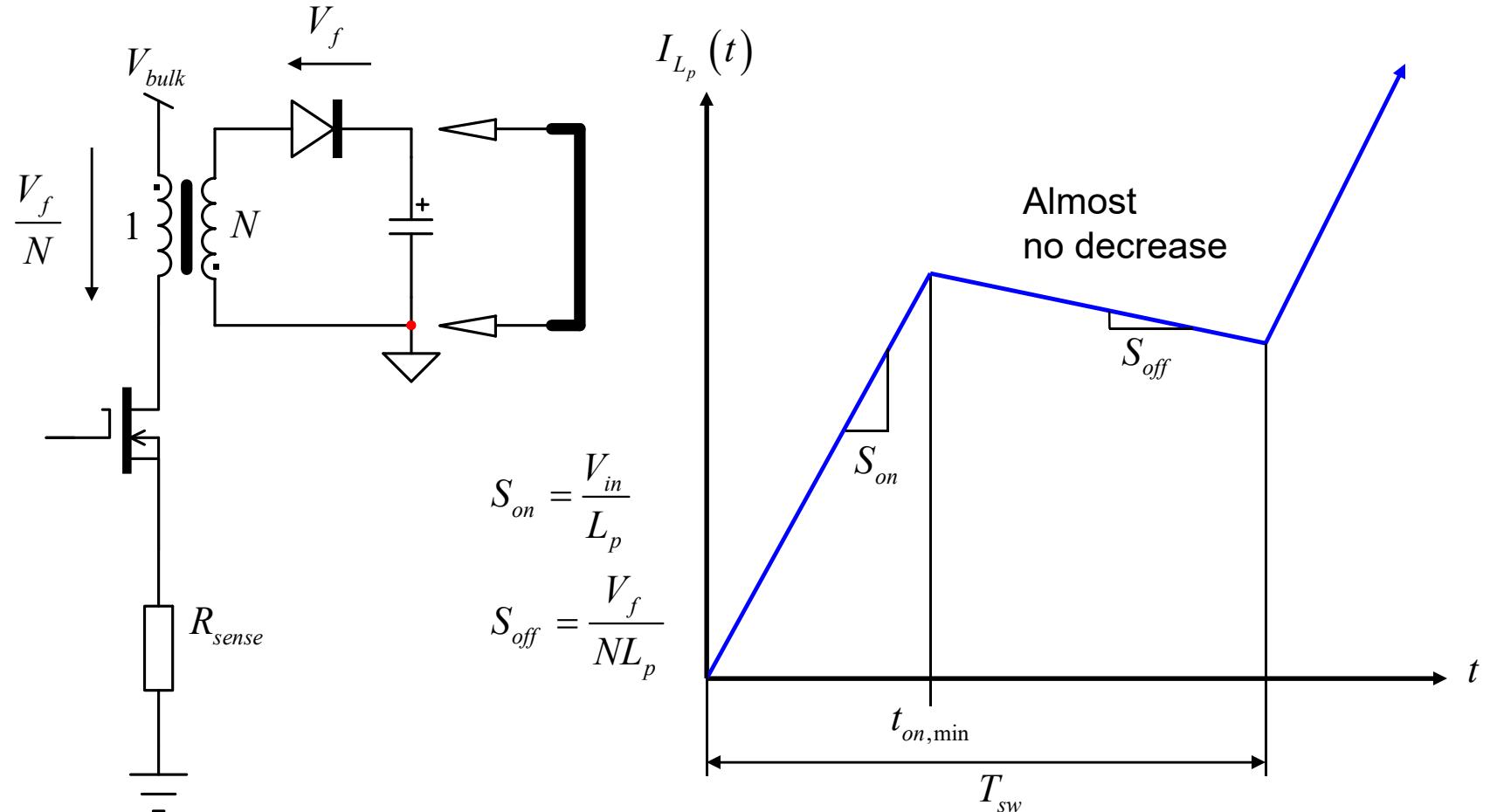
It Limits the Minimum Duty-Ratio

- During the LEB duration, the controller is completely blind!
- In output winding short-circuits, failures are likely to occur



If the Primary Inductor is too Low...

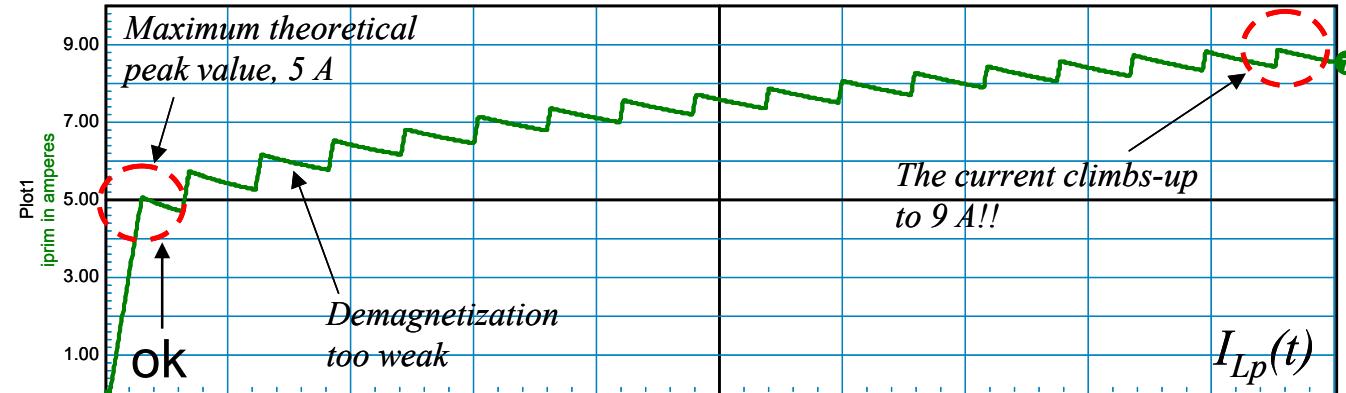
- In short-circuit situations, you reflect the diode forward drop



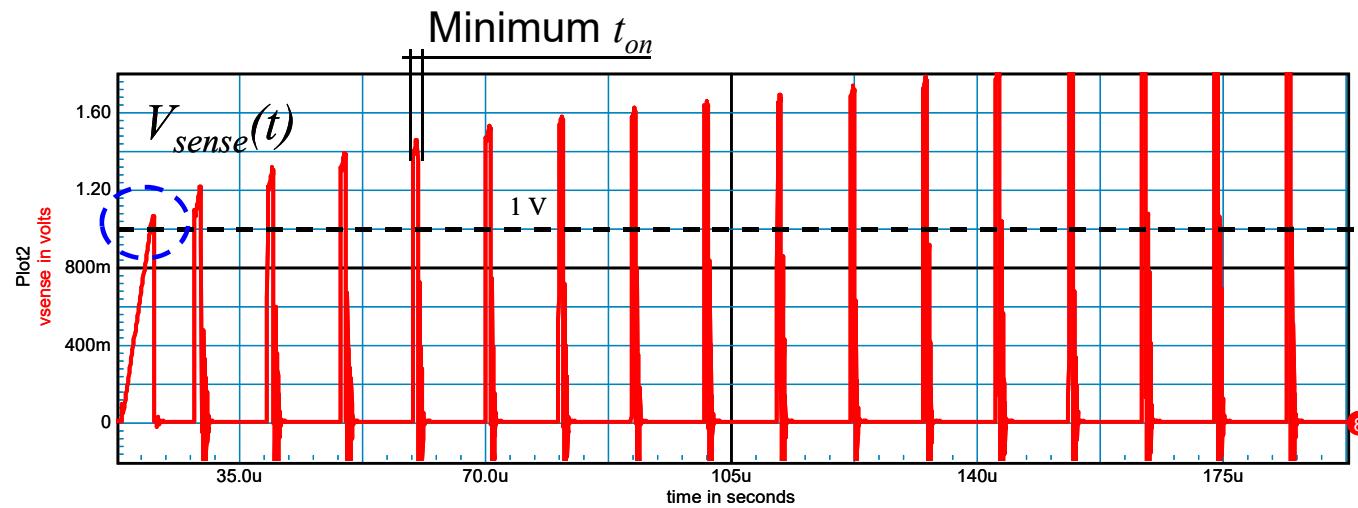
- If you hit the minimum on-time, you cannot limit the current!

The Primary Current Runs out of Control

- The current current climbs cycle by cycle until smoke appears!

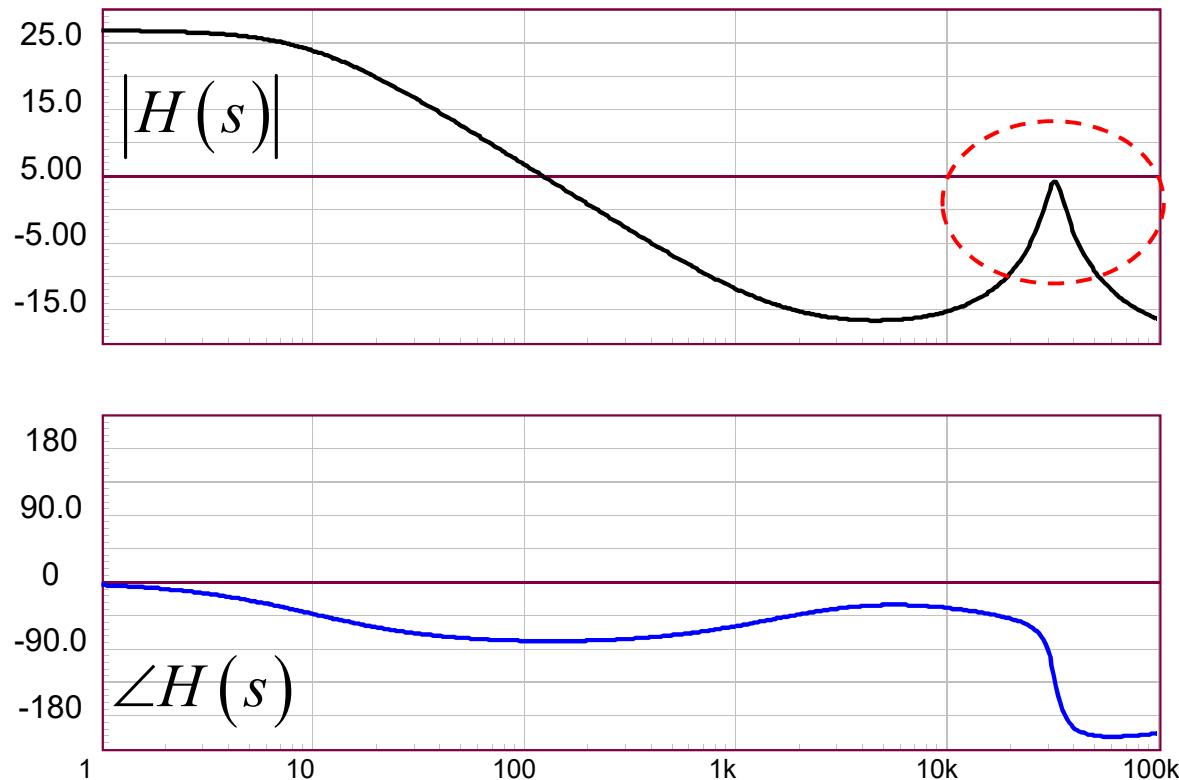


Chris Basso
first design...



Sub-Harmonic Oscillations

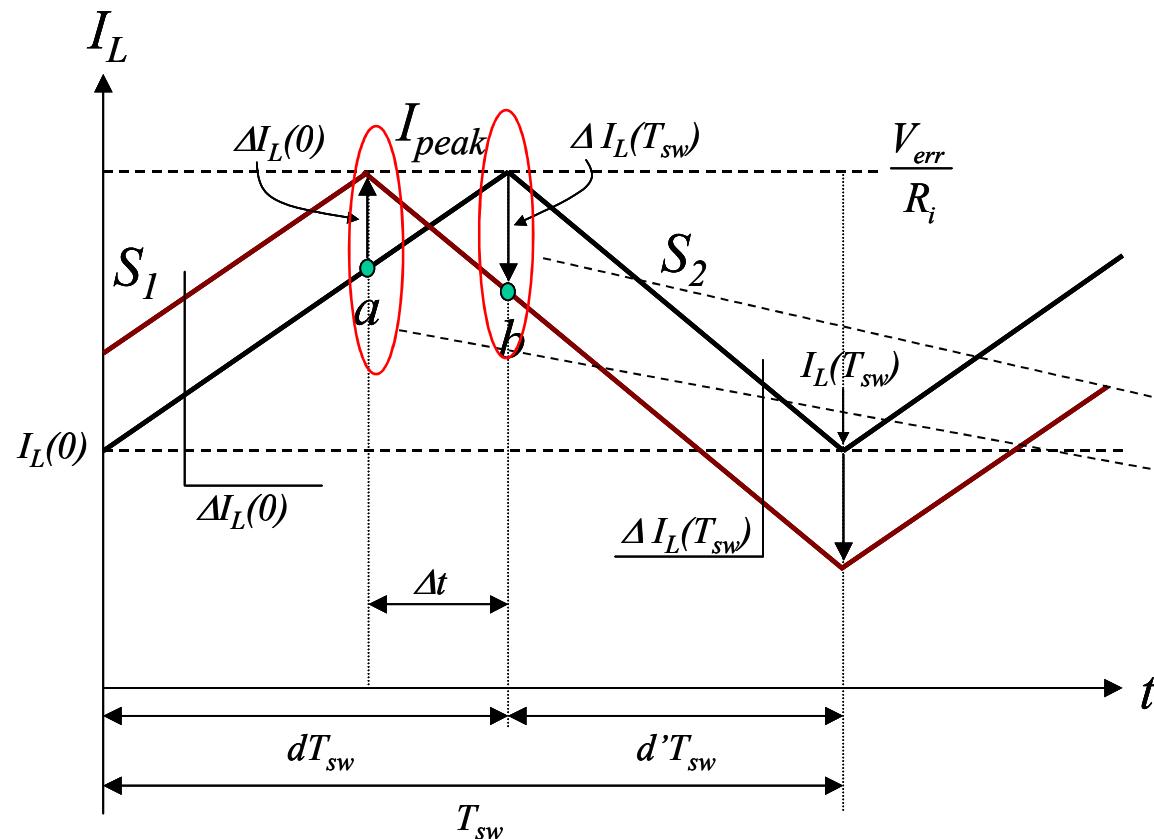
- Ac analysis shows a first-order system at $f_c \ll F_{sw}/2$
 - No LC peaking anymore as in CCM voltage mode
 - But a subharmonic peaking at $F_{sw}/2$ now appears



Flyback power
stage in CCM

Instability Depends on Duty-Ratio

- The condition for instability is: CCM operation + duty-ratio > 50%



$$I_{peak} = a + S_1 \Delta t$$

$$b = I_{peak} - S_2 \Delta t$$

Solving
 Δt

$$\frac{I_{peak} - a}{S_1} = \frac{I_{peak} - b}{S_2}$$

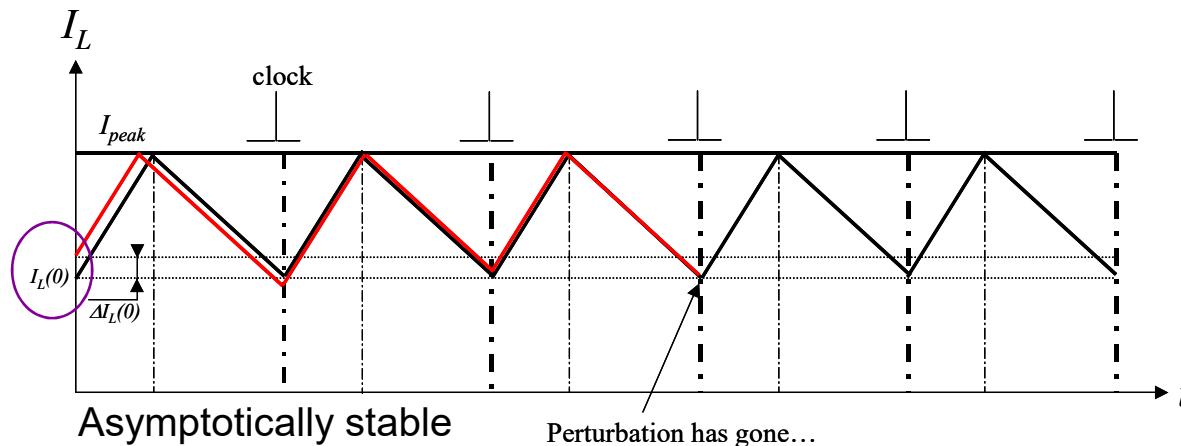
$$\frac{\Delta I_L(0)}{S_1} = \frac{\Delta I_L(T_{sw})}{S_2}$$

$$\frac{S_2}{S_1} = \frac{d}{d'}$$

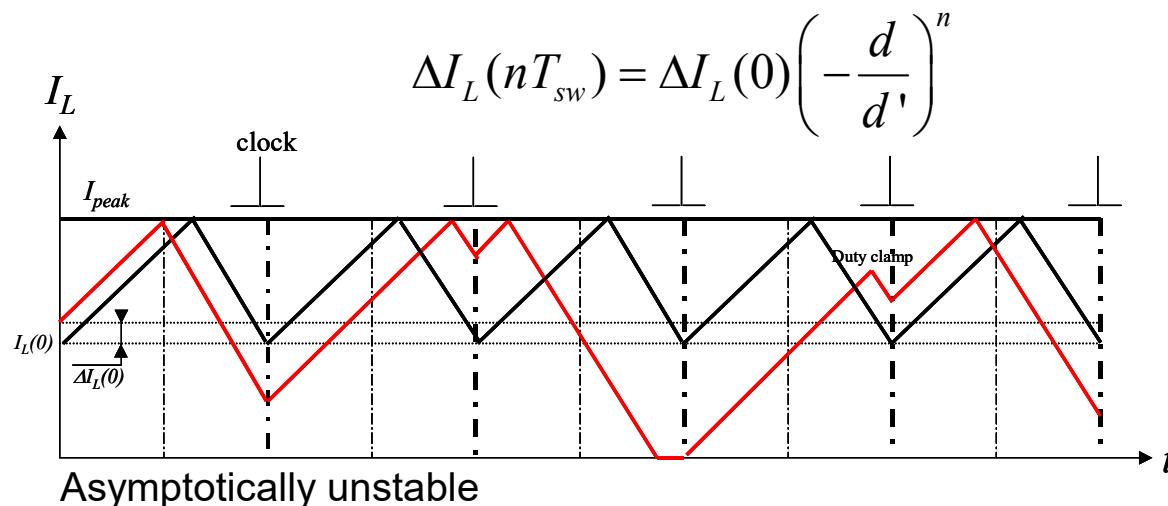
$$\Delta I_L(nT_{sw}) = \Delta I_L(0) \left(-\frac{d}{d'} \right)^n$$

Instability Depends on Duty-Ratio

- With a duty-ratio below 50%, perturbation naturally dies out ...

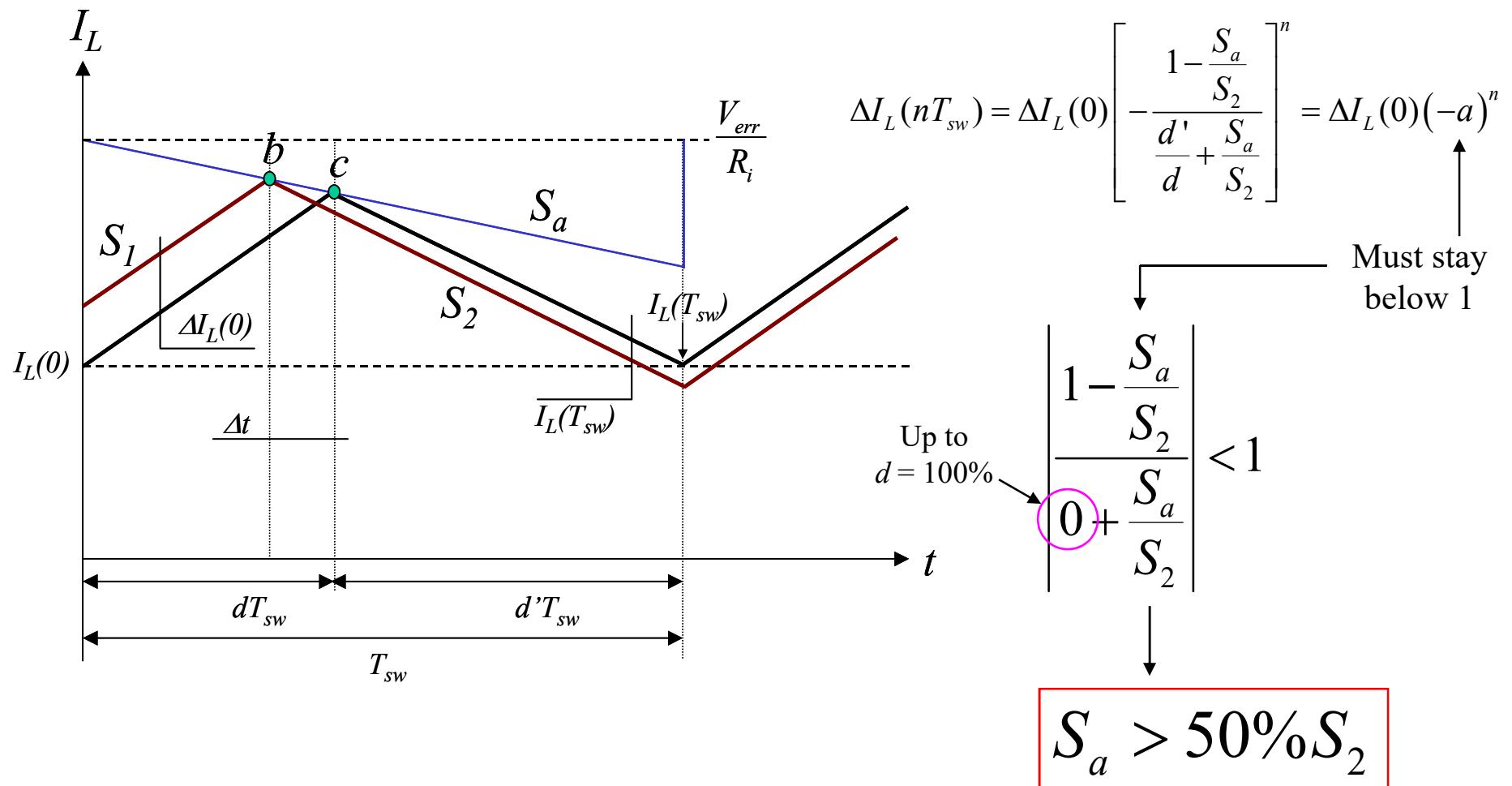


Duty-ratio < 50%



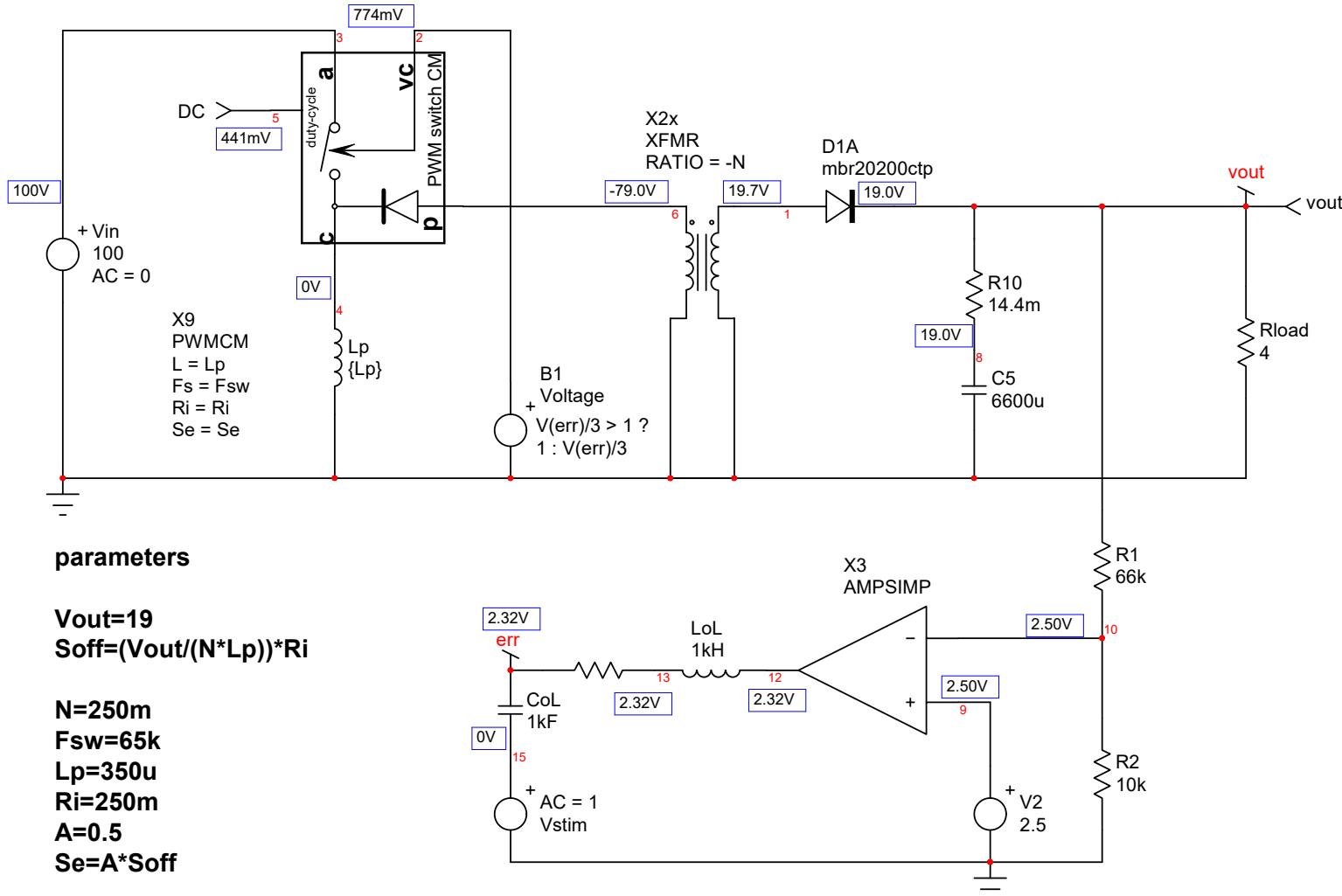
The Cure is in the Ramp

- Injecting a ramp on the feedback signal, damping is obtained



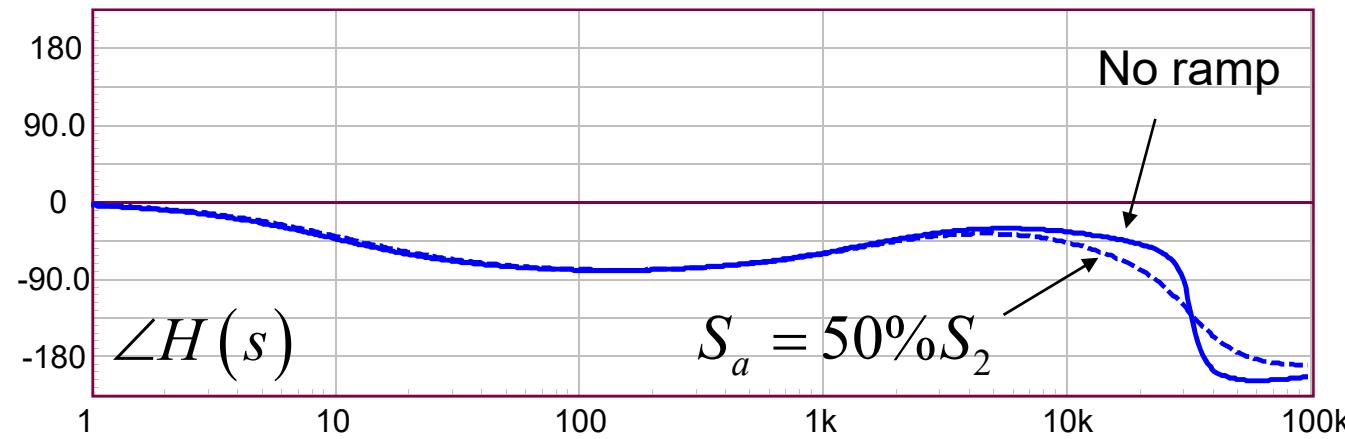
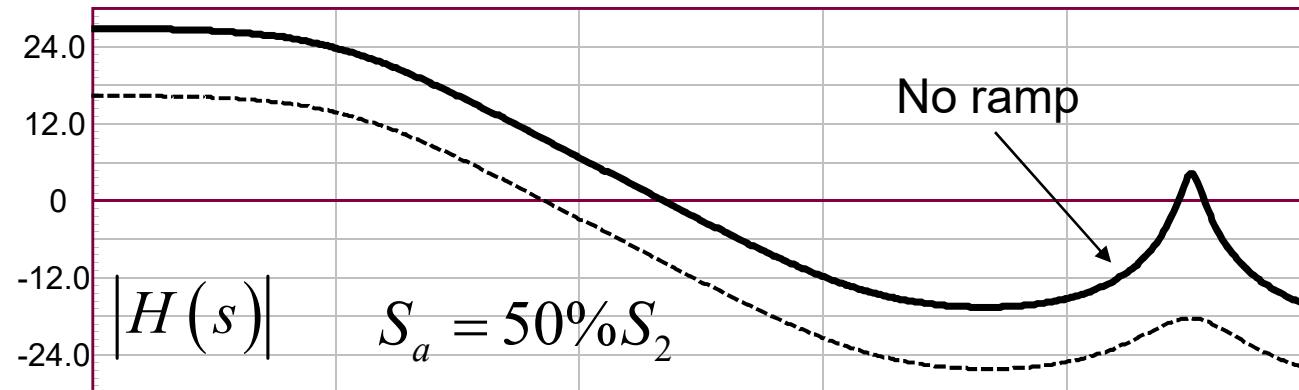
A Model to Simulate a Flyback Converter

- A SPICE model can predict subharmonic instabilities



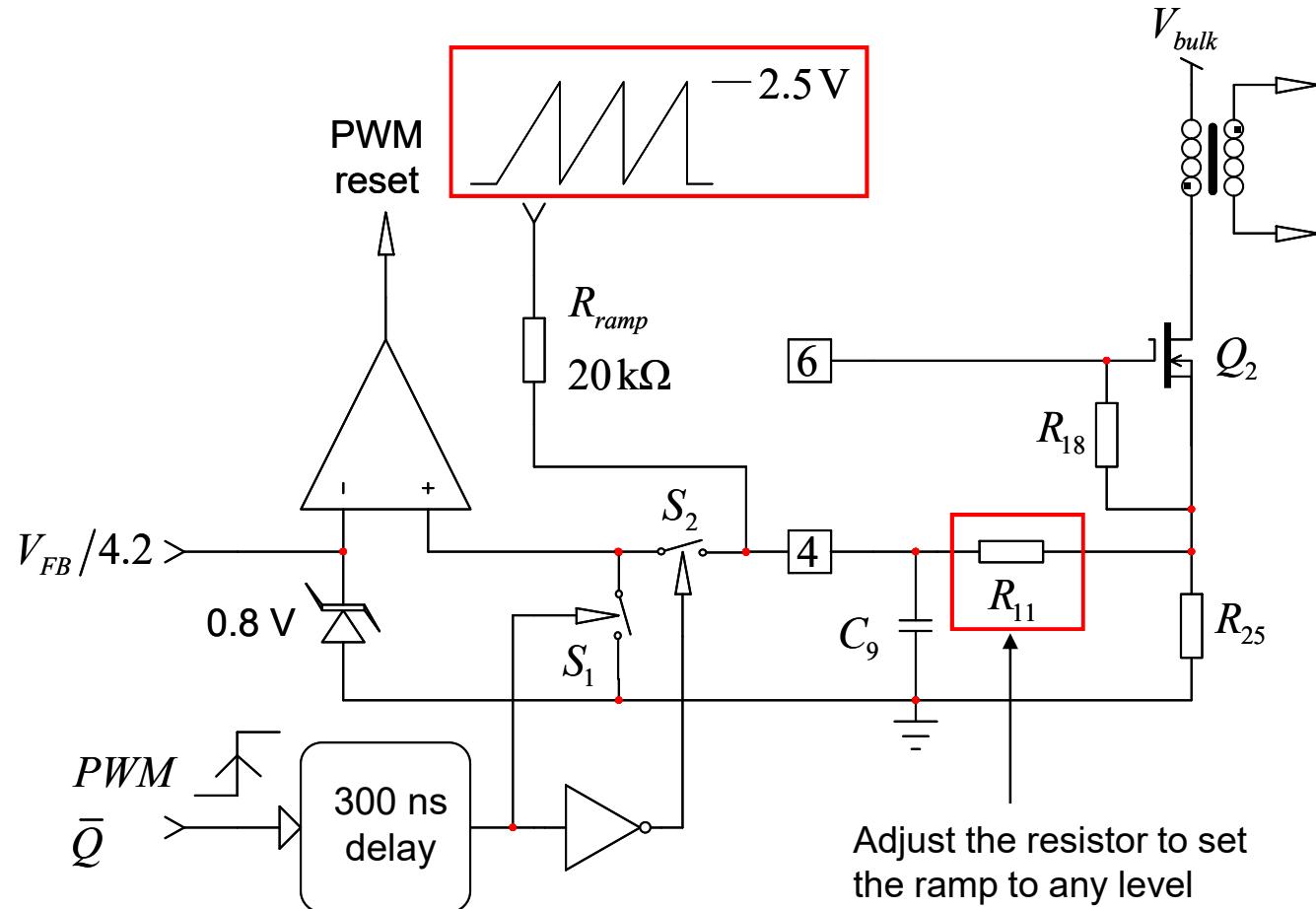
Simulation Results of the CCM Flyback

- ❑ As ramp is injected, the double-pole Q is damped
- ❑ Injecting more ramp turns the converter into voltage-mode



Modern Circuits Include Slope Compensation

- A simple resistor in series with current sense resistor does the job



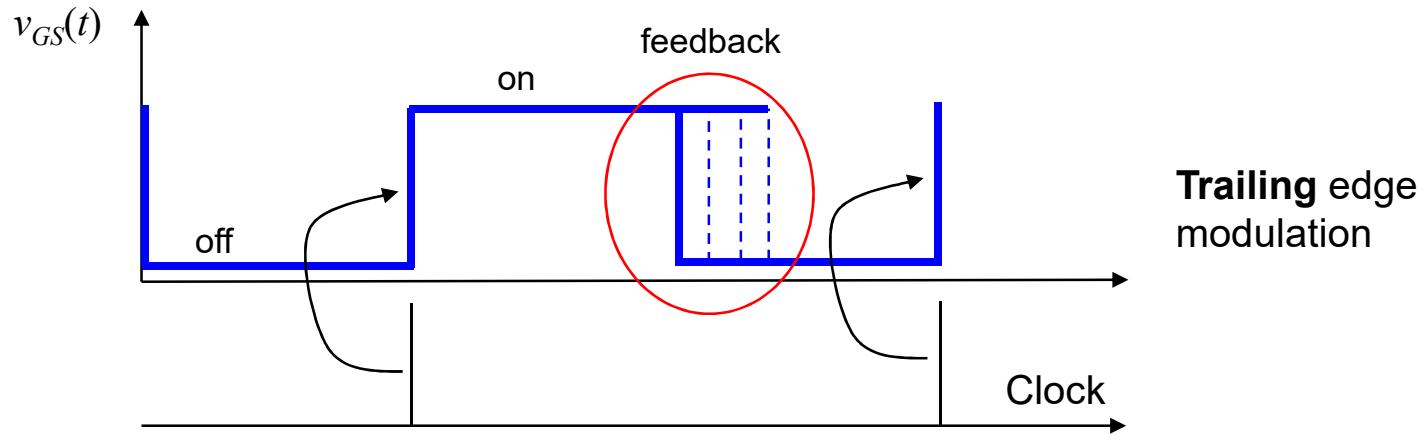
NCP1250

Course Agenda

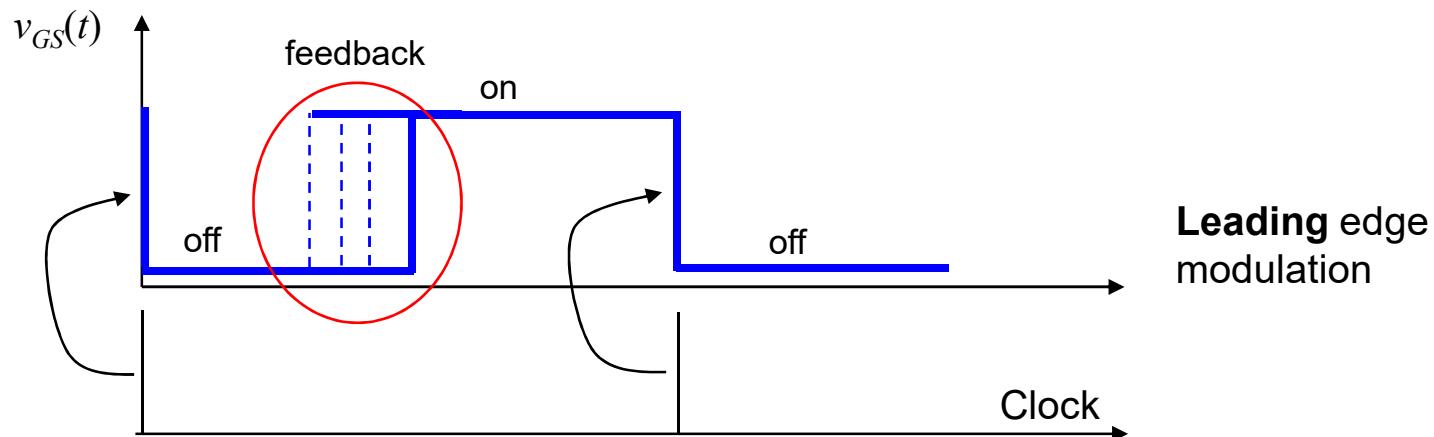
- The Flyback Converter
- The Parasitic Elements
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- **Fixed or Variable Frequency?**
- More Power than Needed
- The Frequency Response
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Modulation Strategies

- The most popular modulation strategy is trailing-edge

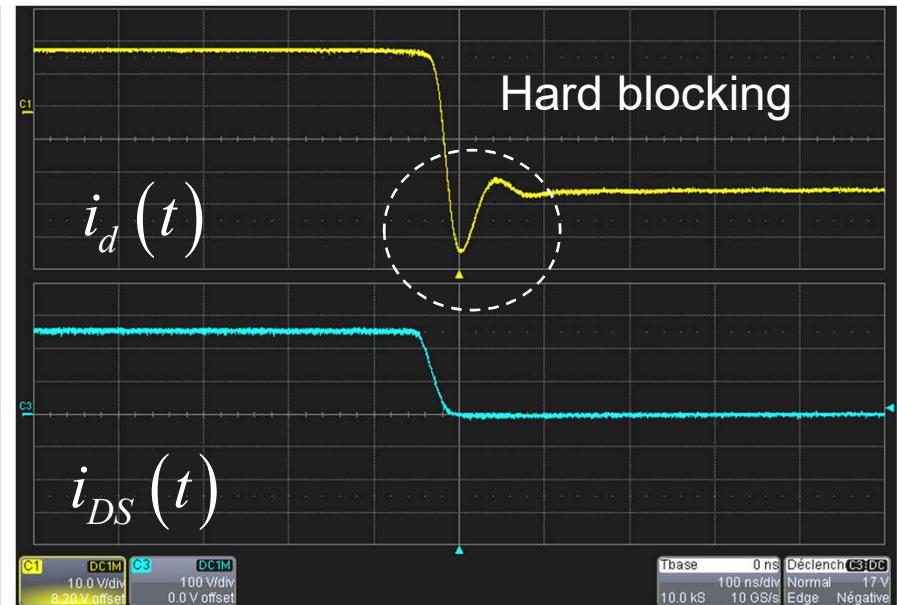
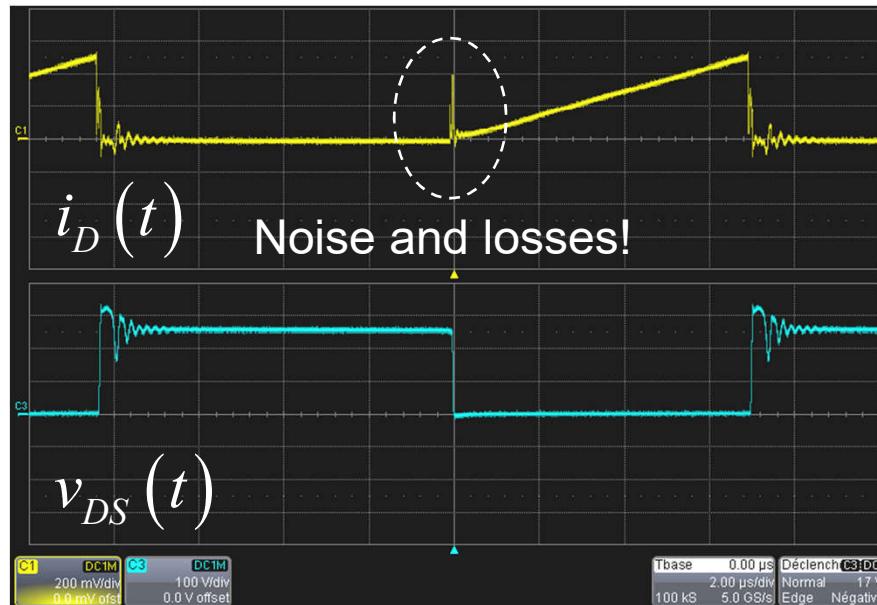


- Leading-edge modulation often appears in post-regulators



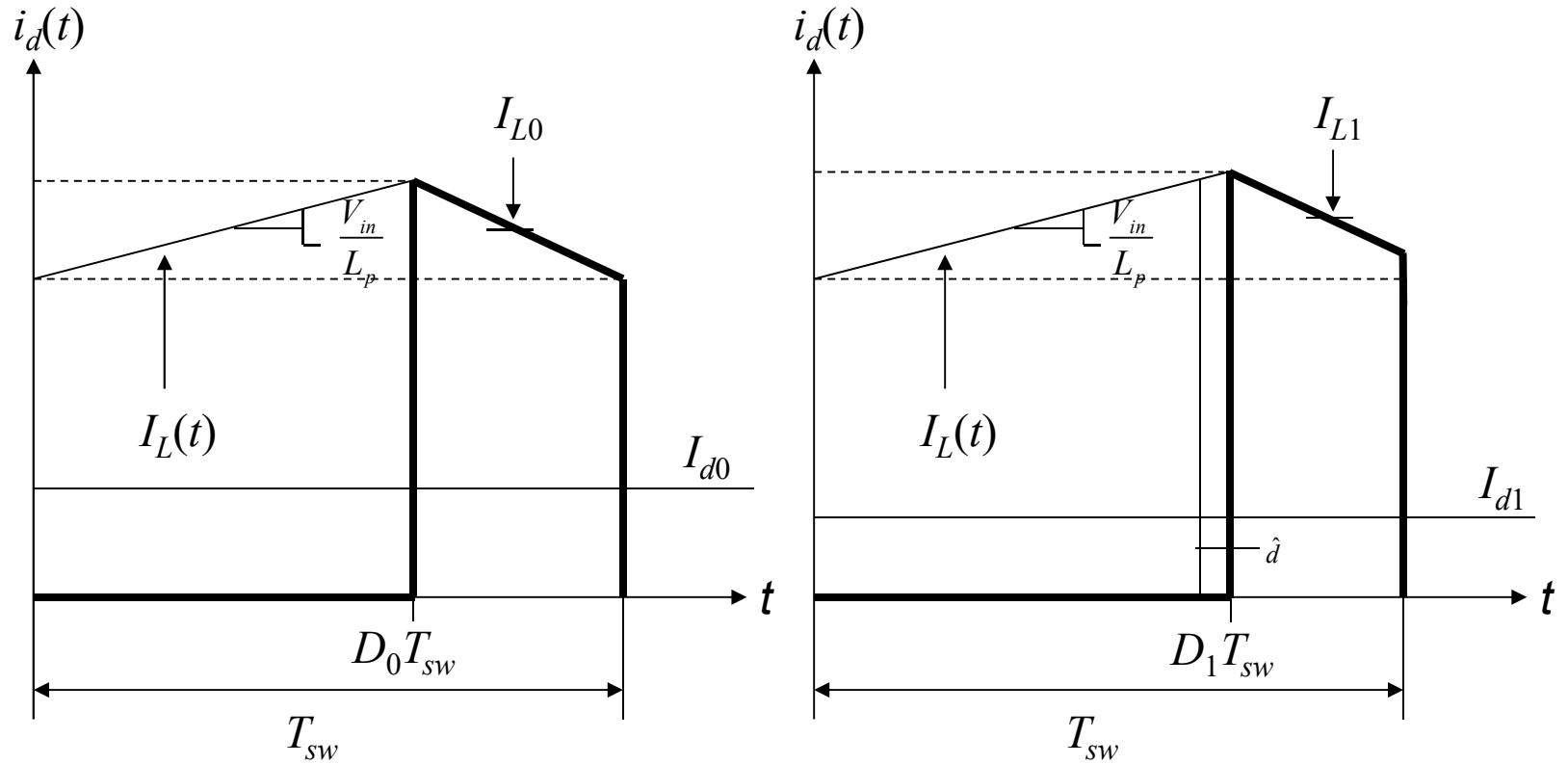
Fixed Frequency Operation

- ❑ The vast majority of converters use fixed-frequency operation
 - Switching losses depend on frequency: high frequency, high losses!
 - Capacitive losses are a brake to efficiency improvement
 - CCM operation induces high losses on the secondary diode
 - Potential shoot-trough hampers synchronous rectification
 - The Right Half-Plane Zero severely limits the available bandwidth



The Right-Half-Plane Zero

- In a CCM flyback, I_{out} is delivered during the off-time:

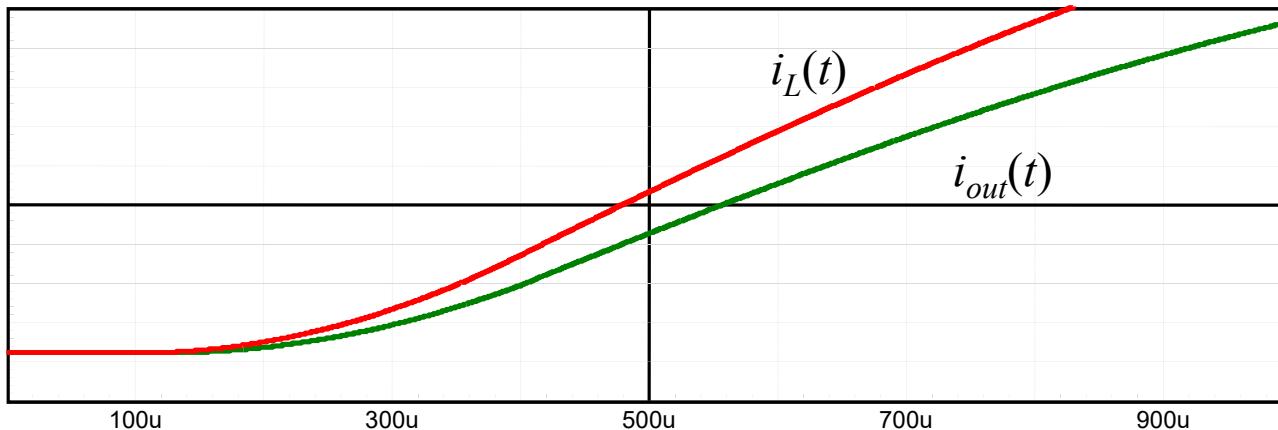
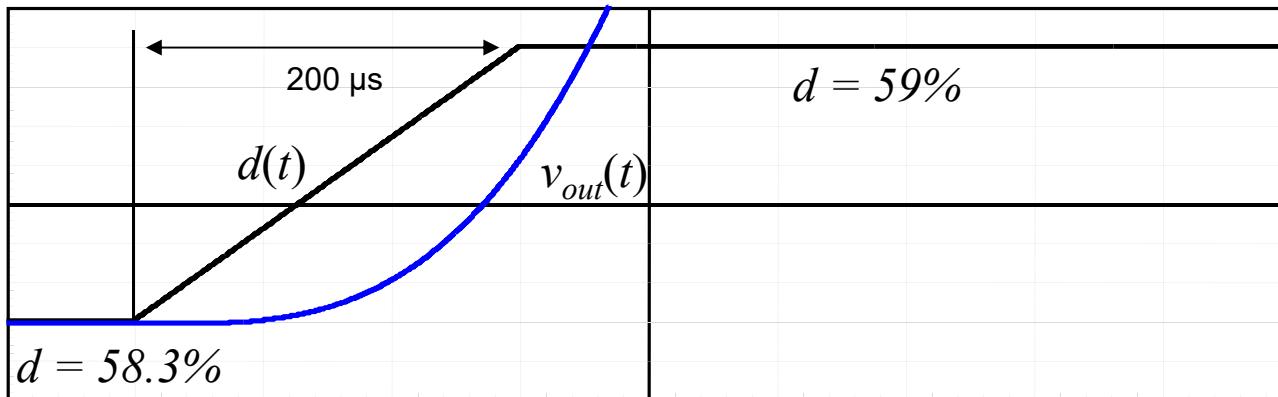


- If D brutally increases, D' reduces and I_{out} drops!
- What matters is the inductor current slew-rate

$$\left\langle \frac{dv_L(t)}{dt} \right\rangle$$

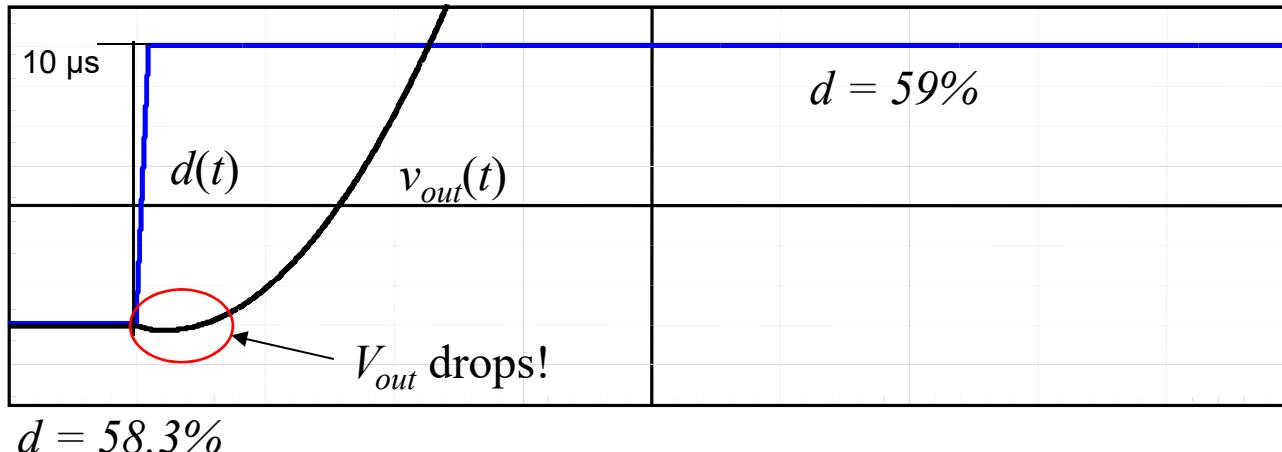
Processing the Output Power Demand

- If $i_L(t)$ can rapidly change, I_{out} increases when D goes up

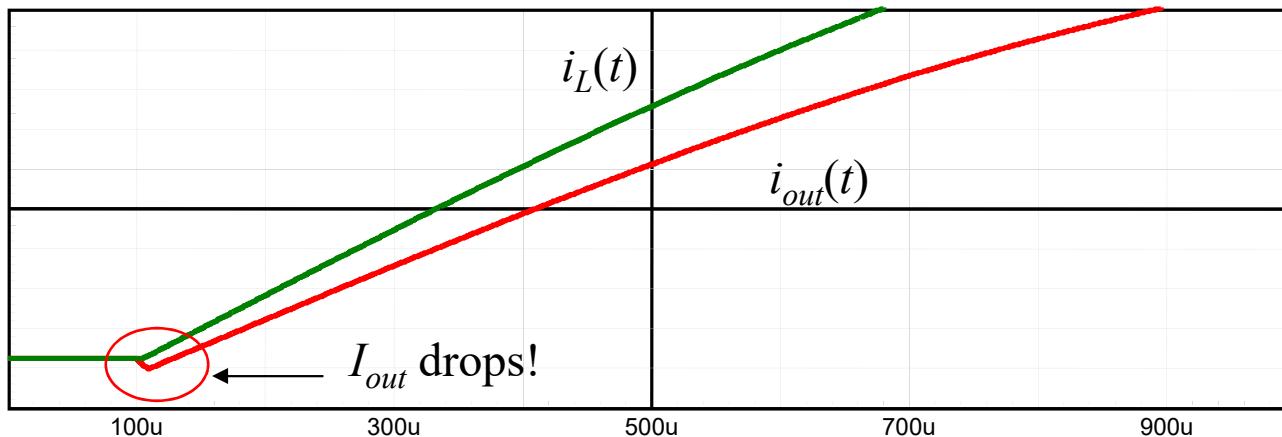


Failing to Increase the Current in Time

- If $i_L(t)$ is limited because of a big L_p , I_{out} drops when D increases



$d = 58.3\%$



The RHPZ is a Positive Root

- Small-signal equations can help us to formalize it

Voltage mode

$$\frac{\hat{v}_{out}(s)}{\hat{d}(s)} = G_0 \frac{\left(1 + \frac{s}{\omega_{z_1}}\right) \left(1 - \frac{s}{\omega_{z_2}}\right)}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

The negative sign indicates a positive root!

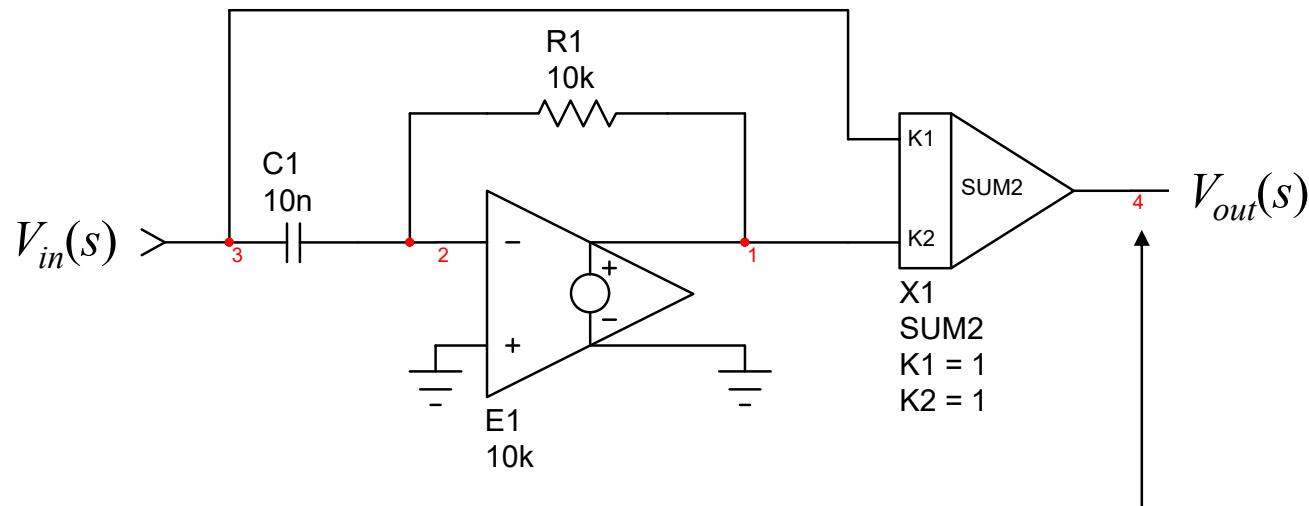
Current mode

$$\frac{\hat{v}_{out}(s)}{\hat{v}_c(s)} = G_0 \frac{\left(1 + \frac{s}{\omega_{z_1}}\right) \left(1 - \frac{s}{\omega_{z_2}}\right) \left(1 + \frac{s}{\omega_{z_3}}\right)}{D(s)}$$
$$\omega_{z_2} = \frac{R_{load} D^2}{N^2 D L}$$

- Voltage mode or current mode, the RHPZ remains the same

Simulating the RHPZ

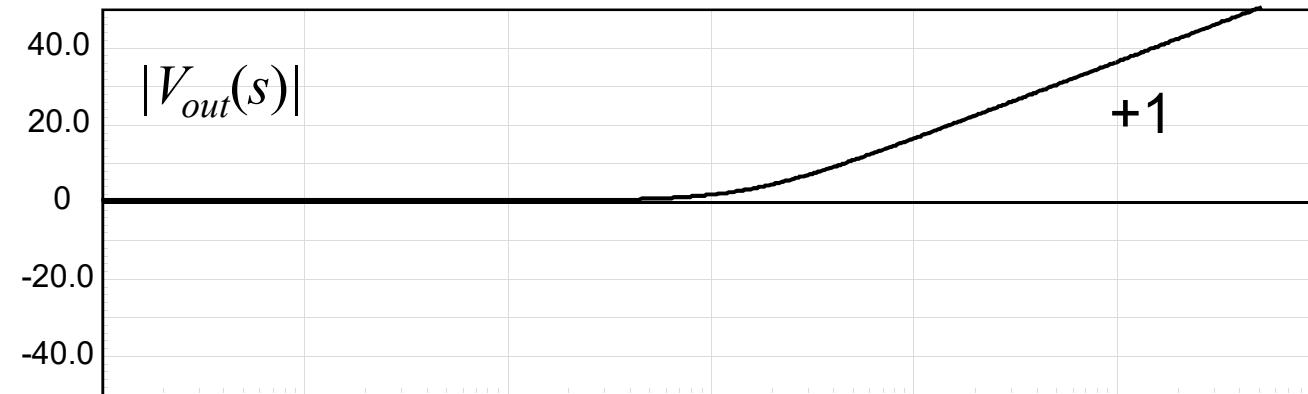
- To limit the effects of the RHPZ, limit the duty ratio slew-rate
- Choose a crossover frequency equal to 20-30% of RHPZ position
- A simple RHPZ can be easily simulated:



$$V_{out}(s) = V_{in}(s) - V_{in}(s) \frac{R_1}{1} = V_{in}(s) \left(1 - \frac{s}{\omega_0} \right)$$

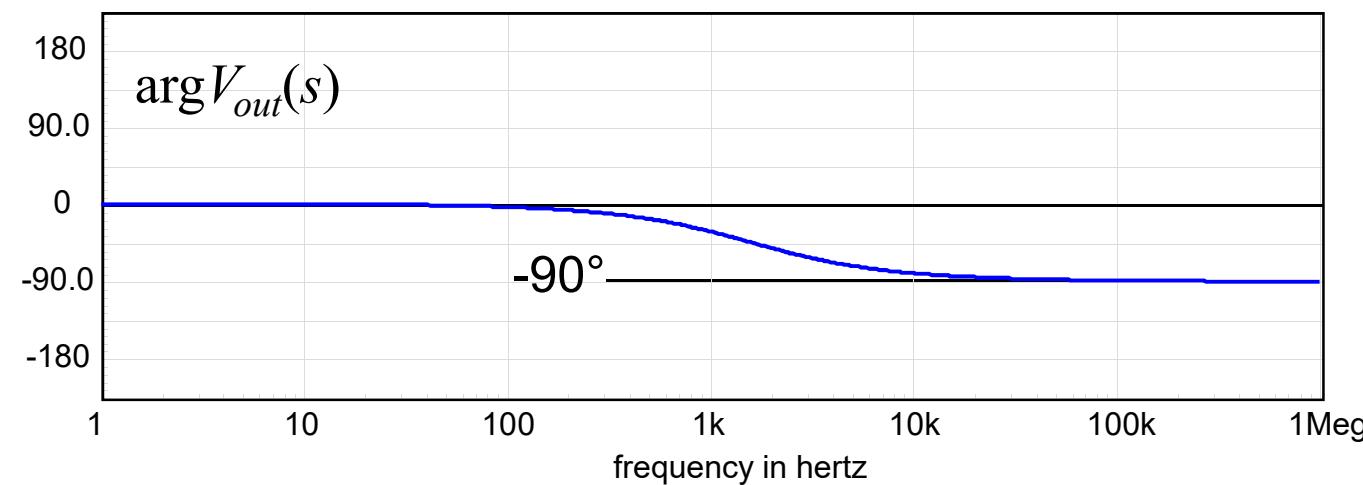
A Zero Producing a Phase Lag

- With a RHPZ we have a boost in gain but a lag in phase!



LHPZ

$$G(s) = 1 + \frac{s}{\omega_0}$$

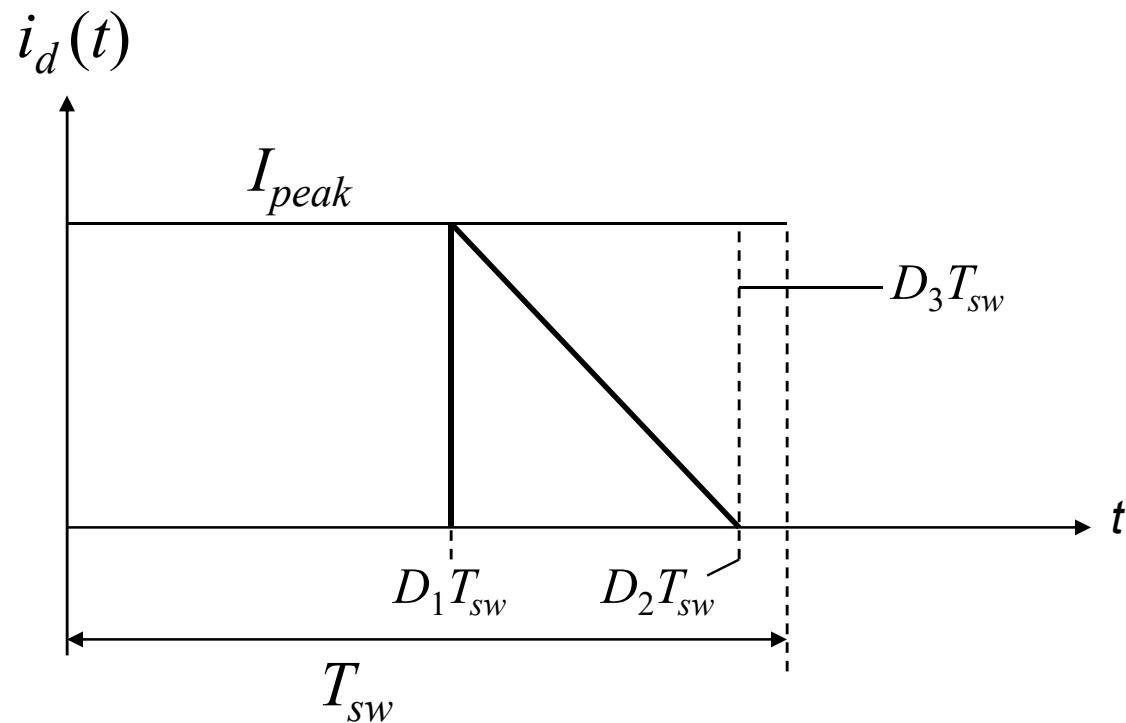


RHPZ

$$G(s) = 1 \boxed{-} \frac{s}{\omega_0}$$

Is There a RHPZ in DCM?

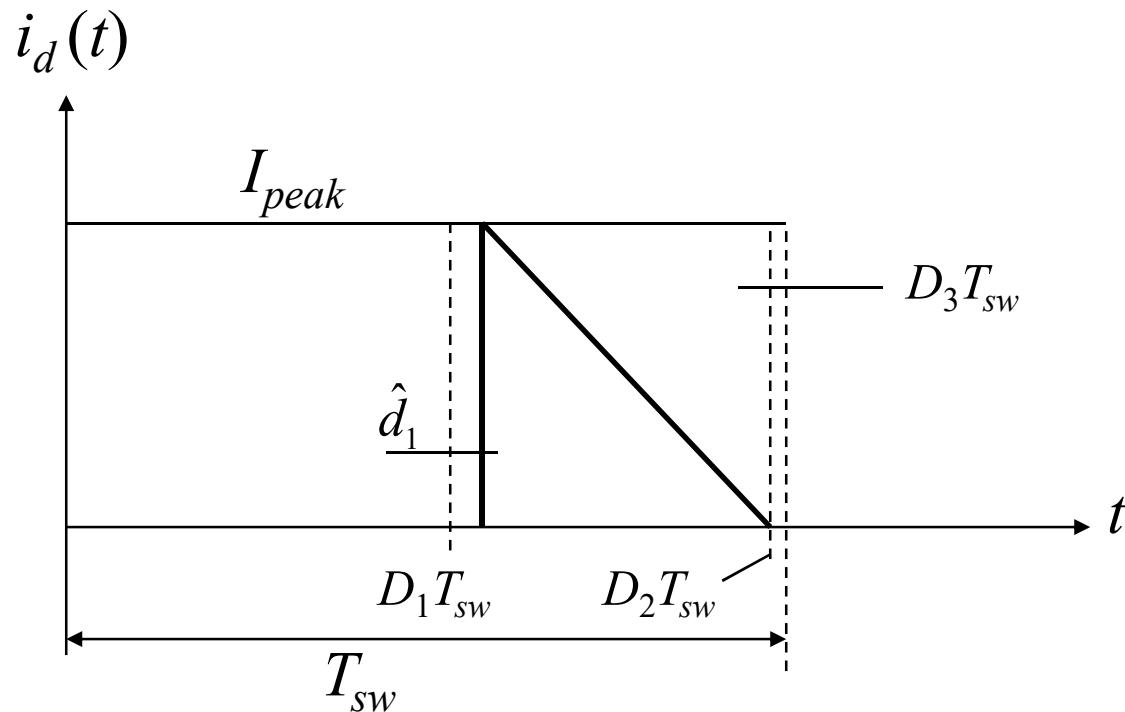
- A RHPZ also exists in DCM boost, buck-boost converters...



- When D_1 increases, $[D_1, D_2]$ stays constant but D_3 shrinks

Is There a RHPZ in DCM?

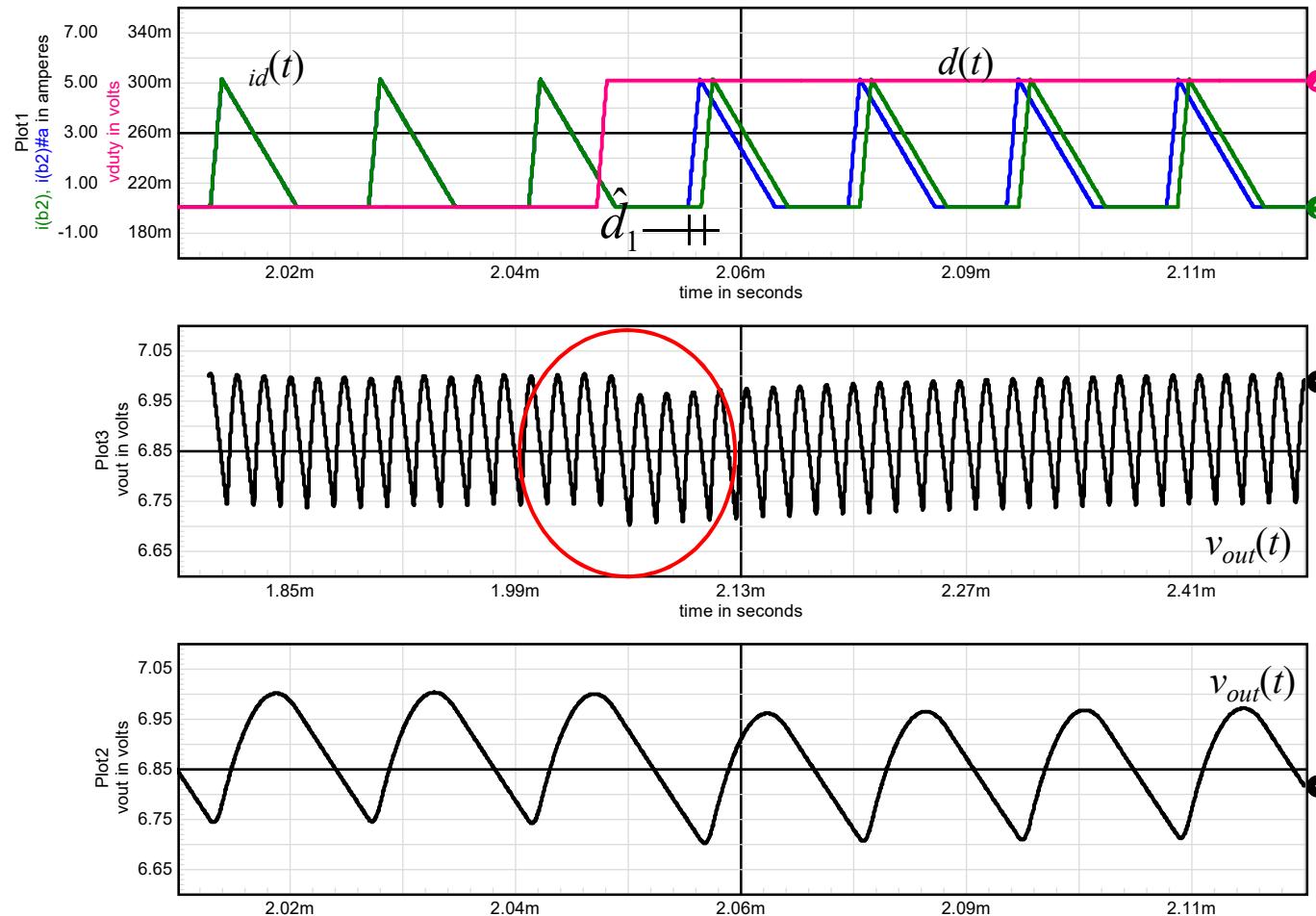
- The triangle is simply shifted to the right by \hat{d}_1



- The refueling time of the capacitor is delayed and a drop occurs

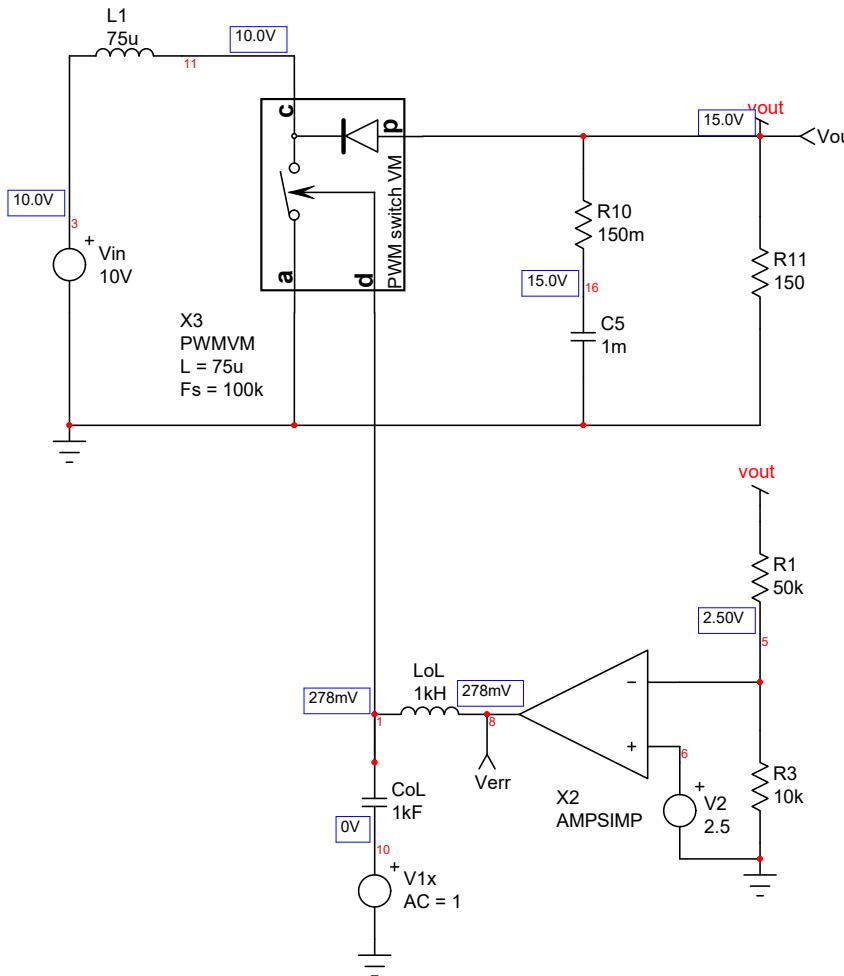
Is There a RHPZ in DCM?

- If D increases, the diode current is delayed by \hat{d}_1



A Large-Signal Model is Available

- Averaged models can predict the DCM RHPZ



$$\frac{\hat{v}_{out}(s)}{\hat{d}(s)} = H_d \frac{(1 + s/s_{z_1})(1 - s/s_{z_2})}{(1 + s/s_{p_1})(1 + s/s_{p_2})}$$

$$s_{z_1} = \frac{1}{C_{out} R_{ESR}}$$

$$s_{z_2} = \frac{R_{load}}{M^2 L}$$

$$s_{p_1} = \frac{2M-1}{M-1} \frac{1}{C_{out} R_{ESR}} \quad s_{p_2} = 2F_{sw} \left(\frac{1-1/M}{D} \right)^2$$

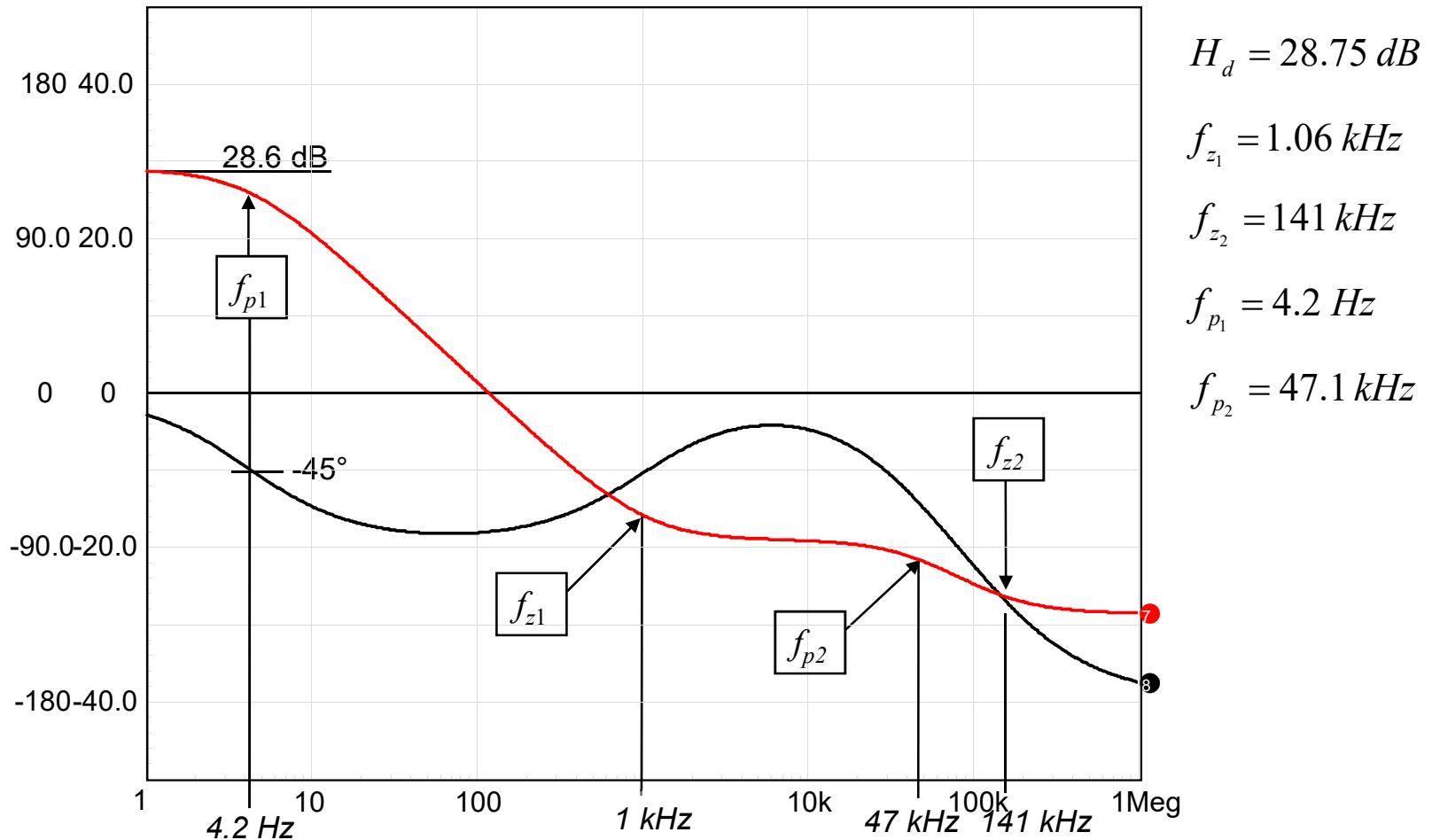
$$H_d = \frac{2V_{out}}{D} \frac{M-1}{2M-1}$$

Merci
Vatché!



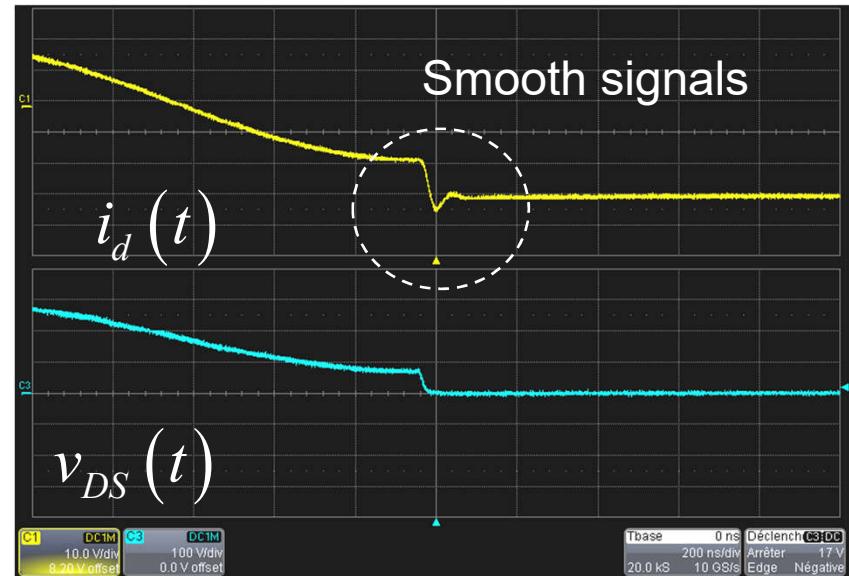
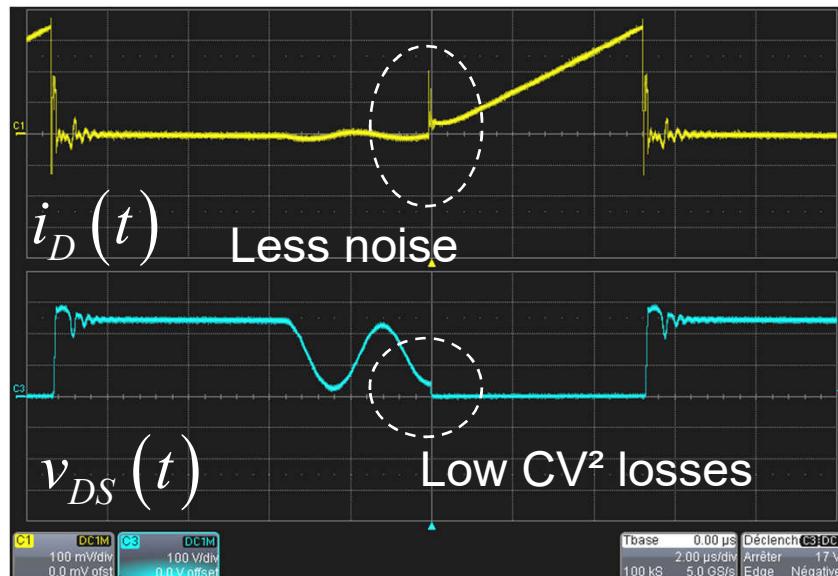
The Model Predicts it!

- Averaged models can predict the DCM RHPZ



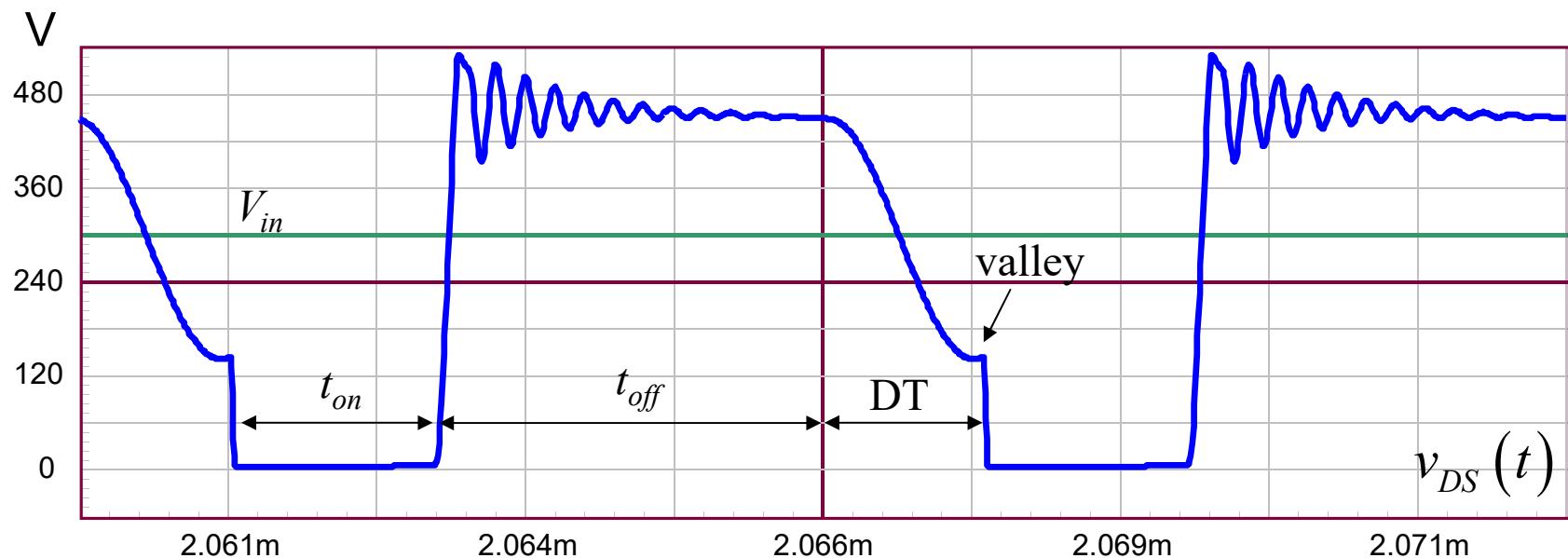
Going to Variable Frequency

- ❑ More converters are using variable-frequency operation
- ❑ This is known as Quasi-Square Wave Resonant mode: QR
 - Valley switching ensures extremely low capacitive losses
 - DCM operation saves losses on the secondary diode
 - Easier synchronous rectification
 - The Right Half-Plane Zero is pushed to high frequencies



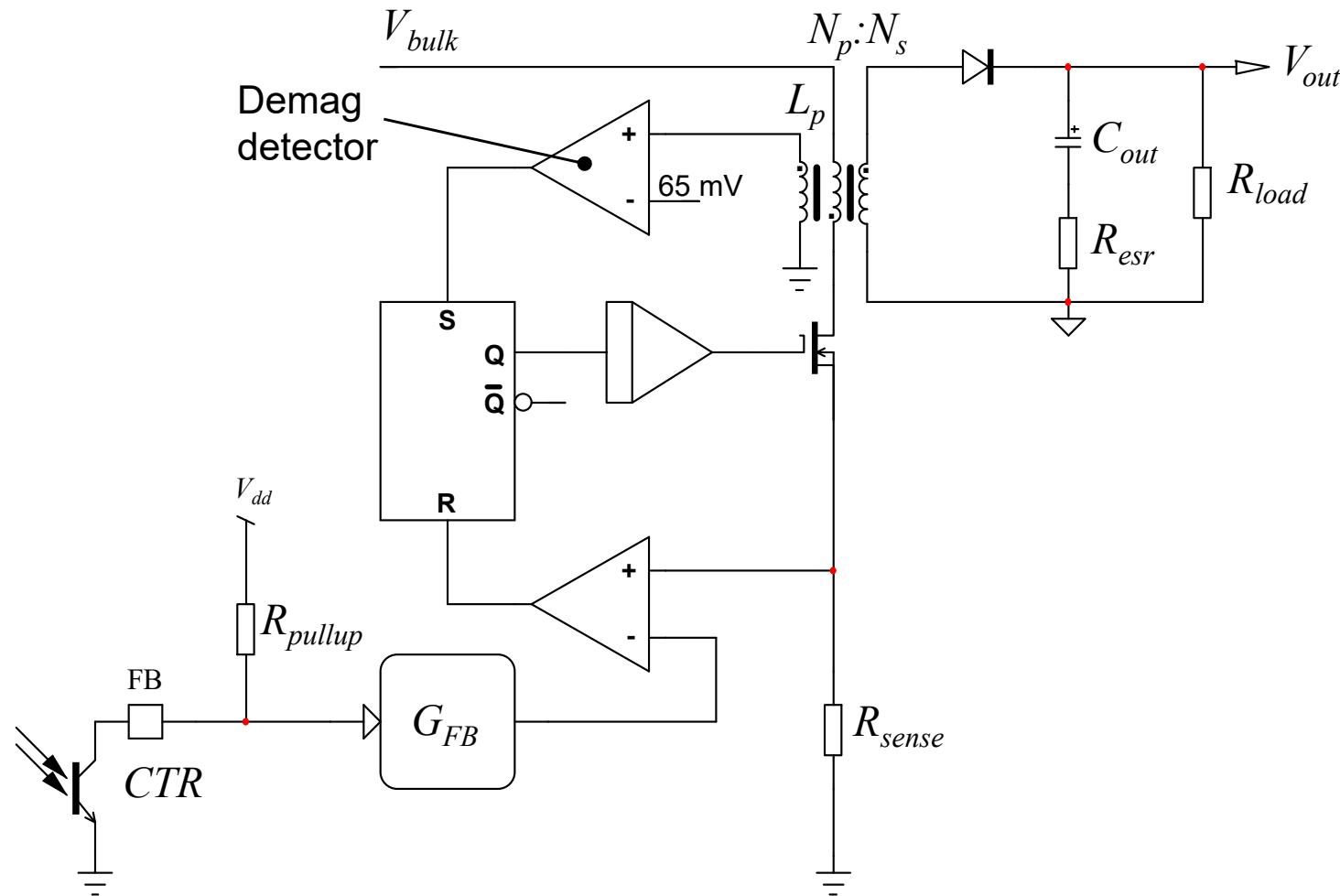
What is the Principle of Operation?

- The drain-source signal is made of peaks and valleys
- A valley presence means:
 - The drain is at a minimum level, capacitors are naturally discharged
 - The converter is operating in the discontinuous conduction mode



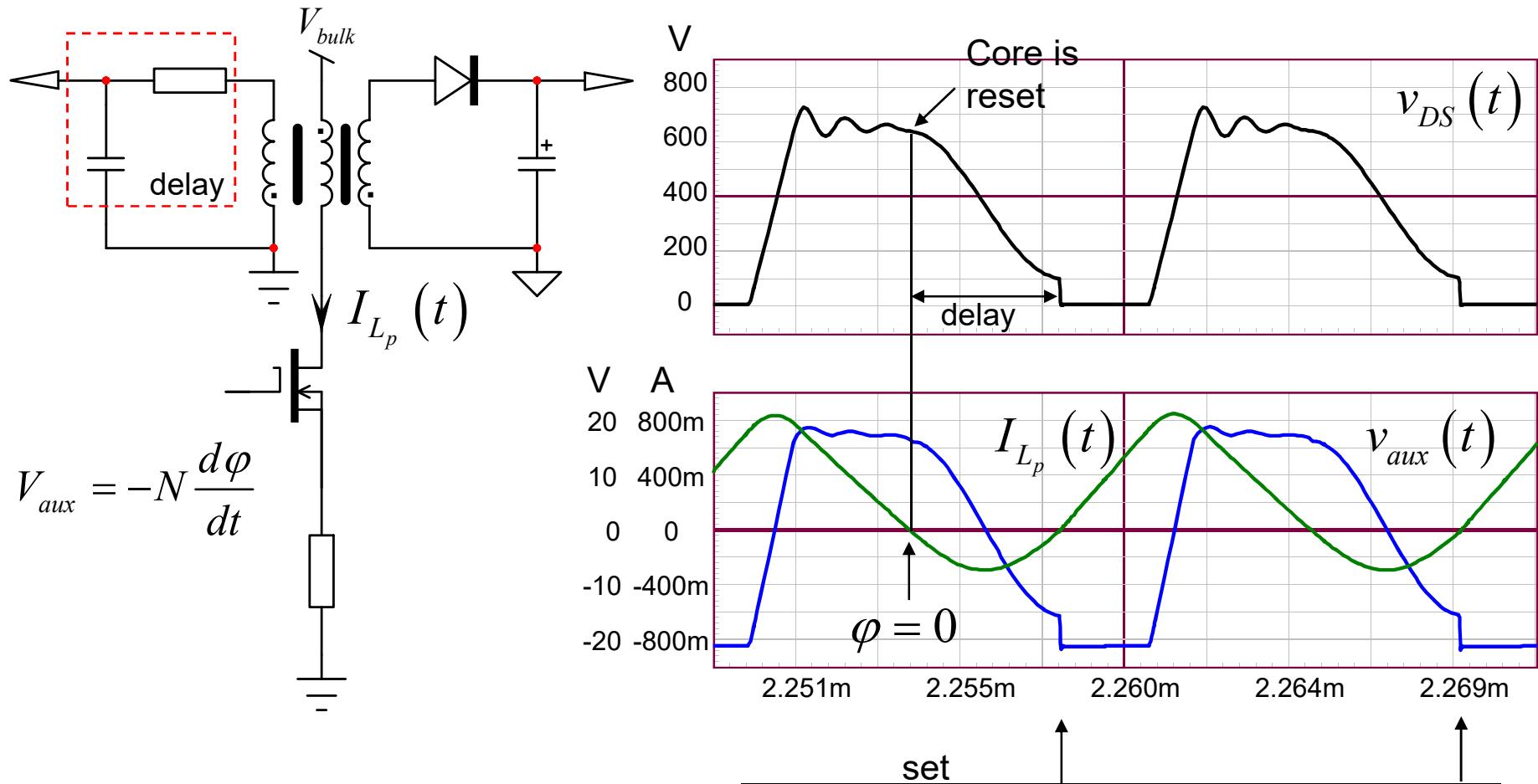
A QR Circuit Does not Need a Clock

- The system is a self-oscillating current-mode converter



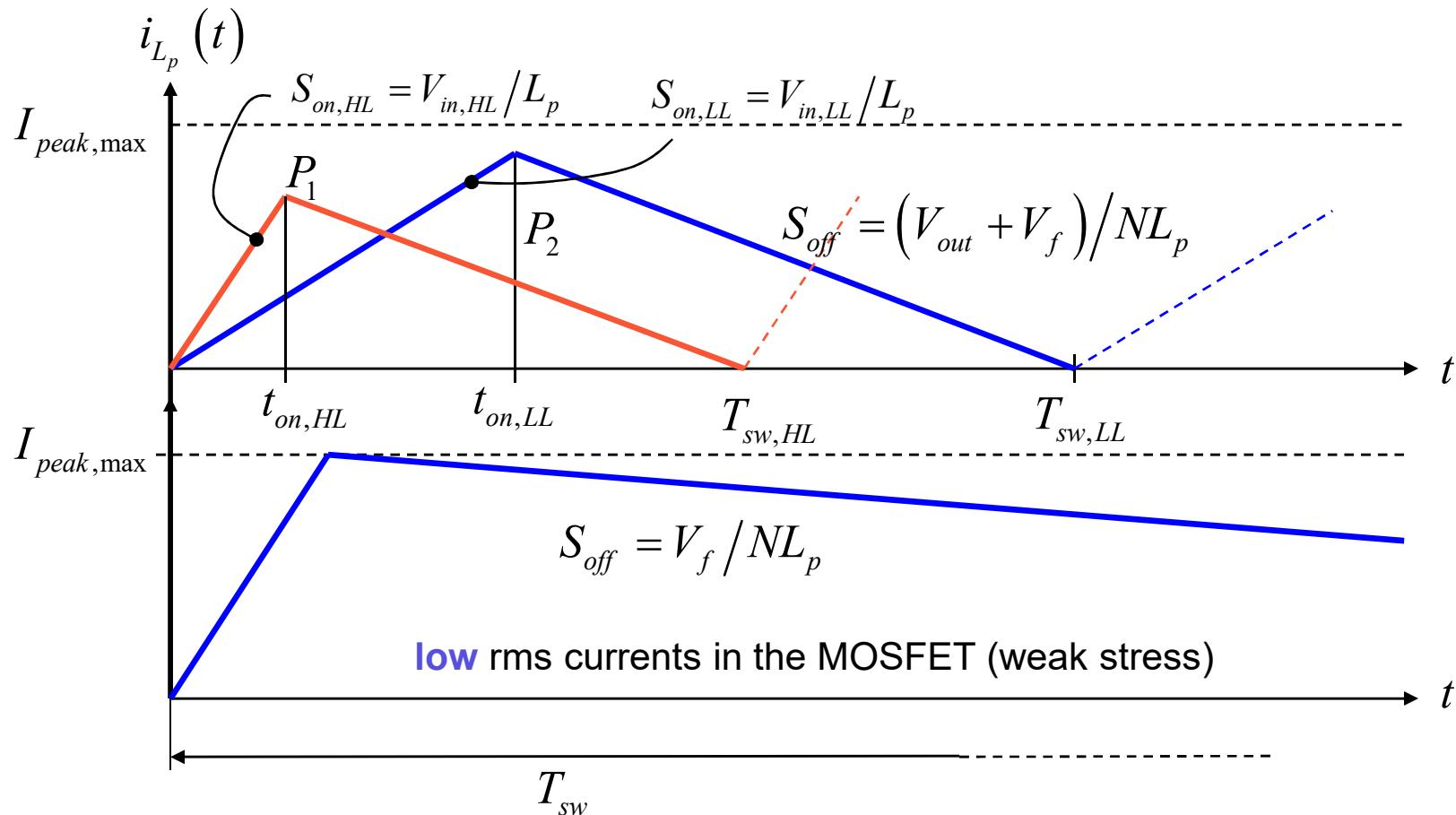
A Winding is Used to Detect Core Reset

- When the flux returns to zero, the aux. voltage drops
- Discontinuous Mode is always maintained



The Frequency Linearly Changes

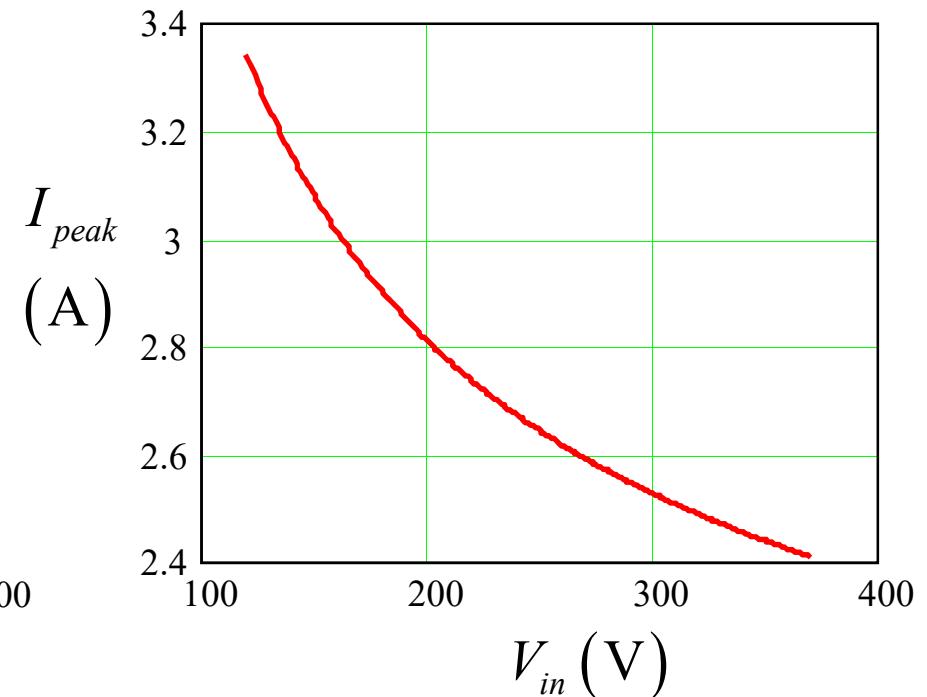
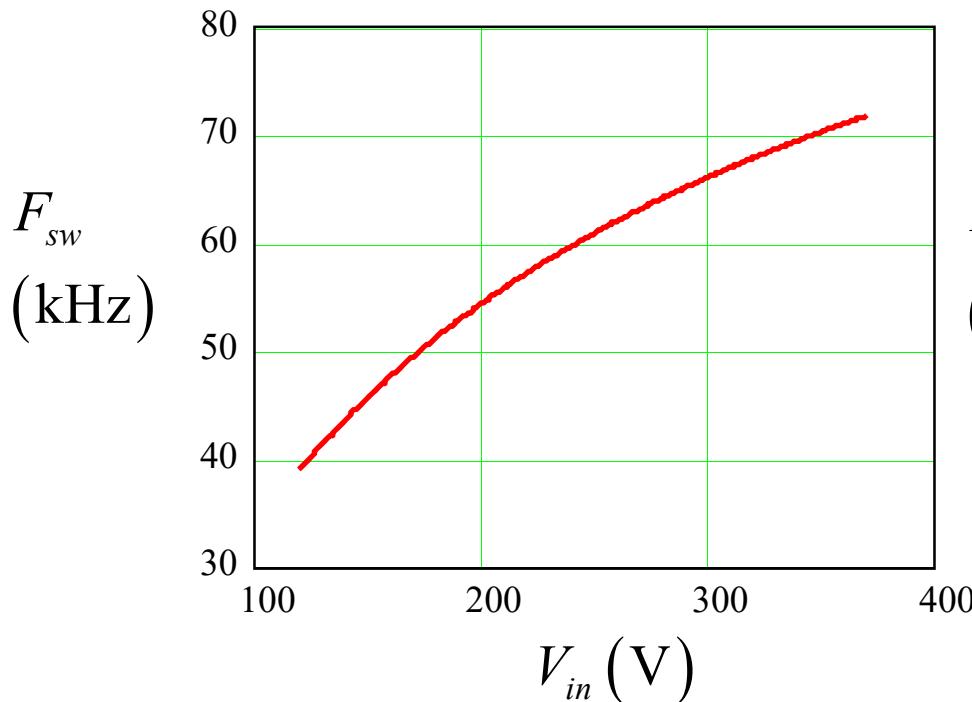
- As the peak current and the on-slope vary, T_{sw} changes



- Excellent behavior in short-circuit conditions!

The Excursion Can be Quite Large

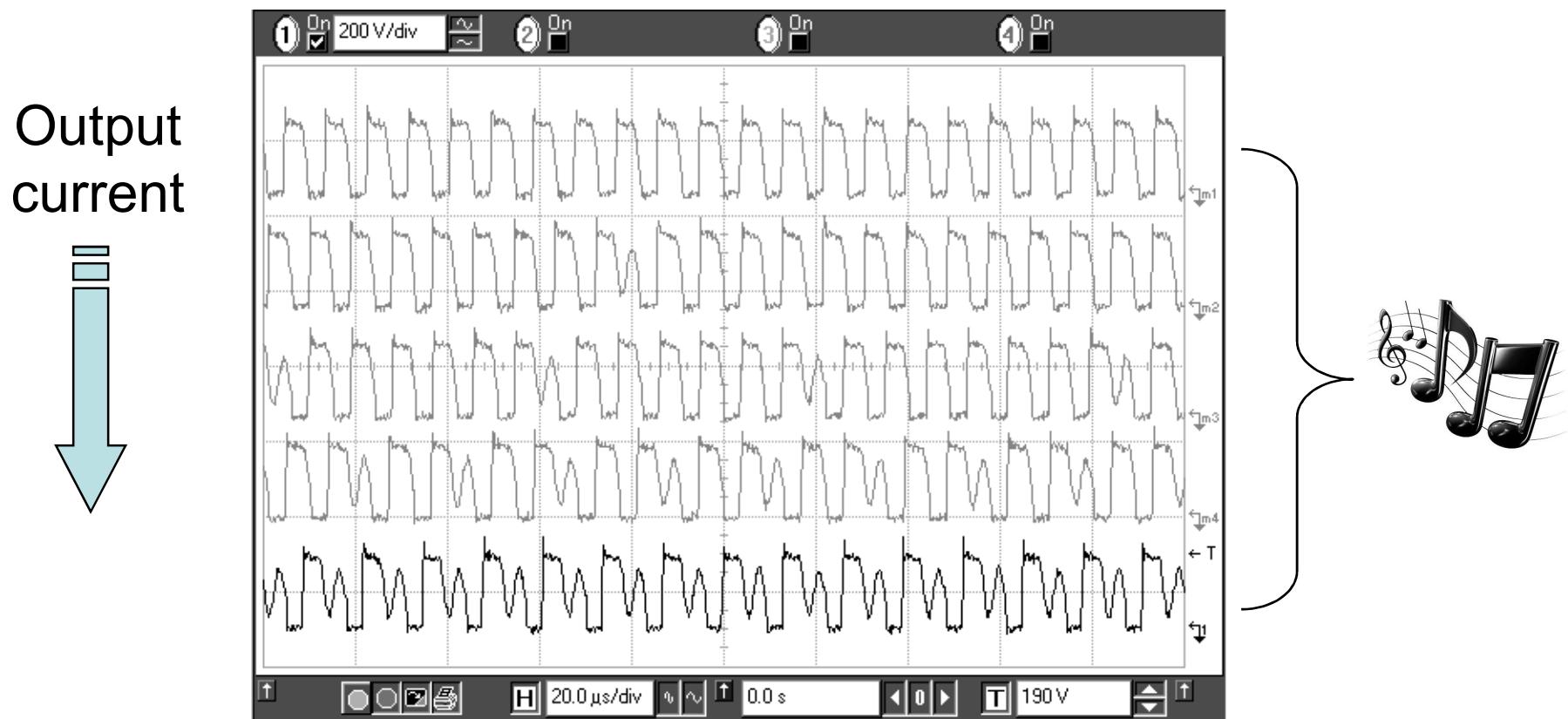
- In heavy load low-line conditions, F_{sw} decreases
- In light-load and high-line operations, F_{sw} can go very high



- EMI and switching losses are at stake as F_{sw} goes up
- Standby power obviously suffers from this condition

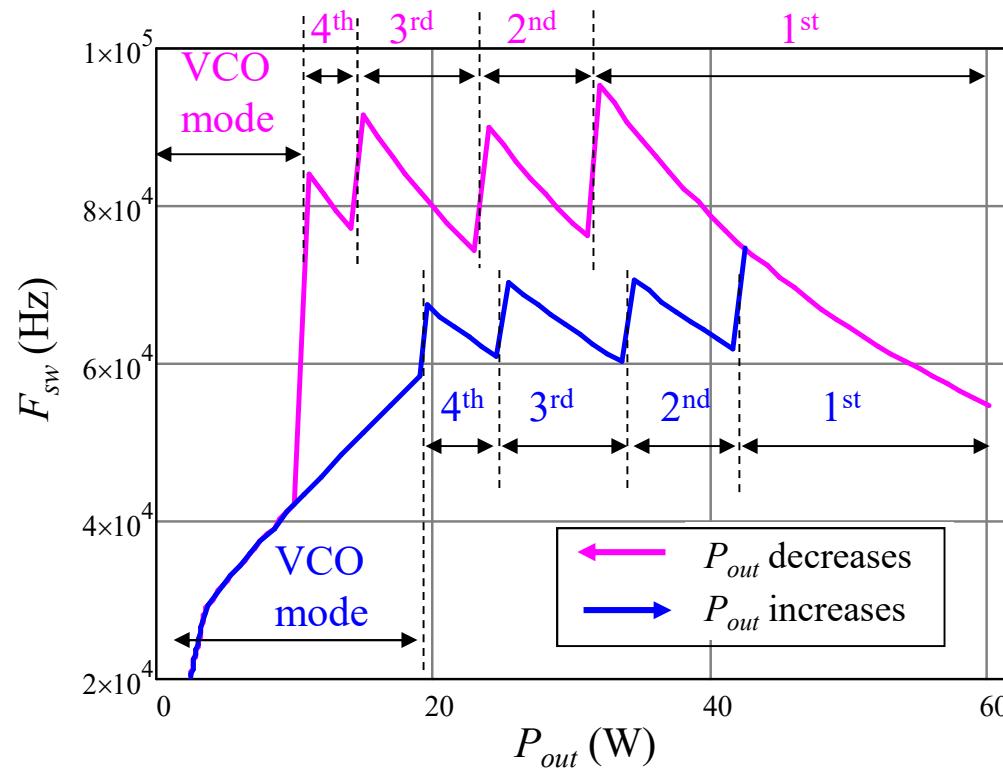
In a Bounded System Discrete Jumps

- As the load gets lighter, the frequency goes to the sky
- Modern controllers fold the frequency back with a VCO
- Problem, the only places to re-start are valleys: discrete jumps



New Controllers Lock in the Valleys

- To prevent the noise, the NCP1380 locks the valley
- The current is allowed to move within a certain limit
- When it exceeds this limit, the controller selects a new valley
- As the load gets lighter, a VCO takes over and reduce F_{sw}



NCP1379/1380

Course Agenda

- ❑ The Flyback Converter
- ❑ The Parasitic Elements
- ❑ How These Parasitics Affect your Design?
- ❑ Current-Mode is the Most Popular Scheme
- ❑ Fixed or Variable Frequency?
- ❑ More Power than Needed**
- ❑ The Frequency Response
- ❑ Compensating With the TL431

What is The Problem?

- ❑ A converter is designed to operate on wide mains – 85 to 265 V rms
- ❑ It can deliver a maximum power before protection trips
- The maximum power delivered at high line is larger than that at low line



85 V rms to 265 V rms

Increase load
until protection
trip.

What Does the Standard Say?

- There is a test called Limited Power Source, LPS
- The maximum power the converter can deliver must be clamped
- If clamped, the manufacturer can use inferior fire proofing materials

Output Voltage V_{out} (V)		Output Current I_{out} (A)	Apparent Power S (VA)
V_{rms}	V_{dc}		
≤ 20	≤ 20	≤ 8	$\leq 5 \cdot V_{out}$
$20 < V_{out} \leq 30$	$20 < V_{out} \leq 30$	≤ 8	≤ 100
-	$20 < V_{out} \leq 60$	$\leq 150/V_{out}$	≤ 100

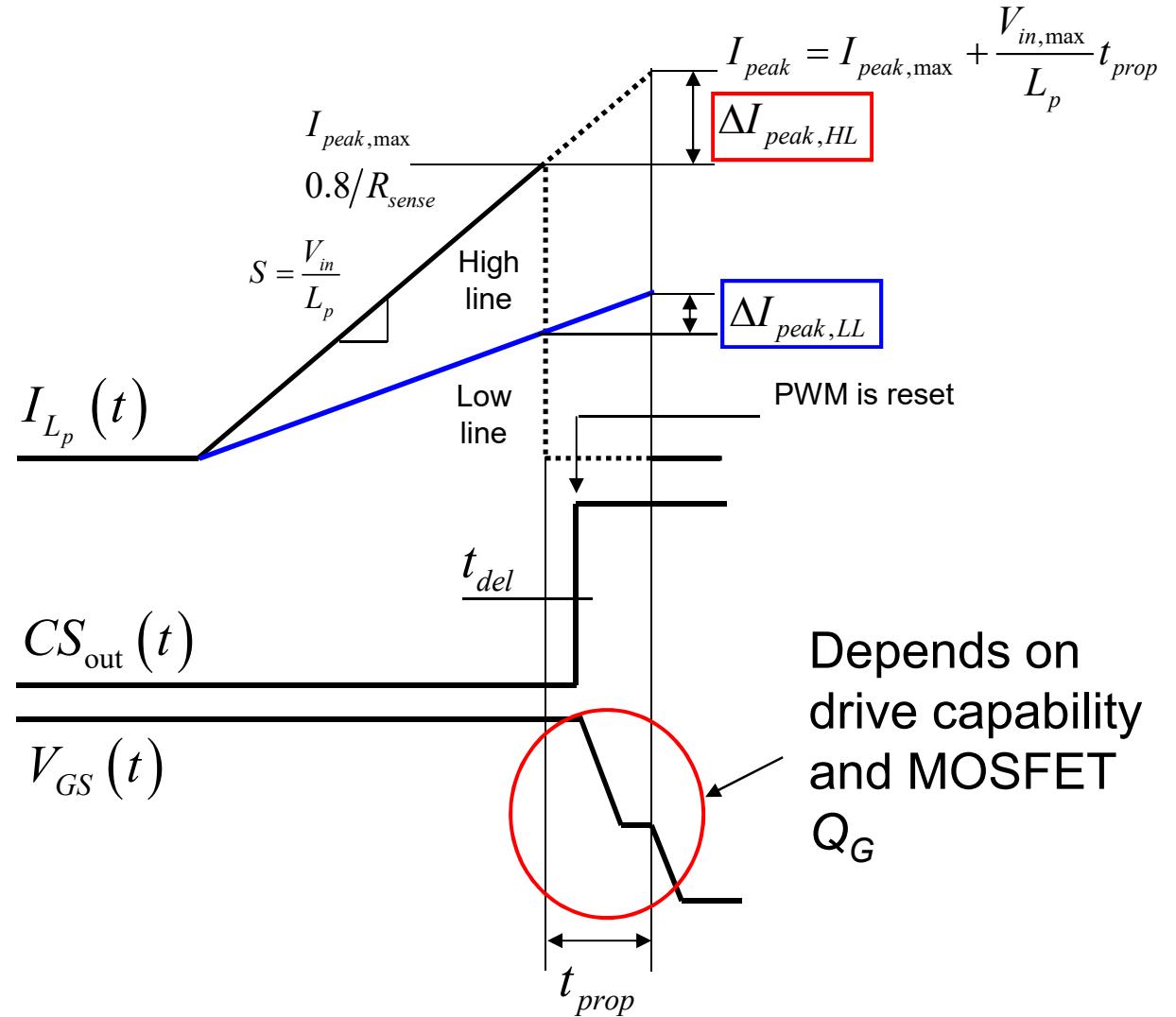
19-V adapter, $I_{out,max} = 5$ A



IEC950 safety standard

Why the Power Runs Away in a Flyback?

- The inductor current slope increases at high line.
- The controller takes time to react to an overcurrent situation.
- The inductor current keeps growing until the MOSFET turns off.
- The overshoot is larger at higher slopes (High V_{in})

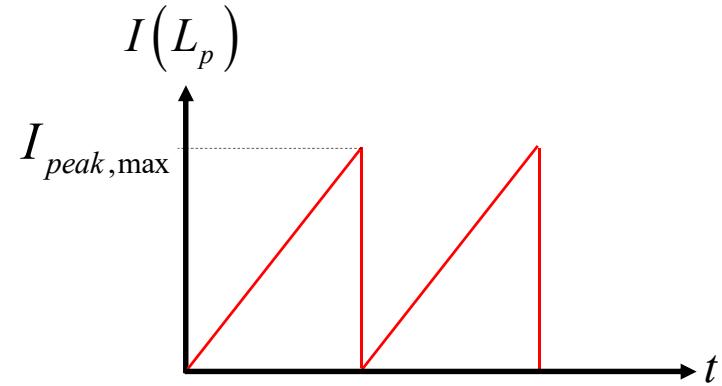


The Effect in a DCM Converter

- A flyback converter operated in DCM obeys the formula:

$$P_{out} = \frac{1}{2} L_p I_{peak,max}^2 F_{sw} \eta$$

↑ ↑ ↑ ↑
 Primary Max. peak Switching Converter
 inductor current in frequency efficiency
 fault



- As L_p and F_{sw} are fixed, $I_{peak,max}$ changes with line input

$$I_{peak,max,LL} = \frac{V_{sense}}{R_{sense}} + \frac{V_{in,LL}}{L_p} t_{prop}$$

Low line

$$I_{peak,max,HL} = \frac{V_{sense}}{R_{sense}} + \frac{V_{in,HL}}{L_p} t_{prop}$$

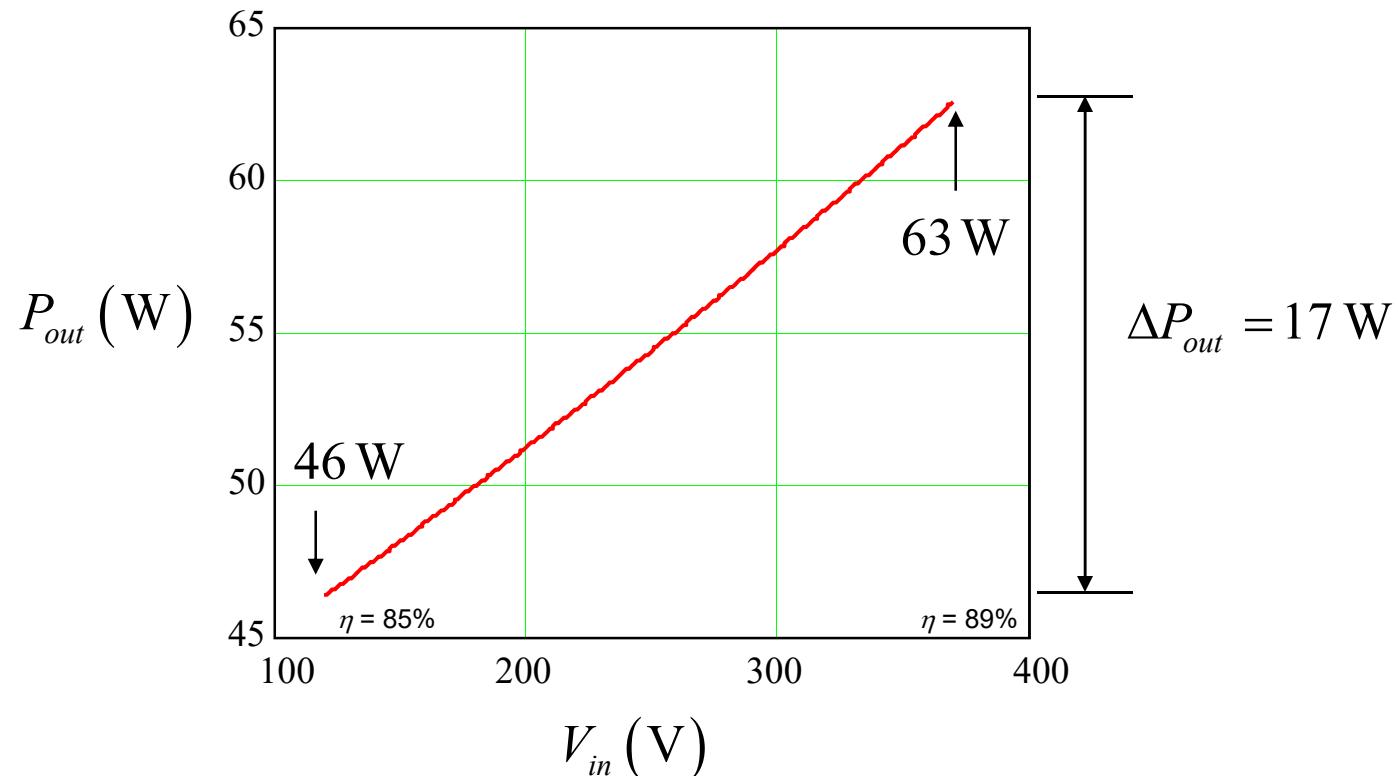
High line

$$\frac{\Delta I_{peak}}{I_{peak,max,HL}} = \frac{V_{in,HL} - V_{in,LL}}{\frac{L_p V_{sense}}{t_{prop} R_{sense}} + V_{in,LL}}$$
$$(1.13)^2 = 1.28$$

A 13.5% overshoot translates
in a 28% power increase
(η is considered constant over the range)

The Power Increases at High Line

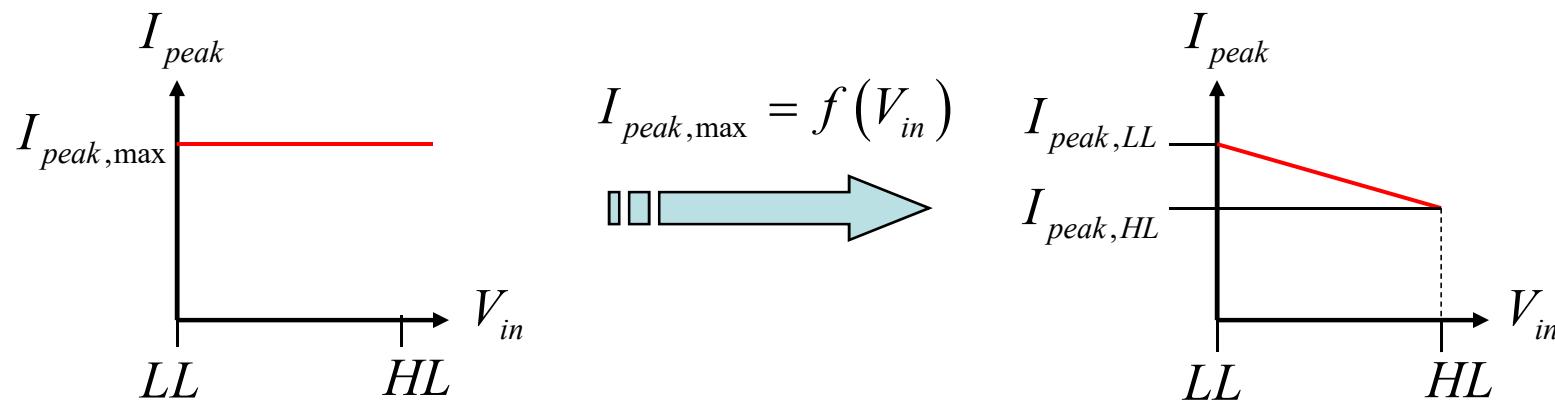
- $L_p = 250 \mu\text{H}$, $V_{sense} = 1 \text{ V}$, $t_{prop} = 350 \text{ ns}$, $V_{in,LL} = 120 \text{ V}$, $V_{in,HL} = 370 \text{ V}$, $R_{sense} = 0.33 \Omega$, $F_{sw} = 65 \text{ kHz}$



- In this example, the converter stays DCM on the whole range.

How to Compensate the Runaway?

- How do we compensate this excess of power?
 - we reduce the maximum peak current at high line
 - this is called Over Power Protection – OPP



- How to calculate the compensated high-line current?
 - ❖ Equate low-line power with high-line power and solve for I_{peak}

$$P_{out,max,HL} = \frac{1}{2} L_p I_{peak,max,HL}^2 F_{sw} n_{HL}$$

→ Solve for I_{peak}

Reducing the Peak Current

- The final inductor peak current must equal:

$$I_{peak,max,HL} = \sqrt{\frac{2P_{out,max,LL}}{L_p F_{sw} \eta_{HL}}}$$

- The compensated setpoint must subtract the prop. delay

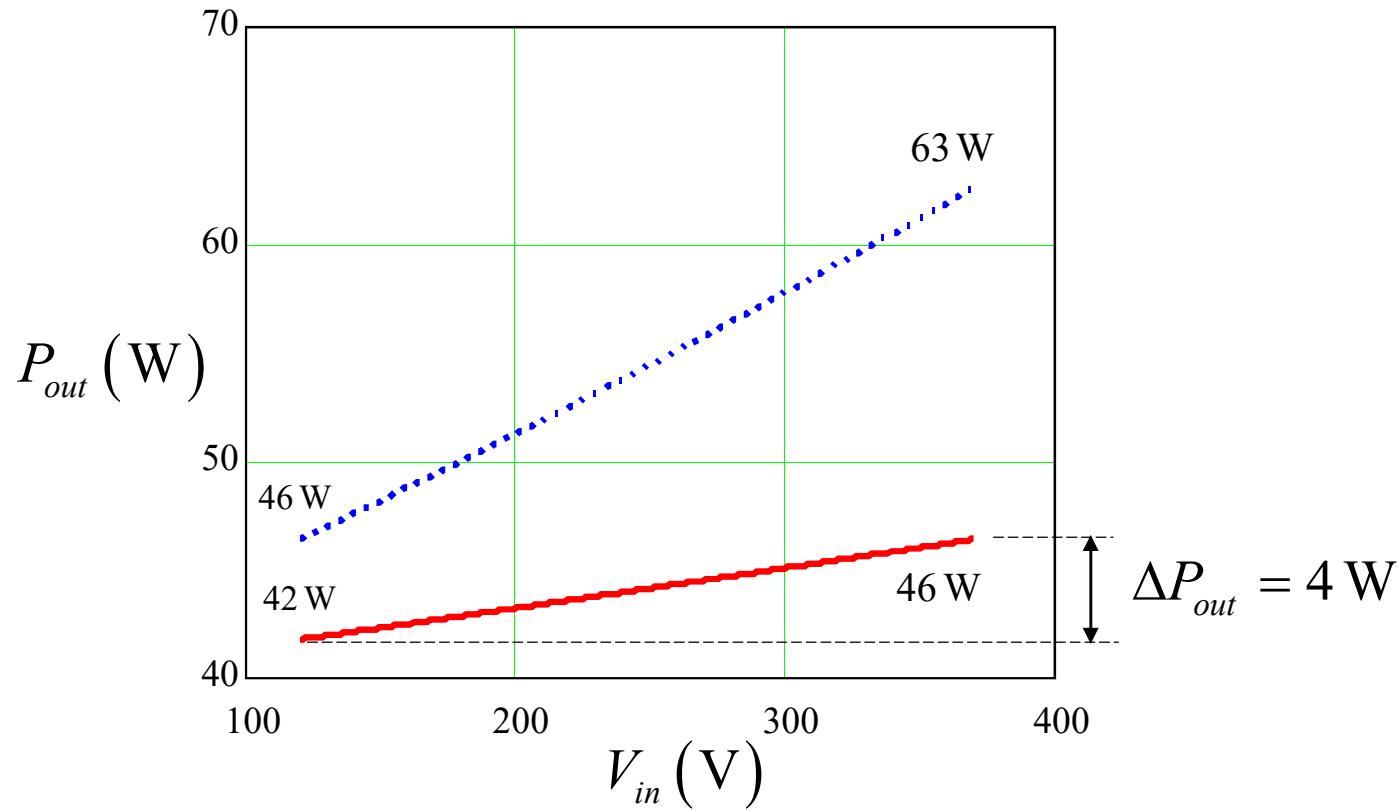
$$\frac{V_{sense}}{R_{sense}} = I_{peak,max,HL} - \frac{V_{in,HL}}{L_p} t_{prop}$$

- The amplitude of the sensed voltage must reduce by:

$$\Delta V = V_{sense} - \left(I_{peak,max,HL} - \frac{V_{in,HL}}{L_p} t_{prop} \right) R_{sense}$$

For What Final Result?

- Thanks to the OPP, the power stays under control



The CCM Case is a Different Picture

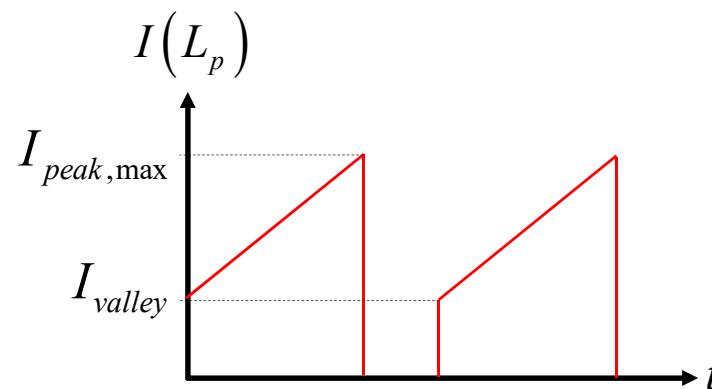
- In DCM, the valley current is zero, the stored energy is:

$$E = \frac{1}{2} L_p I_{peak,max}^2$$

➤ The peak current runaway, alone, affects the transmitted power

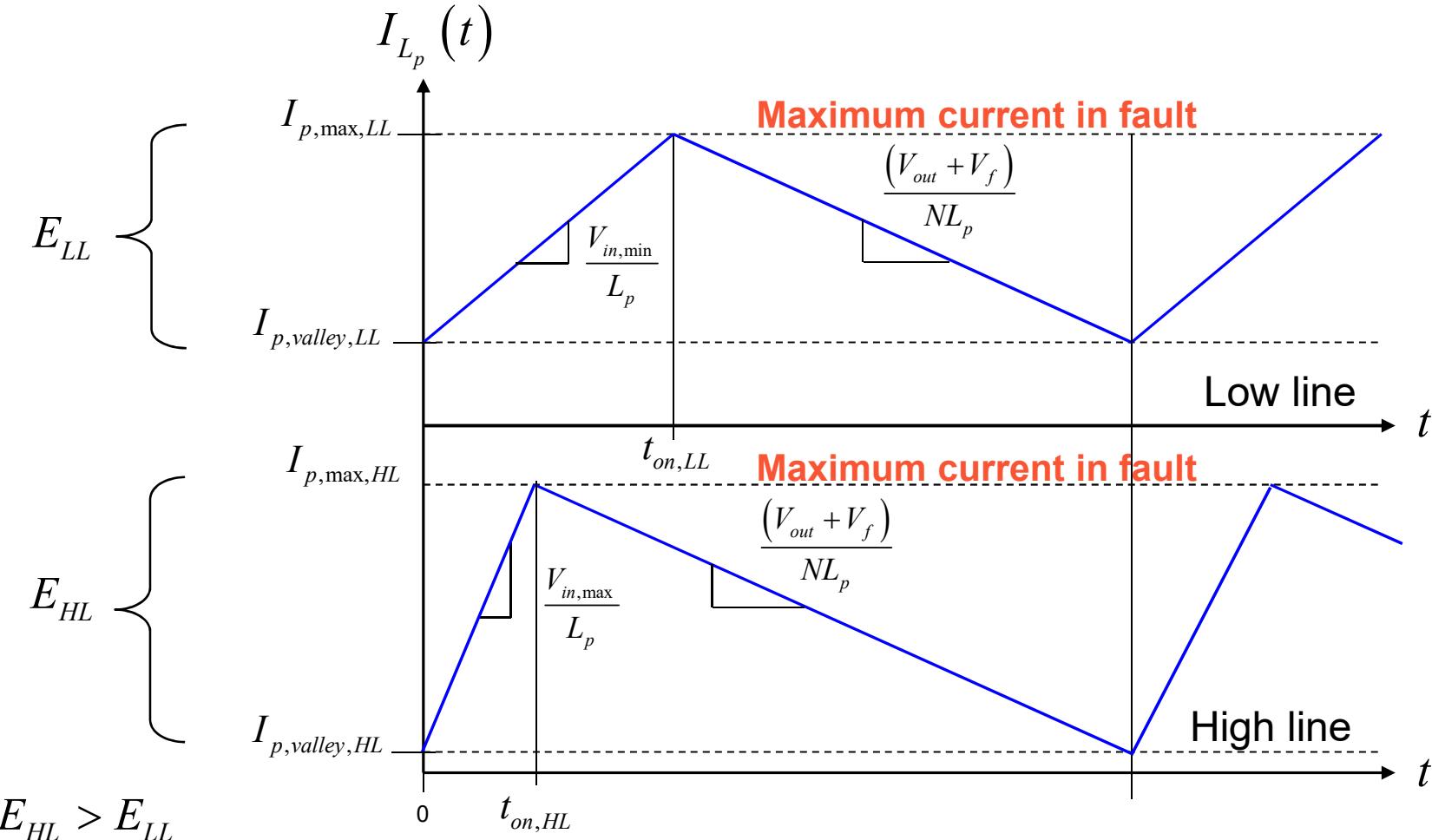
- In CCM, the valley current changes the formula:

$$E = \frac{1}{2} L_p \left(I_{peak,max}^2 - I_{valley}^2 \right)$$



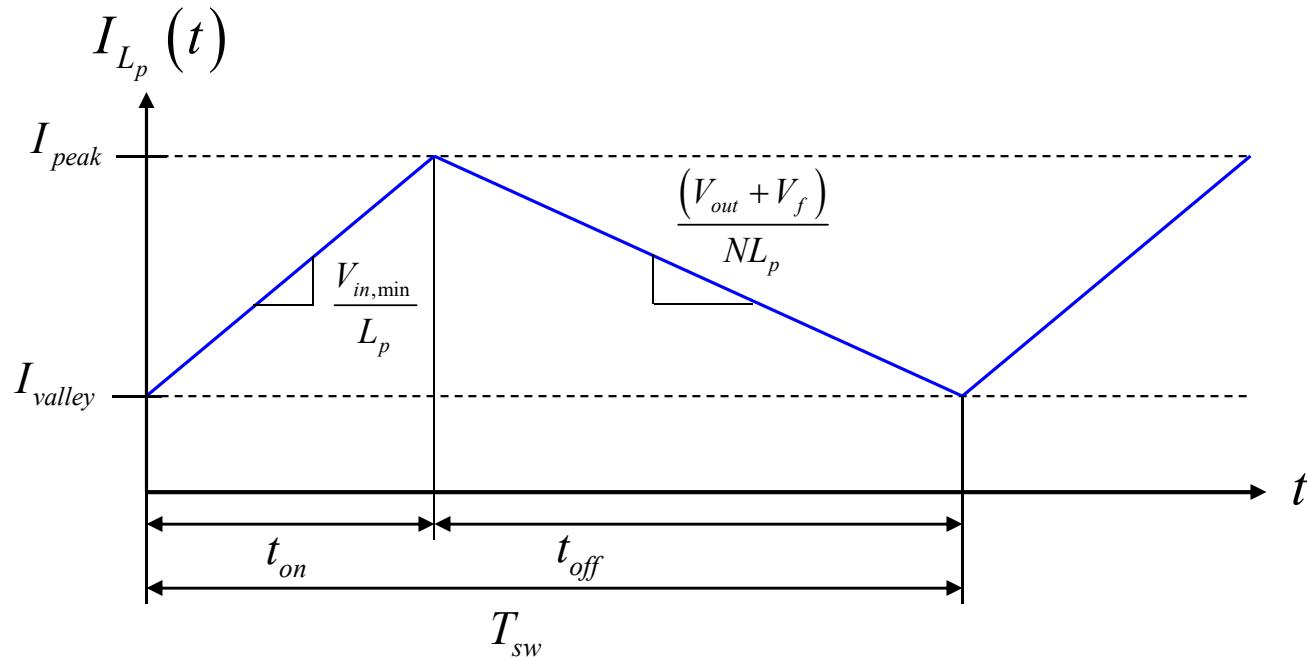
The Converter Changes its Operating Mode

- In fault mode, the converter operates in deep CCM at low line
- As the input voltage increases, the valley current decreases



Computing the Transmitted Power in CCM

- First, we write the t_{on} and t_{off} equations in CCM



$$I_{peak} = I_{valley} + \frac{V_{in}}{L_p} t_{on} \quad (1)$$

$$I_{valley} = I_{peak} - \frac{(V_{out} + V_f)}{NL_p} t_{off} \quad (2)$$

$$T_{sw} = t_{on} + t_{off} \quad (3)$$

Solving for the Valley Current

- By combining the 3 equations, we have:

$$t_{on} = \frac{L_p (I_{peak} - I_{valley})}{V_{in}} \quad t_{off} = T_{sw} - t_{on} = T_{sw} - \frac{L_p (I_{peak} - I_{valley})}{V_{in}}$$

- Replace t_{off} in (2):

$$I_{valley} = I_{peak} - \frac{(V_f + V_{out})(I_{valley} L_p - I_{peak} L_p + T_{sw} V_{in})}{L_p N V_{in}}$$

- Solve for I_{valley} :

$$I_{valley} = \boxed{I_{peak}} - \frac{T_{sw} \cancel{V_{in}} (V_f + V_{out})}{L_p (V_f + V_{out} + N \cancel{V_{in}})} \quad \Delta I_L = I_{peak} - I_{valley} \quad \Delta I_L = \frac{T_{sw} V_{in} (V_f + V_{out})}{L_p (V_f + V_{out} + N V_{in})}$$

↑ LL or HL

$I_{peak,max} = \frac{V_{sense}}{R_{sense}} + \frac{\cancel{V_{in}}}{L_p} t_{prop}$

Max fault current

Identifying the Operating Mode

□ Having the ripple on hand, we can confirm the mode:

$$t_{on} = \frac{\Delta I_L}{V_{in}} L_p \quad t_{off} = \frac{N \Delta I_L}{(V_{out} + V_f)} L_p$$

$$t_{on} + t_{off} = T_{sw} \longrightarrow \text{CCM}$$

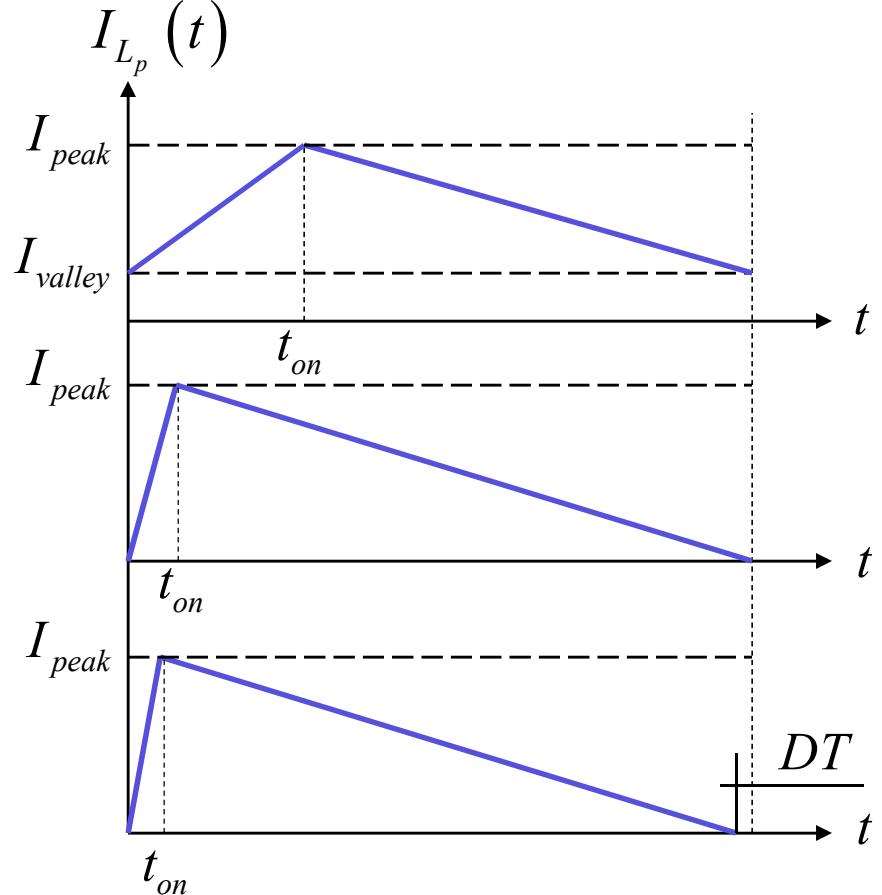
$$I_{valley} > 0$$

$$t_{on} + t_{off} = T_{sw} \longrightarrow \text{BCM}$$

$$I_{valley} = 0$$

$$t_{on} + t_{off} < T_{sw} \longrightarrow \text{DCM}$$

$$DT = T_{sw} - t_{off} - t_{on}$$

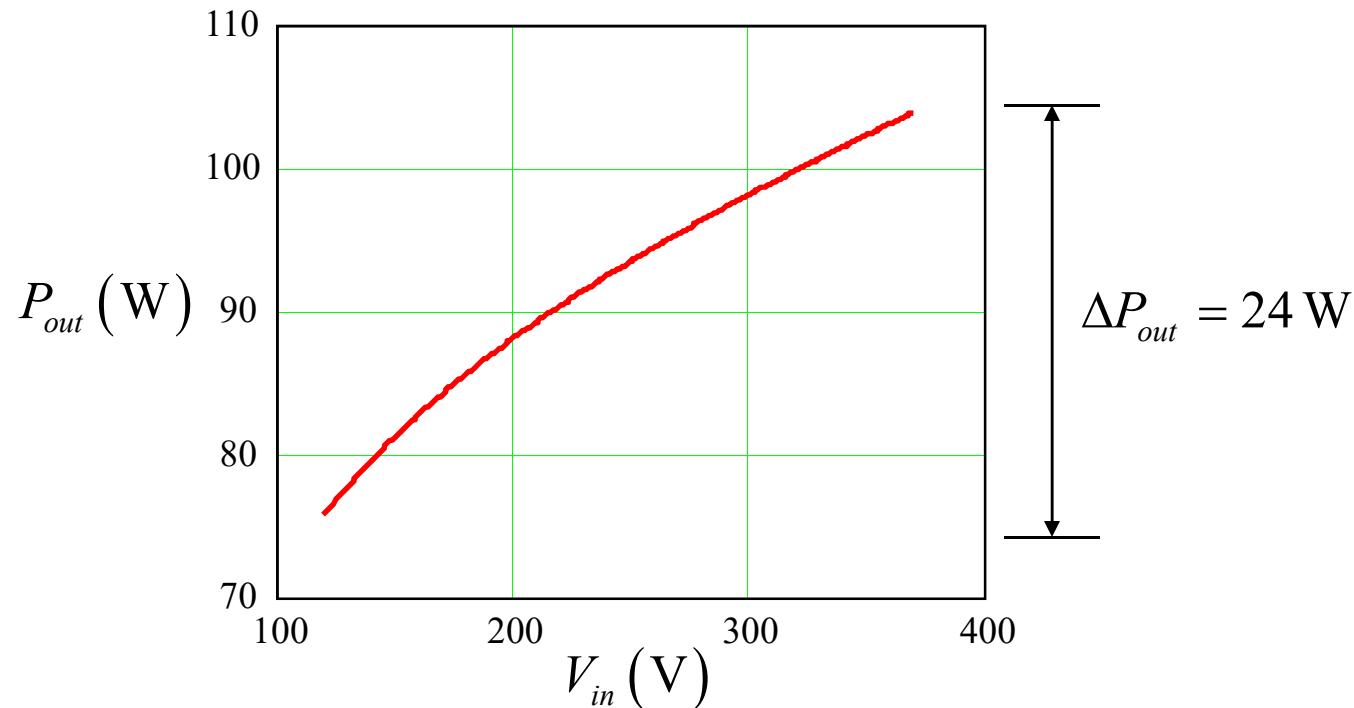


Evaluating the Power in CCM

□ $L_p = 600 \mu\text{H}$, $V_{sense} = 1 \text{ V}$, $t_{prop} = 350 \text{ ns}$, $V_{in,LL} = 120$, $V_{in,HL} = 370 \text{ V}$, $R_{sense} = 0.33 \Omega$, $F_{sw} = 65 \text{ kHz}$

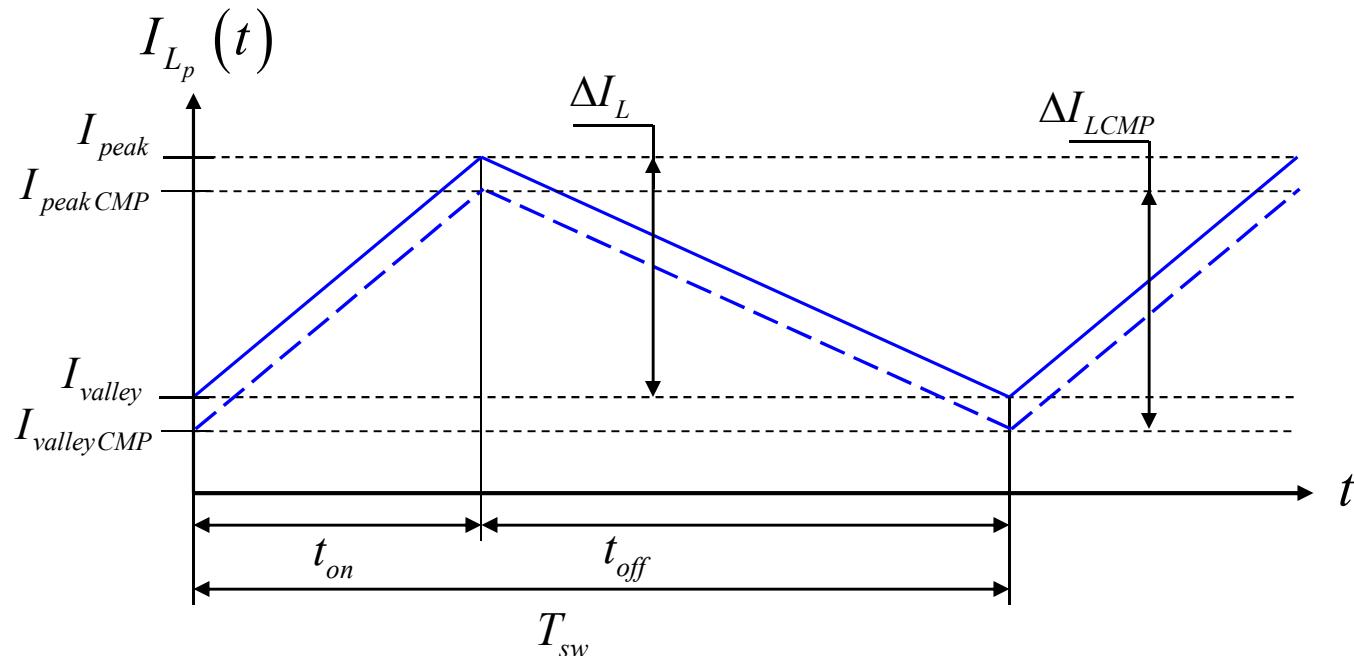
$$P_{\max,LL} = \frac{1}{2} L_p \left(I_{peak,max,LL}^2 - I_{valley,LL}^2 \right) F_{sw} \eta_{LL} \approx 76 \text{ W}$$

$$P_{\max,HL} = \frac{1}{2} L_p \left(I_{peak,max,HL}^2 - I_{valley,HL}^2 \right) F_{sw} \eta_{HL} = 104 \text{ W}$$



Reducing the Peak Current at High Line

- If we lower the peak at high line, the ripple remains the same



- We can re-write the flyback power formula to include the ripple

$$P_{\max,HL} = \frac{1}{2} L_p \left(I_{\max,HL}^2 - \underbrace{\left(I_{\max,HL} - \Delta I_{L,HL} \right)^2}_{0 \text{ in DCM}} \right) F_{sw} \eta_{HL}$$

We Want to Limit the High-Line Power

- We can force the high-line power to match that of low line

$$P_{\max,LL} = \frac{1}{2} L_p \left(I_{peak,max,HL}^2 - (I_{peak,max,HL} - \Delta I_{L,HL})^2 \right) F_{sw} \eta_{HL}$$

- From there, we can extract the compensated peak current value

$$I_{peak,max,HL} = \frac{F_{sw} L_p \eta_{HL} \Delta I_{L,HL}^2 + 2 P_{\max,LL}}{2 F_{sw} L_p \eta_{HL} \Delta I_{L,HL}}$$

- As this is the new setpoint, prop. delay contribution must be removed

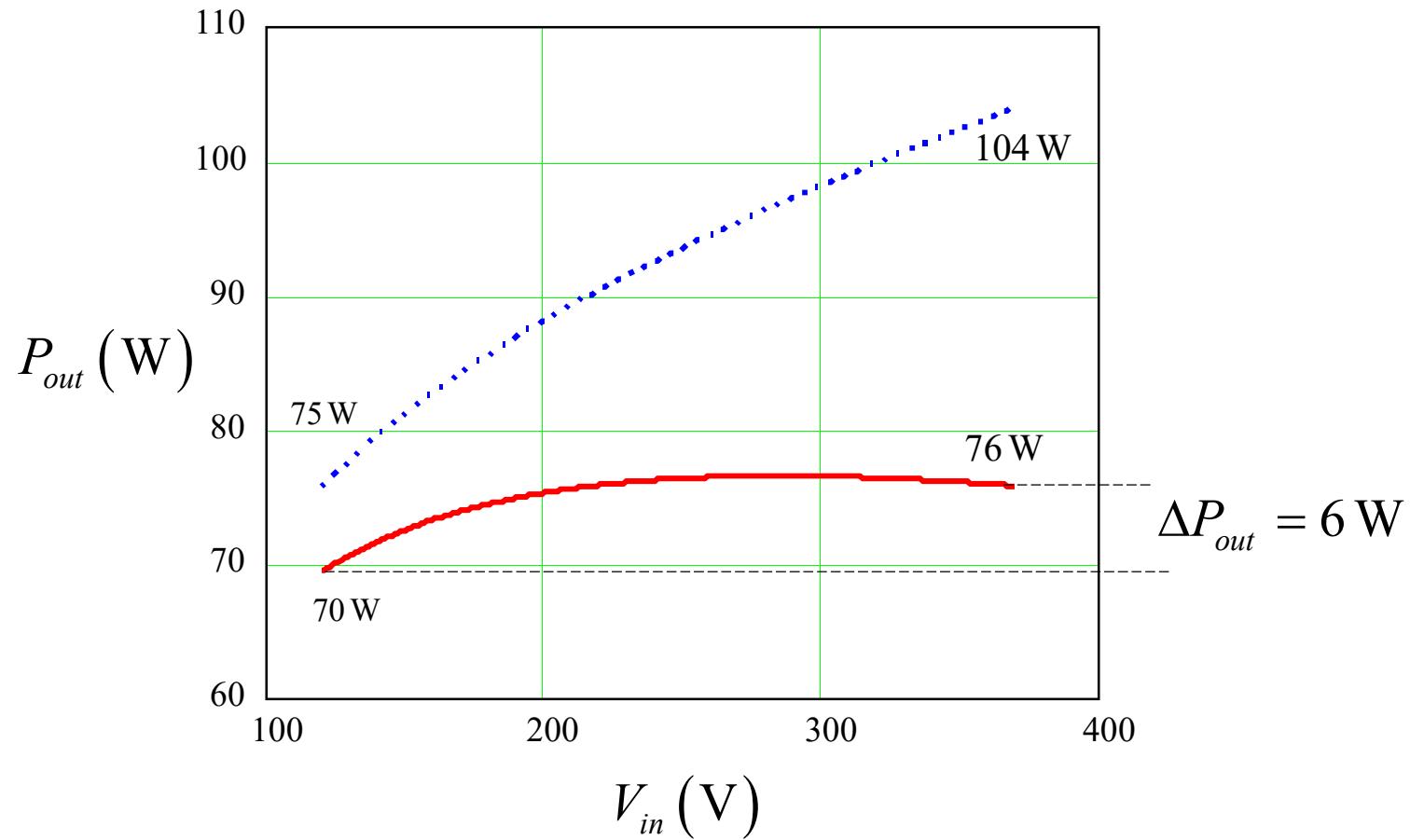
$$\Delta V = V_{sense} - \left(I_{peak,max,HL} - \frac{V_{in,HL}}{L_p} t_{prop} \right) R_{sense}$$

- After compensation, the peak current setpoint at high line becomes

$$I_{peak,max,HL} = \frac{V_{sense} - \Delta V}{R_{sense}} + \frac{V_{in,HL}}{L_p} t_{prop}$$

What is the Final Result?

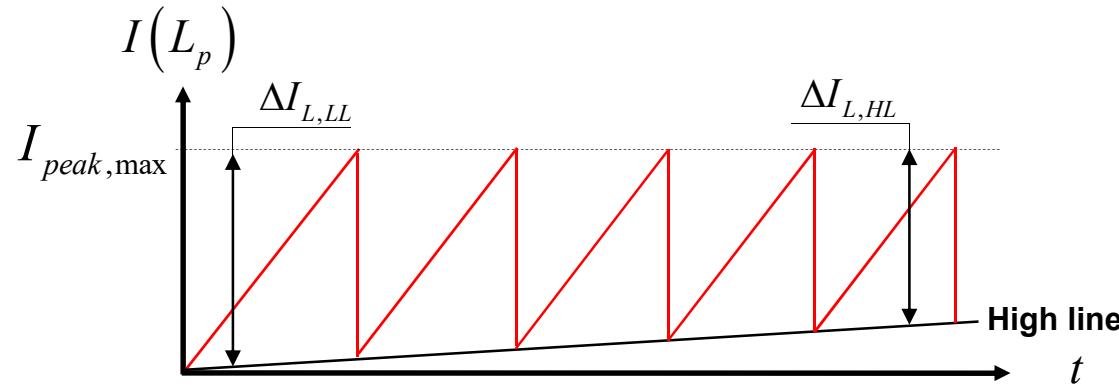
- ❑ The high line power now respects the LPS limit



What Practical Solutions?

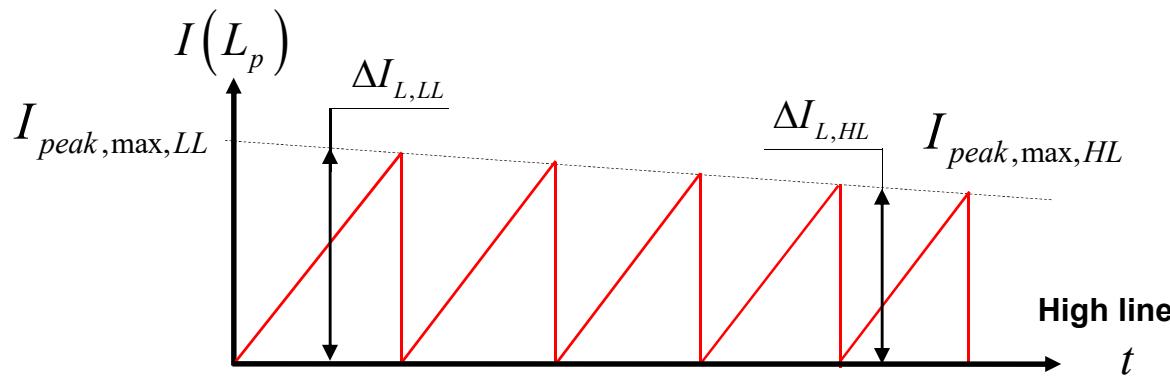
□ There are several possibilities to reduce the peak current

1. Offset the current sense signal in the CS pin:



- easy to do
- affects the no-load stand-by power
- affects light-load efficiency

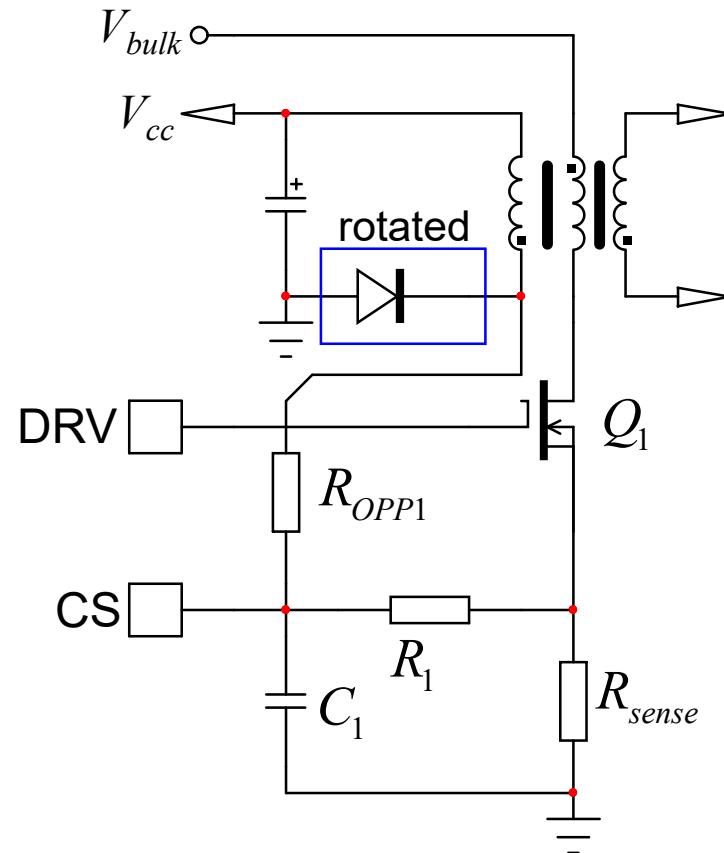
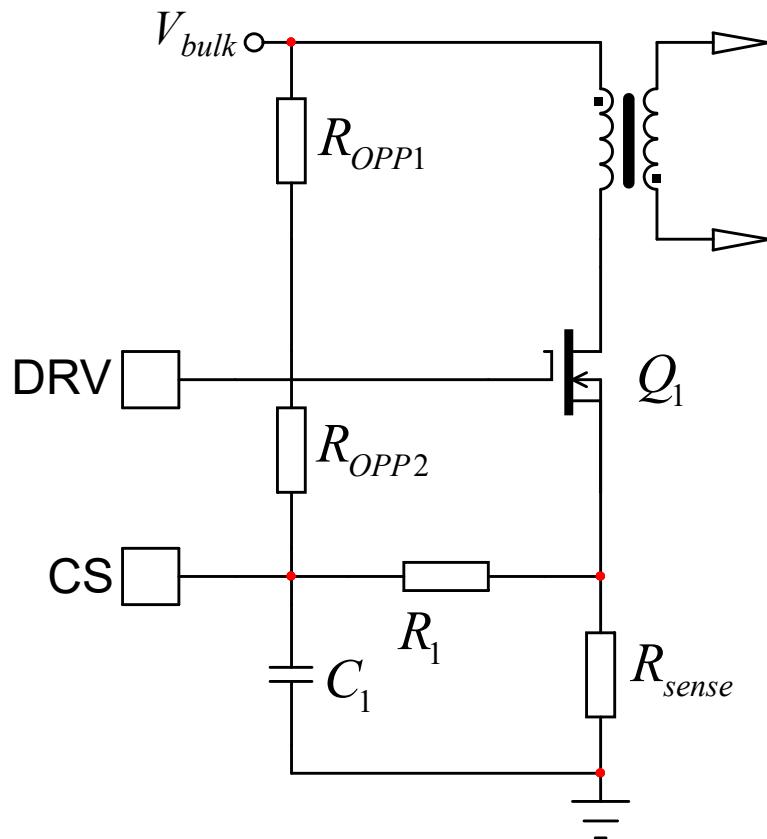
2. Reduce the peak limit as V_{in} increases



- implemented at IC level
- does not affect the no-load stand-by power
- does not affect light-load efficiency

Build an Offset on the CS Pin

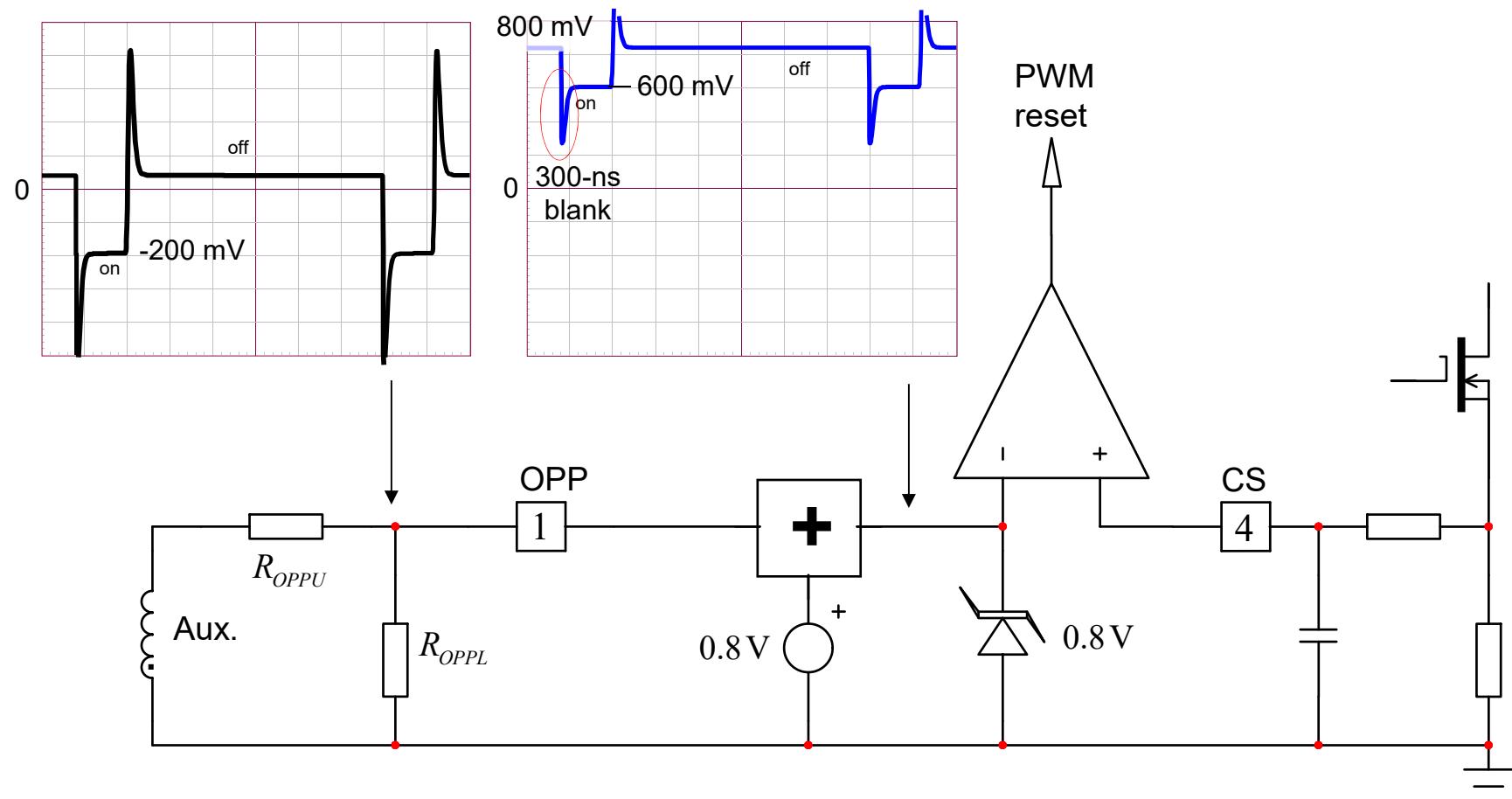
- This offset must be proportional to the input voltage



- Both options degrade light-load operation because of the offset

OPP Implementation in the NCP1250

- The NCP1250 implement a non-dissipative OPP circuitry



- The auxiliary swings to $-V_{in}$ and reduces the setpoint \rightarrow OPP

Checking the Results

- Let us check on a real 19-V adapter built with the NCP1250

$$L_p = 600 \mu\text{H}, V_{sense} = 1 \text{ V}, t_{prop} = 350 \text{ ns}, V_{in,LL} = 120, V_{in,HL} = 370 \text{ V}$$
$$R_{sense} = 0.33 \Omega, F_{sw} = 65 \text{ kHz}, V_{clamp} = 90 \text{ V}, l_l = 2.2 \mu\text{H}, N = 0.25$$



- Without any OPP compensation, we have:

$$I_{out,max,LL} = 4.1 \text{ A} \quad I_{out,max,HL} = 5.7 \text{ A}$$

- Once OPP has been implemented:

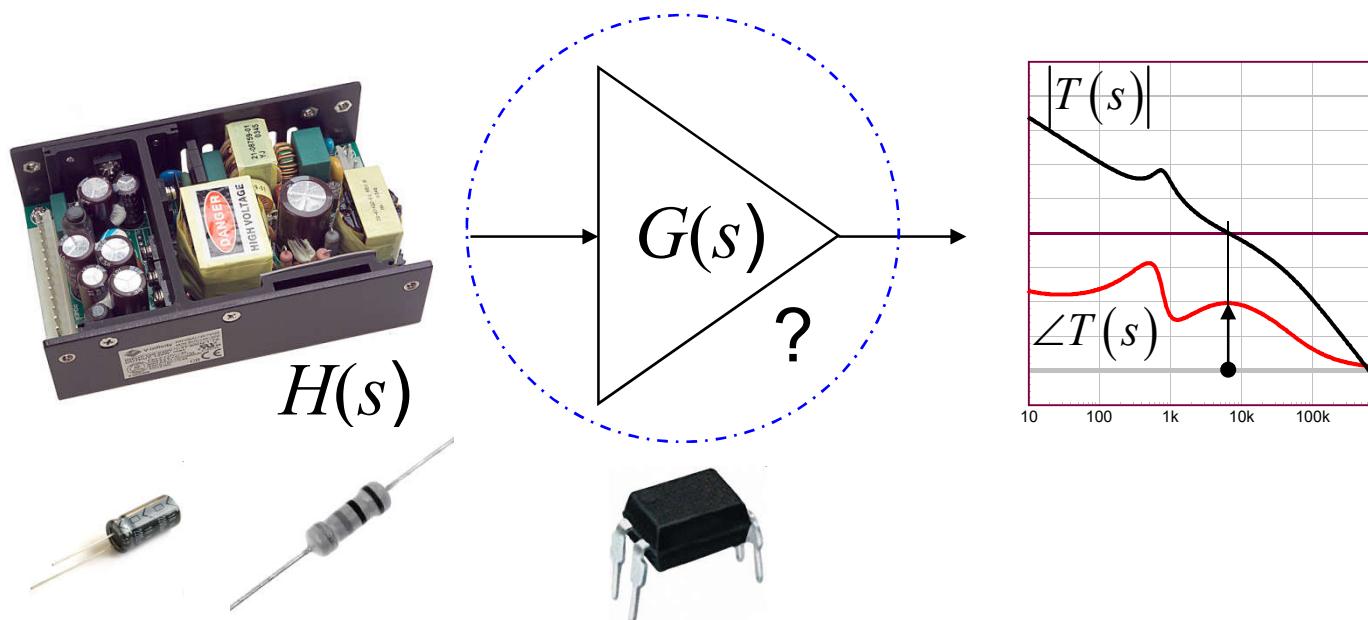
$$P_{out,LL} \approx 72 \text{ W so } I_{out,LL} = 3.8 \text{ A} \quad P_{out,HL} \approx 78 \text{ W so } I_{out,HL} = 4.1 \text{ A}$$

Course Agenda

- The Flyback Converter
- The Parasitic Elements
- How These Parasitics Affect your Design?
- Current-Mode is the Most Popular Scheme
- Fixed or Variable Frequency?
- More Power than Needed
- The Frequency Response**
- Compensating With the TL431

Small-Signal Analysis

- ❑ Loop instability is a common issue in production
- ❑ Due to time pressure, designers often use trial and error
 - no indication on design margins
 - offenders are ignored, robustness is at stake



- ❖ Understand and counteract their variations when building $G(s)$

There are Two Options

- Analytical analysis of the power stage:
 - ✓ best to see where the offenders are hidden (ESR, opto pole etc.)
 - ✓ equations are complex but litterature abounds
 - ❖ transfer function are for DCM or CCM
 - ❖ difficult to predict transient response

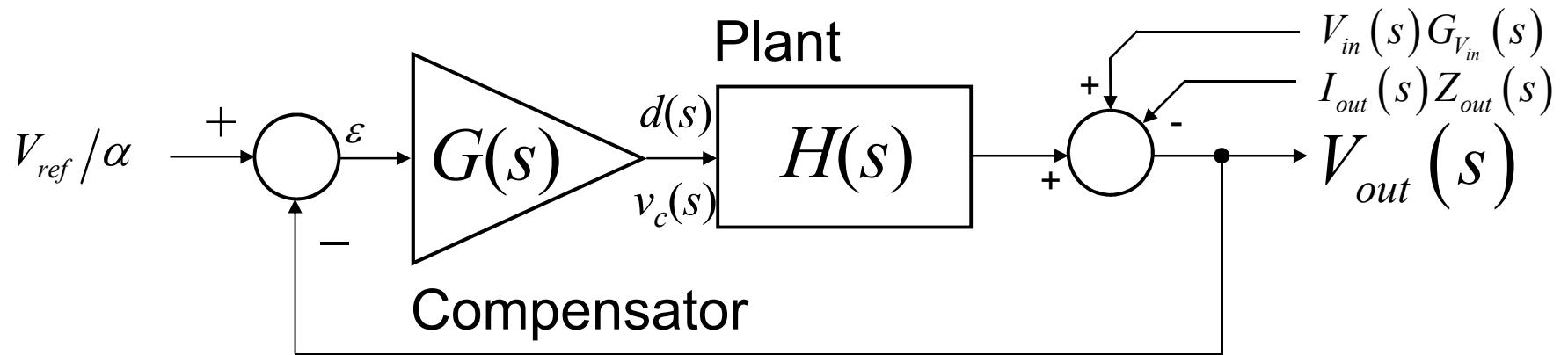
- SPICE models:
 - ✓ easy-to-implement averaged models
 - ✓ can work in ac or transient mode
 - ✓ easily transition between CCM and DCM
 - ❖ do not explicitly disclose the position of poles and zeros



A measurement on the bench is mandatory, whatever you choose!

Analytical Analysis

- You must first characterize the "plant" transfer function
 - what are your power stage ac characteristics?



$$H(s) = \frac{V_{out}(s)}{v_c(s)}$$

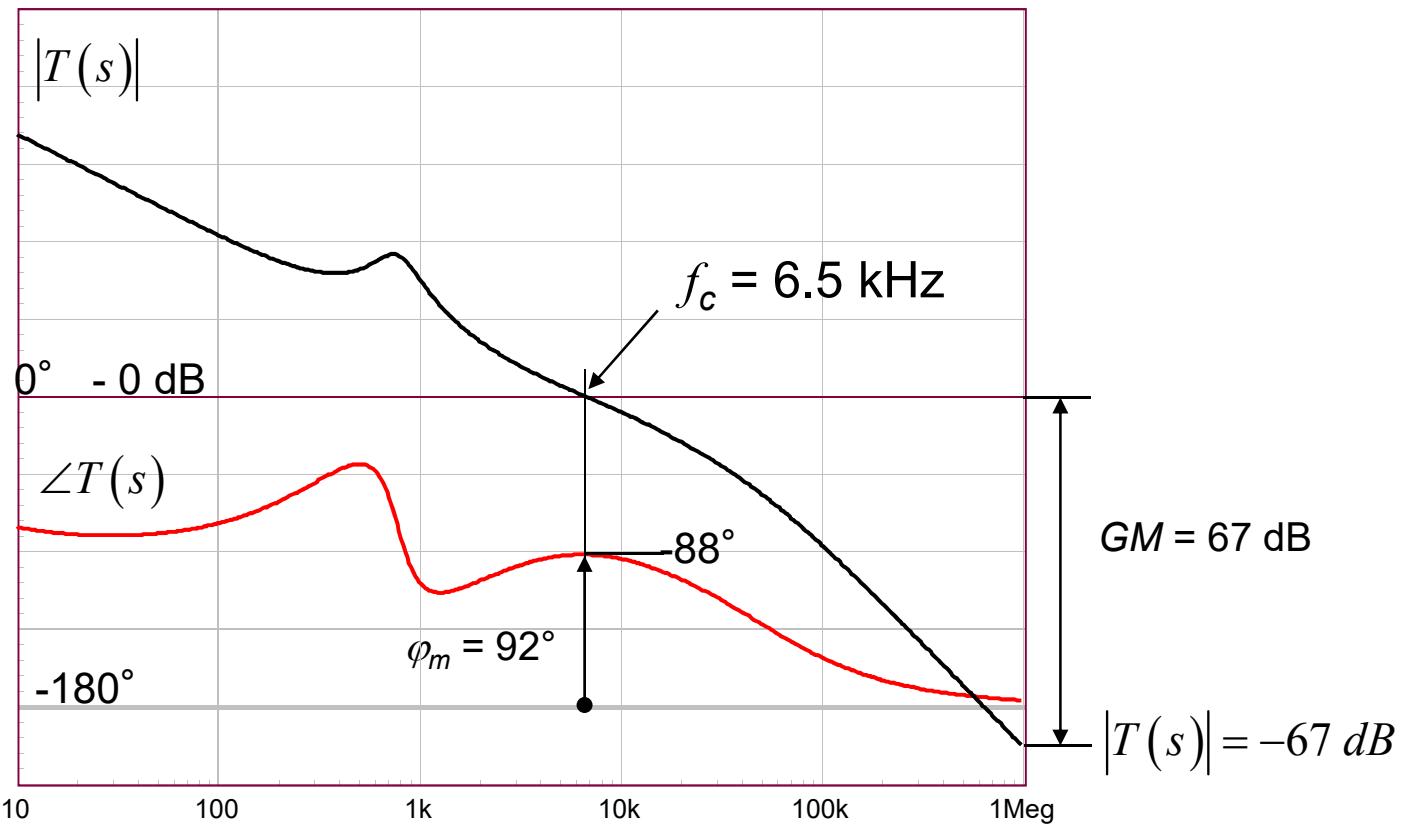
Current-mode control

$$H(s) = \frac{V_{out}(s)}{d(s)}$$

Voltage-mode control

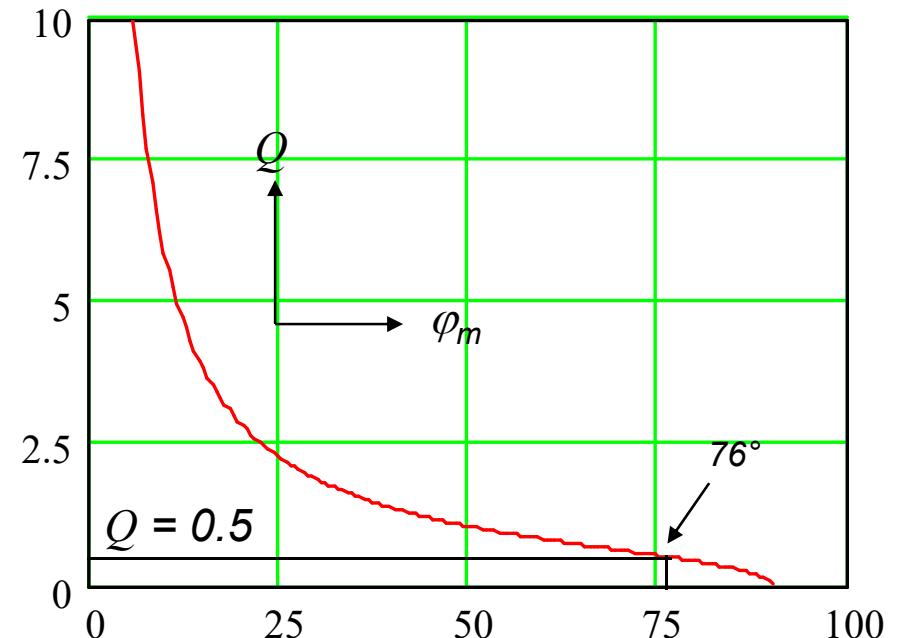
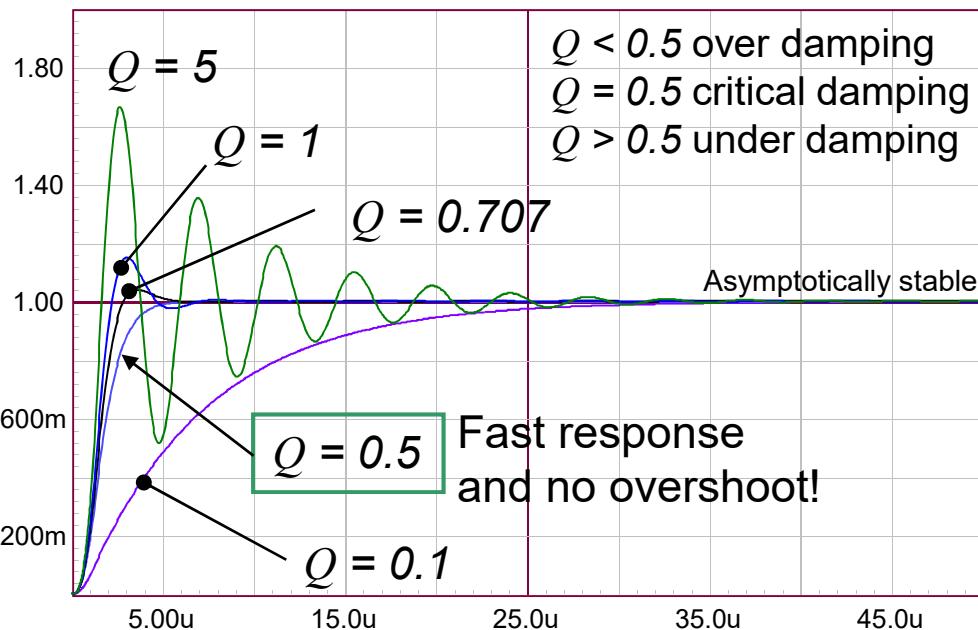
How do we Stabilize a Converter?

- We need a high gain at dc for a low static error
- We want a sufficiently high crossover frequency for response speed
- Shape the compensator $G(s)$ to build phase and gain margins!



How much phase margin to chose?

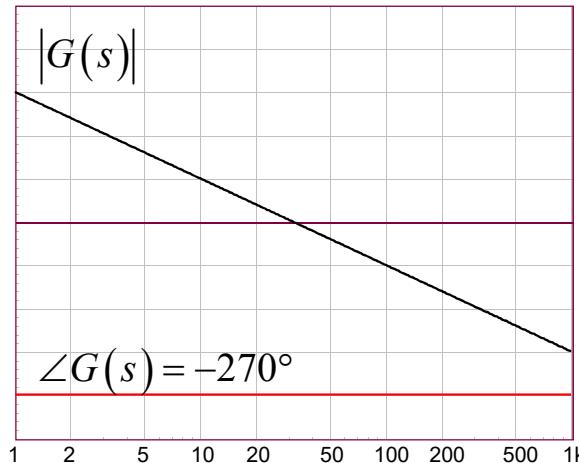
- ❑ a Q factor of 0.5 (critical response) implies a φ_m of 76°
- ❑ a $45^\circ \varphi_m$ corresponds to a Q of 1.2: oscillatory response!



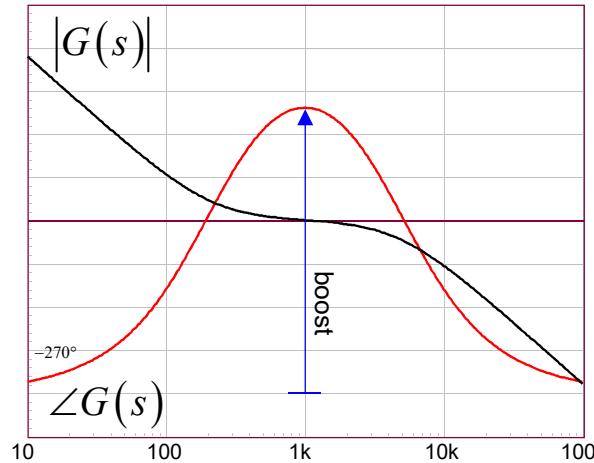
- ❑ phase margin depends on the needed response: fast, no overshoot...
- ❑ good practice is to shoot for 60° and make sure φ_m always $> 45^\circ$

What Compensator Types do we Need?

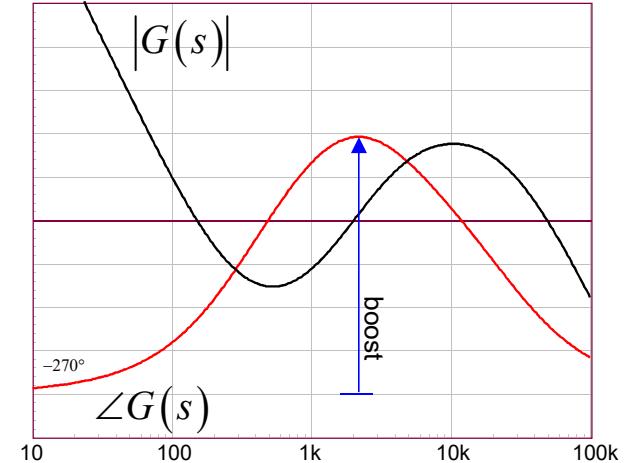
- There are basically 3 compensator types:
 - type 1, 1 pole at the origin, no phase boost
 - type 2, 1 pole at the origin, 1 zero, 1 pole. Phase boost up to 90°
 - type 3, 1 pole at the origin, 1 zero pair, 1 pole pair. Boost up to 180°



Type 1



Type 2



Type 3

Fixed-Frequency Current-Mode

- ❑ First, check the operating mode, CCM or DCM?

$$L_{p,crit} = \frac{R_{load}}{2F_{sw}N^2} \left(\frac{V_{in}}{V_{in} + \frac{V_{out}}{N}} \right)^2 \quad L_p > L_{p,crit} ? \text{ Yes, CCM else DCM}$$

- ❑ Assume CCM, compute the duty-ratio: $D = \frac{V_{out}}{V_{out} + NV_{in}}$
- ❑ Compute M and τ_L : $M = \frac{V_{out}}{NV_{in}} \quad \tau_L = \frac{2L_p N^2}{R_{load} T_{sw}}$
- ❑ Evaluate the dc gain and poles/zeros positions:

$$G_0 = \frac{R_{load}}{R_{sense} G_{FB} N} \frac{1}{\frac{(1-D)^2}{\tau_L} + 2M + 1}$$

Fixed-Frequency Current-Mode

- Compute the poles/zeros positions:

$$f_{z_1} = \frac{1}{2\pi R_{ESR} C_{out}}$$

$$f_{z_2} = \frac{(1-D)^2 R_{load}}{2\pi D L_p N^2}$$

$$f_{p_1} = \frac{\frac{(1-D)^3}{\tau_L} + 1 + D}{2\pi R_{load} C_{out}}$$

- Check the quality coefficient at $F_{sw}/2$

$$S_n = \frac{V_{in}}{L_p} R_{sense}$$

$$S_e = (M_c - 1) S_n$$

↓
1 = no compensation

$$Q_p = \frac{1}{\pi (M_c (1-D) - 0.5)}$$

- Apply to formula to plot the ac response:

$$H(s) \approx G_0 \frac{\left(1 + \frac{s}{\omega_{z1}}\right) \left(1 - \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)} \frac{1}{1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2}}$$

3rd order →

$$M_c = 1 + \frac{S_e}{S_n} \quad \omega_n = \frac{\pi}{T_{sw}}$$

Fixed-Frequency Current-Mode

- Extract the magnitude and the argument definitions

$$|H(f)| = 20 \log_{10} \left[G_0 \frac{\sqrt{1 + \left(\frac{f}{f_{z1}}\right)^2} \sqrt{1 + \left(\frac{f}{f_{z2}}\right)^2}}{\sqrt{1 + \left(\frac{f}{f_{p1}}\right)^2}} \frac{1}{\sqrt{\left(1 - \left(\frac{f}{f_n}\right)^2\right)^2 + \left(\frac{f}{f_n Q_p}\right)^2}} \right]$$

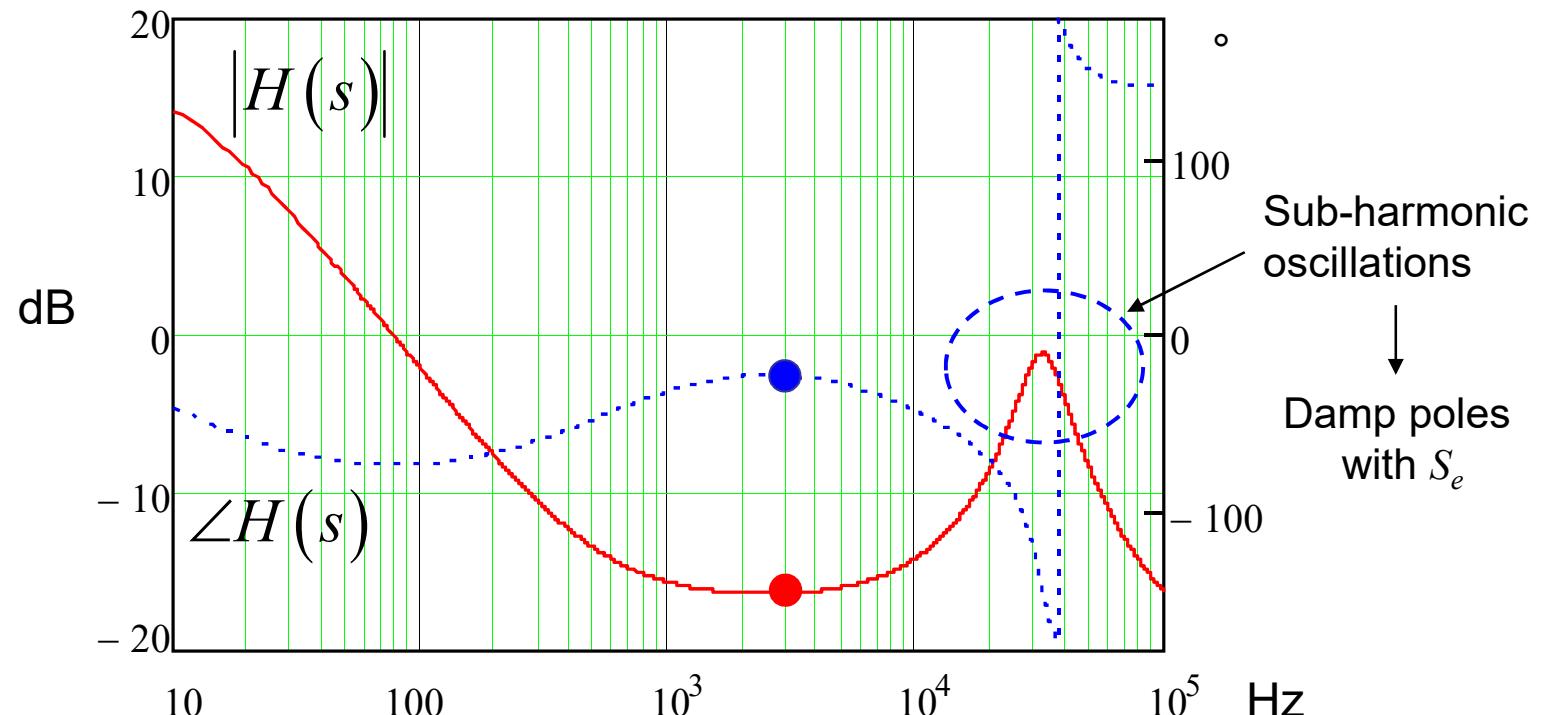
$$\arg H(f) = \tan^{-1} \left(\frac{f}{f_{z1}} \right) - \tan^{-1} \left(\frac{f}{f_{z2}} \right) - \tan^{-1} \left(\frac{f}{f_{p1}} \right) - \tan^{-1} \left(\frac{f}{f_n Q_p} \frac{1}{1 - \left(\frac{f}{f_n}\right)^2} \right)$$

↑
RHPZ

- Plot them with Mathcad® for instance.

Fixed-Frequency Current-Mode

- Extract the information at the selected crossover frequency



$$|H(3 \text{ kHz})| = -16.3 \text{ dB}$$

$$\arg H(3 \text{ kHz}) = -23^\circ$$

Fixed-Frequency Current-Mode

- The compensation strategy is the following:
 - compensate the gain loss at f_c so that: $|G(3\text{kHz})| = +16.3\text{ dB}$
 - evaluate the boost in phase at f_c to get phase 70° margin:

$$\text{Boost} = \text{PM} - \arg H(f_c) - 90 = 3.15^\circ$$

→ Boost = 0 select type 1 – origin pole
→ Boost < 90° select type 2 – origin pole, 1 pole, 1 zero

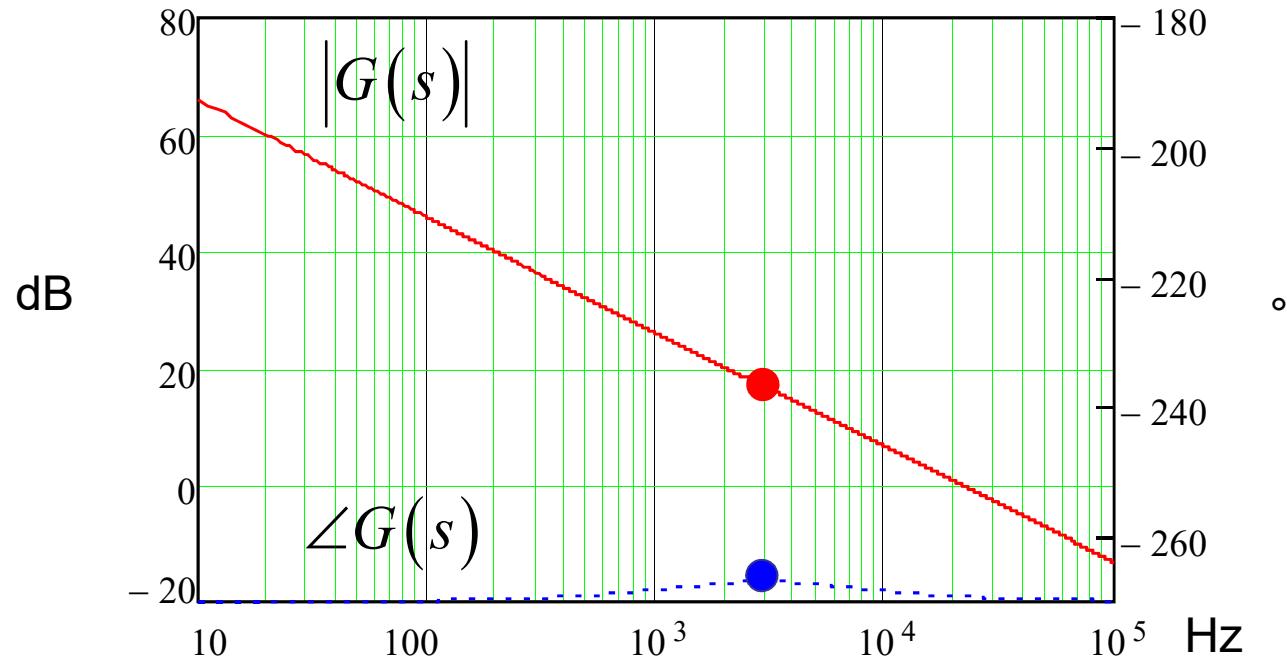
- k-factor can be used to place the pole and the zero

$$k = \tan\left(\frac{\text{boost}}{2} + 45\right) \approx 1 \longrightarrow \text{poles and zeros are coincident}$$

$$f_{pk1} = kf_c = 1 \times 3k = 3 \text{ kHz} \qquad f_{zk1} = \frac{f_c}{k} = \frac{3k}{1} = 3 \text{ kHz}$$

Fixed-Frequency Current-Mode

- Plot the compensator transfer function

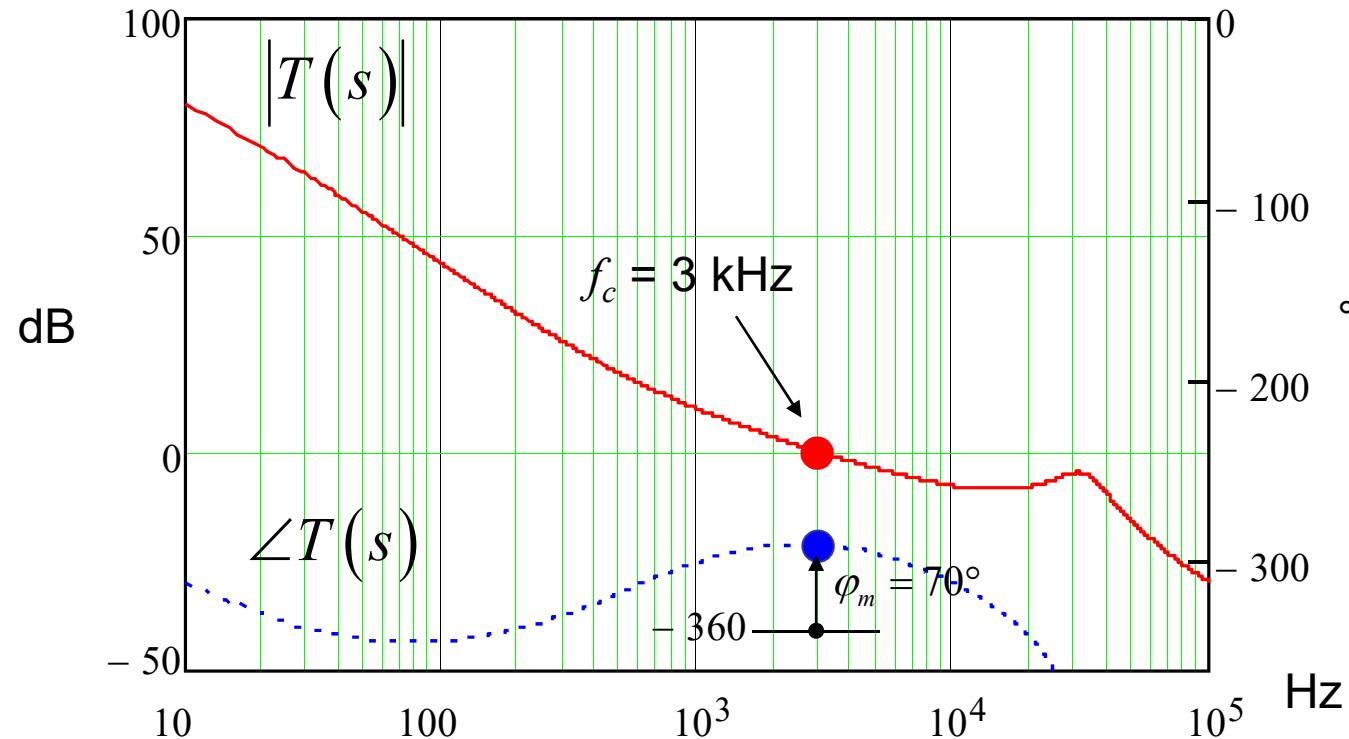


$$|G(f)| = 20 \log_{10} \left[G \frac{\sqrt{1 + \left(\frac{f}{f_{zk1}} \right)^2}}{\frac{f}{f_{pk0}} \sqrt{1 + \left(\frac{f}{f_{pk1}} \right)^2}} \right]$$

$$boost = \left(\tan^{-1} \left(\frac{f}{f_{zk1}} \right) - \tan^{-1} \left(\frac{f}{f_{pk1}} \right) \right) \frac{180}{\pi}$$

Fixed-Frequency Current-Mode

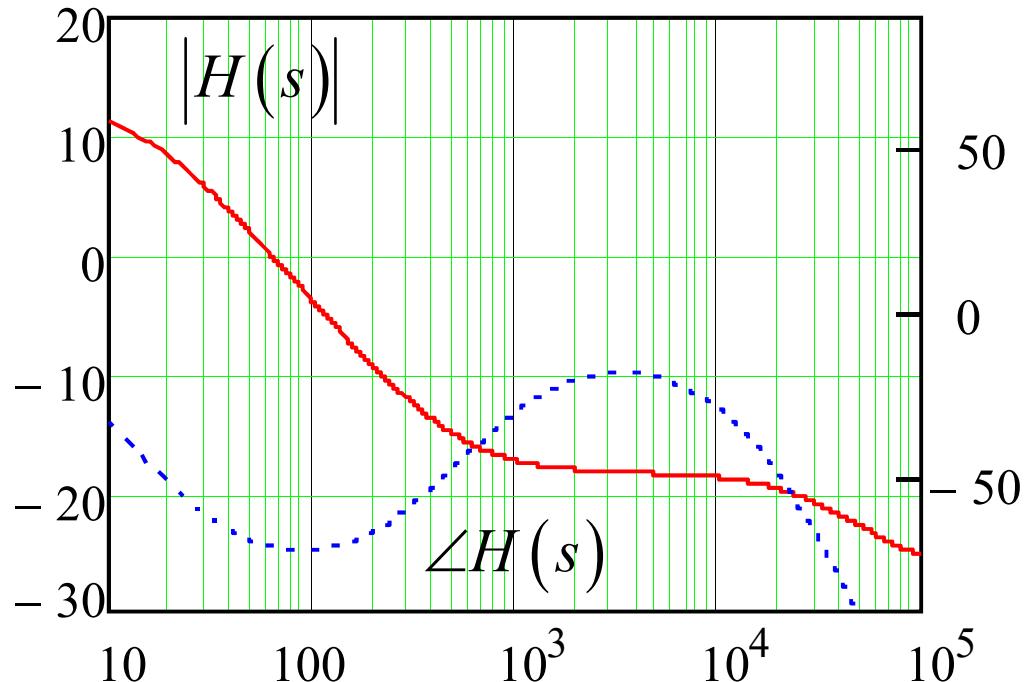
- Plot the loop gain transfer function and check the margins



- Sweep ESR, C_{out} , R_{load} and verify the results

Fixed-Frequency Current-Mode

- ❑ In case the converter transitions to DCM, update the equation!

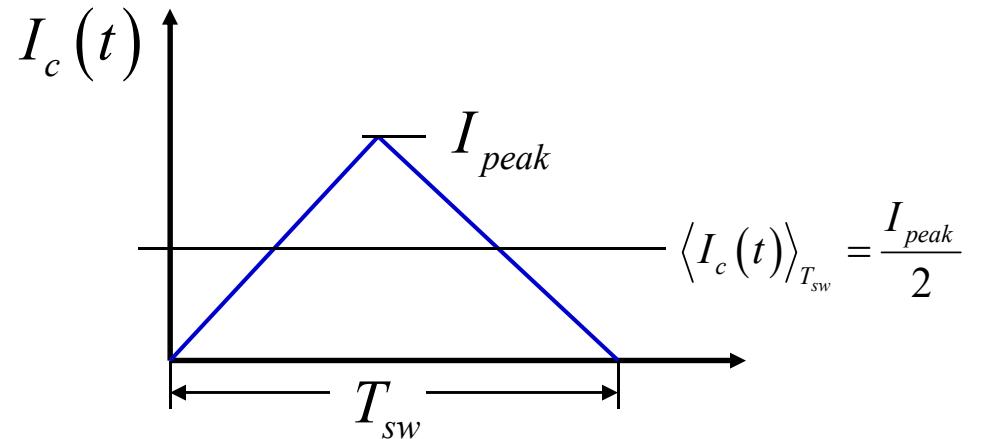
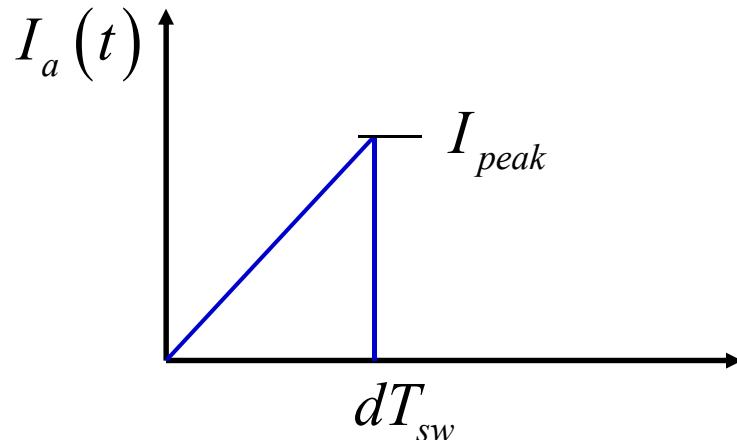


$$H(s) = G_0 \frac{\left(1 + \frac{s}{\omega_{z_1}}\right)\left(1 - \frac{s}{\omega_{z_2}}\right)}{\left(1 + \frac{s}{\omega_{p_1}}\right)\left(1 + \frac{s}{\omega_{p_2}}\right)}$$

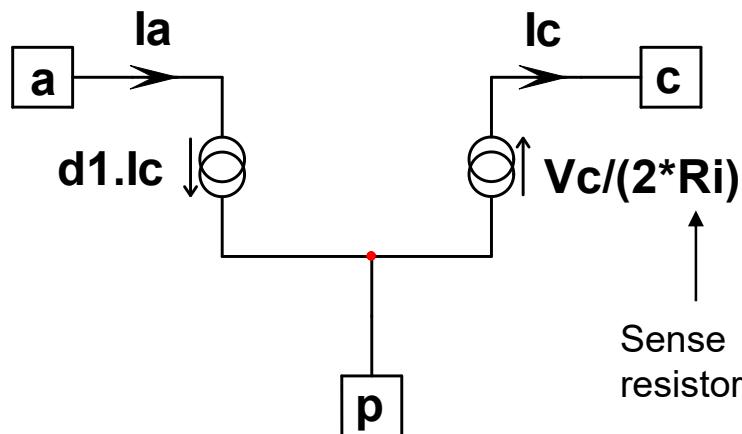
- Yes, analytical analysis is long and tedious.
- But, it teaches where the threats are and how to deal with!

Variable-Frequency Current-Mode

- Observing the waveforms helps us to derive an average model



- It gives birth to a large-signal model



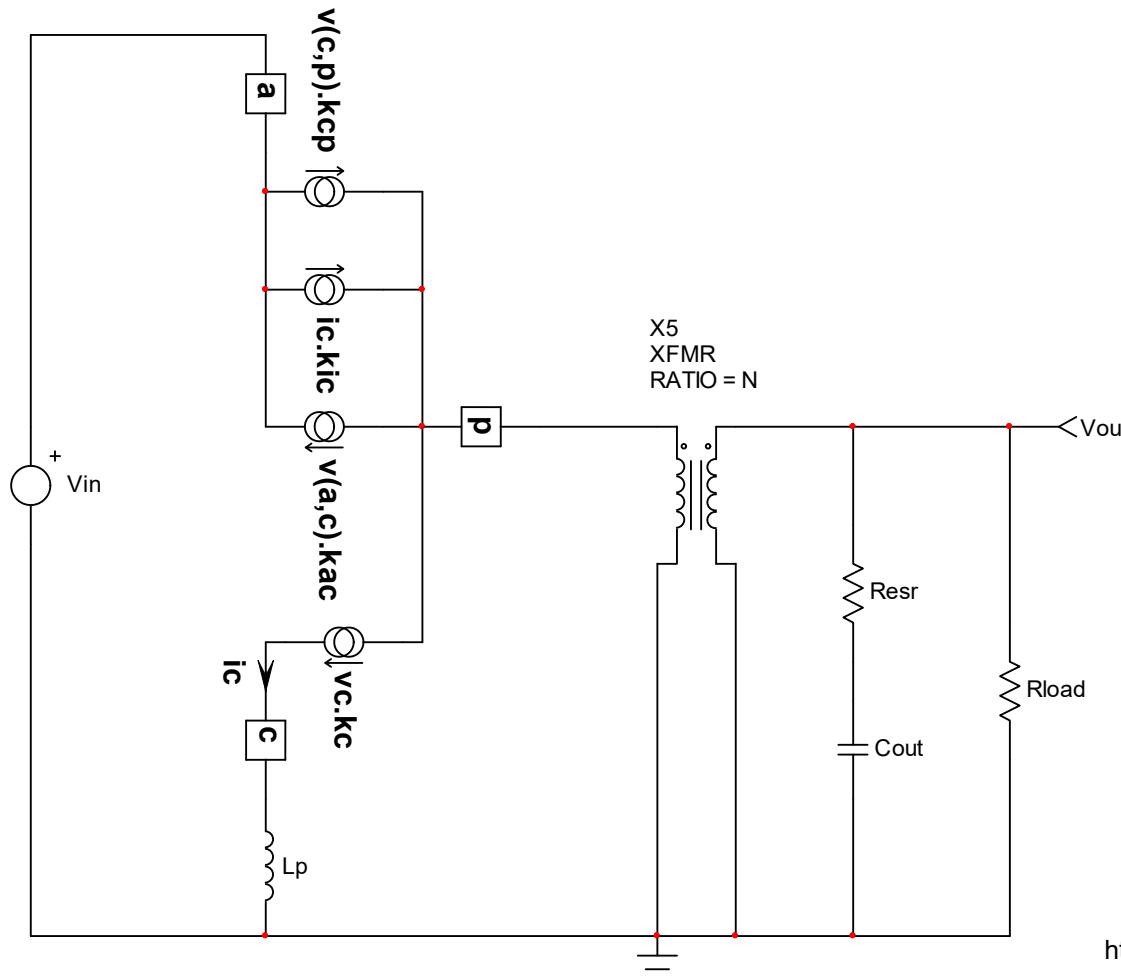
$$V_c = \frac{2R_i P_{out} (V_{out} + N V_{in})}{V_{in} V_{out}}$$

$$T_{sw} = \frac{V_c L_p}{R_i} \left(\frac{1}{V_{in}} + \frac{N}{V_{out}} \right)$$

$$d_1 = \frac{2P_{out} R_i}{V_c V_{in}}$$

Variable-Frequency Current-Mode

- Linearization is needed to get a small-signal model
- Implement this small-signal model in a flyback configuration



<http://cbasso.pagesperso-orange.fr/Spice.htm>

Variable-Frequency Current-Mode

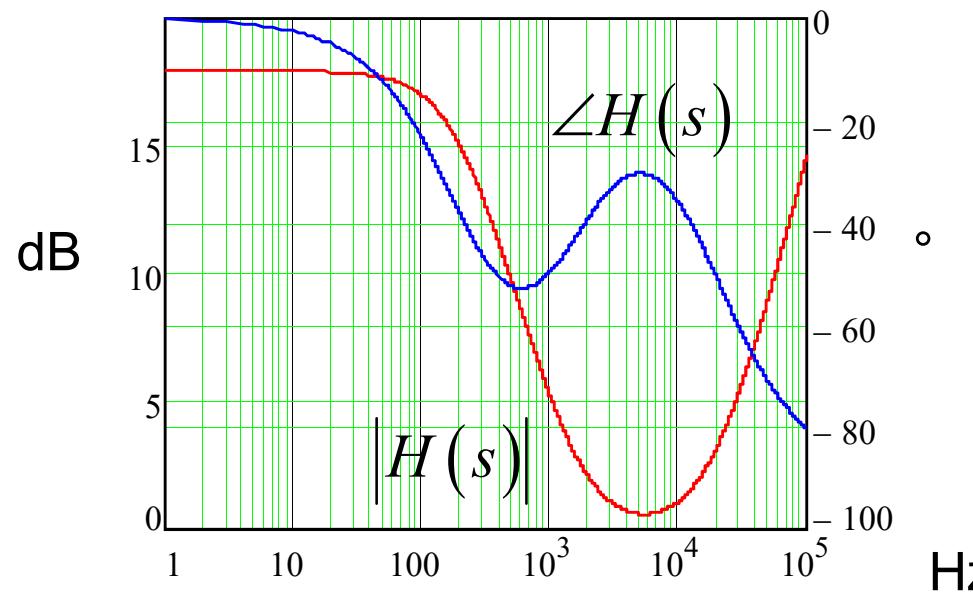
- Derive the transfer function and isolate poles and zeros

$$\frac{\hat{v}_{out}(s)}{\hat{v}_c(s)} = G_0 \frac{\left(1 + \frac{s}{s_{z1}}\right) \left(1 - \frac{s}{s_{z2}}\right)}{\left(1 + \frac{s}{s_{p1}}\right)}$$

1st order \longrightarrow

$$G_0 = \frac{R_{load} Div}{2NR_i \left(\frac{2V_{out}}{NV_{in}} + 1 \right)}$$

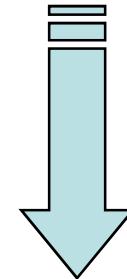
- Then plot the function



$$f_{p_1} = \frac{1}{2\pi R_{load} C_{out}} \frac{2M+1}{M+1}$$

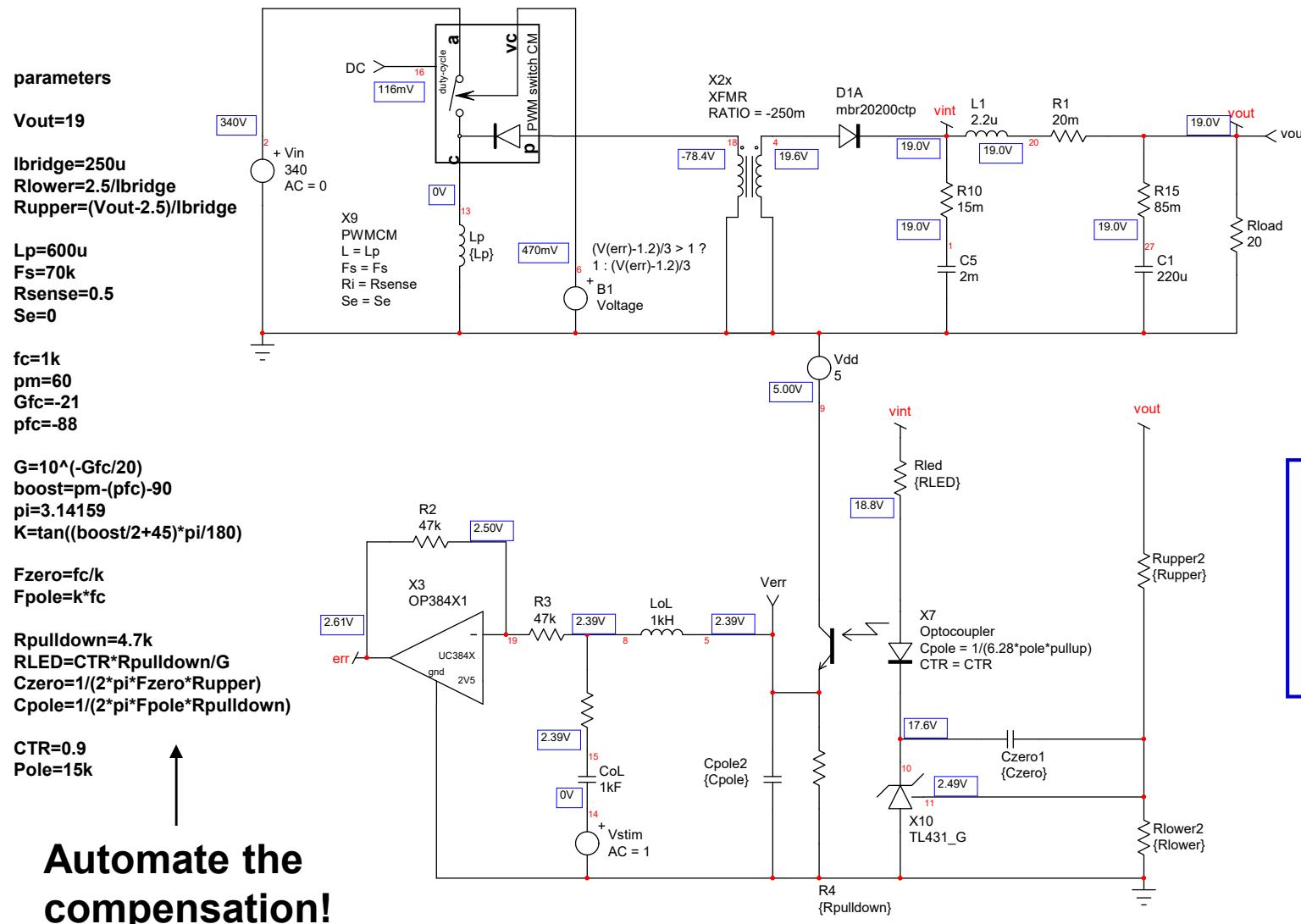
$$f_{z_1} = \frac{1}{2\pi R_{ESR} C_{out}}$$

$$f_{z_2} = \frac{R_{load}}{2\pi N^2 L_p} \frac{1}{M(1+M)}$$



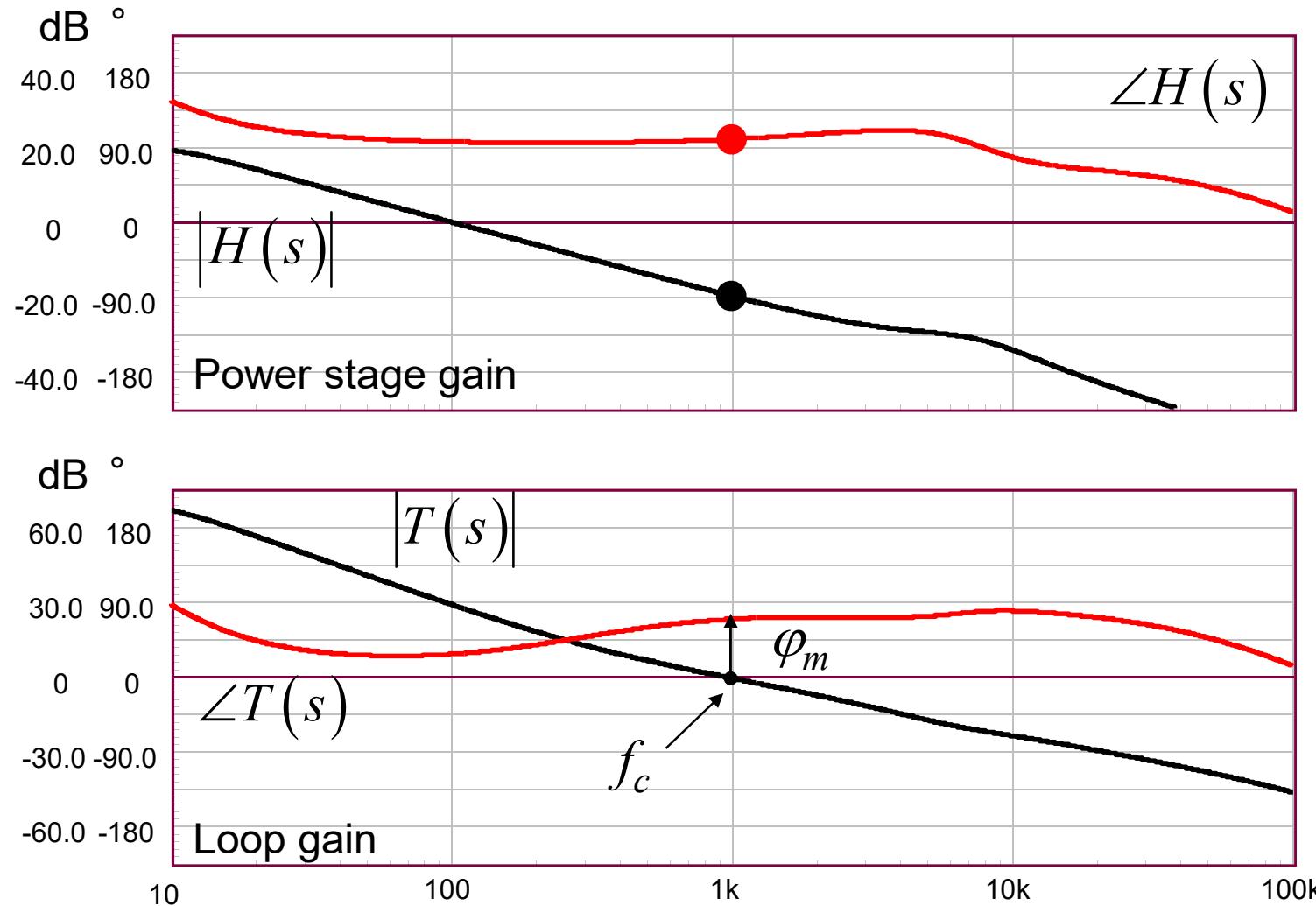
Tailor $G(s)$ to get
the desired f_c

Use a SPICE Model to Stabilize the Converter



Cannot be beaten for simplicity and speed!

Unveil the Transfer Function in a Second

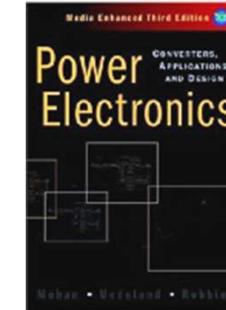
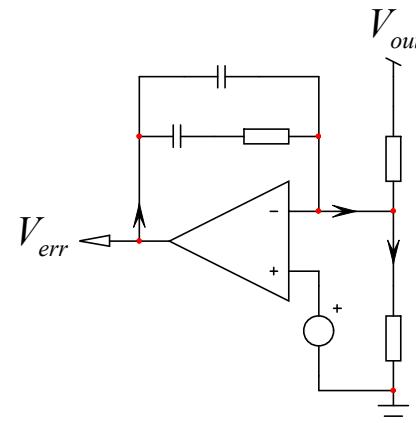
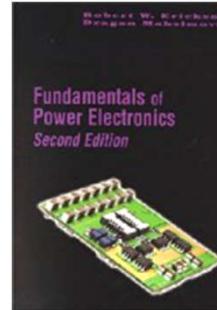


Course Agenda

- The Flyback Converter
- The Parasitic Elements
- How These Parasitics Affect your Design?
- Current-Mode is the Most Popular Scheme
- Fixed or Variable Frequency?
- More Power than Needed
- The Frequency Response
- **Compensating With the TL431**

How is regulation performed?

- Text books only describe op amps in compensators...



- The market reality is different: the TL431 rules!

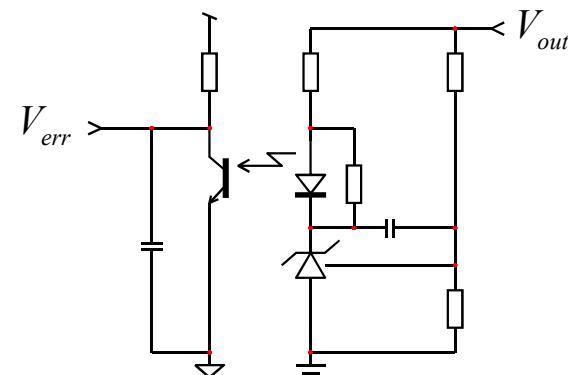
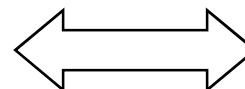
I'm the law!



TL431

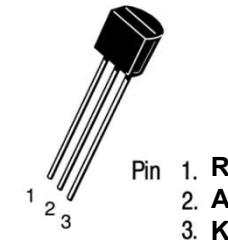
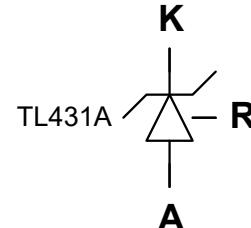
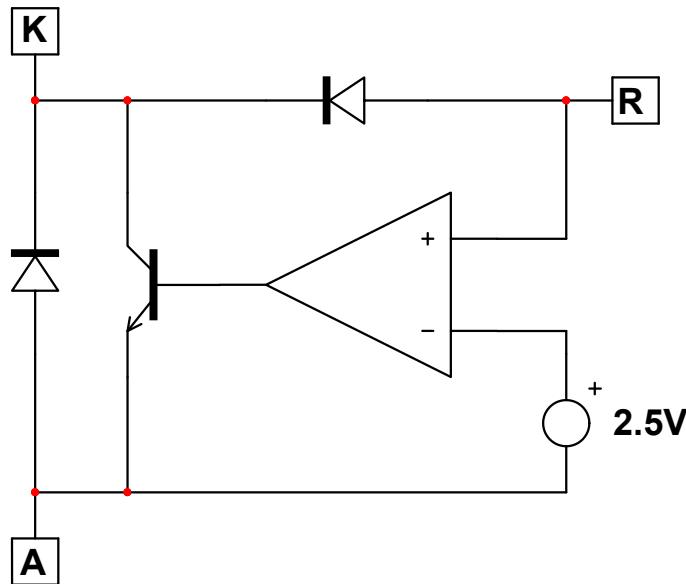


optocoupler



The TL431 Programmable Zener

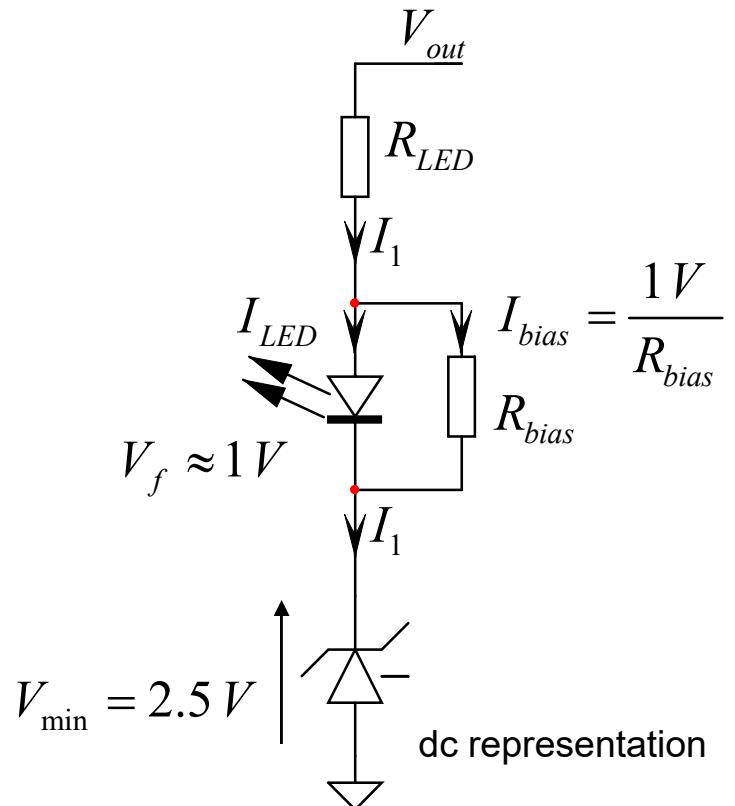
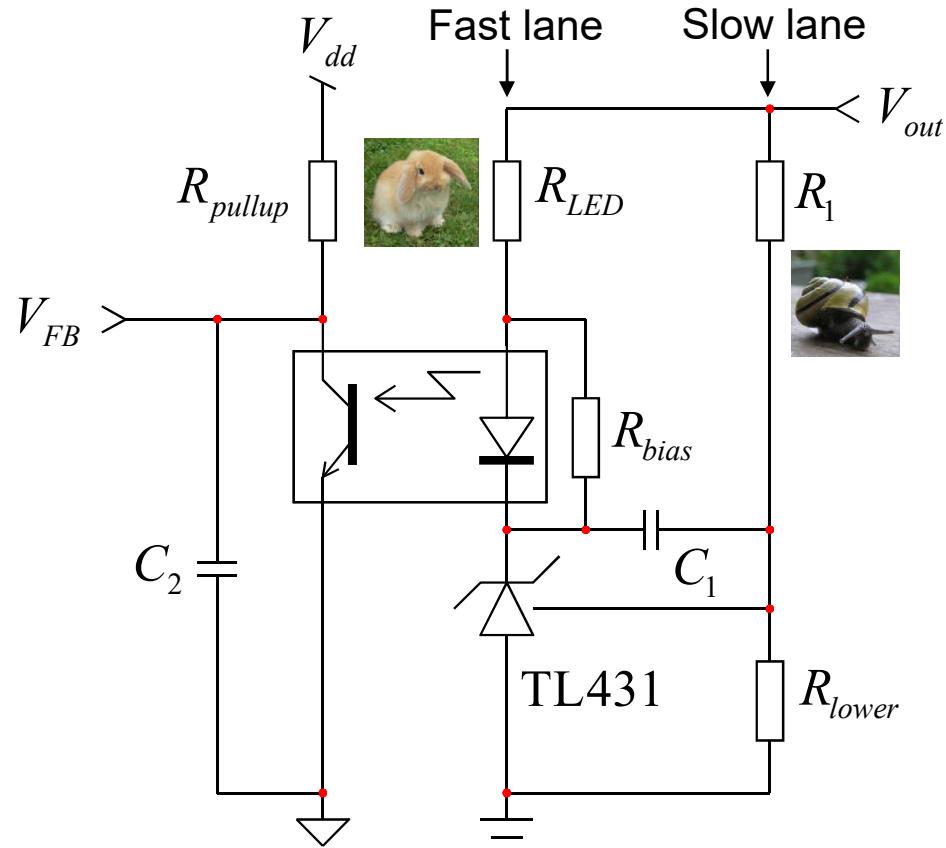
- The TL431 is the most popular choice in nowadays designs
- It associates an open-collector op amp and a reference voltage
- The internal circuitry is self-supplied from the cathode current
- When the R node exceeds 2.5 V, it sinks current from its cathode



- The TL431 is a shunt regulator

A Rabbit and a (French) Snail...

- The TL431 lends itself very well to optocoupler control



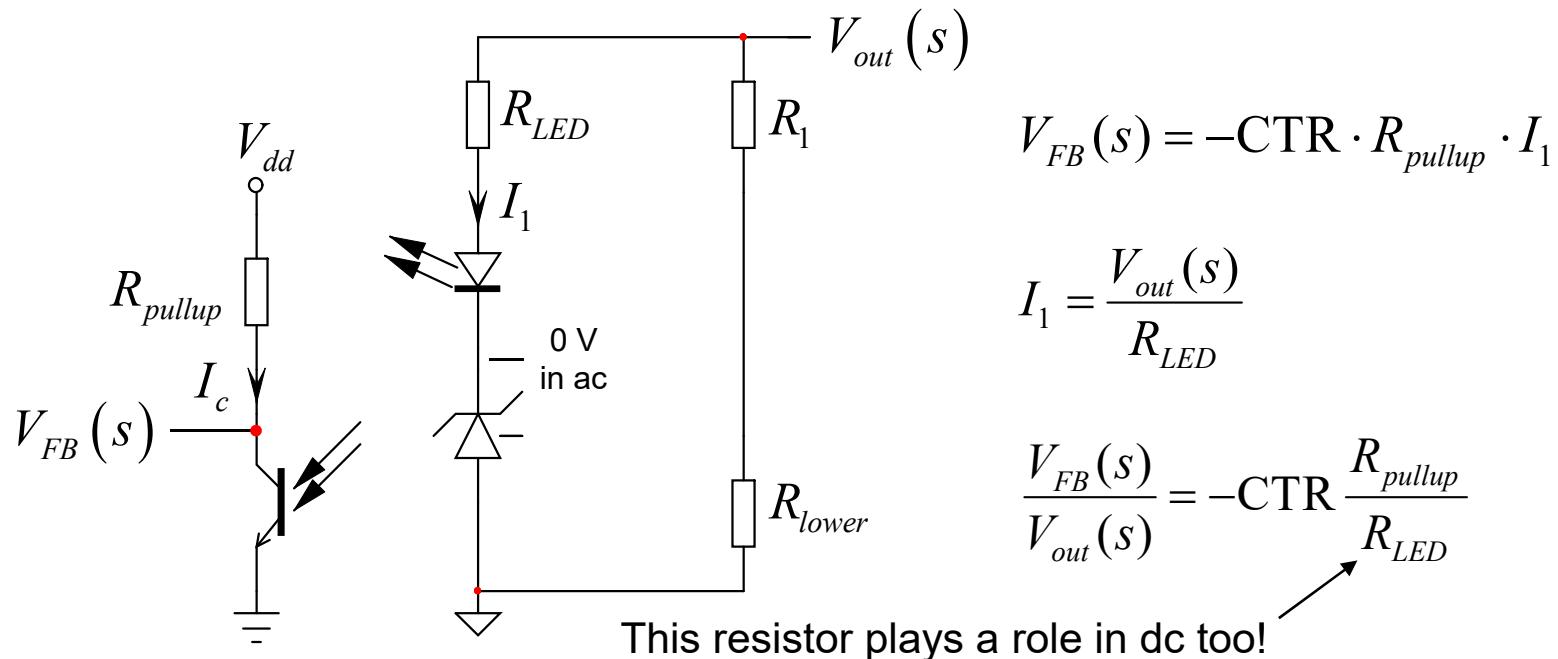
- R_{LED} must leave enough headroom over the TL431: upper limit!

Understanding the Fast Lane Drawback

- This LED resistor is a design limiting factor in low output voltages:

$$R_{LED,max} \leq \frac{V_{out} - V_f - V_{TL431,min}}{V_{dd} - V_{CE,sat} + I_{bias} \text{CTR}_{\min} R_{pullup}} \text{CTR}_{\min}$$

- When the capacitor C_1 is a short-circuit, R_{LED} fixes the fast lane gain



The Static Gain Limit

- Let us assume the following design:

$$V_{out} = 5 \text{ V}$$

$$V_f = 1 \text{ V}$$

$$V_{TL431,\min} = 2.5 \text{ V}$$

$$V_{dd} = 4.8 \text{ V}$$

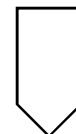
$$V_{CE,sat} = 300 \text{ mV}$$

$$I_{bias} = 1 \text{ mA}$$

$$\text{CTR}_{\min} = 0.3$$

$$R_{pullup} = 20 \text{ k}\Omega$$

$$R_{LED,\max} \leq \frac{5 - 1 - 2.5}{4.8 - 0.3 + 1m \times 0.3 \times 20k} \times 20k \times 0.3$$

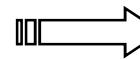


$$R_{LED,\max} \leq 857 \Omega$$



$$G_0 > \text{CTR} \frac{R_{pullup}}{R_{LED}} > 0.3 \frac{20}{0.857} > 7 \text{ or } \approx 17 \text{ dB}$$

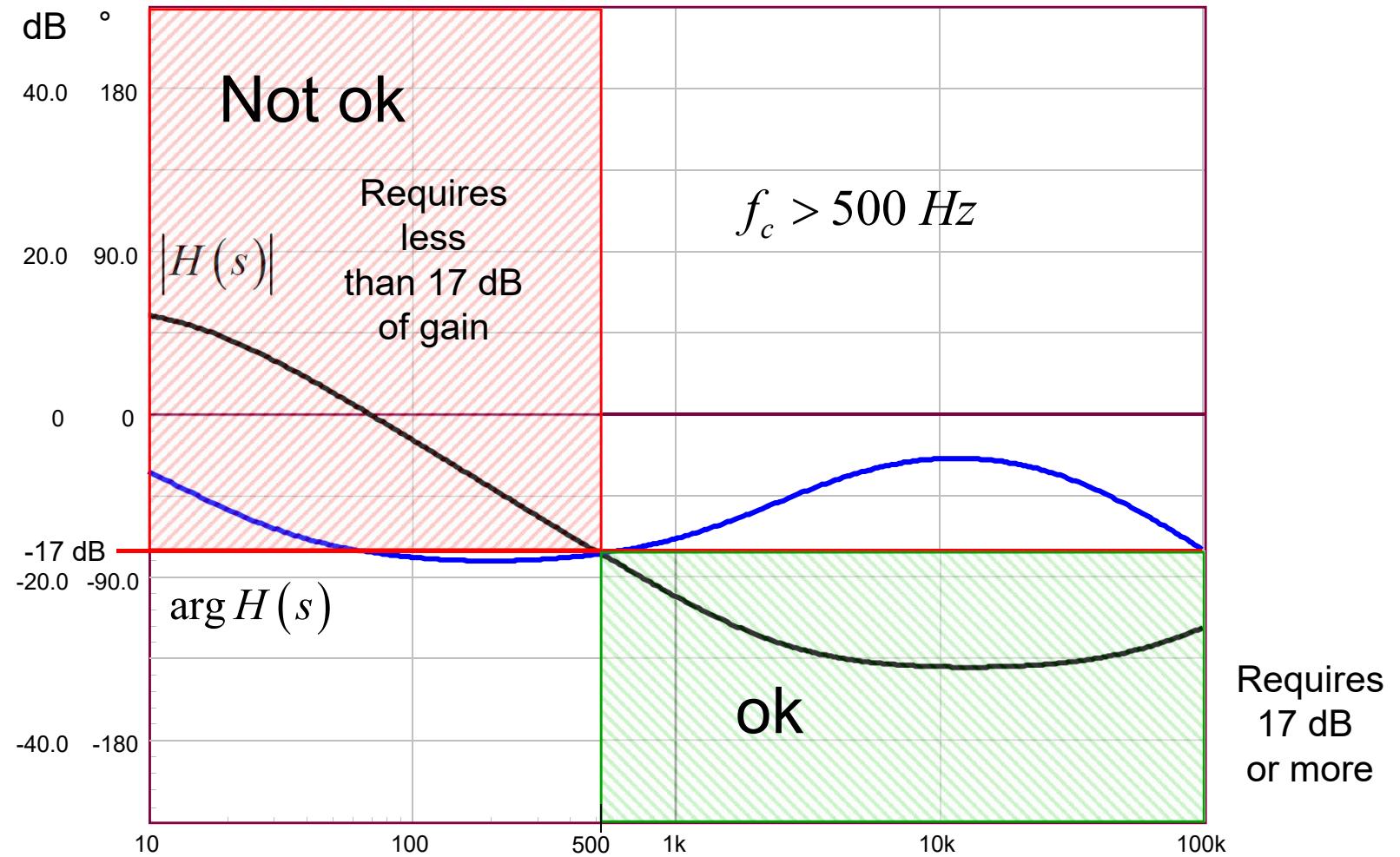
- In designs where R_{LED} fixes the gain, G_0 cannot be below 17 dB



You cannot “amplify” by less than 17 dB

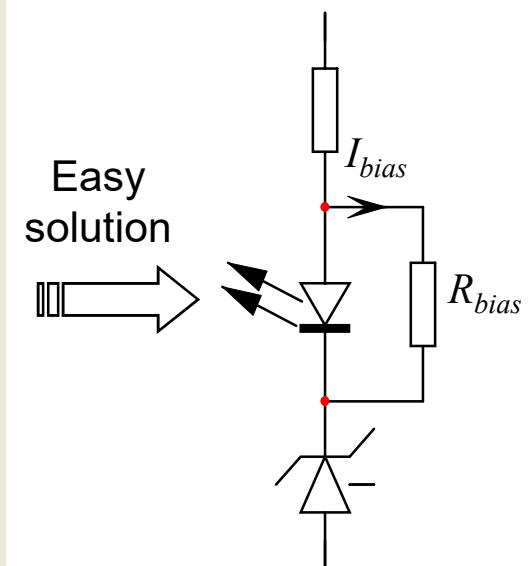
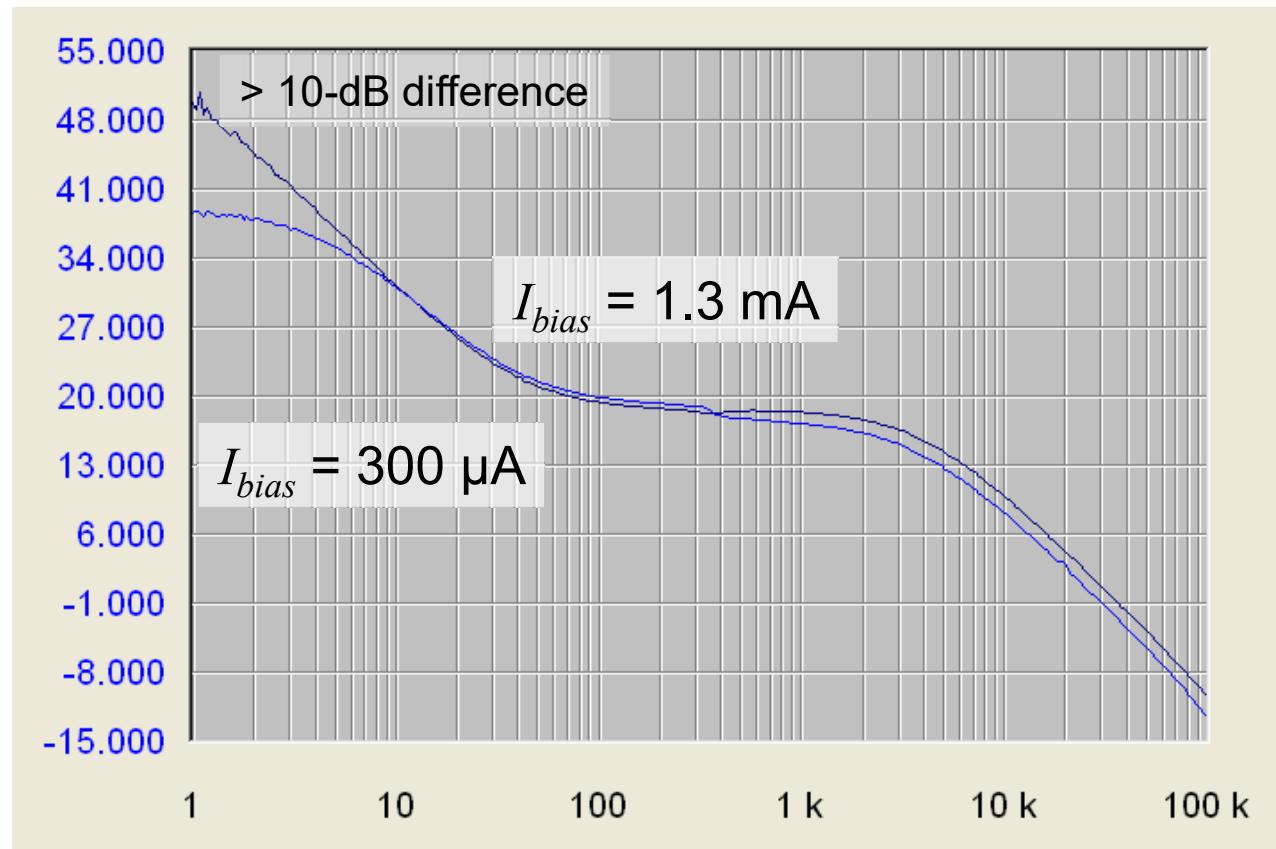
Forbidden Compensation Areas

- You must identify the areas where compensation is possible



Injecting Bias Current

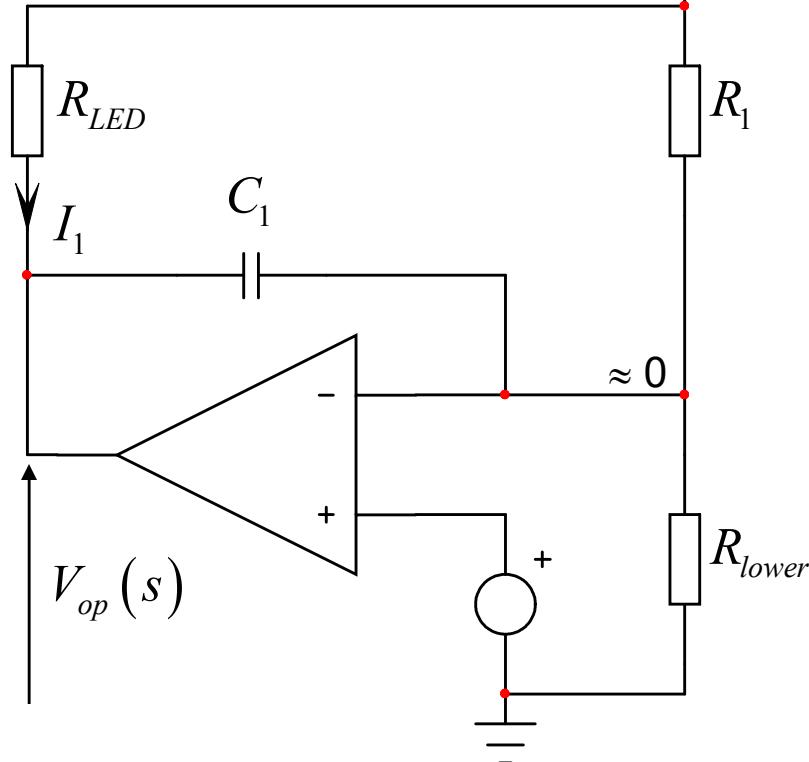
- Make sure enough current always biases the TL431
- If not, its open-loop suffers – a 10-dB difference can be observed!



$$R_{bias} = \frac{1}{1m} = 1 k\Omega$$

Small-Signal Analysis

- The TL431 is an open-collector op amp with a reference voltage
- Neglecting the LED dynamic resistance, we have:



$$I_1(s) = \frac{V_{out}(s) - V_{op}(s)}{R_{LED}}$$

$$V_{op}(s) = -V_{out}(s) \frac{sC_1}{R_{upper}} = -V_{out}(s) \frac{1}{sR_{upper}C_1}$$

$$I_1(s) = V_{out}(s) \frac{1}{R_{LED}} \left[1 + \frac{1}{sR_{upper}C_1} \right]$$

We know that: $V_{FB}(s) = -\text{CTR} \cdot R_{pullup} \cdot I_1$

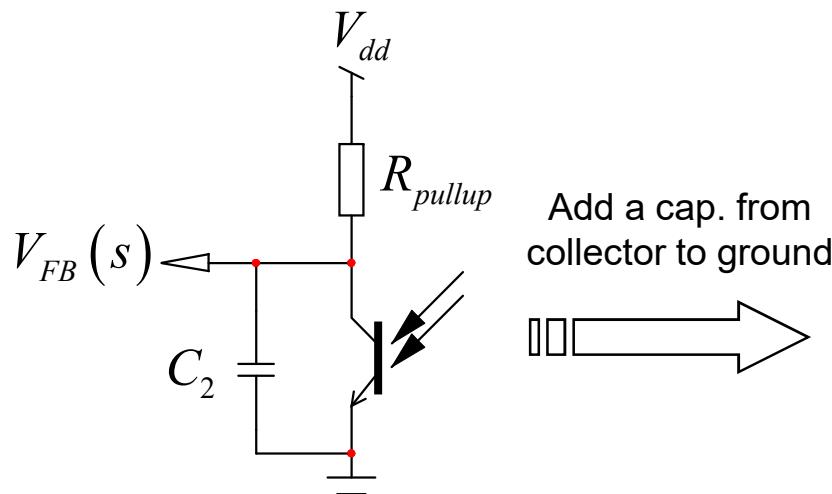
$$\frac{V_{FB}(s)}{V_{out}(s)} = -\frac{R_{pullup}\text{CTR}}{R_{LED}} \left[\frac{1 + sR_{upper}C_1}{sR_{upper}C_1} \right]$$

Creating a High-Frequency Pole

□ In the previous equation we have:

- ✓ a static gain $G_0 = \text{CTR} \frac{R_{pullup}}{R_{LED}}$
- ✓ a 0-dB origin pole frequency $\omega_{po} = \frac{1}{C_1 R_{upper}}$
- ✓ a zero $\omega_{z_1} = \frac{1}{R_{upper} C_1}$

□ We are missing a pole for the type 2!



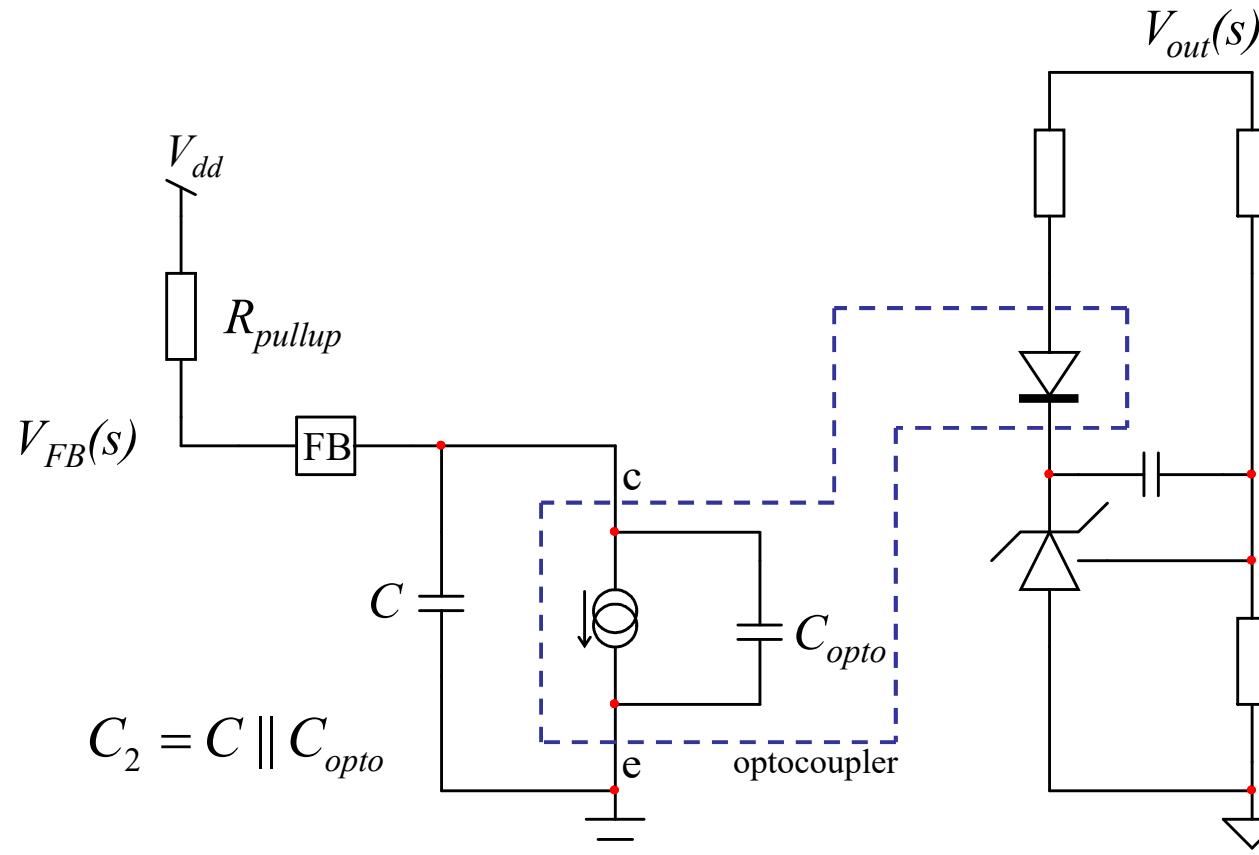
Add a cap. from
collector to ground

Type 2 transfer function

$$\frac{V_{FB}(s)}{V_{out}(s)} = -\frac{R_{pullup} \text{CTR}}{R_{LED}} \left[\frac{1 + sR_{upper}C_1}{sR_{upper}C_1(1 + sR_{pullup}C_2)} \right]$$

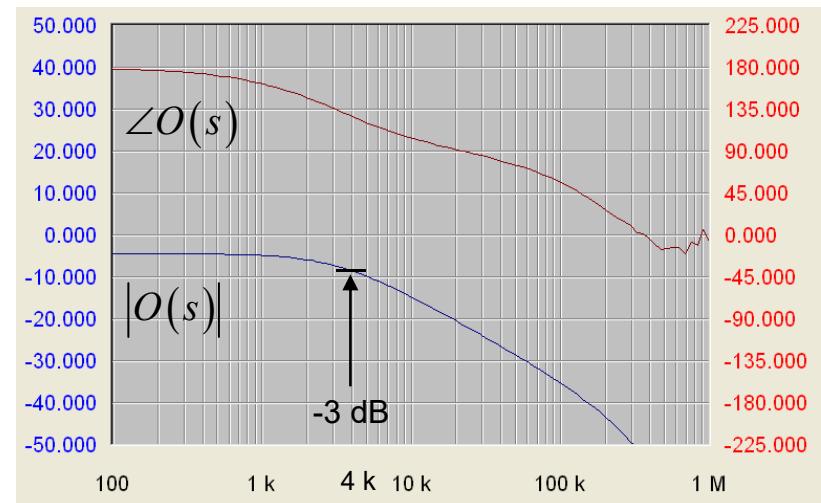
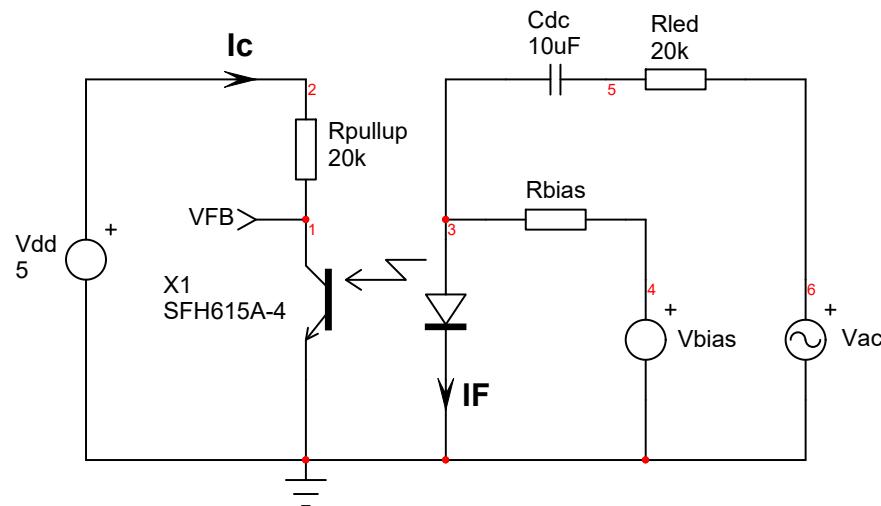
Understanding the Optocoupler Pole

- The optocoupler also features a parasitic capacitor
 - it comes in parallel with C_2 and must be accounted for



Extracting the Pole

- The optocoupler must be characterized to know where its pole is



- Adjust V_{bias} to have V_{FB} at 2-3 V to be in linear region, then ac sweep
- The pole in this example is found at 4 kHz

$$C_{opto} = \frac{1}{2\pi R_{pullup} f_{pole}} = \frac{1}{6.28 \times 20k \times 4k} \approx 2 \text{ nF}$$

Another design constraint!

The TL431 in a Type 1 Compensator

- To make a type 1 (origin pole only) neutralize the zero and the pole

$$\frac{V_{FB}(s)}{V_{out}(s)} = -\frac{R_{pullup} \text{CTR}}{R_{LED}} \left[\frac{1 + sR_{upper}C_1}{sR_{upper}C_1(1 + sR_{pullup}C_2)} \right]$$

$$sR_{upper}C_1 = sR_{pullup}C_2 \quad \Rightarrow \quad C_1 = \frac{R_{pullup}}{R_{upper}}C_2 \quad \text{substitute} \quad \omega_{po} = \frac{1}{\frac{R_{upper}R_{LED}}{R_{pullup}\text{CTR}}C_1}$$
$$\omega_{po} = \frac{\text{CTR}}{C_2 R_{LED}} \quad \Rightarrow \quad C_2 = \frac{\text{CTR}}{2\pi f_{po} R_{LED}}$$

- Once neutralized, you are left with an integrator

$$G(s) = \frac{1}{s} \rightarrow |G(f_c)| = \frac{f_{po}}{f_c} \rightarrow f_{po} = G_{f_c} f_c \quad \Rightarrow \quad C_2 = \frac{\text{CTR}}{2\pi G_{f_c} f_c R_{LED}}$$

A Type 1 Design Example

- We want a 5-dB gain at 5 kHz to stabilize the 5-V converter

$$V_{out} = 5 \text{ V}$$

$$V_f = 1 \text{ V}$$

$$V_{TL431,\min} = 2.5 \text{ V}$$

$$V_{dd} = 4.8 \text{ V}$$

$$V_{CE,sat} = 300 \text{ mV}$$

$$I_{bias} = 1 \text{ mA}$$

$$\text{CTR}_{\min} = 0.3$$

$$R_{pullup} = 20 \text{ k}\Omega$$

$$G_{fc} = 10^{\frac{5}{20}} = 1.77$$

$$f_c = 5 \text{ kHz}$$

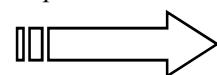
$$R_{LED,\max} \leq 857 \Omega \xrightarrow{\text{Apply 15% margin}} R_{LED} = 728 \Omega$$

}

}

$$C_2 = \frac{\text{CTR}}{2\pi G_{f_c} f_c R_{LED}} = \frac{0.3}{6.28 \times 1.77 \times 5k \times 728} \approx 7.4 \text{ nF}$$

$$C_{opto} = 2 \text{ nF}$$



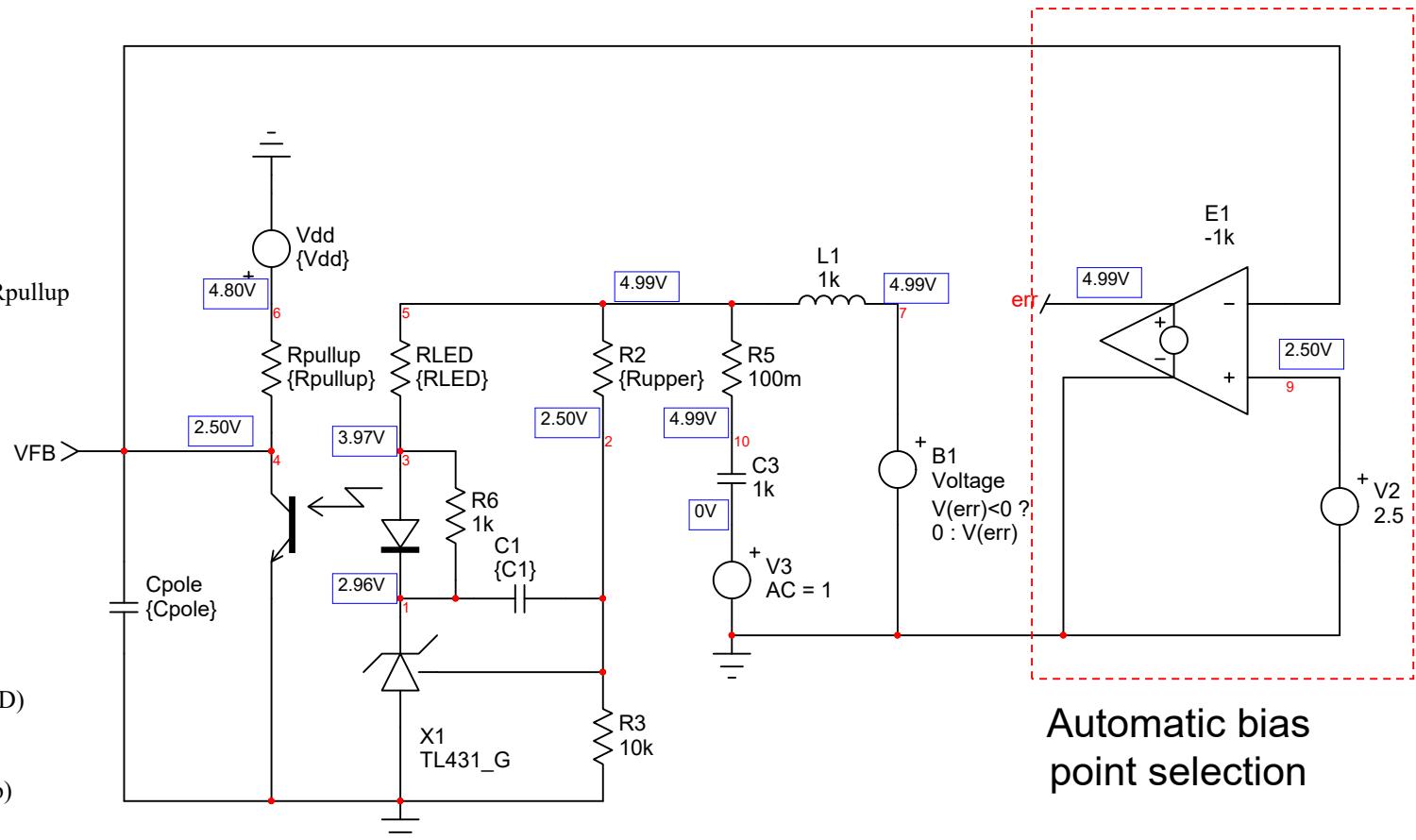
$$C = 7.4n - 2n = 5.4 \text{ nF}$$

$$C_1 = \frac{R_{pullup}}{R_{upper}} C_2 \approx 14.7 \text{ nF}$$

Simulation of the Type 1

- SPICE can simulate the design – automate elements calculations...

parameters
 Vout=5
 Vf=1
 Vref=2.5
 VCEsat=300m
 Vdd=4.8
 Ibias=1m
 $A = Vout - Vf - Vref$
 $B = Vdd - VCEsat + Ibias * CTR * Rpullup$
 $Rmax = (A/B) * Rpullup * CTR$
 $Rupper = (Vout - 2.5) / 250\mu$
 $f_c = 5k$
 $G_{fc} = -5$
 $G = 10^{(-G_{fc}/20)}$
 $\pi = 3.14159$
 $Fpo = G * f_c$
 $Rpullup = 20k$
 $RLED = Rmax * 0.85$
 $C1 = Cpole1 * Rpullup / Rupper$
 $Cpole1 = CTR / (2 * \pi * Fpo * RLED)$
 $Cpole = Cpole1 - Cpto$
 $Cpto = 4k$
 $Cpto = 1 / (2 * \pi * Fopto * Rpullup)$
 $CTR = 0.3$



Automatic bias
point selection

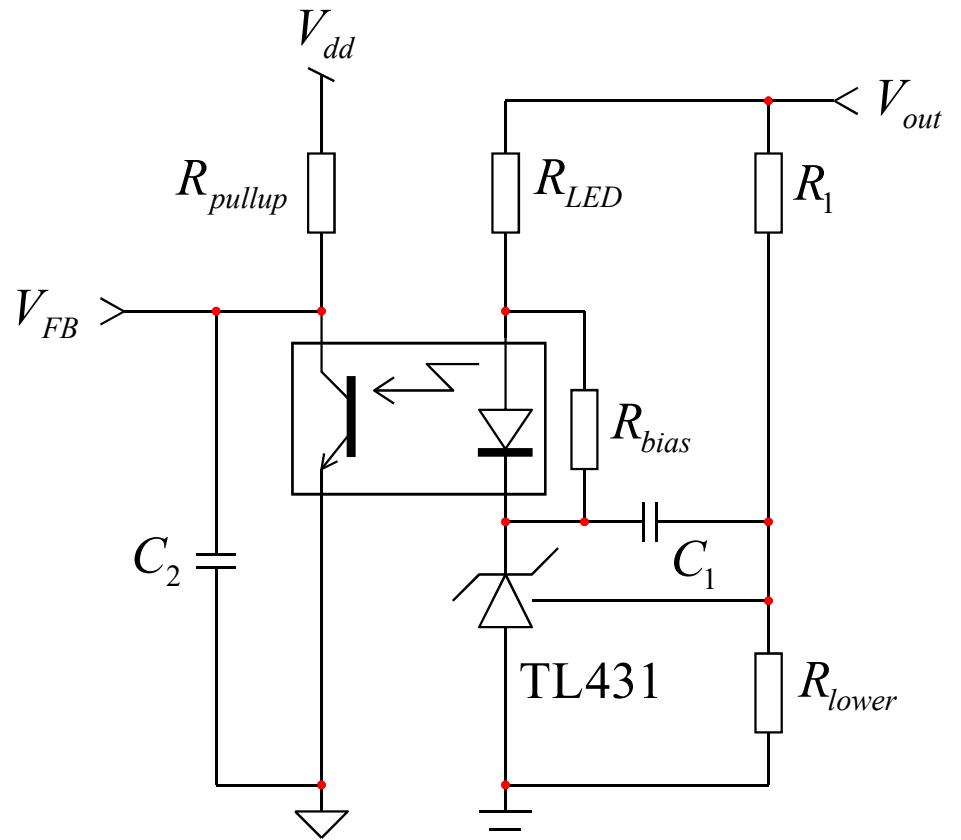
Type 1 Simulation Results

- The pullup resistor is 1 kΩ and the target now reaches 5 dB



The TL431 in a Type 2 Compensator

- Our first equation was already a type 2 definition, we are all set!



$$G_0 = \text{CTR} \frac{R_{pullup}}{R_{LED}}$$

$$\omega_{z_1} = \frac{1}{R_1 C_1}$$

$$\omega_{p_1} = \frac{1}{R_{pullup} C_2}$$

- Just make sure the optocoupler contribution is involved...

Deriving Component Values for the Type 2

- You need to provide a 15-dB gain at 5 kHz with a 50° boost

$$f_p = \left[\tan(\text{boost}) + \sqrt{\tan^2(\text{boost}) + 1} \right] f_c = 2.74 \times 5k = 13.7 \text{ kHz}$$

$$f_z = f_c^2 / f_p = 25k / 13.7k \approx 1.8 \text{ kHz} \quad G_0 = \text{CTR} \frac{R_{\text{pullup}}}{R_{\text{LED}}} = 10^{15/20} = 5.62$$

- With a 250- μ A bridge current, the divider resistor is made of:

$$R_{\text{lower}} = 2.5 / 250\mu\text{A} = 10 \text{ k}\Omega \quad R_1 = (12 - 2.5) / 250\mu\text{A} = 38 \text{ k}\Omega$$

- The pole and zero respectively depend on R_{pullup} and R_1 :

$$C_2 = 1 / 2\pi f_p R_{\text{pullup}} = 581 \text{ pF} \quad C_1 = 1 / 2\pi f_z R_1 = 2.3 \text{ nF}$$

- The LED resistor depends on the needed mid-band gain:

$$R_{\text{LED}} = \frac{R_{\text{pullup}} \text{CTR}}{G_0} = 1.06 \text{ k}\Omega \xrightarrow{\text{ok}} R_{\text{LED,max}} \leq 4.85 \text{ k}\Omega$$



Checking the Optocoupler Contribution

- The optocoupler is still at a 4-kHz frequency:

$$C_{pole} \approx 2 \text{ nF}$$

Already above!

- Type 2 pole capacitor calculation requires a 581-pF cap.!



The bandwidth cannot be reached, reduce f_c !

- For noise purposes, we want a minimum of 100 pF for C
- With a total capacitance of 2.1 nF, the highest pole can be:

$$f_{pole} = \frac{1}{2\pi R_{pullup} C} = \frac{1}{6.28 \times 20k \times 2.1n} = 3.8 \text{ kHz}$$

- For a 50° phase boost and a 3.8-kHz pole, the crossover must be:

$$f_c = \frac{f_p}{\tan(\text{boost}) + \sqrt{\tan^2(\text{boost}) + 1}} \approx 1.4 \text{ kHz}$$

Placing the Zero in the Transfer Function

- The zero is then simply obtained:

$$f_z = \frac{f_c^2}{f_p} = 516 \text{ Hz}$$

- We can re-derive the component values and check they are ok

$$C_2 = 1/2\pi f_p R_{pullup} = 2.1 \text{ nF} \quad C_1 = 1/2\pi f_z R_1 = 8.1 \text{ nF}$$

- Given the 2-nF optocoupler capacitor, we just add 100 pF

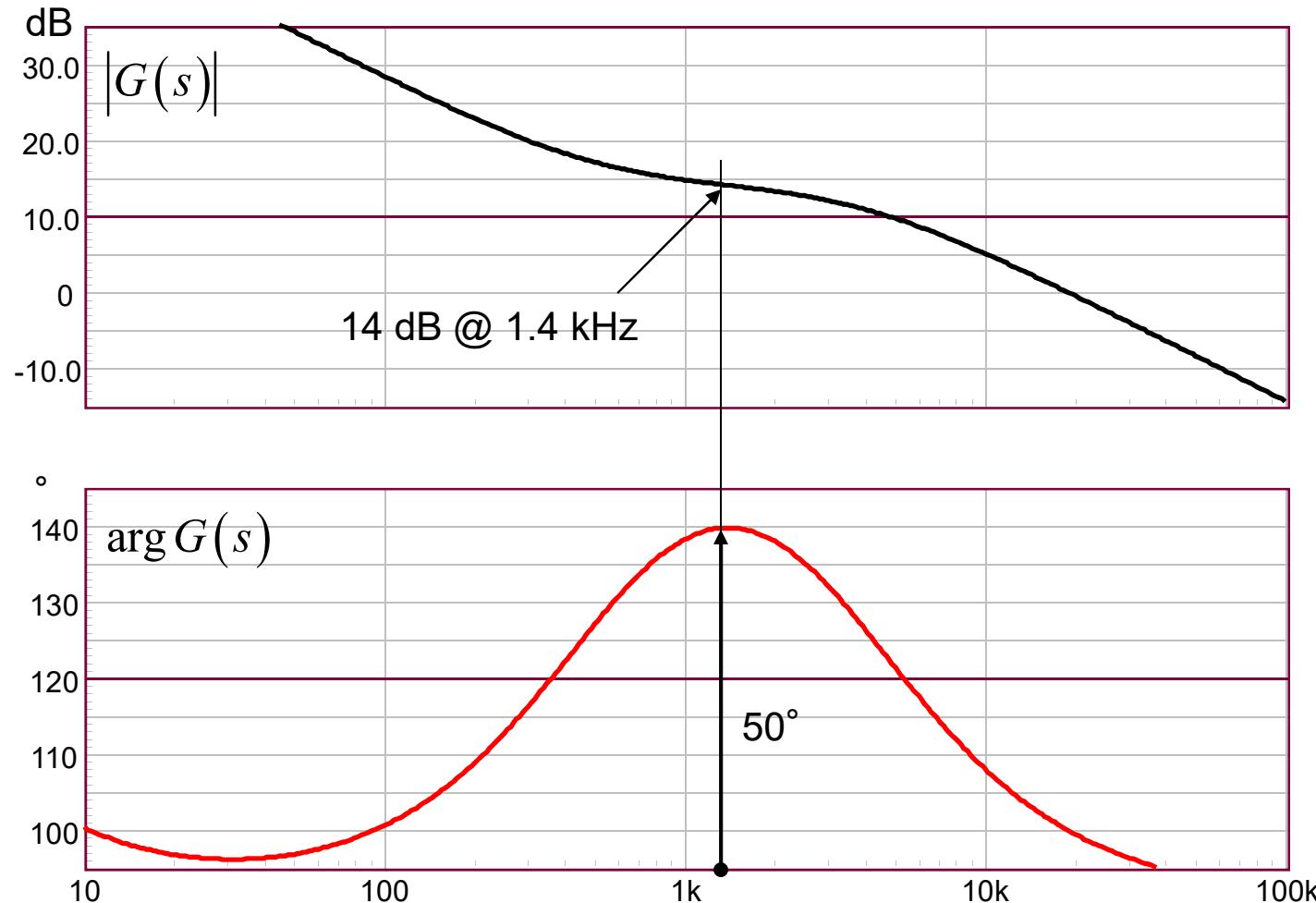
- In this example, $R_{LED,max}$ is 4.85 kΩ

$$G_0 > \text{CTR} \frac{R_{pullup}}{R_{LED}} > 0.3 \frac{20}{4.85} > 1.2 \text{ or } \approx 1.8 \text{ dB}$$

- You cannot use this type 2 if an attenuation is required at f_c !

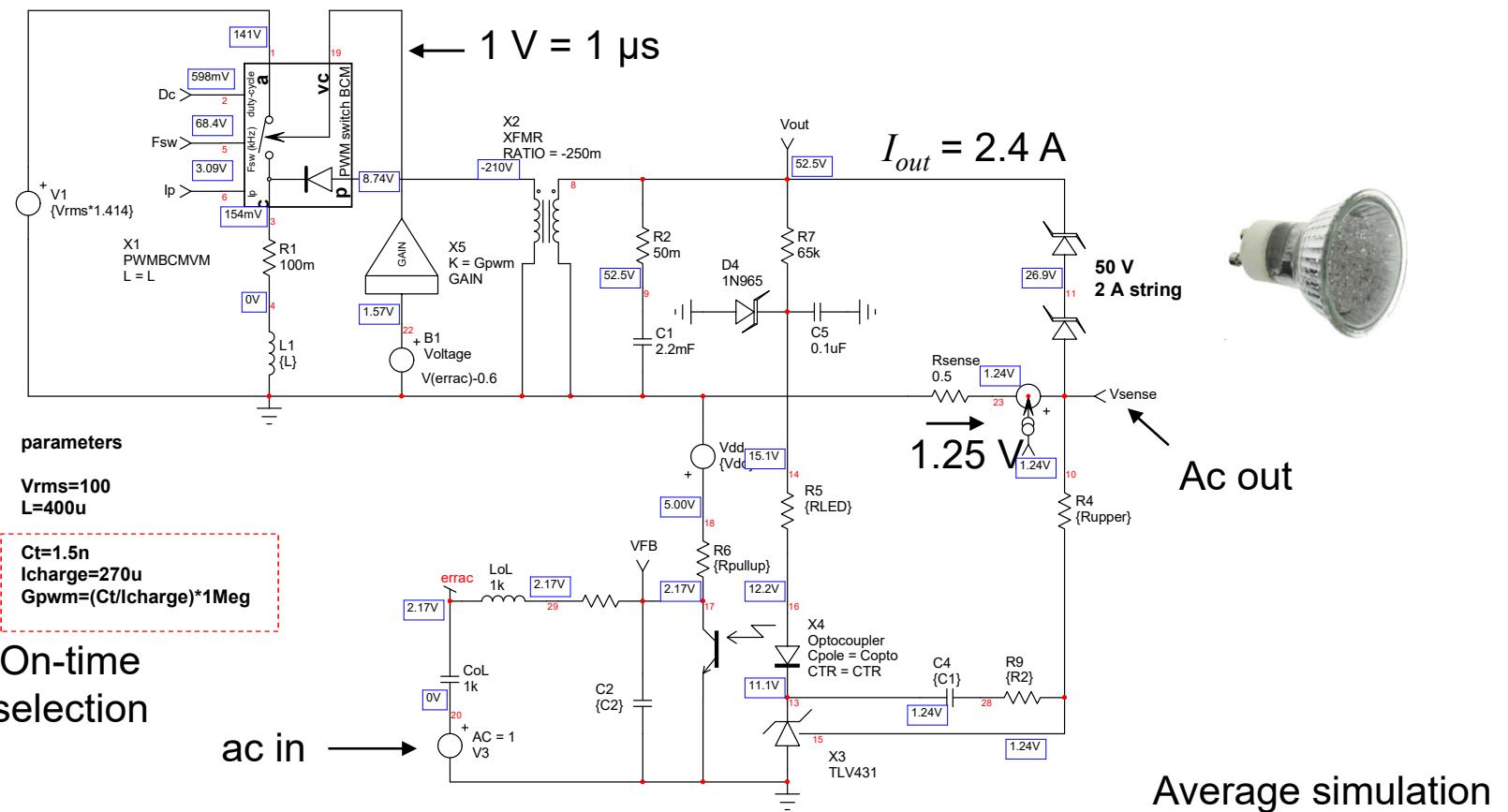
TL431 type 2 Design Example

- The 1-dB gain difference is linked to R_d and the bias current



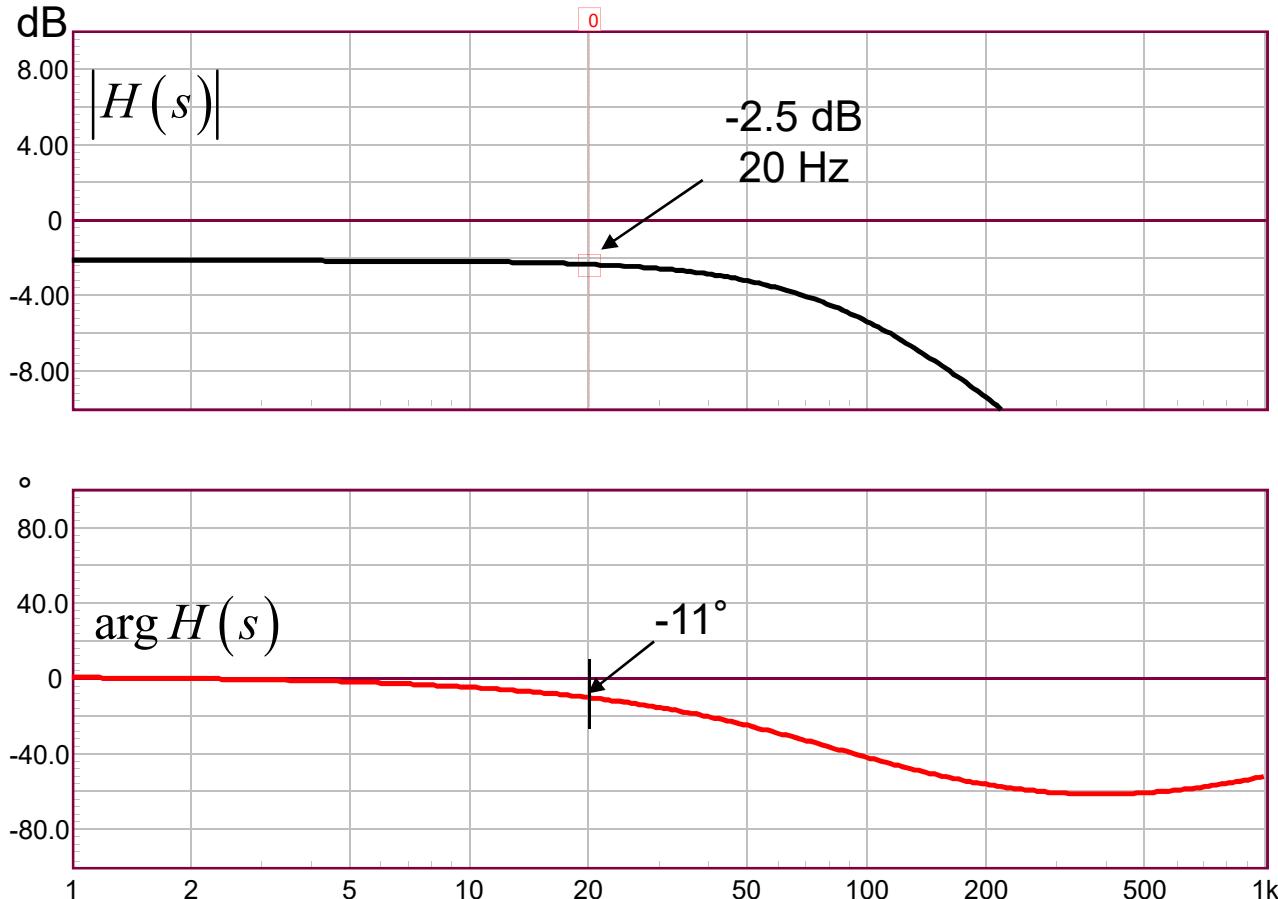
Design Example 1 – a Single-Stage PFC

- The single-stage PFC is often used in LED applications
- It combines isolation, current-regulation and power factor correction
- Here, a constant on-time BCM controller, the **NCP1608**, is used



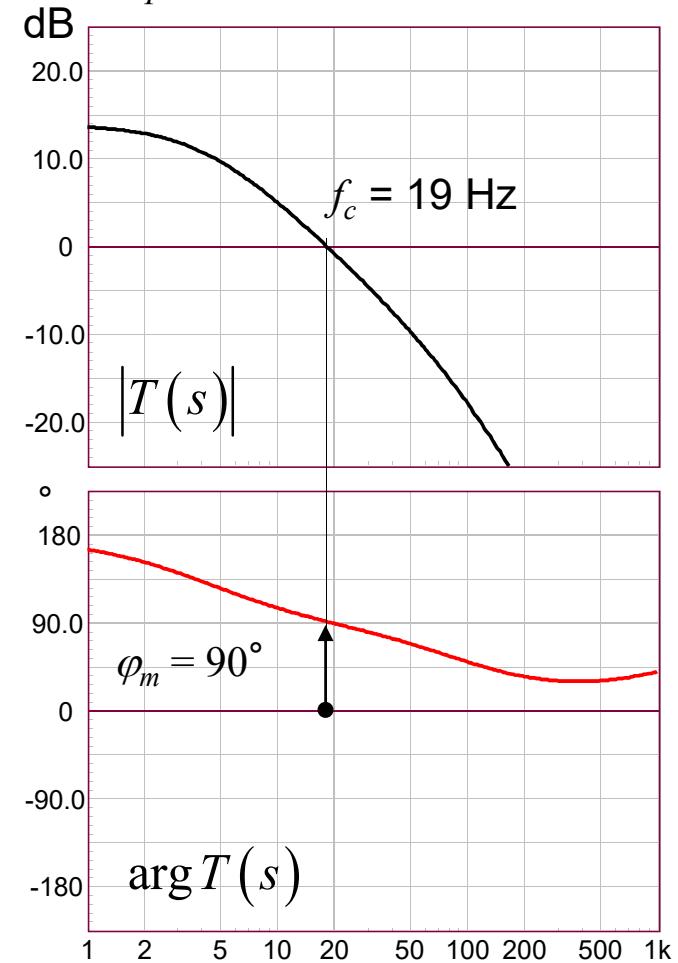
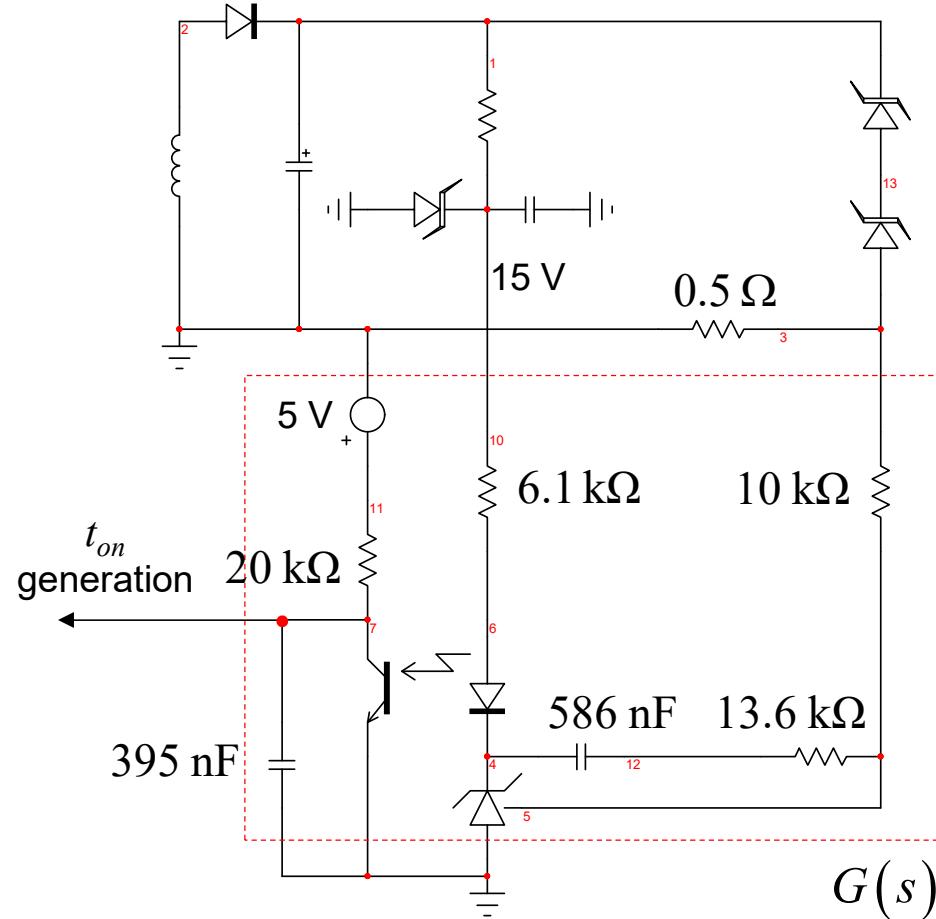
Design Example 1 – a Single-Stage PFC

- Once the converter elements are known, ac-sweep the circuit
- Select a crossover low enough to reject the ripple, e.g. 20 Hz



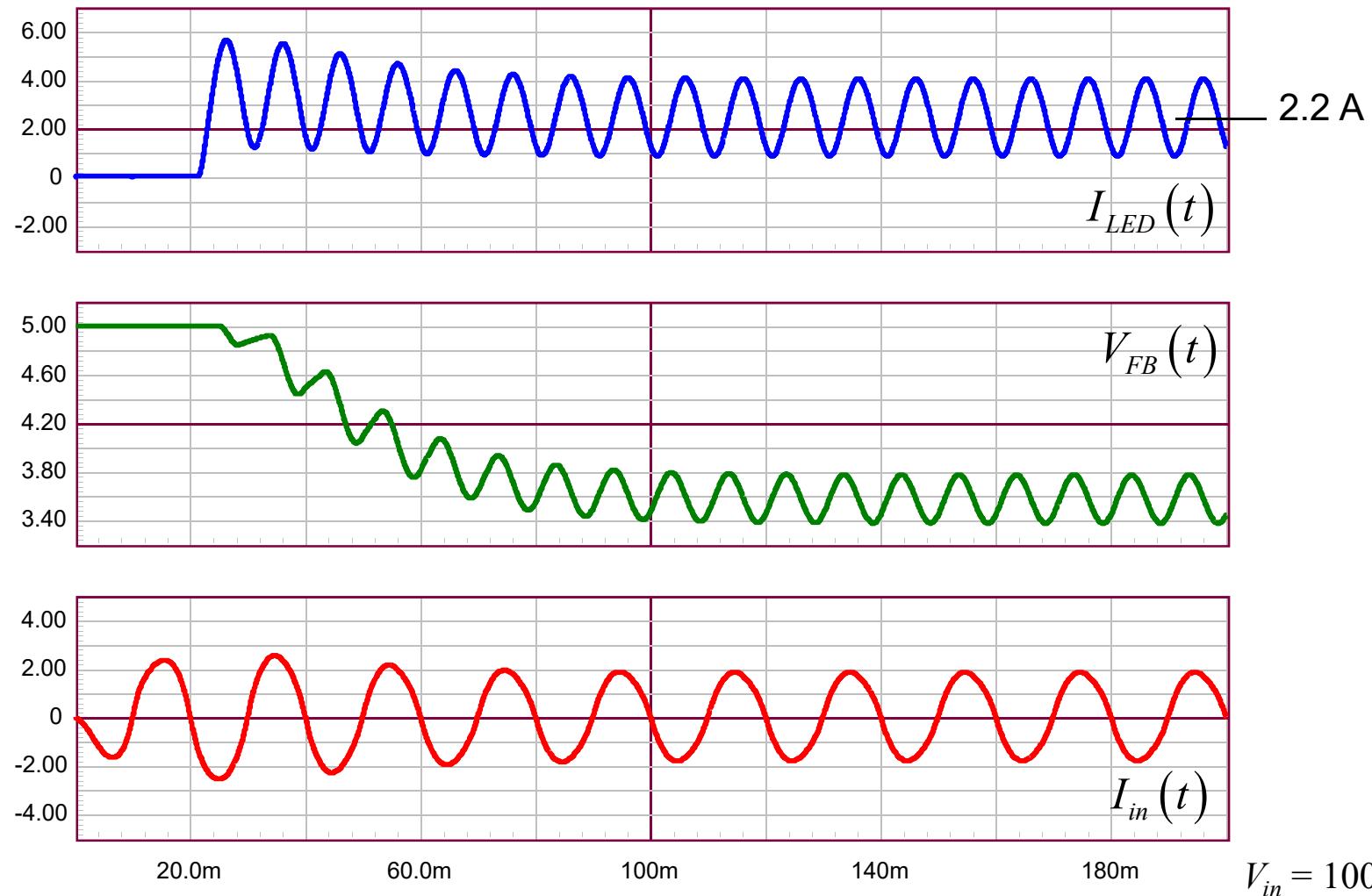
Design Example 1 – a Single-Stage PFC

- Given the low phase lag, a type 1 can be chosen
- Use the type 2 with fast lane removal where f_p and f_z are coincident



Design Example 1 – a Single-Stage PFC

- ❑ A transient simulation helps to test the system stability

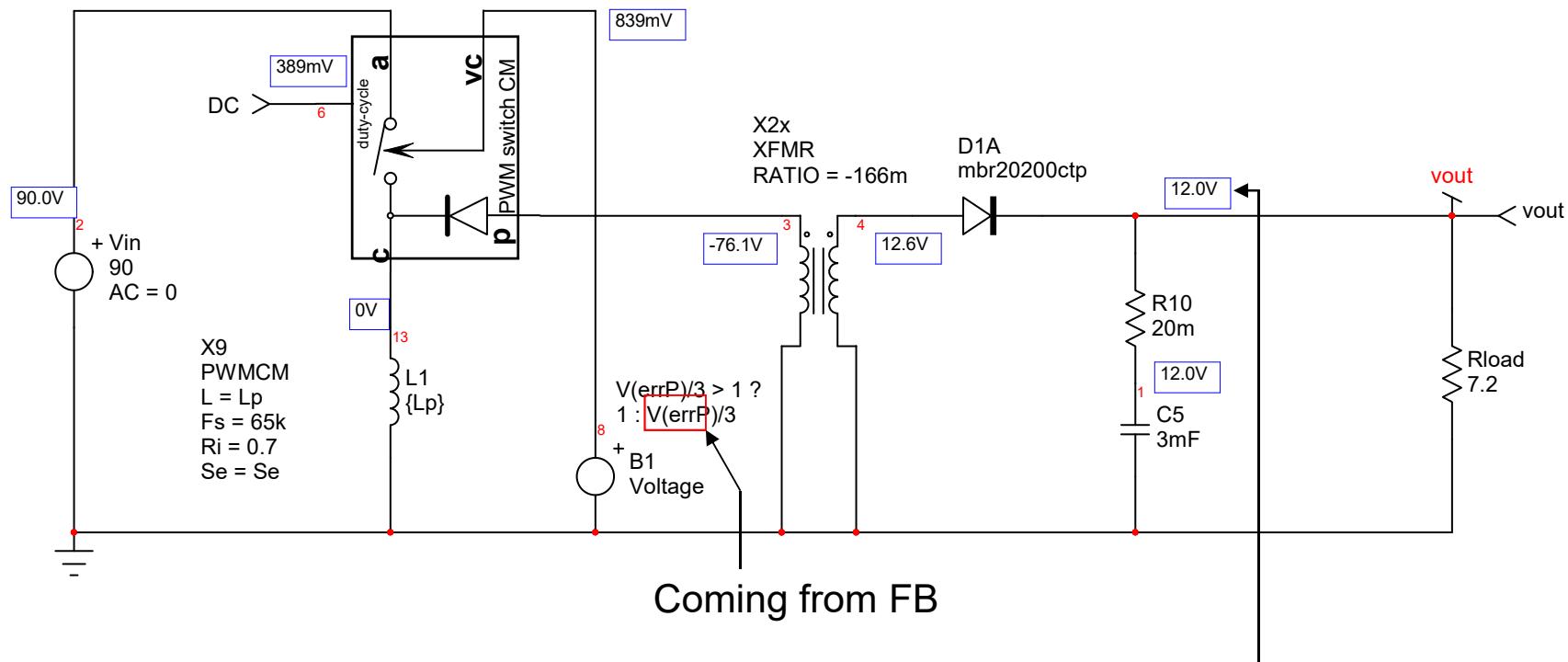


Design Example 2: a DCM Flyback Converter

- We want to stabilize a 20-W DCM adapter
 - $V_{in} = 85$ to 265 V rms, $V_{out} = 12$ V/ 1.7 A
 - $F_{sw} = 65$ kHz, $R_{pullup} = 20$ kΩ
 - Optocoupler is SFH-615A, pole is at 6 kHz
 - Cross over target is 1 kHz
 - Selected controller: NCP1216
1. Obtain a power stage open-loop Bode plot, $H(s)$
 2. Look for gain and phase values at cross over
 3. Compensate gain and build phase at cross over, $G(s)$
 4. Run a loop gain analysis to check for margins, $T(s)$
 5. Test transient responses in various conditions

Design Example 2: a DCM Flyback Converter

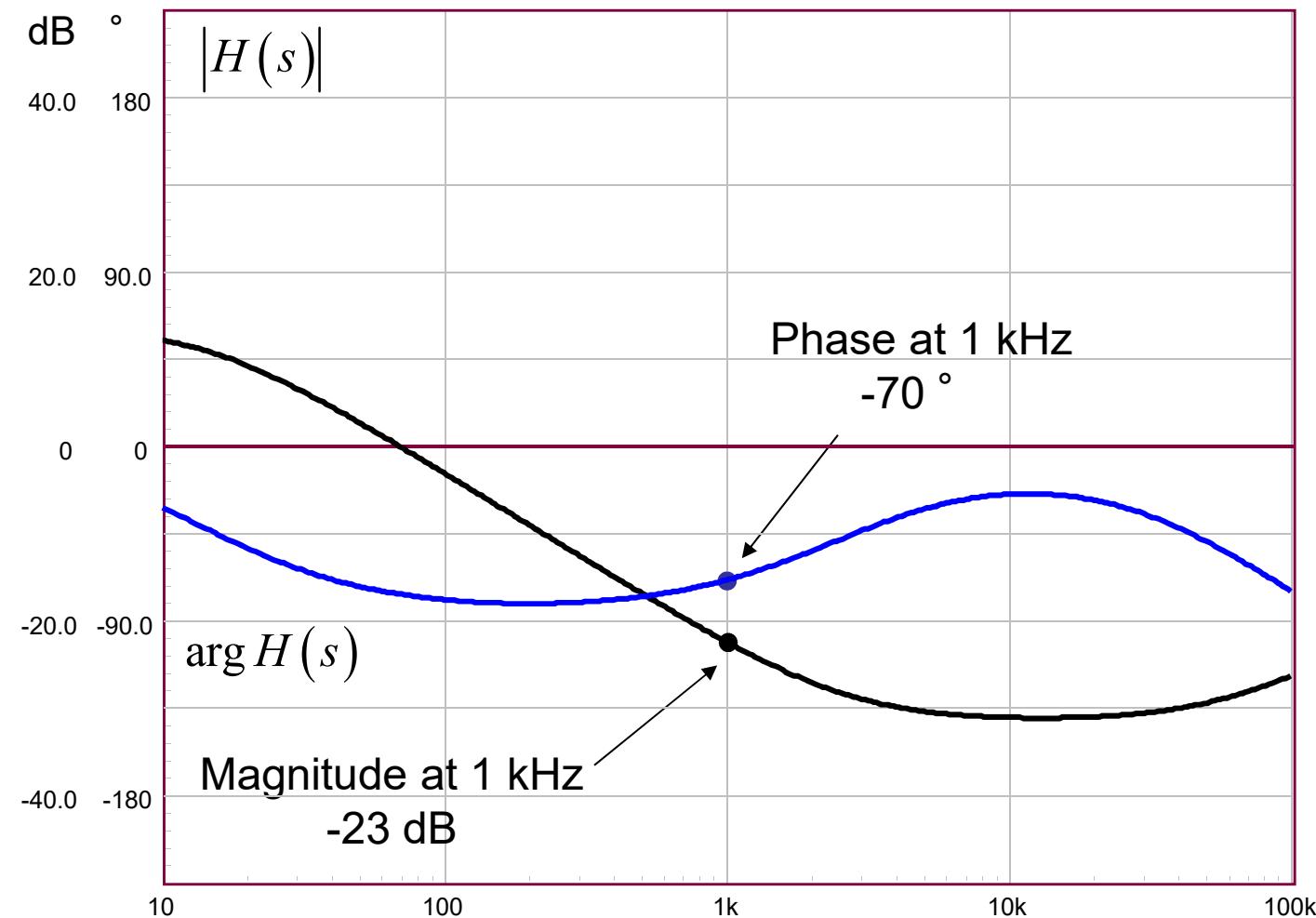
- Capture a SPICE schematic with an averaged model



- Look for the bias points values: $V_{out} = 12 \text{ V}$, ok

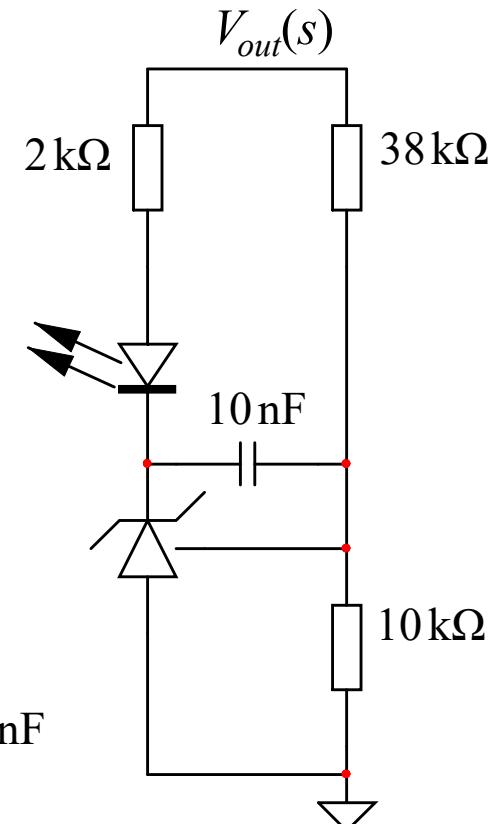
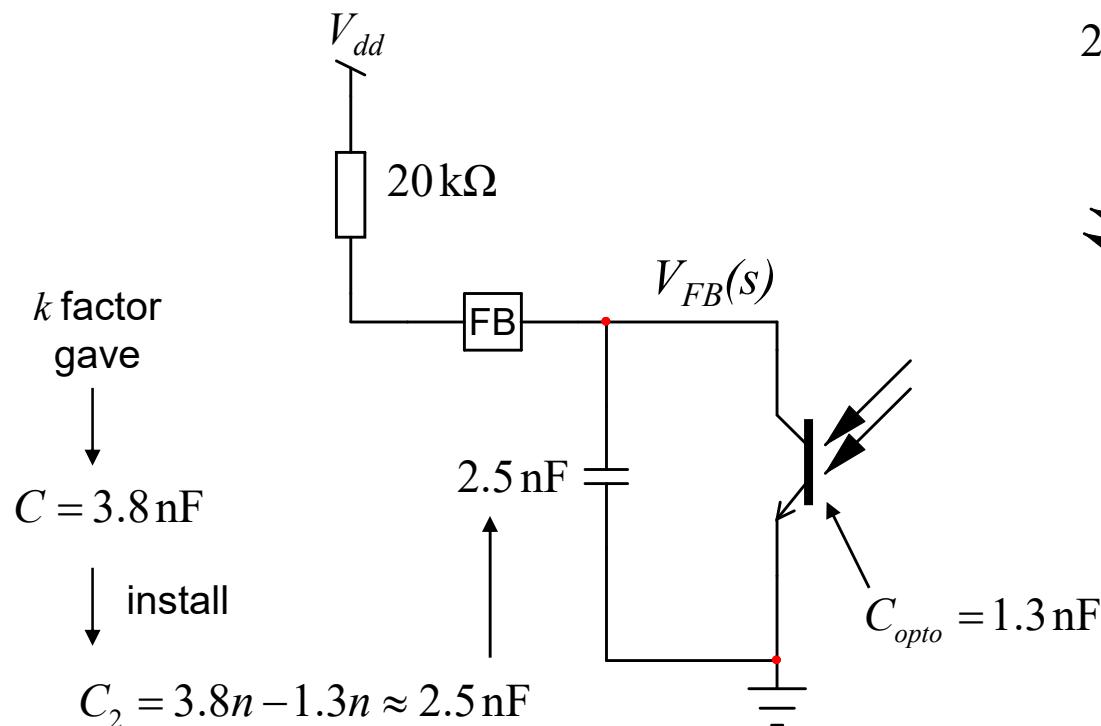
Design Example 2: a DCM Flyback Converter

- Observe the open-loop Bode plot and select f_c : 1 kHz



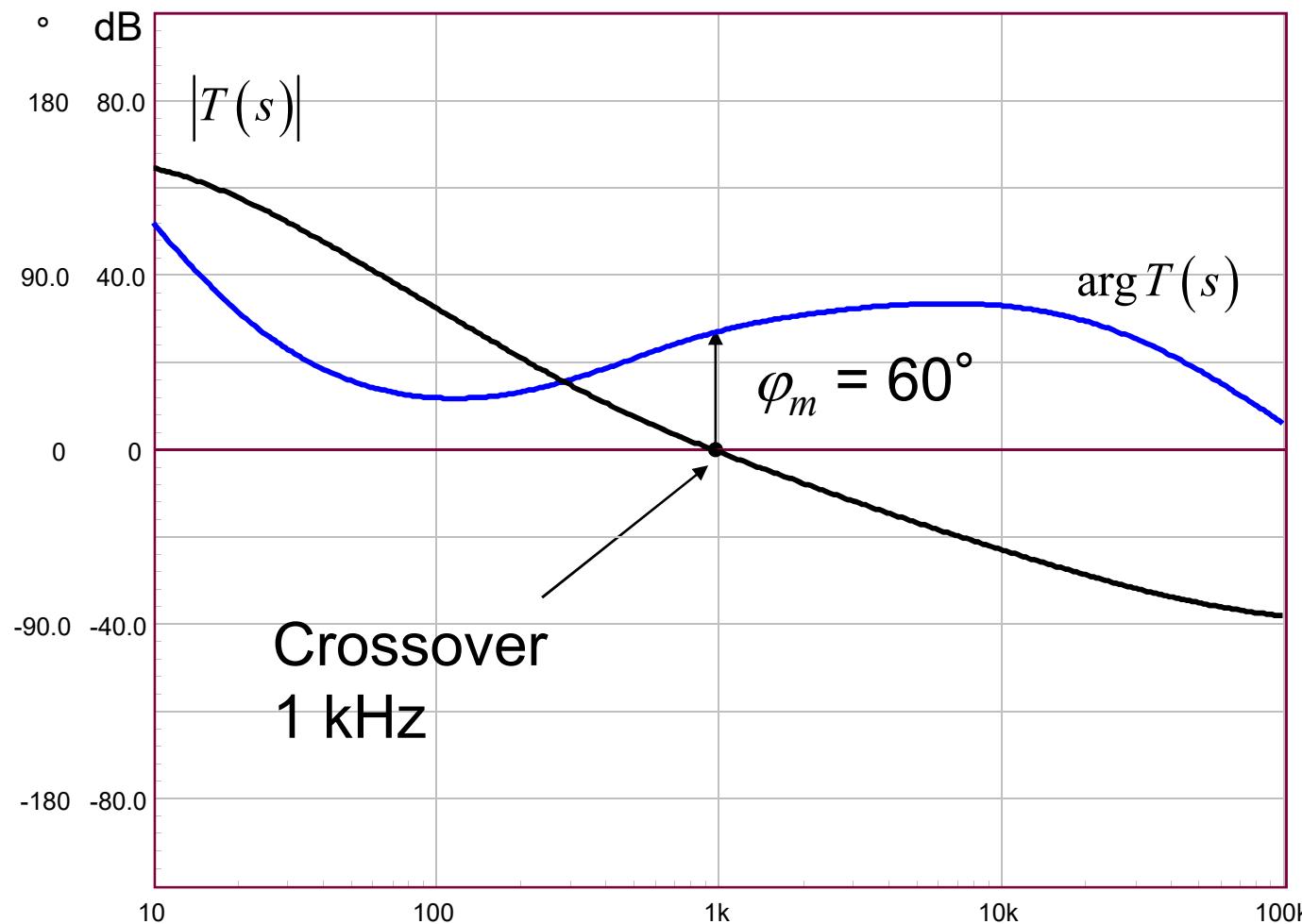
Design example 2: a DCM flyback converter

- Apply k factor or other method, get f_z and f_p
 - $f_z = 3.5 \text{ kHz}$ $f_p = 4.5 \text{ kHz}$



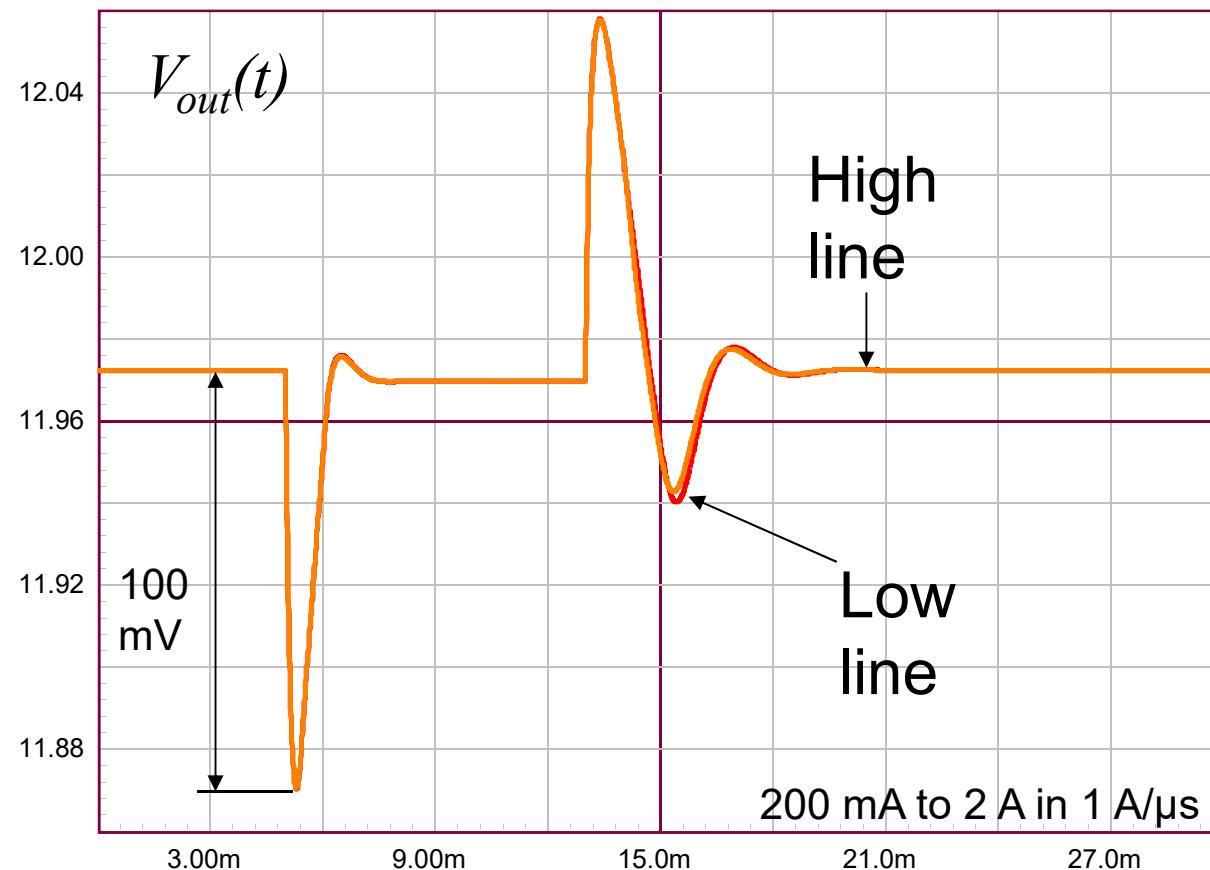
Design example 2: a DCM Flyback Converter

- Check loop gain and watch phase margin at f_c



Design Example 2: a DCM Flyback Converter

- Sweep ESR values and check margins again



Conclusion

- The flyback converter hides several parasitic elements
- Understanding where they hide and how they move is key!
- Despite CM overwhelming presence, QR designs grow
- CM is a 3rd-order system whereas QR is 1st order
- TL431 lends itself well for compensation, watch the optocoupler!
- SPICE eases and speed-up the design
- Always check theoretical assumptions with bench measurement



Merci !
Thank you!
Xiè-xie!