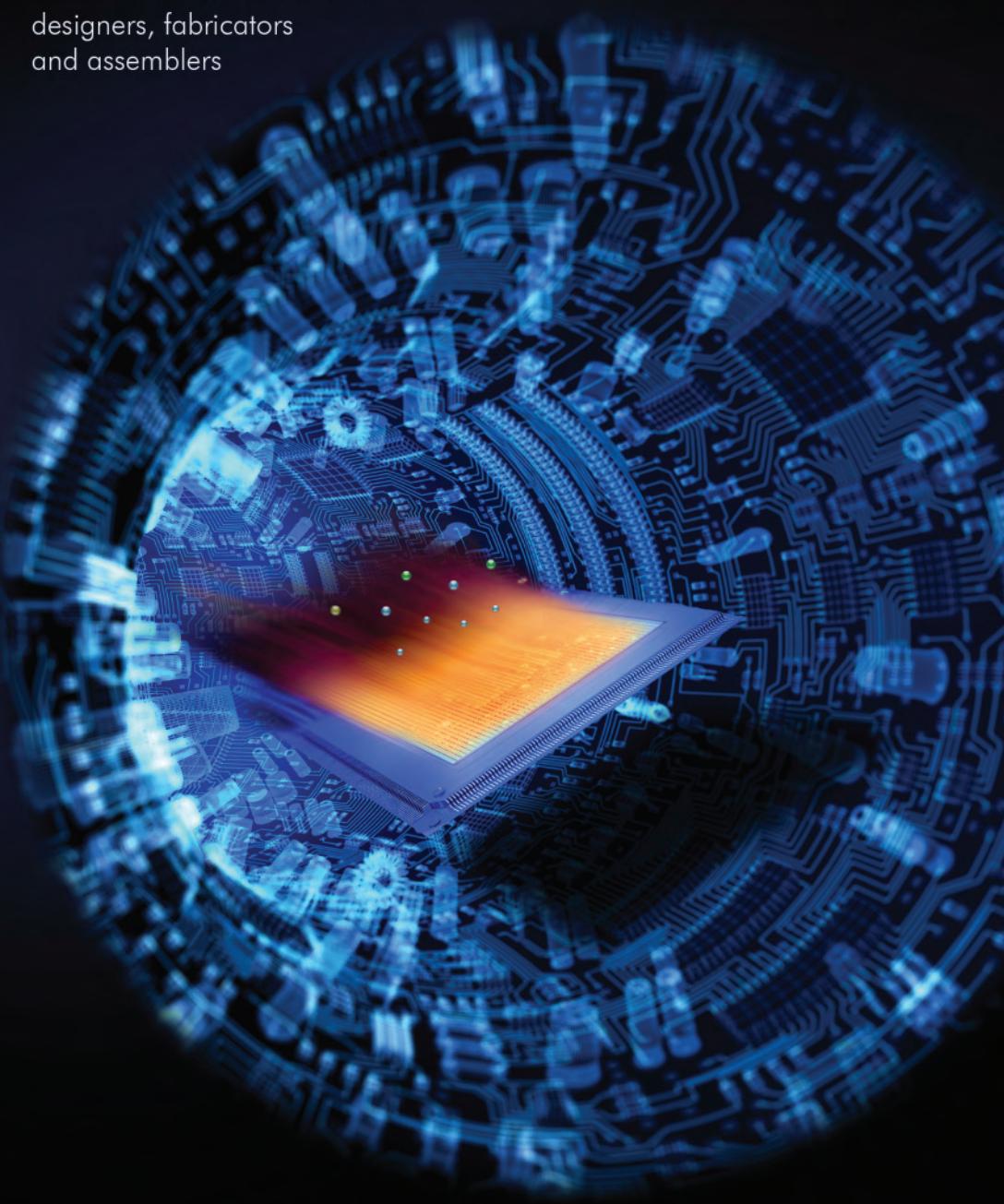


THE HDI HANDBOOK

A comprehensive high-density
interconnection resource for
designers, fabricators
and assemblers

first edition



Written by Happy Holden, et al.

The HDI Handbook
First Edition
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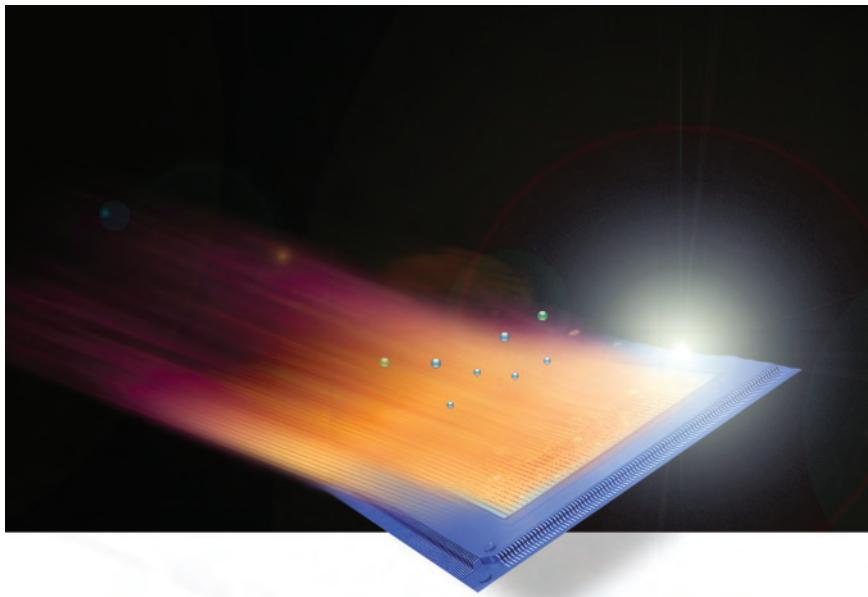
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The HDI Handbook

**A comprehensive high-density
interconnection resource for designers,
fabricators and assemblers**

First Edition

Written by Happy Holden, et al.

Edited by Happy Holden and Diane Neer

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FOREWORD

By

Clyde F. Coombs, Jr.

Editor-In-Chief, Printed Circuits Handbook

The Density Revolution - How To Make It Work For You

The printed circuit has been the basic building block of electronic devices since the beginning of the modern electronic age, just after the Second World War. Because of the printed circuit's unique ability to create large numbers of connections at a single solder step and its capability of being mass produced at a relatively low cost, it will undoubtedly hold this position for some time. Its continued viability is reinforced by the fact that printed circuit technology has been able to adapt to the needs of the product designer and to the constraints of the component industry, as the relentless demands of *smaller, faster, cheaper* continue to define the market place.

While many feel that the term *printed circuit* has become incorrect and outdated and have proposed alternatives, *printed circuit* has become part of the international language of technology and carries no confusion about what it means. It denotes the general family of planar, sometimes flexible, non-conductive materials with conductive traces adhering to it and holes penetrating it that interconnect the components.

The development of printed circuit technology has been a series of *revolutions* forced by the interconnection needs of smaller, denser component structures, followed by *evolutionary* periods as new technologies matured and manufacturing

became more predictable and reliable. When the printed circuit was released, it was a planar board composed of a non-conductive supporting material with traces etched from a laminated sheet of copper connecting to annular rings around holes for component leads.

The next major advance that made the printed circuit technology indispensable and laid the foundation for what we see today, was the ability to put a conductive surface inside a hole in a non-conductive material. This revolution has allowed interconnected circuitry on two sides and through many layers, giving rise to the plated through-hole. The development of the plated through-hole is probably the least appreciated major technical advance of the twentieth century, for without it we would not have the ubiquitous electronic products that have become essential to everyday life.

As long as components had leads that penetrated the board, the board technology evolved predictably and slowly. However, the introduction of surface mount technology launched another major revolution. With surface mount technology, the component leads did not penetrate the substrate board. Board technology had to adapt, since the size of components were no longer constrained by the need to provide relatively large through-hole leads. They could shrink toward the size of the chip itself! It was also possible to use inner-layers without leaving space for holes through the board, which resulted in interconnection structures that were truly three-dimensional. With leads no longer required to go to the perimeter of the component package, they could exit anywhere. Board designers and manufacturers were driven to develop the means to access these ever-smaller connection points for further interconnection in the board, usually by penetrating the board with vias, the sole purpose

Foreword

of which was circuit continuity rather than lead connection. With the introduction of the Ball Grid Array (BGA), discussed in some detail in Chapter 1 – Introduction to High-Density Interconnects, board feature dimensions began dropping from fractions of an inch to thousandths of an inch until it became clear that the traditional manufacturing technologies had reached a point where they could no longer do the same things in the same ways, only smaller. A new revolution was upon the industry, one dubbed the *Density Revolution*, and it continues today. It has officially become the High-Density Interconnect (HDI) Revolution!

At first the challenge of HDI seemed to be making vias smaller, as mechanical drilling became almost impossible. However, HDI quickly raised issues that define the printed circuit technology, including materials, imaging, metallization, testing, assembly, and especially design, not only because of the geometries involved, but because of the electrical properties of the boards. Electrical parameters of the supporting material, which had not been a consideration, became an important concern due to the proximity of circuits combined with the high speed of new processors. The board has gone from a purely interconnective device to an important component in the overall product design.

In *The HDI Handbook*, editor-in-chief, Happy Holden, has brought together authors whose skills in particular elements of this new set of technological issues are of the highest caliber and who are respected throughout the industry. The collaboration of experts is critical since no one person can go into the detail required for so many different issues. The book is not meant to replace or repeat the discussions in the *Printed Circuits Handbook*, but to build upon those discussions and provide details which are beyond the scope of that book.

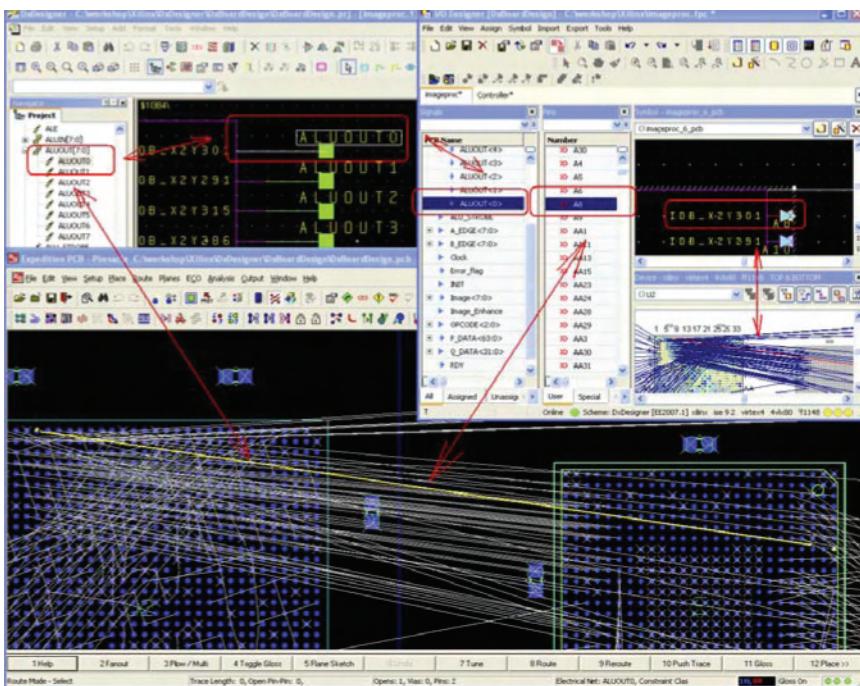
The HDI Handbook

In fact, Happy Holden's own contributions, which introduce HDI in the *Printed Circuits Handbook*, are not reprinted here. He suggests that both books be used in tandem for an understanding not only of HDI, but of printed circuits in general, how the basic technologies provide a background for the total board structure, and how users can rise to the challenge of implementing HDI in order to stay competitive in the market.

The on-line format of the book is also an important step toward making this book remain current and flexible, for the present and the future. HDI is a fast-moving technology and, in some respects, combines the elements of both revolutionary and evolutionary technology changes. The on-line format will allow the editor and authors to update material as appropriate, keeping it fresh, pertinent, and at the leading edge of the technology.

Integrated circuit technology will continue to drive printed circuits into ever smaller and denser packages with increasing interconnection points. As the industry progresses and new designs evolve, HDI technologies will become more and more mainstream for standard printed circuit design, fabrication, and assembly elements. Success in dealing with HDI technology and progress will be critical to success in the market place for electronic products. This book will help you get the most out of HDI and make it work for you.

Foreword



PRINTED CIRCUIT BOARD DESIGN

I/O Designer -- Uniting Disparate FPGA and PCB design flows

FPGA usage has become ubiquitous with applications spanning low power and low cost devices targeting consumer products to large 1500+ pin devices with multi-gigabit transceivers and embedded cores. Whatever the need, today's FPGA's can offer an attractive solution for a broad spectrum of applications.

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The HDI Handbook

P R E F A C E

By

Happy Holden

Once upon a time, back in 1994, Clyde Coombs was preparing to publish the 4th Edition of the *Printed Circuits Handbook*. Clyde asked me if I would write something about the new High-Density Interconnect (HDI) technology for the new edition. I wrote a chapter on “Advanced PCB Technology.” In 2000, for the 5th Edition of the *Printed Circuits Handbook*, I expanded my contribution to two chapters on HDI plus one on “Planning High-Density Boards.” Clyde called the 5th Edition “The Density Revolution” and HDI was leading the charge. By the 6th Edition in 2006, HDI was well-established and growing. However, we had to consolidate the HDI information, to conserve pages and organize the vast amount of information that filled the nearly 1,600 pages of the handbook that is a treasury of information for the PCB industry.

During the years that the *Printed Circuits Handbook* was expanding into HDI, I collaborated with Steve Gold and Ray Rasmussen at CircuiTree, where we started our adventure by publishing The Board Authority as a quarterly journal. During 1999 and 2000, my participation with The Board Authority gave me the opportunity to focus my writing on HDI and related issues. Contributors to The Board Authority’s HDI-related publications are authors in this handbook, Michael Carano (Chapters 7, 8, 9 and 10), Dr. Eric Bogatin (Chapter 4), and Dr. Christophe Vaucher (Chapter 11). Our work on The Board Authority provided Steve and me with the incentive to start planning a much more thorough look at HDI. The result is this e-Book, *The HDI Handbook*.

As an e-Book, I have many improvements planned for future revisions. Because it is electronic, and easy to revise and update,

there will be many small revisions during the upcoming year and I hope next year to add *video chapters*, along with animation, to both improve the learning environment and to add industry authorities who are very knowledgeable but may not have the time to write a chapter for this handbook.

The HDI Handbook would not exist without our contributing authors. Michael Carano has been the most involved. Michael, along with the Advanced Technology Subcommittee of the IPC Suppliers Council, has encouraged us and provided a platform for Workshops and Seminars on HDI. Other members of that Subcommittee, John Andresakis (Chapter 5) and Karen Carpenter (Chapter 2), are contributors to The HDI Handbook as well.

Finally, my fellow Mentor Graphics associates, Per Viklund (Chapter 16) and Mark Laing and Matt Wuensch (Chapter 13), contributed chapters on critical advanced topics on HDI.

All of this would not be possible without the continuing advice and council of Clyde Coombs, who has been my associate, my advisor, my mentor, and most importantly, my friend for over 38 years. I must also acknowledge another old friend and fellow PCB technologist, Joseph Fjelstad. His *Flexible Circuit Technology* book (also an e-Book from PCB007) provided me with the incentive to complete this book. Joe's insight and creativity is well known and a fitting tribute is that Figure 1 of Chapter 1 of this book is provided courtesy of Joe. I also want to acknowledge Dr. Karl Dietz, who has been a significant contributor to The HDI Handbook (Chapter 9) and to the PCB industry, and another life-long friend.

For everyone else who has contributed to this book and the body of knowledge about HDI, I thank you, especially Diane Neer, Erica Jeffrey, and Barbara Hockaday who provided the excellent editing and proof-reading we so desperately needed.

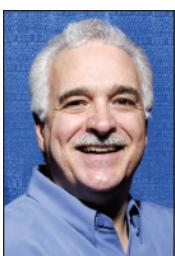
A U T H O R S



John Andresakis is vice president of strategic technology for Oak-Mitsui Technologies. He has over 28 years of experience in the manufacturing of printed circuit boards. Before Oak-Mitsui, he held management positions with Hadco Corporation (now part of Sanmina-SCI Corporation), Nelco, Digital Equipment and IBM. John has received eight US (and several foreign) patents related to PCB production.



Eric Bogatin has held senior engineering and management positions at Bell Labs, Raychem, Sun Microsystems, Ansoft and Interconnect Devices. Eric has written four books on signal integrity and interconnect design, as well as over 200 papers. A self-described "signal integrity evangelist," Eric has taught over 4,000 engineers in the last 20 years.



Michael Carano is with OMG Electronic Chemicals (formerly Electrochemicals). He has been involved in the printed wiring board industry for over 29 years. His primary focus is on metallization technologies, electroplating, solderable finishes, HDI, selective metal finishing, semiconductor packaging and imaging processes. He also looks for new ways to increase the competitiveness of the North American printed wiring board industry.



Karen A. Carpenter is the president of the marketing and technology consulting firm CMTC Associates Inc. She was the marketing manager for IBM's Interconnect Products Group and the director of marketing for Endicott Interconnect Technologies. In 21 years with IBM, she held positions in engineering, finance, strategic planning and marketing management spanning the areas of chip packaging, printed circuit boards and electronic assembly.



Karl H. Dietz is technology manager in DuPont Electronic Technologies' Semiconductor Packaging & Circuit Materials group. One of the industry's leading technologists, Karl has 41 years of experience in a variety of R&D, manufacturing and quality control functions. He has published widely on printed circuit board fabrication materials and processes, and he is active in industry organizations.

A U T H O R S



Happy Holden is the senior PCB technologist for Mentor Graphics' System Design Division. He has been involved with printed circuits since 1970. Prior to joining Mentor, Happy was the advanced technology manager at Westwood Associates and Merix Corporation. In over 28 years with Hewlett-Packard, Happy managed H-P's application organizations in Taiwan and served as head of PCB R&D, PCB engineering manager, and process engineer.



Mark Laing is the product marketing manager for Systems Manufacturing Solutions for Mentor Graphics. He has 16 years of experience in the PCB assembly and test industry. Mark holds a patent in the UK on the testing of integrated circuit devices, as well as a patent on cross-linking netlist data that has been submitted in the US. He previously worked for Marconi Instruments, GenRad, Teradyne and Router Solutions.



Christophe Vaucher has spent 20 years in the PCB industry, dealing with electrical test in particular. He has been recognized through many works, patents, articles, papers, workshops, and awards. In the late 1990s, Chris launched and led the Bare Board Test work group. He is the founder of Beamind, a company that introduced laser direct testing (LDT), a non-contact electrical test technology dedicated to testing HDI substrates.



Per Viklund is director of IC packaging & RF at Mentor Graphics, responsible for IC packaging, RF design and embedded components product lines. He is a longtime IEEE & IMAPS member with close to 30 years' experience with electronic design, and he's spent the last 20 years with development of advanced EDA tools. Per has published numerous papers on IC packaging, embedded passives, RF and high-speed design.



Matt Wuensch is business development manager, Mentor Graphics Corporation Systems Manufacturing Solutions. With over 14 years of experience working in a PCB manufacturing company and 10 years as a supplier to PCB manufacturers, Matt has a unique perspective that enables him to effectively understand customers' needs. His previous employers include Motorola, GenRad, Tecnomatix-Unicam and Router Solutions.

1

Introduction to High-Density Interconnects

By Happy Holden — *Mentor Graphics*

The Evolution of Electronics

Electronics is a relatively new industry, only about 60 years old now. From its beginning in WWII, with communications, radar, and ammunition fusing (especially the radar-altimeter electronic fusing for the first atom bomb), electronics has evolved into the world's largest industry. All electronic components must be interconnected and assembled to form a functioning unit. The design and manufacture of these interconnections have evolved into a separate discipline called electronic packaging. Since the early 1940s, the basic building block of electronic packaging has been the printed wiring board (PWB). This book outlines the advanced design approaches and manufacturing processes needed to produce the most complex of these PWBs, the high-density interconnects (HDI).

This chapter introduces the basic considerations, main advantages, and potential obstacles that must be accounted for in the selection of high-density interconnection methods for electronic systems. Its main emphasis is on the analysis of wiring and component density and the potential effects that the selection of various HDI board types and design alternatives could have on the cost and performance of the complete electronic assembly.

Introduction to High-Density Interconnects

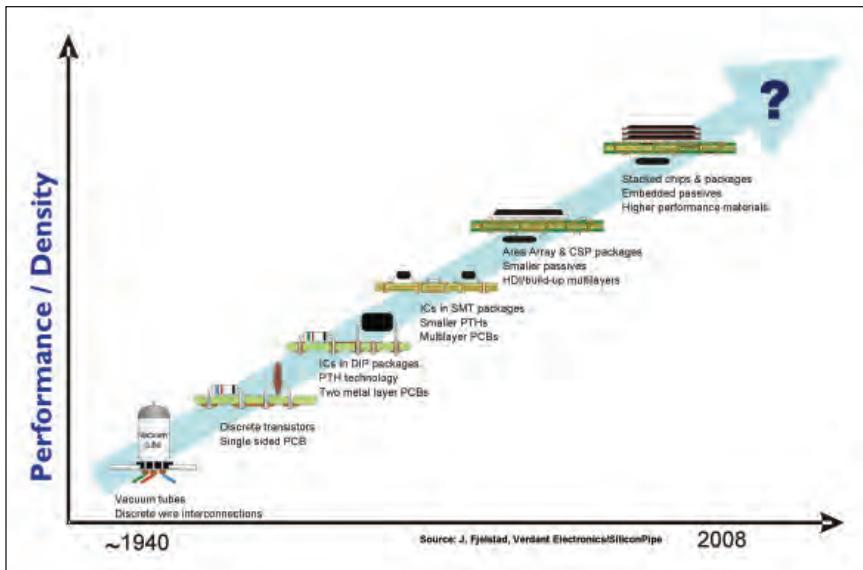


FIGURE 1: Electronics have evolved in density from the 1940s, when first used, to the current state of high-density interconnects that include 3D stacking and embedded components. (Source: Joe Fjelstad, Silicon Pipe)

The continuing increase in component performance and lead density, along with the reduction in package sizes, have required that PWB technology find corresponding ways to increase the interconnection density of the substrate. With the introduction and continued refinement of such packaging techniques as the ball grid array (BGA), chip-scale packaging (CSP), chip-on-board (COB), and system-in-package (SiP), traditional PWB technology has approached a point where alternative ways of providing high-density interconnection have had to be developed. This book will define HDI in detail and provide insights into the design, electrical performance, materials, fabrication processes, inspection/testing, and assembly of these complex structures, as illustrated in Figure 1.

Interconnect Trends

The interconnect trends discussed in this book will be those at the high end of PWB technology—the HDI or build-up multilayers (BUM) which are driven by silicon technology. The impact of the semiconductor trend is in the forms of electronics packaging and interconnect technologies. This effect directly influences IC packaging via die interconnect and PWB HDI technologies.

Electronic Packaging and Interconnection

The technology migration to support higher electronic packaging and interconnection is made up of integrated circuit (IC) packages and printed wiring boards.

Integrated Circuit Packages

IC packages have four major forms:

- Peripheral leaded packages
- Plastic and ceramic ball grid array packages
- Flip-chip BGA packages
- Wire bond and flip-chip chip-scale packages

Printed Wiring Boards

PWBs have four main forms:

- Single- and double-sided
- Multilayer
- Flexible circuits
- Build-up multilayers

IC Technology Trends

Integrated circuit technology has been the driving force in electronics since the early '60s. The trends in IC technology are:

- Shrinking gate size - down to the current 45 nm
- Die size reduction - the opportunity for “die shrink”

Introduction to High-Density Interconnects

- Voltage reduction - the need to control power dissipation
- Higher gate integration - currently, over 1 billion transistors can be on a die
- Faster signal rise times - higher frequencies and clock rates

As seen in Figure 2, these trends lead to other effects in packaging and PWBS, most notably, more complex BGAs.

- Faster rise times → Smaller packages → Finer pitch
- Higher gate integration → Higher I/O → Finer pitch
- Higher gate integration → Higher current → More PWR/GND pins → Finer pitch
- Faster signal rise times & lower voltages → Narrowing noise margins → Smaller packages → Finer pitch
- Faster rise times → Sensitivity to Inductance and Capacitance → Thinner packages → Lower Dk → Shorter signal paths → Smaller packages
- Lower Costs → Smaller Packages

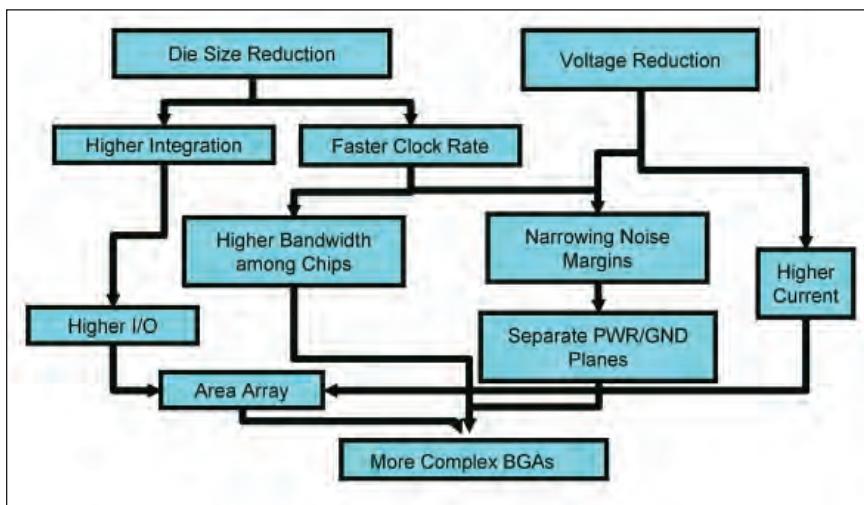


FIGURE 2: IC technology trends, which permit higher functionality and lower cost, also drive higher I/O with more noise sensitivity and the need for more complex BGA packaging.

- Sensitivity to Inductance & Capacitance →
Elimination of pins and balls → Fine-pitch LGAs
- Faster signal rise times → More GND pins → More
I/Os → Finer pitch
- Higher I/O & Finer pitch → Area array packages

Integrated Circuit Packages

Integrated circuit packaging, system-in-package and multi-chip modules will be covered in more detail in Chapter 16 of this book. As a result of the technology trends in IC technology, IC packaging has moved from low-count peripheral leadframe to more complex area-array packages of higher I/Os and finer-pitch. This change can be seen in Figure 3.

The IC chip feature sizes and bonding pads have been constantly reduced in size, as shown in Figure 4. The resulting packages are 1.0 mm pitch, 0.8 mm pitch, 0.65 mm pitch and even 0.4 and 0.5 mm pitches. Many of these packages are now

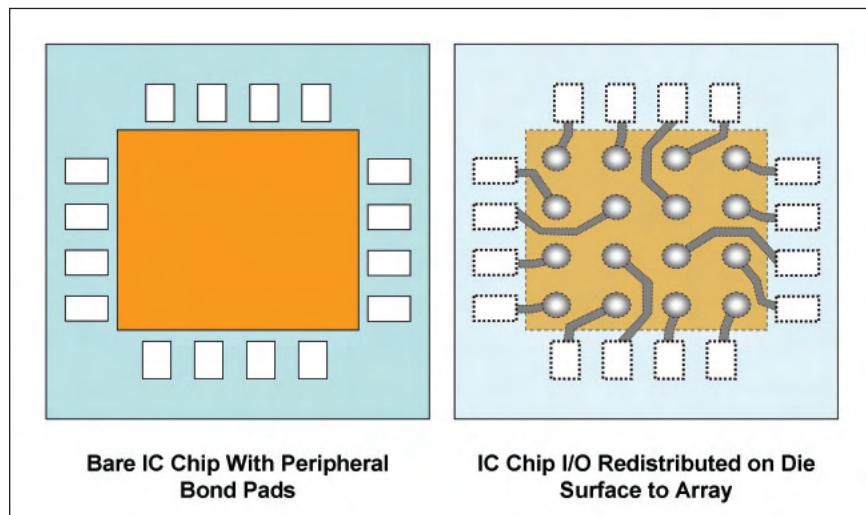


FIGURE 3: A bare IC chip with peripheral bond pads is now converted to an array by redistributing the connections on the substrate.

Introduction to High-Density Interconnects

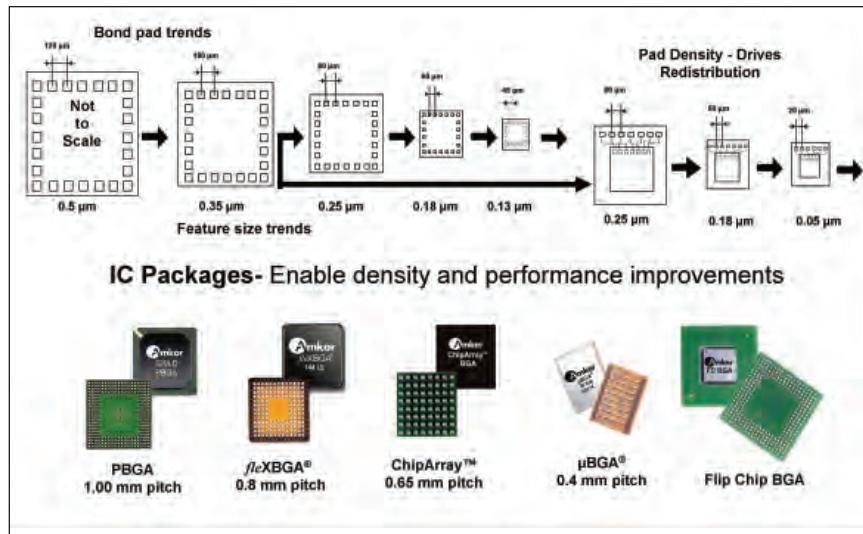


FIGURE 4: IC feature size reduction enables chip-size and bonding-pad pitch reduction. Resulting plastic packages can have high I/O as well as fine-pitch down to 0.4 mm.

flip-chip area-arrays instead of peripheral wire-bonding pad geometries.

PWB and Interposer Wiring Roadmap

A way to look at IC packaging design rules is shown in Figure 5, the packaging feature roadmap. The pitch of various packages, from 1.27 mm to 0.08 mm, is broken out by the design rules required to connect them up on a PWB. The largest pitches are ball grid arrays (BGA) to 0.8 mm. Then, from 0.65 mm to 0.25 mm, they are chip-scale packages (CSP). Below 0.25 mm is the region of direct chip attachment (DCA).

The Classic Multilayer

The classic multilayer is now over 40 years old. The design rules are different, but not by much! If you look at the 1968 16-layer multilayer that Hewlett-Packard used in its now historic HP-9100 desktop programmable computer (Figure

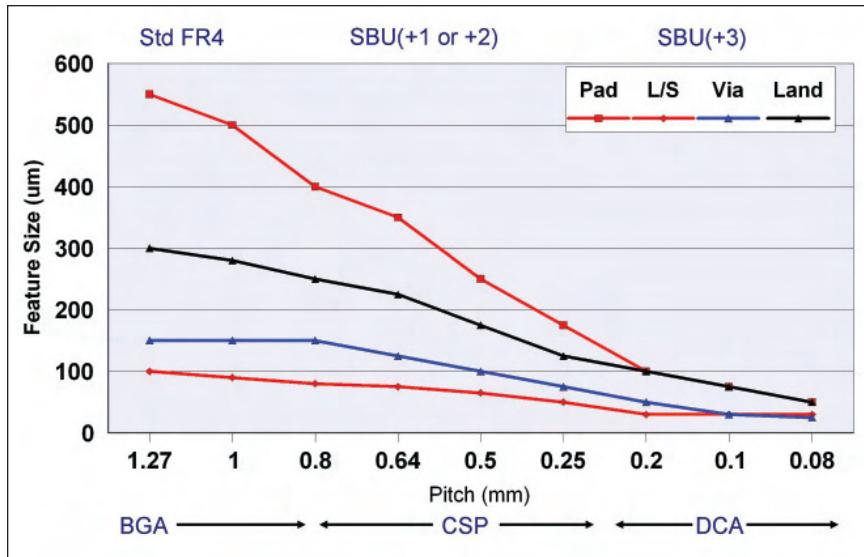


FIGURE 5: IC packaging feature roadmap with via size, via-pad size, lines and spaces (L/S), and SMT land size.

6), the ROM for that computer was created from a 16-layer FR-4 multilayer with sheets of PTFE introduced between the prepreg layers. The 0.150 mm traces and spaces were etched to create 1s and 0s that high-speed pulses could read through coupling, thus creating the 512 64-bit words of the basic operating system. The 100-step programs and variables were



FIGURE 6: Hewlett-Packard 9100A Desktop computer (introduced in 1968) and the 32,768-bit ROM PWB made of a 16-layer FR-4 multilayer with PTFE added to improve magnetic coupling of the inner-layers 1s and 0s, as seen in the center photo.[1]

Introduction to High-Density Interconnects

stored in ferrite memory. This invention moved the computer from million-dollar, air-conditioned office behemoths to “everyman’s” desktop. The ROM PWB was required because ICs of that day had only 12 gates per chip—nowhere near the 32,768 bits (131,072 gates) needed for the operating system ROM. Contrast this to just three years later, 1971, when Hewlett-Packard reduced the desktop to a pocket-sized handheld calculator, the HP-35. This started the modern age of portable electronics.[1]

Problems with Multilayers

Multilayer is a stagnant PWB design flow for the following reasons:

- Technology hasn't changed in 40 years
- Still signal, power, and ground
- Traces, spaces, and holes are smaller, but not by much
- FR-4 is still the major dielectric
- Current and future IC technologies are sensitive to multilayer TH capacitance and inductance
- High-performance, volume, cost-sensitive market segments (Consumer, Telecom, Automotive) have left classic multilayers for HDI-enabled technologies
- Pac Rim fabricators have 10 years' experience pushing the HDI/embedded envelope
- Component vendors' (especially IC) new products depend on HDI
- Decreased functionality and higher costs compared to HDI

North America is still the largest user of classic multilayers over 16 layers, as shown in Figure 7. Asia has tempered that

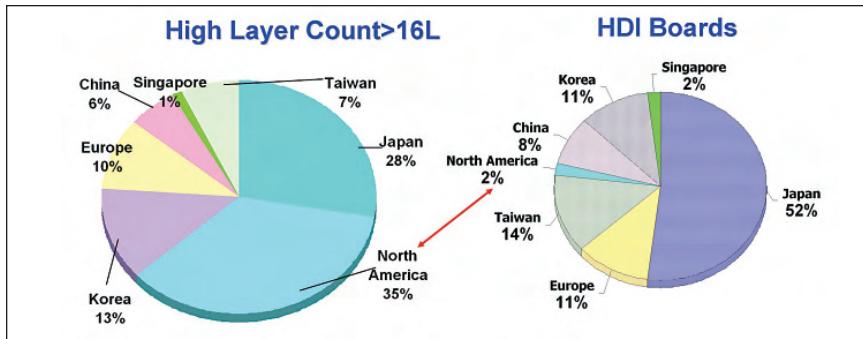


FIGURE 7: High layer count (>16 layers) worldwide usage compared to worldwide usage of HDI PWBs.[2]

use of classical multilayers with the use of HDI PWBs.

HDI Multilayer Platforms

HDI is such a large and growing PWB application market that it is made up of at least four different HDI platforms: (1) Substrates and Interposers; (2) Modules; (3) Portables; and (4) *High* performance. Chapter 2 will provide more detail about the HDI market.

Substrate and Interposer technology is used for flip-chip or wire-bondable substrates. Microvias offer the escape for very dense flip-chip area arrays. Dielectric is new-engineered films. A typical example is seen in Figure 8. Chapter 16 will discuss these substrates in more detail



FIGURE 8: Flip-chip substrate for a memory BGA.

Introduction to High-Density Interconnects

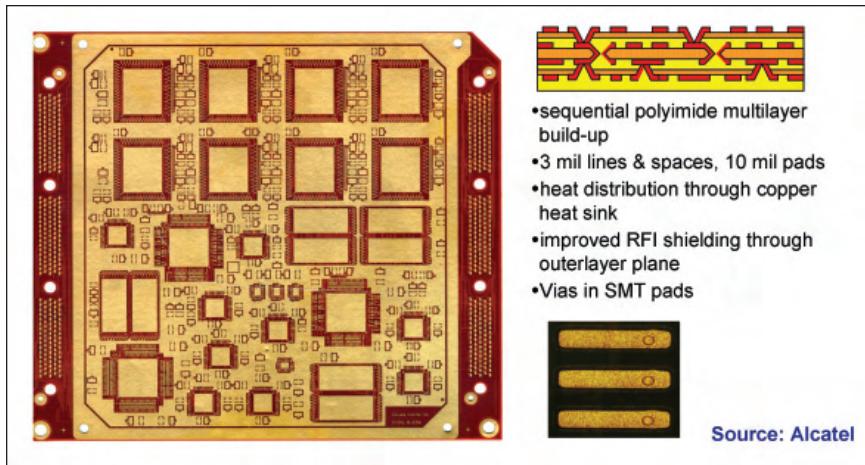


FIGURE 9: High-performance system module for the base-station for video encryption for portable G3 phones.

Modules are small substrates that may have their ICs wire bonded, flip-chipped, or TAB mounted or may use fine-pitch CSPs. The discrete components are typically very small, such as 0201s or 0101s, and may even be embedded. The design rules are usually coarser than the single IC substrate, since the module may be larger than a single IC package. A typical example is seen in Figure 9. Chapter 16 will discuss these modules in more detail.

Portables and miniaturized consumer products are the leading edge in HDI technology. Their dense designs offer small form factors and very dense features including microBGA and flip-chip footprints. Typical products are seen in Figures 10 and 11.

High-performance technology is used for high-layer-count boards with high I/O or small pitch components. A buried via board is not always necessary. The microvias are used to form the escape area of dense components (high I/O, micro BGA). Dielectric is reinforced resin-coated foil, reinforced prepregs and cores and high-performance laminates. A typical example



FIGURE 10: A Sony 1996 DCR-PC7 micro-camcorder using 2+4+2 HDI technology (IPC Type III) and a more recent 2004 Panasonic AV-100 micro-camcorder.

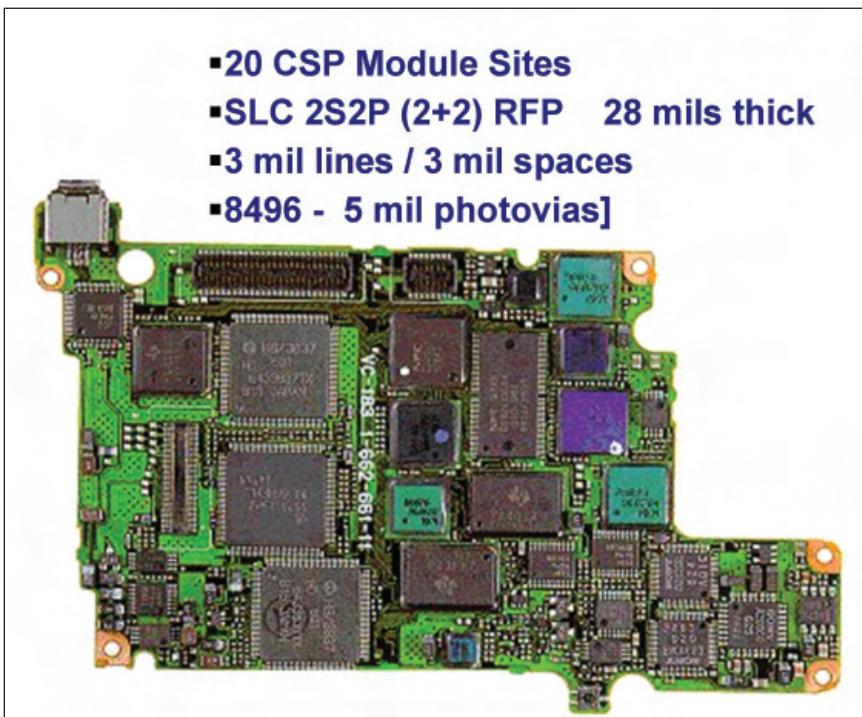


FIGURE 11: One of two HDI boards used in the 1996 Sony DCR-PC7 micro-camcorder. 20 CSPs (of 0.5 mm pitch) were employed on both sides of the assembly.

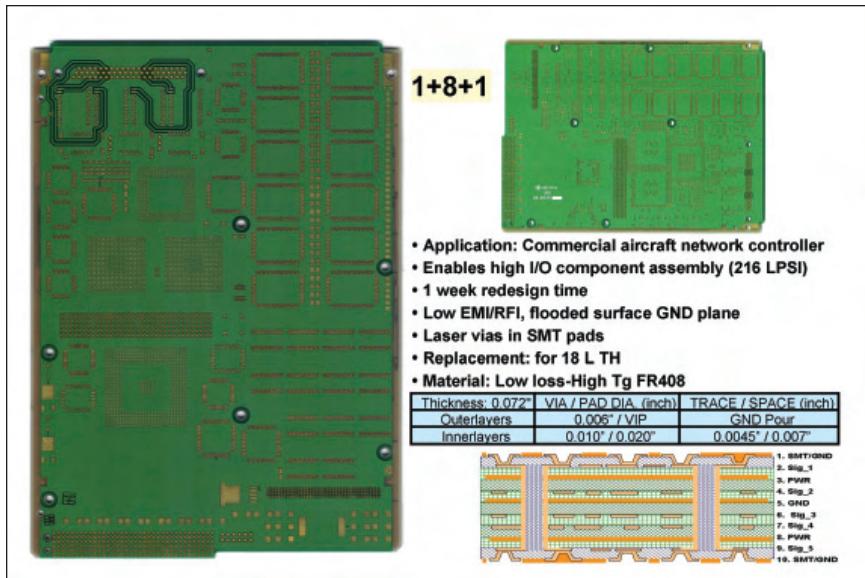


FIGURE 12: A high reliability avionics board for a triple OC-192 (10 Gb/s) optical network controller. Construction is of low-loss laminates and uses a 1+8+1 HDI structure (IPC Type II).

is seen in Figure 12.

A possible fifth HDI platform is for embedded components, either planar or discrete. Figure 13 shows a simple example of how HDI is used to connect embedded components. Chapter 14 will discuss embedded components in more detail.

HDI Opportunities and Drivers

The advantage of higher density and electrical performance comes home when creating a new product! System optimization, as seen in Figure 14, can balance the trade-offs of gains and losses in various technologies while meeting critical schedules, achieving projected performance, and managing costs so that the product will be successful.

These five technologies: Circuits, Components, Materials, Design and Manufacturing processes, as well as many others not mentioned here, are the *Measures of Excellence*.

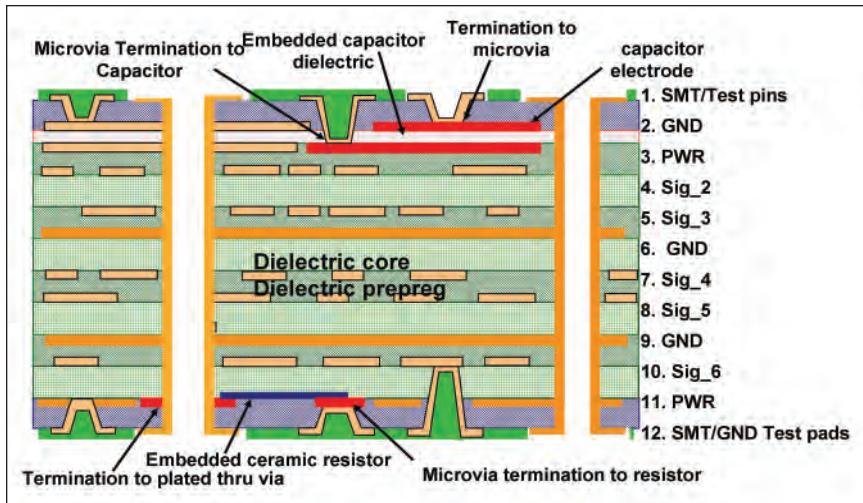


FIGURE 13: The typical usage of microvias to connect various embedded capacitors and resistors.

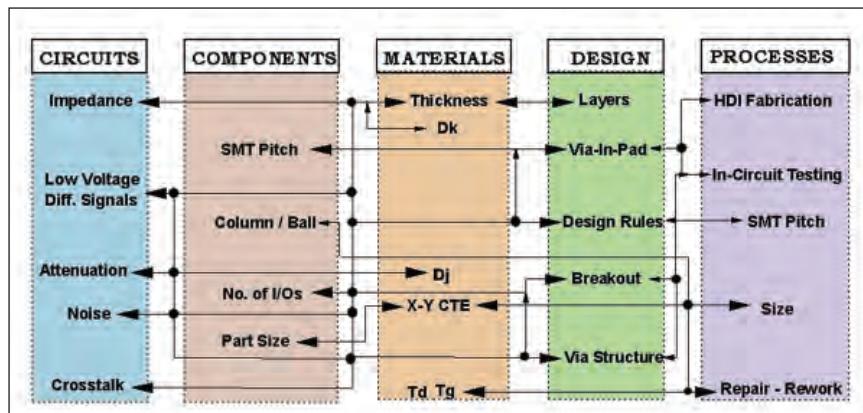


FIGURE 14: This greatly simplified diagram shows the interdependency of critical variables for these five technologies (Circuits/Signal Integrity, Components, PCD Materials, PCB Design, Manufacturing Processes).

Performance Improvements

When performance improvements are required for PWBs, HDI is the leading contributor. In addition to making the PWBs smaller, lighter, and thinner, HDI will give them superior electrical performance. Some of the performance improvements are:

Introduction to High-Density Interconnects

- Lower order of magnitude via electrical parasitic
- Minimal stubs
- Stable voltage rail
- Removal of decoupling capacitors
- Lower crosstalk and noise
- Much lower RFI/EMI
- Closer ground planes
- Closer distributed capacitance
- Surface ground planes with via-in-pads cut emissions

Related to IC technology and smaller gate geometries is the increasing speed of signals which manifests itself not just in higher-frequency applications, but also in shrinking signal rise times. Another result is higher heat dissipation and a consequential reduction in power supply voltage. All of these conspire to increase the sensitivity of circuits to various forms of noise and loss of signal strength. Newer high-performance materials, with higher thermal resistance (for lead-free soldering) are being invented to solve these problems. Additionally, improved processes for microvias improve high-frequency performance.

An HDI test vehicle is an ideal platform to test electrical performance and signal integrity structure stack-ups before they are used on a product. Microvias have nearly one-tenth the parasitics of THs. These structures can validate the lower inductance in microvias and, when combined with low-inductance decoupling capacitors and via-in-pads, show the merits of noise reduction in high-speed but reduced-voltage designs. Other simulations and test vehicles have already proven the advantage of HDI at higher frequencies. Figure 15a shows the simulation from AnSoft of the typical 0.33 mm (0.013" FHS) TH in 1.6 mm thick (0.062") FR-4. Figure 15b is

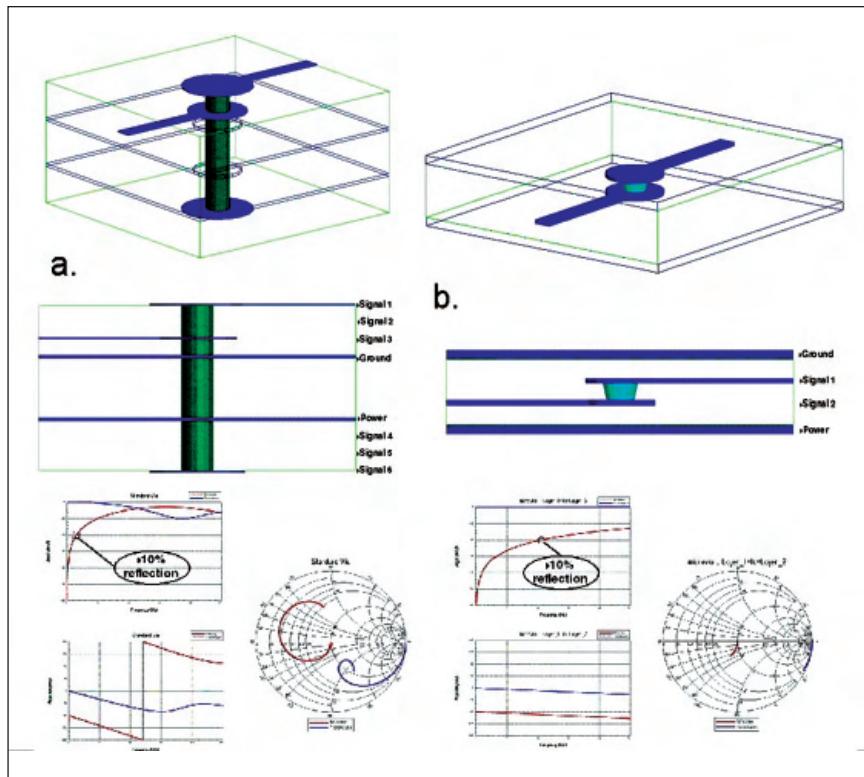


FIGURE 15: Simulation of the difference in the performance of through-hole vias (15a) compared to microvias (15b) (AnSoft Technical Roadshow-2001)[3]

the same simulation, using a 0.15 mm (0.006") microvia, 0.100 mm deep (0.004"), where the microvia has fewer reflections and a much larger frequency tolerance than does the TH.

The lower inductance of a microvia (~30pH) is useful when coupling to power and ground, especially above 1.5 GHz, for decoupling capacitors. A typical TH will have an inductance of at least 2-3 nH, and this inductance will inhibit the performance of decoupling capacitors in the GHz range as seen in Figure 15.[3]

Access to Advanced Components

The semiconductor industry is the primary driver for

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electronics. Smaller gate geometries and greater total gates allow more functions to be performed at a faster rate. With larger wafers, the prices continue to tumble. This allows and inspires more products that grow the entire industry. We (the U.S.) are still the drivers of advanced semiconductor technologies. Much of the foreign construction of wafer fabs has focused on commodity memory and glue chips. IBM, Intel, Motorola, AMD, Sun, H-P, and Texas Instruments, to name just a few, are continuing to lead the IC industry worldwide.

IC packaging, say a 1.0 mm pitch device, benefits from PCB technologies like HDI, but the use of 0.8 mm pitch devices is where HDI really begins to provide advantages. The blind vias save room on inner-layers and have reduced via lands, and make via-in-pads possible. Typical of these devices is the 296 pin, 0.65mm pitch, Digital Signal Processor (DSP) (Figure 16a) or the 257 pin DSP shown in (Figure 16b). Other new components becoming more widespread are ones with very high pin counts of around 600 to 2500, even at 1.27 and 1.0 mm pitches. Although some of these are telecom digital switches (Figure 16c), the vast majority are the new field programmable gate arrays (FPGAs). Current products from Actel, Infineon, Xilinx, and Altera have packages with 256, 348, 396, 456, 564, 692, 804, 860, 996, 1020, 1164, 1296, 1303, 1417, 1508, 1696 and 1764 pins (see Figure 17).

Faster Time-to-Market

Faster time-to-market is the result of easier placement of components using blind vias or via-in-pads. Other design efficiencies come about because of smaller spacing, improved BGA breakouts, boulevards routing (see Chapter 3), and ease of auto-routing using blind/buried vias over TH vias. The overall system design times can be reduced because of the improved

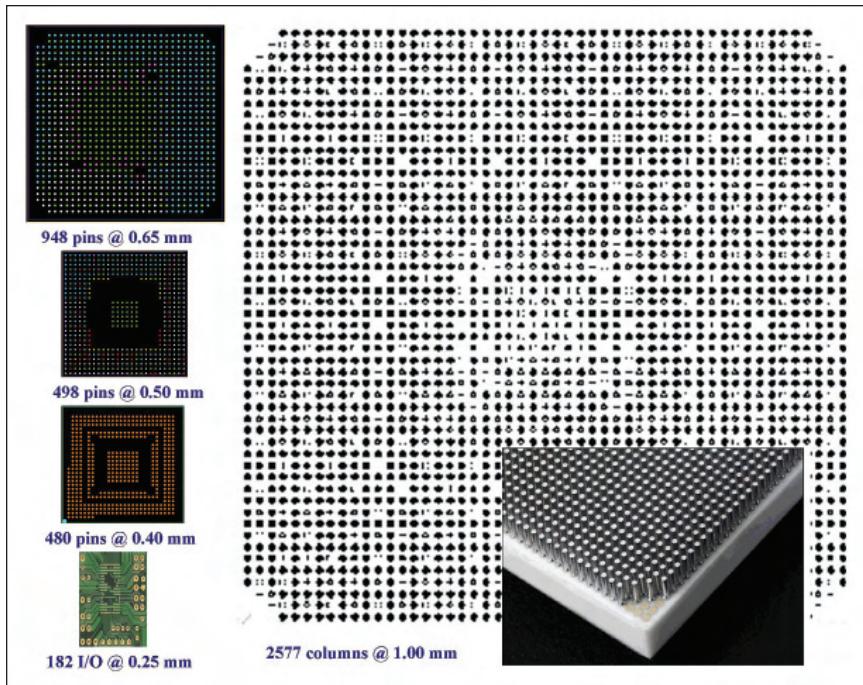


FIGURE 16: Fine-pitch devices such as this 948 pin - 0.65 mm pitch microprocessor, the 498 pin - 0.5mm DSP device or the 480 pin - 0.4 mm controller, even the 182 pin - 0.25 mm require microvias. The 2577 pin - 1.0 mm pitch digital switch now requires microvias in order to connect them on a printed circuit.

electrical performance of blind vias instead of TH vias and the fewer respins required because of signal integrity and noise reduction (see Chapter 4).

Improved Reliability

Extensive reliability testing was performed by the IPC-ITRI in the late 1990s about the reliability of microvias.[4] Other groups (like HDPUG & JPL) have also produced reports on the superior reliability of small-blind vias over TH vias. [5] Understanding why is quite simple! The via aspect ratio (AR-depth to diameter ratio) is less than (<) 1:1 compared to TH which has an AR of >6:1 that goes as high as 20:1. This

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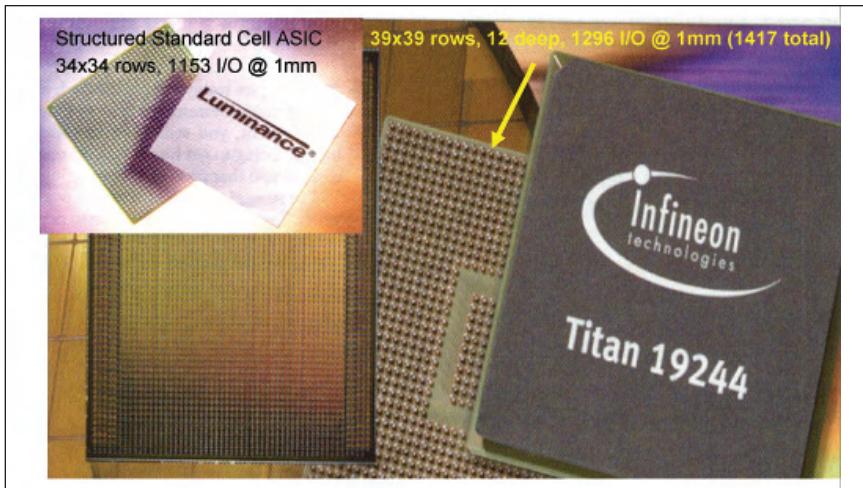


FIGURE 17: FPGAs have increased in popularity and usage, as well in number of pins. Wiring any one of these two FPGAs of 34 by 34 rows or 39 by 39 rows of pins using through-holes (TH) will require more than 20 layers in a multilayer but only 12 layers if using HDI (see Chapter 3).

is a result of the thin materials and low Z-Axis TCE materials used in HDI (see Chapter 5). HDI materials are numerous and exceed multilayer laminate in variety, thus they are covered by the IPC Standard IPC-4104A and not IPC-4101B. If the blind vias are properly drilled and plated, they will perform with many times the thermal cycle life of typical THs (see Chapters 7, 8, 10 and 12).

Thin HDI materials are thus suited for thermal heat transfer as covered in the IPC HDI Design Standards, IPC-2226.

Lower Cost

Chapter 3 will discuss in detail the improved design process for HDI PWBs. Properly planned and executed, an HDI multilayer can be less expensive than the TH board alternative as illustrated in Figure 18, comparing the benchmark of a high-speed, controlled impedance 12-layer TH multilayer to an 8-layer HDI multilayer. By fully utilizing the Secondary Side

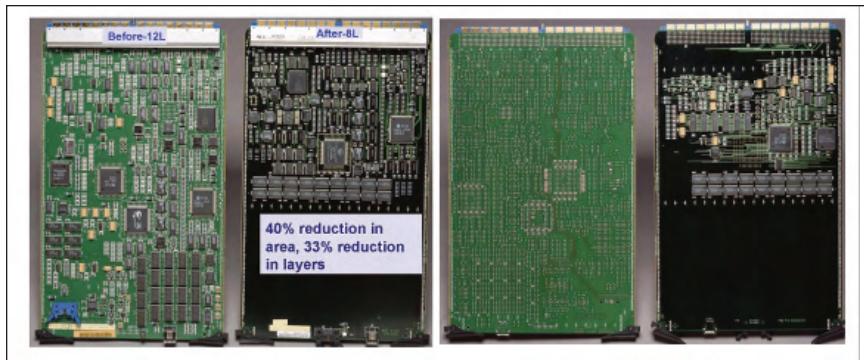


FIGURE 18: The Benchmark redesign of the 12-layer TH controlled impedance multilayer on the left results in the 8-layer HDI multilayer on the RIGHT. In addition, 40% less space is required with the HDI board due to the microvia-in-pads.

of the PWB, 40% less area was required to connect all of the components, in addition to four fewer layers.

The Obstacles in HDI implementation

Historically, there have been a number of obstacles in implementing HDI. These obstacles form implied risks to using the technology. One of the major goals of this HDI Book is to eliminate those obstacles and risks, such as:

Predictability

Customers need to know the HDI stack-up, DRs, and price, *before* starting the project or design.

Fabricators will often quote the design *after* it is designed, but without the numbers up front, no one can afford the time to run down a blind alley. The concept that microvias cost more is based on a lack of knowledge of how to *properly design an HDI board*.

Design Models

We have accurate wiring models that can take basic component data, schematic info and board size to create a

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stack-up and design rules. Very few fabricators have learned the technology of simulating a finished PWB!

CAD Tools

Few fabricators have designed an HDI board, so they are unaware of the changes and new procedures required for their CAD tools. Stack-up, architectures, channel routing, and boulevard routing are new developments in design that most designers have not heard of, so they don't know where to start!

Signal Integrity

Users are not aware of the electrical performance improvements that HDI can offer or the problems THs are creating.

Volume Production

Most volume HDI fabricators focus on cell phone and consumer products. Many fabricators need to focus on low-volume HDI needs as well.

New Materials

HDI has introduced new materials that users are very unfamiliar with (RCF, liquids, and vacuum-laminated films).

Assembly Issues

Many assembly people have never seen via-in-pad (VIP) or (VIL) before and think they will steal solder-paste from the joint. They won't. Volume is less than 1% of the solder paste brick. Forcing VIP to be 'filled & flush' needlessly adds 8%-15% to the price. Putting the dogbone back in an HDI board takes up area and adds a great deal of inductance to the circuit (~25 nH per inch).

Assembly Test

Using VIP and blind vias, there are no THs on the back side to use as test points. Density is so high that there is no room for large 0.050" pads as test points. Reduced test point accessibility is a new concept that many have not adjusted to yet.

This book will tackle all eight issues and present the education and solutions to these implied risks.

Predictability or ‘What Will It Cost?’— the Need For Design Models

I have been working with HDI boards since 1983, when Hewlett-Packard built its first microvia multilayer prototype, the Finstrate. It took many years before we learned how to design with the technology efficiently due to all the different options in stack-up, via structure, and design rules that could be employed. We finally developed a predictive methodology that allowed us to plan the design and select the best stack-up and HDI architecture (Figure 19). The details of this methodology can be found in chapter 19 of the sixth edition of Clyde Coomb's *Printed Circuits Handbook* from McGraw-Hill.[6]

Software to execute this “HDI Planning Methodology” has been developed four times. The first was MCC’s Multichip Design Advisor-MDA which spun off Savansys which eventually created Savantage. Neither organization exists today. Hewlett-Packard Laboratories created the “PCB Design Advisor-PDA” and then “Explorer” to optimize the choices and constraints of the PDA. Finally, I created my own “PCB Advisor” that I have used for many years for HDI consulting (Figure 20).

One of the outcomes of this simulation, as well as many Benchmarking activities (Figure 18), was the TH versus HDI Trade-Off chart seen in Figure 21. In the Price/Density

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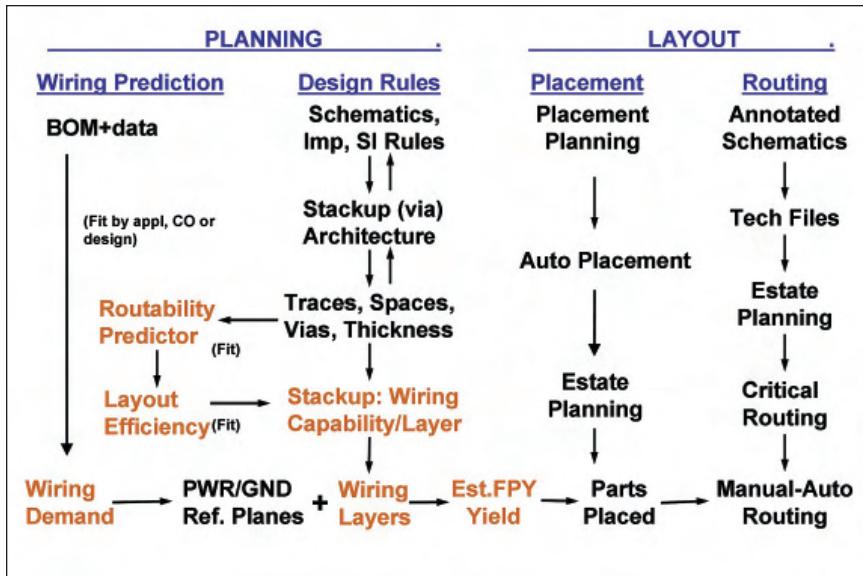


FIGURE 19: HDI Predictive methodology is used before the actual physical design in order to select the appropriate layer stack-up, via architecture, and design rules. Only the schematic, BOM, and estimated design rules are required.

Comparison, the two key variables are RCI (a comparison currency normalized to the actual price of an 8-layer multilayer) and DEN (the average number of pins on a board divided by the length and width of the board).

The RCIs in the matrix are the floor numbers (minimums). But the ceiling numbers for a range are not within our ability to calculate or set up at this time. The maximums are practically limitless, depending on various factors in the design. Yields are very sensitive to minimum diameter, annular rings, minimum trace and spacing, material thicknesses, total number of holes, and their density. Other cost factors, such as final finish, hole filling, and tolerances will affect the price. I have added a column for “Density” (DEN). This is the Maximum Number of Electrical Connections (called ‘pins’) per square inch of surface (for both sides). The dashed lines are equivalent PCBs. So, as an example, an 18-Layer TH (through-

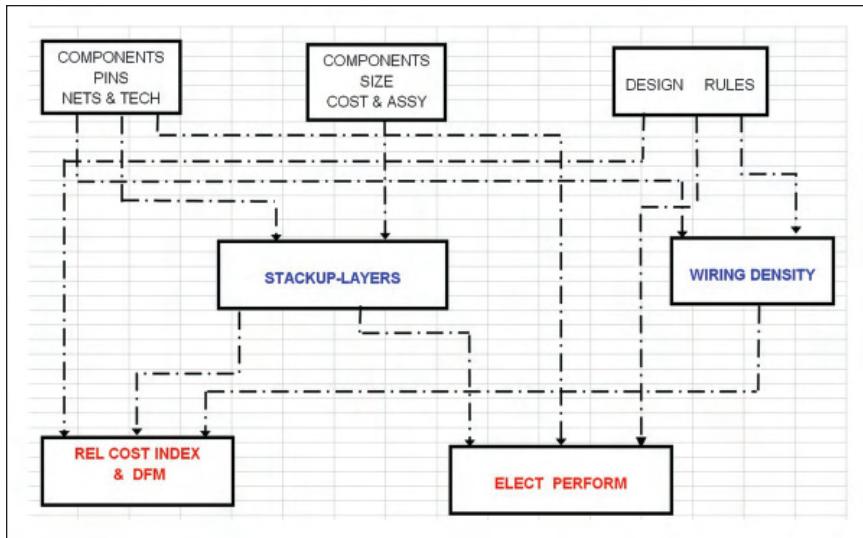


FIGURE 20: PCB Advisor Flow, a simulation system consisting of 35 Excel spreadsheets all driven by 200+ system variable interlocked by macros. The object was to select the optimum stack-up, via structure, and design rules while not exceeding any boundary conditions of cost, performance or producibility.

hole-Column A) board with an average of 100 pins per square inch (p/si) could have been designed as a 10-layer HDI board (1+8+1-Column C) because it can handle 210 p/si. Or, it could have been designed as a 6-layer HDI board with 2+2+2 (Column E, also 200 p/si).

The RCI does not show the absolute cost savings in this example. The relative cost savings is 28.1% for the 10-layer and 20.5% for the 6-layer HDI equivalents. A smaller board could result in more boards per panel and the price would be even lower than the above numbers. In the range of 8L to 18L, the HDI boards, especially the 2+N+2 are *not* the equivalent of 8L to 18L TH boards. They represent boards with *12 to 20 times* the density of TH boards. Even the 1+N+1 HDI boards represent TH boards with 14L to 30L layers!

This matrix, which is based on FR-4, has two important implications. The TH RCI scale (4L – 16L) represents

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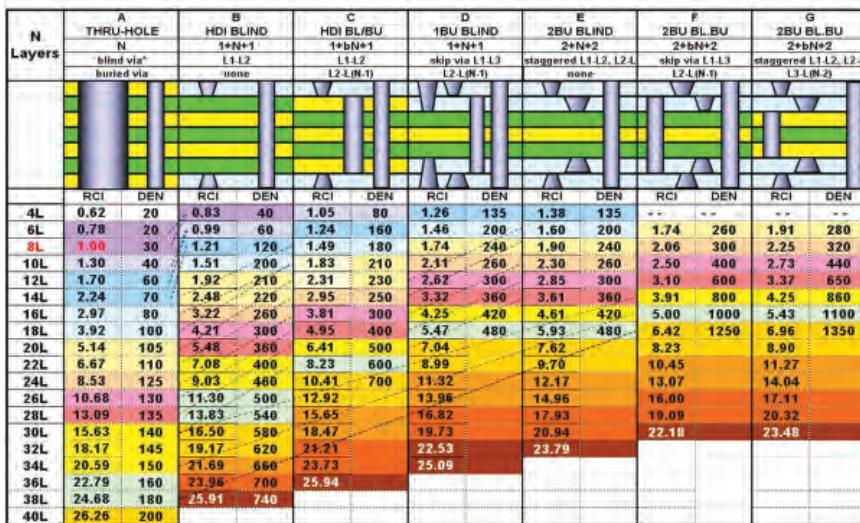


FIGURE 21: TH versus HDI Price/Density Comparison. The Relative Cost Index (RCI) and Density predictor (p/si) provides a quick comparison of TH layers (Column A) to equivalent HDI structures (Columns B – G).

competitive pricing set by China. This scale is depressed compared to the HDI pricing. So the HDI pricing, if equal or lower, *is very competitive*. If the material of construction is *not FR-4*, but a more expensive, low Dk or low Dj material, then the savings from HDI will be *much larger* as you reduce layers!

Design Tools - CAD

EDA tools for HDI have been slow in coming. Fortunately, they are available today and continue to improve. Important differences and additions that are required from conventional TH EDA tools (Figure 22) are:

- Blind and microvia structures of staggered (adjacent), stacked (coincident) and inset structures
- Any layer and layer-pair stack-up structures
- Blind/buried via spacings
- Component breakout and breakthrough for via-in-pad
- Any angle routing

- BGA fanout automation
- Dynamic via and component trace entry
- Via push and shove
- Auto-routers optimized for blind/buried vias
- Links to electrical, thermal, and FPGA simulation tools
- DRCs for HDI structures
- Localized rules under components

More details about EDA tools will be discussed in Chapter 3 - HDI Design, as seen in Figure 22. How complex BGAs are fanned out and broken out to create boulevards for improved routing is an important part of that chapter.

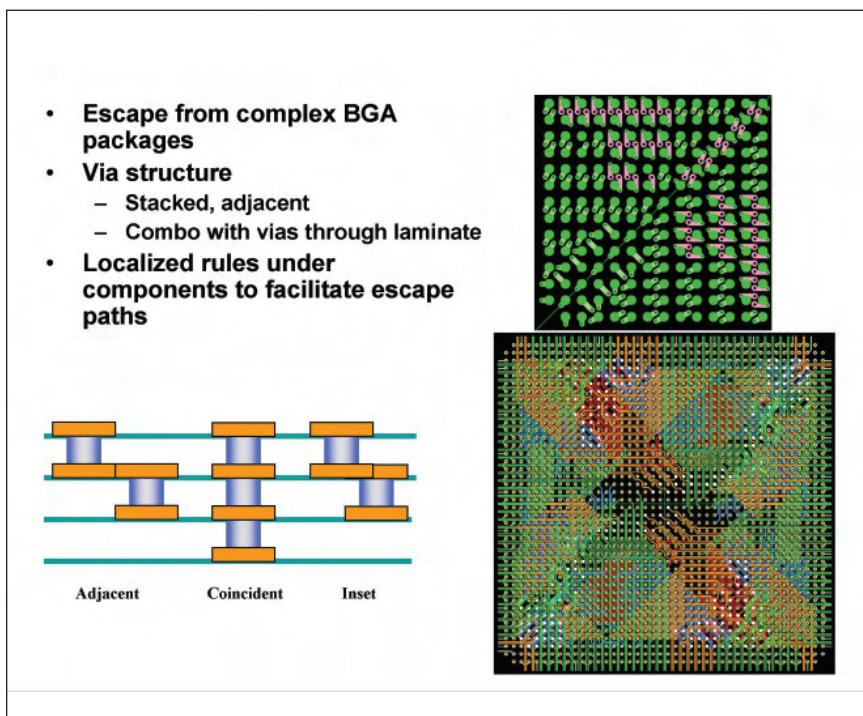


FIGURE 22: High-Density Design Tools, things to consider, especially the breakout and fanout strategy for large, complex BGAs.

Electrical Performance and Signal Integrity

Tightly linked signal integrity, power integrity tools, and HDI layout tools provide insight into the superior electrical performance of HDI structures. With the faster rise-times of modern ICs, board parasitics that we used to ignore are now very important.

These board parasitics are shown in Figure 23 and include: power and ground plane capacitance and inductance, package capacitance and inductance, Circuit Board A connector capacitance and inductance, backplane or cabling capacitance and inductance to board B, and how Circuit Board B's connector and board capacitance and inductance, power and ground plane capacitance, and inductance are structured. This will be discussed in Chapter 4, as well as the influence of vias in electrical performance.

The electrical influence of vias in high-speed nets cannot be overlooked. THs have parasitic capacitance and inductance and can be a significant factor in signal performance. The lumped model of a TH has nearly 10X the parasitic value of a microvia (Figure 24).

Fortunately, signal integrity and power integrity EDA tools

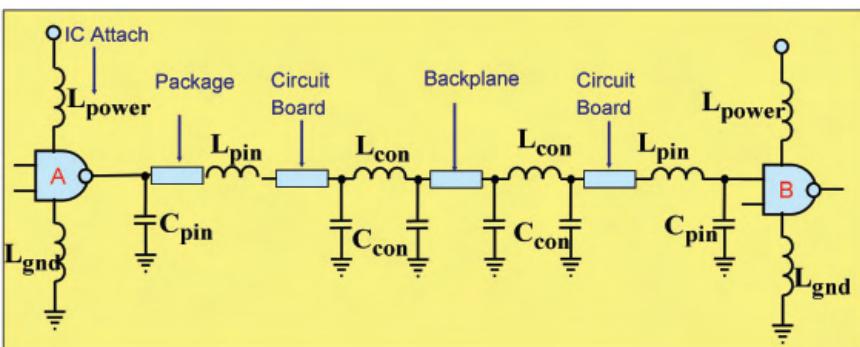


FIGURE 23: Critical electrical path from Driver-to-Receiver, including packaging parasitics that now must be included.

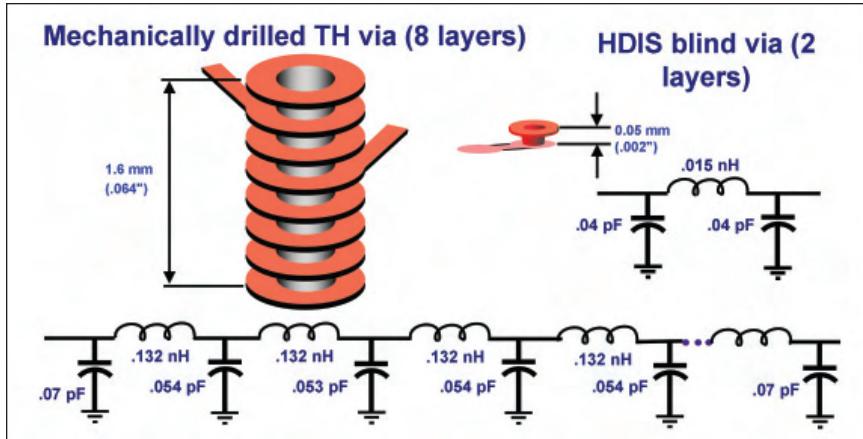


FIGURE 24: Comparison of the electrical performance of TH and microvia-lumped models

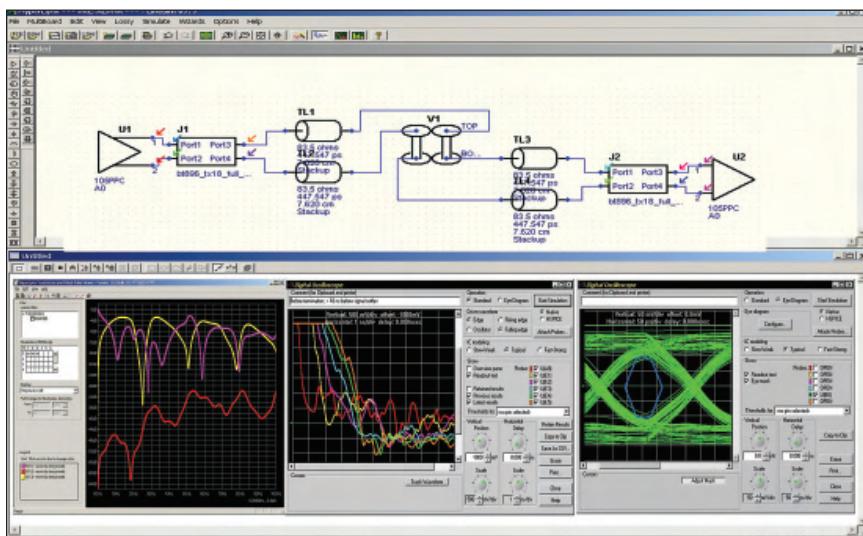


FIGURE 25: Electrical performance and signal integrity simulation of differential microvias. Displays are signal and impedance, losses, and an eye diagram. (Source: Mentor Graphics' HyperLynx)

are available (Figure 25) which makes it possible to quantify the contribution HDI has on electrical performance.

Fabricator Capability

As of 2008, the roster of North American PWB fabricators

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includes 135 that will produce HDI multilayer, as disclosed by the FAB FILE [7]. Further analysis of that database shows that only 95 actually own their own laser drill. Creating and maintaining HDI processes is notoriously expensive and requires a great deal of engineering experimentation and control. Later chapters deal directly with the “how-to” of HDI fabrication.

The IPC has created a number of new “Hands-On” Programs, in partnership with the U.S. Navy’s CRANE NWS high-technology PWB/HDI facility in Crane, Indiana.[www.ipc.org]

New Material

Laminates are increasingly important to high-performance PWBs. Low loss laminates as well as low dielectric constants (or consistent dielectric constants) are both critical. Higher heat resistance is needed for lead-free assembly processes. The new feature that laminates need is a higher Decomposition Temperature (called Td). This is the temperature that a laminate can withstand when it has lost 5% of its weight by thermal gravimetric analysis (TGA). This is an ASTM D 3850 Test Method. **Even 2-3% loss, especially when exposed to multiple thermal cycles, can seriously degrade reliability.** [8]

Other new laminate features are uniform glass to laser drill easier, thinner glass for better electrical properties, thin and high dielectrics for distributed capacitance between power and ground, and a plethora of laminates with embedded passive layers to form resistors (Figure 26) and/or capacitors. But like PWB manufacturing, our dominance here is eroding. Currently, Matshushita (Japanese) and NanYa Plastics (Taiwan) are number one and number two in the world in FR-4 sales and manufacturing while North America still dominates in

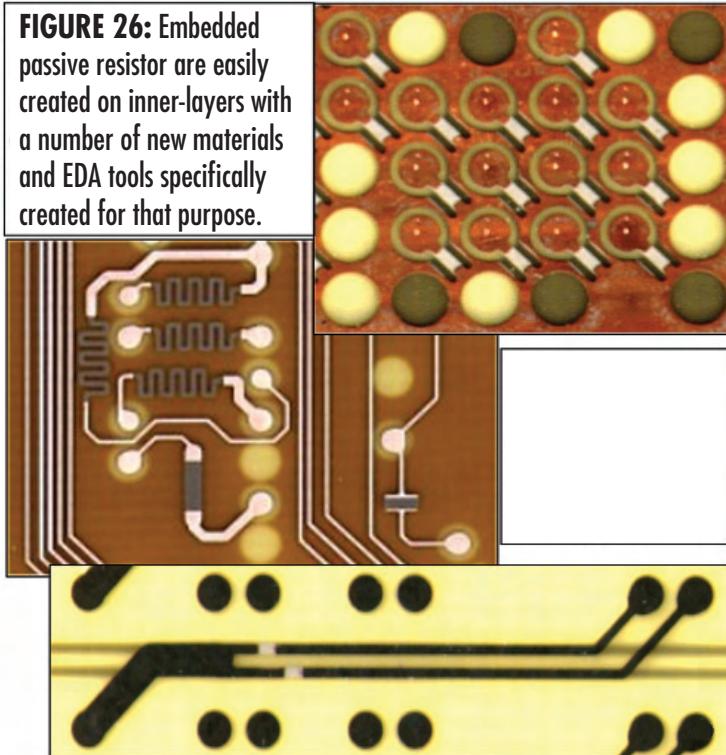
specialty high frequency laminates. All of these HDI materials are discussed in more detail in Chapter 5.

Other important materials for HDI are via-filling. As seen in Figure 27, electrochemical plating to fill blind vias as well as two-part epoxy, conductive or not, can be used to fill vias. This is discussed in Chapter 10.

Assembly Issues

Two important assembly issues are assembling and soldering open blind vias-in-pads and providing for assembly in-circuit testing. Only the open via-in-pad, created by conformal plating is of concern in assembly (Figure 27). Filled vias will solder as normal-flat lands. HDI assembly issues are discussed in Chapter 13.

FIGURE 26: Embedded passive resistor are easily created on inner-layers with a number of new materials and EDA tools specifically created for that purpose.



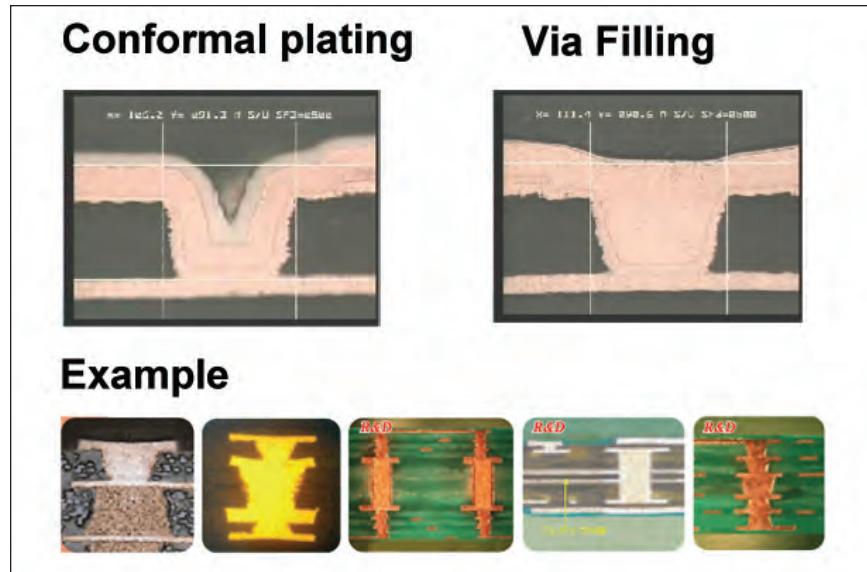


FIGURE 27: Via-filling plating baths to create flat-vias for assembly and via-stacking.

Assembly Test

The **DfT Process** and how it interrelates with the **PWB Design Process** can be seen in Figure 28. DfT software enables test engineers to work concurrently with designers. They can predict the fault spectrum, plan test strategies, understand fault coverage, and test access tradeoffs prior to the layout/routing stage of PWB design. This is important because of the cost versus volume considerations in product testing. Some types of software predict a fault spectrum for every pin, component, and signal on the board and thereby identify which test pads will provide the greatest test coverage. By listing the test pads that provide the greatest test coverage in descending order, designers can make intelligent decisions on which test pads should be provided on boards with limited access. Furthermore, if the software models the fault coverage provided by each machine in the distributed test plan (AXI, AOI, ICT, etc) it can identify which test pads can be removed

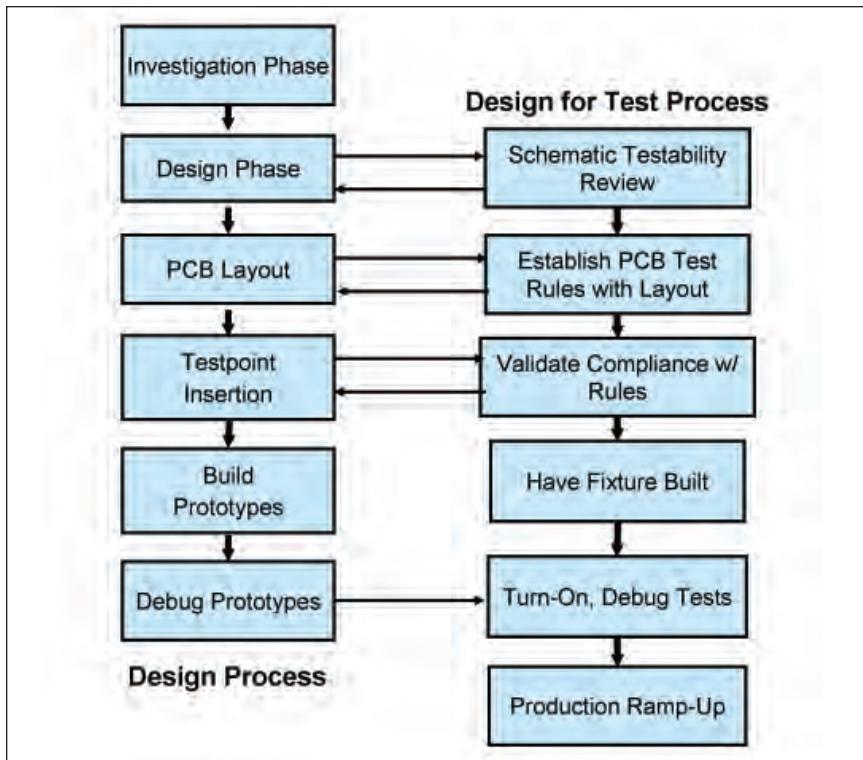


FIGURE 28: Design-for-Test flow chart and process.

because of overlapping fault coverage from other test stages. This is covered in greater detail in Chapter 13.

HDI Value Delivery Chain

While HDI substrates are one the fastest growing technologies in electronics packaging worldwide, they are not the simplest to embrace. Implementation requires a coordinated engineering approach, sometimes referred to as the HDI Value Delivery Chain (VDC). This chain has six links (Figure 29):

- System Partitioning
- PCB Design
- PWB Assembly
- Circuit Design
- PWB Fabrication
- Assembly Test

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These technologies must be present and coordinated in order for a successful HDI product to be realized. The successful integration of HDI technology will result in improved product performance, cost competitiveness, and new product innovations.

System Partitioning: When a new product is conceived, one of the first activities is to break the product down into components or partitions that will allow it to be designed, manufactured, sold, and supported. This is extremely important since a mistake here may result in a product which lacks the right features, costs too much, or arrives on the market too late. Partitions vary but may include the size, weight and volume. They also include distribution of standard active and passive components or custom ASICs, packaging of parts, number and size of printed circuits, and how they connect to each other. HDIS needs to be considered from the very beginning in order to take advantage of the benefits listed above. Applied later in the design process, the advantages will not be as great or may not even be available! Features, components, risk management, and manufacturability have to weighed and traded off in order to have a successful product.

Circuit/Product Design: The bulk of product creation and design involves the logic design, circuit simulation, component selection, custom integrated circuits, and mechanical designs. HDIS offers advantages in electrical and thermal performance. The key to value is the ability to simulate the improved electrical and thermal characteristics of the many HDIS options without which, the HDI structure



FIGURE 29: The HDI value delivery chain.

looks like any other TH board.

PCB Design/Layout: Many challenges have to be faced when designing an HDIS board. The wiring models are important to know in order to select proper design rules and constructions. With blind and buried vias, the HDI structures are more varied and complicated than conventional boards. Knowing what is cost effective from a design-for-manufacturing perspective is essential.

Special design rules must be considered with HDI structures. Each manufacturing process may have special considerations and limits. Design tools, pad stacks, and auto-routers are all used differently in HDI designs. The customization of the design process is not a common activity yet. The newer CAD systems have expert systems available that provide much needed advice. Manufacturability audit software concludes the layout process with a thorough check for any mistakes or errors.

PWB Fabrication: Of the entire value delivery chain, fabrication has become the most established. Currently over sixty companies worldwide are using at least twenty different processes to essentially make the same HDI structures. Making the microvia is the easy part, since lasers, etchers and photo-dielectrics have been rapidly improving over the years. The challenges are the basics: registration, fine line lithography, metallization, and plating. On HDIS, all of these have to perform at a superior level. While this is certainly taxing, it benefits all printed wiring board manufacturing processes. The one area of HDIS fabrication that has lagged behind is electrical test. We can fabricate much finer geometries than we can cost effectively test.

PCB Assembly: Assembly has new value to deliver with HDIS. Components can be closer together, which can change

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reflow profiles and repair. As the top side fills up, the opposite side has to take more components including many active ones. This will alter the assembly process and reflow profiles. With newer smaller and denser area array components like chip scale packages or flip-chips, the total number of connections per square centimeter increases dramatically. These newer smaller components with underfill or very high surface connection densities may have a reliability interaction with thinner HDI structures. Thin structures are more likely to flex during thermal cycles and this introduces new mechanisms and opportunities for failure, which must be thoroughly evaluated and tested.

Assembly Test: The final stage of the HDIS value chain is assembly level test which presents new issues with HDIS and the new smaller area array components. If via-in-pads are used with the area array components, after assembly there are no breakout vias to use to test probes. Design-for-Test becomes a major ingredient for system partitioning. Testing from the perimeter, boundary scan, or built-in self-test becomes a major design factor. Components may be so close now that test pads are either too large or there is no room to get a test pin into the area. Adding test pads to the surface after the board is designed can add to its complexity and cost and add detrimental parasitics to the circuit. Newer assembly level verification schemes will probably be developed that do not require the classical bed of nails fixtures, replacing them with faster non-contact test techniques.

Basics of HDI Technology Metrics

Interconnect Density

When planning an HDI design, there are three linked

measures of performance or metrics for the HDI process. The measures of performance or metrics for the HDI Value Delivery Chain (VDC) are important concepts for they capture the three elements of interconnection:

Assembly Complexity: Two measures of the difficulty to assemble surface mounted components. Component Density (C_d), measured in parts per square inch (or per square centimeter) and Assembly Density (A_d) in leads per square inch or per square centimeter.

$$C_d = p/a \quad \text{Equation 1}$$

$$A_d = l/a \quad \text{Equation 2}$$

Integrated Circuit Packaging: The degree of sophistication of components, Component Complexity, (C_c), measured by its average leads (I/Os) per part. A second metric is component lead pitch.

$$C_c = l/p \quad \text{Equation 3}$$

Printed Wiring Board Density: The amount of density (or complexity) of a printed circuit (W_d) as measured by the average length of traces per square inch of that board, including all signal layers. The metric is inches per square inch or centimeters per square centimeter. A second is the number of traces per linear inch or per linear centimeter. The PWB density was derived by assuming an average of three electrical nodes per net and that the component lead was a node of a net. The result was an equation that says the PWB density is β times the square root of the parts per square inch times the average leads per part. β is 2.5 for the high analog/discrete region, 3.0 for the analog/digital region, and 3.5 for the digital/ASIC region:

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$$\begin{aligned}\text{PWB Density (Wd)} &= \beta \sqrt{[Cd] \times (Cc)} \\ &= \beta \sqrt{[(\text{parts per sq. in.})] \times (\text{ave. leads per part})} \\ \text{Equation 4 [9]} &\end{aligned}$$

Where: p = Number of components (parts)
 l = Number of leads for all the components
 a = Area of the top surface of the board
(square inches)

A new metric for Wiring Density is the *connect*, as seen in Figure 30. A connect is defined as the SMT pad, the via pad and the trace connecting the two. Only so many connects can be placed in any defined area. The maximum connects are what define the red and blue dashed lines in Figure 31. This is the “Through-Hole Barrier.”

Packaging Technology Map

Figure 31 is what I call a Packaging Technology Map. The Packaging Technology Map was first displayed by Toshiba in January of 1991 in their paper, “New Polymeric Multilayer and Packaging” at the Printed Circuit World Conference V in Glasgow, Scotland.[10] I didn’t invent this chart, but I have been unsuccessful since 1991 in finding the Japanese who did. No one in Japan seems to know about this chart!!

By charting products of a particular type over time, an analysis shows how the packaging technology is changing, its rate of change, and the direction of those changes. This is the exercise of *roadmapping!* But now, the exercise will have some data behind it.

A second valuable feature of the map is the area of upper right. I have called this the “Region of Advanced Technologies.” This is where calculations and data have shown

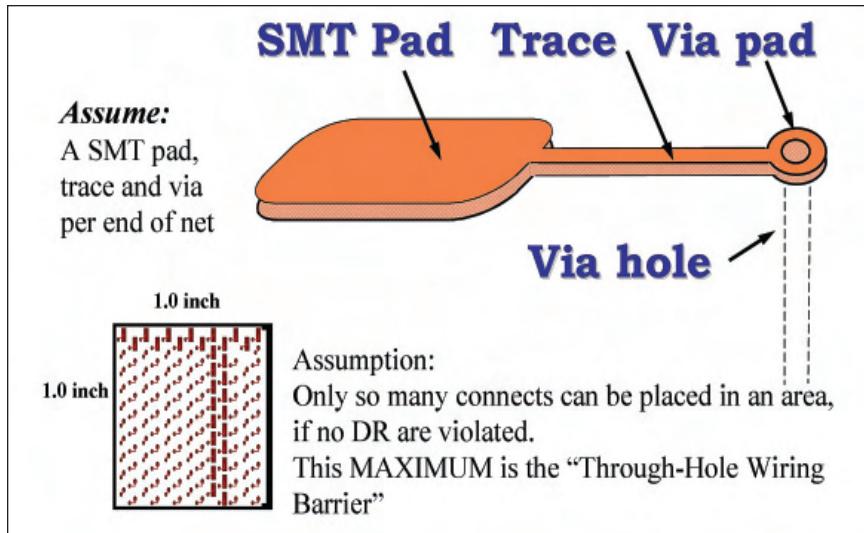


FIGURE 30: Definition of a wiring “CONNECT” = SMT land, its trace and via pad.

that it is necessary to have an HDI Structure. The dashed lines indicate the barrier or wall of HDI. Cross this and it now becomes cost effective to use HDI. Move too far and it becomes a necessity.

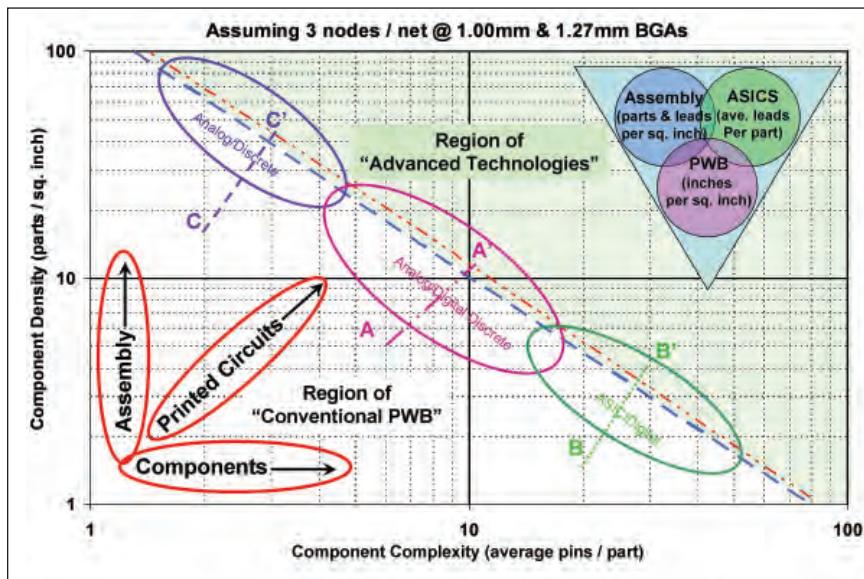


FIGURE 31: The through-hole (TH) wiring barrier as a function of a typical assembly.

Introduction to High-Density Interconnects

To create the packaging map, an assembly is measured for its size, number of components, and the leads those components have. The area is the laminate not the surface area. The components include both sides of an assembly as well as edge fingers or contacts. By the simple division of leads by parts and parts by area of the assembly, the X- and Y-axis are known. Plotting the components per square inch (or components per square centimeter) against average leads per component on a log-log graph, the PWB wiring density in inches per square inch (or centimeters per square centimeters) and Assembly Complexity (in leads per square inch or leads per square centimeter) can be calculated. The Assembly Density is just the X-axis multiplied by the Y-axis.

Through-Hole Wiring Barrier

When the Packaging Technology Map is used to analyze surface mount assemblies, three major zones show up which is why I call it a map. The first group includes products with a high content of analog devices and discrete components, such as camcorders, pagers and cellular telephones (C-C'). They have the highest assembly complexity, up to 300 to 400 leads per square inch (47 leads per square centimeter). The second group includes products with a high degree of digital components and some mixed discretes, such as notebook computers, desktops, instruments, medical equipment, and telecom routers (A-A'). The last group has a highly integrated use of ICs, such as PCMCIA, flash memory, SiPs, and other modules (B-B'). This group has the highest PWB wiring density of over 160 inches per square inch (25 centimeters per square centimeters).

When you look at the Packaging Technology Map, the Assembly Complexity lines cross the Wiring Density lines. At

high discrete levels, less wiring is required for the amount of assembly density. At high ASIC (and low discrete) levels, much more wiring is required to connect the components. This makes assembly metrics like leads per square inch a good indicator, but not adequate to substitute for the PWB wiring density.

If you travel any one of the three cords (A,B,C to A', B',C') and distribute the total leads per square inch into signal layers, Figure 32 shows the signal and total layers required to wire up that number of leads per square inch. Because of the space limitation of TH pads, as well as SMT lands of 1.27 and 1.00 mm pitch BGAs, the number of layers turns up exponentially around 130 p/si.

In contrast, HDI design rules and number of layers (Figure 33), at 130 p/si, require only ten layers. Even at 300 p/si, only 20 layers are required.

HDI Layout

The three layout metrics are:

- **Layout Efficiency** - a measure of the amount of traces on an inner-layer as a percentage of the maximum that could be on this I/L.
- **Routability Predictor** - a measure of how easy it is to route the selected traces (at their designated design rules) into the remaining space available.
- **Routing density** - inches of traces per square inch of inner-layer or cm of traces per sq. cm.

The equations for these can be found in Coomb's *Printed Circuits Handbook*, sixth Edition, Chapter 19.[6] The HDI Value Delivery Chain will use these metrics to establish many more relationships.

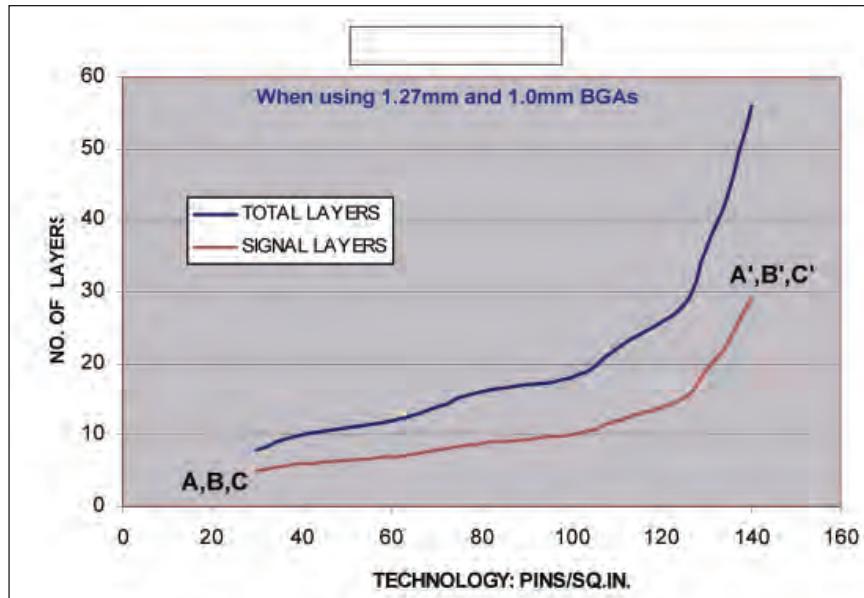


FIGURE 32: The TH density in average p/si versus number of signal and total layers of a board.

How to get started

After reading this book, it is our hope that you will consider using HDI technology for your next PWB design. To help you get started, we recommend a four-phase approach (Figure 34):

- HDI Technology Education
- Test Vehicle Evaluations
- Redesign Existing TH Board
- New Production

First, become familiar with HDI technology and identify your HDI fabricator. Their capability is your first concern. For a bit of advice, consider referencing the IPC Benchmarking Program, PCQR² which provides a set of standardized artwork, for 2 to 24 layers, and a very rigorous electrical testing regimen (including thermal cycling). The artwork and sample report

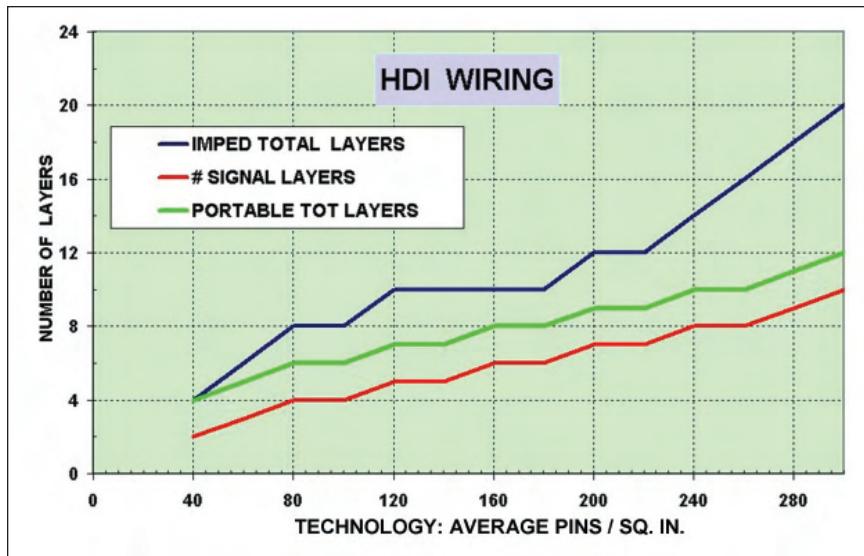


FIGURE 33: The HDI density in average p/si versus number of signal and total layers of a board.

are available at, <http://www.pcbquality.com>. Details and a review of this IPC Program are covered in Chapter 12 – Quality, Acceptability and Reliability. If questions persist about design rules, electrical performance, or reliability, then consider creating a simple Test Vehicle. To establish the design rules and HDI design methodology, consider the redesign of an existing high-density TH board using the advice in Chapter 3 – HDI Design. Finally, with this background and experience, HDI can be applied in the most favorable way.

HDI Technology Education

There are a great deal of technical details involved in using HDI technologies. Hopefully, this book will provide insight and education in this endeavor. PCB fabricators need to be involved and characterized for their HDI capability and prepared to accept your designs. Their DFM information may change your designs or stack-ups.

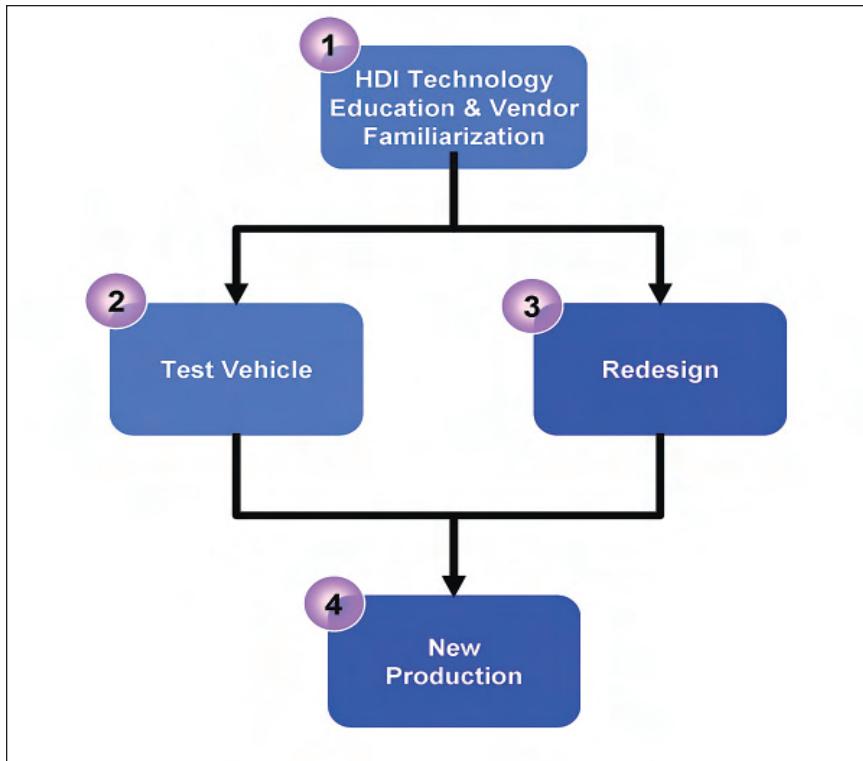


FIGURE 34: Getting started in HDI can involve four phases of learning and development.

Test Vehicle Evaluations

The PCB vendor may not be familiar with the materials you have designed with or you may need to test some of the many new high-temp or high performance materials listed in Chapter 5 – Materials. This is a good time to test high-frequency performance and measure the signal integrity improvements. Reliability can be tested for the HDI stack-up, materials, and fabricator selected.

Redesign Existing TH Board

Simultaneously, a recent high-density board can be redesigned to an HDI structure to test assembly, performance,

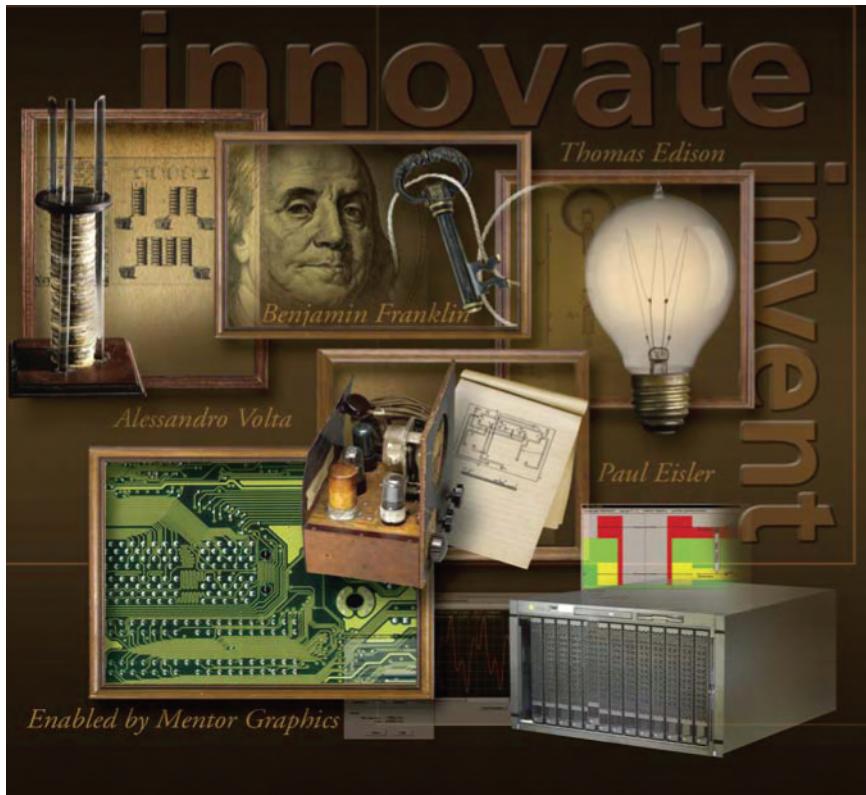
ICT and any other issues. It may not be necessary to fabricate this redesigned board, but if components are not moved, samples can be assembled and tested. If the redesigned board does not take advantage of distributing parts on the secondary side, then only the BGA fanout, boulevard routing and stack-up changes can be evaluated. Additional size and routing advantages will have to wait until the final phase implementation.

New Production

Once all the questions and issues are resolved, design tools mastered, and vendors qualified, the HDI technology can be freely implemented

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PRINTED CIRCUIT BOARD DESIGN

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The HDI Handbook

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The HDI Market

By Karen Carpenter — **CMTCAssociates, Inc.**

The Birth of the Microvia

Beginning in the late 1980s and early 1990s, the electronics market underwent a very significant change. Advancement in semiconductor technology gave rise to the digital revolution. Personal computing evolved to provide users with a higher level of functionality and integration was key in the move to portability of desktop models. Applications that were traditionally mechanical, such as cameras, were redesigned to incorporate electronics.

Mobile computing allowed users the flexibility of working from remote locations, a very attractive idea in many occupations. This freedom, however, resulted in an almost immediate concern with weight and size. Designers searched for ways to reduce the weight of the machines and to make the physical outlines sleek and portable. This quest for smaller, thinner, and lighter machines would become the focus for a growing number of applications over time.

The demand for integrated circuits increased. Surface mount technology (SMT) packaging, introduced in the late 1970s, was rapidly replacing pin-in-hole packages as seen in Figure 1.

SMT eliminated the need for the large through-holes (THs) required for pinned components and reduced the mounting

The HDI Market

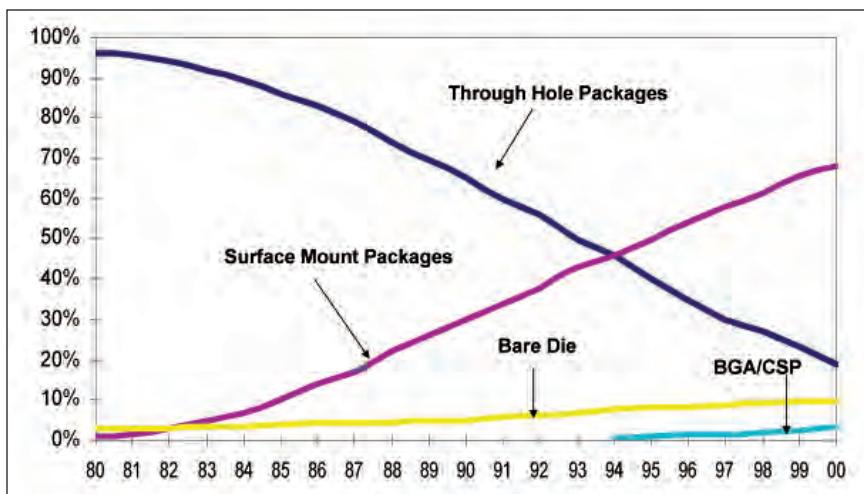


FIGURE 1: Worldwide Package Substitution [Courtesy of BPA Consulting]

area needed on the circuit board. However, the expanding use of SMT components created challenges in the design of Printed Circuit Boards (PCBs). The small through-vias utilized for interconnection increased drilling cost and caused plating issues. Although the smaller components allowed designers to put more components in a given footprint, this resulted in PCB routing challenges which drove layer count up in many applications.

Further complicating the matter was the introduction of area array packaging. BGAs offered the promise of a smaller footprints than pinned packages and could accommodate high I/O devices. CSPs delivered the smallest form factor. Both increased the solder joint density on circuit boards and drove the need for a high-density interconnect.

With layer counts increasing and drilled hole sizes decreasing, costs were on the rise. Engineers focused on ways to combat this trend while at the same time meeting the needs of smaller and lighter PCBs. It seemed logical to explore ways to increase interconnect density, decrease layer thickness, and

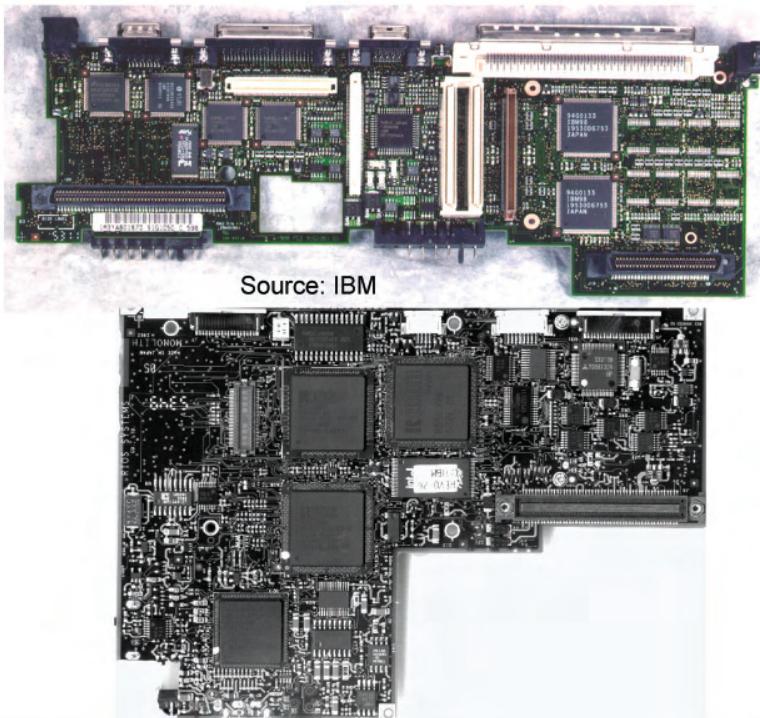


FIGURE 2: Examples of SLC in IBM laptops. Top: ThinkPad card was a 1+8+1 cross section with 4 mil lines and spaces. The 43 mil thick card contained 4299 – 5 mil photovias. Bottom: Palm Top PC 110 Base Card was a 1+8+1, 39 mil thick card with 3 mil lines and spaces and 3681- 5 mil photovias. The raw card outline was reduced by 50% using microvias [Courtesy of IBM]

eliminate the drilling operation where possible. These factors culminated in the introduction of microvia technology.

Different solutions were introduced by a number of companies. In 1991, one of the most recognized commercial applications came from IBM Yasu when microvias were designed into a ThinkPad™ laptop computer. For many years to follow, new designs utilized the microvia technology. Figure 2 includes two examples.

Over the next six years, the majority of companies producing laptop computers were pursuing microvia-based

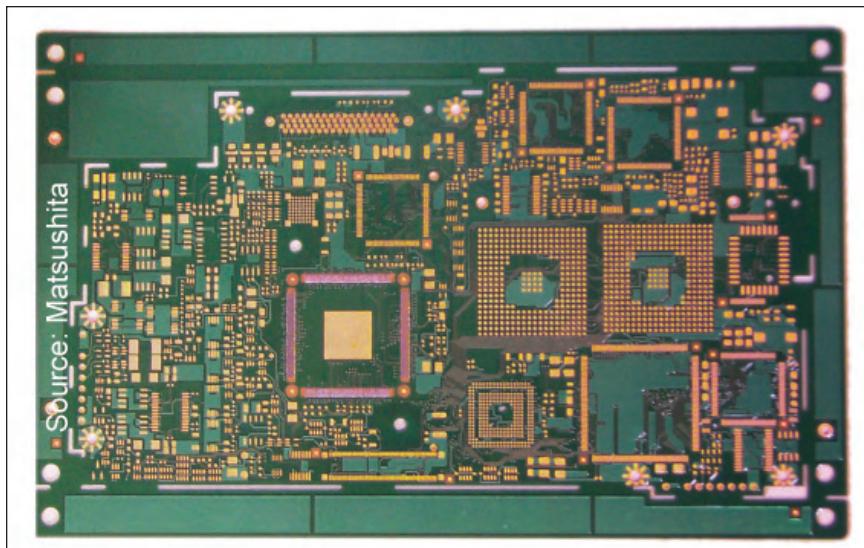


FIGURE 3: Example of Microvia board application by Matsushita ALIVH board for PC with 8 layers, 60 µm lines and 90 µm spaces (Courtesy of Matsushita)

solutions. Figure 3 shows additional examples. Some, such as Fujitsu, in its model FMV-BIBLO NPV 16D sub-notebook [1], chose to implement multichip module packages that used the technology rather than implementing on the motherboard.

Microvia technology slowly found a foothold in a variety of applications, predominately developed in Japan. The high mounting density required in digital cameras and camcorders greatly benefited from the technology. In 1996, Sony introduced a camcorder that utilized a combination of microvias and CSPs. (See Figures 10 and 11 in Chapter 1 – Introduction to High-Density Interconnects.) JVC and Matsushita/Panasonic followed suit. Sharp introduced microvias in its mini-digital cameras. PCMCIA cards and PDAs also utilized the technology. Microvia technology was also in the early stages of design for navigation systems, automotive, and mass storage.

Even with all the interest in the technology, there were many issues. Although many fabricators claimed the ability

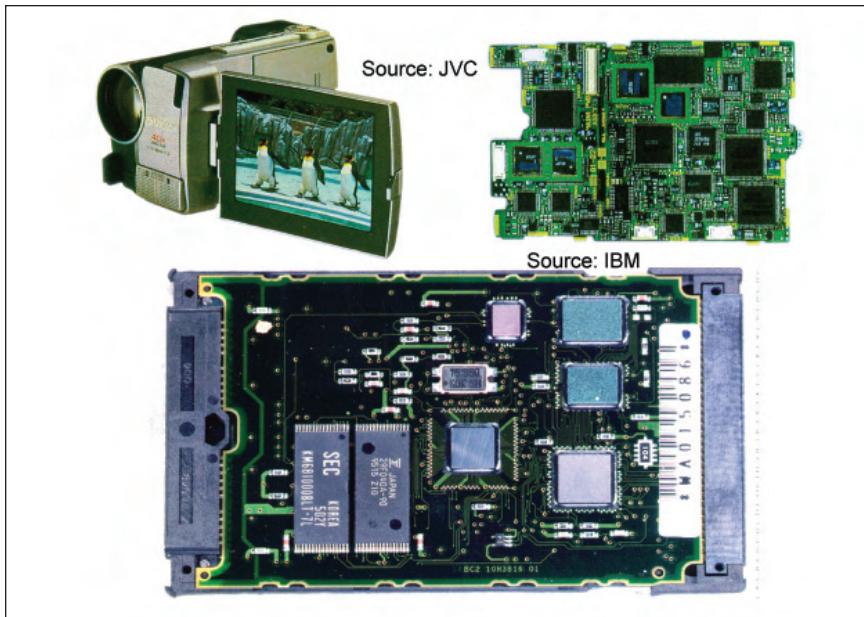


FIGURE 4: Examples of Microvia board application include (1) the JVC digital camcorder microvia board with a 2-4-2 construction with a board that was 68 mm x 39 mm, 0.8 mm thick with 100 lines and spaces, containing 6 - 0.8 mm CSPs. (Source: JVC) and (2) a wireless modem PCMCIA card which is a 1+4+1 cross section with 2 mil lines/3 mil spaces and 5 flip-chip attach sites (Courtesy of IBM)

to build boards, very few had volume production experience. Design tools were not widely available to the industry. Most designs were produced within large OEMs that possessed proprietary systems. But the most important factor was the cost. Early on, many believed that microvias allowed for a lower cost circuit board. In reality this was not always the case. In general, the materials were more expensive no matter what process was used. Lasers were not typically found in PCB shops. In addition, the build requires sequential processing which, by definition, adds process steps and results in lower yields. However, if the designer were able to reduce the board size and/or the layer count, the cost could indeed be decreased.

Any new technology requires volume to drive down costs

The HDI Market

and build infrastructure. This was true for microvias. The killer applications came in two forms. The first was the cell phone. In the mid 1990s the race was on to find ways to reduce weight. According to Nikkei Electronics[2], in 1992, typical phones weighed between 220 and 250 grams. By 1998, mobile phone weights had been reduced to around 70 grams. The target for 1999 was to reduce the phone by another 10 grams, removing 3 grams from the PCB. This weight reduction was made possible by employing a thinner, smaller board with microvias and higher IC integration levels.

Silicon integration enabled an increase in functionality. The introduction of CSP and microvia technology enabled miniaturization. TechSearch International reported that the mounting area was reduced on the order of ten percent per year despite increasing interconnect density. With surging demand, mobile phones became a critical platform to drive the creation of infrastructure, improved yields, and new materials.

The availability of microvia technology enabled another significant evolution in the area of chip packaging. The migration from ceramic substrates to laminate drove investments by many circuit board manufacturers to meet the escalating demand. With a lower dielectric constant and reduced signal delay, laminates offered improved performance. The well-established capability for producing circuit boards was now utilized to produce laminate chip packages for wirebond applications.

Concurrently, semiconductors were continuing to follow Moore's law with the number of transistors roughly doubling every 18 months to two years. The Semiconductor Industry Association saw increases in pin count and interconnect density as seen in Figure 5.

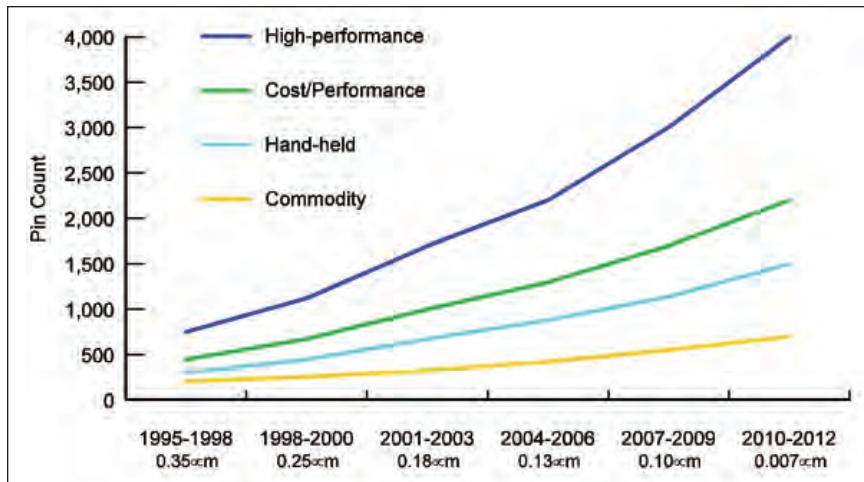


FIGURE 5: I/O Trends for Semiconductor Devices (Courtesy of SIA)

Flip-chip technology provided a way to design the I/O in an area array for high I/O devices. Laminates with a layer of HDI or microvias enabled designers to take advantage of organic solutions.

Workstations, networks, and telecommunication systems utilize ASIC designs with thousands of I/Os requiring fine-pitch packaging. Fujitsu Microelectronics, IBM, LSI Logic, Mitsubishi Electric, NEC, and Toshiba were some of the first companies to offer high I/O ASICs on microvia laminate substrates. Ball counts ranged from about 500 to over 1,700 with constructions ranging from one to three buildup layers per side. The substrates were produced with 25 – 50 μ m lines and spaces.[1]

ASIC packaging pushed the technology envelope for HDI. The application utilized fine lines and multiple layers of microvia for escape. However, it represented only a small volumetric portion of the laminate chip packaging market. Microprocessors, on the other hand, were high volume as well as high I/O. When Intel began shipping the Pentium® II



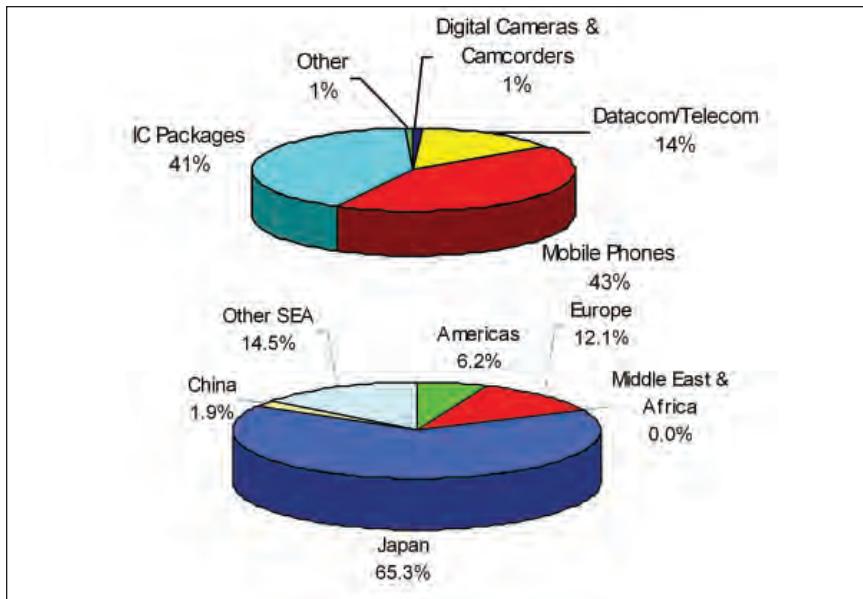
FIGURE 6:
Intel's mini-cartridge
(Courtesy
of Intel)

processor for mobile products, the second killer application was introduced (Figure 6).

The device was packaged on a 31mm x 31mm substrate with a 2-2-2 construction. The initial substrates were produced with a photovia process but future generations were migrated to a laser process.

The volumes associated with Intel microprocessors and cell phones provided strong motivation for fabricators, material suppliers, and equipment producers to improve process, design, throughput, and yields to make microvias and HDI viable solutions.

The period of technology introduction and early adoption

**FIGURE 7:** Microvia Market Profile

of microvias for printed circuit boards and chip packaging was just under ten years. It was during this time that two different definitions for microvias surfaced. One, adopted by the IPC, held that microvia structures were interconnections formed using blind holes of 150 microns (6 mils) or less made by plasma, photo, mechanical, or laser processes. Others suggested that the microvia had a 250 micron (10 mil) via diameter. Utilizing the stricter IPC definition, the total microvia market grew from less than \$1 million to over \$3 billion between its emergence in a commercial application in 1993 and 2000. The number of fabricators grew from a handful to over 70 worldwide. A profile of the market is found in Figure 7 above.

Microvia-enhanced printed circuits for mobile phones and IC packages accounted for over 80% of the market by revenue. Japan, which invested heavily in technology development and capacity, produced over 60% of the substrates.

Current Markets and Applications

The first ten years established microvias as an enabling feature in printed circuits on the road to higher interconnect densities. During this period, the early adopters learned not only how to design, but also confirmed the reliability of circuit boards with this structure. Since that time, there have been numerous advances and extensions of the technology. In addition to blind vias produced in buildup processes, the industry is utilizing traditional buried vias, filled vias, stacked vias, and various combinations of the above to utilize the z-axis to increase interconnection density. These variations in structure are discussed in detail in Chapter 3 – Design of Advanced Printed Circuits (HDI) and Chapter 6 – The HDI Manufacturing Processes.

Technical requirements can vary greatly from application to application across different market segments. The expansion of the original microvia concept has enabled high-density interconnection to be accomplished in a variety of ways, depending on specific application needs. In an effort to provide a complete picture, the platform definitions found in Chapter

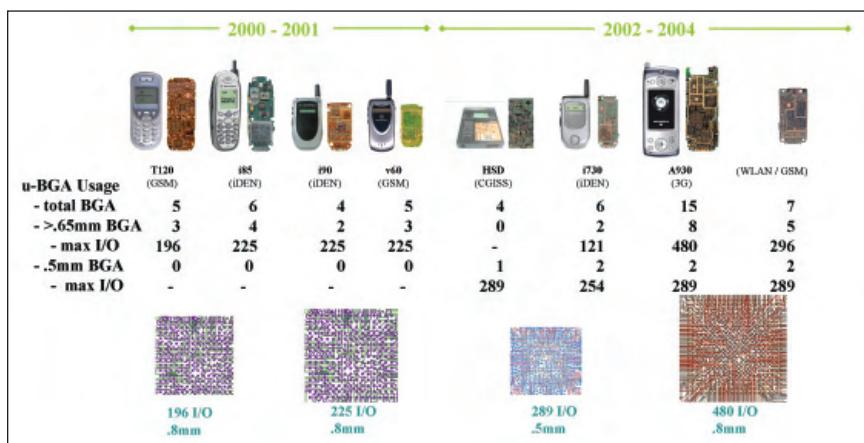


FIGURE 8: Trends in Packaging for Mobile Phones (Courtesy of Motorola from its presentation to IPC)

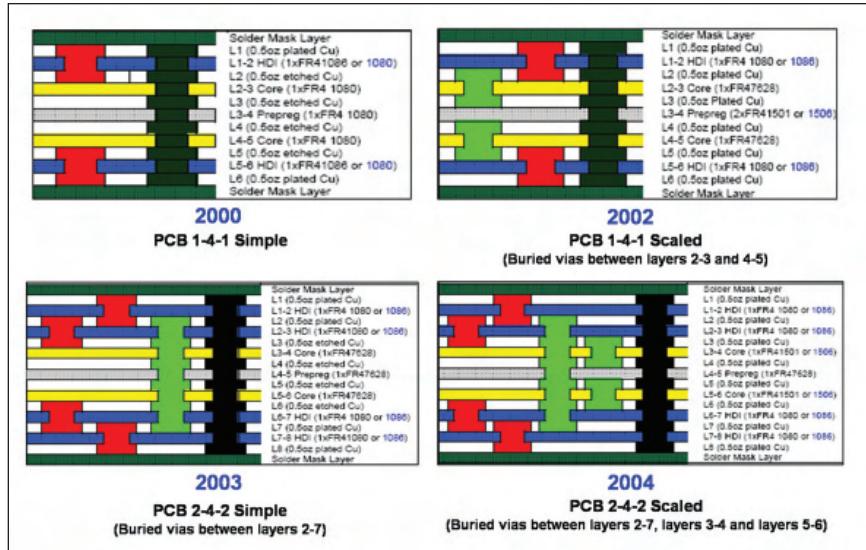


FIGURE 9: Evolution of Motorola Stack-up Technologies (Courtesy of Motorola from its presentation to IPC)

1 have been proposed. With this in mind, the markets and applications employing high-density interconnect solutions is perhaps larger than the originally defined microvia market.

The market for HDI and microvia has continued its upward climb. Cell phones have remained a major growth engine. In 2000, around 400 million phones were sold. The number of phones sold in 2006 was just short of 1 billion. Although the physical size of the phones' boards have been reduced, the increase in cell phone function has driven a significant increase in complexity, adding layers of HDI, and reducing feature sizes. One example of the technology evolution can be seen by examining the work done by Motorola.

Between 2000 and 2004, the company saw a significant increase in both the quantity and complexity of micro-BGA packages used in cell phones. While package pitch was being reduced to accommodate smaller footprints, package I/O was increasing as seen in Figure 8.

The HDI Market

The use of high-density component technologies such as 0.5mm BGAs, 3-D packages, and 0201 components accelerated an increase in design complexity. Pad densities grew from just over 200 pads/in² to over 600 pads/in².

Motorola evolved its use of high-density interconnection as seen in Figure 9. The use of buried and blind vias was key to their strategy.

In 2005, a major shift in mobile phone design was seen when Motorola introduced the RAZR which was not only smaller but was also only one half-inch thick. The main board in the phone, seen in Figure 10, was a 2-4-2 construction.

For 2005, the company's roadmap introduced a 3-2-3 cross section which contained buried vias from layers 3 to 6, layers 3 to 4, and layers 5 to 6. Currently the company is evaluating the use of stacked microvias and the use of HDI flex and rigid-flex.

The chip packaging market has also continued as a growth engine. There have been many hurdles to overcome which has slowed the introduction of the flip-chip. HDI is utilized in area arrays for processors, chipsets, ASICs, FPGAs, and high-end

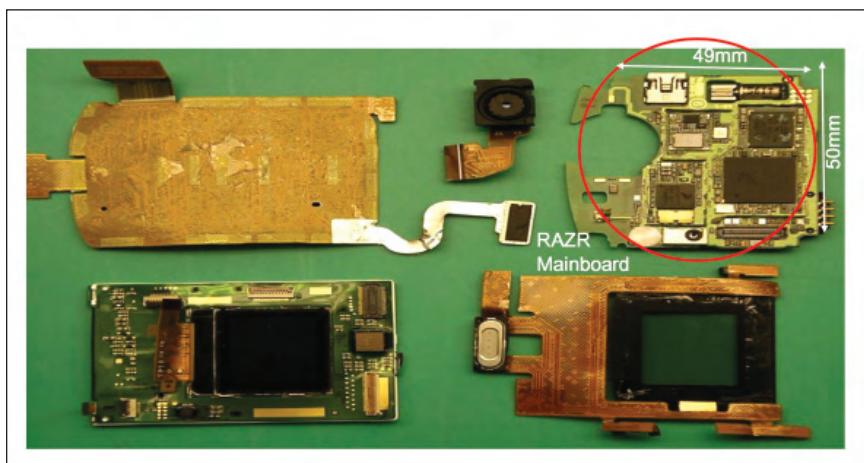


FIGURE 10: RAZR Interconnect Technologies (Courtesy of Motorola)

DSPs where the bump pitch is tight. HDI can also be found in some CSPs, SiPs, and MCMs.

Microprocessor packaging has increased in complexity to accommodate higher function. An example can be seen by examining the Intel Xeon E5410, also known as Harpertown, shown in Figure 11. The 37.5 x 37.5 mm package is 4.1 mm thick with two flip-chip mounted die. The 2-layer, glass reinforced core has five layers of resin coated copper on the top and bottom. The buried via holes which are 28 mm in diameter are resin filled. Layers 1 through 4 contain 100 μm blind vias while the vias in layers 8 through 11 (on the die attach side of the package) are 65 μm . The copper thickness in the HDI layers is 20 μm and 80 μm on the core.

Despite the increasing use of flip-chip, there have been many hurdles to overcome which has slowed the introduction. Over the years, yields, capacity, lack of infrastructure, and pricing for flip-chip substrates have contributed to a slower transition from wirebond chip-to-package interconnect. However, as the market demand for flip-chip increases, these issues are being resolved. TechSearch International estimates that 2.1 billion solder bumped ICs (without saw filters) were shipped in 2006. This number is projected to grow to about

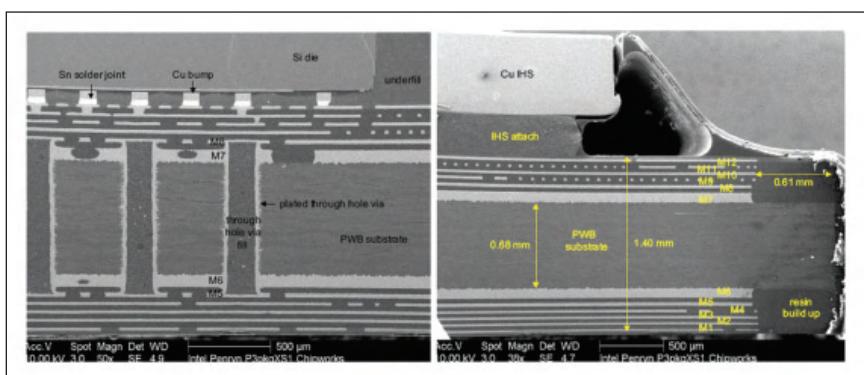


FIGURE 11: Intel's Xeon E5410 Package (Courtesy of Chipworks)

The HDI Market

6.0 billion by 2010, dramatically increasing the need for HDI packages.

Mobile and hand-held digital applications have continued to benefit from the ability of HDI to provide a high level of functionality in a small and light format. Digital still and video cameras, MP3 players, digital games, and automotive applications are currently using HDI.

The technology is less widespread in portable computing. In their recent analysis, Electronics.ca Publications reported that price pressures in the laptop market have limited the use of HDI. to around 10% of the total shipments and is used primarily in systems with screens less than 13 inches in size. [3]

The ultra-mobile PC (UMPC) is defined by Intel as a flat handheld device midway in size between a smart phone or PDA and a notebook PC. One example is the Sony VAIO. According to Prismark Partners, the main board in the system measures 9.5 cm x 9.3 cm x 1 mm. Its construction is a 2-6-2 "plus" with microvias and fine lines and spaces on the outer cores to accommodate the main processor, chipset, and memory.

The challenges in the UMPC market in many ways mirror those in the mobile phone space. With new constraints on product size and the desire for functionality equivalent to laptop or desktop models, HDI in one or more layers of packaging is likely.

At the opposite end of the portable application space lies the high performance market. Applications here are characterized by high data transmission speeds, advanced processing capability, and fast interconnection speed between server and network connections.

High-end systems such as servers, routers, base stations,

- Mainboard UMPC features main components for notebook functions
 - Intel Core Solo MPU
 - Intel 945 GMS Chipset
 - Eight 512Mb DDR2 DRAM from Infineon/Qimonda
- 10 Layer PCB construction
 - 9.5cm x 9.3cm and is 1mm thick
 - 2-6-2 "plus" construction has microvias and fine L/S on outer core layers
 - Fully plated microvia on layers 2 and 9 allow for stacked vias
 - 65 μ m diameter microvias on layers 1,2,3 and 8,9,10
 - 150 μ m - 250 μ m L/S on core layers
- Halogen-free and lead-free compatible PCB made in Japan

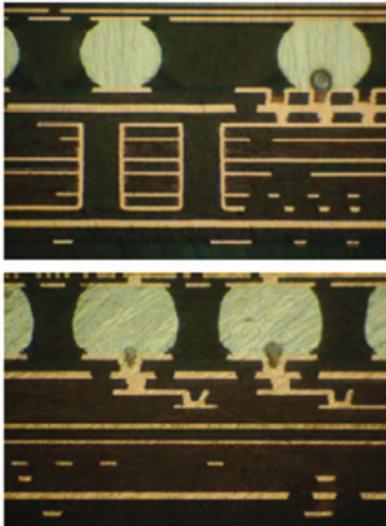


FIGURE 12: Sony VAIO UMPC Motherboard (Courtesy of Prismark Partners (www.prismark.com) and Binghamton University)

and supercomputers are typically constructed with a backplane or mid-plane with line cards or daughter cards that plug into them. The line cards are typically populated with high I/O ASICs, microprocessors, and other components which drive complexity into the board design. Signal integrity issues, resulting from faster rise times, longer transmission lines, and increased parasitic loss from the high number of PTHs required for the components, have designers looking to HDI for solutions. The shortened interconnect lengths, smaller feature sizes, and ability to eliminate THs offer help in the optimization of signal integrity and cycle time.

In the telecom space, Cisco currently employs HDI structures which include up to two layers of build up and buried vias. The company is reportedly evaluating new microvia processes, deep blind vias, and stacked vias. High-end servers or supercomputers from companies like IBM and

The HDI Market

Sun employ various HDI elements such as buried vias, stacked vias for z-interconnect, and microvias. NEC-Toppan recently displayed an 18-layer (5-8-5) board for a supercomputer application. The technology can be found in some base stations as well.

Packaging for the complex, high speed devices for these systems is an area of significant growth for HDI. Although not the focus here, the use of high performance materials in conjunction with a variety of HDI enabled cross sections are employed to achieve the performance levels required for the high-speed devices. A table of the packaging used in high speed applications is found in Figure 13 from a BPA Consulting report on High Speed Electronics.[4]

These flip-chip BGAs are predominately placed on packages that are buildup multilayer core, coreless, or metal core structures, all with HDI features.

As microprocessors, ASICs and other high-end devices

Market Segment	Semiconductor Application	Packaging Types
Routers & Switches	PHY Switching ASIC NPU	FCBGA, 500-1500 I/O FCBGA, >1000 I/O FCBGA, >1200 I/O
Servers & Data Storage	CPU Switching ASIC PHY	FCBGA/PGA, >1000 I/O FCBGA, >1000 I/O FCBGA
Wireless Base Stations	DSP/ASIC/FPGA RF chipset	FCBGA, >400 I/O CSP,BGA
Military & Avionics	As above for communication and control systems	FCBGA

Source: BPA Consulting Ltd.

FIGURE 13: High Speed Packaging Summary (Courtesy of BPA Consulting Ltd.)

have continued to increase in complexity with higher I/O, the package pitch has continued to decrease. These trends make it increasingly difficult to wire out the components, driving increases in layer count. At the same time, designers are looking to improve signal integrity and power management. Increasingly, these designers are turning to HDI. To truly appreciate the power of the technology, it is beneficial to examine some case studies. This is discussed in more detail in Chapters 3 – Design of Advanced Printed Circuits and Chapter 4 – Electrical Performance.

The first example is for a board in a high speed network controller. The board, initially designed as an 18-layer with 10 signal planes, was 73 mils thick. It utilized 4 mil lines and spaces with 13 mil pin through-holes (PTHs). By incorporating a top and bottom layer of HDI, 6,434 PTHs were eliminated which cleared wiring channels in the signal planes (Figure 14).

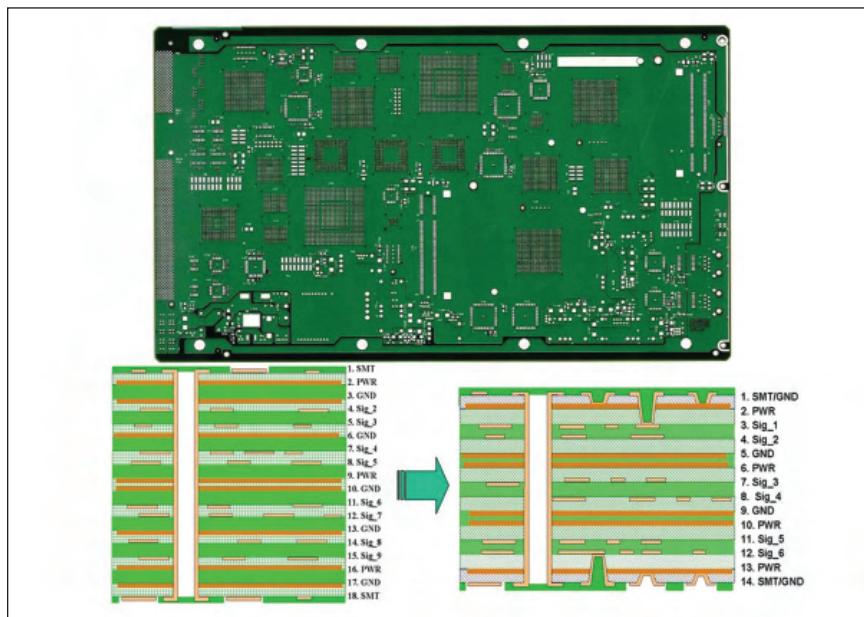


FIGURE 14: Cross Section of High Speed Network Controller (Courtesy of Holden Consulting)

The HDI Market

By increasing the wiring efficiency, two signal planes and two power planes were eliminated reducing the layer count to 14. This redesign provided about a 16% reduction in cost for the PCB. In this case, no change was made to the physical size of the board.

In some applications, changing the board size is not practical because of fixed rack or platform construction. However, when shrinking the footprint is possible, the savings can be even greater. Example two is for a board found in a major avionics application. The original design was a 92 mils thick, 8 inch x 11 inch board with 18 layers driven, in part, by the use of two 676 I/O components on a 1.0 mm pitch (Figure 15).

The redesigned board had a 10-layer, 1+8+1 cross section which was 62 mils thick. Through-holes, utilized in the base 8-layer structure, were filled and the HDI was added as the

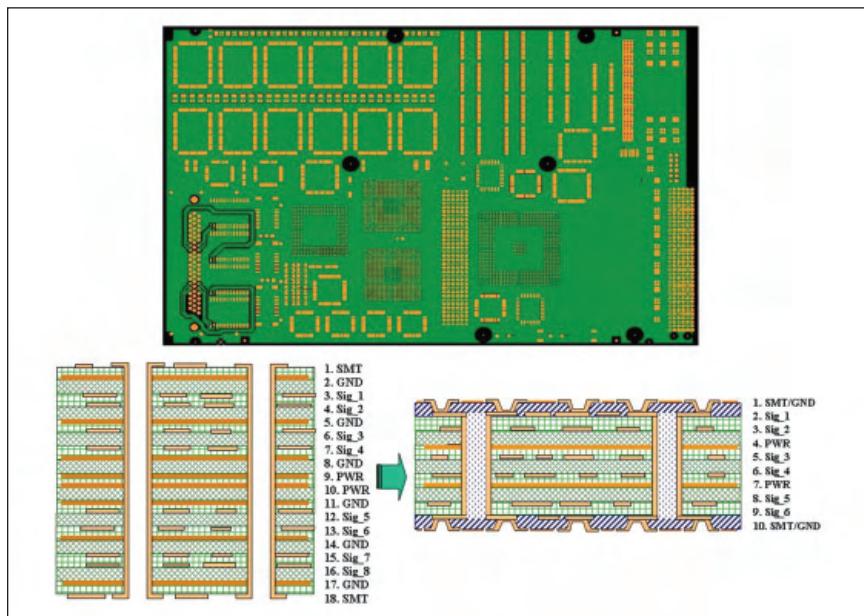


FIGURE 15: High Speed Controlled Impedance Avionics Board (Courtesy of Holden Consulting)

outer layers. The net result was a board with 44% fewer layers, that was 35% smaller, and 33% thinner with shorter signal paths and improved performance. A cost savings of 50% was realized. With careful design and openness to change, significant savings and performance improvements can be realized with HDI. This paradigm shift is now making its way into high end data and telecom, defense, avionics, aerospace, and medical markets. The design methodology is presented in Chapter 3 – Design of Advanced Printed Circuits.

The introduction of system-in-package (SiP) as an alternative to system-on-chip (SOC) and the desire to embed both active and passive devices are emerging as new growth areas. HDI allows many microelectronic solutions to be packaged in a small footprint.

Although many SiP solutions come in the form of package-on-package (PoP) with wirebond connections, there are a number which incorporate a flip-chip in an HDI package. More detail on this topic will be discussed in Chapter 16 – Advanced Packaging and System-in-Packages.

HDI has provided a reliable interconnect methodology for embedding both active and passive devices. Whether the solution utilizes formed or placed components, microvias are often used to create connections between devices. One example can be found in the work undertaken by Casio, which together with CMK, has developed a process to embed a wafer level package (WLP) in an HDI or buildup substrate. The WLP is placed on the carrier and then encapsulated with a liquid epoxy as seen in Figure 16.

Vias are laser drilled to the copper bumps and layers are added by building up from both sides. Additional SMT components can then be attached including WLPs. Casio markets this as a new, smaller, and thinner PoP structure. The

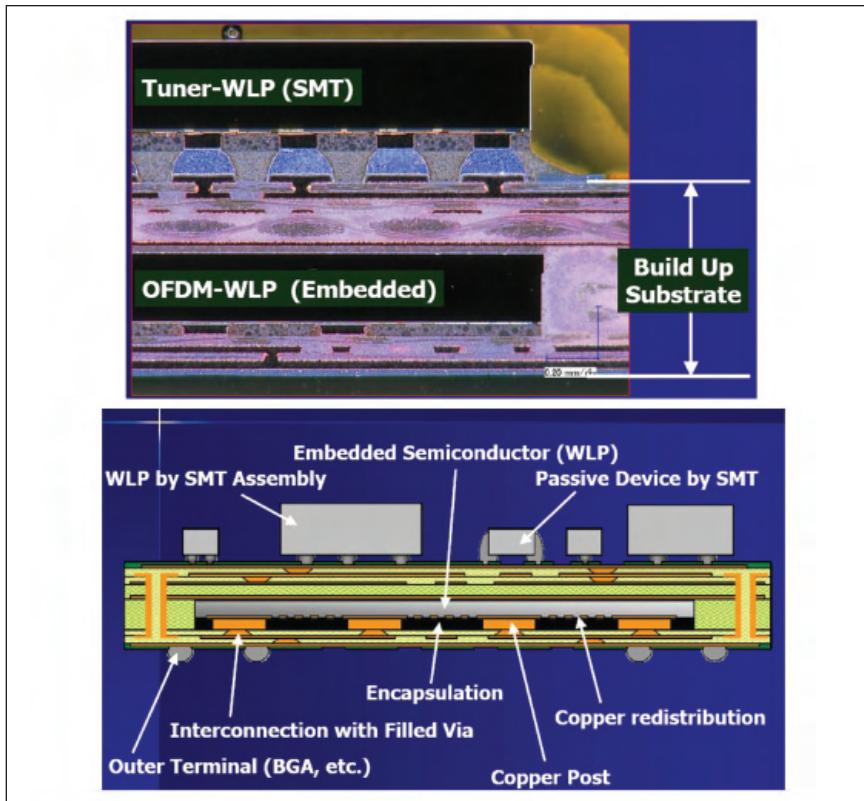


FIGURE 16: Casio's EWLP Module (Courtesy of Casio Micronics)

company has used the technology to develop a digital TV tuner module.

Market Size and Projections

The proliferation of techniques to create high-density interconnects has provided many solutions to a complex problems. The variety of options allows a designer to choose the one that best delivers the performance and cost needed for the application. This dynamic, however, makes it difficult to measure the size of the HDI market as defined in the platforms. To establish a baseline, it is helpful to look at the trends for buildup technology.

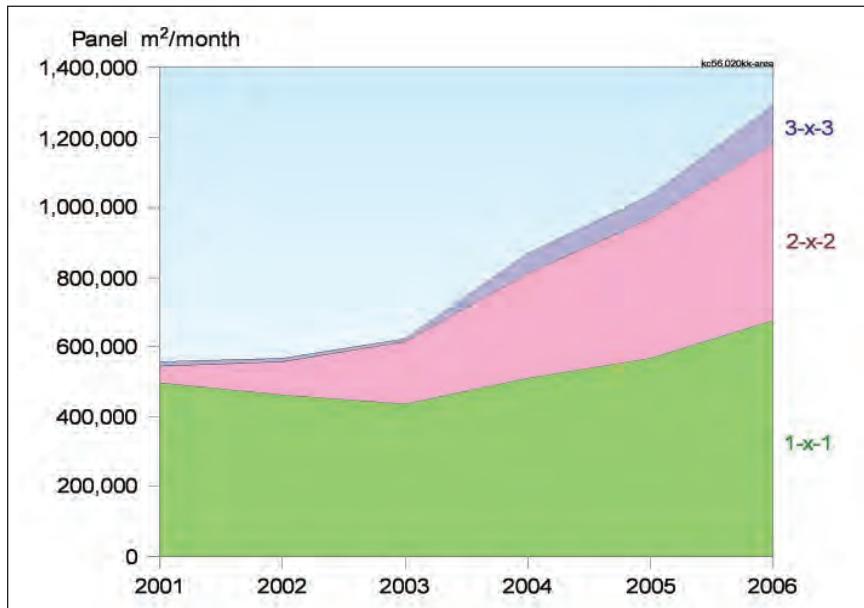


FIGURE 17: Microvia Technology Trends (Courtesy of Prismark Partners, www.prismark.com)

Microvia board and substrate products have increased in complexity as can be seen by examining the data in Figure 17.

While the 1-n-1 structure has continued to be the predominate cross section, significant growth in production of 2-n-2 and 3-n-3 products has occurred as interconnect density has continued to increase. BPA Consulting offers a slightly different look, as seen in Figure 18, by separating the standard buildup from other processes such as ALIVH. Included in their analysis are products that are typically less than 100 microns in diameter and use a thin dielectric that is subsequently added to the board or has conductive post technology. In either view, the trend is clearly toward increased complexity.

Significant capacity has been added to address the expanding market and increasing number of HDI layers. In 2000, the industry was producing fewer than 500,000 panels m^2/month . By 2006, this run rate had increased to roughly

The HDI Market

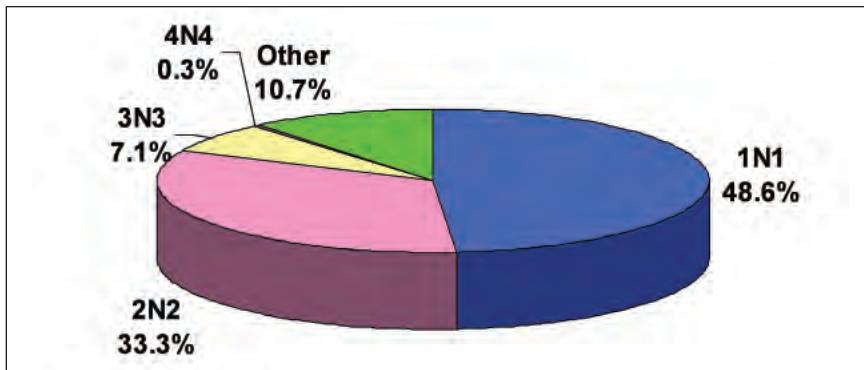


FIGURE 18: HDI Board Split by Buildup Layer Count [XNX] (2006) (Courtesy of BPA Consulting Ltd.)

1,300,000 panels m²/month (Figure 19).

Prismark reports that the panel production rate exceeded 1,400,000 m²/month in 2007.

The rise of the HDI or microvia market has continued. In 2006, the IPC reported that the microvia printed circuit board market had grown to \$5.8 billion. Prismark Partners reported

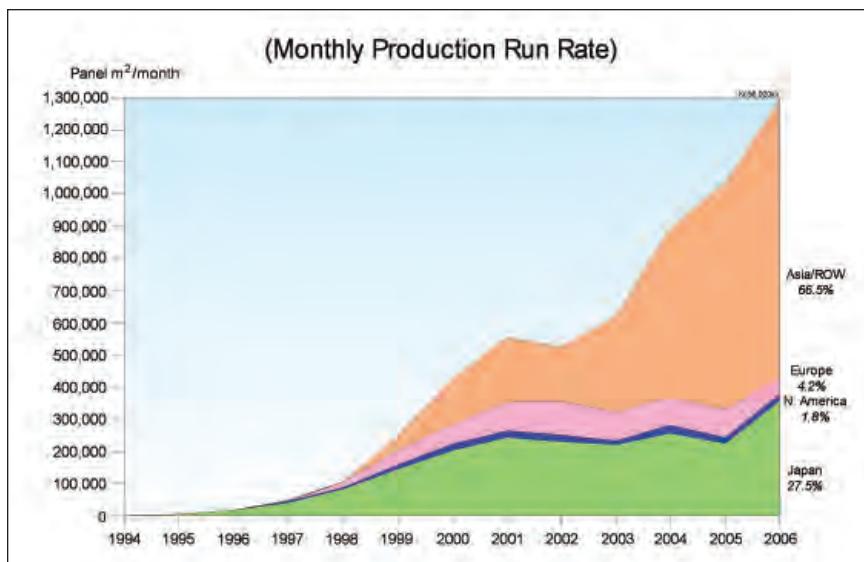


FIGURE 19: Microvia Panel Production (Courtesy of Prismark Partners, www.prismark.com)

that an additional \$3.0 billion IC packages were produced with HDI. Therefore the total market has almost tripled in a five-year period. In 2000, microvia technology accounted for about 8% of the world rigid circuit production by revenue. By 2006, this number had grown to almost 22%.

The changes which have occurred in the market profile since 2000 can be seen in Figure 20 which identifies the 2007 market by both dollar value and area.

In 2007, it is evident that cell phone and IC packages have continued as major growth engines. However, the technology has also expanded significantly in digital handheld applications and the high-end datacom/telecom market. Between now and 2012, the HDI market, measured in dollars, will likely experience growth in excess of 8% Compounded Average Annual Growth Rate (CAAGR). The adoption of flip-chip in packages and the continued proliferation of the technology in the newer markets will drive most of the expansion. If flex and rigid-flex applications with HDI become more widely utilized this number could grow even more.

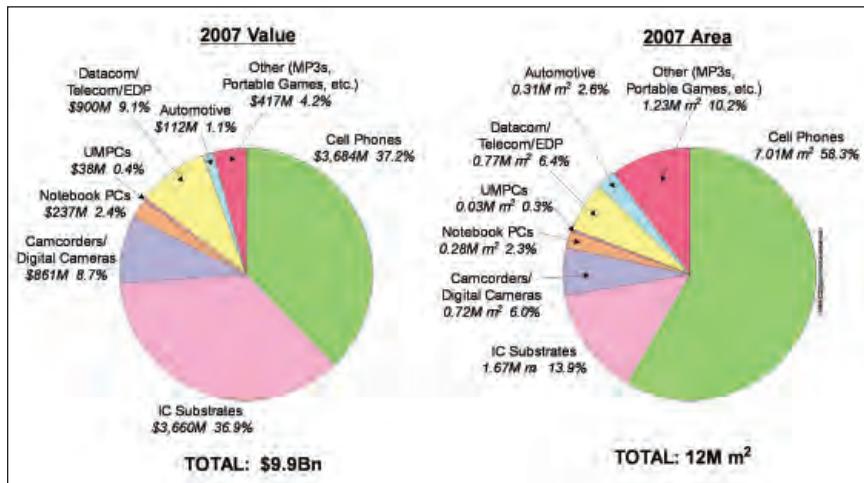


FIGURE 20: Buildup Microvia Printed Circuit Boards and Substrate 2007 HDI Application (Source: Prismark Partners, www.prismark.com)

The HDI Market

Incorporating the platform definition put forth in this book will also increase the market size and potential.

Features that enable HDI are now mainstream requirements in both the printed circuit board and chip packaging industries.

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3

Design of Advanced Printed Circuits (HDI)

By Happy Holden — *Mentor Graphics*

HDI Standards, Guidelines, Specifications, and References

The logical place to start when discussing HDI design is with the IPC Guidelines, Standards and Specifications (www.ipc.org). Four of these specifically apply to HDI design:

- **IPC/JPCA-2315**, Design Guide for High-density Interconnect Structures and Microvias
- **IPC-2226**, Sectional Design Standard for High-density Interconnect (HDI) Printed Boards
- **IPC/JPCA-4104**, Qualification and Performance Specification for Dielectric Materials for High-density Interconnect Structures (HDI)
- **IPC-6016**, Qualification and Performance Specification for High-density Interconnect (HDI) Structures

These four will be discussed briefly as a review and in context to specific HDI design methodologies.

IPC-2226: This specification educates users in microvia formation, selection of wiring density, selection of design rules, interconnecting structures, and material characterization. It is intended to provide standards for use in the design of printed circuit boards utilizing microvia technologies.[1]

IPC-4104: This standard identifies materials used for high-density interconnect structures. The IPC-4104 HDI Materials Specifications contain the slash sheets that define many of the thin materials used for HDI. Material characteristics are the number one factor in high-performance multilayers. The most important step in HDI design is still the selection of materials which will determine performance and fabrication technology. When designing HDI, there is an increasing array of new materials available that are not available for conventional multilayers. The slash sheets of material characteristics are divided into three main material types: Dielectric Insulators (IN), Conductors (CD), and Conductor and Insulators (CI).

These insulator materials come in four varieties:

- **Copper clad resins** (RCF, polyimide film, etc)
- **Laminates** (reinforced epoxy, Cyanate Ester, etc.)
- **Liquids** (epoxies, photosensitive, BCBs, etc.)
- **Films** (un-reinforced epoxy, liquid crystal polymers, etc.)

From a mechanical standpoint, materials may be grouped as reinforced and non-reinforced laminates and prepgres.

Reinforced materials are generally better in dimensional stability, lower in coefficient of thermal expansion (CTE), and less sensitive to thermal cracking, while the non-reinforced materials often have a lower dielectric constant (Dk), are thinner, and may be photo-imageable.

A number of different reinforced and non-reinforced materials enable further miniaturization in the high-reliability market segment, as well as in consumer electronics. Glass reinforced laminates and resin-coated copper foils (RCF) are the most popular HDI materials. Additional details can be found in the Chapter 5 - HDI Materials in this book.

Acceptability of these materials is defined by visual properties, dimensional requirements, mechanical requirements, chemical requirements, electrical requirements, and environmental requirements. A series of specifications (slash sheets) are defined for specific available materials. Each sheet outlines engineering and performance data for materials used to fabricate high-density interconnecting structures. These materials include dielectric insulator, conductor, and dielectric/conductor combinations. The slash sheets are provided with letters and numbers for identification purposes. To start the ordering process, one can use the slash sheets in the IPC-4104 document in combination with relevant IPC documents for each material set (e.g., IPC-CF-148, IPC-MF-150, IPC-4101, IPC-4102, IPC-4103, etc.)[1]

IPC-6016: This document contains the general specifications for high-density substrates not already covered by other IPC documents, like IPC-6011, the generic PWB qualification and performance specifications. The acceptance criteria of HDI layers are organized into slash sheet categories:

- **Chip Carrier**
- **Hand Held**
- **High Performance**
- **Harsh Environment**
- **Portable**

The acceptability requirements are broken down into individual specifications:

- 3.1 General**
- 3.2 Materials**
- 3.3 Visual Examination**
- 3.4 Dimensional Requirements**
- 3.5 Conductor Definition**

- 3.6 Structural Integrity
- 3.7 Other Tests
- 3.8 Solder Mask
- 3.9 Electrical Properties
- 3.10 Environmental Requirements
- 3.11 Special Requirements
- 3.12 Repair

Basic HDI Structures

In order to efficiently interconnect array packages with high I/Os, a new methodology needed to be developed. Although terms such as sequential multilayer or Buildup Multilayer (BUM) have surfaced in the last few years, the real benefit of HDI is in the very small holes identified as microvias. The HDI Design Committee of the IPC has identified a microvia as any hole equal to or less than 150 microns. That's six one-thousandths of an inch. In fact, the language of the new

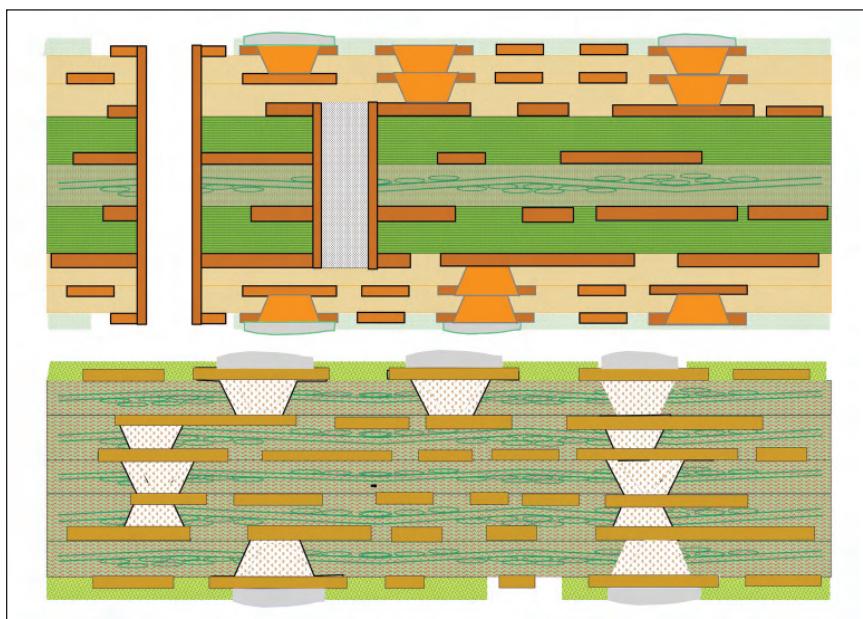


FIGURE 1: The two main structures of HDI boards

package technology is becoming more and more slanted toward microns with both conductors and holes being described in terms of microns (micrometers) or millimeters. The two basic HDI structures that exist are the “buildup” or “sequential buildup” structures and the “any-layer” structures. These two can be seen in Figure 1.

IPC/JPCA-2315 HDI Design Guide

As mentioned, IPC-2315 contains a good number of HDI design tutorials. After a brief overview of HDI structures and microvias, the bulk of the document is designed for the user who may be unfamiliar with HDI design. The first key document is the 2315 flowchart. This is seen in Figure 2 and provides an outline for the rest of the guide.

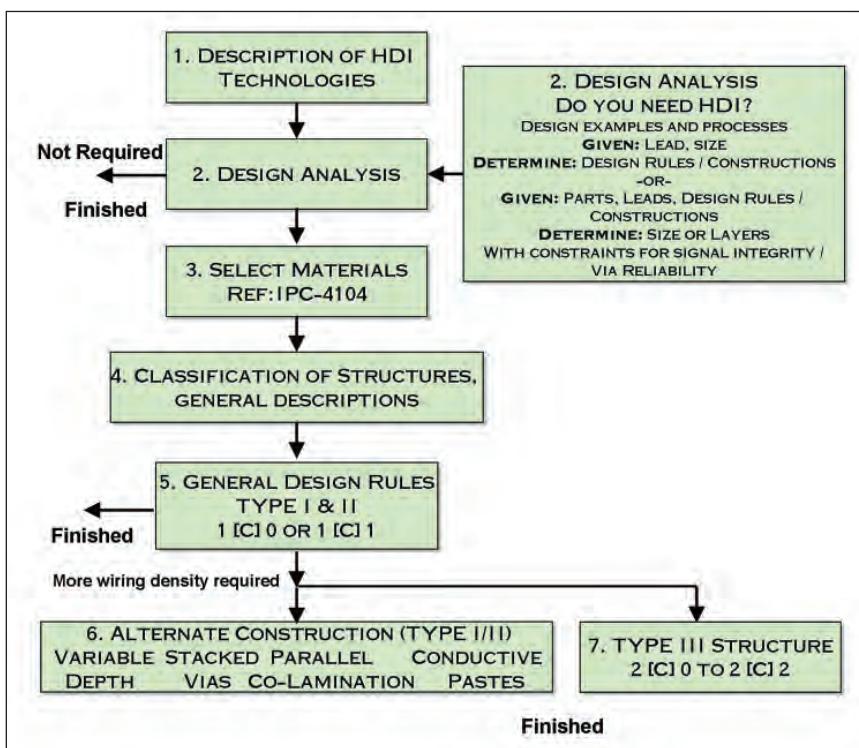


FIGURE 2: Tutorial and design rule flowchart for IPC-2315 [1]

HDI Wiring Requirements

Printed circuit design and layout are processes that require a great deal of discipline and order, while benefiting from creativity. The IPC standards provide some of that discipline, but are basically recommendations. They are the best we have to-date and are always undergoing review and updating.

IPC-2226 HDI Design Standard

The structure of the high-density interconnection is by type. They are: Type I, Type II, Type III, Type IV, Type V, and Type VI characteristics. However it is important to identify that there might be a different type of construction on which the added microvia material would be identified. Thus, the following definitions apply to all HDIs:

TYPE I 1 [C] 0 or 1 [C] 1, with through-vias from surface to surface

TYPE II 1 [C] 0 or 1 [C] 1, with buried vias in the core and may have through-vias connecting the outer layers from surface to surface

TYPE III ≥ 2 [C] ≥ 0 , two or more HDI layers added to through-vias in the core or from surface to surface

TYPE IV ≥ 1 [P] ≥ 0 where P is a passive substrate with no electrical connecting functions

TYPE V Coreless constructions using layer pairs

TYPE VI Alternate constructions of coreless construction using layer pairs

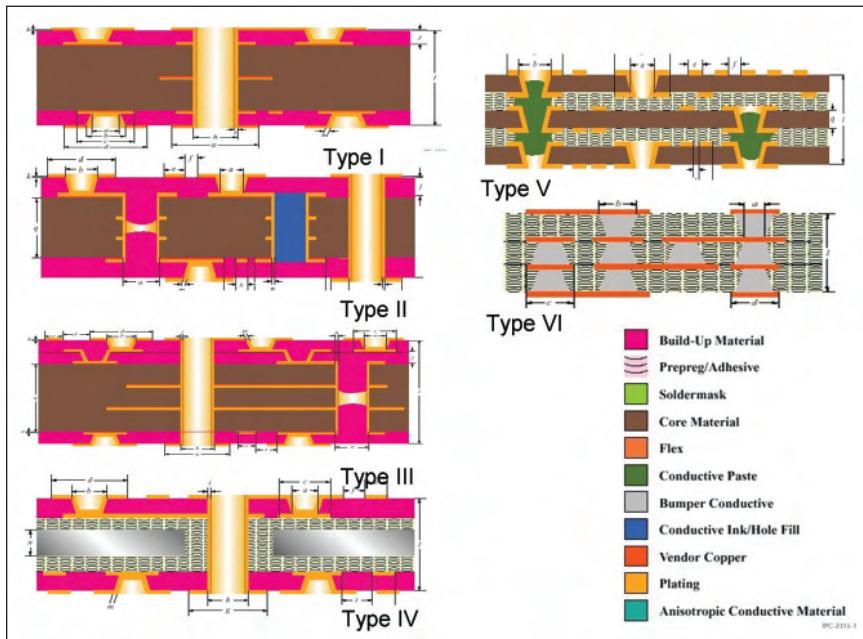


FIGURE 3: IPC-2226 six types of HDI structures[1]

Type I Constructions: 1[C]0 or 1[C]1

This construction describes a high-density interconnect substrate in which there are both plated microvias and plated through-holes used for interconnection. Type 1 constructions describe the fabrication of a single microvia layer on either one 1[C]0 or both sides 1[C]1 of an underlined PWB substrate core. The PWB core substrate is typically manufactured using conventional PWB techniques. This substrate may be rigid or flexible. The substrate can have as few as one circuit layer or be as complex as a prefabricated multilayer PWB with buried vias. A single layer of dielectric material is then placed on top of the core substrate. Microvias are formed in the dielectric connecting layer 1 to layer 2 and layer n to layer n-1. Through-holes are then drilled connecting layer 1 to layer n. The microvias and through-holes are then metallized or filled with conductive material. Layer 1 and layer n are circuitized and fabrication is completed.

Type II Constructions: 1[C]0 or 1[C]1

Type II has the same HDIS layers as Type 1. The difference is the core, [C]. Type 2 allows the through-vias to be placed in the core before the HDI layers are applied. The processes are the same except for the core through-vias being filled before the HDI layers are applied.

Type III Constructions: $\geq 2[C] \geq 0$

This construction describes a high-density interconnect substrate in which there are both plated microvias and plated through-holes used for interconnection. Type 3 constructions describe the fabrication of two microvia layers on either one 2[C]0 or both 2[C]2 sides of an undrilled PWB substrate core. The PWB core substrate is typically manufactured using conventional PWB techniques. This substrate may be rigid or flexible. The substrate can have as few as one circuit layer or can be as complex as a prefabricated multilayer PWB with buried vias. A single layer of dielectric material is then placed on top of the core substrate. Microvias are formed in the dielectric connecting layer 2 to layer 3 and layer n-1 to layer n-2. This first microvia layer is either metallized or filled with conductive material and then circuitized. A second layer of dielectric material is then placed on top of this circuitized layer and microvias are formed connecting layer 1 to layer 2 and layer n to layer n-1. Through-holes are then drilled connecting layer 1 to layer n. The microvias and Through-holes are then metallized or filled with conductive material. Layer 1 and layer n are circuitized and fabrication is completed.

Type IV Constructions: 1 [P] 0 or 1 [P] 1 or >2 [P] > 0

This construction describes a high-density interconnect substrate in which the microvia layers are used as redistribu-

tion layers over an existing drilled and plated passive substrate. The PWB or metal core substrate is typically manufactured using conventional PWB techniques. This substrate may be a rigid or a flexible substrate.

Type V Constructions: 1 [P] 0 or 1 [P] 1 or >2 [P] > 0

This construction describes a high-density interconnect substrate in which the microvia layers are used as redistribution layers over an existing drilled and plated passive substrate. The PWB or metal core substrate is typically manufactured using conventional PWB techniques. This substrate may be a rigid or a flexible substrate.

Type VI Constructions: 1 [P] 0 or 1 [P] 1 or >2 [P] > 0

This construction describes a high-density interconnect substrate in which the microvia layers are used as redistribution layers over an existing drilled and plated passive substrate. The PWB or metal core substrate is typically manufactured using conventional PWB techniques. This substrate may be a rigid or a flexible substrate.

Design rules

The designer should be aware that not all fabricators have equal capabilities in the areas of fine-pitch imaging, etching, layer-to-layer alignment, via formation, and plating. For this reason, the HDI design standard categorizes design rules into three categories, nominally A, B, and C with A being the easiest to produce and C being the most difficult. Selection of more stringent design standards will limit the number of fabricators capable of producing a particular board. Circuits produced with design rules in the 'A' category will be easier to produce, have higher yields, and can therefore be fabricated

Design of Advanced Printed Circuits (HDI)

Table 5-1 Typical Feature Sizes for HDI Construction, μm [mil]

Symbol	Aspect Ratios	Level A	Level B	Level C
		$\leq 5:1$ $(k+j)/a$	$>5:1$ to $1:1$ $(k+j)/a$	$>1:1$ $(k+j)/a$
	Through via hole aspect ratio	$\leq 5:1$ $(2k + \text{Board Thickness})/h$	$>5:1$ to $9:1$ $(2k + \text{Board Thickness})/h$	$>9:1$ $(2k + \text{Board Thickness})/h$
	Buried via aspect ratio	$\leq 5:1$ $(2r+q)/o$	$>5:1$ to $9:1$ $(2r+q)/o$	$>9:1$ $(2r+q)/o$
	Feature	Level A	Level B	Level C
a	Microvia plating aspect ratio (as formed, no plating)	102 μm [4 mil]	76 μm [3 mil]	51 μm [2 mil]
b	Microvia diameter at capture land (as formed, no plating)	152 μm [6 mil]	127 μm [5 mil]	76 μm [3 mil]
c	Microvia target land size = [(a + 2x annular ring) + FA ⁽¹⁾]	406 μm [16 mil]	330 μm [13 mil]	229 μm [9 mil]
d	FA for c =	203 μm [8 mil]	152 μm [6 mil]	102 μm [4 mil]
e	Microvia capture land size = [(b + 2x annular ring) + FA ⁽¹⁾]	406 μm [16 mil]	330 μm [13 mil]	229 μm [9 mil]
f	FA for d =	203 μm [8 mil]	152 μm [6 mil]	102 μm [4 mil]
g	Internal conductor trace width	127 μm [5 mil]	75 μm [3 mil]	50 μm [2 mil]
t	Internal conductor spacing	127 μm [5 mil]	100 μm [4 mil]	50 μm [2 mil]
e	External conductor trace width	127 μm [5 mil]	75 μm [3 mil]	45 μm [1.77 mil]
f	External conductor spacing	127 μm [5 mil]	100 μm [4 mil]	45 μm [1.77 mil]
h	Through via land size = [(h + 2x annular ring width) + FA ⁽¹⁾]	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221
i	Through via diameter (as formed, no plating)	See Table 5-2	See Table 5-2	See Table 5-2
j	Minimum through via hole wall plating thickness	See IPC-2221, Table 4-3	See IPC-2221, Table 4-3	See IPC-2221, Table 4-3
k	Dielectric thickness (HDI blind microvia layer) ⁽²⁾	64	64 μm [2.5 mil]	<50 μm [2 mil]
m	External Cu foil thickness (if Cu foil utilized)	1/2 oz (See IPC-2221, Table 10-2)	3/8 oz (See IPC-2221, Table 10-2)	1/4 oz (See IPC-2221, Table 10-2)
m'	Minimum blind microvia hole plating thickness	10 μm [0.3937 mil]	10 μm [0.3937 mil]	15 μm [0.5906 mil]
n	Minimum buried via hole wall plating thickness	10 μm [0.3937 mil]	10 μm [0.3937 mil]	15 μm [0.5906 mil]
o	Buried via diameter (as formed, no plating)	See IPC-2221, Table 9-4	See IPC-2221, Table 9-4	See IPC-2221, Table 9-4
p	Buried via land size = [(o + 2X annular ring) + FA ⁽¹⁾]	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221
q	Buried via core thickness (excluding outermost conductors)	76 μm [3 mil]	63 μm [2.5 mil]	<63 μm [2.5 mil]
r	Buried via Cu foil thickness (outermost layer)	1/2 oz (See IPC-2221, Table 10-2)	3/8 oz (See IPC-2221, Table 10-2)	1/4 oz (See IPC-2221, Table 10-2)
u	Core board thickness (excluding conductors)	75 μm [3 mil]	63 μm [2.5 mil]	<63 μm [2.5 mil]
	Staggered via pitch	(p+c)/2	(p+c)/2	(p+c)/2

1. F.A. = Fabrication Allowance which considers production master tooling and process variations required to fabricate printed boards.

2. Measured from top surface of Layer 2 Cu to bottom surface of Layer 1 Cu.

FIGURE 4: IPC-2226 design rules categories, Table 5-1, Table Feature Sizes for HDI Construction[1]

at a lower cost. To keep costs to a minimum, the design rules most appropriate for the application should be selected.

Level A

This specification allows conventional HDI processes to be used with relaxed tolerances. It should have the highest yield and lowest cost. It is estimated that 95% of fabricators can meet these design rules.

Level B

This is the conventional HDI process. It is estimated that 60% of suppliers can meet these design requirements under normal production conditions.

Level C

These rules require smaller panels and more exotic fabrication techniques. They are generally required only in electronic package, chip on board (COB) or SiP applications. At present, yields are low and costs are high. It is estimated that less than 5% of all fabricators can achieve these design rules in limited production or research and development volumes.

Typical HDI design rules are seen in Figure 4 from the IPC-2226 Design standards for HDI and Microvias. The Type I-VI HDI structures and recommended design rules for Levels A, B, and C. Since this is only a recommendation, it should be replaced with the actual fabricator's version of Table 5-1 to insure capability. Verification of design rules as well as qualifications are covered in Chapter 12 - *Quality, Acceptability and Reliability*.

Additional Structures

IPC-2226 also has more complex HDI structures (see Figure 5). The list below is from Section 5 in the document:

- **Variable Depth**
- **Stacked Vias**
- **Co-Lamination**
- **Complex Type III**
- **Conductive Inks**

Electrical Properties

Section 6 of IPC-2226 discusses electrical properties. The

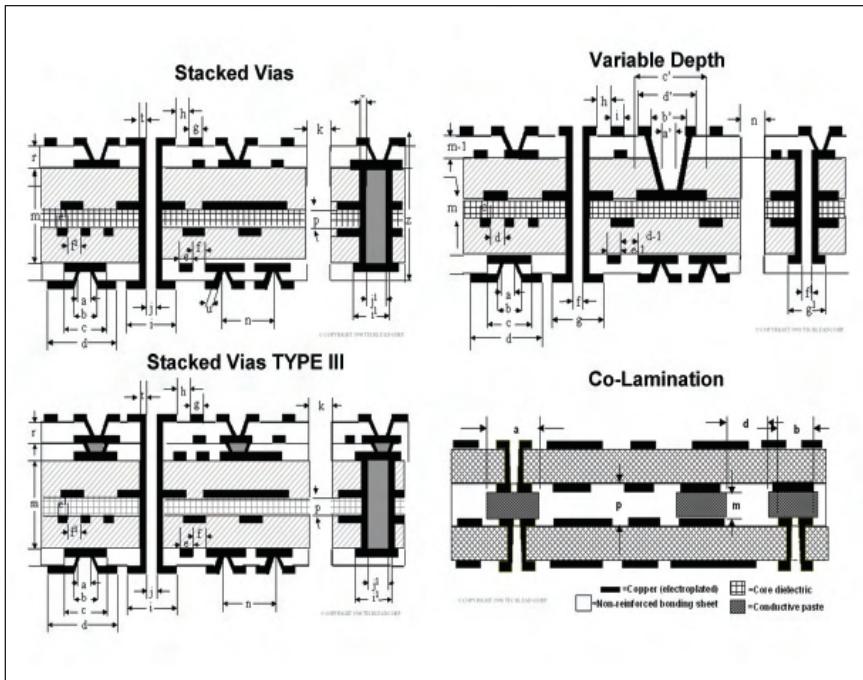


FIGURE 5: Additional HDI structure diagrams from IPC-2315[1]

characteristic impedance of single ended microstrips, strip-lines, coplanar, and differential signals is determined by the material's dielectric constant and the board's thickness stack-up and design rules. Signal attenuation is a function of the material's dielectric loss, design rules, and trace length. Various types of noise (ground bounce, switching noise, power supply spikes, etc.) including cross talk are a function of power supply coupling through the board's stack-up, ground layers, design rules, and material characteristics.

Thermal Management

Section 7 of IPC-2226 involves thermal issues. The thinner dielectrics that go with microvias are an aid to thermal dissipation. The new films and liquid dielectrics also allow better thermal properties than may be found with conventional laminates.

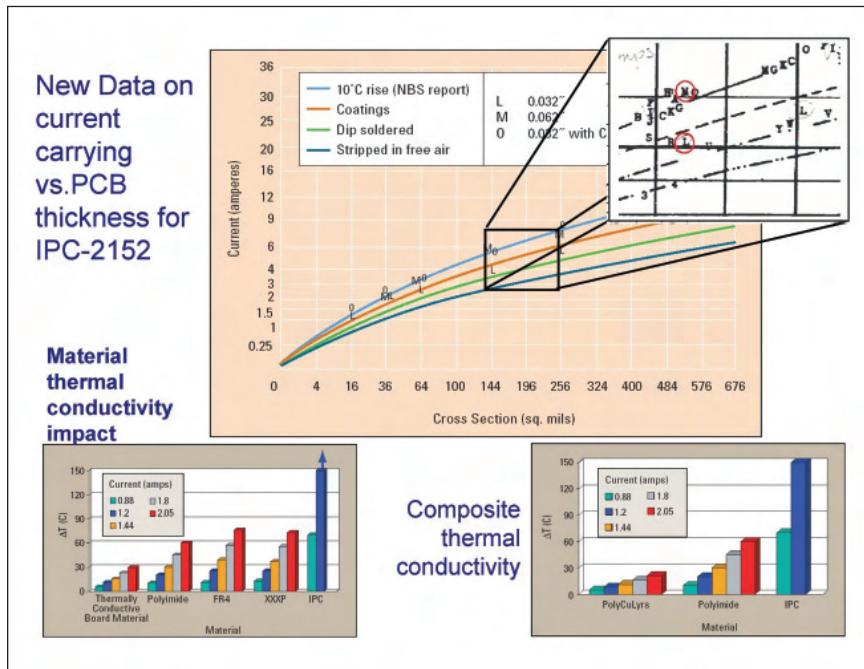


FIGURE 6: This figure illustrates: a. new data on current carrying capacity for IPC-2152; b. material thermal conductivity influence; and c. composite thermal conductivity.

The current work going on with IPC-2152, the Current Carrying Capacity is seen in Figure 6a. The original IPC curves in IPC-2221 were derived from 1954 NIST single-sided phenolic boards. As seen in Figures 6b and 6c, the IPC information is very conservative and sometimes four times higher than test measurements have revealed.

Component and Assembly Issues

Section 8 discusses component assembly issues which follow the IPC-2221 generic standard. Flip-chip lands, I/O capability of square body sizes, and bump options are discussed. Various other package land options, as well as land pattern design and footprints, are highlighted.

Design of Advanced Printed Circuits (HDI)

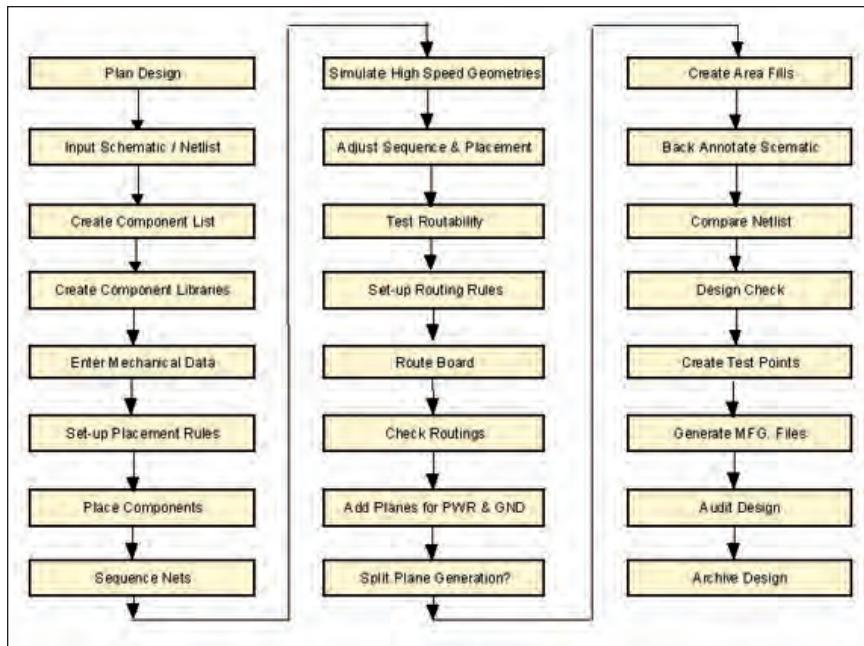


FIGURE 7: A detailed HDI design process with special note of new design activities and analysis steps

Holes/Interconnections

Section 9 involves holes, lands, and minimum annular rings. There is a discussion of the various ways microvias are formed and what the cross section can look like. Sections cover staggered and stacked microvias, as well as variable depth microvias.

Section 10 recaps the Wiring Factor and escape calculations of IPC-2315.

The General Process of PCB Design

The process of PCB design utilizing HDI technology is shown in Figure 7. When designing with HDI technologies, the first step, Plan Design, is the most important. Routing efficiencies for HDI are dependent on stack-up, via architecture, parts placement, and BGA fanout and design rules. However,

the entire HDI Value Delivery Chain must be taken into consideration, including fabrication yields, assembly considerations, and in-circuit tests.

More on HDI Value Delivery Chain

System Partitioning for HDI Products

HDI PCBs start with OEMs that design them into their products. The OEM has to manage and accomplish the HDI Value Delivery System. The first two links in the chain are system partitioning and circuit design.

HDI, as a new, emerging interconnect technology, presents a number of challenges to the OEM. Forty years of printed circuit history does not prepare one to understand how blind and buried microvias can contribute to a product's success. Never-

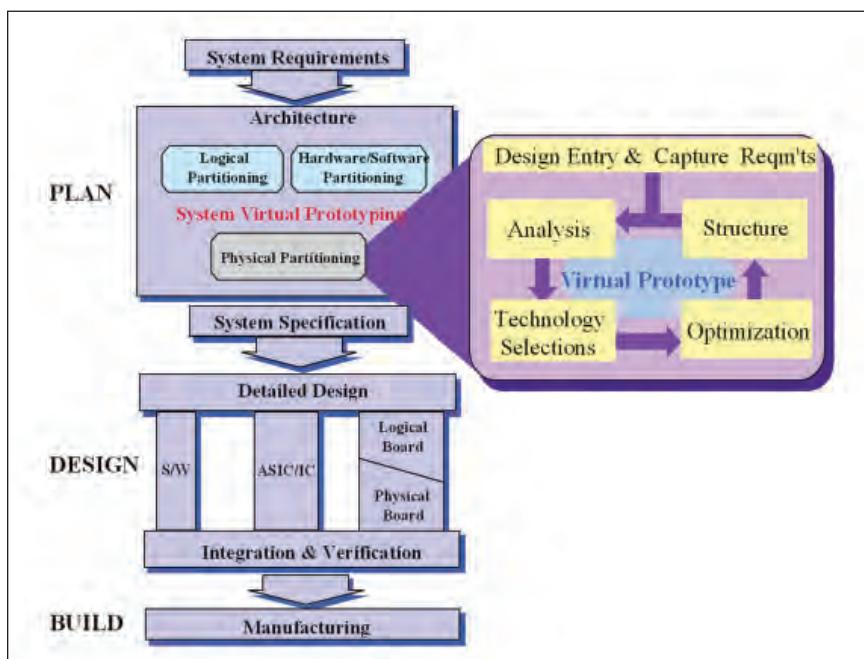


FIGURE 8: System partitioning concepts of Virtual Prototyping [Source:SavanSys (www.savansys.com)]

Design of Advanced Printed Circuits (HDI)

theless, partitioning is the architectural step that allows for the translation of system requirements into system specifications. Like Figure 8 illustrates, if the logical partitioning, hardware/software partitioning, and physical partitioning cannot be done for an HDI approach, it will not be used in products.

The successful employment of HDI requires a *What if?* approach. Fabricators need to be able to do a virtual prototyping of the system, using the processes of analysis, technology selection, optimization, and structure.

The process goes on until the *what ifs?* balance. There are a wide variety of predictive design alternatives:

ANALYSIS	
Manufacturing cost modeling	Manufacturability assessment
Performance estimation	Test prediction
Wiring / routing analysis	Post-manufacturing activities
TECHNOLOGY SELECTION	
Components	Packages
Substrates	Connectors
Materials	Manufacturing process flows
OPTIMIZATION	
Objective function	Constraints and requirements
Allocation and budgeting	Utility functions
Prioritization	
STRUCTURE	
Topology	Disconnection
Partitioning	Reuse
Placement	

By using a predictive engineering framework, HDI structures can deliver performance, size, and cost advantages.

HDI PCB Design

The third link in the chain is PCB design and layout. If you look at Figure 9, which I call the expanded electronic product realization process, the PCB design portion is comprised of Trade-off Analysis, Physical CAD, Design Synthesis with FPGA Trade-offs, Circuit Simulation, and Manufacturability Audit.

PCB design of HDI structures presents a number of new challenges to the OEM. Microvias are used in the land pattern of components to save space and reduce electrical parasitics. However, this means that often component libraries must contain those vias. Many CAD systems do not allow that assignment. HDI can also have very complex via structures, with different via pad diameters in the same stack-up. The via structure also has to match manufacturing capability, so the vias are stacked, offset, or staggered which places new demands on autorouters. If a mass microvia generation process is being used, the number of vias and their diameters are not key in manufacturing costs. The autorouter needs to be able to set

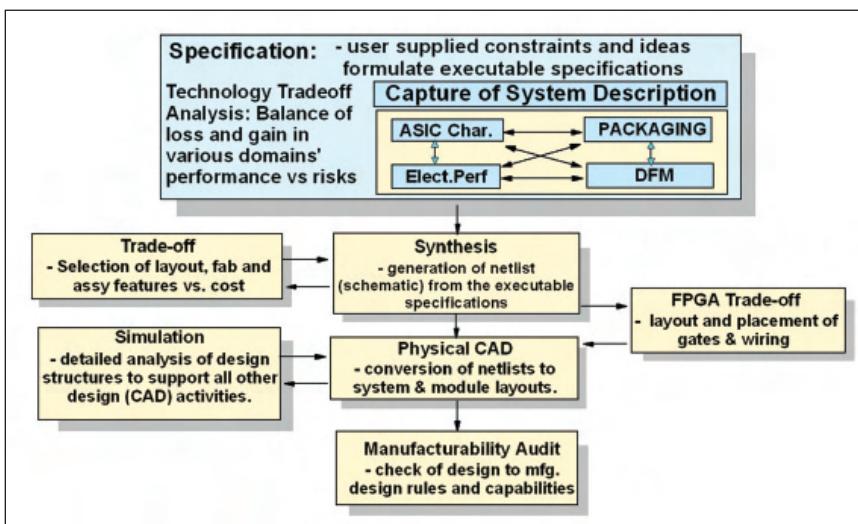


FIGURE 9: Product realization modules for PCB layout and design

the value of the via to zero and use as many vias as it needs to simplify the design. Autorouters typically try to minimize the number of vias.

Trade-off Analysis

After the product has been partitioned, the circuit designed, and the components selected, the physical design needs to be planned with an eye toward maintaining the lowest manufacturing costs while meeting all the performance and operating boundary conditions. This is especially true for HDI designs. Conventional through-hole PCB design has not changed too much in the last forty years. Finer geometries, more layers, and surface mounting have been added, but the process remains essentially unchanged. Microvias and HDI have made many changes and require new design rules and layer structures. Experience and history will not help here. The unfortunate truth about printed circuit layout is that there is an almost infinite number of combinations of layer structures and design rules that can be used to implement the schematic and bill of materials. With all of these choices, especially the new ones that HDI offers, a trade-off tool is required to find the best set of design rules and features that will allow the rapid design of the printed circuit, be producible, and meet all the performance expectations, while providing the lowest total manufacturing cost. Since the actual design has not yet been completed, these tools require predictive models that can anticipate cost and performance. Several of these tools are available on the market and even more have been developed by companies for their own use. One such predictive tool is called the design report card and I will outline it for PWB fabrication, PCB assembly, and assembly test in a future chapter.

Balancing the Density Equation

Printed circuit design and layout are creative processes that have profound implications for electronic products. With the need for more parts on an assembly or the trend to make things smaller to be portable or for faster speeds, the design process is a challenging one. The process is one of “balancing the density equation” with considerations for certain boundary conditions like electrical and thermal performance. Unfortunately, many designers do not realize that there is a mathematical process to the layout of a printed circuit. Let me briefly explain. The density equation, as seen in Figure 10 has two parts, the left side, which is the Component Wiring Demand, and the right side, which is the Substrate Wiring Capability.

Component Wiring Demand

Wiring demand is the total connection length required to connect all the parts in a circuit. When you specify an assembly size, you create the wiring density in inches per square inch (or cm per square cm). Models early in the design plan-

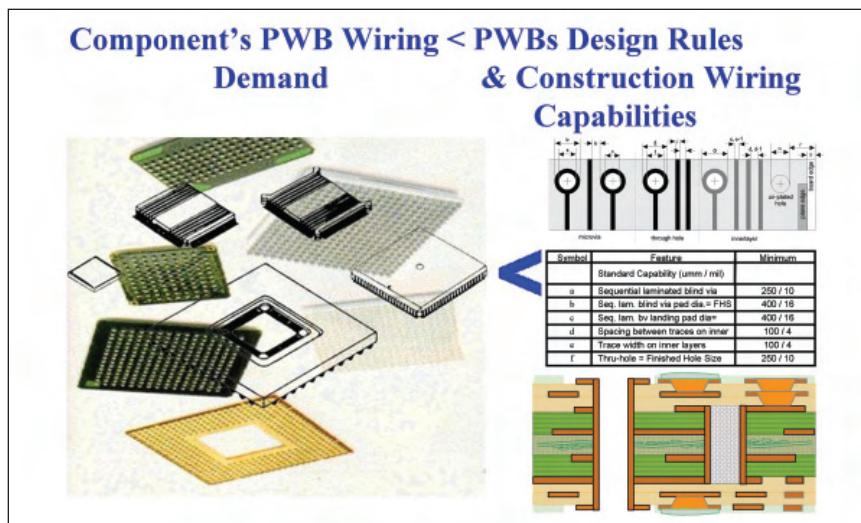


FIGURE 10: The designer challenge: “Balancing the Density Equation”

ning process can estimate the wiring demand. Three factors can affect the maximum wiring demand:

- The wiring required to break out from a component like a flip-chip or chip scale package
- The wiring created by two or more components tightly linked, say a CPU and cache or a DSP and its I/O control
- The wiring demanded by all integrated circuits and discretes collectively

There are models available to calculate the component wiring demand for all three factors. Since it is not always easy to know which factor controls a particular design, you usually have to calculate all three to see which one is the most demanding and thus controls the layout. The models I find most useful for all three can be found in Chapter 19 of Coomb's "PCB Handbook-6th Edition." [2]

Substrate Capability

Substrate wiring capability is the wiring length available to connect all the components. It is composed of three factors:

- **Design Rules** – the traces, spaces, and via lands, keep-outs, etc., that make up the surface of each layer
- **Structure** – the number of signal layers and the combination of through, blind, and buried vias that permit interconnection between layers and the complex blind, stacked, and variable depth vias available in HDI technologies
- **Layout Efficiency** – the percentage of capacity from design rules and structure that a designer can deliver on the board

These three factors determine how much wiring is available on the substrate to meet the wiring demand. The data is straightforward except for layout efficiency. Layout efficiency is a little-used factor that expresses what percentage of wiring capacity can be used in the design. The equation for substrate capacity for each signal layer is below. The total substrate capacity is the sum of all the signal layers:

$$W_c \text{ (Wiring Capacity)} = E t / g$$

(in/sq in, for each signal layer)

Equation 5

Where:

E = Layout efficiency

t = number of traces per grid area or distance between
two via pads

g = grid size or length between centers of via pads above

Layout Efficiency

Layout efficiency is the percentage of capacity from design rules and structure that a designer can deliver on the board.[3] Layout efficiency is the ratio of the actual wiring density it takes to wire up a schematic to the maximum wiring density

TABLE 3.1: Typical layout efficiencies

DESIGN SCENARIO	CONDITIONS	EFFICIENCY*
TH, Rigid	Gridded CAD	6 - 8%
Surface Mount / mixed	w/wo back side passives, gridless CAD	7 - 10%
Surface Mount / mixed	w/ back side actives, gridless CAD	8 - 13%
Surface Mount only	w/wo back side passives, gridless CAD	up to 14%
Surface Mount / mixed	1 sided blind vias, gridless CAD	up to 20%
Surface Mount / mixed	2 sided blind vias, gridless CAD	up to 24%
Built-up technologies [3]	2 sided micro-blind vias, gridless CAD	up to 30%

* Determined from analysis of printed circuit designs, using actual wiring capacity from CAD system divided by maximum wiring capacity (Equation 5).

or W_d divided by W_c . For ease of calculations, layout efficiencies are typically assumed to be 10%. Table 3.1 provides a more detailed selection of efficiencies.

Wiring Demand vs. Substrate Capacity

Four conditions can exist between wiring demand and substrate capacity:

Wiring Demand > Substrate Capacity: If the substrate capacity is not equal to the demand, the design can never be finished. There is either not enough room for traces or for vias. To correct this, either the substrate has to be bigger or components have to be removed.

Wiring Demand = Substrate Capacity: While optimal, there is no room for variability and to complete the design will take an unacceptable amount of time.

Wiring Demand < Substrate Capacity: This is the condition to shoot for. There should be enough extra capacity to complete the design on time and with only a minimum of over-specification and costs.

Wiring Demand << Substrate Capacity: This is the condition that usually prevails. In PCB layout, the schedule is tight and timing is all-important. Many choose tighter traces or extra layers to help shorten the layout time. The impact of this is to increase the manufacturing costs 15 - 50% higher than necessary. This is sometimes called the “sandbag approach.” It is unfortunate, since the models above would help to create a more planned environment.

The key to meeting schedules and keeping manufacturing costs under control is Layout Performance Metrics (substrate capacity / wiring demand), an understanding of what is an optimum design, keeping track of how close you get to it, practice balancing the design equation, and doing *what ifs?*

FPGA Trade-Off

FPGA design optimization provides an opportunity for physical PCB layout optimization through the opportunity to:

- swap pins and banks on the FPGA to minimize trace lengths and crossovers and provide layout optimization. (Figure 11a);
- align PWR / GND / BUS pins in a mirror to allow secondary-side mounting using the same vias;
- orient the original chevron PWR/GND patterns to a boulevard pattern (Figure 11b).

These optimizations and trade-offs are usually provided by a co-design tool providing connectivity between FPGA and PCB software.[4]

Physical CAD

All modern PCB CAD systems can handle blind and buried vias. It is possible to design HDI boards by hand with these systems. Sometimes the libraries do not like via-in-pads and

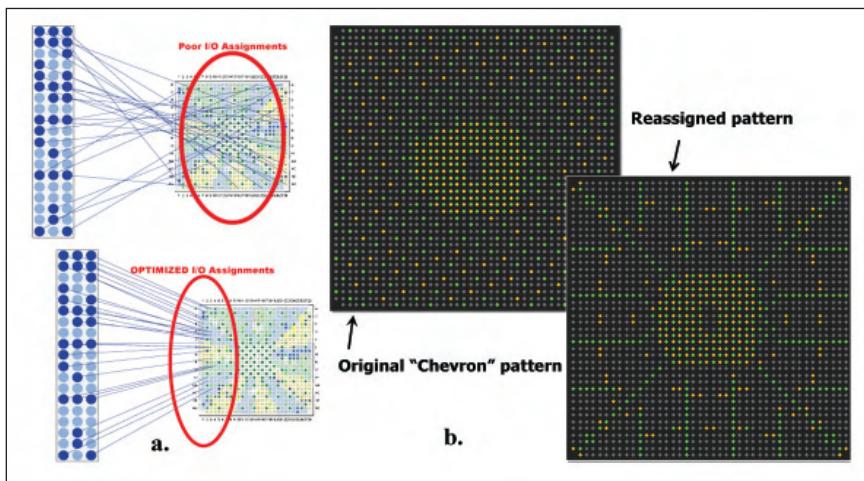


FIGURE 11: Reassigning pins on FPGA can improve routing by (a) moving entire banks along with pin swapping and (b) creating boulevards.[16]

Design of Advanced Printed Circuits (HDI)

the varying pad diameter in the same via stack-up, but the systems can be fooled to accept these design rules. Most high-performance CAD systems have features that can be used to design an HDI board, but we are talking here about common HDI boards that have evolved from through-hole boards. The autorouter can be tuned to HDI mass via generation processes like photodielectrics or chemical etching. Some autorouters design a different HDI board under these circumstances than they would when tuned for a laser drill or microvias that were stacked or of variable depth.

After fanout of BGAs, the autorouter is the major feature that needs to be improved when designing HDI. A partial list of key features for an HDI autorouter and CAD system includes:

- Optimization of mixed via by autorouter
- Staggered via control (crankshaft, zipper, etc.)
- Autorouter cost budget for mass via generation processes
- Via-in-pad control
- Buried/blind via control on layers (variable depth blind vias, stacked vias)
- Breakout patterns (or rather, breakthrough patterns)
- Via pad stack control (landless vias)
- Stepping down to power (planes), minimizing through-vias
- Through-blind via/trace push-shove in manual routing
- Auto test point creation including, boundary scans; the pad, via to use, which side, grid, and spacing
- Pad within pad (blind via landing on through-via land)
- Buried components (screened / sheet resistors, donut resistors)
- Solid paste vias/colaminated vias
- Any angle routing
- EMI control (surface ground plane) via-in-pad
- Manufacturing process rule areas

Circuit Simulation

Fortunately, the modern design environment has numerous simulation tools to evaluate and validate design options. Electrical simulation for signal integrity, power integrity, timing, and EMI/RFI are available for the electrical functionality. Thermal simulation provides for temperature rise, heat flow, and cooling. Vibration, reliability, manufacturability simulation, and modeling are also available in the design phase.

Manufacturability Audit

Finally, a new generation of producibility audit software has come into the market that allows a PCB design to be checked before it is sent off to a fabricator. This can find costly mistakes such as a power wired to ground or a small island of copper that may etch away and create a short. These errors or poor selections can be easily changed and the design can be released to quickly pass through fabrication. A great deal of time and money is saved through the use of audit software. OEMs report that the payback in using audit software comes quickly.

A new generation of software was created to address critical mistakes in the PCB design file. You would expect that the design rule checkers or “right by design” features of CAD systems would find all the mistakes in a design. The unfortunate reality is that today’s PCB designs are so complex with surface mount technologies, signal integrity, thermal issues, and now, HDI, that many mistakes that will seriously affect manufacturing time and costs slip through. These mistakes are not just judgment calls, but are serious enough to halt or delay the fabrication of the substrate or the assembly. Using manufacturability audit software, most of these errors are found and can be corrected immediately. A partial list of the features that this type of software checks for is included here:

TABLE 3.2: Checklist for a Manufacturability audit

CAD database to Gerber netlist compare	Part-to-part clearance/automation
Annular ring error	Quality parts
Padstack checklist	Hole audit/lead diameter
Plane clearance errors	Surface mount part density
Manufacturability analysis & DRC	SMT height clearance
Thermal leg count violation	Allowable assembly machine span
Circuit checklist	Part-to-part spacing
Unterminated lines	Drill path optimization
Resist slivers	Automatic solder mask generation
Copper islands	Bare board test point analysis & additions
Solder mask checklist	In-circuit test point analysis
Solder short violations	In-circuit test checklist
Solder mask coverage	Boundary scan audit
Mask to via check	Test point management
Solder paste check	Design profile
Silkscreen clipping	Registration generator
Teardrop pad addition	Keep-out audit

The PCB design process is the most important financial step in the product development process. The specifications and design features determined at this point will control the ultimate manufacturing costs and, many times, its quality. Unfortunately, it is the least researched and least understood of any process we have in developing a new product.

HDI Fabrication, Assembly, and Test

What is required for the HDI Value Delivery Chain is a method of predicting the cost of fabrication of the HDI substrate, the assembly, and doing the assembly test. With these tools and the wiring density metrics, trade-offs can be performed early in the product's life. Many call this Design For

Manufacturing and Assembly, I call it the DFM Report Card because that is what its creator, Tucker Garrison[5], called it. With the two DFM Report Cards that I will outline here, a fairly accurate estimate can be made of the costs of a proposed design. Placed into a spreadsheet, this forms a powerful tool to select HDI parameters and hopefully to optimize a design.

Design for Manufacturing Report Cards

Fabrication Report Card

The fabrication report card is a matrix supplied by a PWB fabricator that relates the various design choices on a PWB to design points. These points are based on the actual prices a fabricator will charge for these features. Typical factors that fabricators use to price a printed wiring board are:

- size of the board and number that fit on a panel;
- smallest hole diameter;
- number of layers;
- solder mask and component legends;
- material of construction;
- final metallization or finish;
- trace and space widths;
- gold-plated edge connectors;
- total number of holes;
- design-specific features, etc.

Once the fabricator has collected the factors that influence his prices, he collects these costs and normalizes the figures with the smallest non-zero amount.

Predicting Productivity

The simple truth about printed circuit boards, multichip modules, and hybrid circuits is that the design factors, like

Design of Advanced Printed Circuits (HDI)

those listed previously, can have a cumulative effect on manufacturing yield. These factors all affect producibility. Specifications can be selected that may not adversely affect yields individually, but cumulatively can significantly reduce yields. A simple algorithm is available [7] that collects these factors into a single metric, in this case called the Complexity Index (CI). It is given in Equation 6:

$$CI = \frac{(\text{area}) (\# \text{ of holes}) (\# \text{ layers})}{(\text{min. trace width}) (\text{min. annular ring})} \times Z - \text{factor} \quad \text{Equation 6}$$

Where:

CL=Complexity Index

area= top area of the substrate to be designed (sq in)

holes= total number of holes, blind, buried, and through

trace width= minimum trace width on the substrate (in)

layers = total number of wiring layers in the substrate

annular ring= half the difference between the via land
diameter and the hole diameter (in)

Complexity Adjustment Table	Z-factors:
PTFE or Duroid	200
Aspect Ratio > 10	aspect ratio x 10
HDI (microvias)	10
Sequential lamination	6

First Pass Yield: The first pass yield equation is derived from the Weibull probability failure equations [6]. This equation is of a more general form of the equation typically used to predict ASIC yields by defect density and is given in Equation 7.

$$\text{First pass Yield (FPY)\%} = \frac{100}{e^{[(\log CI/A)^B]}} \quad \text{Equation 7}$$

To determine the constants A and B in Equation 7, a fabricator will need to characterize his manufacturing process by selecting a number of printed circuits currently being produced that have various complexity indexes, hopefully some low, some medium, and some high. The first pass yield (at electrical test without repair) of these printed circuits for several production runs are recorded. Any statistical software [6] program that has a model-based regression analysis can now determine A and B from this model:

$$\text{FPYestimate} = f[x] = 100, \text{EXP}\{\text{LOG}(\text{complexity index}, \\ \text{PARM[1]})^{\text{PARM[2]}}\}$$

Where x = Complexity Index, PARM[1] = A and PARM[2] = B

Constant A determines the slope of the inflection of the yield curve and constant B determines the x-axis point of the inflection. A detailed process is available in CircuiTree Magazine, Sept. 2005.[7]

Assembly Report Card

The metrics of assembly trade-offs relate factors of process, component selection, and test to assembly prices. Yields and rework are factored into the points of the Assembly Report Card. The point total provides an estimation of the relative prices of assembly and test.

The assembly report card is a matrix supplied by the PCB assembler. It relates various process assembly and test choices

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that the assembler provides along with various component sizes, orientation, complexity, and known quality to the costs of providing for these design choices. Typical factors that affect assembly costs are:

- One-pass or two-pass IR reflow
- Wave solder process
- Manual or automatic parts placement
- Odd shaped parts
- Part quality level
- Connector placement
- Test coverage
- Test diagnosability
- Assembly stress testing
- Repair equipment compatibility

By collecting all the costs associated with assembly, test, and repair and then normalizing these costs with the smallest non-zero value, a Report Card Matrix can be created. (See Chapter 19 of *Coomb's PCB Handbook-6th Edition*)[2]

Estimating Wiring Lengths

Seven wiring models are reported in the literature but the first three are most commonly used:

- Coors, Anderson & Seward Statistical Wiring Length[8]
- Toshiba Technology Map[9]
- H-P Design Density Index[10]

The other four wiring models include:

- Equivalent ICs per square inch[11]
- Rent's Rule[12]
- Section Crossing[13]
- Geometric Analysis[14]

Coors, Anderson & Seward Statistical Wiring Length

This wiring demand model is based on a stochastic model of wiring involving all terminals. The probable wire length is calculated based on the distance of a second terminal and the spatial geometry of all other terminals. This is the most recently determined wiring model and represents the most practical approximation of surface mounting technology. Equation 8 presents the mathematical model that results.

$$d = D * N_i / A \text{ (in / sq in)} \quad \text{Equation 8}$$

Where:

D = average interconnection distance (in)

N_i = total number of interconnections

A = routing area (sq in)

$$D = E(x) * G$$

$E(x)$ = expectation of occurrence

G = pad placement grid (in)

$$E(x) = \frac{1}{a} \left[\frac{((S-T)(Sa-2))e^{aS} + S(2-(S-T)a)e^{a(S-T)} - 2T}{(S-T)e^{aS} - Se^{a(S-T)} + T} \right] \quad \text{Equation 9}$$

Where: $S = M + N$, $T = (M^2 + N^2)^{.5}$, $a = \ln \alpha$

α = empirically derived constant = 0.94

M = board width of grid pt. = (width / G) + 1

N = board length of grid pt. = (length / G) + 1

$N_i = 2 * N_t / 3$

N_t = total number of component pins

Toshiba's Technology Map

The Packaging Technology Map [9] is a simple technique to predict a PWB, Chip-On-Board, or MCM-L wiring demand and its assembly complexity. By plotting components per sq in (or components per sq cm) against average leads per component on a log - log graph (Chapter 1, Figure 31), the Wiring Demand (WD) in inches per sq in (or cm per sq cm) and Assembly Complexity in leads per sq in (or leads per sq cm) can be calculated.

H-P's Design Density Index

Another metric is called the Design Density Index (DDI) [10]. It is a correlation of the actual design rules for a PWB compared to the DDIndex (Equation 10).

$$\text{DDI} = 13.6 \text{ (EIC/board area)}^{1.53} \quad \text{Equation 10}$$

Where:

Equivalent Integrated Circuits (EIC)= total component leads / 16

Board Area = top surface area of printed circuit board
(sq in)

This equation gives a good visual record of how efficient a company has been in PWB layout. As various PCBs are charted, their DDIs form a distribution which is a form of layout efficiency (e) since at the bottom of the distribution, more EICs are connected than at the top of the distribution.

Equivalent ICs Density

Equivalent Integrated Circuits (EIC) per unit area has been a traditional measure of density since the introduction of CAD

systems in the early 70s. A simple measure of the number of electrical connections required per unit area of the board, it remains in use with Surface Mount and is usually referred to as EIC Density. An EIC is the total number of leads of the components divided by 14 or 16, the old number of pins on a DIP. Many people also use 20 as a divisor. Equation 11 defines EIC density mathematically in ICs per sq cm (EIC/sq in).

$$\text{EIC Density} = \text{connections} / 16 / \text{Board Area} \quad \text{Equation 11}$$

Where:

Connections = total component leads

Board Area = top surface board area (in sq cm or sq in)

Rent's Rule

Rent's Rule is based on an estimation of the average interconnection length for a given design. The total wiring length required to connect a set of chips is predicted according to Equation 12.

$$d = (f/f+1) R(m) N_{io} F_b \text{ (in per sq in)} \quad \text{Equation 12}$$

Where:

$R(m)$ = average interconnection distance (in)

N_{io} = total number of interconnections

A = routing area (sq in)

N_c = expectation of occurrence

f = average fan out of ICs

$$R(m) = \frac{2}{9} \left[\frac{N_c^\beta - 0.5 - 1}{4^\beta - 0.5 - 1} - \frac{1 - N_c^\beta - 1.5}{1 - 4^\beta - 1.5} \right] \frac{1 - 4^\beta - 1}{1 - N_c^\beta - 1}$$

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Where:

$$F_b = A / R(m) \cdot 1.4; N_{io} = N_t + N_i$$

β = empirically derived constant = 0.6

N_c = number of ICs

N_t = number of terminal leads

N_i = number of terminal off board

Section Crossing

Developed by Sutherland and Oestreicher [13], this technique estimates the number of connections which must pass through various board cross sections. The number of wires, which cross the section, yields the probability of crossing multiplied by the total number of nets in the system:

$$F_i I_c L = N_{io}/n (1 - P_1 n - P_2 n) \quad \text{Equation 13}$$

Where:

$$P_1 = P_2 = 1/2$$

F_i = actual wiring efficiency

I_c = interconnect capacity

L = board length

N_{io} = total number of I/Os to be routed together

n = average number of pins per net (i.e. the fan out + 1)

P_1 = the probability that the wire starts on side 1 and connects only to pins on side 1

P_2 = the probability that the wire starts on side 2 and connects only to pins on side 2

Geometric Analysis

A geometrically based wiring estimation was first developed by Moresco.[14] It is based on an extended neighbor counting method similar to Seraphim. In Moresco's approach the wiring

requirement is computed by assuming that a fraction of the nets (A) are nearest neighbor routed and the rest of the nets (1-A) are globally routed.

$$Total \cdot wiring \cdot length = A \frac{N_{chip} N_{ioc} F_p}{2} + (1-A)(N_{chip} - 1)N_{chip} F_p + \frac{N_{ioe} F_p - N_{chip}}{v}$$

Equation 14

Where:

A = 1 is maximum parallelism, A = 0 is the minimum

N_{ioc} = number of signal and control I/O per chip

N_{ioe} = number of signal and I/O leaving the module

v = 2 for edge connector and 4 for an area array

connector on the bottom of the module

A = fraction of nets that are nearest neighbors
routed (0 < A < 1)

N_{chip} = number of chips in the module

F_p = wiring limited chip footprint dimension

What's Different in HDI Design

Three New Principles

There are three new principles for HDI microvia design that do not exist in through-hole design:

- Microvias must replace through-hole vias, not just be used in addition to TH vias.
- Consider new layer stack-ups that allow the elimination of through-hole vias.
- Place microvias in such a way that they create boulevards for improved routing.

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The main idea is that microvias replace or allow the removal of through-hole vias, thus allowing the routing density on inner-layers to improve by two or three times, using the space the through-hole vias used to occupy. This will allow fewer signal layers and fewer reference layers for those signal layers.

This last principle is more profound than it first appears. This is because there are three dimensions on how the microvias are placed:

- The blind-vias can be “shifted or swung” in the X-Y or theta (ϕ) angle to create more routing space.
- The blind-vias can be placed on inner-layer (3-D) to further create more breakout spaces.
- The center-to-center distance can be altered on inner-layers to provide additional space for traces.
- If all of this is happening on or near the Primary Side, then there will be space created under the BGA on the Secondary Side for traces or more important, for discretes like decoupling capacitors.

Microvias Replacing Through-Holes

If you study the first principle you may ask yourself, “What jobs do my vias do?” The answer is that the most common via on a PWB is the via to GND. This makes the second most common via obvious. It is the via to PWR. Thus, moving the GND plane that usually is layer 2 up to the surface provides the opportunity to eliminate all those vias to GND. In the same vein, moving the most used PWR plane up to layer 2 will replace those through-holes with blind vias. These provide four advantages over the conventional ‘microstrip’ stack-up:

- There are no fine-lines to plate or etch on the surface.

- The surface can be an unbroken GND pour to reduce EMI and RFI.
- The closer Layer-2 (PWR) is to Layer-1 (GND) the more planar capacitance is available and the lower the planar inductance is.
- The energy stored in the planar capacitance can be delivered to components with the lowest series inductance available.

Layer Stack-up Alternatives

Figure 12 shows some of the most common HDI stack-ups to reduce the number of through-hole vias. The three common HDI stack-ups are shown with the IPC-Type structures (I, II & III).

The possible dielectrics available between Layer-1 and Layer-2 can be conventional prepregs, laser-drillable prepregs, RCCs, reinforced RCCs, or BC cores. These materials are described in Chapter 5-Materials. If the dielectric is thin (as seen in Figure 13), then it is practical to also utilize a ‘skip-via’ from Layer-1 to Layer-3, thus saving the cost of not having to utilize

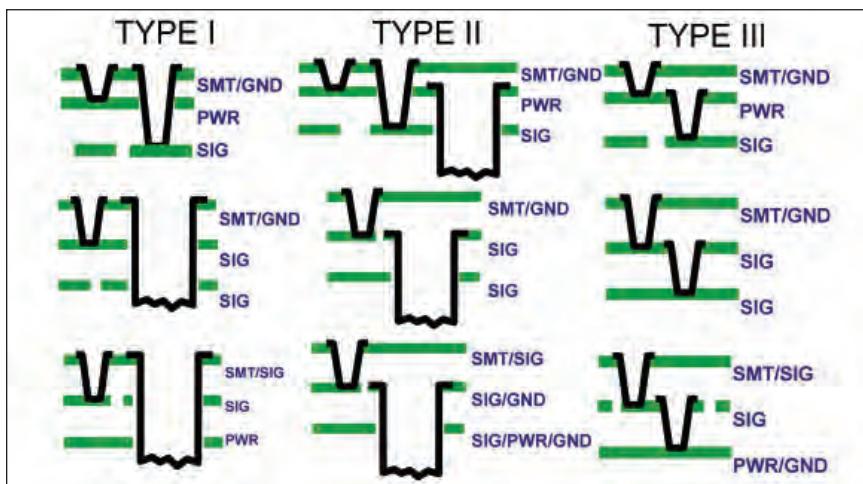
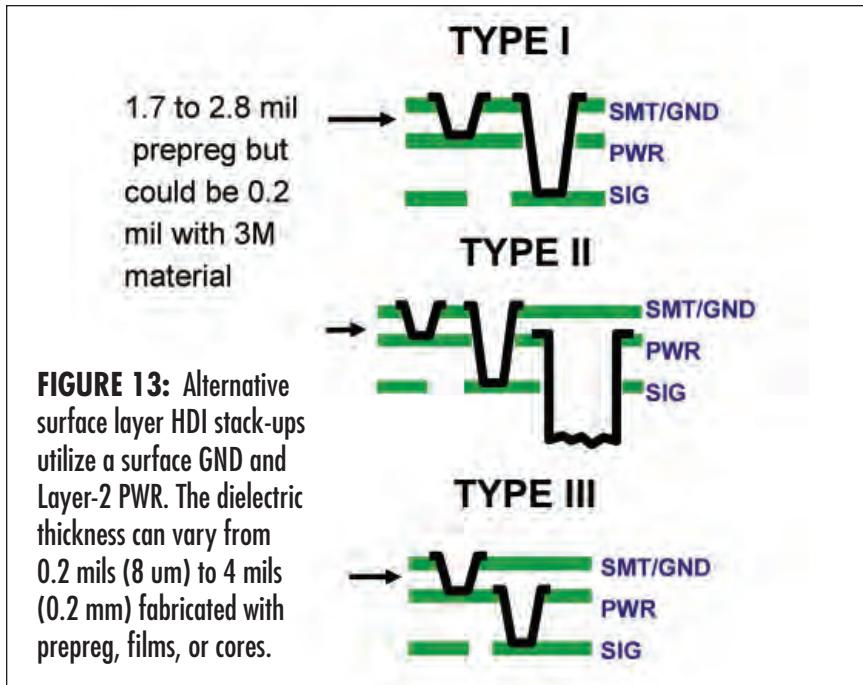


FIGURE 12: Three alternative surface layer stack-ups compared to IPC-Type I, II & III structures



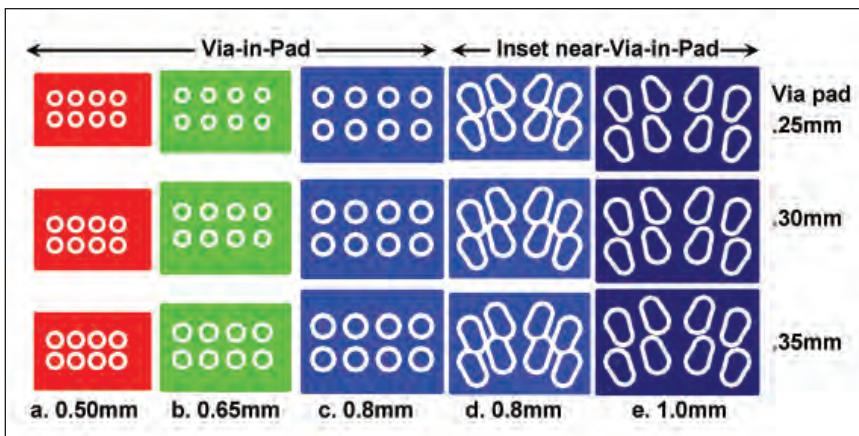
an IPC-Type III structure. Even if a thin dielectric is not employed, any dielectric thickness less than 0.005 inches (<0.125 mm) will couple GND to PWR and provide a lower power supply (PS) impedance and will reduce PS resonances and noise.

Surface Ground Pours

If moving the GND plane to the surface has such an advantage, what do you do with the via-connections, especially for BGAs? This is the critical question and it depends on the design rules utilized, the pitch of the BGA, what a fabricator can accommodate, and if the soldering is Pb-free or conventional SnPb. Table 3.3 shows some of the assumptions for the various ground pours seen in Figure 14. If the pitch is large enough, the vias do not have to be in-the-pad, as Figures (14 d & 14 e) show. The smaller the via land, the more copper is available.

TABLE 3.3: Design rules for surface ground pour around BGAs with pitches of 0.4 mm, 0.5 mm, 0.65 mm, 0.8 mm, and 1.0 mm.

Via Architecture	Via-In-Pad			Inset Near-via-in-pad		
BGA Pitch	0.4 mm	0.5 mm	0.65 mm	0.8 mm	0.8 mm	1.0 mm
SMT Land	0.22	0.25	0.30	0.4	0.40	0.45
	0.20	0.22	0.25	0.36	0.40	0.45
	0.18	0.20	0.20	0.30	0.40	0.45
Via Pad Dia (mm)	In-land	In-land	In-land	In-land	0.35	0.35
					0.30	0.30
					0.25	0.25
Via Dia (mm)	0.10	0.10	0.125	0.15	0.15	0.15
	0.10	0.10	0.10	0.15	0.125	0.125
	0.10	0.10	0.10	0.125	0.10	0.10
Cu Clearance	0.10	0.10	0.125	0.15	0.15	0.15

**FIGURE 14:** This figure illustrates surface ground pours, around BGAs with pitches of 0.5 mm, 0.65 mm, 0.8 mm, and 1.0 mm. 0.4 mm pitch had too small a copper web to fabricate.

When via-in-pad is utilized, as in Figures 14 (a), (b), and (c), the BGA SMT land is the critical dimension. Fortunately, Pb-free solders like the SAC alloys have a greater strength when soldered to bare copper and the BGA land size can be reduced. Table 3.3 depicts some of the choices for lands, vias, and design rules.

In Figures 14d & 14e, notice that the inset vias are swung around. This will be discussed in the next section. Below 0.8 mm, there is not sufficient clearance to have the via outside the SMT land and partial or full VIP has to be used. At 0.4 mm pitch, there are no longer clearances for the copper pour.

Microvia Placement

The microvia used for BGA fanout was shown in Figure 14. As seen in Figure 15, the microvia can be placed outside the BGA land (inset), partially in/out of the land (partial vip) or completely in 'the pad' (vip). If placing the via-in-pad, then the via should always be off-center and not placed in the direct center of the land. This is to minimize any trapped air voids during soldering. If the via is placed in the center of the BGA

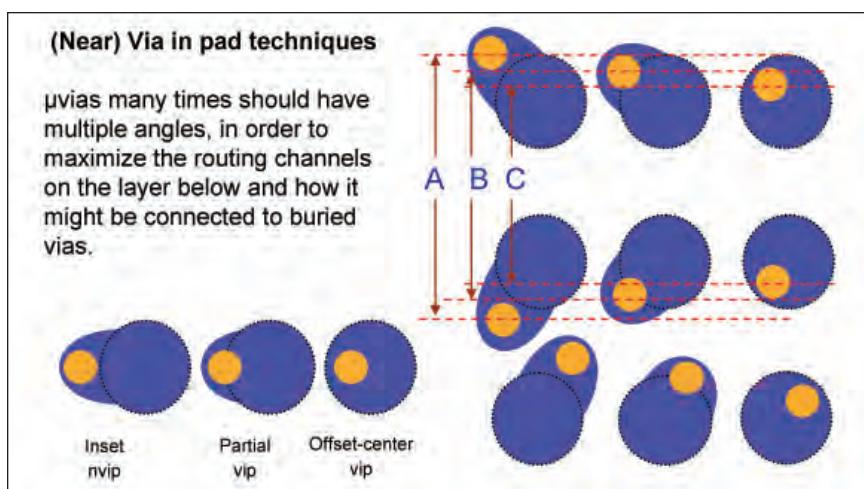


FIGURE 15: Via placement can be adjacent, inset or in-pad and at multiple angles to provide better clearances.

land, and it is not-filled, when the solder paste is applied on the land, and the BGA placed on the paste-land, during reflow, as the solder melts, the BGA ball drops and traps any air that may be there, much like a cork in a bottle. By placing the via off-center, the air has a chance to escape as the solder melts and flows into the microvia. The solder paste brick does not need to be changed, as the volume of a microvia is less than 1% that of the normal solder paste brick.

Using Blind Vias To Create Boulevards For Routing

One useful HDI design technique is to use blind vias to open up more routing space on the inner-layer. By using blind vias between the through-vias, the routing space effectively doubles on the inner-layers, allowing for more traces to connect pins on the inner rows of a BGA. As seen in Figure 16, for this 1.0 mm BGA, only two traces can escape between vias on the surface.

However, beneath the blind vias, now six traces can escape, increasing the routing by 30%. With this technique,

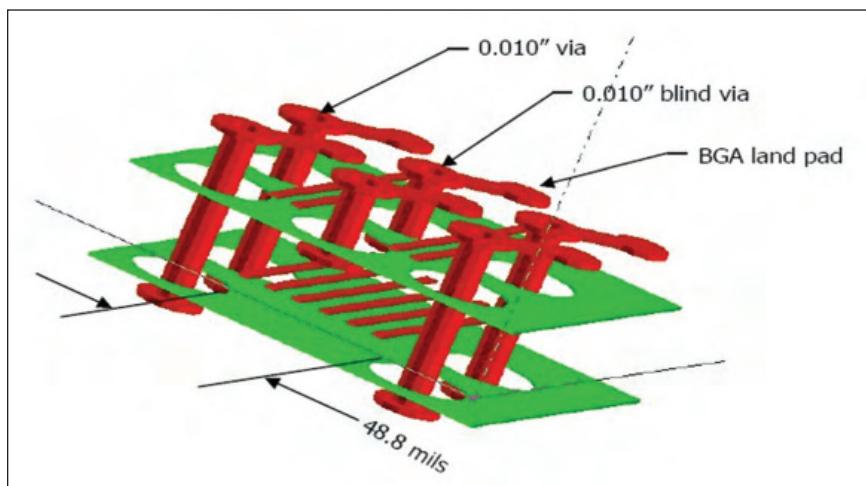


FIGURE 16: Blind vias can be used to form boulevards in inner-layers allowing 30% more routing out of the BGA.

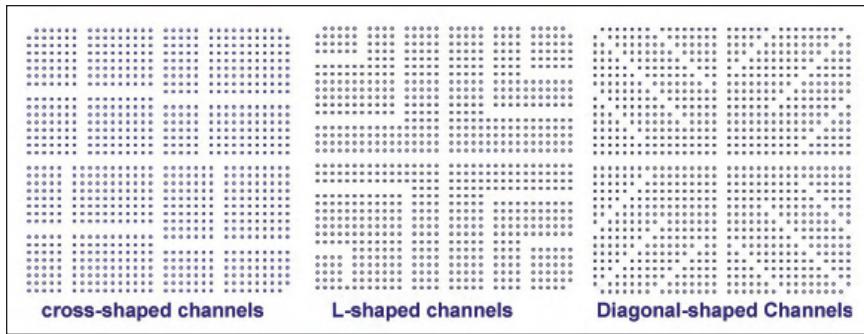


FIGURE 17: Placement of blind vias in cross, L-shaped, or diagonal shapes creates boulevards on the inner-layers to allow higher density routing and escapes.

one-fourth the number of signal layers is required to connect a complex, high-I/O BGA. Blind vias are arranged to form boulevards either in a cross, L-shaped, or diagonal formation (Figure 17). Which formation to use is driven by the power and ground pin assignment. This is why, for an FPGA, reprogramming the placement of power and ground pins can be so productive. (See Figure 11 in this chapter)

As an example, in Figure 18 is a 1153 pin (34 x 34),

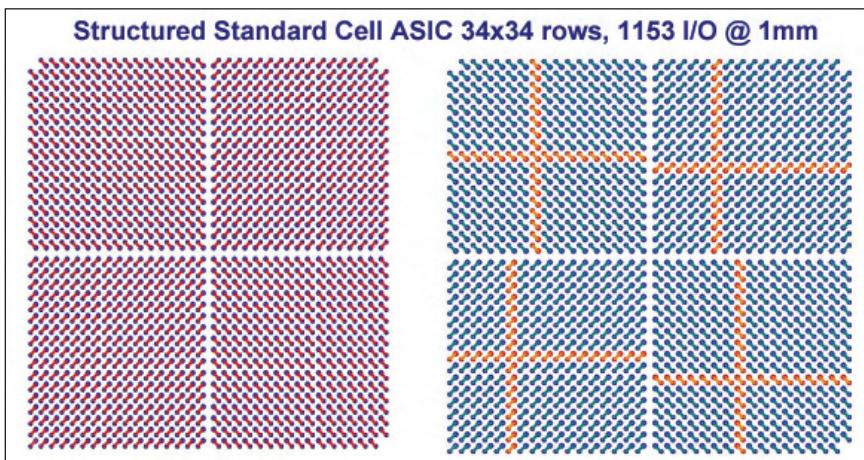


FIGURE 18: The illustrations show the placement of blind-vias to create boulevards within a BGA to improve breakout. Left: Conventional 4-quadrant fanout of a BGA; Right: Cross-shaped blind vias added that permit 48 additional escapes in the boulevards created on the inner-layer, resulting in four less required to breakout the device.

1.0 mm BGA. There are 132 possible escape routes per signal layer (one trace between vias plus 20 traces in the cross-channel [five traces each]). This means that eight signal layers would be required (plus five reference planes) to connect this BGA to the rest of the circuit. The through-holes create a fence that makes breakout routing very layer-intensive.

If we create more routing space by generating boulevards, we can connect more traces per layer and reduce the total number of signal layers. In Figure 18, blind vias are used to form four cross-shaped boulevards. The new boulevards allow 48 additional escapes per layer (8×6 traces) with better signal integrity for the inner traces. Two routing layers and two reference planes can be eliminated.

An additional benefit of creating boulevards with the blind via is seen on the secondary side of the PWB. The through-holes telegraph through the entire board, but, as seen in Figure 19, the boulevards now open within the BGA. The figure on the LEFT has 58 discrete components connected under the BGA by sharing 104 vias. However, on the RIGHT, 183 discrete components can be connected using the boulevards by sharing 366 vias.

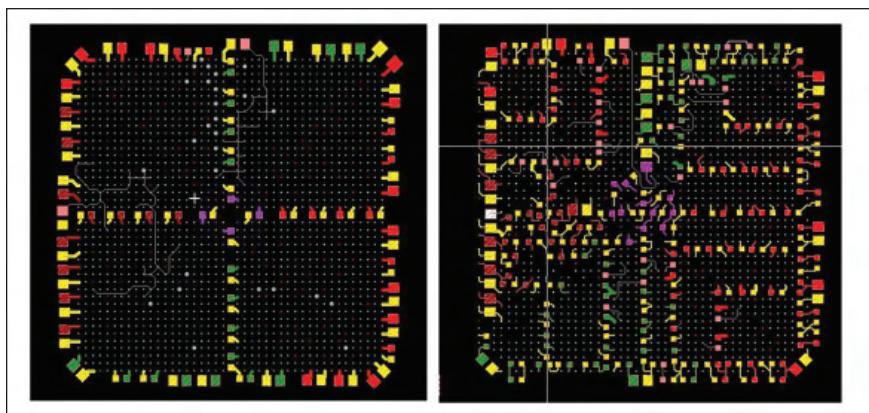


FIGURE 19: These figures show the backside of two BGAs. One is the traditional quadrant fanout with through-holes, allowing 58 discrete components connected by 104 vias. The other utilizes blind via boulevards where 183 discrete components can be connected.

An Example of Boulevard Fanout

The best way to see the advantages of this HDI breakout scheme is to look at an example. Figure 20 is an example taken from the telecom industry. The board in Figure 20 was a 20-layer through-hole design with 8 internal signal layers.

Some of its characteristics are seen in Table 3.4.

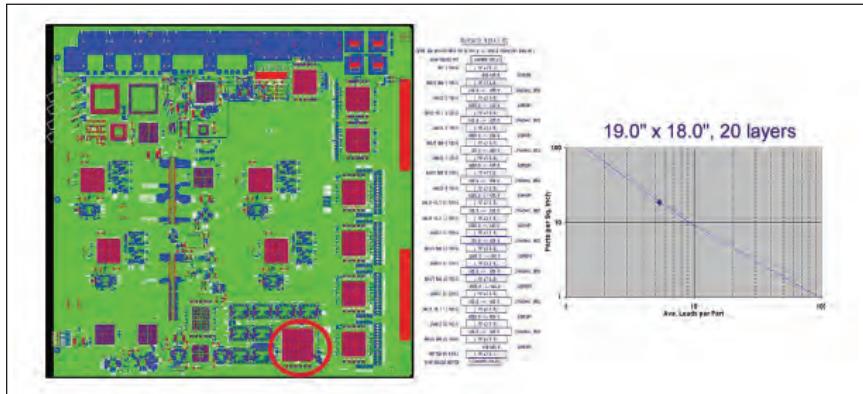


FIGURE 20: This figure shows a 20-layer telecom multilayer that was redesigned into a 14-layer Type I HDI multilayer. The Wiring Analysis for the board is also shown.

TABLE 3.4: Description of telecom board redesigned from TH to HDI, seen in Figure 20

FEATURES (Metrics)	TOP (Primary Side)	BOTTOM (Secondary side)
Parts	2,525	3,784
Pins	24,106	9,911
Large BGAs	81 w/ 1-1089 @ 1.27 mm, 13-625 @ 1.27 mm, 8-676 @ 1.0 mm	35 all small
(Ave. Pins per Part)	20.7	
(Ave. Leads per Sq Inch)	5.4	
Thickness= 0.098" +/- 0.10" No. of TH= 28,057 (82 / sq inch)		
Size: 19.00" X 18.00"		

This is a very dense card, as seen in Figure 20. It is right along the through-hole barrier (Chapter 1, Figure 31) with its 99.5 average leads per square inch density.

This PC card was redesigned using just the simple IPC-Type I structure. The large BGA on the bottom of the board (red-circle 1089 pins) was selected to show the effects of boulevards. On the left side, Figure 21 shows the original 20-layer design and on the right half the redesigned 14-Layer HDI version. In the figure, the orange represents the surface GND pour. Boulevards are created on the top half using L-shaped boulevards and on the bottom-half using diagonal boulevards. The boulevards are formed by GND connections, signal and PWR pins. The rest of the connection utilizes through-holes.

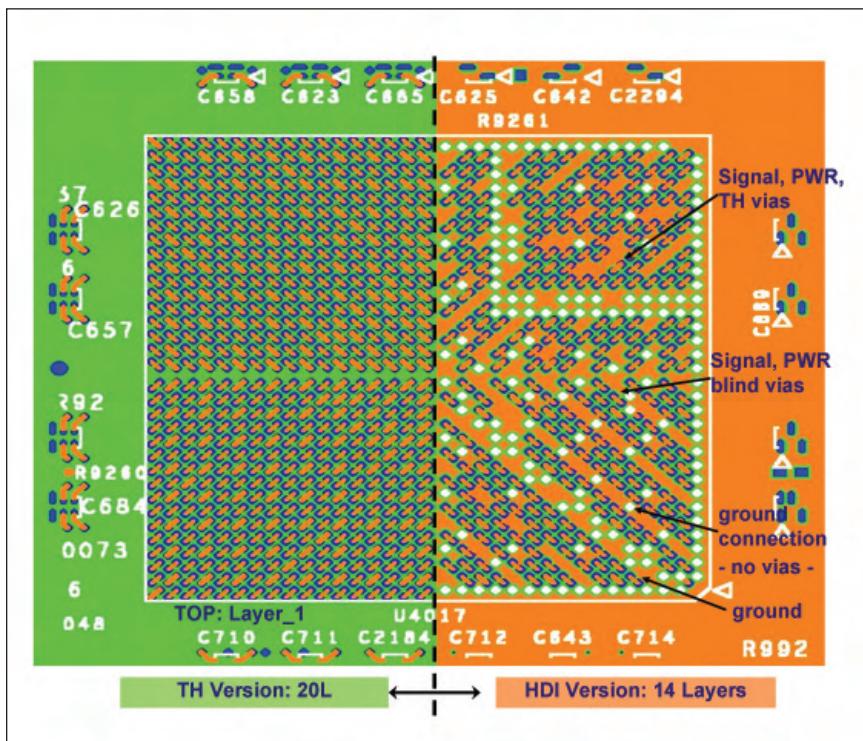


FIGURE 21: The top side of this multilayer shows where the blind via boulevards are arranged, with the top half-using L-shaped and bottom half-using diagonal boulevards.

Design of Advanced Printed Circuits (HDI)

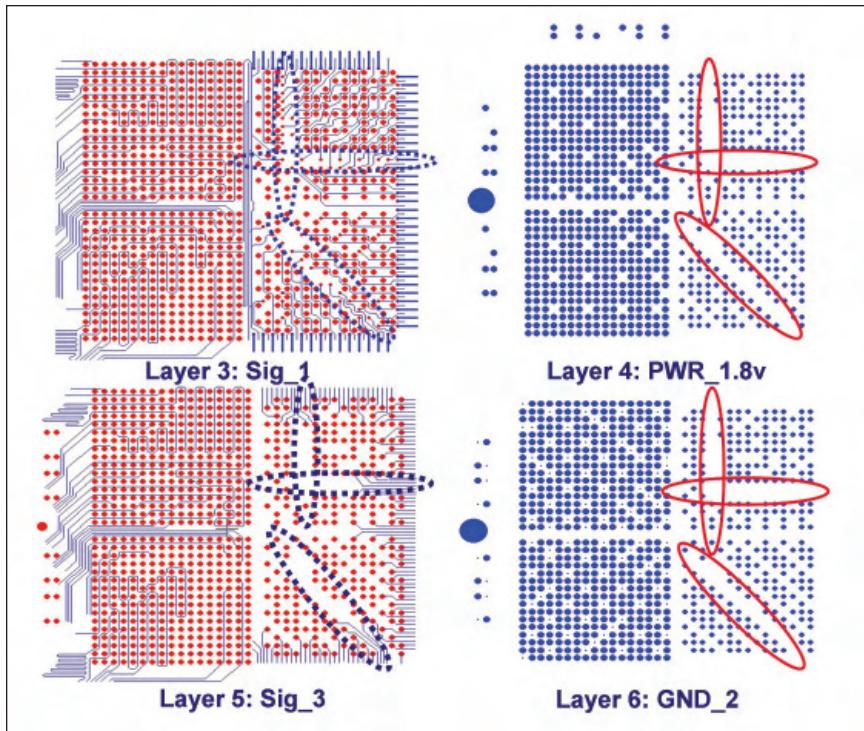


FIGURE 22: This shows layers 3 to 6 of this multilayer. The right-side panels show the escapes opened up by the boulevards.

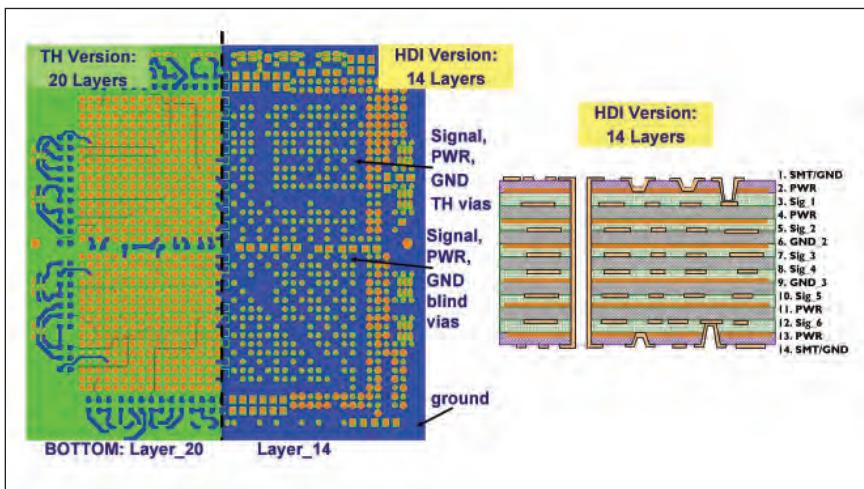


FIGURE 23: The bottom side of this multilayer clearly shows where the blind via boulevards are. On the left is the 14-Layer HDI stack-up of the redesigned board.

Figure 22 continues with the routing of the BGA, again the left side is the through-hole version and the right side starts to clearly show the boulevards. By layer six, the right side has completed the BGA fanout, while the left side will require eight more layers until its fanout is completed.

Figure 23 shows the bottom of each board. The left (through-hole) has the clear array of through-holes in the BGA, while the right (14-layer HDI) shows the boulevards created. Figure 23 also shows the 14-layer HDI stack-up of the redesigned board used in this example.

Boulevards Enhanced By Via Structures

Boulevards can be enhanced by the 3-D via structure. The various depths of blind vias, as seen in Figure 24, help to create larger boulevards. These structures can be created by skip vias, multiple buildup, or sequentially laminated, drilled, and laminated vias. This is also a via structure you will want to have because it provides routing of high-speed critical nets using only the cross-over from horizontal to vertical of small low-inductance blind vias. These are the lowest inductance vias in the board and are ideal for the highest-speed nets. These will also have a very high-density because the crossover will be small blind vias, not the larger buried or through-hole vias.

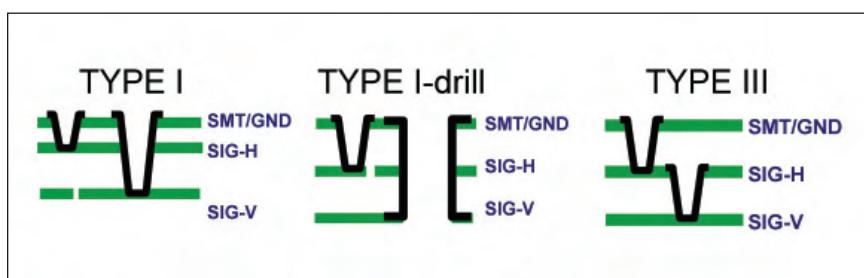


FIGURE 24: Boulevards can be enhanced by creating various blind-via structures with skip, sequentially laminated, and multiple buildup layers.

Boulevards Created by Via Placement

A new concept in applying different types of fanout patterns for BGAs has been developed by Mentor Graphics (www.mentor.com). [15] Instead of the standard 4-quadrant dogbone, as seen in Figure 25 left, the BGA is segmented into *four regions* from the outside in as seen in Figure 25 on the right.

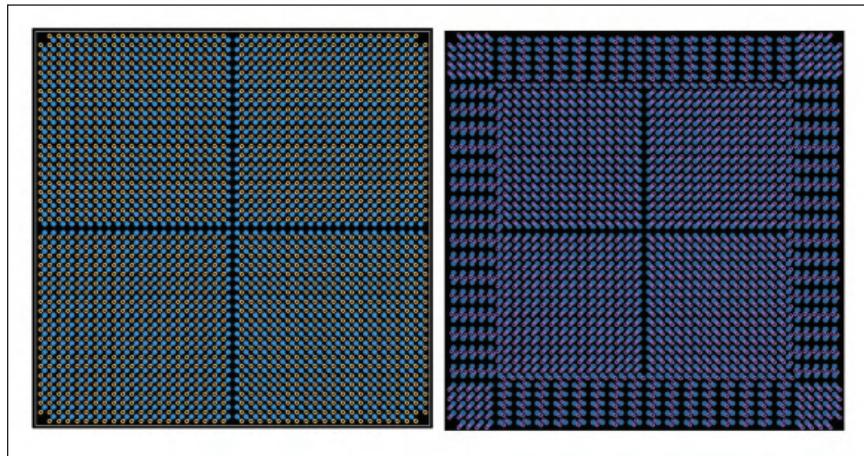


FIGURE 25: Conventional quadrant fanout versus newer and improved four-zone fanout

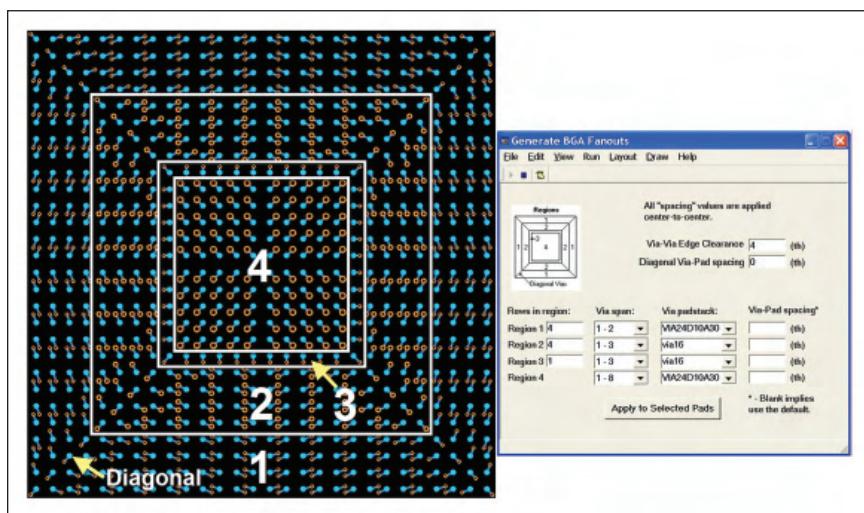


FIGURE 26: Four region via fanout software for EDA tools[15]

Figure 26 left shows a sample BGA with the four regions. The figure shows the software menu (Figure 26 right) that creates the fanout automatically.

The description of this concept is provided by Charles Pfeil, the developer:

"Region 1 comprises the outer rows. The number of rows will vary from 4 to 6, depending on the design rules. As shown in Figure 27a, this region uses a 1:2 microvia with the intent of routing the traces on Layer 2 at maximum route density. This pattern can be varied by moving the via closer to the ball pad and changing the angle, so that the via spacing exceeds the minimum. If you do this, the route density will decrease; how-

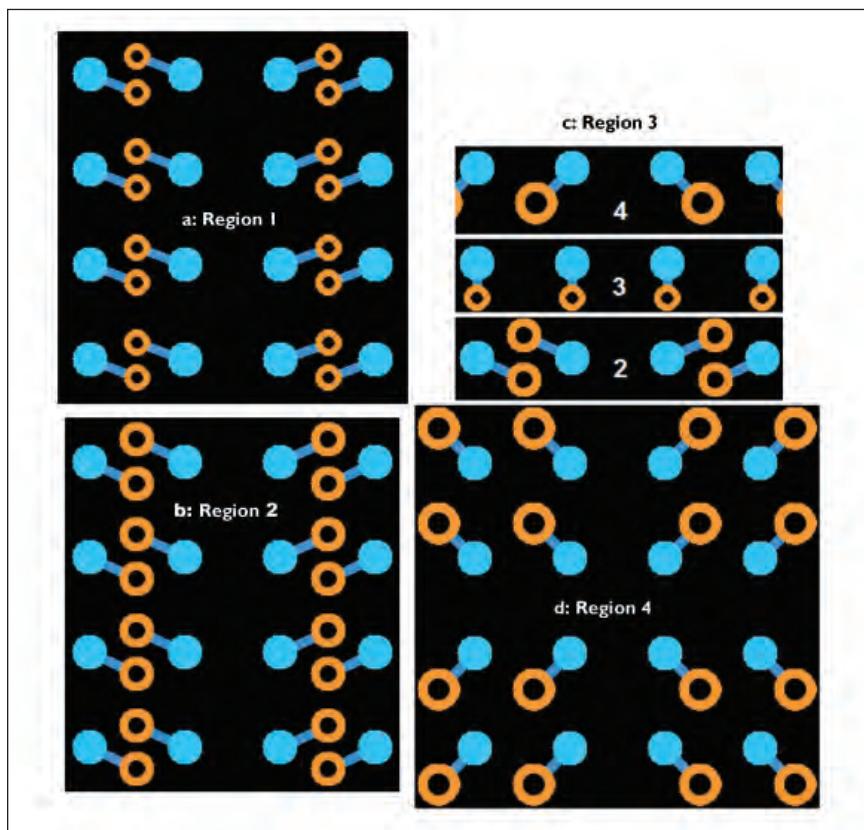


FIGURE 27: The four-region via patterns for Figure 26[16]

ever, you may increase room for plane fill and reduce potential crosstalk between the vias.”

“Region 2 includes all the inside rows. Once the outer rows of BGA pins are routed using the 1:2 microvias, the next 4 to 6 rows should use the 1:3 skip-vias, with the intent of routing the traces on Layer 3 at maximum route density, as shown in Figure 27b. Using the skip-via allows a connection from Layer 1 to Layer 3 without a pad on Layer 2. This pattern can also be varied by moving the via closer to the ball pad and changing the angle so that via spacing exceeds the minimum.”

“Region 3 is the transition between the inside rows (Region 2) and the center rows (Region 4). Since the patterns between regions 2 and 4 will usually conflict and cause DRC violations, a transition area is appropriate. Figure 27c shows a useful pattern for the transition area. A 1:2 or 1:3 via can be used in the transition area depending on your routing strategy. In this example, the pattern is a simple orthogonal short dog-bone. Other angles may be used depending on the via size used.”

Region 4 is the center. The center rows are those left over after other regions have been defined. Usually, the center of the BGA has power and ground pins, and thus putting the through-vias in a standard dog-bone pattern as shown in Figure 27d makes sense. Note that the vias are not located in the exact center of the ball pad matrix – this allows for a greater ground plane fill on Layer 1.”

“The Diagonal Region (1). The pins along the diagonals could have conflicting patterns when the Region 1 and Region 2 fanouts merge. The example in Figure 28 shows a method that not only merges the patterns, but also spreads the vias away from the centerline, providing greater route density along the diagonal. Dividing up the BGA into regions enables maximum route density, and can thereby reduce the number

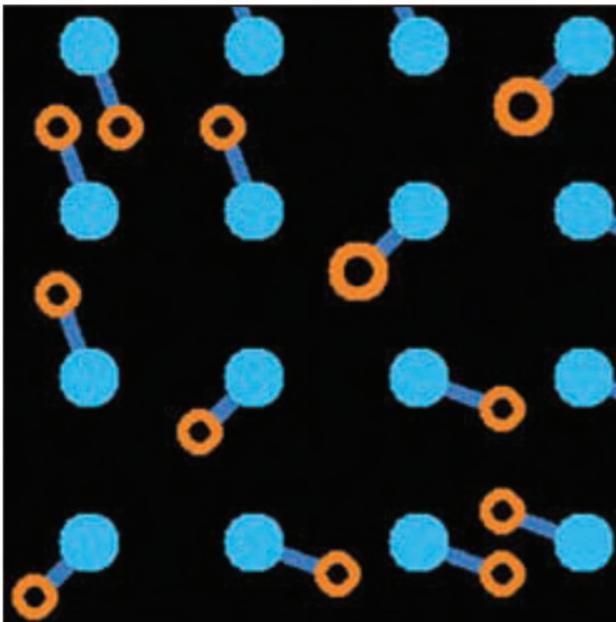


FIGURE 28:
The BGA
diagonal region
on the corners for
the diagram in
Figure 26

of layers needed. When the BGA has over 1,500 pins, simply routing out of the BGA tends to be the primary contributor to increased layer count. By varying the number of rows used in each region, based on the stack-up and via spans available, you can obtain the most optimal fanouts and routing in the context of your own specific design.”[16]

This aligned-via pattern of shifted blind vias increases breakout from big BGAs significantly. It also has other advantages:

- There is a 24% increased route density per layer over through-vias and unshifted blind vias.
- There is more room for a ground plane on the mount layer (but not as much room as with via-in-pad).
- If you route the high-speed single-ended nets on the layers using blind vias, via stubs are eliminated and via-to-via cross talk is minimized.

- Any signal routed on the blind via layers will not need to have a buried via, thus opening up route space on the buried via layers.

A disadvantage is that blind and buried via stack-up is slightly more expensive than through-via stack-up.

The last new concept resulting from HDI is to arrange the blind-via rotation not in the normal North-East-West-South rotation but to move them into the same channel and stagger them as shown in Figure 29. This arrangement forms a broad boulevard between the buried vias four times larger than the device pitch. This boulevard is 4.0 mm and can permit the routing of up to 13 traces — a vast freeway for global routing.

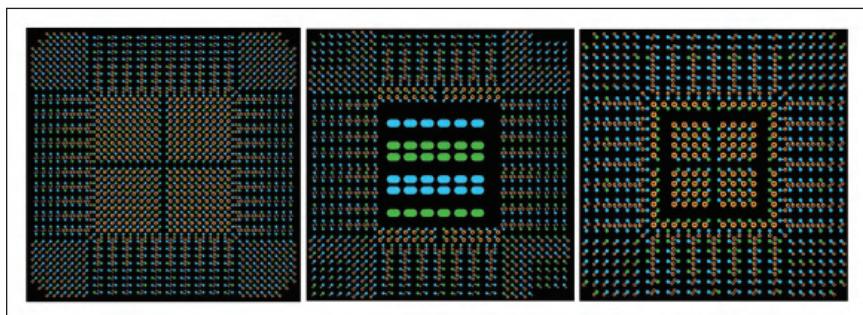


FIGURE 29: Three examples of the 4-Zone BGA Fanout macro

Example of Shifted Blind Vias

An excellent example of shifted-aligned-via pattern is the Xilinx Virtex-4 and Vertex-5 FF1760 series FPGA with 1760 pins and a 1 mm pin-pitch from an article by Charles Pfeil.[17] Xilinx Application Data sheets show the use of a 6-signal layer to breakout its device. In Pfeil's article, using the shifted-aligned-via pattern to form boulevards, he completed the breakout in only two signal layers as seen in Figure 30. The stack-up is also seen in Figure 30 and is a common and cost effective IPC-Type II 12-layer HDI.

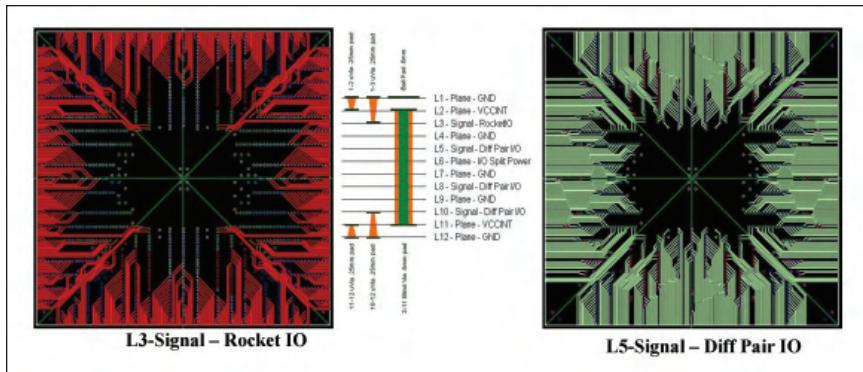


FIGURE 30: Example for a Vertex 5, 1760 pin FPGA

To understand how this was accomplished requires that you look closely at both the HDI stack-up and the aligned-shifted blind vias. This close-up can be seen in Figure 31. Two rows of the FPGA pins fanout to layer-3 (with a skip-via for the 50 ohms single-ended Rocket I/O) and the next two rows fanout to layer-2 then drop to the buried via to layer-5 (the 100 ohm differential-pair I/O). This arrangement forms a broad boulevard between the buried vias four times larger than the device pitch. This boulevard is 4.0 mm and can permit the routing of up to 13 traces — a vast freeway for global routing.

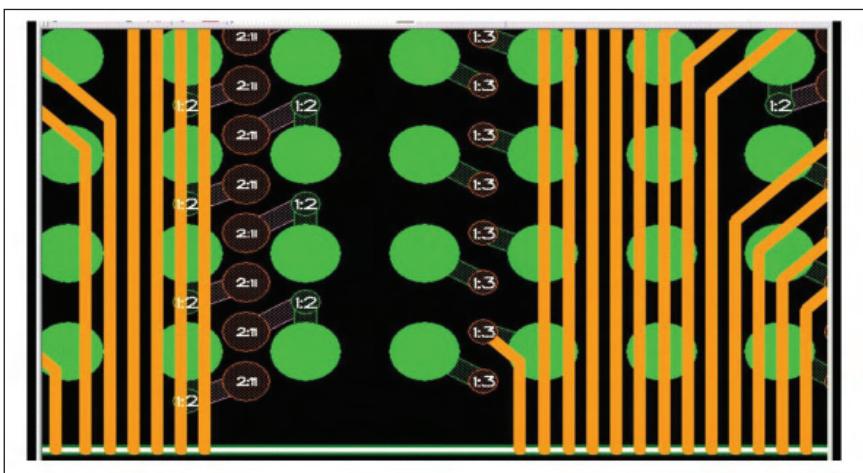


FIGURE 31: Close-up of Vertex 5 breakout of Figure 30

Design of Advanced Printed Circuits (HDI)

Under layer-5, the BGA disappears as there are only the buried vias creating this via-lined-boulevard for mass routing.

Fine-pitch BGAs

Fine-pitch BGAs are fanned out either by moving the microvia within the pad or by using a microvia that is only partially in the pad. (See Figure 13 again.) If routing with 0.1 mm or 0.075 mm traces, then via-to-via spacing is shown in Table 3.5. Figure 32 shows possible breakout schemes for different fine-pitch BGAs. Detailed design rule diagrams are at the end of this section.

TABLE 3.5: Design rules for SMT BGA lands, blind vias, traces, widths, and spacings for fine-pitches of 0.65 mm, 0.5 mm, and 0.4 mm.

Via Architecture	Surface Layer			Inner-layers		
	0.4 mm	0.5 mm	0.65 mm	0.4 mm	0.5 mm	0.65 mm
SMT Land (mm)	0.22	0.25	0.30	0.22	0.22	0.25
	0.20	0.22	0.25	0.20	0.20	0.22
	0.18	0.20	0.22	0.18	0.18	0.20
Via Dia (mm)	0.10	0.10	0.125	0.10	0.10	0.125
	0.10	0.10	0.10	0.10	0.10	0.10
	0.10	0.10	0.10	0.10	0.10	0.10
Trace Width (mm)	---	0.075	0.10	0.075	2-0.075	0.075
	0.075	0.075	2-0.075	0.075	2-0.075	2-0.075
	0.075	0.075	2-0.075	0.075	2-0.075	2-0.075
Trace Spacing (mm)	0.180	0.0875	0.125	0.075	3-0.075	2-0.0825/.085
	0.0625	0.1025	3-0.0825	0.075	3-0.075	3-0.093
	0.0725	0.1125	3-0.093	0.075	3-0.075	3-0.100

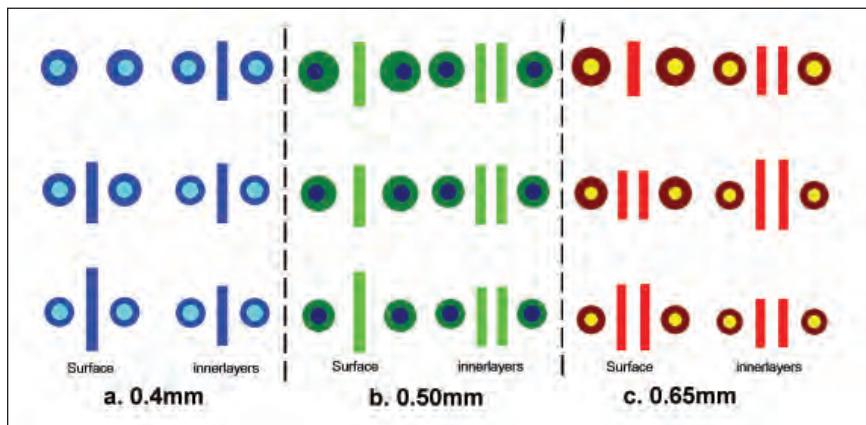


FIGURE 32: Illustrations of the design rules for SMT BGA lands, blind vias, traces, widths, and spacings for fine-pitches of 0.65 mm, 0.5 mm, and 0.4 mm

Notice in Figure 32 that for 0.5 mm and 0.4 mm pitches, the via holes are not in the center of the lands. This is to improve the spacing on the traces on the inner-layers to a minimum of 0.075 mm.

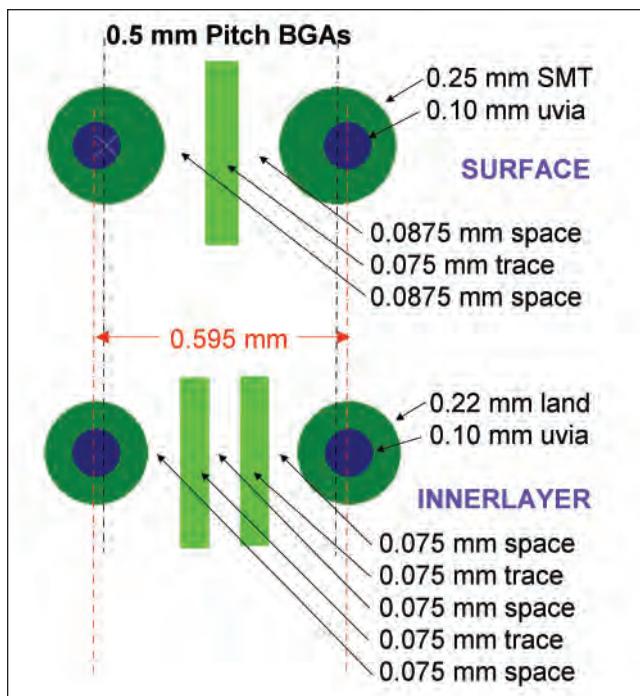


FIGURE 33:
Illustrations of the design spacing for 0.5 mm SMT BGA lands, blind vias, traces widths and spacings for the surface versus inner-layer

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A magnification of this spread is shown in Figure 33. The 0.5 mm pitch BGA with the 0.25 mm SMT land and 0.22 mm inner-layer pad is illustrated. When selecting design rules for fine-pitch BGAs, be sure to contact your favorite PCB fabricator to find out what geometries he can support and tolerances that he can hold.

Stack-ups

HDI stack-up is one of the most important features to decide on early in the HDI board's life. There are many factors to consider and there are many variations in the Type I thru Type VI structures. Again, taking a page from Charles Pfeil's Book, on "BGA Breakouts and Routing"[15], in "Chapter Three-HDI Stack-ups", Mr. Pfeil used a meter as a measure to show the "best five" and "worst one" of four key performance metrics:

- HDI Cost—Based on the number of critical cost defining fabrication processes of lamination, and plating. The fewer number of these cost driving processes, the higher the score. Maximum is 5.
- Route Density – Highest score for maximum routing density using boulevards and buildup layers without through-hole or buried via obstructing routing space.
- Power Integrity – Highest score for PWR/GND plane coupling and low inductance power delivery.
- Signal Integrity – Highest score for routing critical nets on buildup layers, lowest reflection, surface GND for low EMI/RFI, and lower cross talk.

Seven Popular HDI stack-ups

These seven HDI stack-ups are from Pfeil's book and represent seven of the most useful and practical stack-ups (Figure 34). The total score is beside each Metric Meter. (A perfect score would be 20. None come close, the highest being 15.)

The HDI Handbook

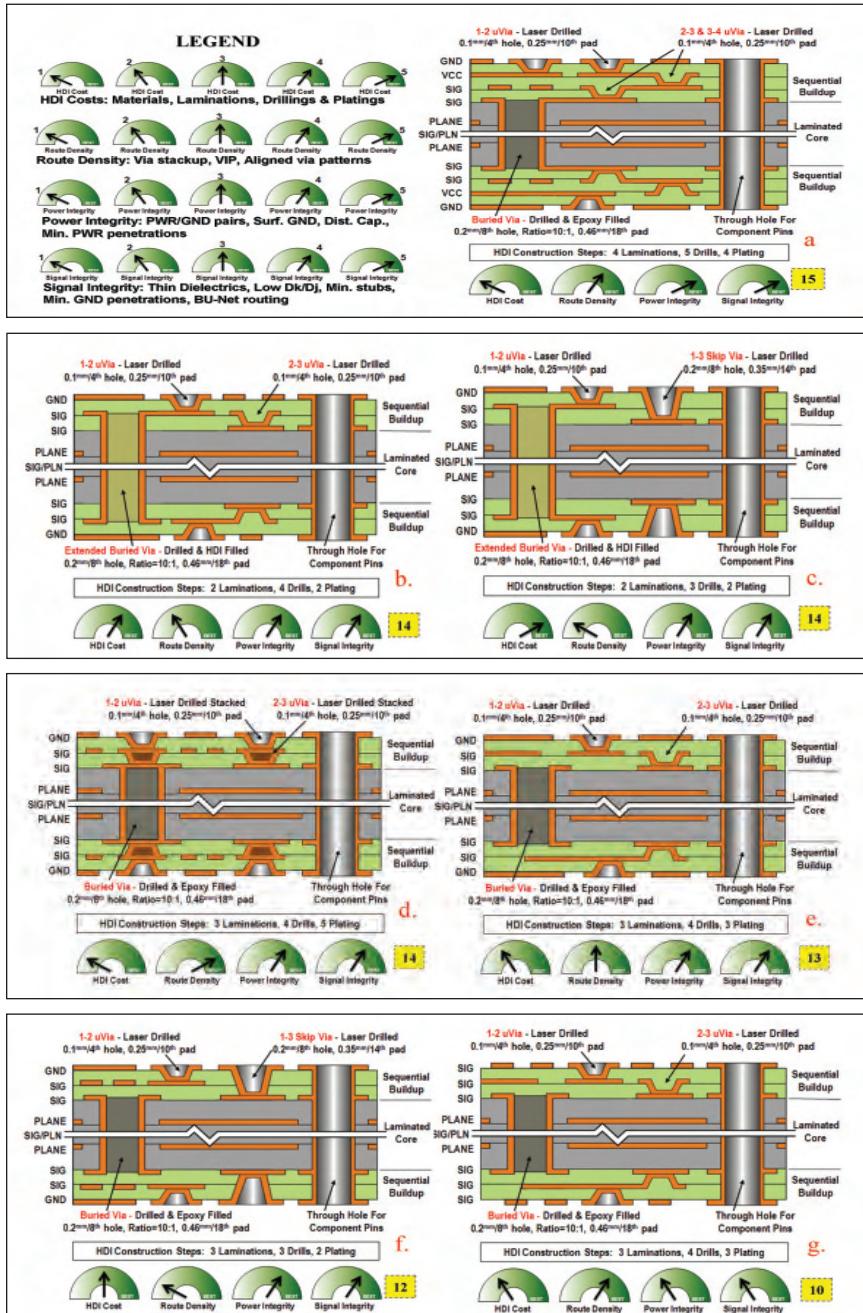


FIGURE 34: Seven typical HDI stack-ups with ratings for Cost, Density, Power Integrity, and Signal Integrity (Reprinted with permission from "Big BGA Breakout" courtesy of C.Pfeil)[15]

Stacked vias

A necessary complication with HDI is created by fine-pitch BGAs when the design rules selected do not have clearance for staggered blind vias. When that situation is created, stacking of microvias or stacking a microvia on top of the buried via is called for. Figure 35 shows these two situations, the left is a microvia stacked on top of a buried-via that has been filled and remetallized. The right figure is two laser-drilled microvias. The base microvia (Layer 2/3) is fully plated.

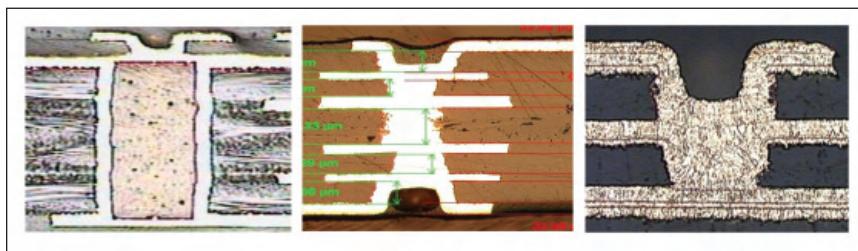


FIGURE 35: Stacked vias: blind via stacked on drilled/filler buried via; two panels of microvias stacked on plated microvia

Filled vias, on which the stacked vias are built, can be filled by three techniques:

- Conductive paste and cap plating
- Non-conductive filling, metallization, and cap plating
- Special high-throw electroplating that will fill the via

All three processes are detailed in Chapter 10 – Electrodeposition and Solderable Finishes for HDI.

SMT HDI Backplanes

A growing application for HDI is the backplane and its replacement, the midplane. As Figure 36 illustrates, the press-fit connector requires a large through-hole. Because the inductance in a thick backplane can be so significant, over 4 dB loss

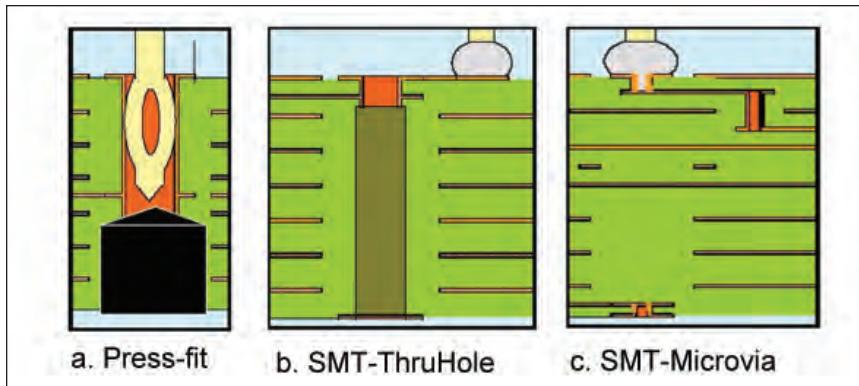


FIGURE 36: Backplanes: a. press-fit connector in a through-hole with backdrilling; b. SMT connector with through-holes also 'backdrilled'; c. SMT connector but using microvias (Courtesy of FCI)

in a 0.6 mm drill on a 6 mm thick backplane (from Figure 37), the through-holes are back-drilled to reduce the loss to 1 dB at 10 Gb/s. Newer connectors are now surface mounted, (Figure 36b), but the backplanes are still thick, so even these through-holes need to be back-drilled. However, using these new SMT connectors with microvias, as seen in Figure 36c, the layers

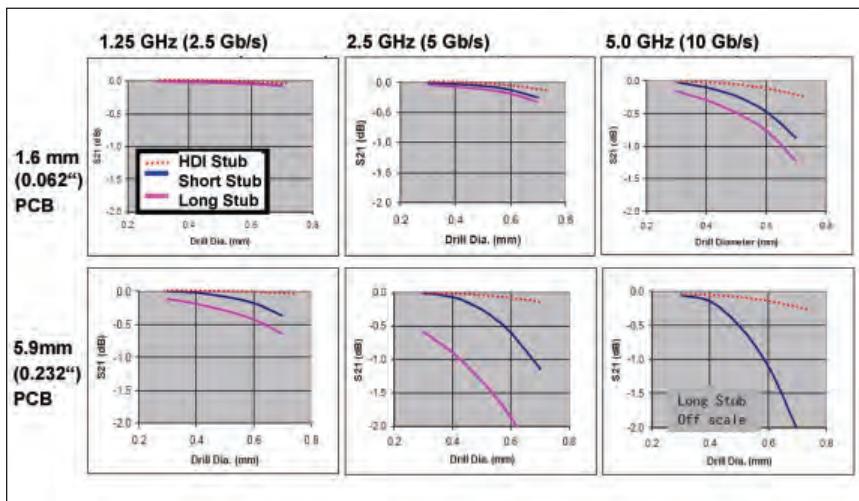


FIGURE 37: Parasitic effect of via stub (through-hole long), backdrilled (through-hole short), and microvia on high-frequency performance of two different board thicknesses[18]

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and loss are greatly reduced. For a 6.0 mm backplane at 10 Gb/s, it is only 0.2 db (Figure 37).

Loss in vias is proportional to the via depth and to its diameter. Capacitance coupling is proportional to the number of layers. As Figure 37 shows, the losses increase with thickness, diameter, and frequency. The lowest losses occur in the HDI via nets.

A new alternative to the conventional backplane when using microvias is the midplane. As seen in Figure 38, the midplane uses the blind microvias to surface mount connectors on both sides of the board. This permits many fewer layers and significantly shorter interconnects, as seen in the left-most two panels in Figure 38 (the red lines are the interconnects). Many times these midplanes are also made of low-loss laminate like GETEX, as seen in the cross section in the lower right.

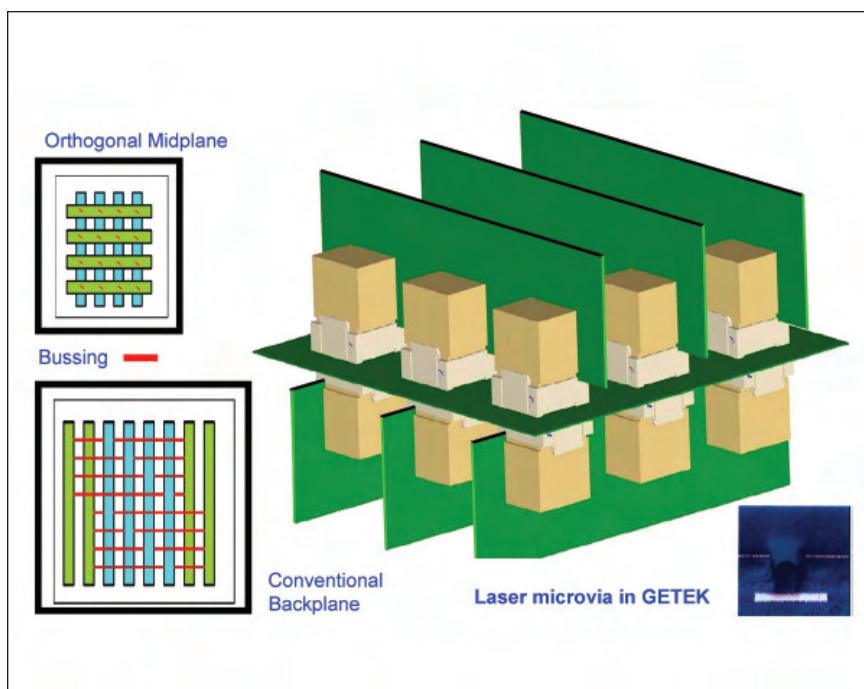


FIGURE 38: Midplane advantage over backplane[19]

The advantages of the midplane can be seen in the electrical chart of Figure 39, from a through-hole backplane with press-fit connectors, having 14.5 dB insertion loss, to only 5.2 dB for the BGA midplane with microvias. From personal experience, I have seen 32-layer press-fit through-hole backplanes be redesigned to only 6-layer HDI midplanes that were also 40 % smaller as well as 120% thinner. The costs dropped by more than four times.

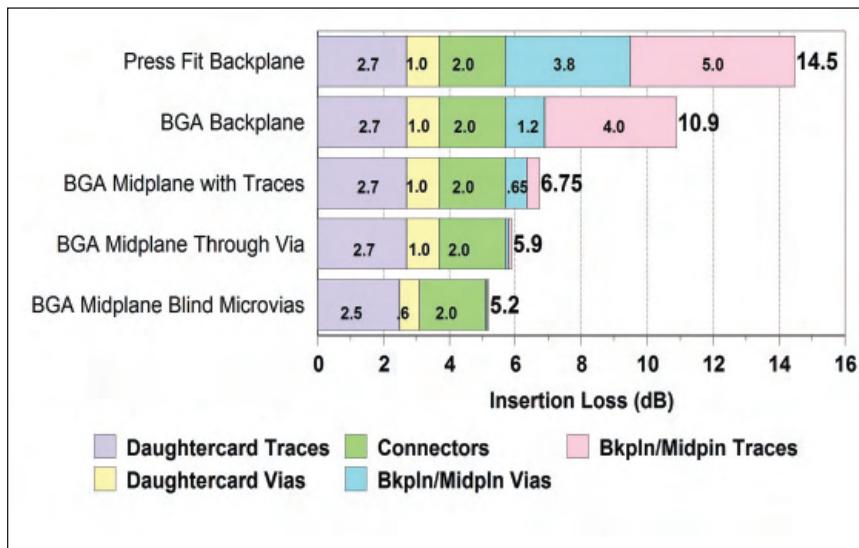


FIGURE 39: Midplane performance advantages over press-fit backplane, estimated link loss at 2.5 GHz (5 Gb/s)[20]

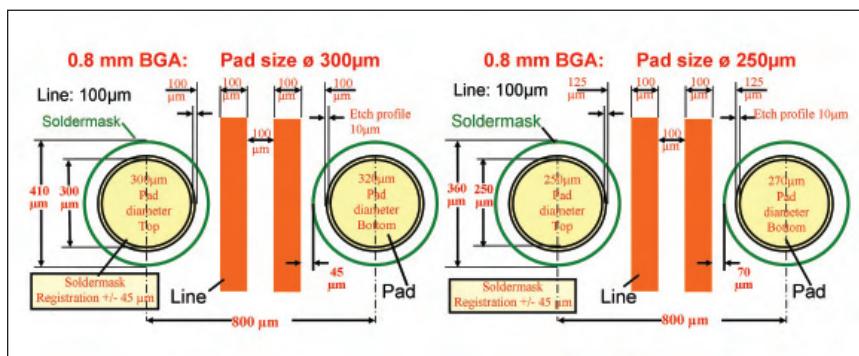


FIGURE 40: 0.80 mm pitch design rules

BGA Routing Design Rules

The detailed design rules for fine-pitch routing are shown in the next four figures. This covers 0.8 mm pitch, 0.65 mm, 0.50 mm and 0.4 mm pitches. These design rules were used in Figure 14 , Figure 32, and Figure 33.

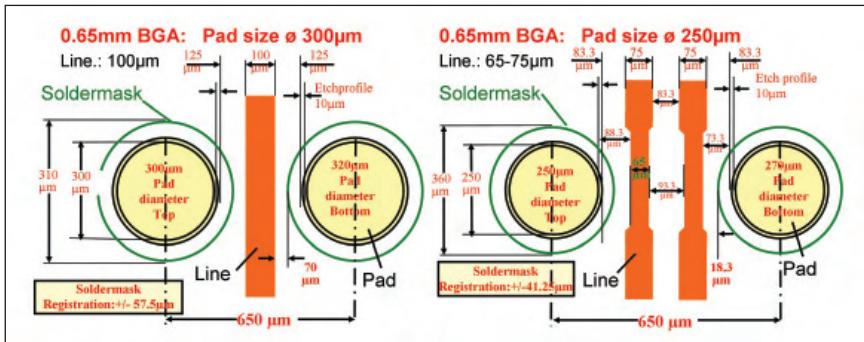


FIGURE 41: 0.65 mm pitch design rules

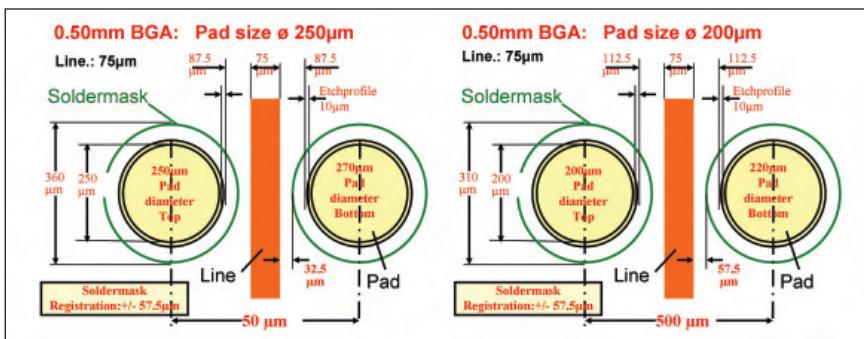


FIGURE 42: 0.50 mm pitch design rules

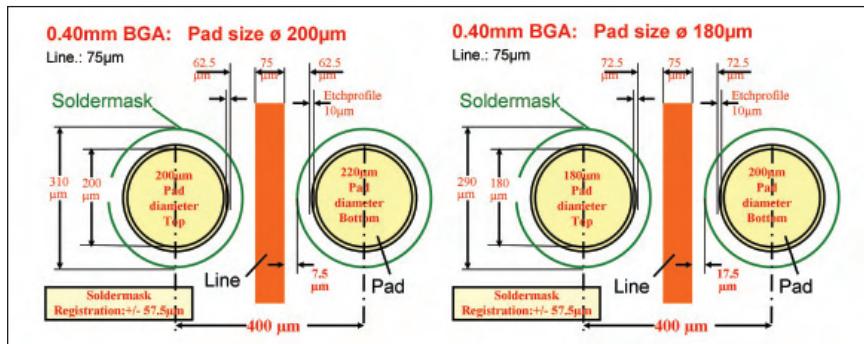


FIGURE 43: 0.40 mm pitch design rules

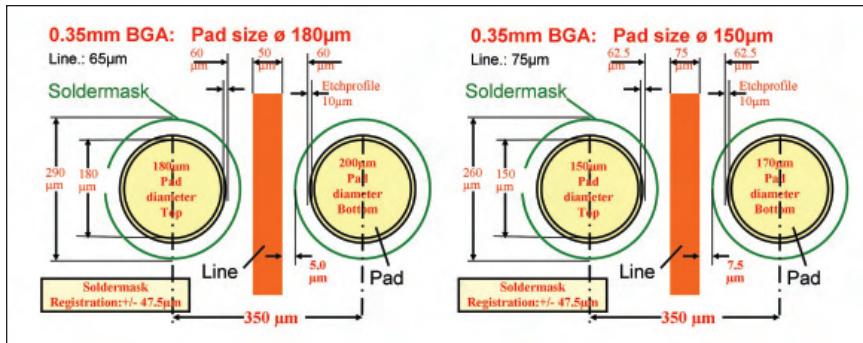


FIGURE 44: 0.35 mm pitch design rules

References:

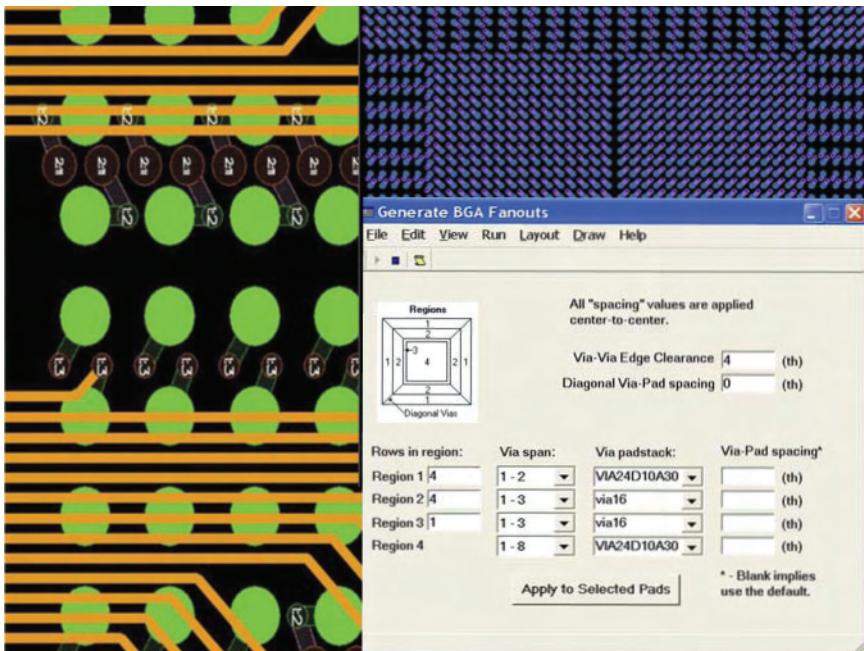
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Design of Advanced Printed Circuits (HDI)



PRINTED CIRCUIT BOARD DESIGN

Designing with HDI / Microvia Technology

Driven by the need for denser, higher performing, and lower cost products, the use of High Density Interconnects (HDI) and Microvias is rapidly emerging in many industries. By using this technology a designer can effectively break out from dense, fine pitch BGAs, reduce PCB layer counts and size, and improve performance.

But designers need the tools that fully understand the complex via stacking rules as well as automate the routing process.

Mentor's Expedition™ Enterprise and Board Station® XE flows enable highly efficient automatic and interactive routing of HDI/Microvia layers to provide the productivity you need to get the job done quickly and develop the most competitive products for your company.

To connect with other innovators and visionaries
of future HDI and microvia technology
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4

Electrical Performance

By Eric Bogatin

Introduction

Moore's Law has always driven the electronics industry, resulting in ever-smaller transistor channel lengths which cause ever shorter rise times. This is the fundamental driving force which has enabled electronic products to move toward higher and higher clock frequencies. When technology surpassed the 100 MHz clock frequency and into the sub nanosecond regime, interconnects were no longer transparent and electronic products entered the signal integrity era.

Whether the application calls for it or not, chips built on a state-of-the-art fab line, will have shorter channel lengths, shorter rise time signals and will be more sensitive to signal integrity effects. With clock frequencies currently in excess of 1 GHz and rise times in the sub 100 psec regime, signal integrity is oftentimes a limiting factor in the design of products.

Signal integrity is about why the interconnects are not transparent to signals and what can be done in the design and materials selection to meet the ever more challenging performance specs. It is inevitable that signal integrity will play an increasingly important role in ALL future product designs. This is why it is often said:

"There are two kinds of engineers, those with signal integrity problems and those who will have them."

Electrical Performance

The electrical performance of all interconnects arises from the interaction of physical design and material properties. The goal in any product design is to arrive at an acceptable design that achieves the performance spec, while meeting the cost targets, in terms of dollars, time, and risk.

While IC technology has advanced by orders of magnitude in reduction in transistor channel length and a reduction in rise time, resulting in more signal integrity challenges, the traditional TH board technology has not advanced nearly as much in performance. This is why it is increasingly important to consider alternative technologies which offer performance advantages that are not constrained by simple scaling, but allow a jump to a new level of performance.

Signal integrity problems generally fall into six categories, based on their root causes:

- **Signal quality due to reflection noise**
- **Cross talk**
- **Ground bounce (a special type of cross talk)**
- **Lossy lines**
- **Power Delivery Network (PDN)**
- **ElectroMagnetic Interference (EMI)**

In the following sections, the impacts of the special features in HDI technology on these problems are addressed.

Scaling

The electrical properties of a signal line are described in terms of four simple qualities:

- **characteristic impedance**
- **time delay**
- **loss or attenuation**
- **cross talk to nearest neighbors, as measured by NEXT or FEXT**

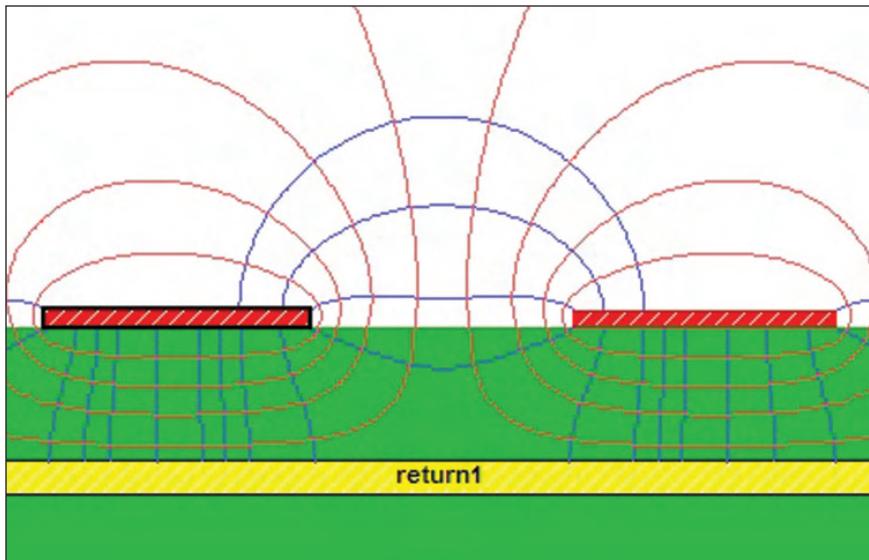


FIGURE 1: Dual 50-ohm microstrip traces, with 10-mil lines and 10-mil spaces, simulated with Mentor Graphics' HyperLynx (www.mentor.com/products/pcb/analysis_verification/hyperlynx)

When an interconnect is designed as a uniform transmission line, the reflections from impedance discontinuities along the path are minimized. This means keeping a constant cross section down the length of the interconnect.

For uniform interconnects, the cross section defines the characteristic impedance and cross talk. An example of the cross section for a pair of microstrip or surface traces with 10-mil wide lines and a 10-mil space, with one half ounce of copper, is shown in Figure 1.

One way of describing cross talk is in terms of the figures of merit, the Near End Cross Talk (NEXT) coefficient and the Far End Cross Talk (FEXT) coefficient. These comprise the ratio of near and far end noises generated on the quiet line in a uniform pair of transmission lines when the ends are terminated in their characteristic impedances, to the signal on

Electrical Performance

the active line. It is a measure of the typical cross talk noise that would be observed.

The dielectric thicknesses, line width and dielectric constant primarily define the characteristic impedance, while the spacing to the adjacent traces defines the cross talk.

These electrical qualities scale with geometry. If every feature in the cross section were reduced by a factor of five, the characteristic impedance and NEXT and FEXT figures of merit would not change. The following shows the geometric features for a conventional PCB and HDI interconnect, with exactly the same performance:

	PCB	HDI
Line width	10 mils	2 mils
Dielectric thickness	5.1 mils	1.02 mils
Copper thickness	0.5 oz	0.1 oz
Dielectric constant	4	4
Length	10 inches	10 inches

This principle is illustrated in Figure 2.

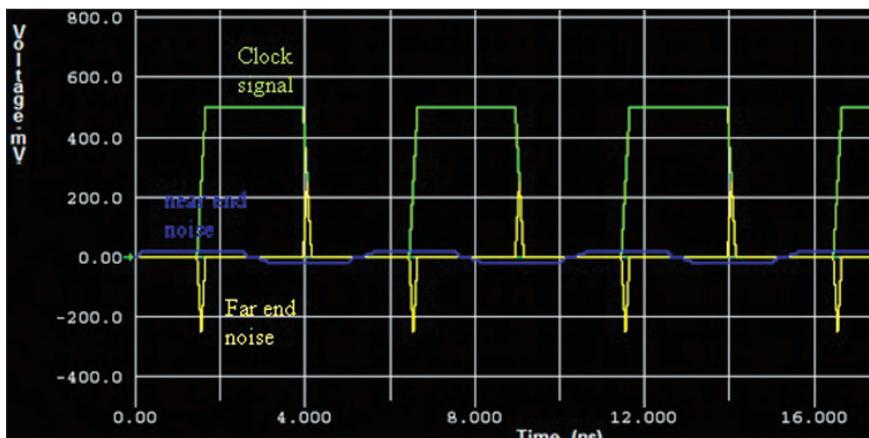


FIGURE 2: The near end and far end noise between two microstrip traces are simulated in this figure. The simulated noise of the 10-mil line and space pair and the 2-mil line and space pair are superimposed and indistinguishable from one another.

This property of scaling has often created a sense in designers' intuition that there are no electrical advantages to considering HDI designs. Scaling all the features down maintains the same electrical performance.

While this is true for scaling the cross section of uniform signal lines, two important non-scaling terms that influence electrical performance are that HDI interconnects can be shorter in length and HDI interconnects can use non-reinforced laminates with a lower Dk. These features enable shorter and more controlled time delay and lower cross talk

Because some electrical properties do not scale with lower feature size, HDI technology can offer a "nonlinear" improvement in performance in some cases. This is especially true for via design and PDN.

However, scaling the line width narrower also introduces a downside from the higher resistive losses which results in more rise time degradation which can be compensated for by leveraging the best of HDI and the best of conventional TH technology. Since the TH technology is sometimes referred to as "low-density interconnect," the combination of these technologies is sometimes referred to as HDI/LDI.

Shorter and More Controlled Time Delay

The time delay of any interconnect depends primarily on the speed of the signal and the length of the interconnect:

$$TD = \frac{Len}{c} \sqrt{Dk}$$

Where:

TD = the time delay in nsec

Len = the interconnect length in inches

c = the signal speed of light in air, 11.8 inches/nsec

Dk = the dielectric constant of the laminate

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An HDI version of a conventional PCB would typically have components closer together and consequently typical interconnect lengths shorter. This length scaling reduction factor could be from 2 to 5 depending on the routing features.

With shorter interconnect lengths, time delays will directly scale shorter by a factor of 2 to 5.

In the construction of typical PCB laminates, a mat of woven fiberglass is coated with an epoxy resin. Successive layers are laminated together. The glass fibers have a dielectric constant on the order of 6, while the resin has a dielectric constant on the order of 3.

In any given layer, the higher the glass content, the higher the dielectric constant. The resulting composite layer has a dielectric constant that will vary from 3.8 to 4.5 depending on the relative amount of glass and resin.

In the construction of the HDI buildup layers, typically on top of cores, the resin clad copper (RCC) dielectric does not use a glass weave reinforcement, but is a homogenous resin. This means that the dielectric constant is about 3, independent of the construction.

The advantages of this feature include the lower dielectric constant and resulting shorter time delay. For the same lengths, two interconnects with a dielectric constant of 4.5 and 3 would have a time delay difference based on the ratio of the square root of their dielectric constants. This would be a reduction in wiring delay in one line of 180 psec/inch to 145 psec/inch for the other, a reduction of 20% in the time delay of similar length interconnects.

Another advantage is that the local dielectric constant that the signal sees in a homogenous material system is constant everywhere. This means the time delays for the signal in any interconnect will be accurate and predictable.

This is not the case in a glass weave laminate system. The local dielectric constant a signal sees may vary depending on if the signal is traveling over a glass bundle, where it would see a higher dielectric constant, or in the valley between bundles, where it would see the lower dielectric constant of the resin.

This effect is called “glass weave skew” as the local variation introduces a varying time delay which is referred to as “skew.” This effect is statistical in nature, as it requires the coincidence of multiple signal lines traveling exactly positioned relative to the glass weave.

In studies conducted measuring large numbers of traces in typical FR4 laminates, the weave-induced skew has been measured to be about 4 psec/inch. This is out of the typical 160 psec/inch wiring delay, which is about a 2.5% skew. In a 10 inch long interconnect. The glass weave skew can be 40 psec, which for PCIe Gen II busses, can account for the entire skew budget.

With the homogenous dielectric of HDI layers, the glass weave skew problem is eliminated.

Shorter Length and Lower Cross Talk

In microstrip or surface traces, the magnitude of far end noise on a victim line from an adjacent aggressor depends on the stack-up geometry and the coupling length between the two lines. It varies as follows:

$$FEXT = k \frac{Len}{RT}$$

Where:

FEXT = far end cross talk coefficient

k = coupling term between the two lines in nsec/inch

Len = coupling length in inches

RT = rise time of the signal in nsec

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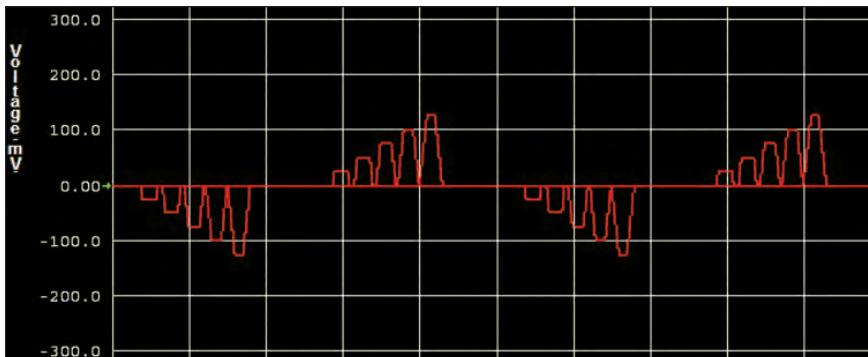


FIGURE 3: Far end cross talk is shown as the coupling length increases from 1 inch to 5 inches long, with increments of 1 inch for 2 mils wide and 2-mil spaced 50-ohm microstrips with 500 mV aggressor signal and 0.1 nsec rise time.

The longer the coupling length, the larger the far end cross talk. This is illustrated in Figure 3, which shows a simulation of the far end cross talk for a pair of 2-mil lines and 2-mil spaces and 50-ohm surface traces with a rise time of 0.1 nsec. The coupled lengths are 1 inch, 2 inches, 3 inches, 4 inches, and 5 inches. The far end noise increases linearly with length. In this case, the signal is 500 mV.

This example illustrates that the FEXT is 120 mV out of a 500 mV signal, or 24% when the coupled length is 5 inches. This is a disastrous amount. However, if the length of the surface trace were reduced to 1 inch, a factor of 5 reduction, the FEXT would also be reduced by a factor of 5 to 5%, an acceptable level.

In HDI systems, with typically shorter interconnect lengths, the far end noise will be reduced, scaled directly with the interconnect length scaling factor, by roughly a factor of 2 to 5.

Far end noise arises from the inhomogeneous nature of the dielectric layer at the interface of the surface. Some field lines between the two signal lines are in air and some are in the bulk dielectric. This non-uniform distribution of dielectric

constant ultimately gives rise to far end noise. However, only surface traces will experience far end noise and scale with length. Buried traces, such as in a stripline geometry, will experience only near end noise.

While it is true that near end noise saturates in magnitude and does not scale with increasing coupling length, this only occurs if the coupling length is longer than a critical length, referred to as the saturation length. If the coupling length can be reduced below the saturation length, the near end noise will decrease with length.

The near end noise saturates and reaches a maximum when the time delay of the coupling length is half the rise time, or

$$\text{Len}_{\text{sat}} = v \times \frac{RT}{2} = \frac{12 \times RT}{2\sqrt{Dk}} = 3.5 \times RT$$

Where

Len_{sat} = saturated coupling length in inches

RT = signal rise time in nsec

Dk = bulk dielectric constant = 3

v = signal speed in the material in inches/nsec

For example, if the rise time is 0.5 nsec, the saturation length would be $3.5 \times 0.5 = 1.7$ inches. If the coupled length can be decreased below 1.7 inches, the near end cross talk will be reduced with shorter coupling lengths. But, if the coupled length is longer than 1.7 inches, the near end noise will not be affected by changes in the coupled length. (Figure 4)

In this example, when the coupled length is longer than 1.5 inches, the near end noise saturates and changing the length does not affect the near end noise. But, if interconnects can be shorter than the saturation length, the near end noise can be reduced by decreasing the interconnect length. Shorter

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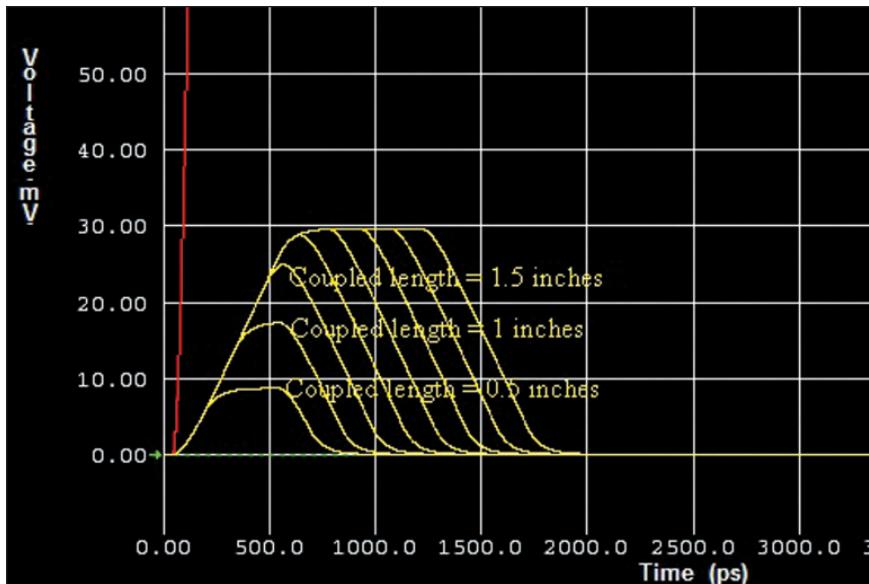


FIGURE 4: Near end noise for a 0.5 nsec rise time, 1 V aggressor signal, increasing the coupling length from 0.5 inches in 0.5 inch increments, simulated with Mentor Graphics' HyperLynx (www.mentor.com/products/pcb/analysis_verification/hyperlynx)

interconnect lengths in HDI boards can result in lower near end noise if the interconnect lengths can be driven below the saturation length.

Lower Cross Talk from Lower Dielectric Constant

There is another source of reduced cross talk from lower dielectric constant. If the cross section geometry is fixed and the dielectric constant is reduced, there is no impact on the cross talk. This is why it is generally believed that reducing the dielectric constant has no impact on cross talk.

However, if the dielectric constant is reduced and the geometry fixed, the characteristic impedance will go up. In order to bring the characteristic impedance back to the target value, typically 50 ohms, some other feature, like the dielectric

thickness, must change. When the dielectric constant is reduced, the dielectric thickness must be decreased to maintain the target impedance. It is the reduction in dielectric thickness that decreases the saturated near end cross talk coefficient.

The following table summarizes the dimensions for 50-ohm striplines with two different dielectric constants and cross sections. (Figure 5)

Trace thickness	0.1 oz	0.1 oz
Line width	2 mils	2 mils
Spacing	2 mils	2 mils
Dielectric constant	4.5	3
Dielectric thickness per layer	2.5 mils	1.7 mils

Even though these pairs of lines are each 50 ohms, with the same line and space, the closer spacing of the return planes for the lower dielectric constant material creates lower cross talk. In this example, the reduction in dielectric constant enables a reduction in near end noise from 60 mV out of a 1 v aggressor signal, or 6%, to 30 mV out of 1 v or 3%. This is a 50% reduction in cross talk possible by using lower dielectric constant material.

This is seen in the simulated saturated near end noise on the victim lines for 1 v signals on the aggressor lines in

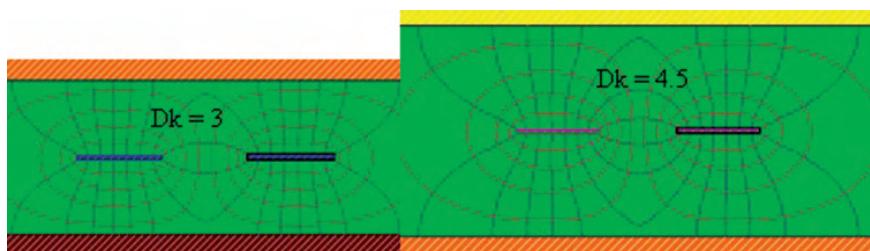


FIGURE 5: Stripline pairs with 50-ohm impedance, 2 mils wide with 2-mil spacing, but designed with $Dk = 3$ on the left and $Dk = 4.5$ on the right.

Electrical Performance

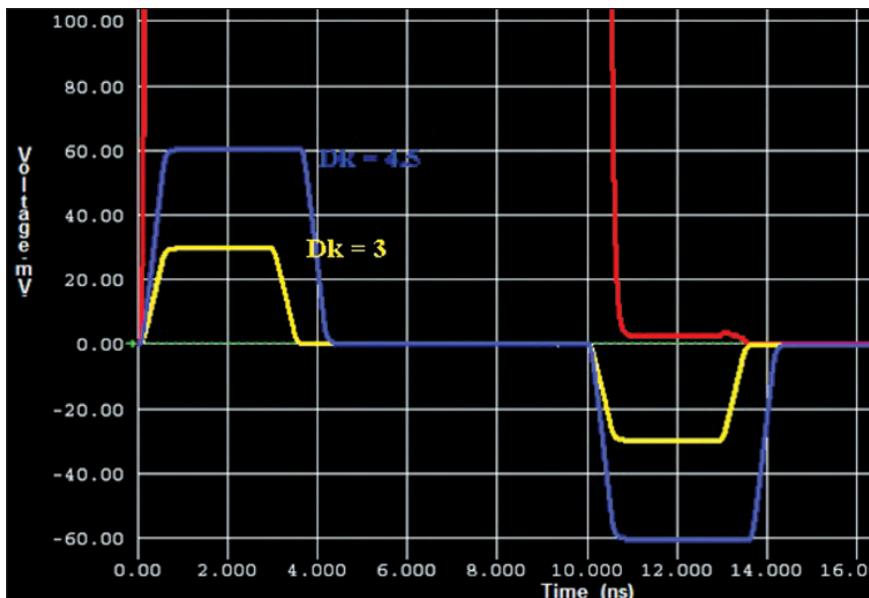


FIGURE 6: Near end noise on victim line for two different dielectric constants, simulated with Mentor Graphics' HyperLynx (www.mentor.com/products/pcb/analysis_verification/hyperlynx)

Figure 6. Of course, for the same level of cross talk, the line to line spacing could be decreased, resulting in even higher interconnect density.

Limitations from Scaling - Losses in the Lines

When all the cross section features are scaled down in size, though the impedance and cross talk remain the same, the narrower line width increases the series resistance of the signal traces.

The DC series resistance is roughly:

$$R_{DC} = \frac{\rho}{t} \times \frac{Len}{w}$$

Where

R_{DC} = DC resistance in ohms

ρ = bulk resistivity of copper, about 1.8 $\mu\text{hm}\cdot\text{cm}$

t = trace thickness in cm

Len = line length in inches

w = line width in inches

As frequency goes up, skin depth effects force the current to flow in only a thin region of the surface of the conductor. The effective conductor thickness decreases, which increases the resistance with frequency. When current is skin depth limited, the resistance of a surface trace is frequency-dependent. The higher the resistance, the higher the attenuation, and the larger the impact on rise time

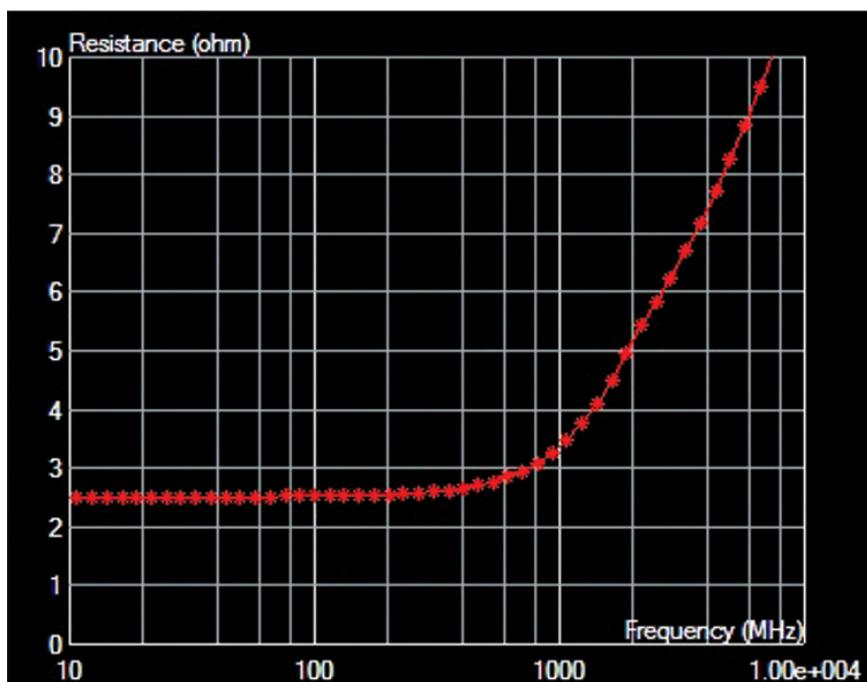


FIGURE 7: Resistance per length, in ohms/inch for a 2-mil wide line, and thickness of 3.5 microns, simulated with Mentor Graphics' HyperLynx (www.mentor.com/products/pcb/analysis_verification/hyperlynx)

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degradation.

The resistance per length of a 2-mil wide signal line is shown in Figure 7. When the skin depth is thinner than the geometric thickness, the series resistance is frequency-dependent and increases with the square root of frequency. For this example of 0.1 oz copper, a thickness of about 3.5 microns, the turn on of skin depth effects begins at about 500 MHz.

The series resistance is one of the loss mechanisms in interconnects. The other is dielectric loss. However, when the line width is less than 3 mils, even for the worst-case lossy materials, with a dissipation factor of 0.02, the resistive losses dominate and are the chief factors influencing the rise time degradation.

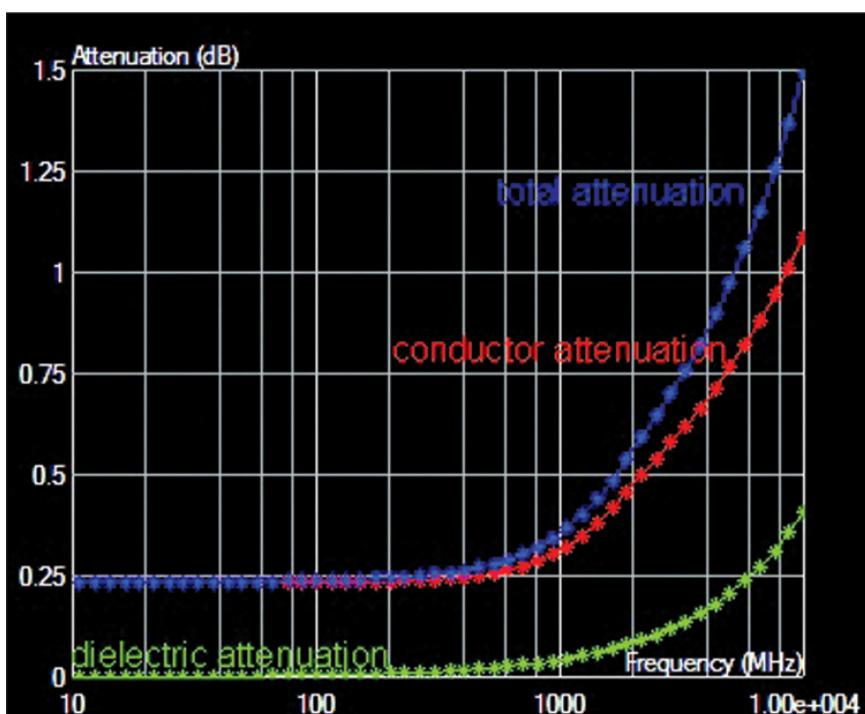


FIGURE 8: Relative contributions of attenuation per inch for conductor and dielectric loss, simulated with Mentor Graphics' HyperLynx (www.mentor.com/products/pcb/analysis_verification/hyperlynx)

Figure 8 shows the relative impact on attenuation from conductor and dielectric loss for a 2-mil wide line, assuming the dissipation factor of the dielectric is the typical value of $D_f = 0.01$.

This frequency-dependent resistance will cause the rise time to be degraded, and the impact on rise time will increase as the interconnect length increases.

Due to the complicated nature of the frequency-dependence of the series resistance and contribution of dielectric loss, it is difficult to estimate the rise time degradation just from the attenuation per length and interconnect length. However, it can be simulated for a few cases.

Figure 9 shows the impact on a 50 psec rise time signal entering a 2-mil wide interconnect for five different lengths, from 1 inch to 5 inches. The rise time increases as the interconnect length increases, due to the higher frequency-dependent attenuation.

In a 5-inch long interconnect, 2 mils wide, the rise time of the signal increases from 50 psec to about 100 psec. This will

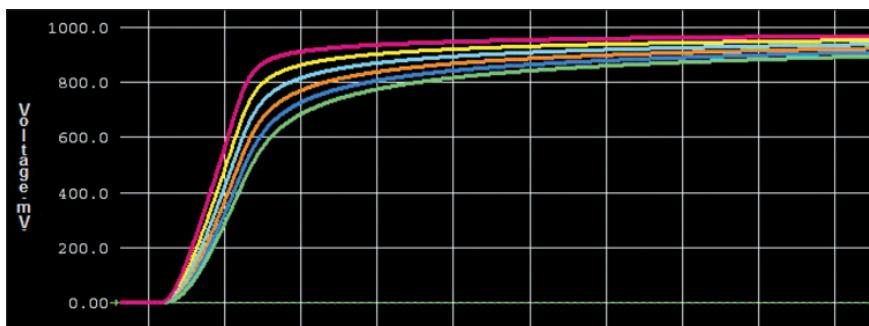


FIGURE 9: Output signals are shown in a 50-ohm interconnect using 2-mil wide traces for lengths of 1 inch to 5 inches in 1-inch increments. The top trace is the incident signal with a 50 psec rise time. The time positions of the signals were shifted for easy comparison. The time scale is 50 psec/div. Simulated with Mentor Graphics' HyperLynx (www.mentor.com/products/pcb/analysis_verification/hyperlynx)

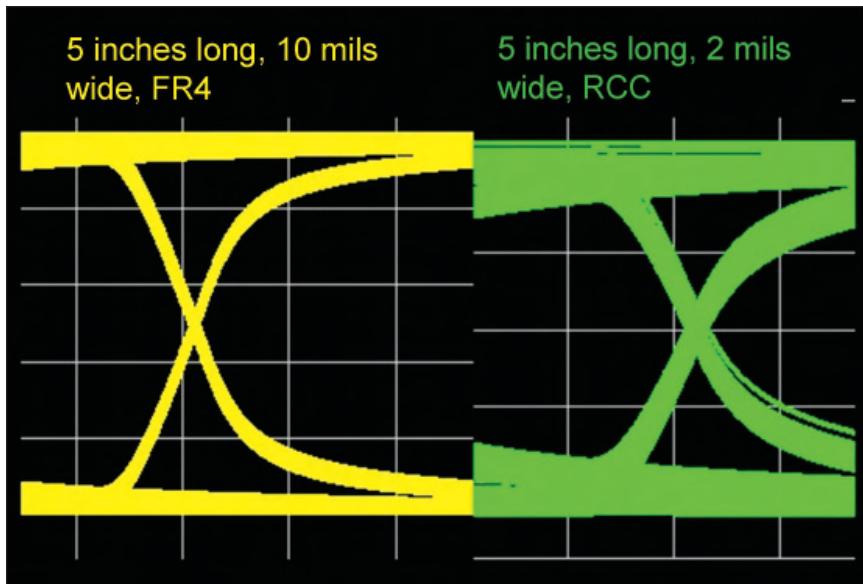


FIGURE 10: Eye diagrams of 5 Gbps PRBS data patterns, in a 10-mil wide interconnect and a 2-mil wide HDI interconnect, simulated with Mentor Graphics' HyperLynx (www.mentor.com/products/pcb/analysis_verification/hyperlynx)

have an impact only for circuits where 100 psec rise times are significant, which would typically be for clocks above 1 GHz. High speed serial busses would see an impact from the extra rise time degradation in long HDI interconnects.

For example, in 5 Gbps serial busses, such as PCIe Gen II, the eye diagram from a 5-inch long HDI interconnect would be noticeably collapsed compared to an equivalent length in conventional 10-mil wide signal lines. This is shown in Figure 10.

Of course, one way around the limitations of HDI interconnects is to route all the short, high-density interconnects in the HDI layers. All the signal paths longer than some length, like 5 inches, could be routed in the conventional core layers which might have line widths on the order of 7 to 10 mils.

In this partitioned approach, sometimes referred to as HDI/LDI, you get the best of both worlds. In a high-density system, most of the interconnects would be of short length, spanning two to three package pitch lengths, where high-density is required, while the fewer, longer interconnects might easily fit in the lower density, wider lines of the conventional line width PCB layers.

Signal Quality Problems from Vias

Vias have often received an undeserved bum rap. The widely held belief is that vias cause significant signal integrity problems. Most of the time, it is not the vias that cause the problems, it is the residual dangling stub, an artifact of the through-hole manufacturing process, that causes the problems.

Figure 11 shows the impact of a via stub in a typical through-hole via that connects a surface trace to a signal line on a signal layer nearby that has a dangling via stub. The

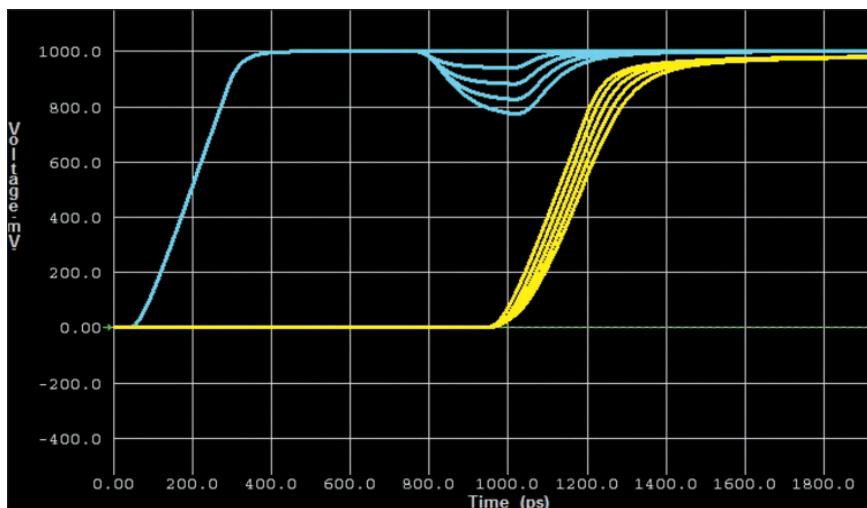


FIGURE 11: Reflected and transmitted response through a via with stub lengths of 0 through 200 mils, at 50-mil steps, for a signal rise time of 250 psec, simulated with Mentor Graphics' HyperLynx (www.mentor.com/products/pcb/analysis_verification/hyperlynx)

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length of the via stub is increased from 0 to 200 mils, in 50-mil steps.

Remove the via stub and virtually all of the issues of vias and problems with signal quality disappear. The primary benefit of the sequential buildup technology of HDI and microvias is from the structure of the vias. Each via only connects adjacent layers or between, at most, two layers, resulting in stub-less vias. The lack of stubs makes the vias nearly transparent up to bandwidths above 10 GHz.

Figure 12 shows the impact on a 250 psec rise time signal as it encounters a 35-mil long via in HDI layers.

As Figure 12 illustrates, the via is nearly transparent to the 250 psec signal. Most HDI vias would be significantly shorter than the 35 mils used in this simulation. A comparison of a 20 psec rise time transmitted signal through a microvia and a

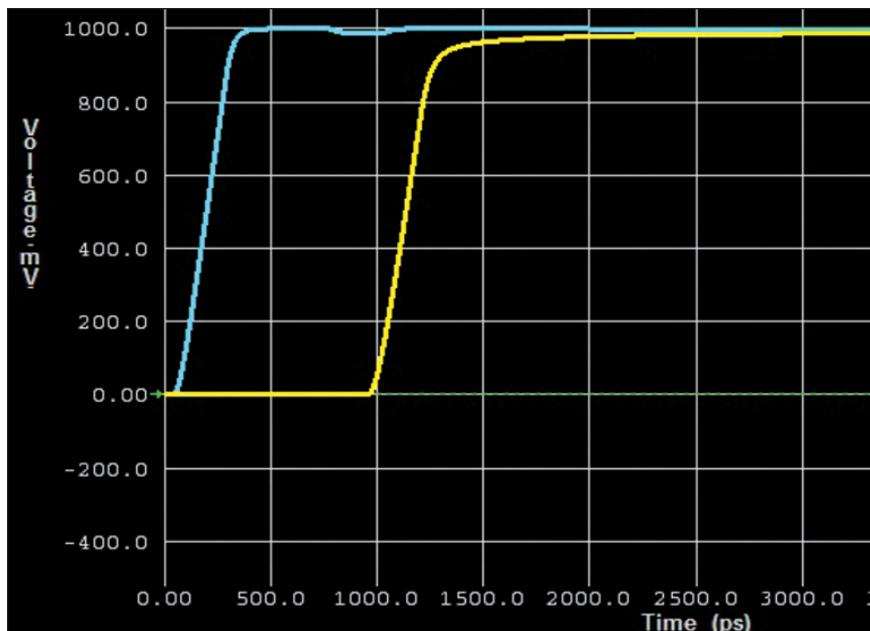


FIGURE 12: Reflected and transmitted response through a 35-mil long via in HDI layers, simulated with Mentor Graphics' HyperLynx (www.mentor.com/products/pcb/analysis_verification/hyperlynx)

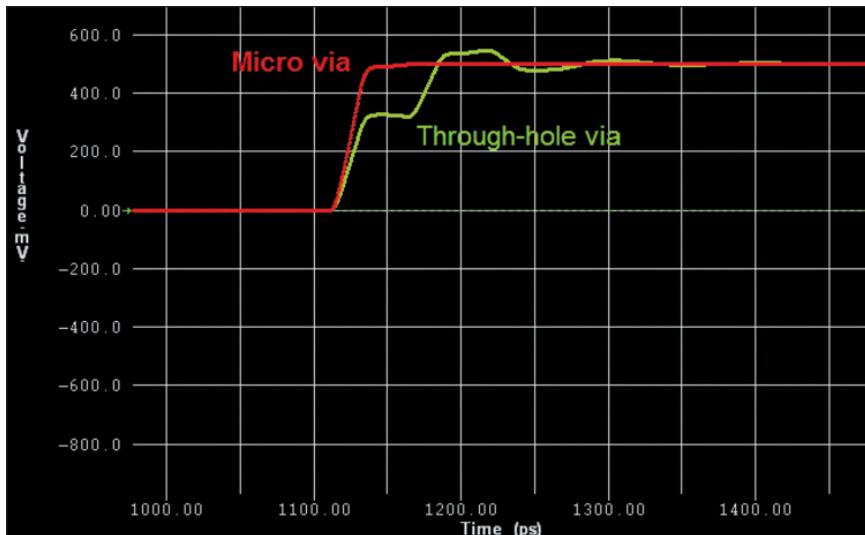


FIGURE 13: The impact on a 20 psec rise time signal through a microvia and a through-hole via having a 150-mil long stub, simulated with Mentor Graphics' HyperLynx (www.mentor.com/products/pcb/analysis_verification/hyperlynx)

through-hole via with stub is shown in Figure 13. This illustrates that the blind and buried vias inherent in the HDI fabrication process create vias that are effectively transparent even in extreme cases. The via structures in HDI layers are blind and buried vias, by design. The fact that they are also short is a small factor, but is also an electrical advantage of microvias.

Of course, in addition to the signal via, an adjacent return via is assumed for all of these via simulations. It is a good design practice to assure low cross talk into the plane cavities that make up the return planes.

Enhanced Power Delivery Network (PDN) Design

The last electrical area where HDI structures enable enhanced performance over through-hole laminated boards is in the PDN.

Electrical Performance

The PDN encompasses all of the interconnects, from the pins of the voltage regulator module (VRM) to the voltage rail pads on the chip, including the packages, the power and ground planes, all the vias, and the decoupling capacitors on the board.

The goal of the PDN is to keep the voltage across the pads of the die constant to within the ripple spec, which is typically $\pm 5\%$. As current from the chip fluctuates and flows through the impedance of the PDN interconnects, voltage drops are generated which cause the voltage delivered to the chip to fluctuate.

The voltage drop in the PDN interconnects can drive EMI, so minimizing the voltage drop in the PDN will also minimize EMI.

The most important design guideline to minimize the voltage noise in the PDN is to minimize the impedance of the PDN. The impedance needs to be low from DC up to the bandwidth of the currents that might switch in the interconnects. Depending on the type of packages used and the amount of capacitance on the die, the typical maximum board level frequency that is important for the PDN is about 100-300 MHz.

At the higher frequency end, the most important electrical quality that influences the impedance of the PDN is the loop inductance of each element that makes up the PDN. The goal of minimizing the impedance of the PDN is really to minimize the inductance of the components. This is accomplished by following three important guidelines:

- **Use the right values and the right number of capacitors to keep the impedance profile below the maximum allowable level.**
- **Use power and ground planes with a dielectric between**

the planes that is as thin as possible.

- **Minimize the mounting inductance between the decoupling capacitors and the pads on the chip.**

Four important qualities of HDI designs enable better PDN performance:

- **thinner dielectric layers between the power and ground planes**
- **via-in-pad geometry when mounting the decoupling capacitors**
- **use of copper-filled top layers for power islands**
- **placing the nearest cavity plane very close to the surface of the board**

The impedance a package pin would see looking into the power and ground planes depends on the size of the planes and their spacing. At low frequency, the impedance is related to the capacitance between the planes. At high frequency, the impedance is related to the loop inductance between the planes.

The loop inductance between two planes depends on the geometry. When the thickness (h) between the planes is thin compared to a lateral dimension, the loop inductance from one edge to the opposite edge of the pair of planes is:

$$L_{\text{loop}} = \mu_0 \times h \times \frac{\text{Len}}{w} = 32\text{pH/mil} \times h \times \frac{\text{Len}}{w} = L_{\text{sq}} \times n$$

where

L_{loop} = loop inductance in nH

μ_0 = permeability of free space = $4\pi \times 10^{-7}$ H/m = 32 pH/mil

h = spacing between the planes in mils

Len = length of one side of the planes in inches

w = width of the planes in inches

L_{sq} = sheet loop inductance in nH/square = 32 pH/mil x h

n = number of squares = Len/w

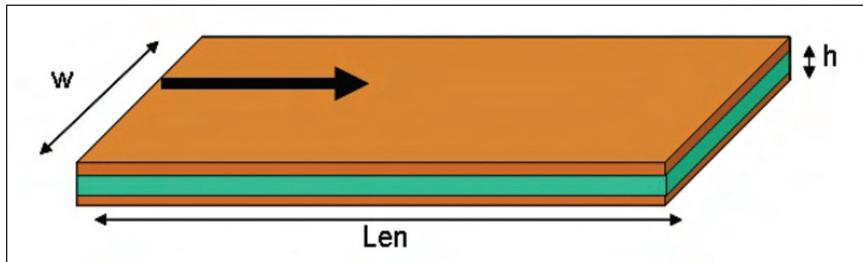


FIGURE 14: Loop inductance between edges of a pair of planes with a high aspect ratio

The loop inductance between edges of the pair of planes can be described in terms of the sheet loop inductance multiplied by the number of squares. The sheet inductance is the loop inductance of one square of planes. Sheet inductance is a very good metric for the spreading inductance from a pin's via contact into the cavity made up by the planes, looking outward into the rest of the planes.

Sheet inductance is simply 32 pH/mil x h. The thinner the cavity thickness between the power and ground planes, the lower the spreading inductance, and the lower the impedance of the planes at high frequency.

Figure 15 shows the impedance a package pin would see, looking into the cavity of the power and ground planes for a board 4 inches on a side

The thinner dielectric that is routinely possible with sequential buildup fabrication, means that the impedance between the power and ground planes can be kept to a minimum.

The second feature that contributes to the low impedance in the PDN is the loop inductance between the decoupling

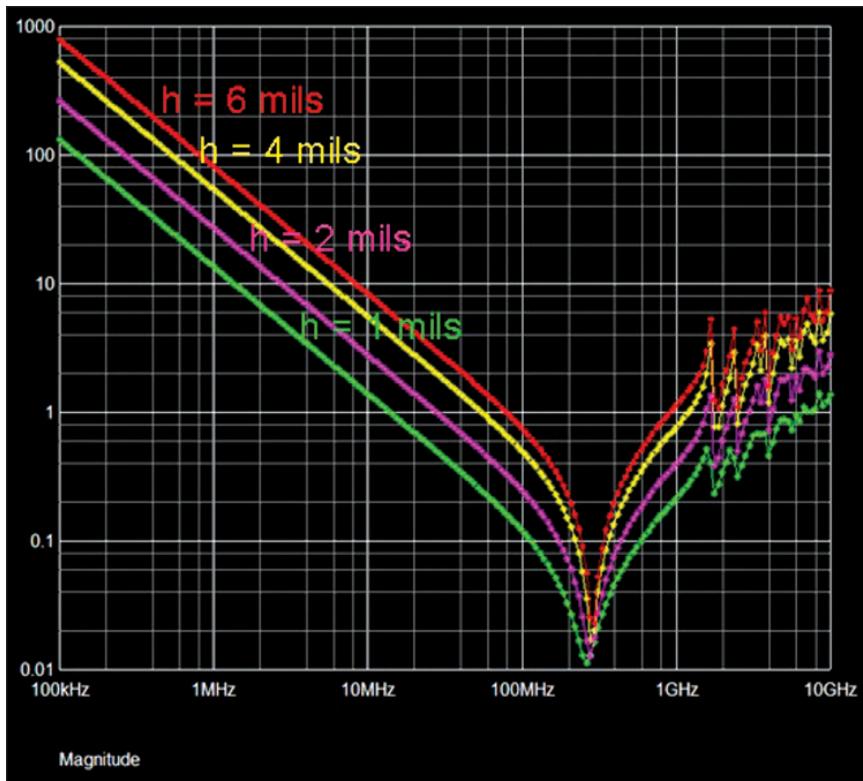


FIGURE 15: This graph illustrates the impedance profile of planes with different spacing, from 6 mils to 1 mil. The thinner the spacing, the lower the impedance. Simulated with Mentor Graphics' HyperLynx (www.mentor.com/products/pcb/analysis_verification/hyperlynx)

capacitor and the package it is decoupling. It is the entire path that contributes to the loop inductance. (Figure 16)

The loop inductance from the decoupling capacitors to the package pins can be divided into three sections. The first section is the loop inductance of the capacitor itself to the board. This is dominated by the mounting surface traces of the capacitor and the capacitor body. The distance from the top of the cavity to the top of the board, where the capacitor is located, will strongly influence the loop inductance.

Obviously, minimizing this inductance requires surface traces

Electrical Performance

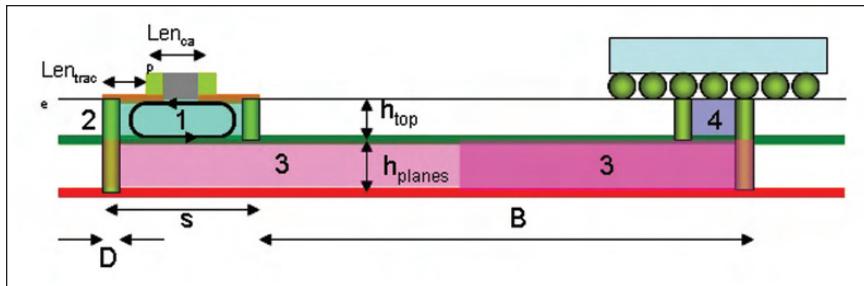


FIGURE 16: Cross section of the current path from the decoupling capacitor to the package pin

that are as short as possible. This is why via-in-pad is so beneficial. It dramatically reduces the mounting inductance.

The second contribution to loop inductance is from the vias between the surface pads and the cavity created by the power and ground planes. The closer the cavity is to the top surface, the lower the loop inductance of the vias.

The third contribution is the spreading inductance in the planes, which is related to the sheet inductance of the cavity. The thinner the dielectric of the cavity, the lower the spreading inductance.

Using simple approximations, the loop inductance from each of these regions can be estimated to compare design choices. In the following, three examples are compared, each using an 0603 capacitor located 0.5 inches from the BGA pin it is decoupling.

Case 1: Conventional approach – 50-mil long surface traces, 50 mils wide, with a cavity 5 mils thick located 10 mils from the surface of the board

Case 2: Same as Case 1, but with HDI technology, using via-in-pad and dielectric 2 mils thick

Case 3: Same as Case 2, but using a copper-filled power island on the top surface so that the top layer makes up part of the power and ground cavity



FIGURE 17: Analysis of the loop inductance contributions for the three cases described in the text, simulated with the ESL Virtual Lab Bench on www.beTheSignal.com

The loop inductance of the conventional case of a capacitor attached with just one square of trace connecting the capacitor pads to the via, offers a loop inductance of about 1.7 nH. This is a very low loop inductance.

By using via-in-pad technology, the loop inductance of the surface traces can be eliminated, and by reducing the cavity thickness, the spreading inductance can be reduced. The loop inductance after these two changes is reduced to 0.8 nH, a significant reduction.

Finally, by using the top surface as a power island and connecting the decoupling capacitor to the top power plane

Electrical Performance

and to the ground plane 2 mils below, the loop inductance is dominated by the small amount of capacitor body loop inductance and the spreading inductance in the cavity. This can be reduced to 0.44 nH.

The ability to get the lower loop inductance in the cavity when the top layer is a copper-filled power island is based on the fact that the dielectric layer between the signal and nearest return plane must be thin anyway in order to achieve a 50-ohm impedance for signal lines on that layer.

If the top layer is nominally a signal layer, with line widths on the order of 3 mils, the distance to the nearest ground layer beneath it must be less than 2 mils for 50 ohms. This means that if copper fill is used on the signal layer as a power island, it will create a cavity with a ground layer that is very thin and has very low spreading inductance.

By incorporating the features of HDI technology, such as via-in-pad, thin cavity, and copper-fill power islands on the surface, it is possible to reduce the loop inductance between decoupling capacitors and the package pin they decouple, by a factor of more than 4 over the best case with conventional board technology. These three cases offer a simple comparison of how different design choices enabled by HDI technology can dramatically improve the PDN performance.

Summary

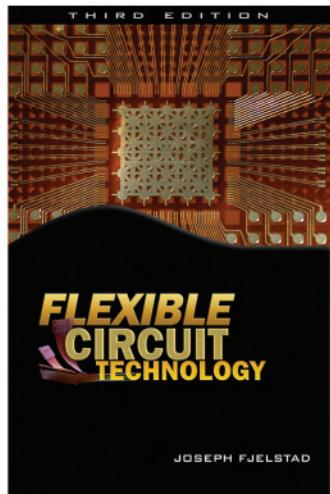
When the design is constrained by conventional through-hole circuit board technology, with its coarser feature set, thicker dielectrics, and via stubs, it is increasingly difficult, in some designs, to achieve cost/performance tradeoffs in high performance designs. HDI technology, with its finer features, thinner-layers, and inherent blind and buried via technology, can sometimes offer a different set of constraints and a cost

structure which can enable the design to jump to a different cost/performance curve. In higher performance designs, this can sometimes mean providing higher performance at lower costs.

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1. Bogatin, E., Signal Integrity Simplified, published by Prentice Hall, 2004.
2. www.beTheSignal.com
3. Additional reading

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Flexible Circuit Technology has become one of the most popular texts available on the subject as a result of its simple approach to tackling this important technology. The book was written to provide a bridge of understanding by offering a clearly defined set of steps which take the reader from basic concepts to a more detailed review of the various methods and materials that must be brought together to create these modern wonders of electronic interconnection wizardry.



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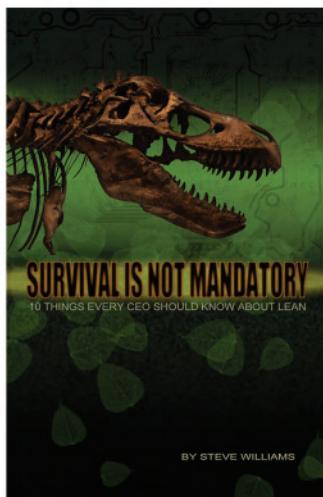
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5

Materials for HDI

By John Andresakis — Oak Mitsui

In this chapter we will discuss the materials used to manufacture HDI circuits. Several good resources exist on the subject of materials for PCBs (such as the *Printed Circuits Handbook* edited by Coombs) so we will concentrate on those materials that are specific to HDI. That being said, since most HDI boards include layers that are like traditional PCBs, a general overview will be helpful.

The current HDI materials market worldwide (in 2006) was estimated by BPA Consulting Ltd. to be 51 million square meters. Figure 1 shows a breakdown by BPA Consulting [1] of the eleven HDI materials used. The 11 materials are, in order of usage :

- **Laser Drillable Prepregs-38.4%**
- **RCC-28.3%**
- **Conventional Prepregs-19.2%**
- **ABFilm-5.0%**
- **Epoxy-3.3%**
- **Other-3.2%**
- **BT-1.8%**
- **Aramid-0.4%**
- **Polyimide-0.3%**
- **Photo Dry film-0.1%**
- **Photo Liquid-~0.0%**

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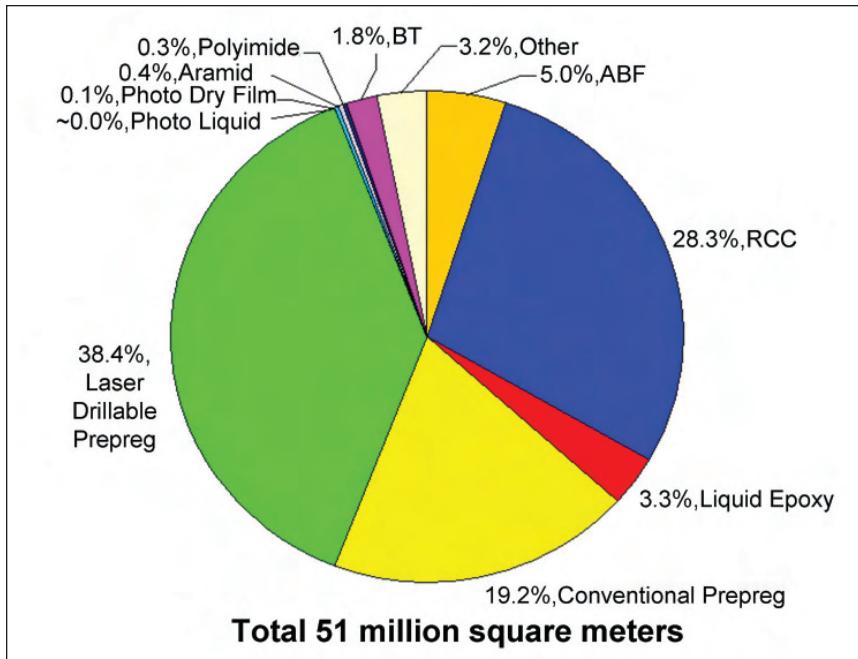


FIGURE 1: Breakdown of the HDI materials market in 2006 (Courtesy of BPA Consulting)

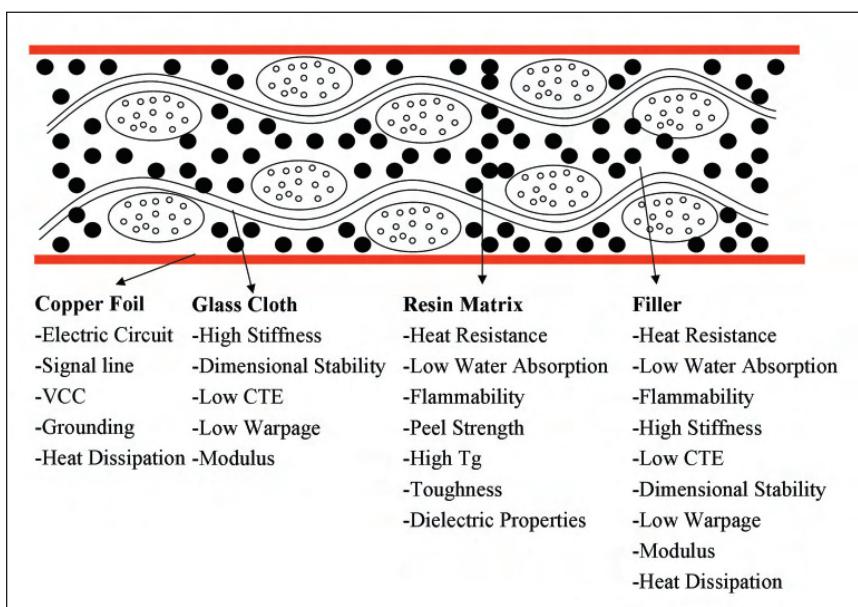


FIGURE 2: Composition of laminate and its functions

The HDI Handbook

Type of Materials Suppliers	Thermally Cured Resins (Tg)					Photo Cured Resins	
	Halogen-free	LD Prepregs	RCC	Film Type	Ink Type	Film Type	Ink Type
Isola	X		150 160				
Polyclad			165 200				
Nelco			180				
NanYa	X	X	172 180				
Asahi Chemical			X	X			
Ajinomoto Fine Technology	X		177	9X	X		
Tamura Kaken					X		X
Shipley Far East							X
Taiyo Ink			UD	UD	X		X
Chubu Specialty Chemical							X
Oy Pent						X	
Tokyo Ohba Kogyo					X		
Hilachi Chemical			135 190	X		X	
Asahi Denka Kogyo					X		X
Toshiba Chemical			X				
Matsushita Electric Works	X		170 155				
Mitsubishi Gas Chemical			220				
Nippon Industries			X				
			150 190 130 165				
Mitsui Metal & Mining	X	X					
Sumitomo Bakelite			X	X			
Nippon Paint						X	X
Doosan	X		145 185				
Grace Electron			X				
Sheng Yi	X	X	155 165				

FIGURE 3: This survey of HDI materials including thermally cured and photo-cured types contains laser drillable laminates, buildup films, RCF, and liquid dielectrics. Conventional laminates were excluded.

The major material components of PCBs are the polymer resin (dielectric), with or without fillers, reinforcement, and metal foil. To form a PCB, alternate layers of dielectric, with or without reinforcement, are stacked in between the metal foil layers. A typical stack-up is shown in Figure 2.

Figure 3 shows a current list of HDI materials taken from the Internet. The majority of the materials are epoxy, but some are BT, PPE, cyanate ester, and modified acrylates. The newest materials are the growing number of laser drillable preprints.

Resins

There have been many advances in the resins used to make PCBs over the years. The backbone of the industry has been the epoxy resin. Epoxy has been a staple due to its relatively

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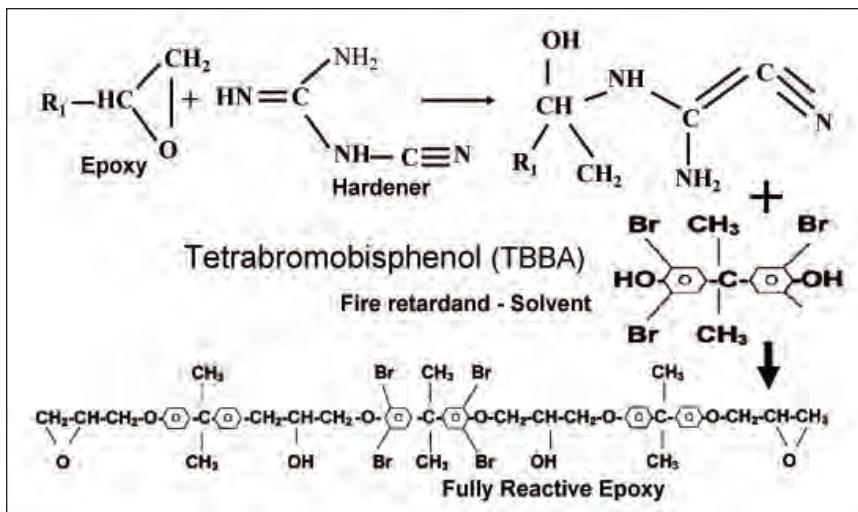


FIGURE 4: Resin composition of laminate and bromine flame retardants for most modern laminates

low cost, excellent adhesion (both to the metal foils and to itself), and good thermal, mechanical, and electrical properties. As demands for better electrical performance, ability to withstand lead-free solder temperatures, and environmental

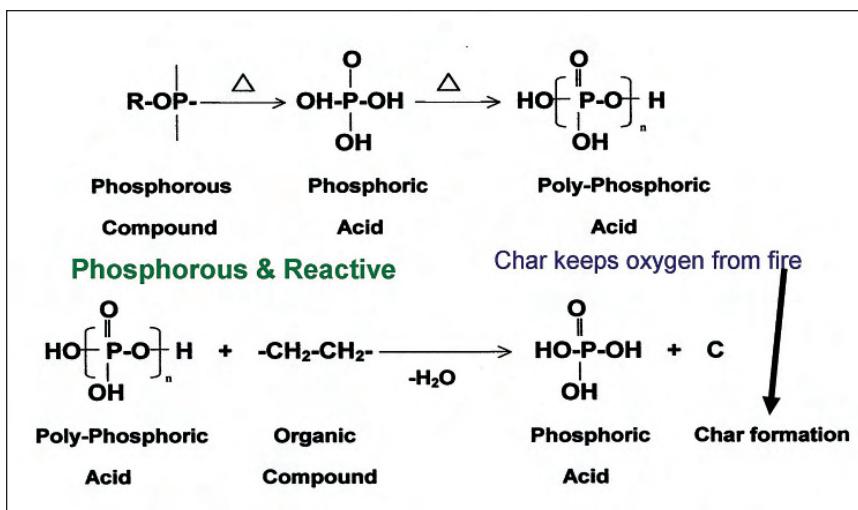


FIGURE 5: Composition of halogen-free fire retardant like phosphoric acid, which is a char producer

compliance have entered the picture, the basic epoxy chemistry has been dramatically changed over the years.

Epoxies are thermosetting resins and use hardeners and catalysts to facilitate the cross-linking reactions that lead to the final cured product (see Figure 4). Epoxies are also inherently flammable, so flame retardants are incorporated into the resin to greatly reduce the flammability. Over the last several years, resins have been modified to change the curing chemistry to make the resins more robust during the higher temperatures of lead-free soldering. Traditionally, the main curing agent was Dicy, but now various phenolic compounds are used. The traditional bromine compounds (i.e., TBBA) used as flame retardants are being substituted with other compounds such as those containing phosphorous because of concerns about bromine getting into the environment when the PCBs are disposed of. As of the writing of this book, the use of the standard bromine compound, TBBA, is not restricted, but many companies have gone to a Halogen-Free requirement in anticipation of an eventual ban or for the appearance of being green (Figure 5).

Other resins are in common use and are typically chosen to address specific weaknesses of epoxy systems. BT-Epoxy is common for organic chip packages due to its thermal stability, while polyimide and cyanate ester resins are used for better electrical properties (lower Dk and Df) as well as improved thermal stability. These resins are more expensive than epoxy and are used only as needed. Sometimes they will be blended with epoxy to keep costs down and improve mechanical properties.

Besides thermosetting resins, thermoplastic resins are utilized, including polyimide and polytetrafluoroethylene (PTFE). Unlike the thermosetting version of polyimide, which

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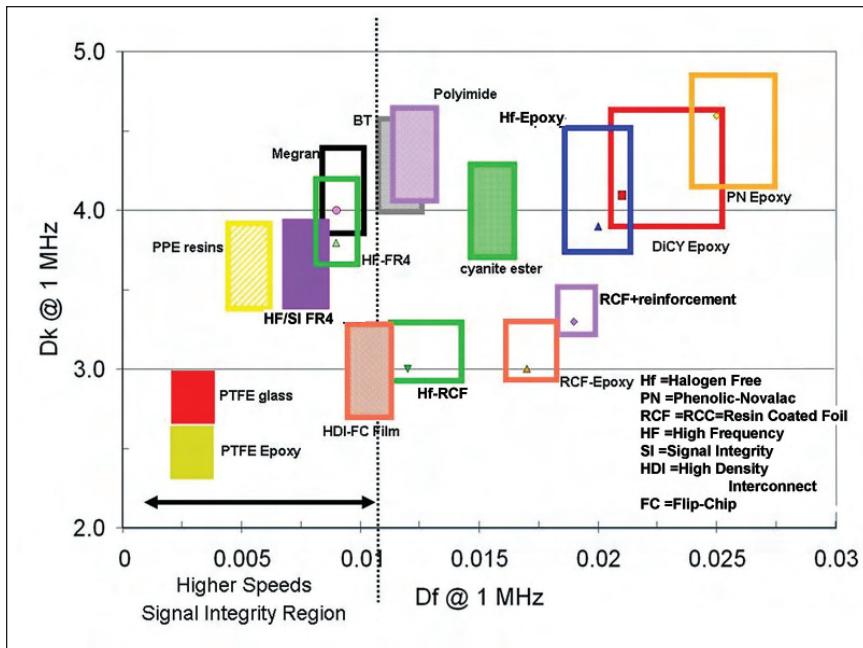


FIGURE 6: Chart of typical epoxies and other resins and their electrical properties

is relatively brittle, the thermoplastic version is flexible and is supplied in film form. It is typically used to make flexible circuits as well as the combination circuits called rigid-flex. The polyimide film can be made in several ways, and is usually supplied as a completely cured laminate with copper foil on one or both sides. It is also more expensive than epoxy and is only used as needed. Figure 6 shows the range of electric properties of all the common HDI dielectrics.

PTFE is valued for its excellent electrical properties and low moisture absorption. It typically has filler added to modify its dielectric constant for specific applications. A typical example is a circuit used in microwave applications where low loss and high Q are needed at very high frequencies.

PTFEs are among the most expensive materials, but as frequencies continue to rise and wireless applications grow,

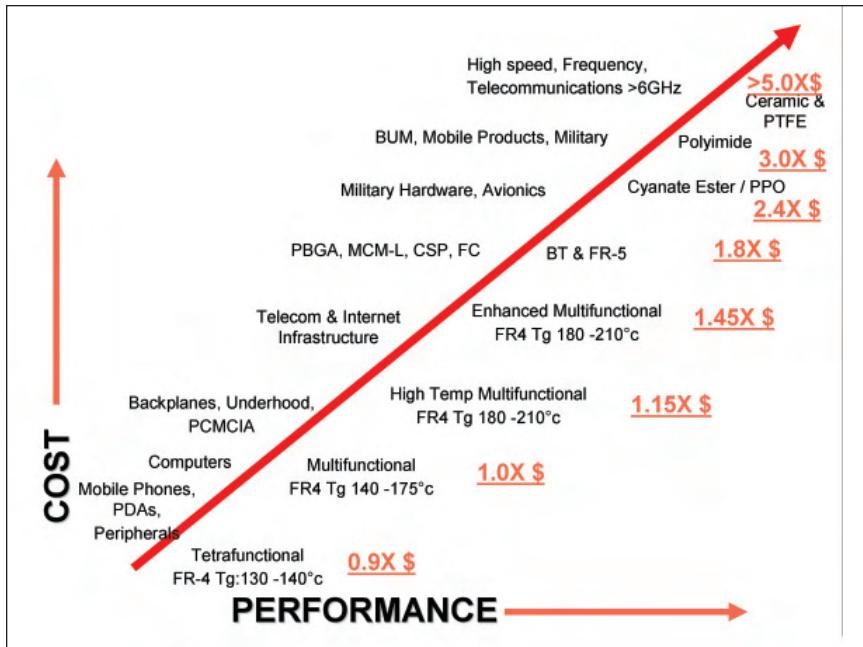


FIGURE 7: Chart of relative costs of dielectrics compared to their performance

their use continues to grow. Figure 7 summarizes the cost and performance of all the common dielectrics for HDI boards.

Reinforcements – Laser Drillable and Conventional Fiberglass

Most of the dielectric materials that are used to make printed circuit boards incorporate reinforcement into the resin system. Reinforcement usually takes the form of woven fiberglass. Woven fiberglass is just like any other cloth, made up of individual filaments that are woven together on a loom. By using different diameter filaments and different weave patterns, different styles of glass cloth are created.

Fiberglass adds both mechanical and thermal durability to the dielectric, but it does present some problems when used in HDI constructions. Figure 8 shows that glass fabric is

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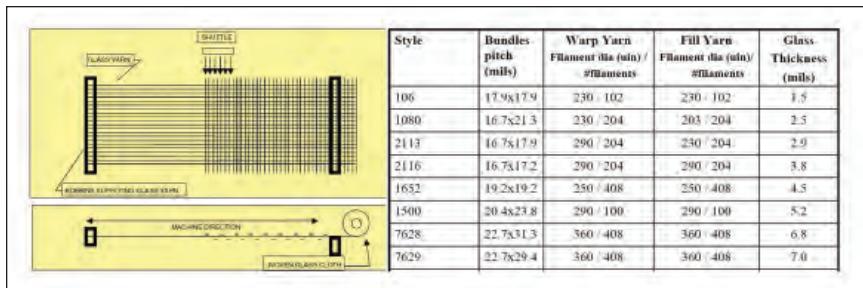


FIGURE 8: Picture of glass cloth manufacturing and table of glass cloth styles

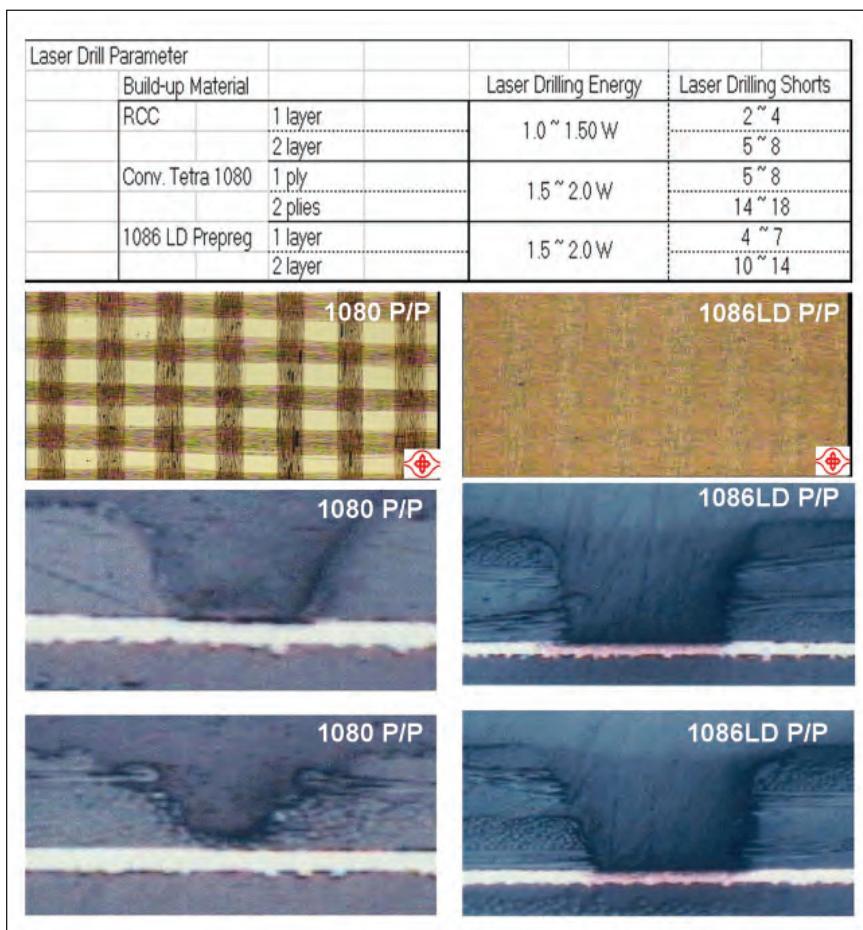


FIGURE 9: Laser drilled vias and the conventional fiberglass reinforced dielectric used compared to the new laser drillable prepgres (Courtesy of NanYa Plastics)

woven and the table in Figure 8 shows the styles, yarns, and thicknesses of those yarns. When lasers are used to create the vias, the difference in ablation rates between the fiberglass and the surrounding resin can cause poor hole quality. Also, since the fiberglass cloth is not uniform due to having areas with no glass, areas with one strand, and the intersections of strands (also known as knuckles), it is difficult to set up drilling parameters for all these regions. Usually the drilling is set up for the hardest to drill region which is the knuckle area. Figure 9 shows some examples of poor hole quality due to laser ablation of fiberglass reinforced dielectrics and the improvement with the new laser-drillable prepregs (LDP).

The fiberglass manufacturers have been working on ways to minimize drilling problems. They have created so-called laser-drillable dielectrics by spreading the yarns in both directions and making the fabric more uniform which minimizes the areas with no fiberglass, as well as the knuckle area. Figure 10

Cloth Style	Warp x Fill	Glass Cloth Thickness (mm)		Air Permeability (M3/M2min)		Warp & Fill Yarn Width (mm)			
		Standard	LDP	Standard	LDP	Warp	Fill	Warp	Fill
1015	75 X 75	--	0.020	--	23-45	--	--	0.163	0.270
1027	75 X 75	--	0.020	--	22-42	--	--	0.163	0.270
1037	71 X 74	--	0.025	--	20-40	--	--	0.210	0.270
106	56 x 56	0.037	0.028	120-140	20-40	0.138	0.254	0.163	0.385
1067	70 x 70	--	0.033	--	9-14	--	--	0.215	0.351
1078	54 x 54	--	0.044	--	9-14	--	--	0.255	0.419
1080	60 x 48	0.055	0.045	85-105	20-40	0.213	0.296	0.283	0.413
1086	60 x 61	--	0.047	--	6-10	--	--	0.285	0.398
2112	40 x 40	0.071	0.069	60-75	5-20	0.318	0.439	0.356	0.537
2113	60 x 56	0.070	0.065	32-50	4-12	0.302	0.319	0.329	0.452
2313	60 x 64	0.072	0.067	17-30	3-8	0.308	0.311	0.313	0.403
2116	60 x 58	0.092	0.088	8-18	5-10	0.360	0.365	0.365	0.395

FIGURE 10: Table of laser drillable fiberglass

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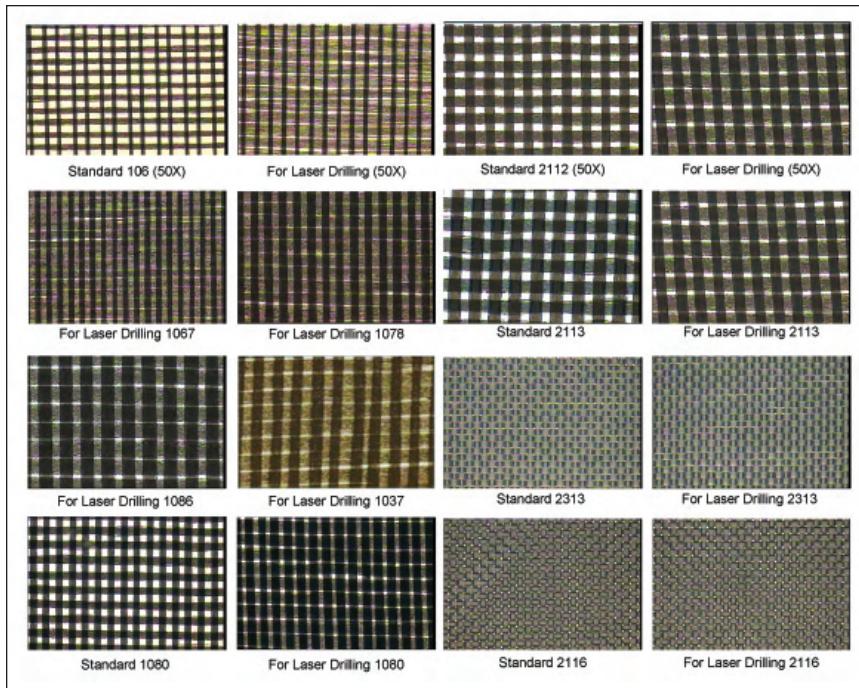


FIGURE 11: Close-ups of conventional pre-prints and laser drillable fiberglass pre-prints (Courtesy of NanYa Plastics)

shows the 12 currently available LDPs and their properties. It still takes more energy to penetrate the fiberglass than the resin, but now the drilling parameters can be optimized to get consistent results throughout the panel. Figure 11 shows examples of these new types of fiberglass cloth.

Another characteristic of woven fiberglass is the type of glass that is used to make the filaments. The differences among the various types of glass are the amount and type of each oxide incorporated into the material. The most standard type of glass used in the industry is called E glass which has very good mechanical properties and adequate electrical properties. However with electronics running at higher speeds there has been increased interest in other types of glass that have better electrical properties (lower Dk and Dj). D glass and SI glass

Property	Units	Si Glass	E Glass	Components	Units	E-Glass	D-Glass	T-Glass	S-Glass	Si-Glass
Coefficient of Expansion	ppm/ $^{\circ}$ C	3.4	5.5	SiO ₂	Wt %	52-56	72-76	62-65	64-66	52-56
Heat of Conductivity	Kcal/mh $^{\circ}$ C	0.86	0.89	CaO	Wt %	16-25	0	0	0	0-10
Specific Heat	cal/g $^{\circ}$ C	0.206	0.197	Al ₂ O ₃	Wt %	12-16	0-5	20-25	24-26	10-15
Dielectric Constant	1 MHz	4.4	6.6	B ₂ O ₃	Wt %	5-10	20-25	0	0	15-20
Dissipation Factor	1 MHz	0.0006	0.0012	MgO	Wt %	0-5	0	10-15	9-11	0-5
				Na ₂ O, K ₂ O	Wt %	0-1	3-5	0-1	0	0-1
				TiO ₂	Wt %	0	0	0	0	0.5-5

FIGURE 12: Comparison of E-glass, T-glass, S-glass, D-glass, and Si-glass

have started to get used in PCBs laminates allowing doubling of high-speed signals. Fabric manufactured with this type of glass is more expensive and only used when necessary. It is also used in conjunction with high-performance resin systems making the resulting dielectric relatively expensive. Figure 12 compares these glass properties.

Other Reinforcements

Other reinforcements have been used to make PCBs over the years. One product that is no longer available is a chopped aramid fiber paper called Thermount. It was supplied by DuPont and had a number of good properties. Being a thermoplastic material, it laser ablated more like the resin and, since it was a paper, it did not have the issue of knuckles to deal with like woven fabric. It also had a very good dielectric constant which was an advantage for high-speed circuitry. Thermount had some issues with moisture absorption and was relatively expensive. In 2006, DuPont decided to discontinue manufacturing this product. However, Shin-Kobe Electric in Japan still manufactures three different types of aramid laminate and prepreg. Alternatives to this product are still being investigated.

In addition to Thermount, other nonwoven reinforcements have been used, including a chopped fiberglass paper, as

well as an expanded PTFE matrix. The PTFE matrix has been incorporated with a high performance resin and is available as a product called GorePly. While GorePly has excellent electrical properties, it is expensive and only used when necessary.

Non-Reinforced Materials

Resin Coated Copper (RCC) Foil

The limitations of fiberglass-reinforced dielectrics prompted companies to look at alternative dielectric solutions. In addition to the problems with laser drilling (poor hole quality and long drilling times), the thickness of woven fiberglass available limited how thin the PCBs could be. To overcome these issues the copper foil was utilized as a carrier for the dielectric so it could then be incorporated into the PCB. RCC foil is manufactured using a roll to roll process as shown in Figure 13.

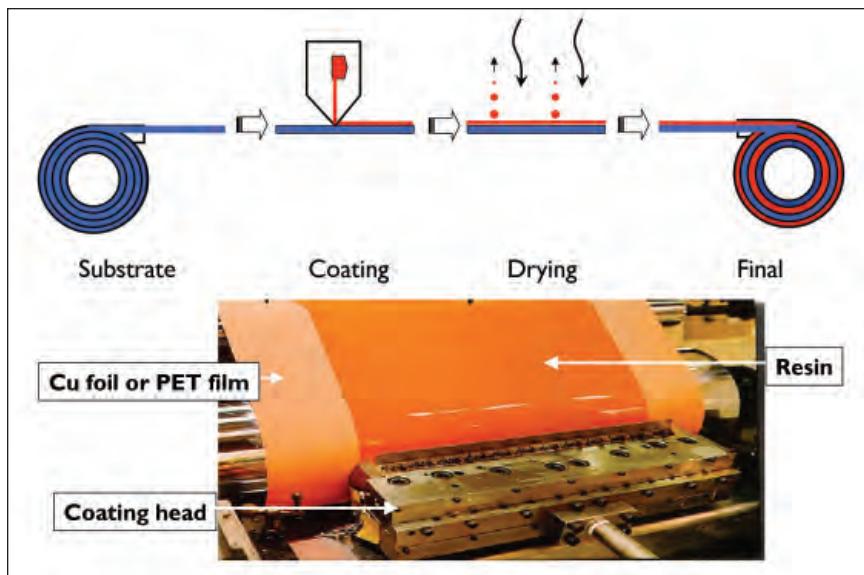


FIGURE 13: Picture of coating RCC

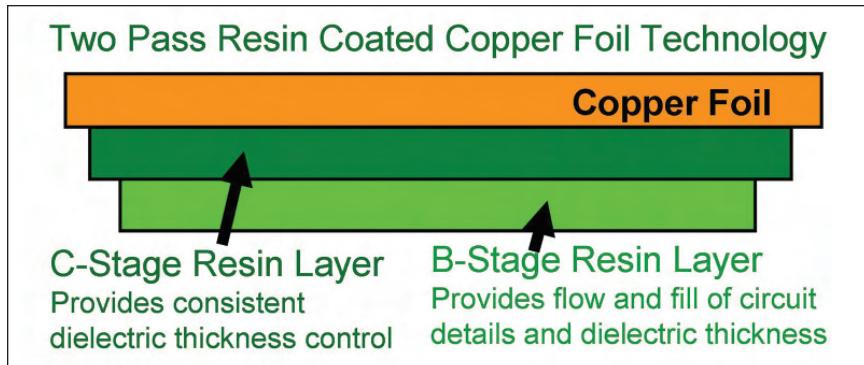


FIGURE 14: Picture of two-stage coating RCC

The copper goes through a coating head and the resin is deposited on the treated side of the copper. The resin coated foil then goes through drying ovens and is partially cured or B staged which will allow it to flow and fill in the areas around the internal circuitry and bond to the core. The resin systems are usually modified with a flow restrictor to prevent excessive squeeze-out during the lamination process.

Most of the RCC foil is manufactured this way, but additional types exist. One of these types is a two-stage product (Figure 14). After the first resin layer is coated, it is put through the coater again to add a second layer. During the second coating the first layer is fully cured, while the second layer is B staged. The benefit of this process is that the first stage acts like a hard stop and guarantees a minimum thickness between layers. The disadvantage is that the product is more expensive than the single coated version.

For all the benefits of RCC foil, there are concerns over the lack of reinforcement in terms of dimensional stability and thickness control. A new material was developed to address these concerns. MHCG from Mitsui Mining and Smelting incorporates an ultra-thin fiberglass (either 1015 or 1027) during the resin-coating process. The fiberglass is so thin that

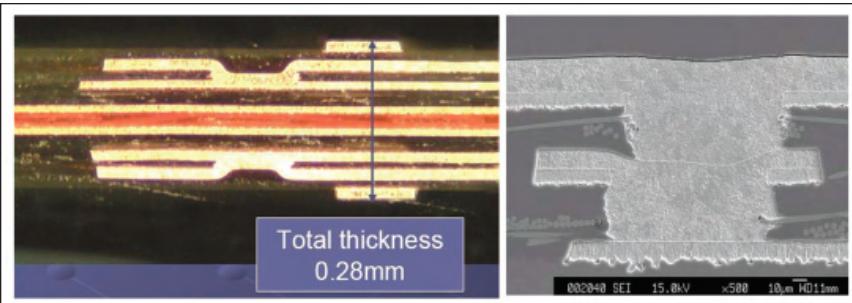


FIGURE 15: Picture of Fiberglass reinforced R-CCF (Courtesy of Oak-Mitsui)

it cannot be made into a prepreg since it cannot go through a treater tower like traditional fiberglass (Figure 15).

The fiberglass does not impact laser drilling significantly, yet it provides dimensional stability equal to or better than standard prepreg. Dielectric layers as thin as 25 microns are now available allowing for very thin multilayer products.

Cost is another aspect of RCC foil that is of concern. RCC foils almost always cost more than the equivalent prepreg/copper foil combination (Figure 16). However, the RCC foil can

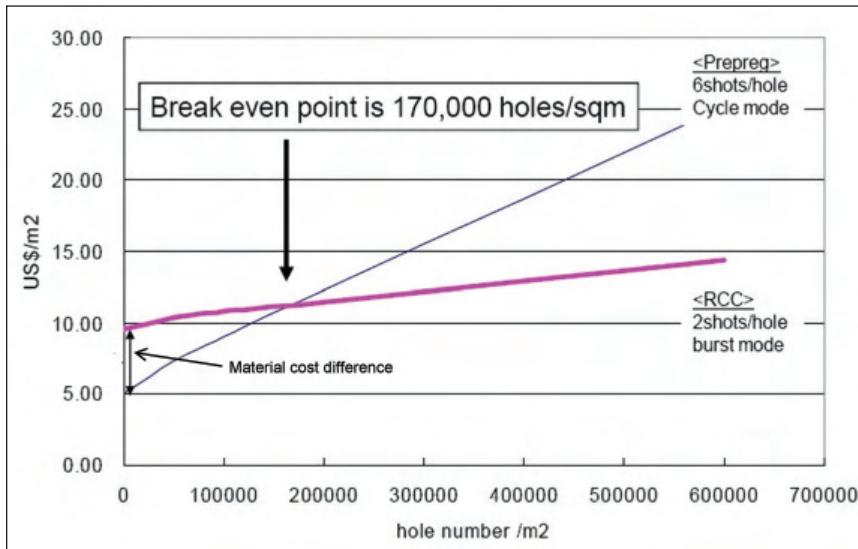


FIGURE 16: Hole density compared with the cost of drilling and materials (Courtesy of Oak-Mitsui)

actually result in a less expensive product when laser drilling time is taken into consideration. As the number of holes and size of the area increase, the improved throughput of the laser drills more than offsets the increased cost of the RCC foil.

Ajinomoto Buildup Film

The Ajinomoto Buildup Film (ABF) is a series of very thin film dielectrics made with epoxy/phenol hardener, cyanate ester/epoxy, and cyanate ester with thermosetting olefin (Table 1). The epoxy type is also available halogen-free. The thin film (15 – 100 um thick) is supported by a 38 um PET film and protected by a 16 um OPP cover film. The material is vacuum laminated in special conveyorized machines (Figure 17) using a five-step process:

- Surface preparation of core dielectric and copper
- Dry core (130° C for 30 min)
- ABF auto-cutting, remove cover film, and placement
- ABF vacuum lamination and metal hot-press (Figure 18)
- Remove PET film and post-cure (170-190° C for 30 min.)

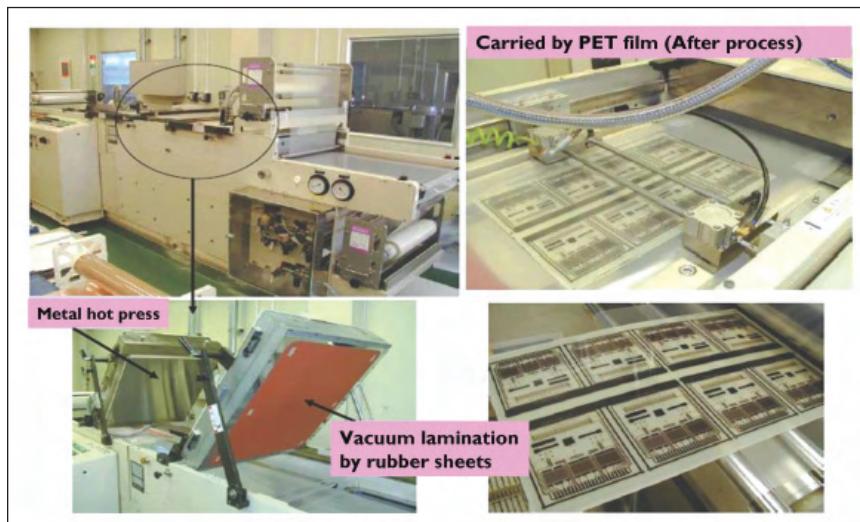


FIGURE 17: Conveyorized vacuum lamination and hot press[2]

Materials for HDI

ABF type	SH9k	GX3	GXI3	GX60	GZ9-2	GZ11	GZ20	GZ30	TB
Resin	Epoxy	Epoxy-HF	Epoxy	Epoxy + phenol	Cyanate ester + epoxy	Cyanate ester + Olefin			
Solvent residue (wt% ave)	2.8	2.8	2.8	3	2.0	2.0	1.7	1.7	3.2
Vacuum Lamination	OK	OK	OK	OK	OK	OK	OK	OK	OK
Minimum viscosity (poise ^o C)	1400/145	1400/145	1400/145	3000/136	3100/104	3100/104	3200/90	9500/90	5500/106
Cure (°C x min)		180 x 90				190 x 90			
CTE x-y (25-150°C) (tensile TMA)	95	46	46	39	36	35	28	21	52
CTE x-y (150-250°C) (tensile TMA)	180	120	120	114	105	100	75	58	14
Tg (tensile TMA)	178	156	156	163	170	173	177	190	150
Tg (DMA)	200	177	177	185	195	201	210	205	190
Young's modulus (GPa)	4.0	4.0	4.0	5.1	4.9	4.9	7.1	7.8	4.9
Tensile strength (MPa)	93	93	93	104	109	109	130	125	86
Elongation (%)	5.0	5.0	5.0	3.6	3.5	3.5	2.8	2.3	2.1
Dielectric constant @ 5.8 GHz	3.4	3.1	3.1	3.3	3.2	3.1	3.1	3.2	3.0
Loss Tangent @ 5.8 GHz	0.022	0.019	0.019	0.025	0.009	0.012	0.010	0.008	0.006
Water absorption (100°C, 1 h (wt%)	1.1	1.1	1.1	1.1	0.8	0.8	0.7	0.6	0.5
HAST L/S=20/20 mm (130°C, 85%, 3.3V)	>200h	>200h	>200h	>200h	>200h	>200h	>200h	>200h	>200h
Flame retardancy (UL94)	V0	V0	V0	V1	V1	V1	V1	V0-V1	N/A
SiO ₂ amount (wt%)	38	38	38	40	38	38	50	60	40
Status	Mass	Mass	Mass	U.D.	Mass	Samples	Samples	U.D.	U.D.

TABLE 1: Ajinomoto Buildup Film characteristics[2]

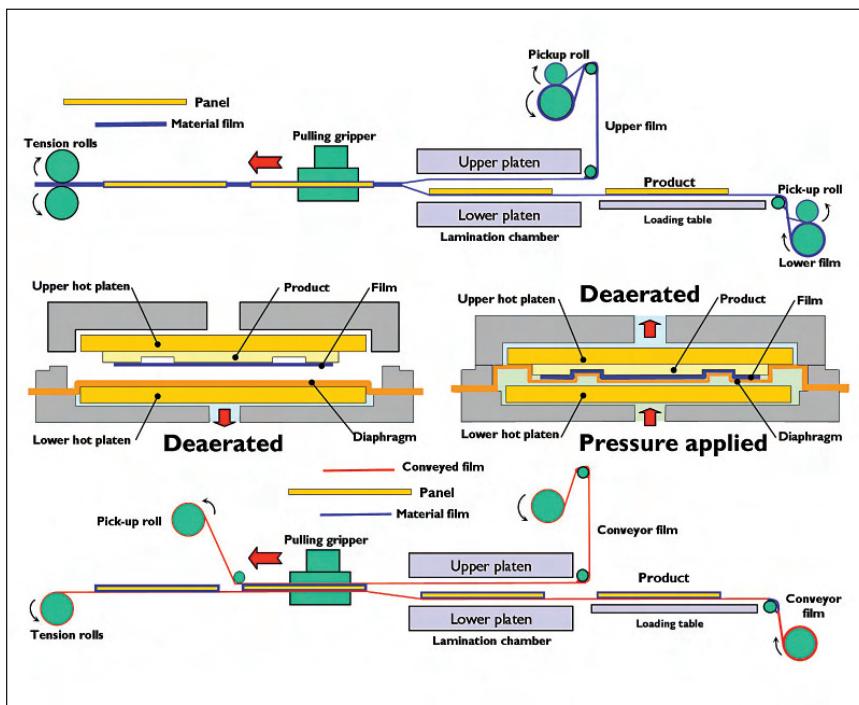


FIGURE 18: Details of the material flow through the vacuum laminator and the lamination step

ABF films, like the liquid dielectrics and dry films, have to be semi-additively metallized. The critical steps are desmear, solvent swell, film etch before metallization, etching, and annealing (post-curing). The conditions and steps will determine the resulting copper peel strengths and are covered in Chapter 8 – Desmear and Metallization.

Epoxy Liquids

Optimized liquid epoxy can provide the lowest cost of any of the dielectrics for HDI. It is also the easiest to apply in thin layers for fine-line wiring. It can be coated by screen printing, vertical or horizontal roller-coating, meniscus coating, or curtain-coating. The Taiyo Ink brand is the most used but Tamura, Tokyo Ohka Kogyo, and Asahi Denka Kogyo also have products.

Other Dielectrics

Cyanate Ester: Tg > 200° C is generally 100% cyanate ester resin with a minimal amount of epoxy (to aid in crosslinking) designed to yield polyimide-like thermal properties while enhancing electrical performance, such as dielectric constant.

Polyphenyl Ethers/Polyphenylene Oxide: M.P > 288° C are thermoplastics of Polyphenyl Ethers (PPE) or Polyphenylene Oxide (PPO) with melting points well over 288°-316° C. PPO/Epoxy blends have a Tg >180° C with higher decomposition temperatures. Their popularity is a result of their excellent electrical performance due to having lower dielectric constants and loss tangents than many of the thermosets like epoxy and BT with low water absorbtion. Their high melting points and chemical resistance make desmearing a critical process.

Bismaleimide/Triazine (BT) and BT/Epoxy: Tg >180° C and blends of various ratios of BT and standard di-functional

Materials for HDI

epoxy resins were designed to yield improvements in thermal performance, decomposition temperature, chemical resistance, and dielectric performance. BT/EPOXY can be used where higher continuous operating temperatures are required.

Polyimide: $T_g > 220^\circ C$ is a blend of polyimide resin with epoxy or 100% polyimide systems designed to yield the best reliability of high-density circuit boards. Polyimide can generally be used in rough environmental conditions, such as extreme differences in hot and cold temperatures. Polyimide systems also allow for easier rework of components

Photo Dry Film

Photosensitive dry film dielectrics were once thought to be the ultimate HDI dielectric as no external equipment was required to produce the vias. This proved not to be the case, as these were negative acting photo-systems. By negative acting, ultraviolet energy was required to cure the dielectric permanently. Any area of the film not exposed would develop away. The problem proved to be the cleanliness of the coating and exposure facility. Any dust, debris, or dry film slivers that were present on the dry film during exposure would prevent the dielectric from fully curing and would result in voids and rejects. A semiconductor Class-100 Clean Room was the condition required and proved to be too expensive for most fabricators. In Japan, certain OEMs that still have their own facilities continue to use this dielectric.

Photo Liquid

Photosensitive liquid dielectrics suffer the same fate as the dry film. Their advantage is less waste and the ability to control the applied thickness. Their disadvantage is the critical coating machinery and clean-room facility requirement.

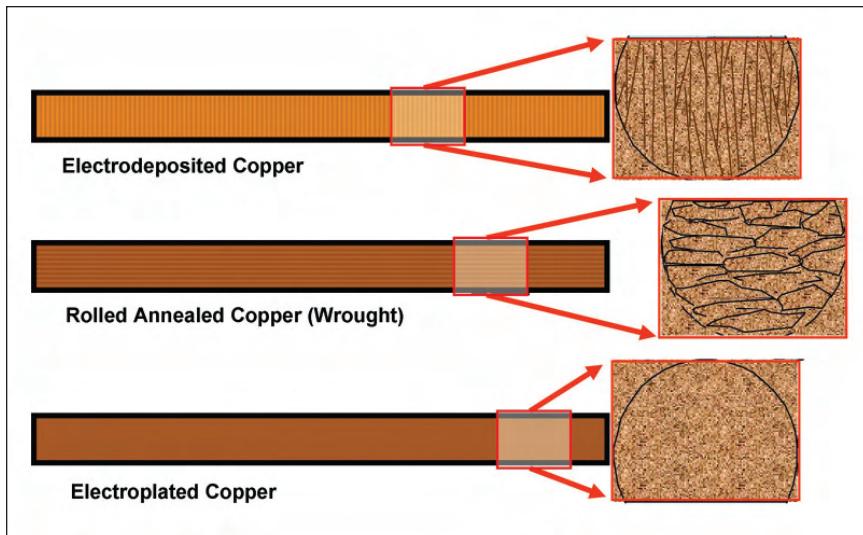


FIGURE 19: Three main types of copper foil used on printed circuits with magnification of the copper grain structure

Photoresists in semiconductor fabrication suffered the same problem until the early days of the 1980s when positive acting photoresists were perfected by Shipley. Today, all photoresists in semiconductor fabrication are positive acting. Only the areas that you want developed away need to be exposed. The bulk of the photoresists are acceptable, once dried.

Copper Foil

The copper metal on PWBs is our only method of conducting electrical currents. This is a brief review because Coombs' *Printed Circuits Handbook*, 6th Edition, Chapters 6, 7, 8, and 9, covers laminates, resins, and copper foil extensively. Metal cladding types, foil weights, and thicknesses are summarized in IPC-4101A / B.[3] IPC-CF-148, IPC-4562, and IPC-CF-152 are actual metal cladding specifications.[4]

There are three normal copper foils used in PWB production (Figure 19).

Materials for HDI

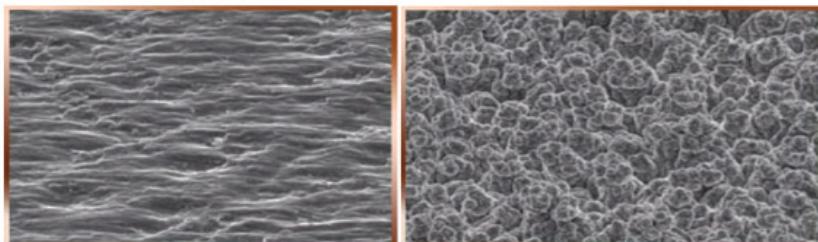
- Electrodeposited
- Wrought (rolled annealed)
- Electroplated

Figure 20 describes copper and other metal foils that can be used on PWBs. The second panel shows the eight different IPC Copper Foil Types.

Metal Foil	Resistance $\Omega/\text{cm} \times 10^6$	Temperature Coefficient of Resistance	Thermal Conductivity $\text{W}/\text{m}^\circ\text{K}$	Tensile Strength (psi)	Elongation (annealed)	Copper Foil Type	Number	Designator	Description
Copper	1.67	0.00393	393	32,000	20	Electrodeposited (E) Copper Foils	1	STD - Type E	Standard electrodeposited
							2	HD - Type E	High ductility electrodeposited
							3	HTE - Type E	High temperature elongation electrodeposited
							4	ANN - Type E	Annealed electrodeposited
Copper Electrodeposited	1.77	0.00382	393	25,000	12	Wrought (W) Copper Foils	5	AR - Type W	As rolled wrought
							6	LCR - Type W	Light cold rolled wrought
							7	ANN - Type W	Annealed wrought
							8	LTA - Type W	As rolled wrought low-temperature annealable
Aluminum	4.33	0.0039	225	16,000	30	Electroplated (E) Nickel Foils	9	--	Standard electrodeposited
							10	LTA-Type E	Low temperature annealable
							11	A-Type E	Annealable

* Dead soft ** Full hard

FIGURE 20: Metal foil properties and the IPC 11 Foil Types and descriptions[4]



SEM picture of Hoz shiny side
SEM picture of Hoz matte side

Item	Unit	Toz	Hoz	1oz	Test Method
Area Weight	g/m ²	112	153	287	IPC-TM-650
	Kg/mm ²	36	37	36	IPC-TM-650
Tensile Strength (Kg/mm ²)	23°C	4 ↑	5 ↑	10 ↑	
	180°C	26	26	25	IPC-TM-650
Elongation (%)	23°C	4 ↑	5 ↑	8 ↑	
	180°C	26	26	25	IPC-TM-650
Surface Roughness	S/S Ra	0.43 ↓	0.43 ↓	0.43 ↓	IPC-TM-650
	M/S Rz	6.5	7.5	9.6	IPC-TM-650
Peel Strength (FR-5)	Normal	5.5 ↑	6.5 ↑	↑ 8.0	A
	After Solder Float	5.5 ↑	6.5 ↑	8.0 ↑	S-4
	After Baking	5.2	6.0	7.6	E-48/180
Peel Strength Degradation Rate	After Pressure Cooker	3.0 ↓	3.0 ↓	3.0 ↓	D-2/100
	After HCL	5.0 ↓	5.0 ↓	5.0 ↓	12 * 25°C * 30min
	After NaOH	3.0 ↓	3.0 ↓	3.0 ↓	7% * 80°C * 60min

FIGURE 21: SEM pictures of the HTE-Type E electrodeposited foil (Courtesy of NanYa Plastics)

Electrodeposited

The most common foil used in manufacturing printed circuits is electrodeposited copper (ED) foil. ED foil is produced through an electrochemical process in which purified copper sulfate/sulfuric acid solution is used to electroplate copper onto a cylindrical drum typically made from titanium. The rotation speed determines the resulting foil thickness.

One of the most-used electrodeposited foils is the HTE-Type E, as seen in Figure 21. HTE-Type E has the property of high-temperature elongation required for lead-free assembly temperatures.

Wrought

Wrought type foils (Types 5-8) are milled and rolled from poured sheet copper. Consequently, the grain structure is columnar and is more ductile and capable of more flexing than electrodeposited and electroplated foils (Figure 22).

Property	Wrought Annealed Foil-TYPE 7			TYPE 3 Copper Foil HTE		
	1/2 Ounce	1 Ounce	2 Ounce	1/2 Ounce	1 Ounce	2 Ounce
Tensile strength @ 23°C:						
kpsi	15	20	25	30	40	40
MPa	103	138	172	207	276	276
Elongation % @ 23°C	5	10	20	2	3	4
Tensile strength @ 180°C						
kpsi	7	14	22	15	20	20
MPa	69	97	152	103	138	138
Elongation % @ 180°C	4	6	11	2	2	3

FIGURE 22: Properties of RA Type-7 foil compared to ED-HTE-Type 3 foil (Courtesy of Nanya Plastics)

Electroplated

Electroplated copper has a primary task of depositing copper in via holes. Because of this, the focus of its formulation is throwing power (covered in Chapter 10 – Electrodeposition and Solderable Finishes for HDI). There are three main properties of electrodeposited copper:

1. Composition - 99.8% (99.5% min, ASTM-E-53)
2. Elongation - 10–25% (6% min, ASTM-E-8 or ASTM-E-345)
3. Tensile strength - 40–50 kpsi (36 kpsi min, ASTM-E-8 or ASTM-E-345)

Profiles

Copper foils are being made thinner for finer lines and spaces. Their profiles are being reduced to improve imaging and to encourage higher frequency signals that propagate on the surface of the conductor (skin effect). Figure 23 compares the standard HTE foil with super-HTE foils and Very Low

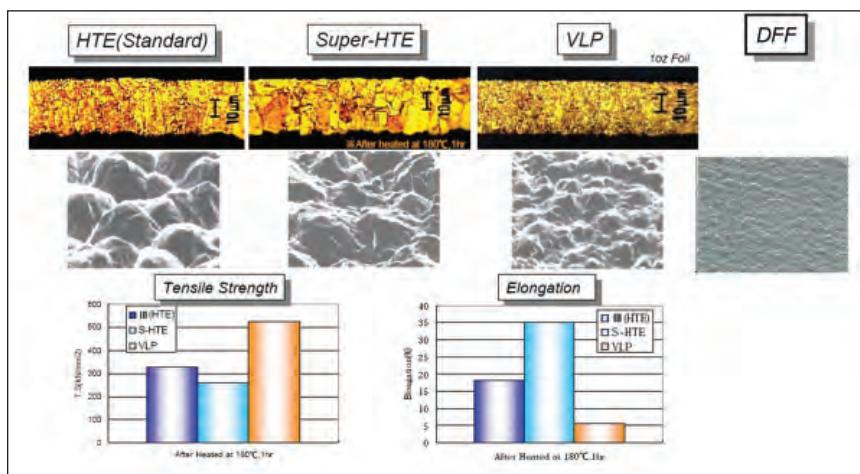


FIGURE 23: Properties and profiles of four copper foils: HTE, super-HTE, VLP, and DFF (Courtesy of Oak-Mitsui]

Profile (VLP) foil. I have included a new super-smooth foil from Mitsui, the DFF foil.

DFF foil has a special property of being extremely smooth, which is required to reduce signal losses at GHz frequencies. Figure 24 shows the micro-profile of DFF compared to conventional VLP foil.

Treatments

There are various surface treatments that can be applied to copper foil.

Bonding Treatments or Nodularization increase the surface area of the foil by plating copper or copper-oxide nodules to the surface of the foil.

Thermal Barriers, such as a coating of zinc, nickel, or brass, are usually applied over the nodules. The coating can prevent thermal or chemical degradation of the foil to resin bond during manufacture of the laminate, the printed circuit, and the circuit assembly.

Passivation and Antioxidant Coatings, in contrast to the other coatings, are almost always applied to both sides of the foil.

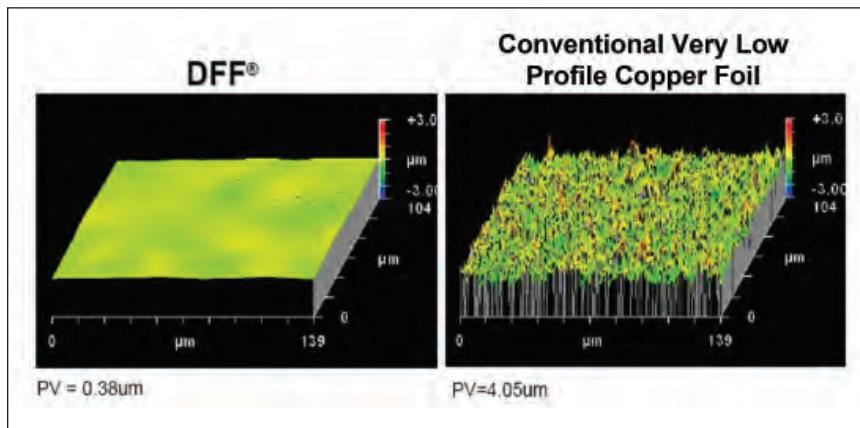


FIGURE 24: Profiles of DFF copper foil and standard VLP foil (Courtesy of Oak-Mitsui)

Coupling Agents, primarily silanes such as those used to promote fiberglass to resin adhesion, can also be used on copper foils.

Drum-side treated foil (DSTFoil) or reverse treated foil (RTF) are electrodeposited copper foils, but the treatments are plated onto the smooth drum side of the foil, rather than the matte side, as with conventional electrodeposited foil.

Adhesive Coated Foils

For the ultra-low profile and ultra-thin copper foils there are now special minuscule anchor nodules and chemical treatment layers along with special primer resins that can be applied to improve peel strength and bonding to prepregs. Some of these are shown in Figure 25.

Thin Copper on Carriers

To fabricate very fine traces and spaces, thin copper is available on removable carriers. Figure 26 shows new foils

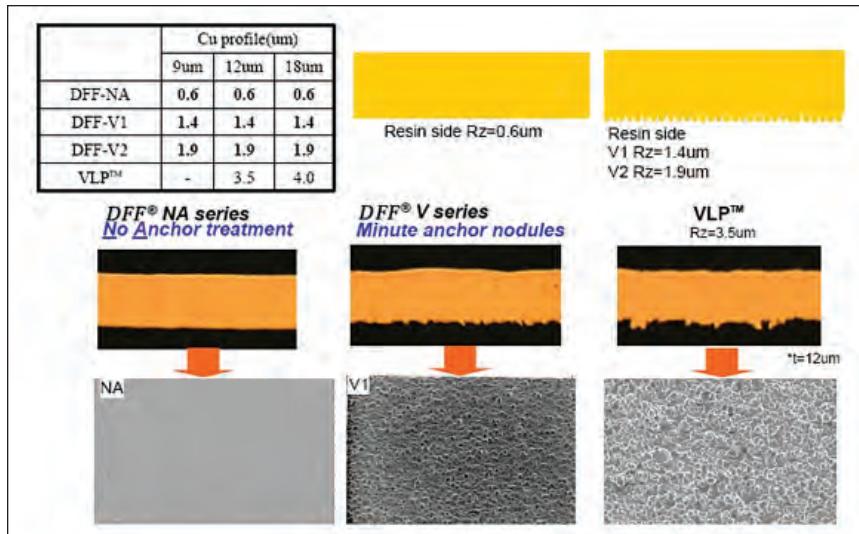


FIGURE 25: Profiles and anchor treatment for three copper foils: DFF, DFF V series and VLP foil (Courtesy of Oak-Matsui)

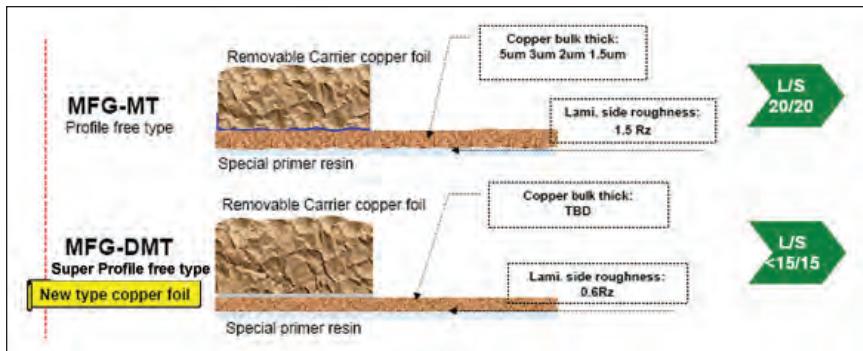


FIGURE 26: New thinner copper foils of 1.5 um, 2.0 um, and 5 um are available on removable copper carriers (Courtesy of Oak-Mitsui)

from Mitsui that are only 5 um, 2 um, and 1.5 um thick, consequently, they require a carrier copper foil. These foils are intended to offer an alternative semi-additive process (SAP) that is covered in Chapter 9 – Fine-Line Imaging and Etching and Chapter 10 – Electrodeposition and Solderable Finishes for HDI.

“Etch Down” Process for Thin Copper

Another popular method of achieving very thin copper foils is to etch down the copper foil on laminate cores. Half-ounce (H type-17 um) is normally selected because of its lower cost and low pin-hole properties. A specially controlled etcher and etchant are dedicated to this purpose using either an ammonium persulphate or hydrogen peroxide-sulphuric acid type etchant. The copper is etched down to 12 um (type T) or to 9 um (type Q). Five (5 um - type E) is usually too thin to control by this method. The possibility of etching down to the bare fiberglass is also likely.

Enabling Fine Traces and Spaces

All of these thin copper foils enable the fabrication of very fine traces and spaces. As Mitsui has shown in Figure 27, pattern-plating onto their DFF-V2 ultra-thin copper foil

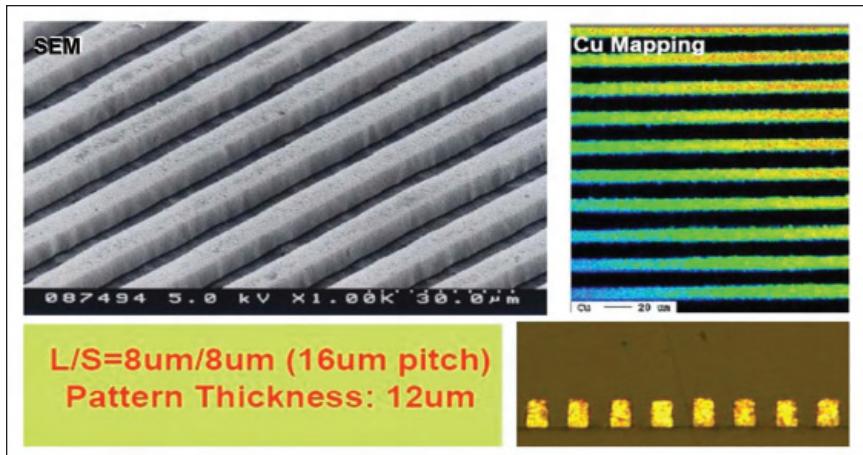


FIGURE 27: Very fine traces and spaces are possible with the ultra-thin and ultra-low profile DFF copper foils (Courtesy of Oak-Mitsui)

(on a carrier) and plating 10 um of copper enables the flash etching of 8 um traces and spaces. A larger discussion of these processes is covered in Chapter 9 – Fine-Line Imaging and Etching and Chapter 10 – Electrodeposition and Solderable Finishes for HDI.

Electrical Performance

When operating frequencies increase, more of the electrical signal travels in the outside surface of the conductor. This is the *skin effect depth* and this is where much of the signal travels. Figure 28 shows the transmission loss in dB/m as a function of frequency. As seen in this graph, above 5 GHz, the skin effect has a difference of nearly 3 dB/m due to the difference of the average roughness of half-ounce copper foil compared to the low-profile VLP Cu foil. At these higher frequencies, signal attenuation due to conductor losses (related to the roughness of the foil) becomes an important factor.

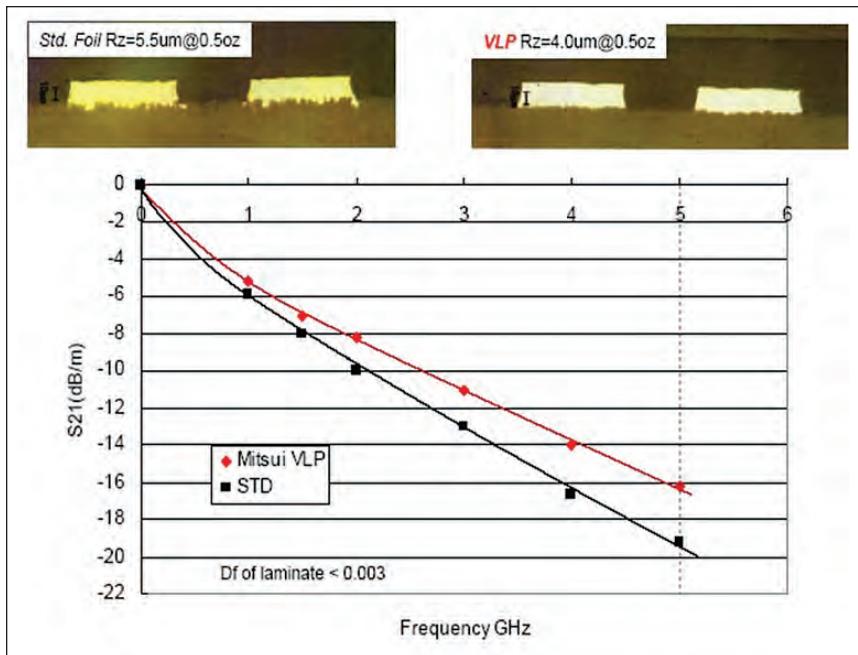


FIGURE 28: Dendritic Cu foil surface will increase AC resistance at frequencies above 1 GHz. The low profile copper foils have fewer losses than conventional copper foil with its rougher dendritic treatments. (Courtesy of Oak-Mitsui)

Dielectric Properties

Important considerations for HDI dielectrics are thermal, mechanical, electrical, and reliability properties.

IPC standard IPC-4104A was specifically created for HDI materials, including dielectrics, metal conductors, and conductors on dielectrics. IPC-4101B is the standard that covers copper clad laminates and prepgres.

Thermal

Thermal properties are important and include the following:

- maximum operating temperatures and decomposition temperatures (T_g and T_d);

- reflow endurance including rework (T260, T288 and T300 as seen in Figure 29);
- solder float time or immersions for 10 sec at 288°C.

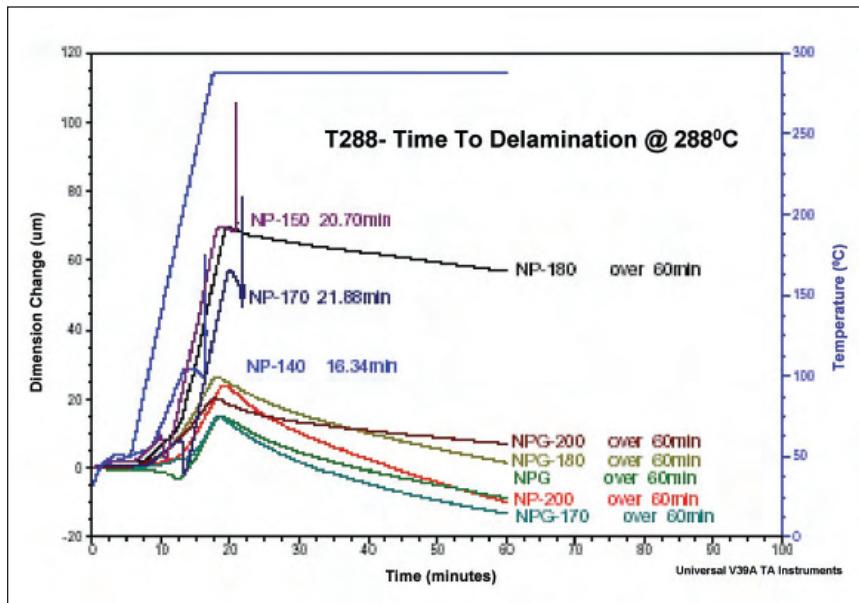


FIGURE 29: T288 Time-to-Delamination of thermal properties of various FR-4 laminates, from 16 minutes for low T_g and T_d laminates to over 60 minutes for the newer improved FR-4 laminates (Courtesy of NanYa Plastics)

Mechanical

The mechanical properties that are important are tensile strength and dimensional stability (CTE) in X-Y and Z-axis.

Electrical

Important electrical properties are dielectric constants (D_k) and dissipation factor (loss tangent- D_f). Figures 30 and 31 show D_k and D_f as a function of frequency and temperature for a typical FR-4 core. These properties vary with relative humidity.

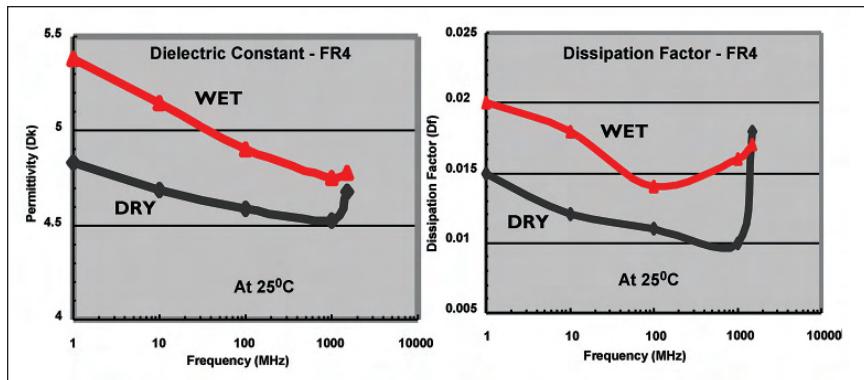


FIGURE 30: Typical dielectric constant (D_k) and dissipation factor (D_f) of FR-4 as a function of frequency and whether wet or dry, measured at 25°C

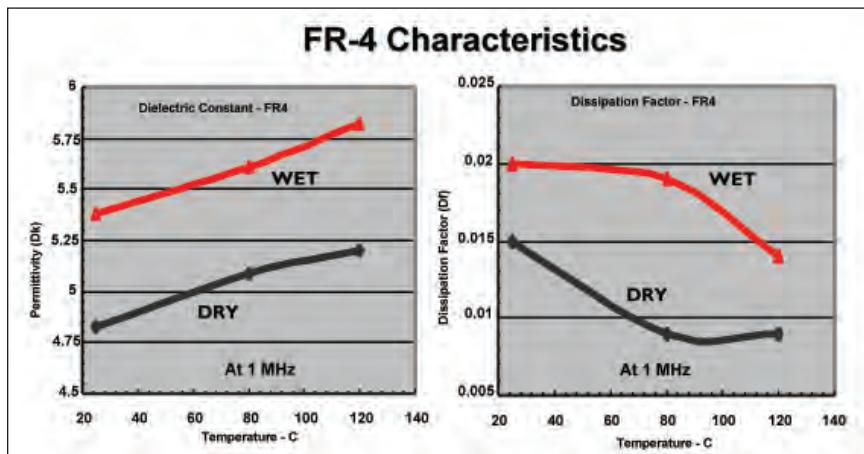


FIGURE 31: Typical dielectric constant (D_k) and dissipation factor (D_f) of FR-4 as a function of temperature and whether wet or dry, measured at 1 MHz

Reliability

Reliability is measured by conductive anodic filament resistance (CAF) in hours.

Distributed Capacitance Materials

In Chapter 4 – Electrical Performance, we introduced important concepts in a power distribution network (PDN)

to enhance high-frequency performance of fast rise-time electronics. One of those concepts was to reduce the distance between the power and ground plane to keep the impedance of the PDN to a minimum. Another was to minimize the loop inductance of each element that makes up the PDN. The typical components of a circuit board's PDN include a switching power supply, bulk decoupling capacitors, high frequency decoupling capacitors, and inner-layer power and ground planes.

The use of ultra-thin, high dielectric constant (D_k) dielectrics can greatly increase the effectiveness of efforts to enhance PDN. Standard FR-4 technology is limited to 2-mil thickness, a D_k value of approximately 4 and a capacitance density of only 49 to 68 pF/cm² (0.31 – 0.43 nF/in²). Thinner (<25 μ m) dielectric materials, especially those filled with high dielectric ceramic particles such as barium titanate, are now being used for the power distribution issues of today's high frequency designs. The use of thin dielectric cores for decoupling may require the use of PCB shops and materials that are licensed by Sanmina-SCI Inc.

Some of the novel, recently developed, ultra-thin embedded capacitor laminates have dielectric thicknesses in the range of 8 to 14 microns (0.31 to 0.55 mils) and a D_k of up to 40. In combination, these features deliver a high capacitance density of 0.3 to 3.6 nF/cm² (2 to 23 nF/in²). A partial list of distributed capacitance materials can be seen in Figure 32. Each offers many benefits when used for decoupling high speed digital electronics, including:

- lowering impedance of power distribution network;
- dampening board resonances;
- reducing noise on power planes;
- reducing radiated emissions;

- possibly replacing large numbers of discrete decoupling capacitors;
- possibly replacing discrete SMT filter capacitors.

Lowering Impedance of the Power Distribution Network

The following is an example of the improvement in impedance by using embedded capacitor layers. The product has a 14-layer board with a CPU running at 1.3 GHz. At lower frequencies the decoupling capacitors on the surface do an effective job of keeping the transfer impedance low, but at higher frequencies the thin planes do a much better job due to the lower inductance (Figure 33).

DISTRIBUTED CAPACITANCE MATERIALS									
TYPE (CCL / PP / RCF)	THICKNESS (mil)	THICKNESS (mm)	CAPACITANCE (nF/in ²)	CAPACITANCE (pF/cm ²)	Dk @ 1 MHz	DJ @ 1 MHz	DESCRIPTION	P/N	PWB Processing
CCL	0.39	0.010	22.831	3638.0	40	0.005	Cond-Film	--	Sequential Lam
CCL	0.63	0.016	10.701	1705.9	30	0.019	FaradFlex	BC16T	Sequential Lam
CCL	0.35	0.009	10.273	1656.9	16	0.005	C-Ply	C-Ply	Sequential Lam
CCL	1.18	0.030	7.610	1212.7	40	0.005	Cond-Film	--	Sequential Lam
CCL	0.47	0.012	4.590	696.3	9.6	0.019	FaradFlex	BC12TM	Both side Etching
CCL	0.31	0.008	3.045	485.1	4.2	0.016	FaradFlex	BC8	Both side Etching
CCL	0.47	0.012	1.980	312.4	4.1	0.015	FaradFlex	BC12	Both side Etching
CCL	1.97	0.060	1.827	291.0	16	0.005	High-Dk	--	Sequential Lam
CCL	0.63	0.016	1.462	233.0	4.1	0.015	FaradFlex	BC16	Both side Etching
CCL	0.50	0.013	1.398	222.0	3.1	0.009	TCC	TCC	Both side Etching
CCL	0.71	0.018	1.108	178.5	3.5	0.01	InternalHK	HK4	Both side Etching
CCL	0.94	0.024	0.980	156.2	4.1	0.015	FaradFlex	BC24	Both side Etching
CCL	0.98	0.025	0.913	145.5	4	0.02	ZBC	BC-1000	Both side Etching
ECL	1.00	0.025	0.787	125.3	3.5	0.01	InternalHK	HK4	Both side Etching
CCL	2.00	0.051	0.494	75.8	4.4	0.02	ZBC	BC-2000	Both side Etching
CCL	3.00	0.076	0.307	48.9	4.1	0.02	Standard	0.003*	Both side Etching
Film	1.97	0.060	3.853	582.1	32	0.007	NipFlex	--	Sequential Lam
Prepreg	1.10	0.028	0.877	139.7	4.3	0.02	106 LD	106 LD	Sequential Lam
Prepreg	1.30	0.033	0.744	118.5	4.3	0.02	1087 LD	1087 LD	Sequential Lam
Prepreg	1.18	0.030	0.742	118.2	3.9	0.02	1037LD	1037LD	Sequential Lam
Prepreg	1.30	0.033	0.675	107.5	3.9	0.02	1067LD	1067LD	Sequential Lam
Prepreg	1.70	0.043	0.568	90.6	4.3	0.02	1086LD	1086LD	Sequential Lam
Prepreg	1.73	0.044	0.658	88.9	4.3	0.02	1078 LD	1078 LD	Sequential Lam
Prepreg	1.77	0.045	0.533	84.9	4.2	0.02	1080LD	1080LD	Sequential Lam
Prepreg	2.00	0.051	0.427	80.0	3.8	0.02	108	108	Sequential Lam
Prepreg	2.50	0.064	0.351	55.3	3.9	0.02	1080	1080	Sequential Lam
RCF	0.79	0.020	12.843	2046.4	45	0.021	RCC	MCF-HD-45	Sequential Lam
RCF	0.63	0.016	10.702	1705.3	30	0.019	RCC	BC16T-RCC	Sequential Lam
RCF	1.97	0.050	5.137	818.6	45	0.021	RCC	MCF-HD-45	Sequential Lam
RCF	1.0	0.025	0.889	143.2	4	0.019	RCC+RF	MHC100G	Sequential Lam
RCF	1.6	0.041	0.534	85.0	3.8	0.015	RCC	MR500(LM)	Sequential Lam

FIGURE 32: Partial list of available dielectrics from around the world that can be used for the power/ground PDNs in modern high-speed multilayers, including HDI multilayers

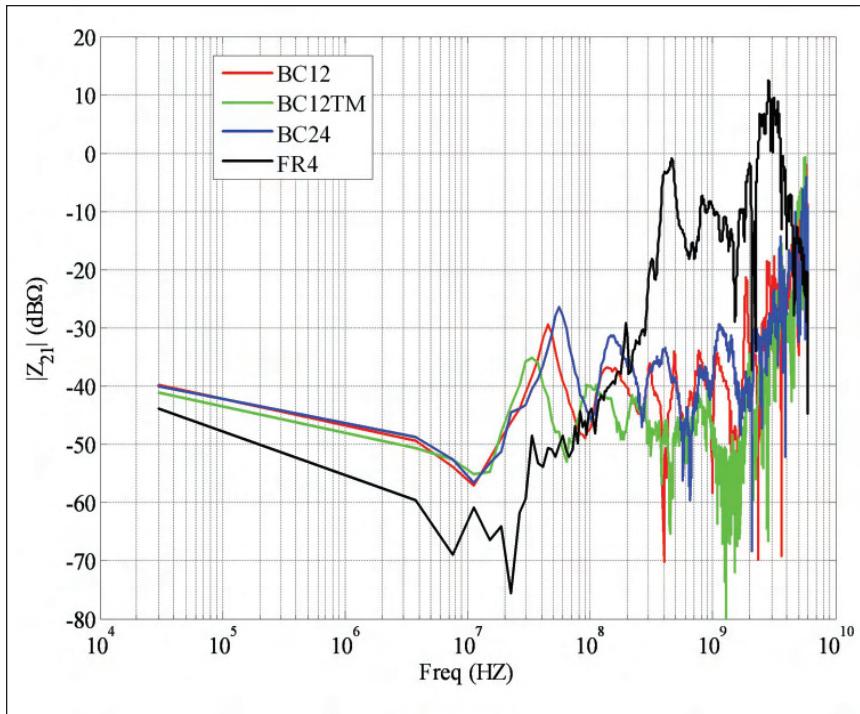


FIGURE 33: PDN impedance of four different CPU boards running at 1.3 GHz, using normal FR-4 between PWR/GND and BC24, BC12TM and BC12 materials[5]

Figures 34 (a) and (b) illustrate that at lower frequencies, capacitance density is higher, and impedance is lower. As the frequencies increase and go through the resonance point, the thinner the dielectric, the lower the impedance, due to the lower inductance. With two planes of the same thickness, the higher D_k will result in slightly lower impedance.

Dampening Board Resonances

In addition to reducing the overall impedance of the PDN, the use of thin dielectrics reduces the resonances that can propagate between the planes. The higher D_k materials result in lower resonances, but also shift the peaks to lower frequencies. This needs to be considered, as you do not want

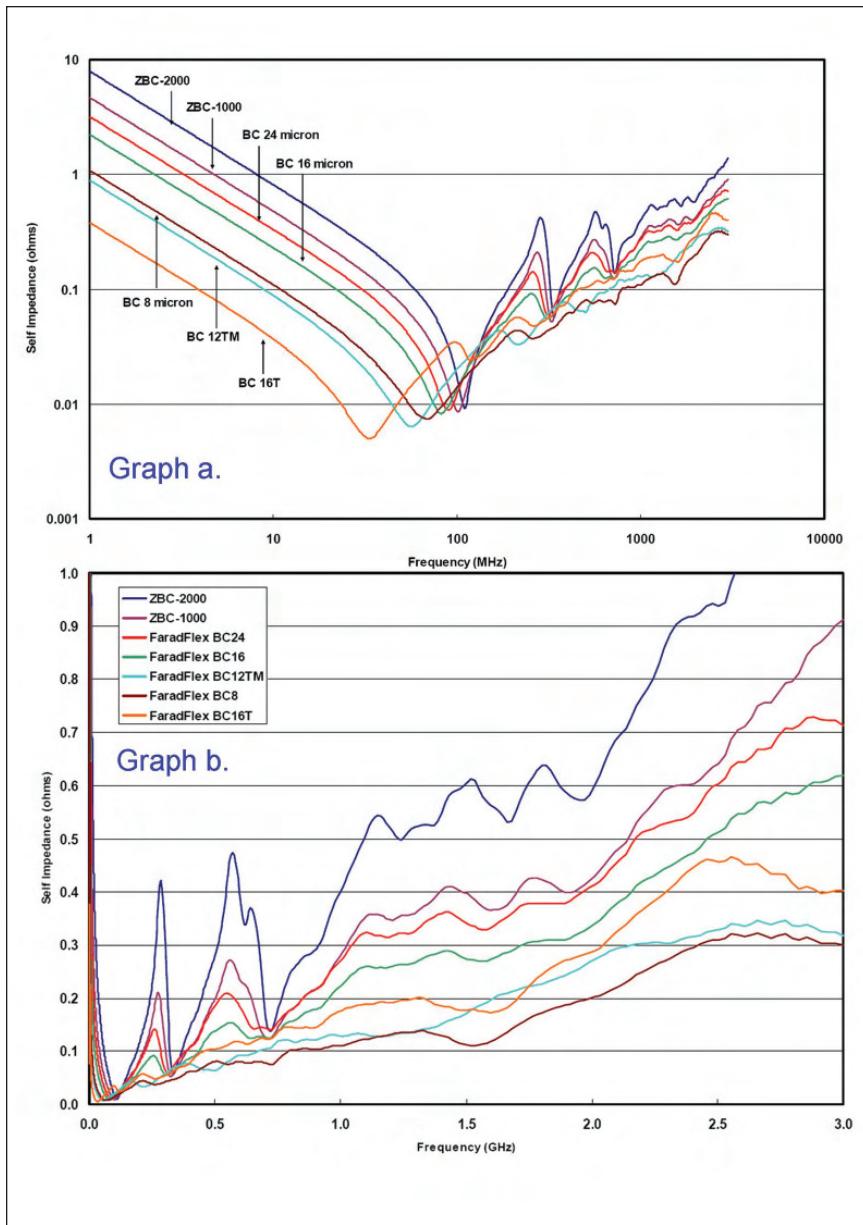


FIGURE 34: Graphs (a) and (b) illustrate the effect at various frequencies of both thin dielectrics between PWR/GND and of the higher dielectric constant of that dielectric. With two planes of the same thickness, the higher D_k will result in slightly lower impedance.[6]

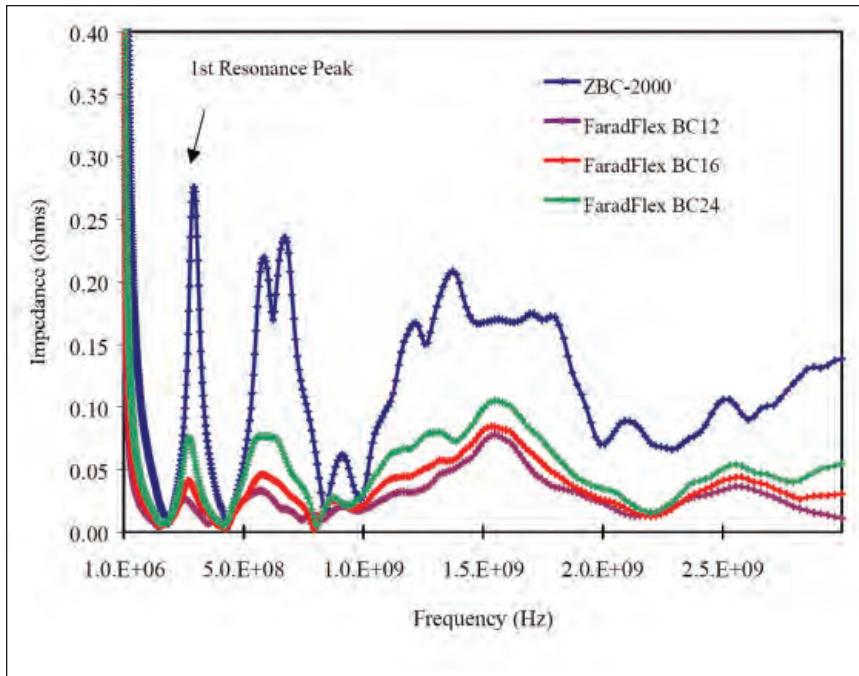


FIGURE 35: Effect of four materials of distributed capacitance between PWR/GND on the power distribution networks plane resonances[6]

to have a peak at a critical operating frequency, as seen in Figure 35.

Reducing Noise on Power Planes

The previous examples show what happens in the frequency domain, but we also need to look at the time domain. The following examples show that the thinner dielectrics can result in significantly lower noise. Figure 36 shows the same 14-layer board as before, measured in the time domain (a) and frequency domain (b) while Figure 37 and Figure 38 show a different three BC materials helping to reduce noise on the power system and eye diagrams showing the effect on jitter.

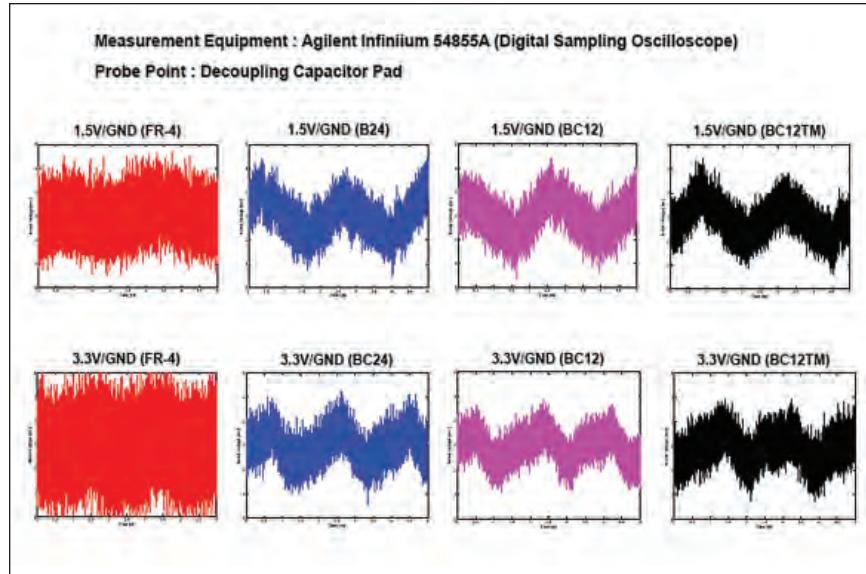


FIGURE 36 (a): Noise on the PDN 1.5V and 3.3V plane of four different CPU boards running at 1.3 GHz, using normal FR-4 between PWR/GND and BC24, BC12TM and BC12 materials

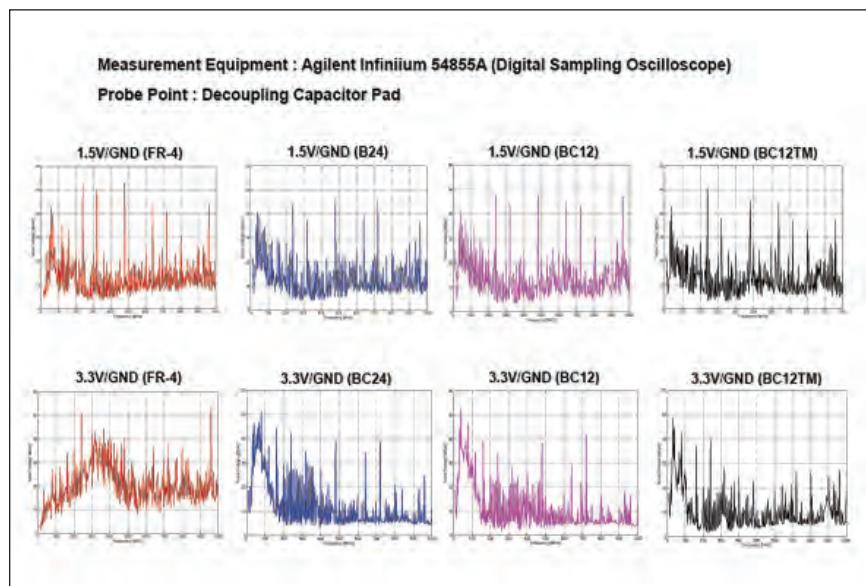


FIGURE 36 (b): Frequency-domain illustrations of the same waveforms[5]

Materials for HDI

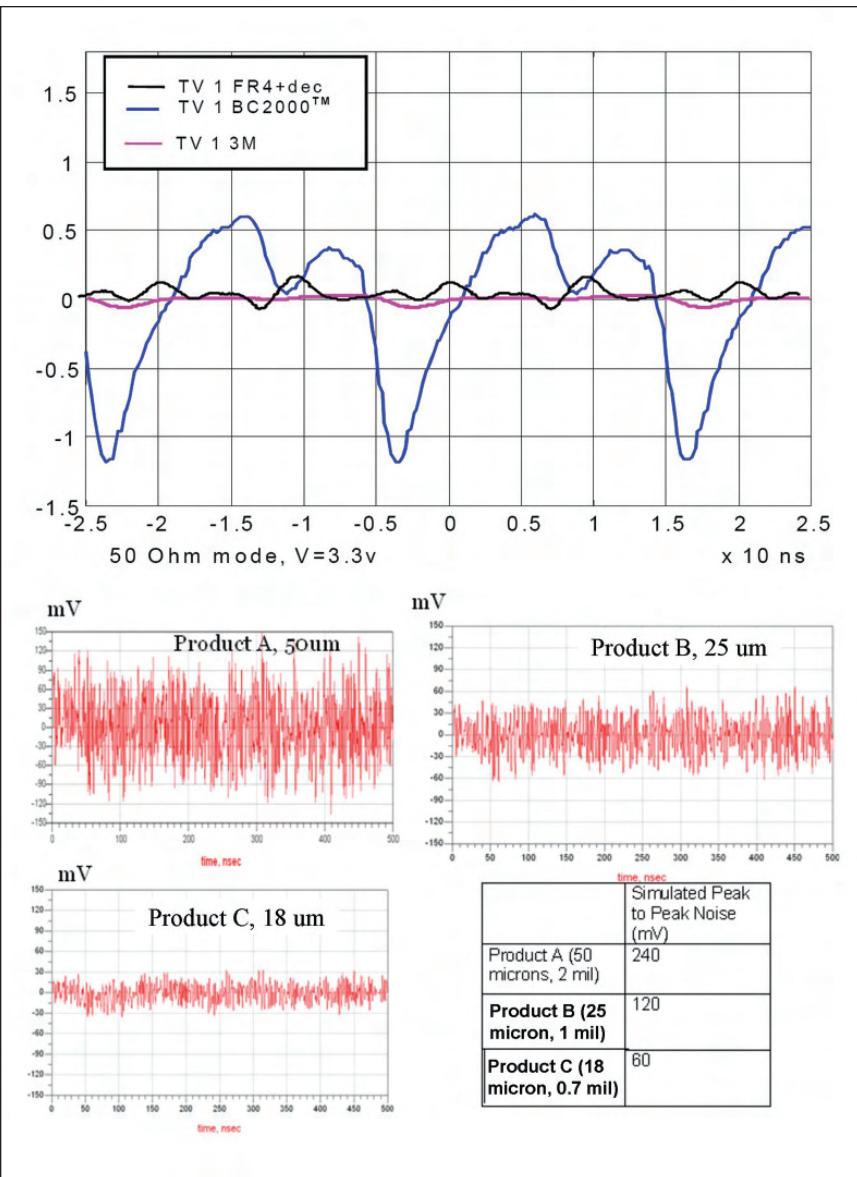


FIGURE 37: TOP: The effect of three distributed capacitance materials between PWR/GND on the noise of the power distribution 3.3V plane[7]; BOTTOM: Three materials, 50-um FR-4, 25-um HK-04 BC, and 18-um HK-04 measuring the peak-to-peak noise (mV)[8]

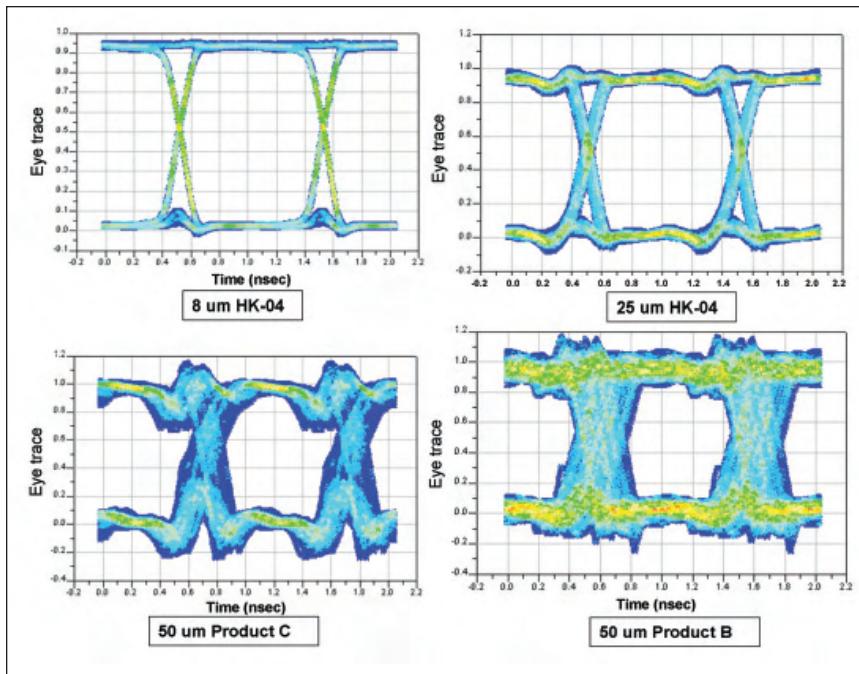


FIGURE 38: Eye diagrams of the three materials in Figure 37 plus a second 50-um FR-4 (product B)[8]

Reducing Radiated Emissions

When resonances are present in a PDN, the energy usually escapes out of the end of the boards, or some components can even act as antennas and cause electro-magnetic interference (EMI). As frequencies go up, this radiation becomes a bigger issue. It has been demonstrated that less noise in the PDN results in less EMI. Taking the 14-layer PCB as an example again, we measured the radiation coming off the board from 1 to 7 GHz (Figure 39). The FCC requires testing to 5 times clock frequency. Thinner dielectrics result in lower EMI. The higher D_k material (in this case D_k of 10 compared to 4.4 for the other material) had the lowest EMI on average, but did shift the EMI distribution. This improvement in EMI was shown by Sun Microsystems in one of their server designs as shown in Figure 40.

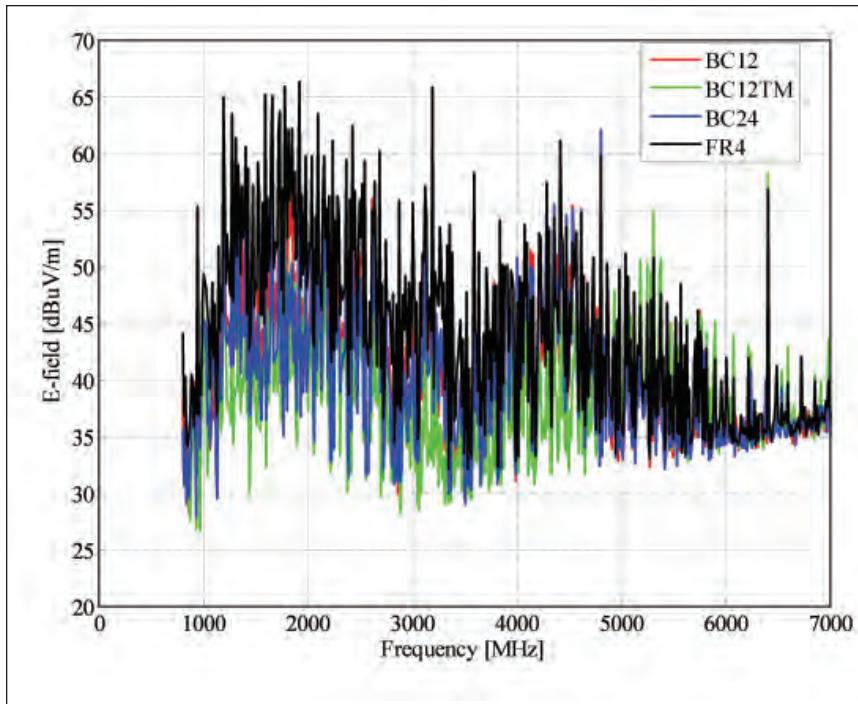


FIGURE 39: Effect of three materials of distributed capacitance between PWR/GND on the noise of the power distribution 3.3V plane[5]

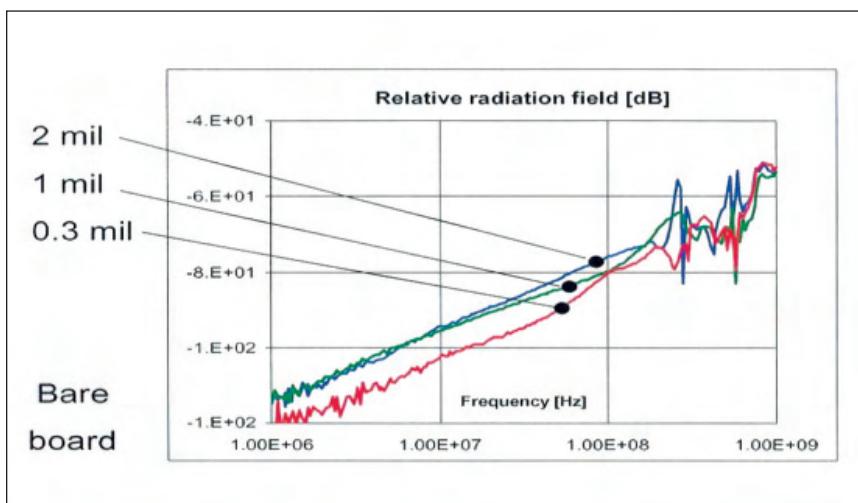


FIGURE 40: Effect of three materials of distributed capacitance between PWR/GND on the close-field EMI radiation from the power distribution 3.3V plane[7]

Design	Discrete Capacitance Removed (nF)	Embedded Capacitance (nF)	Ratio of Removed to Embedded	% of Total Discrete Caps Removed
EDC TV1	330 <small>$33 \times 0.01 \mu F$</small>	105	3.1	100%
OEM A	12,600 <small>$126 \times 0.1 \mu F$</small>	300	42.0	>75%
OEM B	6,310 <small>$62 \times 0.1 \mu F$ $11 \times 0.01 \mu F$</small>	210	30.0	>60%
OEM C	3,180 <small>$29 \times 0.1 \mu F$ $28 \times 0.01 \mu F$</small>	305	10.4	>75%
OEM D	52,900 <small>$529 \times 0.1 \mu F$</small>	1970	26.9	>75%
OEM E TV	9,900 <small>$99 \times 0.1 \mu F$</small>	660	15.0	100%
OEM F	~35,000 <small>443 total (mostly 0.1 μF)</small>	~1000	~35	100%

FIGURE 41: Seven different OEMs' results of using distributed capacitance materials between PWR/GND to replace SMT decoupling capacitors[7]

Replacing Discrete Decoupling Capacitors

With the improvement in the PDN by the use of thin dielectrics, it is now possible, in fact desirable, to remove the discrete capacitors on the surface. Using the 14-layer PCB as an example, 781 decoupling capacitors of 0.1 μF value were removed with performance remaining as good or better.

The table in Figure 41 shows similar studies where typically 75 to 100 percent of the decoupling capacitors were removed. The important thing to remember is that this is due to the lower inductance of the thin planes and not due to the total capacitance of the planes.

Replacing Discrete SMT Filter Capacitors

The above examples were based on removing decoupling capacitors due to the lower inductance of thin power/ground (PWR/GND) planes. In order to realize maximum passive integration, we need to be able to embed capacitors of a specific value to perform other functions. Higher D_k materials

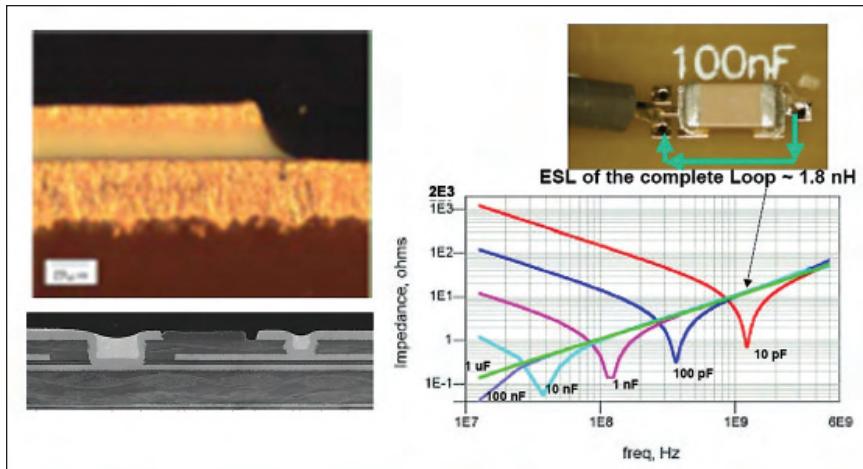


FIGURE 42: A cross section of HDI planar capacitors used to replace SMT discrete capacitors by OEMs[6]

are now available that allow embedding of small (typically 1 to 20,000 pF) capacitors. These capacitors can make use of any open room and be of any shape. Design tools from companies like Mentor Graphics and Zuken allow placement of these capacitors into the design. Design and materials are covered in more detail in Chapter 14 – Embedded Components. Individual parametric capacitors are seen in Figure 42. HDI is an enabling technology that maximizes the area available for embedded capacitors, minimizes the inductance of the vias, and improves the performance of capacitors.

Embedded capacitors and HDI are complementary technologies. The use of thin dielectrics maximizes some of the benefits of HDI, such as thinner PCBs and packages. The resulting smaller form factor also takes advantage of blind microvias. HDI interconnect technology improves the electric performance of the embedded capacitors by minimizing inductance and maximizing area available for discrete embedded capacitors.

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6

The HDI Manufacturing Processes

By Happy Holden — *Mentor Graphics*

Original HDI Fabrication

High-Density Interconnect printed circuits actually started in 1980, when researchers started investigating ways to reduce the size of vias. The first innovator is not known, but some of the earliest pioneers include Larry Burgess of MicroPak Laboratories (developer of LaserVia), Dr. Charles Bauer at Tektronix (who produced photodielectric vias),[1] and Dr. Walter Schmidt at Contraves (who developed plasma-etched vias). Laser drilled vias were used in mainframe computer multilayers in the late 1970s. These were not as small as the laser drilled vias today and were produced only in FR-4 with great difficulty and at great cost.

The first production build-up or sequential printed boards appeared in 1984, starting with the Hewlett-Packard laser drilled FINSTRATE computer boards, followed in 1991 in Japan with Surface Laminar Circuits (SLC) [2] by IBM-YASU and in Switzerland with DYCOstrate [3] by Dyconex. Figure 1 shows one of those first Hewlett-Packard FINSTRATE boards.

HP Finstrate Laser Via

H-P did not intend to develop laser drilled microvias. They were the result of reverse-engineering their new 32-bit microcomputer chip. They called it the “FOCUS” chip, a

The HDI Manufacturing Processes

32-bit microprocessor developed in NMOS-III, which has the characteristic of being very current-hungry. One of the early surprises with this new microprocessor was that it could not drive the inductance of a standard 0.3 mm diameter through-hole via in a 1.6 mm thick board. It could only drive 20-30 nHenrys of inductance. The second surprise was that it did not have the energy to drive the normal losses of FR-4 ($D_j=0.020$). The requirement was for a metal-core board with very tiny blind-vias and a very low-loss dielectric. The resulting board created was a copper-core, build-up technology that had direct wire-bonded integrated circuits (ICs). In the copper core, holes were mechanically drilled through and insulated with polytetrafluoroethylene (PTFE), then laminated layers of PTFE

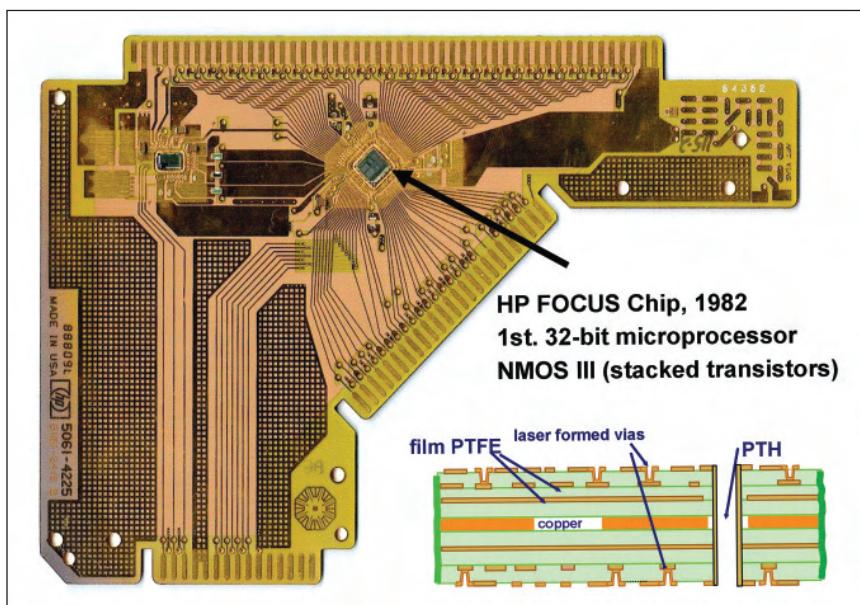


FIGURE 1: The first microvia PCB in general production, Hewlett-Packard's FINSTRATE, was put into production in 1984. It was a copper-core, build-up technology that had direct wire-bonded integrated circuits (ICs). After laminating layers of plasma-metallized polytetrafluoroethylene (PTFE) to the copper core, vias were mechanically drilled through the copper core and insulated with PTFE. Additional through-holes were then drilled along with 5-mil blind vias.

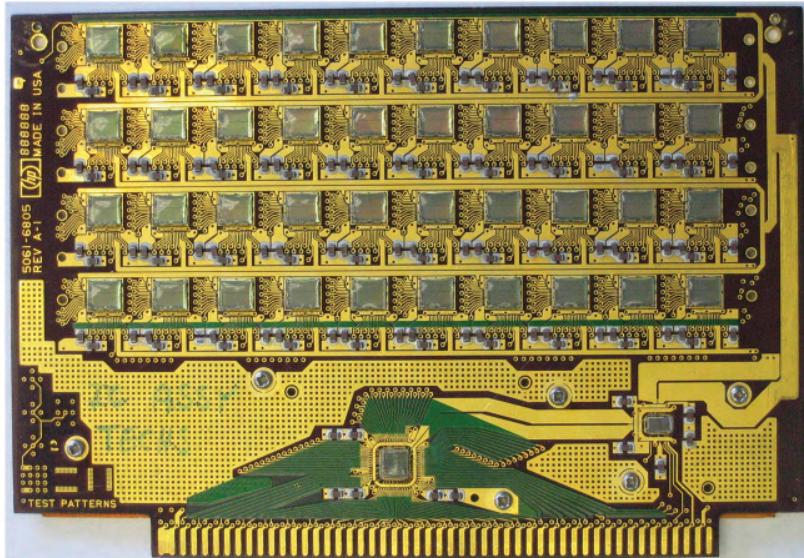


FIGURE 2: The Hewlett-Packard FINSTRATE memory board. This 32-bit computer was only the size of a child's lunch-pail.

were applied and a home-made laser drill produced 0.125 mm diameter blind-vias. All were plasma-metallized. Additional through-holes were then drilled along with 0.15 mm blind vias. Figure 2 shows the memory board and like Figure 1, which is the microprocessor and clock circuit, were made of this "Finstrate" architecture.

IBM SLC Photo-via

Since the introduction of SLC technology in 1991 (see one of the first IBM SLC boards in Figure 3), many variations of methods for mass-producing HDI wiring boards have been developed and implemented. Figure 4 shows some of the design rules of that early SLC Technology. However, if one technology is to be picked as a winner, judged in terms of volume produced, laser drilling technology is the one. Other

The HDI Manufacturing Processes

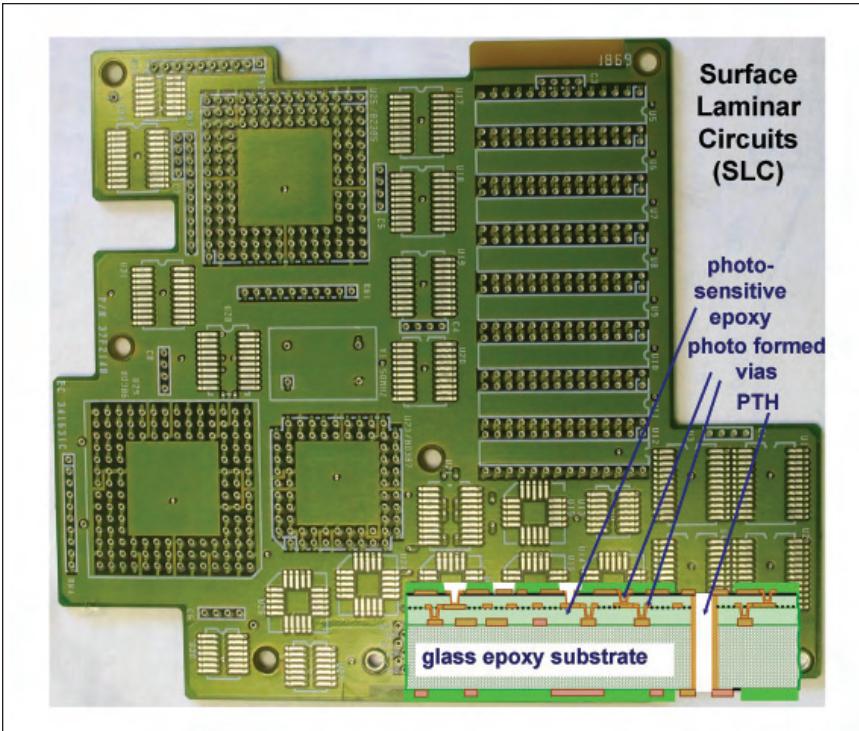


FIGURE 3: The first photodielectric microvia board was produced in volume in Japan by IBM-Yasu. This is the SLC technology with two buildup layers on one side of the four conventional FR-4 layers. Cross sectional view of microvia hole board made by SLC process (IBM-Yasu)[2]

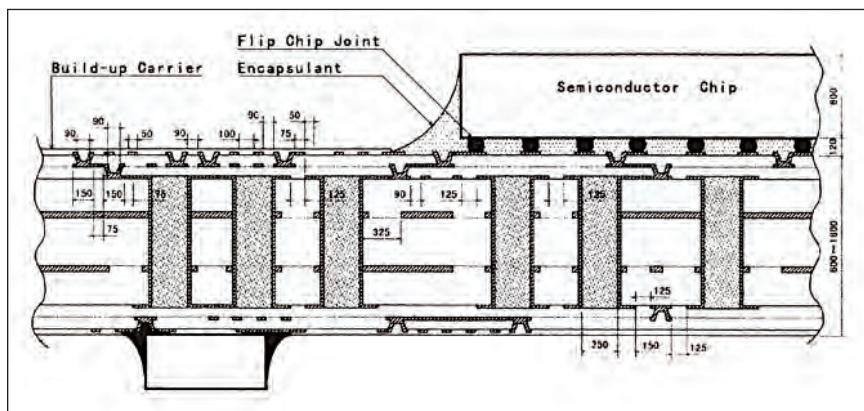


FIGURE 4: SLC technology has had a long life. This is SLC III, as used by IBM Endicott, NY and Austin, TX. Currently, the technology is owned by Kyocera of Japan.[2]

methods are still used by a number of PWB manufacturers, but on a much smaller scale.

However, a greater emphasis will be placed on the laser drilling process (laser via hereafter) since it is the most popular process today and it seems that its popularity will grow in the future. It must be understood that via hole formation is just one element of fabricating HDI wiring boards. Fabrication of HDI wiring boards with microvia holes involves many processes not common to conventional board fabrication. Therefore, additional emphasis will be placed upon the fabrication processes that are common to other microvia technologies in forthcoming Chapters 7, 8, 9, 10, 11 and 12.

HDI Fabrication Basics

Figure 5 shows the breakdown of Sequential Buildup Technologies (SBU) or High-Density Interconnects. The three basic elements are dielectric format, via formation, and metallization methods.

Materials and dielectrics are covered in detail in Chapter 5, while Chapter 7 covers via formation, and Chapter 8 covers metallization.

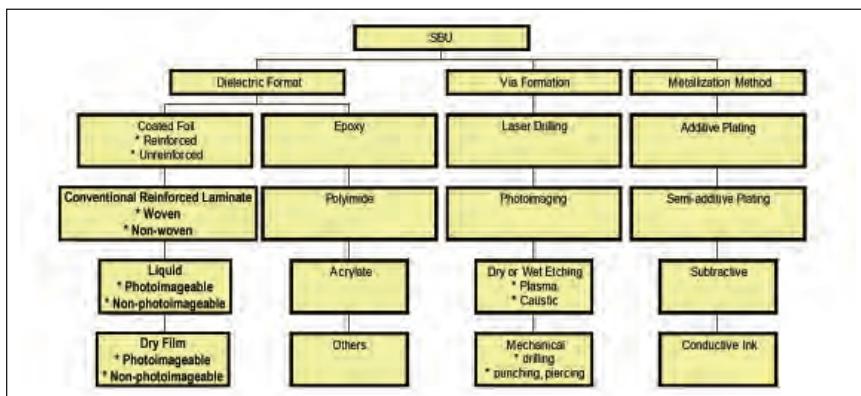


FIGURE 5: Sequential buildup technology (HDI) has three major characteristics: dielectric format, via formation, and metallization methods (Courtesy of DuPont.)

Dielectrics and Insulators

This section provides an overview of the dielectric and applied conductive materials used in microvia fabrication. Some of these materials can be used in both IC chip carrier and PWB HDI applications. The discussions are focused on the HDI PWB arena and on materials for which information is readily available. In Chapter 5, cross references are made to the relevant material specifications of the IPC/JPCA-4104 specification for HDI and microvia materials. A brief material roadmap discussion is included to illustrate material property trends.

Figure 5 shows a material and technology selection flowchart for use when choosing dielectric materials. In using the flowchart, you should ask the following questions regarding the dielectric you are considering:

- Will the dielectric use chemistry compatible with current chemistry used by core substrate material?
- Will the dielectric have acceptable plated copper adhesion? (Many original equipment manufacturers [OEMs] want >6 lb/in [1.08 kgm/cm] per 1 oz [35.6 µm] copper.)
- Will the dielectric provide adequate and reliable dielectric spacing between metal layers?
- Will it meet thermal needs?
- Will the dielectric provide a desirable “high” Tg for wire bonding and rework?
- Will it survive thermal shock with multiple SBU layers (i.e., solder floats, accelerated thermal cycles, multiple reflows)?
- Will it have platable, reliable microvias that will have latitude to ensure good plating to the bottom of the via?

There are nine different general dielectric materials used in HDI processes. IPC slash sheets like IPC-4101B and IPC-4104 cover many of these, but many are not yet specified by IPC standards. The materials are:

1. Photosensitive Liquid Dielectrics
2. Photosensitive Dry Film Dielectrics
3. Polyimide Flexible Film
4. Thermally Cured Dry Films
5. Thermally Cured Liquid Dielectric
6. Resin Coated Copper Foil (RCC), dual-layer and reinforced
7. Conventional FR-4 Cores and Prepregs
8. New 'spread-glass' laser drillable (LD) Prepregs
9. Thermoplastics

Many of these resins and reinforcements are shown in Figure 6, arranged by their dielectric constant and dissipation

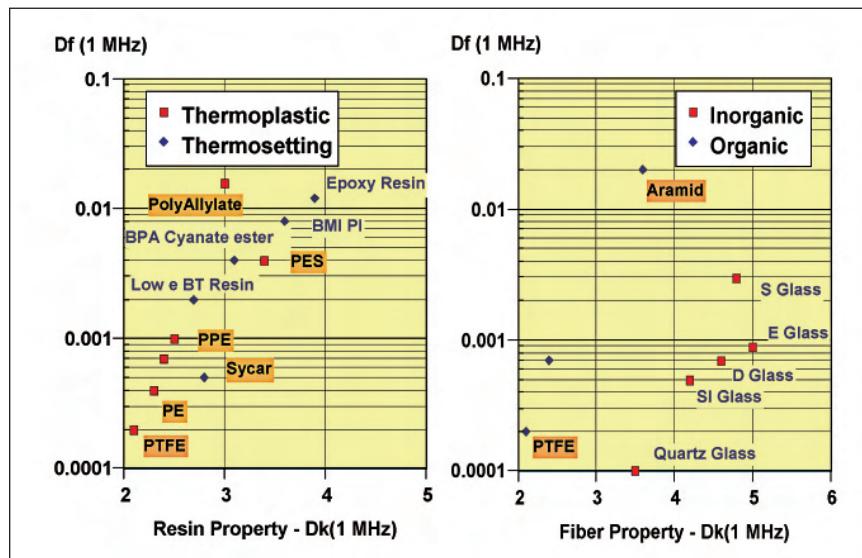


FIGURE 6: Dielectric options of resins and reinforcements by dissipation factor (D_f) versus dielectric constant (D_k) (Courtesy of Holden Consulting)

The HDI Manufacturing Processes

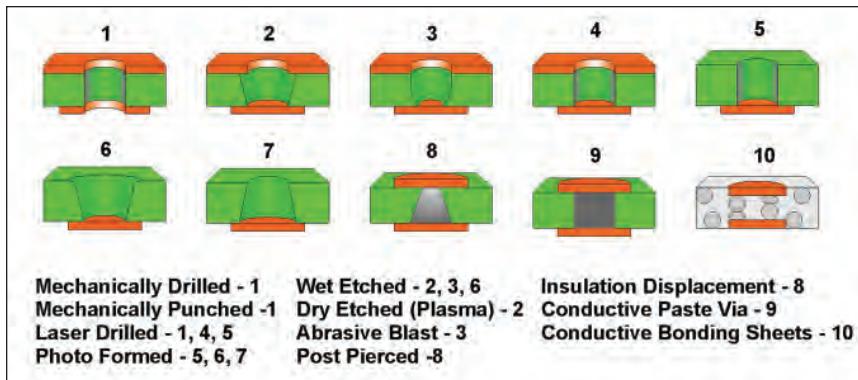


FIGURE 7: Ten methods of vertical via connections (From IPC-2315 and IPC-2226)

factor. When considering a dielectric, you also need to consider the method of via formation. Figure 7 shows more details of ten possible HDI via formation methods. Because of the possible differences in cross-sectional appearance, it is usually not feasible to cross-section microvias. Acceptability is discussed in Chapter 11.

Figure 8 shows the compatibility of laser via, mechanical drilled via, photovia, plasma via, and three other methods with four basic surface dielectric structures on which microvia holes are to be formed. Although laser via methods can cope with all four dielectric structures, photovia and plasma via methods are applicable to only one or two structures, respectively, as shown in the figure. This is one reason why laser via is more widely used today. Another wiring layer is built over the existing microvia holes, which become buried via holes (BVHs).

Interconnect Via Formation

This section discusses processes that employ various drilling via-hole formation techniques. Through-via drilling is possible below 0.20 mm (0.008 in), but cost and practicality discourage this. Below 0.20 mm (0.008 in), laser and other via-formation processes are more cost-effective. There are seven

Compatible O Not X	Standard Configuration Copper Foil	RCC Copper Foil	Thermally Curable Resin	Photoimageable Resin
Laser via, CO ₂	O	O	O	O
Laser Via, UV	O	O	O	O
Mechanical Drill Via	O	O	O	O
Photo Via	X	X	X	O
Plasma Via	X	O	O	O
Insulation Displacement	O	O	O	O
Chemical Etch	X	O	O	O
ToolFoil	X	X	O	O

FIGURE 8: Compatibility of various materials to the various types of via generation

different methods of forming the IVHs used in HDI processes. Laser drilling is the most prominent, but the other six come into use as well. The methods are:

1. Various laser drilling methods including UV-Yag, UV-Eximer and CO₂
2. Mechanical drilling
3. Photo process to define vias in photo-dielectrics
4. Plasma drilling
5. Insulation displacement of via pastes
6. Photo, plating and etch of solid vias
7. Tool foil

The manufacturing process for each microvia technology begins with a base core, which may be a simple double-sided board carrying power and ground planes or a multilayer board carrying some signal pattern in addition to power and ground

The HDI Manufacturing Processes

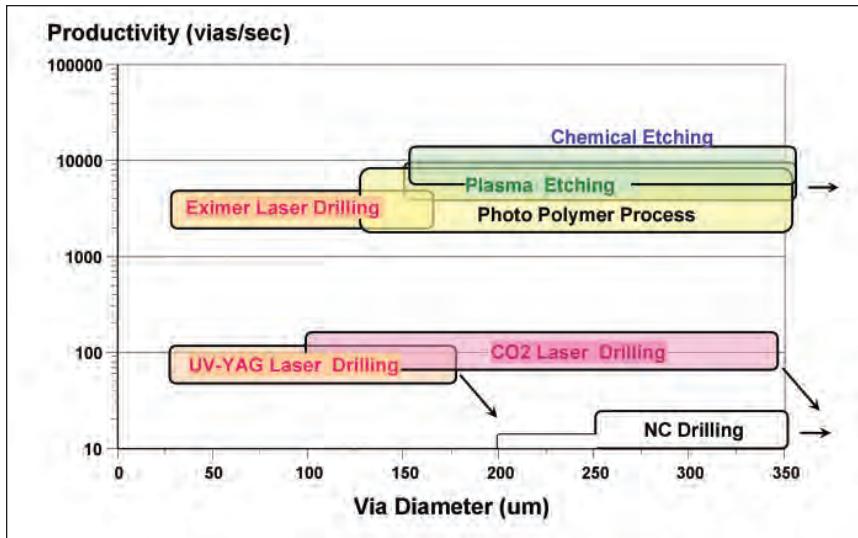


FIGURE 9: Rate of blind via creation by mechanical drilling, various lasers, plasma, photovia, and chemical etching

planes. The core usually has plated through-holes (PTHs). These PTHs become BVHs. Such a core is often called an active core.

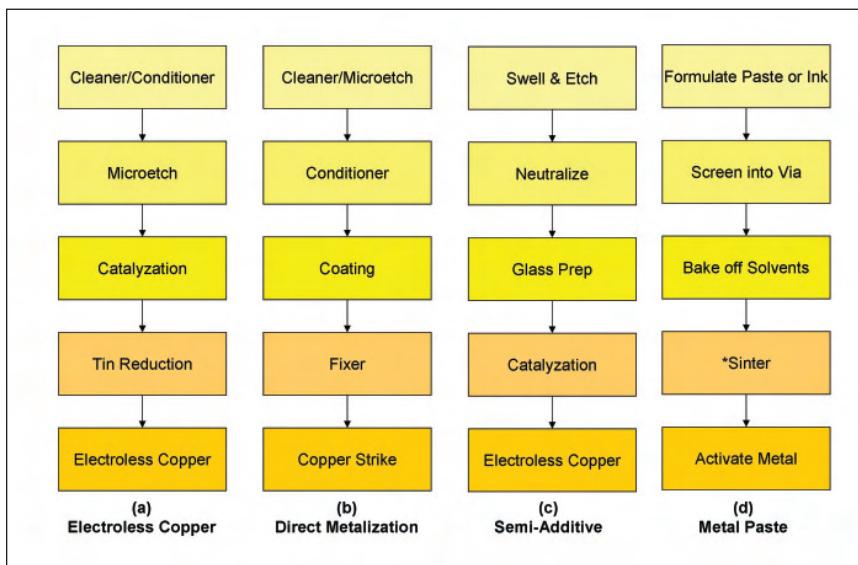


FIGURE 10: Four common processes for metallization of vias

These different methods of via formation have some limits on the minimum size of the vias they form, as well as significant differences in rate of via formation. Figure 9 summarizes some of these differences.

Method of Metallization

The last process is metallization of the vias. There are five different methods of metallizing the IVHs used in HDI processes. The methods are:

1. Conventional Electroless and Electroplating Copper (Figure 10a)
2. Conventional Conductive Graphite or other Polymers (Figure 10b)
3. Fully and Semi-Additive Electroless Copper (Figure 10c)
4. Conductive Pastes or Inks (Figure 10d)
5. Fabricating Solid Metal Vias

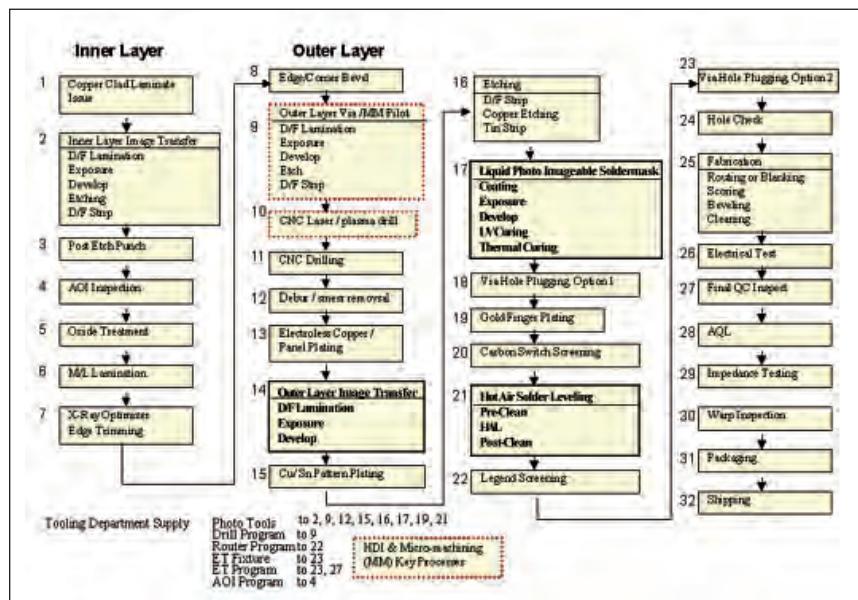


FIGURE 11: The general multilayer fabrication process with HDI laser drilling highlighted by red-dashed lines

The HDI Manufacturing Processes

Figure 10 shows more details of four of the more common methods of metallization of IVH.

HDI Fabrication Processes

Seven major HDI fabrication processes exist around the world for HDI and will be described in detail in Figures 12 through 16, subtitled (a) through (k). The most common process, laser drilling, borrows from the conventional mechanical via drilling process. As seen in Figure 11, laser drilling is just added as another drilling process.

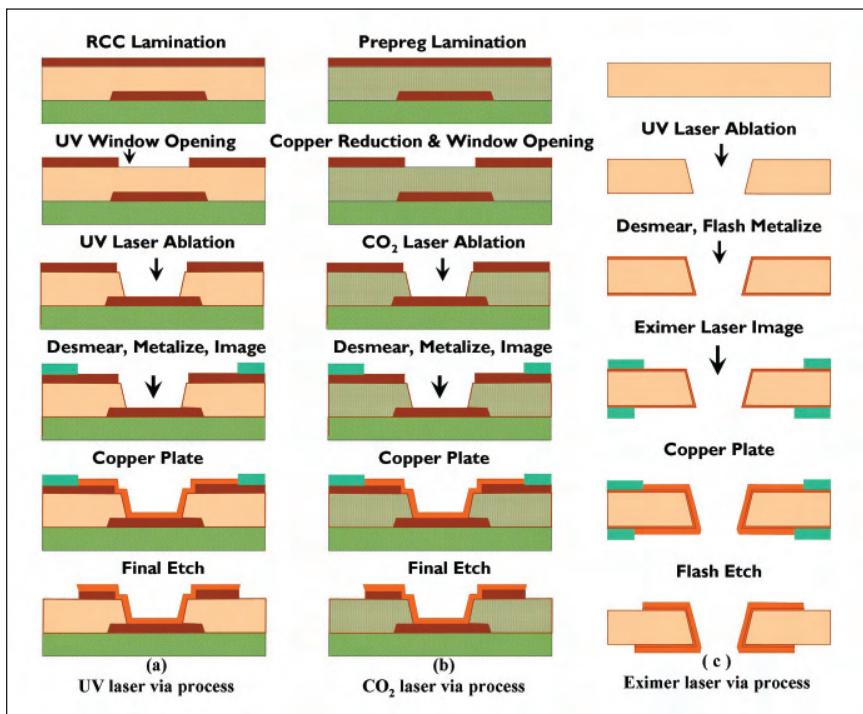


FIGURE 12: Laser generated via process employ (a) UV, (b) CO₂, and (c) eximer methods

Laser Via Technology

Laser via processing is by far the most popular microvia hole formation process. But it is not the fastest via formation

process. In Figure 9, the chemical etching of small vias is the fastest, with an estimated rate of 8,000 to 12,000 vias per second. This is also true of plasma via formation and photovia formation. These are all mass-via-formation processes. Laser drilling is one of the oldest microvia generation techniques.[4] The wavelengths for laser energy are in the infrared and ultraviolet region. Laser drilling requires programming the beam fluence size and energy. High-fluence beams can cut metal and glass, whereas low-fluence beams cleanly remove organics but leave metals undamaged. A beam spot size as small as approximately 20 microns (<1 mil) is used for high-fluence beams and about 100 microns (4 mils) to 350 microns (14 mils) for low-fluence beams.[5,6]

The laser is the most common method of production of microvias to be plated or filled with a conductive paste. Lasers are capable of ablating dielectric material and stopping when intercepting the copper circuitry, so they are ideally suited for creation of depth-controlled blind vias. Figure 12 shows these three major laser processes.

Most laser processes utilize either CO₂ or UV lasers since they are the most readily available and economical lasers. When using a CO₂ laser to produce vias in epoxy laminates, the copper must be removed above the area to be ablated. The CO₂ laser is primarily used for laminates not supported by glass. This includes unsupported laminates such as flexible polyimide and resin-coated copper (RCC) foil and laminates reinforced with alternative materials such as aramid fibers. The modified TEA CO₂ (Transversely Excited Atmospheric) lasers are specifically created to laze through glass fibers using 9,000 nm wavelength and higher peak power.

However, there are many variations. For the purpose of drilling microvia holes, there are five laser systems: UV/

The HDI Manufacturing Processes

Eximer, UV/Yag laser, CO₂ laser, Yag/ CO₂, and CO₂/ TCO₂ combinations. There are also many dielectric materials: RCC, resin only (dry film or liquid resin), and reinforced prepreg. Therefore, the number of ways to make microvia holes by laser systems is driven by the permutation of five laser systems and these dielectric materials.

Higher power lasers (i.e. Ultra Violet-UV) can remove glass and copper and can therefore be used with conventional laminates, but are typically slower when going through copper and glass fibers. There are several factors to consider in laser via processing: position accuracy of lased holes (microvia holes), uneven diameters of holes, dimensional change of the panel after curing dielectric, dimensional change of the panel due to temperature and humidity variations, alignment accuracy of the photo-exposure machine, unstable nature of negative artwork, and so on. These should be carefully monitored and are important for all microvia hole processes.

Mechanical Drilling Blind Via Technology

Mechanical drilling has traditionally been the most widely practiced method worldwide for hole creation, but newer techniques have emerged since an increasing number of designs require microvias below 0.20 mm (0.008") diameter. The use and popularity of blind and buried vias has accelerated that trend. Mechanical drilling is anisotropic, that is, the vertical walls are straight up-and-down. Many of the non-drilling processes are isotropic, that is, the walls of the via recede laterally as much as they go deep or have sloped walls so the entry opening is larger than the exit opening. A larger entry opening facilitates metallization, but the isotropic receding wall can prevent metallization and is difficult to plate-up. Thin plating on the hole wall is a definite reliability

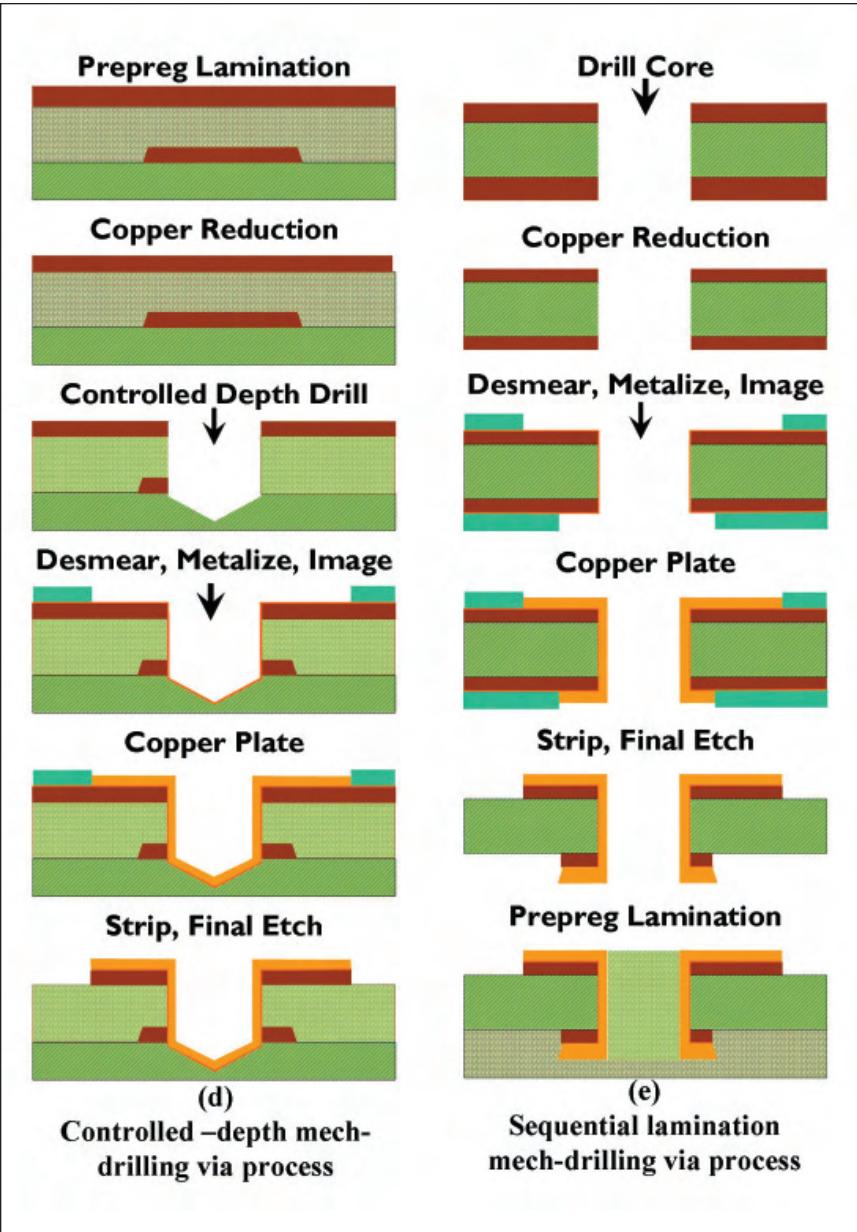


FIGURE 13: Mechanical drilling of blind vias by (d) controlled depth and (e) sequential lamination

problem. Figure 13 shows these two mechanical methods of blind via creation.

Photo Process Defined Vias

The photovia process is one of the oldest for forming microvias. The patent for this process was filed in 1983.[1] The process starts with a bare core. Prior to dielectric material coating, the copper surface of the base core must be treated by an adhesion promotion process to ensure good adhesion of dielectric material to the copper surface. Today, very few manufacturers use oxide treatment for this purpose. The most popular adhesion promotion treatment is a special etching process offered by many suppliers of chemicals. This step is common to all microvia processes.

Dielectric resin is semicured after coating to eliminate tackiness, and then the hole pattern is exposed by photo exposure processing. The usual photo developing process creates microvia holes and the dielectric is fully cured, typically at 160°C for about 1 hour. The panel then goes through a permanganate etching process to remove any residual resin at the bottom of the hole and simultaneously create microporous surfaces that act as anchors and ensure desirable peel strength after copper plating.

The level of peel strength is controversial. Minimum peel strength required for chip package substrates is about 600 g/cm², but motherboard users, particularly cell phone makers, demand a minimum of 1.0 kg/m² or more in order for cell phone handsets to withstand drop tests. Laser via materials usually yield stronger peel strength because of fillers that can be added to dielectric resin. When etched, these fillers generate a superior microporous surface structure needed for strong peel strength.

After permanganate etching, the panel is catalyzed and metallized in an electroless copper bath and panel-plated galvanically to desired thickness. Some photovia process

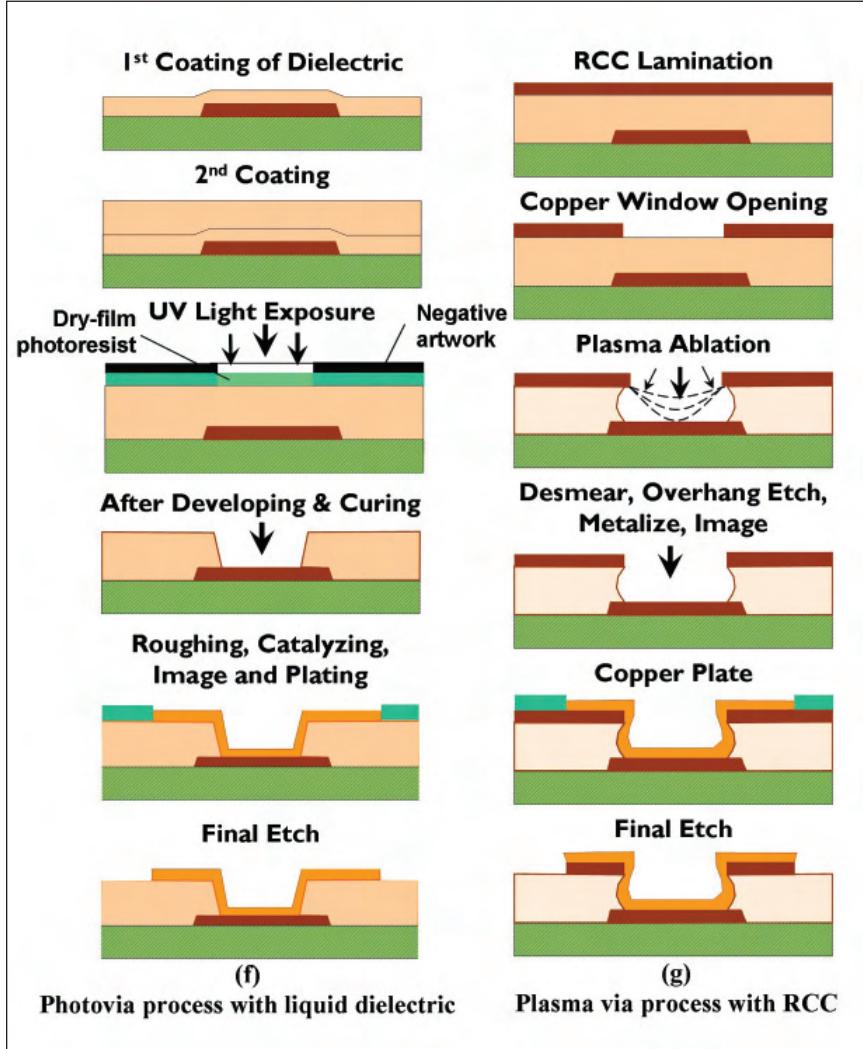


FIGURE 14: Standard HDI manufacturing processes: (f) a typical photovia process with liquid resin dielectric; (g) the standard plasma via process with RCC

practitioners roughen the resin surface mechanically by brushing or liquid honing prior to catalyzing. Then, the conductor pattern is formed by dry-film tenting and etching. Some manufacturers prefer to use the pattern-plating method for this purpose. Very few microvia board manufacturers use direct metallization methods for metallizing holes prior to

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galvanic plating. Several Japanese manufacturers use electroless copper all the way to the desired thickness in panel plating and use a positive electrodeposited (ED) system to achieve fine lines and very small annular rings.

One important step in microvia hole board fabrication when resin is the dielectric choice, whether the process is photovia or laser via, is the removal of residual catalysts (normally palladium) entrapped in a microporous surface that can cause migration. The process used in this step is normally a trade secret.

Photovia processing is now used primarily to fabricate semiconductor chip package substrates because a large number of holes can be formed in one photo exposure and development step. However, as mentioned previously, photovia processing suffers more from material shrinkage than laser via processing after full cure, and hole locations tend to move randomly, which makes subsequent registration for patterning difficult. Because of this problem, photovia users limit the size of the panel to about 400 mm × 400 mm, much smaller than the usual panel size prevalent in motherboards. Small hole formation is also difficult with the photovia process. As a result, even makers of package substrates are now resorting more to laser via processes as the laser drilling speed is being improved. Photovia process users engaged in mass production are found only in Japan today. All photodielectric processes have certain characteristics in general. A standard photovia process sequence is described in Figure 14f.

PhotoImageable Dielectric (PID) technology has been used to manufacture high-density printed circuits and IC package substrates for computer and communications equipment and consumer electronics. Figure 3 is an example of system board used in a laptop computer, and Chapter 1- Figure 7 and

Chapter 2 - Figures 2 and 3 illustrate the main board used in a digital camcorder.

PID technology is based on photoimageable polymeric systems to form blind microvias in dielectric material between layers of circuitry. The use of PIDs allows all microvias on a panel to be formed simultaneously, with no incremental per-via cost. Their use is particularly advantageous on applications having high densities of vias (e.g. more than 50,000 on an 18" x 24" panel).

In order to differentiate between liquid and dry PID, a typical flowchart of the PID technology fabrication process, with multilayer core is given in Figure 14f. At this level in the process, PID technology is the same whether a liquid or dry film PID is used. Liquid and dry-film PIDs do provide slightly different via wall profiles. The liquid PID has tapered via walls, while the dry-film PID has essentially vertical via walls. The tapered via walls provide good plating coverage on the via walls and base. Vertical walls allow for a smaller via top opening, and correspondingly smaller capture land for a given via bottom diameter.

The use of a liquid PID requires two unique pieces of equipment: a coater of some variety, either curtain, slot, roller-coater, or screen-printer (with associated drying ovens), and a leveling tool (surface sander). A leveling tool is required to planarize the surface of the cured liquid PID to accommodate fine-line photolithography on the surface. Liquid PID provides a conformal coating over underlying circuit features, producing non-uniform planarity. The leveling operation also removes a lip of exposed PID which overhangs the via openings in these processes. Many liquid PIDs have a self-leveling characteristic, and do not require leveling.

The use of a dry-film PID requires only one unique piece of

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equipment: a vacuum laminator. Vacuum laminators are not common at printed-circuit fabrication shops, but the capital to obtain one is significantly less than for a curtain or slot coater. The dry-film PID has excellent planarization, does not require a leveling process due to the film's low solvent content, low shrinkage, and vacuum lamination process.

Larger printed circuits can be designed with more relaxed rules, while the most aggressive rules are limited to small printed circuits, such as chip carriers, to achieve optimized yields and minimize cost.

Plasma Via Technology

Products made with the plasma via process are called DYCOstrate. There are many variations to the plasma via process, one of which is illustrated in Figure 14g. Today, it is mainly used to fabricate sophisticated flex and flex-rigid wiring boards in small quantities.

First, an opening or window is made through copper foil by a normal etching process. When plasma etching is applied through this window, the shape of the hole tends to be like a bowl (as shown in Figure 14g). Another problem is related to how the microvia hole is formed. The copper edge of the window hangs out over the hole, which results in poor reliability after panel plating. Therefore, to ensure reliable plated holes, a secondary etching is necessary to remove this copper overhang. A beneficial result of this secondary etching is that since surface copper is thinned, formation of finer conductors is made easier. Nevertheless, by the time the panel is ready for plating for subsequent conductor pattern formation, it takes several times longer than other processes in a mass-production environment.

Plasma via processing is effective for forming through-

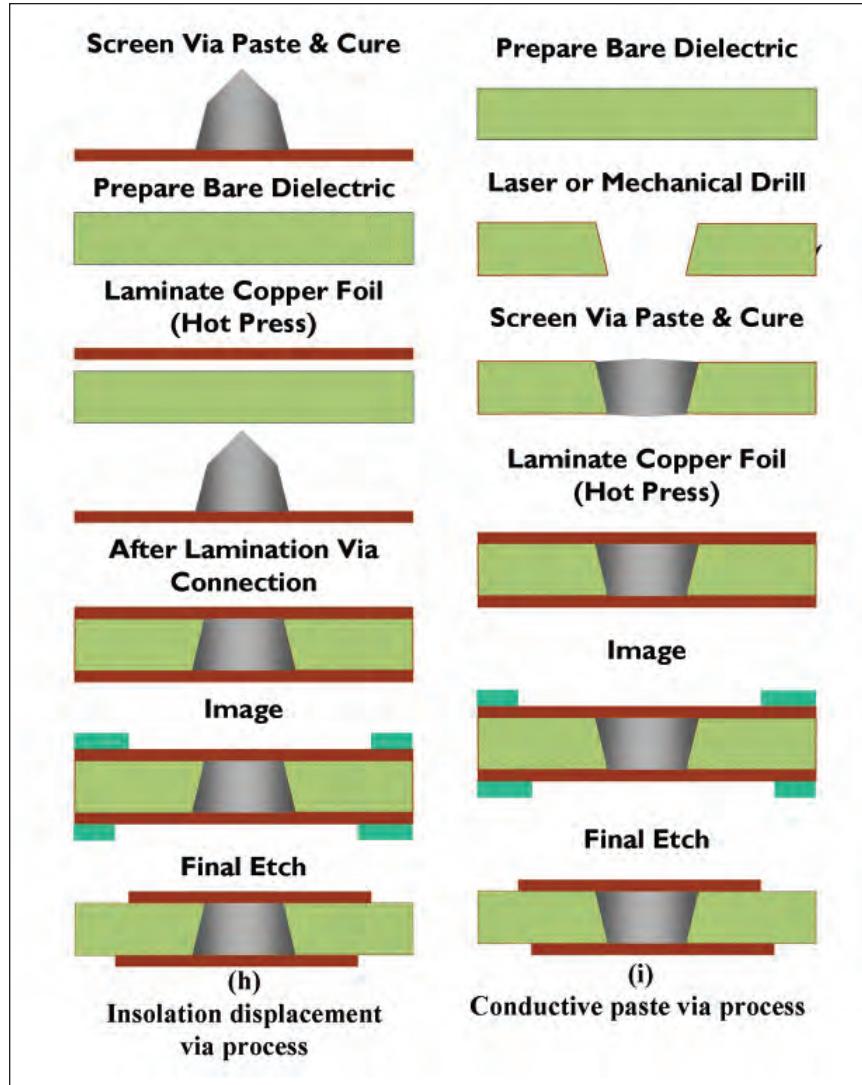


FIGURE 15: Solid microvia from (h) pastes created by insulation displacement and (i) screening paste into the microvia

holes on flexible materials since holes are formed by plasma etching from both sides of the film and the bowl effect is minimized. Plasma via etching evolved from the traditional process of plasma desmearing of through-holes. Different gas, magnetrons, and equipment fixturing are employed by current

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plasma via-etching equipment. The plasma is generated in a partial vacuum filled with a mixture of oxygen, nitrogen, and chlorofluoro (CF_4) gasses. Microwave magnetrons create the plasma field and special low-frequency kilowave units help provide rapid etching of organics.

Insulation Displacement

Three types of dry metallization are insulation displacement, conductive ink, and conductive paste. Insulation displacement is a unique process in that the silver conductive paste is screened on copper foil and cured. The conductive paste forms a “pointed” spike that penetrates conventional preps during lamination and adheres to the copper foil on the reverse side, forming a via. Figure 15h shows this via formation process.

Conductive ink describes a single-layer dielectric with microvias formed by photoimaging, laser, or insulation displacement. A conductive paste is used to fill the microvias and act as the conductive path between layers. Surface metallization may be accomplished either by laminating copper foil onto the dielectric surface or by chemical deposition. This process is shown in Figure 15i.

Standard HDI processes concentrate on the use of photoimaging and metallization, while solid paste vias are used to overcome the limitations and expense associated with processes such as plating and etching. The concept is built on the use of a photoimageable dielectric to produce both vias and circuit channels that are then filled with a conductive ink. These approaches eliminate the need for a separate dielectric and clad-metal layer that requires either etching or a combination of plating and etching to produce a circuit. They also eliminate the resist deposition and stripping previously

required to define the circuit. The conductive ink technique of metallization virtually eliminates the generation of metal waste streams.

Photo or Etch of Solid Vias

Defining the via structure with solid vias can be accomplished by either using photoresist to define these vias and then electroplating them or having the photoresist protect where you want the vias and then etching the rest of the copper away. Either way, you end up with a solid via post. This is actually one of the oldest ways of making a microvia board. As early as 1980, PACTEL Corp. in Los Angeles had produced

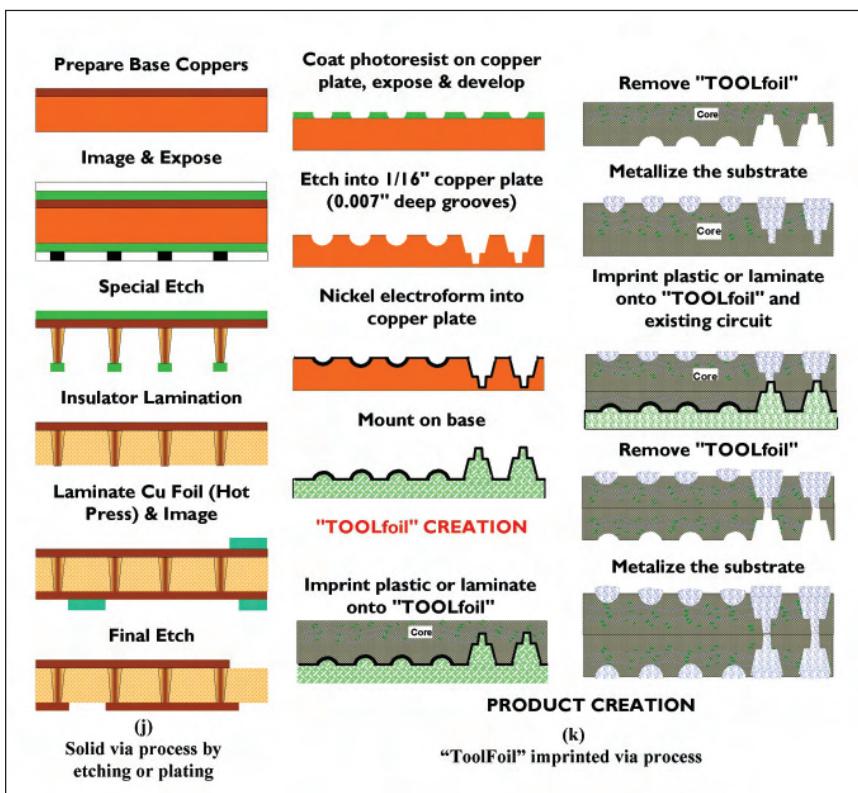


FIGURE 16: Solid copper microvias formed by (j) etching a solid copper sheet and (k) ToolFoil imprinting process

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small modules with this “Plated Post Via” and used a liquid polyimide resin to fill around the via as the dielectric.

The plated or etched solid copper via might be considered a third-generation HDI technology since technologies such as ALIVH are considered second-generation HDI technology. Figure 16j shows the structure of the etched via substrate. The manufacturing process for these structures is unusual in that it does not drill the via connections. Instead, a new material is employed that consists of two different coppers (one thicker than the other) that are bonded together. The thicker copper is imaged and etched to form the interconnect vias. The structure is then filled with a film or liquid dielectric. It is bonded to copper foil and both are cured. These copper foils are then imaged and etched to circuitize the layer pair. The layer pairs can be tested and later stacked with uncured structures to form the final multilayer. Like the second-generation ALIVH HDI structure, these structures allow the connection of any layer to any other layer. This manufacturing process is shown in Figure 16j.

Tool Foil

Imprint patterning is a technique used to manufacture compact discs (CDs). No photoresist, registration, or conventional techniques are employed. Every substrate is a copy of the mold (or ToolFoil, in this case), and each can be done in sequence to make a buildup substrate. The unique characteristic of CDs and DVDs is the millions of 0.5 micron pits or vias. A typical CD includes over 3 km of these. The simple manufacturing process and perfect reproduction of the master tool creates inexpensive and accurate substrates. The patented process is a lab process. Actual implementation is still under evaluation. Figure 16k shows a diagram of the imprinted

circuit structure using a ToolFoil. The unique characteristic of this structure is that all features are embedded in the substrate. The critical dielectric is the part that is imprinted or molded. A long fiber molding compound, such as that used on components' overmolding, is best suited for this task. Such a compound can be used with or without an FR-4 backing. The cross section of an imprint circuit shows the features similar to a CD or DVD, that is, the various impressions. All are metallized but the vias are deeper. This allows the vias to contact the next layer of imprinted circuits.

Creating the ToolFoil starts when a master of the substrate is machined in copper by a UV laser or by photochemical machining. The vias are deep, and the circuits and pads are shallow. Since only one master tool, called a ToolFoil, is required, time can be taken to make sure the master is perfect. With a laser, it is possible to have perfect registration of lands to via holes or even landless vias. This master is electroformed with nickel and back-filled to make a master tool. For production, the mold is filled with a thermoset or thermoplastic resin and then cured. The substrate is additive or semi-additive metallized, and plated thicker with copper. The recesses are filled with an etch resist, and the surface resist is removed to expose the copper surface by polishing or by using an abrasive agent. The exposed copper is etched away and the etch resist is dissolved. The entire manufacturing process does not employ photoresists, exposure, or registration. Because of this, the yield is expected to be very high. Figure 16k shows the process for tool generation and production substrate.

More Details on HDI Manufacturing

The next six chapters of this book cover HDI manufacturing in much more detail. You can see how

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Chapters 7 through 12 are the main sections on the details of HDI manufacturing.

Chapter 7: Small Hole Creation

This chapter will cover key via formation technologies including laser via formation and where appropriate, mechanical drilling and photovia formation

Chapter 8: Metallization

Desmear and metallization (electroless), including the materials and processes for paste in vias

Chapter 9: Fine-Line Imaging and Etching

Image transfer processes, stripping and etching fine lines, registration, equipment, and materials for fine-line image transfer

Chapter 10: Via-fill, Plating and Finishes

Plating, pulse-plating, small-holes plating and filling, final finishes

Chapter 11: Inspection and Testing

Inspection, AOI, and electrical testing of HDI

Chapter 12: Quality, Acceptability and Reliability

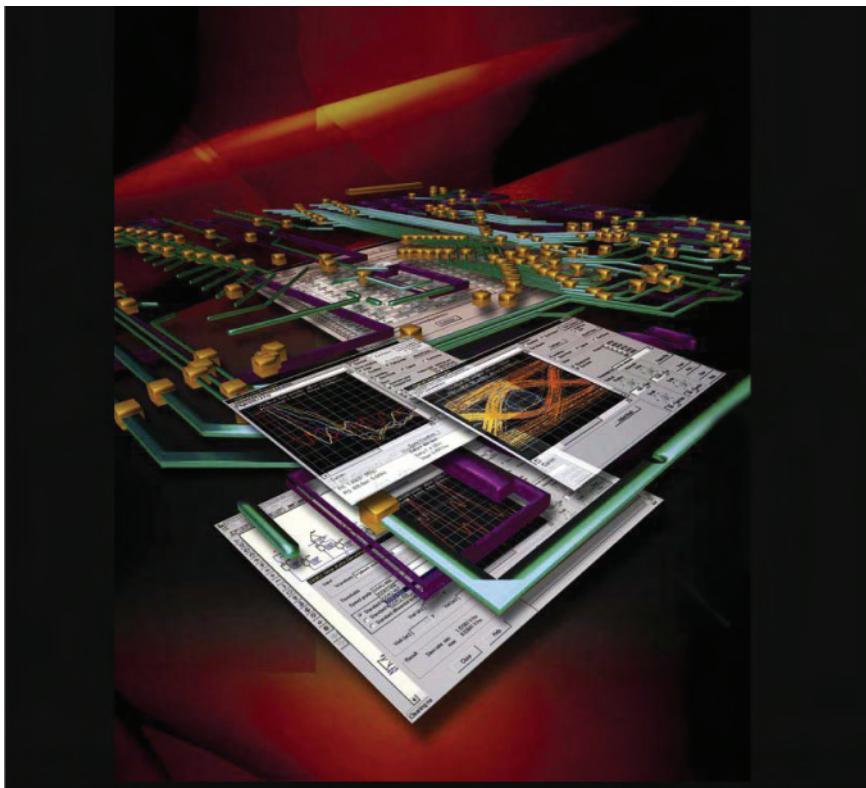
Performance of HDI benchmarking, vendor readiness, qualification, quality issues, lab techniques, and equipment

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7

Small Hole Via Formation

By Michael Carano

Introduction

“Of all the interconnection methodologies, the manner in which holes (or vias) are produced has the most effect on the relationship of the interconnecting structure and how it is produced.”[1] These are very insightful words that must never be taken for granted. Any experienced fabricator knows that via quality has a direct relationship to via plating and most often end-product reliability. Fabricators involved in HDI must understand that there are trade-offs between mechanical via formation and alternatives such as laser. Productivity, capital expense costs, maintenance, and overall via quality limitations must be considered.

Technology Drivers

It is all about density. As early as 1988 a few Ball Grid Array (BGA) packaging developers were attempting to evolve Pin Grid Arrays into surface mountable packages. Real BGAs began showing up in 1990, and by 1993 a few major companies like Motorola, IBM, and Compaq placed the BGA on the mainstream roadmap. Currently BGAs and microBGAs are the packages of choice for high pincount (>240) applications. Higher pincount is forcing finer pitch and pincount is expected to reach 2400 in the year 2009

Small Hole Via Formation

with a body size of 50 mm. The signal I/O escape wiring and its interconnect to other high I/O packages will require very dense PCBs. Circuit board designers need to provide solutions for interconnecting high I/O components. While they can add layers, it quickly becomes apparent that “Via Starvation” is the biggest stumbling block to successful circuit design which will impact not only the design, but the cost to fabricate as well. Additional solutions encompass finer etched lines and spaces, which come at a tremendous cost. Smaller mechanically drilled holes also become cost restrictive as holes are reduced to less than 0.010 inches (0.254 mm).

Mechanical Drilling of Microvias

Analysis of the different mechanical and laser techniques shows that mechanical drilling is predominant for through-vias and large via diameters (Figure 1). However, one should not discount the ability of mechanical drilling to form high quality microvias. Of course there are limitations as to the via diameter attainable with mechanical via formation. Mechanical drilling is limited to via sizes larger than approximately 100 um (4 mils). Also the production of blind vias requires special techniques like drill depth control to ensure repeatable blind via depth.

Mechanical drilling is a proven technology that covers a large range of via diameters with high aspect ratios (depth to width). It is most economical for through-vias and blind vias larger than 200 um (8 mils) in diameter. To bridge the gap to microvias, special techniques are used to achieve depth controlled drilling of small via sizes. High speed spindles are combined with different kinds of depth sensors. Thanks to a technique called Electric Field Sensing (EFS), a very high precision blind via can be formed. EFS is based on a simple

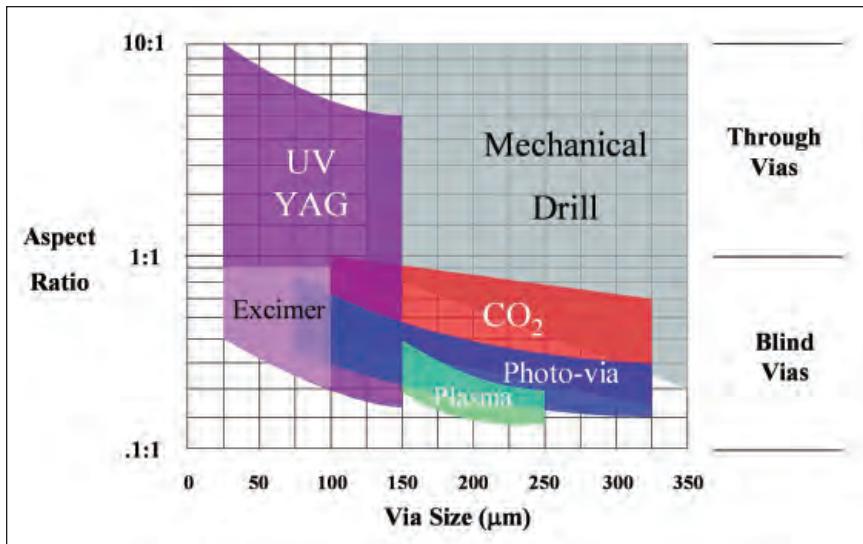


FIGURE 1: Via Technology map

antenna theory where the pressure foot is flooded with a low power microwave field. The drill bit is used as an antenna to sense this field and monitor the output signal. The drop of the signal indicates the drill bit touching a metal surface such as a copper surface of the board. From this "ZERO" position, the Z-axis drills into the board with an accuracy of 15 um (0.2 mils) without the use of mechanical parts that are prone to wear and tear or optical elements which are prone to debris.[3]

With improvements in software and drill bit quality, it is possible to manufacture blind vias mechanically. Generally, one must recognize that there are limitations as to the depth and minimum via diameter that are attainable. Yet, the capital cost for a mechanical drilling tool may already be fully depreciated, making the move to HDI fairly easy from a capital equipment standpoint. This may allow for a competitive cost solution to via formation. The use of existing mechanical drilling equipment for microvias offers a great opportunity to start manufacturing microvias. Some of the depth control

Small Hole Via Formation

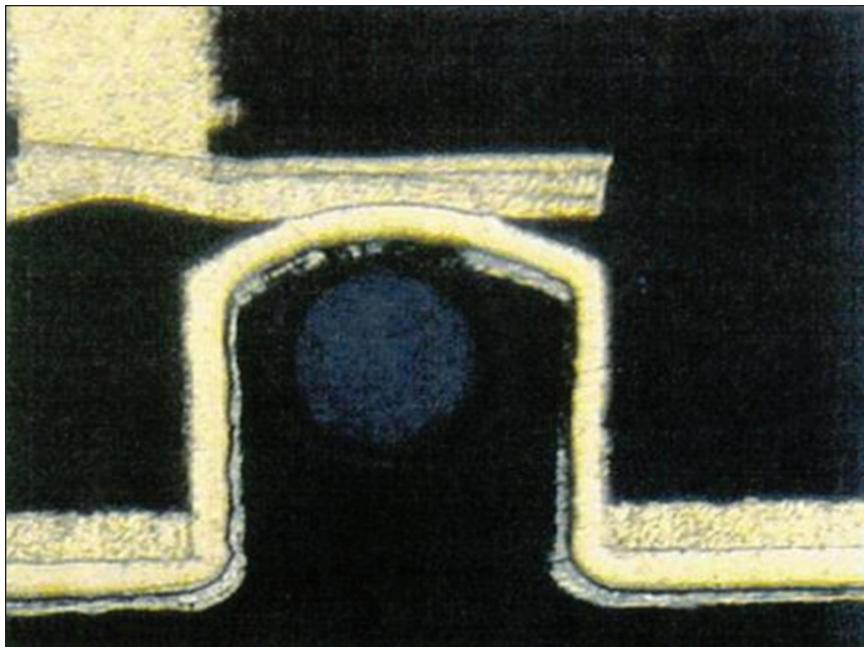


FIGURE 2: Mechanically drilled microvias

systems are even available as upgrades for existing machines. With very limited capital expense, the cost model for mechanical drilling is very simple and is reduced to the cost of operation. An example of mechanically formed microvias is shown in Figure 2.

The advantage of a smooth transition from traditional drilling to microvia formation on existing equipment is also significant. Transition costs, resulting from downtime while fine-tuning upstream and downstream processes (plating, inner-layer alignment, etc.), can be limited. Having the processes under control will make the adoption of other microvia formation technologies much more rapid.

So, why consider laser drilling at all and not use mechanical drilling for all microvia production? Although the capital cost may be very low for mechanical drilling, the operating cost may not be. The cost per via is mainly

determined by drill bit cost which is strongly dependent on the bit (via) diameter. Worn and broken drill bits increase the cost of operation significantly. The cost of drill bits is dependent on the price of tungsten and cobalt. During the last year or so, both metals prices have increased significantly.

With advances in laser via formation equipment, one must consider its implementation and the factors that effect it as via diameters decrease for certain applications:

- Laser characteristics
- Fluence
- Pulse rate and duration
- Beam size
- Peak power

Laser Via Formation

Laser via formation has already been established for high volume production of blind vias and microvias and is strongly growing. Worldwide microvia production output nearly doubled from June 1999 to August 2000, while the laser share increased to more than 90% during the same period.[2] The capital costs for laser via formation are considerably higher. Due to the high processing speed resulting in high throughput, the cost per 1,000 vias can be significantly lower than with mechanical drilling. Depending on the application, required accuracy, and via diameter, different laser types and techniques are applied.

CO₂ Lasers

CO₂ lasers are efficiently used for blind via formation in copper clad or unclad dielectric materials. With wavelengths between 9.6 um and 10.6 um, they are available with high peak and average power to achieve high ablation rates.

Small Hole Via Formation

Conformal mask processing uses chemical etching to open the copper over the capture pads. The dielectric is then drilled with a CO₂ laser, using the opening in the copper as a conformal mask. Laser systems for drilling unclad material use a mask in the laser beam to define via size. Either way, state-of-the-art CO₂ systems achieve net drill rates of 20,000 vias of 100 um (4 mils) diameter per minute. With system prices of approximately \$450,000, the cost can be as low as \$0.05 per 1,000 vias.

There are limitations in via diameter and accuracy related to CO₂ lasers. Due to the wavelength, CO₂ lasers are limited to via sizes larger than 75 um (3 mils). Moreover, the etching process doesn't allow the alignment of the vias to the signal layer and there is no correction of individual shrinkage or stretch possible. The result can be misregistration and lower yield. This technology is therefore applied for low margin, mass production products such as handheld devices (cell phones, pagers, etc.). These products are typically manufactured in Southeast Asia to take advantage of the low labor costs. As smaller via diameter and higher accuracy are required, UV or hybrid laser processing should be considered:

- RF excited CO₂
- TEA CO₂
- CO₂ laser drilling rates
- Nd:YAG lasers

The Nd:YAG Laser with a wavelength of 355 nm (UV) is very effective at ablating most of the metals (Cu, Ni, Au, Ag) that are found in printed circuit applications. These metals show absorption rates of more than 50%. Organic materials can also be accurately ablated. The high photon energy of UV lasers at 3.5-7.0 eV cracks the chemical bonding as the

ablation process in the UV spectrum is partly photo-chemical and partly photo-thermal. These capabilities make a UV laser system the first choice for applications in printed circuit board fabrication.

UV lasers can produce microvias down to 25 um (1 mil), due to their short wavelength. Industrial, diode-pumped, solid-state (DPSS) UV lasers deliver stable output, combined with maintenance cycles, of around a thousand hours. Good beam quality ensures a minimum focus diameter and maximum depth of focus, resulting in well-defined vias with small taper angles. As more powerful UV lasers become available, productivity will improve greatly.

To achieve blind vias with a desired diameter, the UV laser is used like a milling tool to ablate copper and dielectric. Starting from the center of the via, the laser spot (approximately 25 um) is moved in concentric circles or spirals until the desired via diameter is achieved. This is known as “trepanning.” It is obvious that this procedure takes more time with increasing via diameter and material thickness. An example of UV drilling a board of FR4-1080 material (2.5 mils) with 46,800 vias of 150 um (6 mils) diameter shows a net drilling rate of below 40 vias per second, resulting in costs that can be ten times higher compared to CO₂ systems. These costs are only justified if the accuracy requirements are so stringent that a UV laser with its high resolution is absolutely needed.

Hybrid laser systems feature both a DPSS UV laser and a CO₂ laser. These systems combine the best of both worlds. The UV laser is only used for the most precise copper ablation, while the CO₂ laser is used for fast and efficient dielectric drilling:

- Nd:YLF lasers
- Excimer lasers

Overview of the Different Laser Via Formation Options

The various laser via formation options are presented below. A wide variety of material can be laser drilled but the speed and, therefore, the throughput of the drilling process depends on the material properties.

Via Formation with CO₂ Lasers

CO₂ lasers efficiently remove dielectrics, even non-homogeneous, glass-reinforced dielectrics. However, the CO₂ laser alone cannot create small vias (say below 75 µm) and cannot remove copper, aside from limited success in removing pre-treated thin foils 5 µm and below.

While the ability of CO₂ lasers to create many more vias per unit time than UV lasers, the conformal mask process must be employed to realize the increased throughput. The conformal mask process is graphically illustrated in Figure 3. In the conformal mask technique, the copper surface is used as a mask in which holes are etched using standard developing, etching, and stripping methods. A laser beam is then used

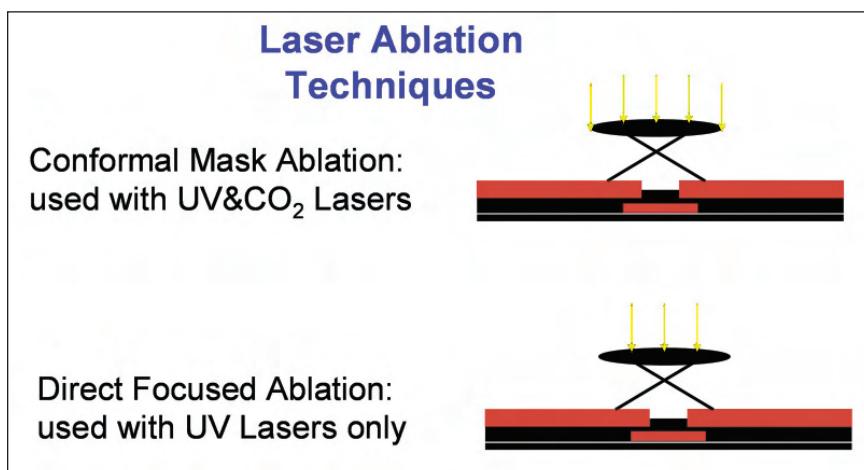


FIGURE 3: Two masking type laser ablation techniques to form blind vias

to illuminate the holes and remove the exposed dielectric material. Either a CO₂ or an excimer laser may be used to process the dielectric material. Naturally, the developing, etching, and stripping process adds cost and time to the manufacturing process. Practical high-volume via size, using the conformal mask technique, is limited by the etching process to between 80 mm and 150 mm.

UV YAG Direct Via Formation (DPSS)

The diode-pumped solid-state UV laser can be used to create very small vias and remove all common copper foils (from 3 µm up to 36 µm, 1 ounce, and even plated foils). UV lasers alone can also remove dielectrics but the material removal rate is slow. Moreover, the results are generally poor for non-homogeneous materials such as glass-reinforced FR4s because the glass can only be removed if the energy density is increased to levels that can damage the inner-layer capture pad. The DPSS technique uses a focused beam from a pulsed laser to ablate both copper and dielectric PWB materials. In general, copper is highly reflective in the far infrared (FIR) and absorptive in the UV (Figure 4). Recently, however, coatings

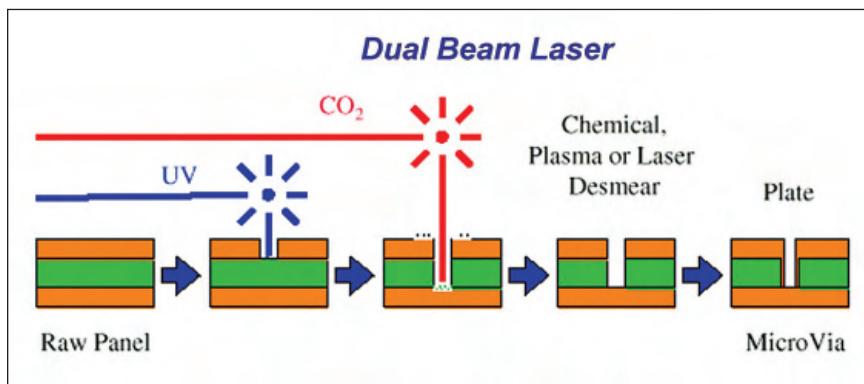


FIGURE 4: Dual laser drills have both the CO₂ laser and the UV laser present to optimize drilling flexibility and speed.

Small Hole Via Formation

have been developed which, when added to thin copper (pre-etched to reduce thickness), increase the copper's absorption in the FIR, allowing drilling of copper with FIR lasers such as CO₂. The advantage of adding coatings to thin copper is that higher drilling speeds, compared to the speed of current UV drilling, can be obtained. While this technology is in mass production today, most copper drilling is still done with DPSS lasers. The shorter wavelength of the DPSS permits the system to focus on a much smaller spot. However, when drilling larger diameter blind vias, the UV laser must be made to trepan or spiral in order to form the larger diameter vias. Of course, this takes time, an issue that CO₂ systems do not face.

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8

Desmear and Metallization

By Michael Carano

Overview of Desmear and Metallization Technologies

Hole preparation and metallization are critical processes in the creation of reliable plated through-holes and blind vias. The function of the desmear process is to remove via formation residues from interconnects and via capture pads in order to effect a tightly adherent bond of the subsequent metallized coating. Residues originate from the heat of drilling and from materials remaining on the capture pad from laser drilling. The desmear process, whether alkaline permanganate, plasma, or a combination of the two, is also designed to create *topography* or micro-roughening of the resin. Topography alteration enhances the adhesion of the subsequent deposit and improves the overall dynamics, allowing for a more uniform distribution of the deposit, whether it be a conductive coating for direct metallization or a palladium-based catalyst used in conventional electroless copper processes.

Numerous experts in the field of PTV/BV reliability have proven that long-term reliability is heavily dependent on the quality and uniformity of the copper deposit within the through-hole and blind via. However, it is often not recognized that the metallization process that precedes the application of the electrodeposited copper is critical to

Desmear and Metallization

depositing a uniform copper layer in a blind via and through-hole. The process of making the via conductive determines whether or not the subsequent electrodeposited copper will be continuous and adherent to the resin and any supporting structures, such as glass or other fiber material. Today, there are several processes that can be utilized to render vias conductive:

- **Electroless Copper**
- **Palladium-based Direct Metallization**
- **Graphite**
- **Carbon Black**
- **Conductive Polymer**

These metallization processes (also known collectively as “making holes conductive” or MHC) are well-developed for both plated through-hole and blind via metallization. The information on each process will be presented elsewhere in this chapter. First, however, the process of desmear must be approached, as it is integral to the overall success of the MHC operation.

Plasma Desmear Technology

Using plasma to desmear eliminates an entire wet process line, reduces chemical disposal cost, and reduces water usage and treatment costs. Labor costs are reduced as well, since there are no baths to maintain. With plasma etching, the panels are placed in a vacuum chamber and gas is introduced and converted to reactive plasma by a power supply. The plasma reacts at the panel surface and volatile by-products (resin smear) are removed by the vacuum pump.

The addition of relatively inert gases, such as nitrogen or argon, stabilizes the plasma and controls the rate of ionization. Reactive oxygen species oxidize organic contaminants on the

surface, creating volatile species that are pumped away. Etch rates are increased by providing more reactive species in the form of fluorine such as F₂, CF₄, or CHF₂.

One potential drawback of using only plasma desmear is that it can leave the treated resin in a somewhat inert condition. This type of condition, if not carefully studied, may lead to metallization issues such as voids and plating adhesion failures. A possible remedy is to follow plasma desmear with an alkaline permanganate cycle. There are some additional limitations to plasma when manufacturing HDI type PWB designs. The first was the dielectric undercut beneath the copper around the microvia hole, a phenomenon caused by the isotropic nature of the unrefined plasma etching process. For every 0.001 inches of dielectric etched downward, 0.0009 inches of lateral undercut was made around the sidewalls of the microvia hole. For example, in a 0.002 inch epoxy thickness, a plasma etched microvia hole would have a circumferential etching of 0.0018 inches, and a nominal 0.004 inch diameter microvia would be undercut to an actual size of 0.0076 inches.

The second process limiter was the requirement to remove the copper clad overhang from the blind via holes prior to copper plating. To remove 0.0018 inches of copper overhang, one half-ounce of copper foil would be reduced by nearly 400 micro-inches, leaving the panel with only 200 micro-inches of copper foil across its surface. Two options were available. The first was to process the boards multiple times through a persulfate microetch. The second was to process them through a special dilute cupric etchant. Although both expedients worked and some nice prototype microvias were produced, it soon became clear that significant process breakthroughs were needed to develop a production process for reaching the goal

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of manufacturing 0.003 inch microvia holes in 0.010 inch land pads.

The Alkaline Permanganate Process

Unlike the dry method of plasma, alkaline permanganate is a multi-step process designed to remove smear and micro-roughen the resin. The desmear cycle removes the smear, allowing the electroless copper and acid copper to bond properly to the inner-layer. The desmear process is also used to make sure the resin surface is properly prepared so that the catalyst and electroless copper can bond to the resin.

The desmear process consists of four steps:

1. Solvent Sweller
2. Permanganate
3. Neutralizer
4. Glass Etch (Optional)

Solvent/Sweller/Hole Cleaner

The purpose of the solvent is to swell the resin so that it can be more easily attacked by the permanganate solution that follows. Important factors include dwell time, concentration, and temperature. If dwell time in the solvent is low, there will be minimal removal by the permanganate. If dwell time in the solvent is high, the solvent may penetrate farther than necessary and remain in the resin after processing through the permanganate.

Permanganate

The purpose of the permanganate is to remove resin by oxidizing the resin bonds. It consists of permanganate and hydroxide. Important factors include dwell time, concentrations of the permanganate and hydroxide,

temperature, and buildup of residue. If dwell time in the permanganate is low then resin will not be properly removed. If dwell time in the permanganate is high then too much resin will be removed and the hole wall may be uneven. Excessive dwell time may also result in less topography along the hole wall due to removal of resin beyond what has been swelled by the solvent step.

Neutralizer

The purpose of the neutralizer is to remove any permanganate remaining on the panel. Important factors include dwell time, sulfuric acid, and E-Prep Neutralizer concentration and temperature. If permanganate is left on the panel this will inhibit proper catalyst adsorption which may cause electroless copper voids on the resin, hole wall pullaway, and a general contamination on the capture pads or the interconnects. If permanganate is left on the copper inner-layer or capture pad, plating separation is highly probable.

Glass Etch

The purpose of the glass etch (if required) is to frost or remove glass fibers from inside the holes. Important factors include dwell time, sulfuric acid concentration, glass etch concentration, and temperature. The glass etch step can be combined with the neutralizer step, however, it is more cost-effective if they are separate.

The effectiveness of the desmear process is dependent upon maintaining the proper times, temperatures, and concentrations. Rinsing is very important in the desmear process. Proper rinsing will prevent problems with excessive drag-in causing contamination of baths. Rinse time, rinse temperature, and the quality of the rinse water are very

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important. In the desmear process it is critical to follow all posted rinse times, especially between solvent and permanganate because improper rinse times can lead to poor micro-roughening of the resin. Poor rinsing after the permanganate can cause high consumption of the neutralizer.

It is important to recognize that higher performance resin systems typically used for many HDI applications are much more difficult to desmear and texture. The fabricator may need to adjust the permanganate cycle to account for these materials. Less than optimum topography on any resin system, as shown in Figure 1, presents problems with respect to the subsequent metallization process. Smooth topography has less surface area to attract both the catalyst (from the electroless copper process) or the conductive coatings used in the direct metallization processes.

High Tg resins are more chemically resistant to certain desmear systems. The solvent conditioner must have the

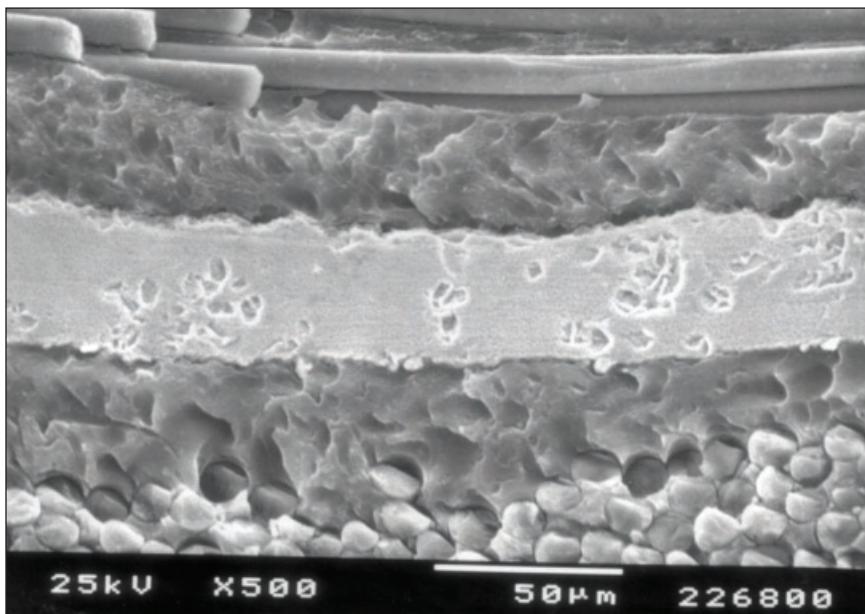


FIGURE 1: Resin surface after desmear - high Tg resin

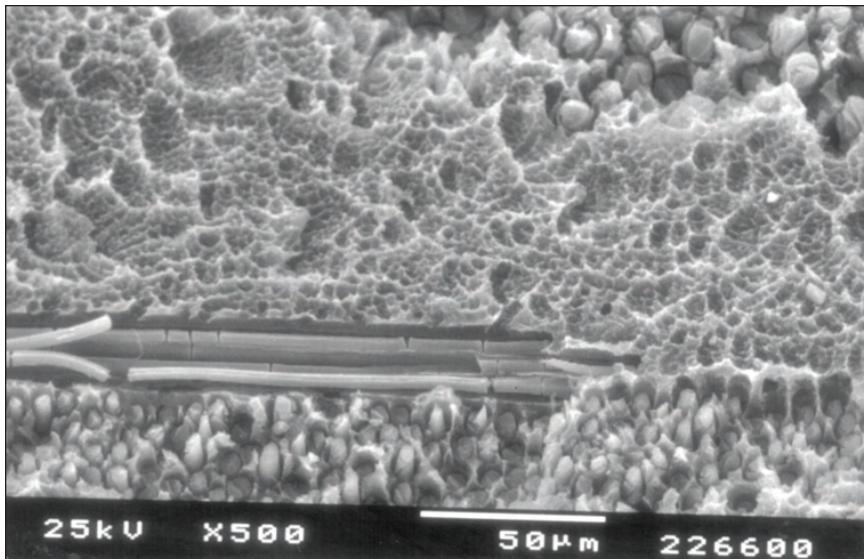


FIGURE 2: Resin surface after desmear-140 Tg resin

ability to penetrate the polymer resin matrix and weaken those polymer-polymer bonds. This interaction is sometimes referred to as a swelling action. Once weakened (or swelled), the bonds are more easily attacked (oxidized) by the alkaline permanganate solution. The oxidation that takes place is responsible for the honeycombed appearance of the resin. However, with less solvent interaction and penetration with the resin, the topography will be less pronounced. Keep in mind that the modified solvent systems do not dissolve the resin. Through the swelling action, the solvent acts as a barrier to additional solvent penetration. Thus this could be considered self-limiting.

Figure 2 shows a typical topography on 140 Tg FR-4. Note the texturing that is visible. This degree of roughening is due to the lower cross-linking inherent in the standard FR-4 material.

It stands to reason that the higher Tg materials exhibit lower resin removal rates. But, experience tells us that resin

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removal is less of an issue than actually achieving some degree of topography. The topography is needed to enhance the adsorption and adhesion of either the electroless copper catalyst or, in the case of direct metallization, the conductive material required to enable electrodeposition.

Special Conditions

One must also be very careful not to be overly aggressive in the desmearing of the resin in the blind vias. Excessive dwell times, temperatures, and chemical concentrations will cause undercutting of the resin near the junction of the capture pad. This condition will result in plating folds or voids.

Electroless Copper

The electroless copper process is designed to deposit a copper coating on the board surface and along the hole wall. Its purpose is to make the hole conductive to allow further buildup of copper in acid copper plating. The electroless copper process involves four major pretreatment steps:

Cleaning/Conditioning

The cleaner/conditioner is designed to remove soils from the surface and holes. It also conditions the glass and resin to ensure proper catalyst adsorption to these surfaces. Dwell time, concentration, and temperature are important factors.

Microetching

The microetch is designed to micro-roughen the copper surface, improving the bond between the electroless and laminate copper. Important factors are copper concentration, sulfuric acid concentration, oxidizer concentration, dwell time, and temperature. Too low of an etch can cause poor electroless

adhesion. Too high of an etch can cause reduced copper thickness and negative etchback.

Catalyzation

The catalyst is designed to deposit palladium on the wall of the hole. The palladium will then act as an activation site to initiate electroless copper deposition. The catalyst is preceded by a pre-dip that acts as a sacrificial bath. The pre-dip removes oxides, reducing the copper contamination in the catalyst. It also provides common ion drag-in to the catalyst. Important factors in the catalyst are acid normality, chloride normality, stannous chloride concentration, catalyst concentration, dwell, and temperature. Improper catalyzation may cause voids, poor adhesion (peelers), and hole wall pullaway.

Electroless Copper Bath

The basic formulation of electroless copper baths are very similar. They contain five major constituents:

- A source of copper ions, usually copper sulfate or copper chloride
- A reducing agent, usually formaldehyde
- pH adjusters (commonly sodium hydroxide) - used to maintain a pH between 11 and 13
- Chelating agents, used to hold the copper ion in solution
- Proprietary chemicals, including stabilizers, wetting agents, ductility enhancers, and grain refiners

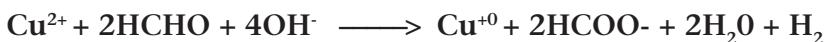
The electroless copper bath is used to deposit a copper coating on the board surface and along the hole wall. It makes the holes conductive to allow further buildup of electrolytic copper plating. The plating rate of the electroless copper bath

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is influenced primarily by concentration of bath components, bath temperature, resin micro-roughening, and palladium adsorption.

Metallization with Electroless Copper for Microvias and High Aspect Ratio Through-holes

Metallizing 4 mil diameter blind vias or smaller and through-hole aspect ratios of 10:1 or greater are a challenge. Critical success factors include ensuring adequate process solution flow in the through-holes, sufficient palladium adsorption on the resin and glass, and minimizing and removing the hydrogen gas bubbles that form as a by-product of the electroless copper deposition. Gas bubbles formed as hydrogen gas are often blamed for small hole voiding, particularly in very small, high aspect ratio vias and blind vias. The electroless deposition reaction below indicates that the generation of H₂ gas is sometimes trapped in the via, inhibiting deposition of copper:



During this reaction, a sufficient amount of hydrogen gas can effectively fill a high-aspect-ratio via. The result can be voiding and thin and/or irregular plating. The equipment set-up, particularly when the electroless plating process is carried out in the vertical mode, must be adapted in order to displace gas bubbles from the via. Inside the holes is where the action is. Process and system design for smaller diameter vias must take into account that chemical material needs to make contact with the interior of the via. However, contact is not enough. There must be ample time, allowing chemical

reactions to take place. This is true whether the reaction is conditioning of the glass fibers or solvent penetration (swelling), etc. Providing a means of replenishing chemical reactants into the via and displacing the material (reactants and by-products) remaining is a challenge for high aspect ratio vias. Expelling the gas bubble before it can cause a void is critical.

In vertical plating, flow characteristics of the solution must be improved. When a PWB is moving back and forth (work bar agitation) through the solution, pressure builds up in front. The velocity of the flow caused by the pressure must be great enough to overcome surface tension of the fluids within the hole. Work bar (through-hole agitation) may not produce sufficient velocity to produce complete material exchange or gas bubble evacuation. As the processing solution enters the hole, a zone of turbulence develops. Laminar flow develops as a consequence and the solution velocity profile is reduced. This reduction in velocity can prohibit not only the displacement of the gas bubble, but can also limit the exchange of material (chemistry and reaction by-products) from the hole walls.

When transitioning from a hole diameter of 0.6 mm (24 mils) to 0.25 mm (10 mils), the amount of flow volume drops significantly, yet substantial surface area of the hole wall remains to be treated, even with the smaller diameter vias. Solution transfer in vertical systems is difficult. The flow in through-holes is pressure driven. It is not uncommon for small-hole voiding problems to be addressed by multiple passes through the electroless copper plating line. From a cost and productivity standpoint, this is undesirable. There have been several process refinements implemented to address this problem:

- Vibration systems for the racks
- Special rack design to aid solution drainage
- Angling of the panels to help gas bubbles dislodge
- Ultrasonic agitation in process solutions including desmear and electroless pre-dip
- Surface tension monitoring of process solutions

There are other techniques that are responsible for incremental improvements in the elimination of small-hole voiding. Certainly, ensuring that all process solutions related to the MHC process are optimized is a critical success factor. Other data suggest that lowering the surface tension in the various process solutions, particularly the alkaline permanganate and the electroless copper deposition solutions, will minimize the incidence of small-hole voiding. Reduction in surface tension is accomplished through the addition of surfactants into the process solution.

Horizontal Electroless Copper Processing and Direct Metallization/ System Enhancements

Horizontal processing for desmear and metallization of through-hole and blind via PWBs is not new to the industry. Direct metallization (discussed below) is well-established as a preferred means of making holes conductive. Electroless copper is a somewhat more involved undertaking, but nonetheless, is operational in many fabrication sites worldwide. With this approach, which is similar to several of the direct metallization systems described below, solutions from the various process chemistries are circulated from the sump of the process solution to the various chambers. The chambers are outfitted with either flood bars or spray tubes.



FIGURE 3: Horizontal conveyorized metallization process

Flood bars are preferred for most of the processing chambers, however spray mode is preferred for rinsing by some process providers. Flood bar or fluid head technology is ideal for pushing process solution through the holes. Improved wetting of the holes is necessary to ensure sufficient contact of the process chemistry to the hole wall. This forced flooding not only brings the chemical reactants to the vias, but also assists in removing the by-products of the reactions. The horizontal positioning of the panels helps the materials make contact with the wall of the hole, as well.

With this approach, the PWB is transported horizontally through each metallization process chamber (Figure 3). In certain chambers, such as the cleaner/conditioner, ultrasonic transducers are located to aid in solution movement. Process solutions are forced through the flood bars under high pressure. As the panel is transported through the chamber, a flood of solution is formed. Figures 4 (a) and 4 (b) show the action of the cleaner/conditioner module in a graphite direct metallization process. The forced flooding action is enhanced by the pressure buildup from the flood heads. This means that



FIGURE 4 (A): Details of solution in the horizontal conveyorized metallization process

more material can be exchanged through the vias per unit time compared to conventional vertical processing. “Tsunami” flood system from Hoellmueller GmbH is one such flood system to dislodge air bubbles and assure wetting of blind vias. Tsunami tube/rollers alternate top and bottom positions to cause “push” and “pull” through the holes. Schmid GmbH has a similar system to assure laminar flow using roll based fluid-jets.

It is highly recommended that ultrasonic agitation be used for horizontal processing, regardless of whether conventional electroless copper or the graphite-based direct metallization processes is employed. Ultrasonic technology has proven to enhance hole wall wettability for permanganate solvent conditioning (swelling), which is critical to shortening the process times in horizontal processes. Ultrasonics are very effective for cleaning and conditioning of the vias immediately prior to making the vias conductive. Ultrasonics enable the improved wettability of the glass fibers while removing loosely held debris that can cause voids. Ultrasonic technology, if



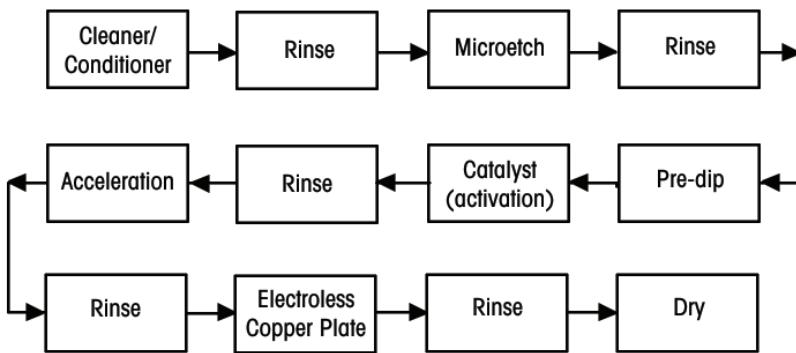
FIGURE 4 (B): Details of solution in the horizontal conveyorized metallization process

designed properly, reduces processing time. The transducers produce vibrations in the process solution. And, depending on the frequency of the vibrations, zones of compression and decompression of the solution are formed. This causes the formation of very small air bubbles or cavities. This is the process of cavitation. As the bubbles compress, a significant amount of energy is released in the immediate vicinity of the release which will permit high energy flows directly on the PWB as it passes over the area, enhancing the contact of the cleaner/conditioner with the hole wall.

In order to achieve the same quality with horizontal processing, there may be modifications in the chemistry due to reduced dwell time and the extensive contact of the chemistry with the holes. Dwell times must be shortened in order to make the equipment process system both cost-effective and

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manageable. Standard electroless copper processing requires more process steps than most direct metallization systems. The steps for electroless copper are outlined below:



There are some electroless copper plating systems that are self-accelerating. In other words, after the PWB is treated with the catalyst and rinsed, the board will move directly to the electroless copper plating solution. The actual accelerating (the removal of some of the tin surrounding the palladium) takes place here, enabling the electroless copper deposition process.

Direct Metallization - Overview of Processes

The direct metallization process for through-hole and microvia metallization involves alternative means with which to effect a copper deposit in the via. These various processes enable the direct electrodeposition of copper without the means of the conventional electroless copper department. These alternatives, in particular, are applicable to horizontal processing, although vertical systems can also be used. These processes typically involve the deposition of a conductive coating, such as palladium, conductive polymer, graphite, or carbon black. This step is followed by the electrolytic copper deposition, eliminating the actual electroless copper step.

Carbon-based Direct Metallization Processes

Carbon-based Processes

There are two acceptable methods for enabling the electrodeposition of copper on non-conductive surfaces using carbon particles. One process is based on carbon black, an amorphous material of approximately 1,000 angstroms in diameter. The other is based on a highly crystalline form of synthetic graphite. The graphite particles are highly ordered and are approximately 10,000 angstroms in diameter. The crystalline graphite conducts electricity anisotropically, as opposed to carbon black which is isotropic. This affects the resistivity of the coated surface. It has been shown that the anisotropic graphite coating is of lower resistance than the carbon black coating. Both types of carbon-based direct metallization systems are used widely by the bare board printed wiring industry.

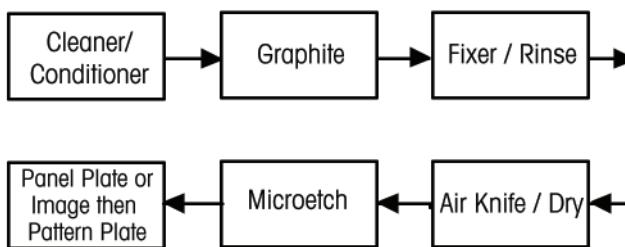
Graphite-based Process

The graphite process uses a stable dispersion of graphite particles to coat the surface of a printed wiring board substrate. A conditioner solution creates a positive charge on the resin and glass surfaces. The conditioned surface is then able to react with the negatively charged graphite particles, causing a flocculation of the graphite particles out of the solution and onto the surfaces of the printed wiring board. The reaction of the graphite particle with the conditioner results in a cross-linking of the binder molecule (which surrounds the graphite particles) with the active hydrogen group on the conditioner. This reaction provides a stable continuous film of graphite on the resin and glass. The excess graphite that is not reacted to

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the conditioner must be removed before the drying step takes place. Generally, an air knife positioned after the application of the graphite dispersion, is sufficient to remove the excess material. However, as aspect ratios have significantly increased and diameters of blind vias have decreased, it is possible that some excess material may be left on the interconnects and capture pads. The acid-based fixer solution is designed to remove the excess graphite by neutralizing the functional group on the binder, which results in a precipitation. The precipitate is then rinsed away by a spray rinse prior to drying.

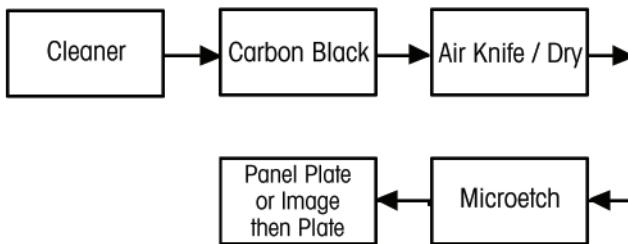
Graphite Process Flow



Carbon Black-based Process

The carbon black system is similar to the graphite-based process but with a few exceptions. From a process standpoint, the carbon black system does not have a fixer step as an option, and often requires a second pass through the carbon black solution in order to achieve sufficient conductivity. The carbon black dispersion is dried and then subjected to the microetch in order to remove the carbon from the metallic surfaces. However, as technology improvements have been advanced, there are newer single-pass carbon black systems on the market.

Carbon Black Process Flow

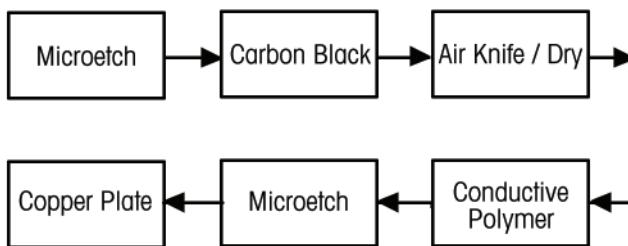


Conductive Polymer

The carbon black process is dependent on the formation of an organic conductive layer on the resin and/or glass surfaces. The process can be operated in either a horizontal or vertical mode. The processing sequence is as follows: after-drilling, solvent, permanganate solution, rinse sequence, catalyst, fixation, and dry.

A critical aspect of this process is that the by-product of the permanganate reaction (with the resin) is not neutralized. The manganese dioxide that remains on the resinous surfaces and on the glass will act as an oxidizing agent. Basically, the catalyst contains a solution of a monomer, such as pyrol, or a thiophene derivative. Sufficient formation of the manganese dioxide film is critical to forming a conductive polymer film of sufficient conductivity to enable the electrodeposition of copper. In the catalyst step, the board is wetted with a solution containing the monomer. In the fixation step, the acid in the solution immediately starts a reaction known as oxidative polymerization. The manganese dioxide serves as the oxidizer for the monomer in the presence of the acid. The result of this sequence is a conductive polymer film that is directly electroplated with copper.

Conductive Polymer Process Flow



Critical Process Considerations When Using Direct Metallization

Fabricators must recognize that certain processes prior to metallization will impact overall quality. Direct metallization is less forgiving when drill quality in the via is extremely poor. This is typically noted when the via has deep drill gouges and wedge voids. Drill gouges that are greater than 1.5 mils deep are problematic. Nailheading (where the flare-out of the copper is greater than two times the actual thickness of the original copper foil) may lead to small plating voids. The primary cause of voids is the removal of the thinned out copper at the edge of the nail heads. The copper is removed by the microetch prior to electroplating of copper. The action of the microetch in the process of removing the thin portion of the copper interconnect creates a void by removing the conductive material.

Copper plating folds are another concern with direct metallization systems. While plating folds are most often caused by poor drilling (especially with torn out glass bundles) conventional electroless copper systems tend to show less of this problem. The theory behind this observation is that certain direct metallization systems (DM) do not readily coat glass fibers as effectively as electroless copper. As a result, the conductivity in the area of the torn-out or rough glass is

somewhat less with DM processes. In addition to excellent via formation control (if glass reinforced resin materials are used), the engineer must optimize the electrolytic copper system for optimal throwing power and leveling.

Palladium-based Process

Palladium-based direct metallization processes use dispersed palladium particles to make non-conductive surfaces conductive. In general, the palladium particles are stabilized either by tin or by an organic polymer. In both processes, the catalytic particles are adsorbed directly onto the non-conductive surfaces, creating a layer sufficiently conductive to be directly plated with copper. There are six typical steps for the palladium-based process:

- Cleaner/Condition
- Microetch
- Predip
- Conductor
- Accelerator
- Post-dip

Note: Rinses have been omitted from the process steps for simplicity purposes.

The organic palladium process uses a water soluble polymer to form a protective colloid around the palladium, preventing it from agglomerating while in solution. The cleaner/conditioner prepares the hole wall to receive the catalyst. Once the palladium is deposited on the hole wall, the accelerator will remove the organic polymer, rendering the palladium active. The organic palladium process can be successfully operated in conveyorized or non-conveyorized modes.

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Tin-palladium processes use tin to stabilize the palladium colloid. After the tin-palladium colloid is adsorbed onto the surface, the tin is stripped away. There are two variations of the tin-palladium process in commercial use. Each process differs in the way it makes the palladium particles more conductive. One process employs a copper-containing accelerator that, in the process of removing the tin, allows copper to deposit on the palladium particles, which aids in making the palladium more conductive.

Semi-Additive Process (SAP)

To achieve the density requirements necessary for sub 2- mil lines and spaces, PWB fabricators resort to semi-additive processing or modified semi-additive processing. In the following tables the various process steps are outlined. As shown, there are different versions of semi-additive processes. The plating thicknesses listed are, of course, only estimates because actual numbers depend on the uniformity of the copper base (in Processes B-D), the throwing power of plating processes, and the etch uniformity of the etching step.

The semi-additive Process A, outlined in the table below, allows the formation of the finest circuitry but requires excellent process control. It appears to be the process of choice for very fine lines in Japan. The modified process sequence of Process B is more robust but cannot deliver the very fine circuitry that Process A is capable of. Process B is widely used in Taiwan. The variations outlined as Process C and Process D are less common.

A less popular variation (Process C) starts with thinned base copper but omits the panel plate strike. Pattern plating height needs to be higher than in the semi-additive process

Semi-additive Process (Process A)

Step	Copper Thickness
1. High-density inner-layer core (prepared by T & E, all subtractive processing, 40-50 µm L/S)	9 µm base Cu & 10 µm panel plated Cu (total about 18-20 µm)
2. Apply dielectric layer over core	
3. Form microvias with laser- or photo-process	
4. Electroless Cu (very thin; tightly controlled)	Add 2-3 µm Cu to dielectric surface and blind via
5. Apply resist (pattern plate resist pattern), expose, develop. Resist does not conform to the via because via diameter is only 50-75 µm, therefore resist can be cleanly developed. Via depth: 40-50 µm.	
6. Electroplate up to 20 µm Cu on surface, about 17 µm in via	Cu thickness on surface (plated area): 22-23 µm. Cu thickness in via: about 19-20 µm
7. Resist strip	
8. Flush etch for differential etching	Remaining Cu height about 19 µm on surface. Cu in via: about 16-18 µm
9. Repeat steps from Step 2 for multilayer buildup	

(about 25 µm vs 20 µm) to retain about 15 µm of copper in the hole after differential etch without tin etch resist. If a tin etch resist is used in this process pattern plating height may be reduced to 20 µm (Process D).

Modified Semi-additive Process (Process B)

Step	Copper Thickness
1. High-density inner-layer core	
2. Apply resin coated foil	Cu foil thickness 1/2 oz (17 µm). Cheaper and easier to handle than 1/4 oz Cu. Now 1/3 oz (11 µm) becoming popular because of availability, cost, and relative ease of handling.
3. Reduce Cu thickness (etching)	Remaining Cu thickness 0.2-0.3 mil (5-7.5 µm)
4. E-less Cu	Add 0.5µm Cu; total thickness: 5.5-8 µm on surface, 0.5 µm in hole
5. Panel plate (occasionally: no panel plate, in which case the process resembles the Japanese process)	Add 5-7.5 µm panel plated Cu.; total Cu thickness: about 13 µm on surface, about 7 µm in hole
6. Microetch	Remove 1-2 µm Remaining: about 11-12 µm on surface, about 5 µm in hole
7. Apply resist, expose, develop	
8. Electroplate	Add about 20 µm on surface, add about 15 µm in hole. Total Cu thickness: about 32 µm on surface, about 20 µm in hole
9. Apply tin metal etch resist.	
10. Strip	
11. Etch	Etch: Cu protected by metal etch resist. Surface Cu remains at 32 µm, in hole about 20 µm

Modified Semi-additive Process (Process C)

Step	Copper Thickness
1. Reduce base copper to 6 µm	Surface Cu: 6 µm
2. Electroless Cu (0.5 µm)	Surface Cu: 6.5 µm. Cu in hole: 0.5 µm
3. Pattern plate 25 µm on surface, about 22 µm in hole	Surface Cu (plated area): 31.5 µm. Cu in hole: 22.5 µm
4. Strip resist, differential etch	Surface Cu: 24-25 µm. Cu in hole: 15-16 µm

Modified Semi-additive Process (Process D)

Step	Copper Thickness
1. Reduce base copper to 6 µm	Surface Cu: 6 µm
2. Electroless Cu (0.5 µm)	Surface Cu: 6.5 µm. Cu in hole: 0.5 µm
3. Pattern plate 20 µm on surface, about 15 µm in hole	Surface Cu (plated area): 26.5 µm. Cu in hole: 15.5 µm
4. Apply tin etch resist	
5. Strip resist, differential etch	Surface Cu: 26.5 µm. Cu in hole: 15.5 µm

Details of surface prep for films and liquid resins

Processes A and B require that the metallization be performed on a dielectric surface. There is no base copper involved. Therefore it is critical that the dielectric material be sufficiently micro-roughened in order to achieve adhesion of the plated copper to the dielectric material. These materials are from a variety of sources. One of the most popular is a dry

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film dielectric supplied by Ajinomoto. Other materials include liquid thermal cured resins. The desmear process for these materials must ensure a sufficient topography in order to achieve proper adhesion of the subsequent electroless copper deposit. The adhesion is measured as *peel* or *bonding* strength.

SEMs and Figures on H-type and V-type Equipment with Peel Strengths

Figure 5 is an SEM of the surface resin before and desmear and roughening process. This surface has insufficient topography to provide adequate peel strength for electroless copper adhesion.

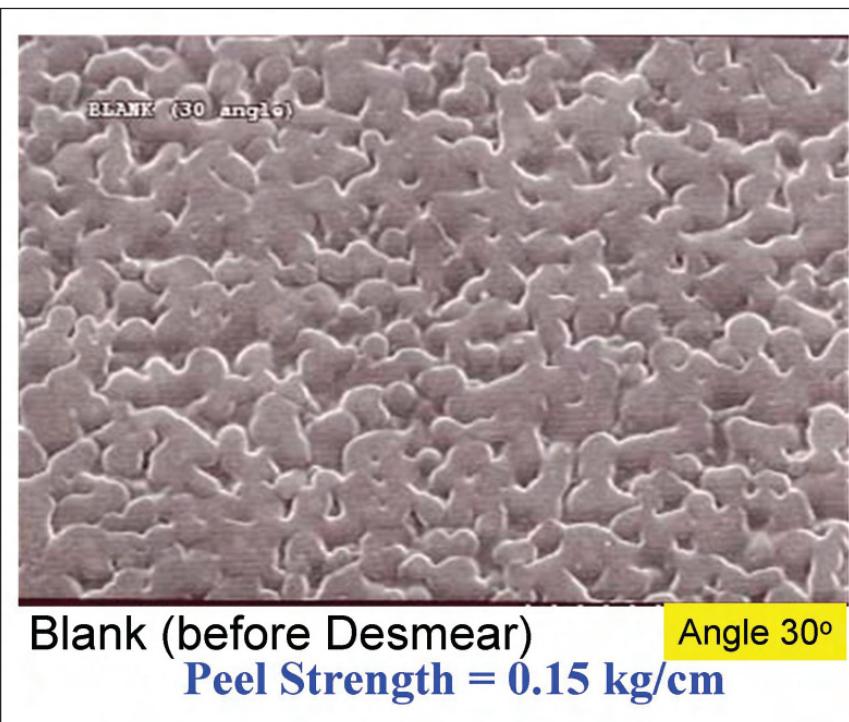


FIGURE 5: This is a view of resin dielectric before the desmear process. Electroless copper would peel from this type of finish.

Horizontal Desmear on Resin Material

Horizontal versus Vertical Desmear for Semi-additive (SAP) Process:

- H-Type equipment is used.
- Surface roughness and topography of the buildup layer resin is not only made by chemical effects, but also by mechanical effects such as ultrasonic effect, spray effect, and so on (Figure 6).
- There is a uniformity issue due to equipment.
- Different type equipment results in different surface roughness and topography.
- V-Type Equipment is used.
- Surface roughness and topography of the buildup layer resin is only made by chemical effects (Figure 7).
- Good uniformity is achieved.

Electroless Copper for SAP

Electroless copper for SAP must have such characteristics as uniform thickness of the film deposited in BVH, good adhesion between copper foil and plated film of copper at the bottom of BVH, good adhesion between dielectric resin and plated film of ELC, etc. It is very likely that BVH diameter

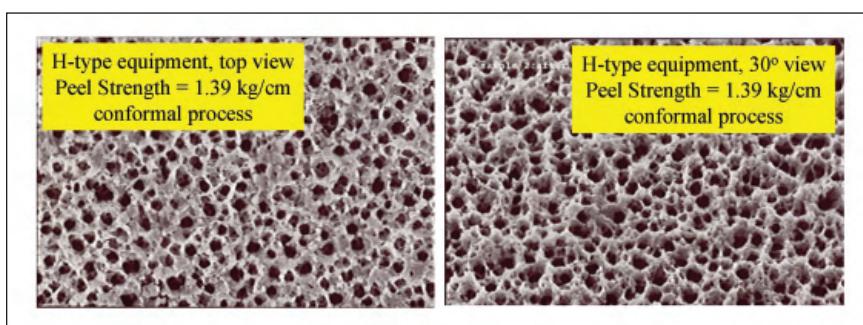


FIGURE 6: This is a view of resin dielectric after the horizontal desmear process. Electroless copper is well anchored.

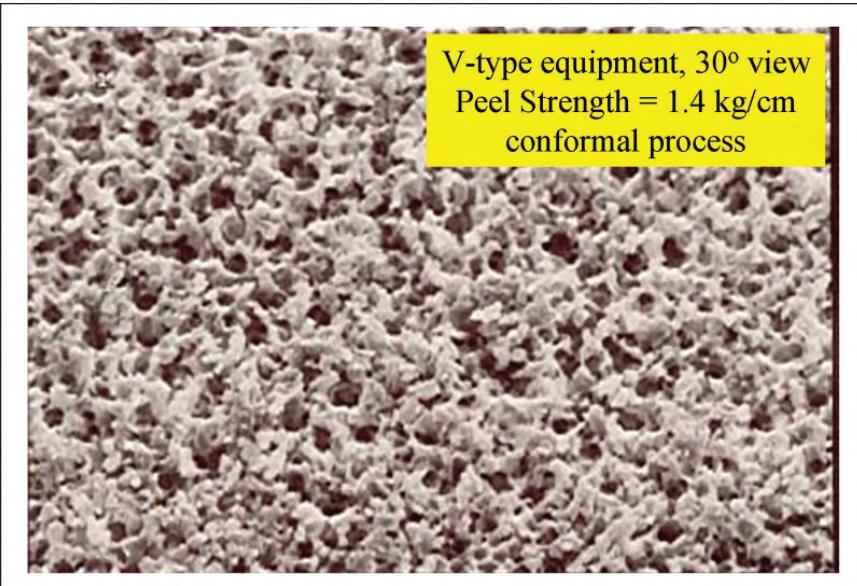


FIGURE 7: Vertical desmear

and L/S of SAP buildup boards will be further reduced with diameters of no more than 40 μm and L/S of no more than 25 μm being commonplace. To cope with reduction of L/S, smaller and more ductile (and less stressed) copper deposits are required. Copper plating thicknesses that were in the range of 1.5 μm to 2.0 μm in the past trend toward 0.5 ~ 1.0 μm these days, but the characteristics of uniform deposition into small-diameter BVH and of electrical conductivity for copper electroplating of patterns must be secured. Moreover, trends for adaptation to reduction of L/S such as reduction of filler diameter, elimination of filler, smoothing of surface, etc., are also seen as critical success factors.

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Fine-Line Imaging and Etching

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The focus of this chapter is on image transfer processes, including stripping and etching fine-lines, registration, equipment, and materials for fine-line image transfer.

The Image Transfer Process

The imaging process for HDI requires much tighter controls than conventional print and etch applications. The need for finer lines and spaces, smaller annular rings on the vias, and plated through-holes requires more vigilance with respect to phototool quality, imaging parameters, and surface preparation.

The Conventional Image Transfer Process

Today, contact printing is the standard mode of imaging PWBs. Two major problem sources in contact printing, especially with fine-line boards, are radiation in non-exposure areas and the imaging of dirt, defects, or other unwanted features. Projection imaging and laser direct imaging have the potential to prevent some of these problems, but these technologies are not yet widely used. In this chapter, additional information is presented on operating practices, equipment, and material selection for all of the image transfer processes.

Fine-line Resist Adhesion

Fine-line, and by default, very dense circuit features require an integrated approach to imaging. In this sense, the fabricator takes special care to ensure that the resist is adherent to the copper surface. While resist lamination parameters and their relative importance on adhesion are addressed in the following topic, one must also consider that the surface preparation of the copper foil surface goes hand-in-hand with the lamination step. The ideal copper surface (for optimum resist adhesion) requires special processes and tools.

There are numerous changes in surface preparation and substrate construction partially driven by cost pressures and the need to establish the capability to handle and clean thin cores (e.g. 2-3 mil dielectric with 1/2 ounce copper) without damage or distortion. New analytical tools such as OSEE, ISS, SIMS, SERA, and Interferometry, as well as traditional measurement techniques, are available to characterize new cleaning processes and surfaces.[1]

Aluminum Oxide Jet or Brush Cleaning

Al_2O_3 jet scrubbing was first introduced by Ishii Hyoki (Japan). AOX is a domestic US supplier of comparable equipment and IS (Parma, Italy) supplies Al_2O_3 brush scrubbers.

The jet scrubbing process is not to be confused with pumice cleaning. Compared to pumice, there are some important differences. Aluminum oxide does not disintegrate to fines as rapidly as pumice does. As judged by the particle size distribution, aluminum oxide lasts much longer and results in less maintenance, downtime, and sludge disposal. On the other hand, aluminum oxide particles *wear round*. Over time the particles become smoother, *peening* the copper and

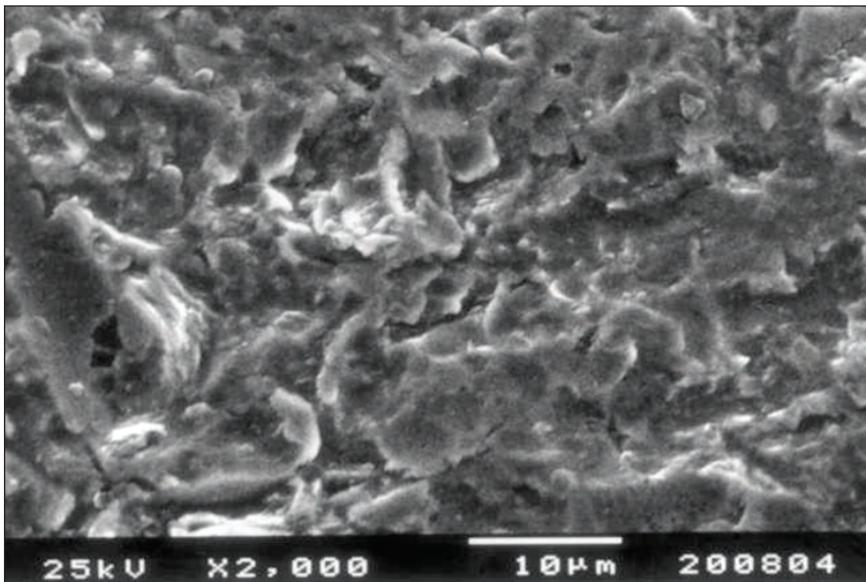


FIGURE 1: Surface structure after processing with aluminum oxide cleaning

creating a smoother surface which is detrimental for dry film adhesion. Aluminum oxide needs to be replaced before fine particle buildup suggests that replacement is due. Suppliers of aluminum oxide equipment don't seem to have hard and fast rules based on data when it comes to aluminum oxide replenishment frequencies.

The grade and particle size of aluminum oxide are also variables with evolving specifications. According to an IS study, brushing of aluminum oxide gives a rougher, more preferred, surface than jetting.[2] Data also indicate that jetting distorts (elongates) thin copper foil more than brushing. If jet pressure is lowered to counteract this phenomenon, there may be a problem with insufficient surface roughening due to reduced particle impact.

To avoid dimensional distortion of thin cores, mechanical surface preparation methods are being avoided in favor of *chemical cleaning* (microetch or acid clean/microetch

combinations) or *no-clean* options. Single step chemical cleaners (e.g., Alpha Metals' HP5195 or Ingopur) are being offered. Reverse current cleaning methods are being introduced to remove chromate with a minimum of copper while maintaining the dimensional stability of thin cores. No-clean options include double-treat copper, reverse-treated foils, CAC™ foils, and combinations thereof. On the other hand, we are noticing the growing popularity of aluminum oxide jet and brush scrubbing on thicker boards, apparently driven by cost and productivity considerations.[1]

Low profile, fine-grain foils and non-woven dielectric constructions such as aramid laminates offer the promise of better conformation of thin resists to planar foil surfaces.

Let us look at some of these developments in more detail:

Non-standard Copper Foil Types

Double-Treated (DT) Copper[1]

There has been an increase in the use of double-treated foil in the US and Japan. Furukawa Circuit Foil is reporting increased use of its 18-micron DT foil on inner-layers. Several reasons have been cited:

- The price differential between double-treat and standard foil appears to be offset by true value-in-use, at least in certain applications.
- DT does not require the application of a multilayer bonder and avoids the potential of pink ring defects. On very thin foils, the conversion of a substantial amount of copper to copper oxide for use as a bonder may not be acceptable.
- No pre-lamination surface preparation is required, which results in cost savings. More importantly,

as inner-layer cores become very thin, brush or pumice scrubbing can cause unacceptable distortion.

Double-treat surfaces are not necessarily compatible with wet lamination. We have studied the use of surfactants in wet lamination of double-treat boards and have identified promising wetting candidates. Other concerns include difficult AOI recognition in the reflectance mode, a tendency for etch retardation with alkaline etchants, scuffing of the surface, staining, or lock-on with extended hold times for some photoresists.[1]

Reverse-Treated Foils (RTF)

Polyclad has introduced a laminate with Drum Side Treated Foil (DSTF) and Mitsui is offering MLS foil. As ED foil is formed, it typically has a smooth side facing the drum and a rough side facing the copper solution. In the RTF process, the foil receives a zinc treatment only on the smooth side which is laminated to the dielectric. The rough, non-treated side faces the dry film. Because of its surface roughness, no mechanical or chemical roughening step is needed for dry film adhesion. However, since the roughness ($R_a > 0.3$ microns) exceeds optimal topography, best results are achieved with wet lamination. The omission of an acid cleaning step for tarnish and chromate removal is somewhat controversial. Careful yield studies are needed to define the trade-offs, and multilayer oxide bonder formation may suffer as a result.

Fine Grain, Low Profile Foil and Non-Woven Dielectrics

The need for impedance control and fine-line etching has accelerated the development of *low profile copper foils* which

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often have a fine grain structure. *Low profile* refers to the smoother, more uniform topography of the copper foil side facing the dielectric. Suppliers of fine grain foils are Mitsui Mining & Smelting (SQ-VLP), Gould (JTCAM), and CircuitFoils VLP (very low profile). SQ-VLP is reported to yield a better etch factor. DT-VLP is MM&S' fine grain inner-layer foil. Fine grain foils seem to yield a more uniform, high surface area, planar topography, especially when combined with non-woven dielectric constructions. This development will accommodate surface mount needs and provide good conformation of thin resists for high resolution and etch uniformity. Reported yield improvements do not appear to be directly related to the grain structure, but more to the overall quality of the laminate and shorter etcher residence times.

Very Thin Foils

For *ultra thin copper* (UTC) for MCMs and BGAs, minimal copper removal during surface preparation is an issue. MM&S' 12-micron foil is an example of such a thin foil. Atotech's Electrochemical Cleaning System may be a viable solution for removing chromate conversion coatings with only minimal copper removal. The use of 12-micron double-treat foil without surface preparation would be a viable alternative, which Gould can supply in developmental quantities. To facilitate the handling of very thin foil, eliminate surface cleaning, and avoid contamination of the copper surface with epoxy spots, thin foils are offered as more rigid sandwiches of copper/aluminum/copper or copper/aluminum.

Photoresist Lamination

In hot roll lamination, heat is applied to the rolls and transferred through the polyester film coversheet and the resist

to the resist/copper interface to achieve good resist to copper conformation and adhesion. The rolls are heated by a variety of methods, including cartridge heaters and surface heaters applied to the inner surface of a hollow roll. Other laminators use an external IR source to heat the outer surface of the roll. Pressure is by far a more important variable than temperature when it comes to achieving conformation of the resist, but temperature plays an important role in reducing the resist viscosity for improved flow.[3]

A more direct heat application is sometimes used to supplement roll heating. The board is preheated just prior to lamination. Preheat units may use hot rolls, such as the triple hot rolls of the Hakuto Mach 610i, or they may employ IR heat. Since these preheat units add cost to the lamination process in the form of capital expense, clean room floor space requirement, electricity consumption while heating the unit, and more electricity consumption to keep the clean room at a comfortable temperature, one needs to carefully assess if such equipment is justified. One reason to use preheat units might be that the PWB fabricator is processing thick multilayers, such as back planes that form a bigger heat sink than thin inner-layers. To achieve the desired resist/copper interface temperature at an acceptable lamination speed, the supplemental heat from the preheat unit may be justified.

It is also interesting to note that resist suppliers whose dry film resists tend to have a high viscosity, are more likely to recommend a preheat unit. Low viscosity dry films may have viscosities in the range of 20 to 60 m poise (milli poise = poise/1,000) whereas high viscosity resists that benefit more from preheating may have viscosities in the range of 130 to 160 m poise.[3]

The actual temperature at the resist/copper interface

depends on the contact time of the resist with the heat source, the temperature of the heat source, the heat transfer coefficients of the materials between the heat source and the resist/copper interface, and the thermal mass and temperature of the board. The contact time, in turn, is a function of the lamination speed and of the roll/film *footprint* in the lamination roll nip. The lamination speed is set by the hot roll rpm and the diameter of the rolls, while the footprint, the width of the hot roll/board contact zone in the nip, is determined by the durometer and thickness of the roll covering, the diameter of the roll, and the roll pressure.[3]

The board exit temperature guidelines should depend on the board type. As a rule of thumb, aim for 60-70°C (140-160°F) for thin inner-layer boards. If the inner-layer boards feature drum-side-treated copper foil which has a rougher outer surface than standard foils and is therefore more difficult to conform to, aim for a higher exit temperature, e.g. 70-75°C (160-170°F). We measured the average roughness of standard copper foil and found it to be in the range of $R_a = 0.1\text{--}0.2$ microns whereas reverse-treated foil gave an R_a of 0.38 microns.[3] For thicker outer-layer boards aim at 45-55°C (110-130°F). If the outer-layer resist will be subjected to a harsh nickel/gold plating cycle, go for the upper end of the outer-layer range, i.e., 50-55°C (120-130°F). Note that suppliers of harder, higher viscosity resists may suggest higher board exit temperatures than provided here.[4]

The actual resist/copper interface temperature is indirectly monitored and controlled. Controlled variables are the hot roll temperature, the lamination speed, and, where applicable, the preheat unit temperature. The board exit temperature, the temperature of the laminated board just as it leaves the roll nip, is often used as an indicator of the desired resist/copper interface

temperature during lamination. Since there are additional variables affecting board exit temperature, such as board thermal mass, room temperature, conveyor speed, and the time to reach the temperature sensor, those variables need to be considered and controlled to make the reading meaningful.[4]

The low end of the recommended board exit temperature range has been established empirically and is the result of extensive yield studies and DOE tests to find the lowest temperature that still guarantees good resist conformation and adhesion. The high end of the recommended board exit temperature range is established empirically and is the highest *safe* temperature at which one can run without getting into trouble, notably avoiding resist wrinkling.

Printing

Printing - The Fundamentals

Contact printing involves the transfer of an image template (phototool), consisting of transparent and opaque areas, into a polymerized resist pattern by radiating a certain dose of UV-light through the transparent areas of the phototool to initiate photopolymerization. Polymerization is reasonably well limited to the exposed resist areas if two conditions are met: inhibitor levels in the resist are sufficiently high to provide a threshold against unwanted polymerization in non-exposure areas due to scattered radiation; and polymerization kinetics are fast compared to the speed of inhibitor migration.

This exposure process works well if the light is collimated (parallel), if it is perpendicular to the exposure plane (no declination angle), and if the light is not scattered. However, these conditions cannot be perfectly met and some radiation reaches non-exposure areas where it causes some degree of

polymerization. This unintended partial exposure can be minimized by bringing the phototool in very close contact with the resist and by eliminating sources of scatter along the light path.[7]

Digital Circuitizing Techniques

There are several alternatives to contact (or proximity) printing of printed wiring boards. Laser direct imaging (LDI) comes to mind. However, there are also other viable alternatives. Some are commercial, some were developmental or commercial but faded away, and others are at the conceptual or lab development stage. LDI itself offers a variety of technical approaches in terms of laser source, working wavelength, and imager architecture as shown in Table 1.[10]

Laser Direct Imaging (LDI)

The increasing demand for miniaturization and better functionality of electronic components and devices has a significant effect on the requirements facing the PCB industry. PCB manufacturers are driving to produce high-density HDI boards while significantly reducing cost and implementation time. The interconnection complexity of the PCB is still growing, and today is calling for 50/50 μm or 25/25 μm technology. Imaging of HDI boards poses a rapidly increasing challenge for PCB manufacturers due to line width and space having smaller and tighter registration requirements. Existing technologies are unable to offer an acceptable solution. Currently, LDI technology is considered an answer for these challenges. LDI is a process of imaging circuitry pattern directly on the PCB without the use of a phototool. The exposure of the photo-sensitive resist is carried out using a laser beam that is scanned across the photoresist surface

and switched on and off by means of a computer control system according to the electrical circuit pattern. Usually the laser used in LDI generates the UV line, which is suitable for commonly available photoresists.

With imaging times now getting close to those of Contact Printing, the use of LDI offers manufacturers an alternative. With the current LDI systems using high-speed dry film resists, productivity rates of 60 double-sided panels per hour are not unreasonable. The system can now be viewed as a production tool and the benefits given serious thought.[8,10] Cost reduction in the manufacture of LDI can be the result of many things:

- **Cost savings from the elimination of phototools and the cost of their manufacture and storage**
- **Savings in the cost of manufacture of the printed circuit by minimizing the time to set up between prints and jobs**
- **Elimination of the need to produce first-offs for the proving of the set-up and phototools**
- **Opportunity for a flexible manufacturing route and printing varied panels to meet the demands of production without impact on throughput**
- **Opportunity to reduce manufacturing lead times by allowing manufacture to start as soon as the data leaves the engineering department**

Additional benefits are gained from potential quality improvements:

- **Elimination of film-related and *printed-in* defects**
- **Possibility of eliminating or reducing temperature and humidity effects on the product and minimize the ingress of dust due to the controlled environment within the laser imaging systems[11]**

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TABLE 1:

Imaging Technology	Examples	Features
Laser Direct Imaging	UV (Argon) Laser Examples: DP100™ (Orbotech, Israel), Automa-Tech (France)	Flat bed, single sided exposure Use of standard UV sensitive photoresists or high-speed UV photoresist for high throughput
	Solid State UV Laser Example: Gemini (Mania-Barco)	Vertical, double-sided exposure Automatic load/unload Development seized 1.Q. 2002.
	Solid State UV Laser Example: DP-100SLTM (Orbotech, Israel)	Throughput: up to 120 prints/hour Resolution: 6.3 µm or 5 µm Radiation source: solid state laser (355 nm), requiring only 3-4 kW, compared to about 60 kW for the argon ion laser. Maximum substrate size: 660x812 mm Maximum image area: 609x812 mm Minimum line and spacing: 50 µm (6.3 µm resolution), 40 µm (5µm resolution) Positioning accuracy: +/-12 µm Side-to-side registration: 24 µm
	Paragon™ 6600i (Orbotech, Israel).	355 nm diode solid state laser Suitable for prototyping
	Paragon™-8000 (Orbotech, Israel)	355 nm diode solid state laser; 4 W 24-inch wide-scan lens Up to 160 prints/hour Resolution: 4000 or 8000 dpi For 8000 dpi model: minimum feature size = 1 mil; positioning accuracy = +/- 0.5 mil; side-to-side registration = 1 mil; maximum exposure area = 24x32 inches Dynamic scaling
	Paragon™ 8800 (Orbotech, Israel)	355 nm diode solid state laser; 8 W For HDI mass production
	Paragon™ 9000 (Orbotech, Israel)	Resolution capability: 20 µm L/S
	Paragon™ Ultra 80 (Orbotech, Israel)	For BGA and CSP substrates Resolution of 40 µm pitch (18 µm lines, 22 µm spaces), address resolution 1 µm, 8 W solid state laser, 30 panels (500x400 mm) per hour, registration accuracy +/-5 µm, side-to-side registration 10 µm
	Visible (green) Laser. Example: DI-2000 (now ORC, formerly Asahi Kogogaku)	Use of special dry film or liquid sensitive in the visible range

TABLE 1 — CONTINUED

Imaging Technology	Examples	Features
	Thermal Laser Example: Diamond 2028F (CREO)	External drum construction for imaging of flex material and inner-layers Use of IR sensitive, positive liquid Effort discontinued 1.Q. 2002.
	Visible (405nm) laser DI-Impact by ORC (formerly Pentax)	DMD (Digital Micromirror Device) High pressure mercury light source Double-sided exposure Automated loading/unloading Minimum feature size: 15 µm L&S Position accuracy (repeatability): +/- 7.5 µm Side-to-side registration: +/- 10 microns Exposure time: 35 sec for 340x510 mm
	Hitachi Via Mechanics (DE-series),	DE-H, DE-S, and DE-F series differentiate in their resolution capabilities Imagers use a diode laser, operate at 405 nm, and make use of Texas Instrument's DMD™ micromirror array model XGA DE-H has highest resolution, capable of producing 10 micron lines and spaces Overlapping pixels have an addressability (center to center spacing) of 1.2 microns DE-S capable of doing 20-micron L/S (2.6-micron addressability) DE-F does 40-micron L/S
	Mercurex (Dainippon Screen)	Min. L/S: 20 µm Combination of a SLM (spatial light modulator) and high pressure mercury lamp (350-420 nm) SLMs are translucent or reflective liquid crystal microdisplays
	INPREX semiconductor laser by Fuji Film (350-410nm)	Multiple beam splitting for high exposure speed Ten second exposure for 510x600 mm panel Minimum feature size: 15 microns (for highest resolution model)
	Miva 2808 xDI (MIVA Technologies GmbH, Germany)	Direct imager, using Texas Instrument's DMD™ Micromirror array and xenon flash lamp light source Radiation output mostly in visible range, sharp drop off in UV Fairly high output in IR (IR filter needed to avoid heat buildup)

Fine-Line Imaging and Etching

In addition to the cost savings benefits and the potential yield improvements, there are a number of technical advantages:

- Improved resolution with the small laser spot size
- Sub 50 um features are easily resolved
- Improved registration is also achieved by the use of CCD

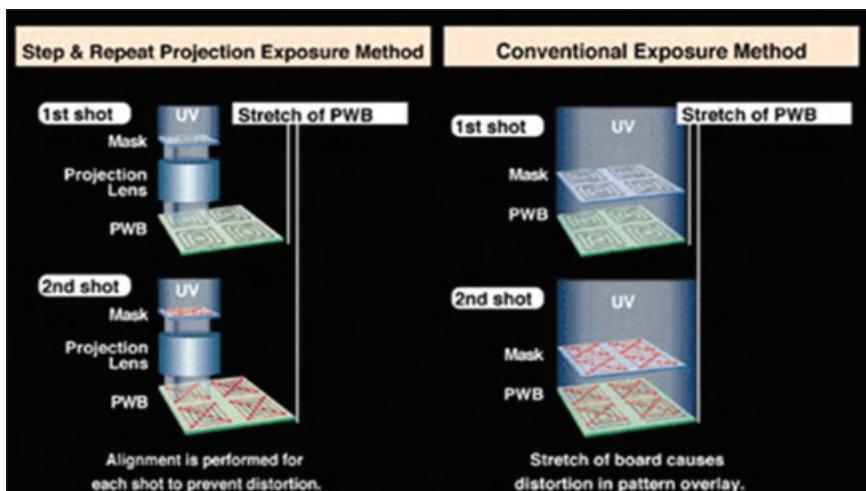
Improvements in registration are achieved by eliminating the phototool, which has always given rise to issues, especially as the tools move anisotropically with temperature and humidity changes.[11] Coupled with the tendency for contact printers to run hot, the phototool makes the alignment of film and panel an ongoing challenge. With LDI, however, it is possible to use a CCD camera system and target fiducials on the panel to align the print image and panel. It is also possible to use these target positions to calculate any panel or drilling movement and scale the rasterized print image so that we improve the registration and achieve the best fit.

Projection Imaging

A second, very broad category is projection imaging (Table 2), the best known of which is the step-and-repeat technique that has become the standard technology in IC imaging but is just beginning to penetrate the world of PWBS, particularly organic packaging substrates.[5] In projection imaging one can distinguish between conventional photomasks that have a fixed image, (e.g., chromium on glass and *dynamic photomasks*) which feature a pixel array that can be addressed electronically with CAD data and which change as the stepper moves into the next position.[11]

TABLE 2:

Imaging Technology	Examples	Features
Projection Imaging	Step & Repeat Exposure Systems from ADTEC (SPR600), USHIO (UX-5038SM), Tamarack	High intensity projection lens systems Typical field size 4x4 to 6x6 inch exposure area Chrome-on-glass photomask steps with light head Image size compensation by focus adjustment
	Laser Projection Imaging. Example: Anvik System	1:1 Projection, XeF excimer laser source (UV 351-353 nm range) Mask and panel mounted on a planar scanning stage Large mask areas can be scanned seamlessly in a serpentine pattern with a large cross-section laser beam (about 16 cm ²) Suitable for flex and rigid substrates
	Projection with dynamic masks such as micro-mirrors or digital light matrix screens. Examples: MDI (Mercury Direct Imager) by Mivatec, Ball Semiconductor's Direct Imaging System, and CUVIS (computerized ultraviolet imaging system) by FSL Germany	Dynamic digital photomask (e.g. DMD™, Digital Micromirror Device™), UV light source, image size reduction in projection Ball Semiconductor (www.ballsemi.com), Allen, TX, uses TI's. DMD™, Digital Micromirror Device™ UV light source, image size reduction in projection Digital light matrix screen (mask) and light source scan over a stationary substrate

**FIGURE 2: Projection imaging step and repeat**

Contact Printing

Manual exposure units (photoprinters) use vacuum frames of various constructions in the process known as contact printing. The phototools, in close contact with the photoresist-covered board help to avoid off-contact exposure. To create the vacuum, air is evacuated through one or more vacuum ports. Air channels to these ports need to stay open to avoid entrapping air without an escape route. These open channels are formed by an arrangement of bleeder veins, bleeder strips, shims, or spacers.[7] Vacuum frames may come with a top cover made of polyester foil (e.g. Mylar®) and a glass bottom, or glass-to-glass fixtures, either hinged or frame mounted. Shims or spacers in glass-to-glass fixtures not only form the bleeder channels, but also protect the glass from breaking if there is a large difference between the panel and the glass size.[7]

Vacuum frame Mylar® coversheets may be four to seven mils thick smooth or textured sheets. One would expect textured sheets to allow faster air escape, but smooth sheets are preferred. With textured sheets Newton's Rings are not formed. These rainbow colored features are interference patterns that indicate close proximity of two surfaces, a tell-tale sign of good vacuum draw-down, if and when these features become stationary. Another disadvantage of textured coversheets is the refraction of light by the textured pattern that is detrimental to resolution. The texture also makes it harder to see and remove dirt from the cover.

The proper positioning of bleeder strips provides an air path from the perimeter of the phototool/panel package to the vacuum port. Without such air channels, a gas seal forms prematurely around the panel leaving trapped air between the phototool and the panel, as illustrated in Figure 3.

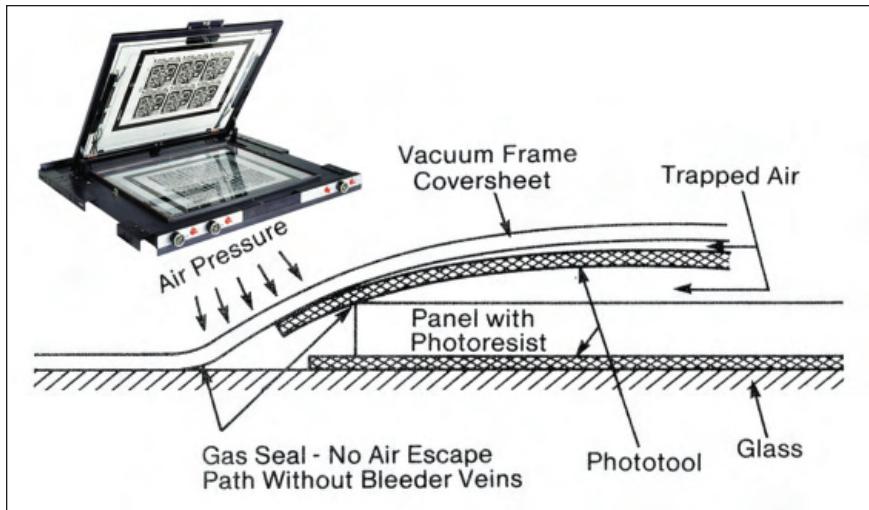


FIGURE 3: Vacuum frame

Registration-Image to Hole

Several strategies are being employed in PWB fabrication to assure that metallized vias and drilled through-holes align with circuit patterns and solder connections.

Use of a Diazo Phototool

The UV-opaque areas of a diazo phototool are transparent to most of the visible spectrum which means an operator can visually align pads on the phototool with holes on the resist covered outer-layers or the soldermask covered board. The phototool is then taped to the board in the correct position and the procedure is repeated on the backside of the board. The transparent, dark amber-colored pattern on the yellowish background of the phototool, which the operator uses for alignment, is formed when a diazonium salt is exposed to ammonia vapors and links to couplers that are present in the phototool. When the phototool is plotted, the diazonium salt decomposes in areas that are exposed to UV-radiation, leaving

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only the yellow background coloration. The dark amber color that is formed during development is actually not the UV-opaque material that gives the phototool its functionality. Another diazo “dye” that absorbs in the UV region is developed in the non-exposure areas, invisible to the eye.[5,6]

Automatic Exposure Machines

Automatic exposure machines typically make use of CCD cameras to achieve pattern-to-hole alignment. Safe light shines from the back side through the photoresist-covered registration/tooling holes and is detected by the CCD cameras at the front side. The board position is then adjusted to be in the right position when the phototool makes contact.[7]

Hinged Glass Frame Fixtures

Hinged glass frame fixtures use pins to position the board. Phototools with pre-punched registration holes are placed on the top and bottom surfaces of the board, using the same pins. Vacuum is then drawn between the phototools and the supporting glass frames through vacuum groove channels in the glass. After the phototools are positioned securely on the glass by the vacuum, the phototools are taped in the correct position.[7]

Post-Etch Punch

A popular method for image-to-hole registration for inner-layers involves the use of a post-etch punch. Front and back side circuitry need to be only side-to-side (or front-to-back) registered. After lamination, exposure, development, and etch, the board enters the post-etch punch, often in line with the DES line. CCD cameras then locate copper fiducials and adjust the position of the board before punching tooling holes. This

method has the added advantage that any punching debris is formed after the dirt sensitive image transfer is complete.[7]

Image Scaling in LDI

One very useful feature of LDI is its ability to scale the digital image for the best fit to a panel with a drilled hole pattern that has shifted due to dimensional changes of the board during processing. The LDI calculates the best fit of the image and adjusts dimensions before plotting. Some LDI systems can scale locally for best fit to sub-segments of the board area. Scaling in x and y directions can be independent, i.e., anisotropic.[8]

Step and Repeat Imagers

Step and repeat imagers can adjust the focus of the image within certain limits to adjust one-up exposure dimensions on *multiple-up* images for best fit, using CCD cameras to locate reference holes.[9]

Use of X-ray Drills

To align the NC drill pattern for plated through-holes to buried inner-layer features, an X-ray drill can be used. The X-rays *see* the inner-layer features and then drill reference holes which serve as tooling holes for positioning the board in the NC drill for drilling the through-holes.[9]

Self-Aligning Via-to-Circuit Technologies

There are several techniques, none of which are mainstream PWB manufacturing technologies yet, that are inherently hole-to-circuit self-aligning such as the formation of circuit grooves and via holes in a single laser ablation step. Metallization follows, using the dual-damascene technology

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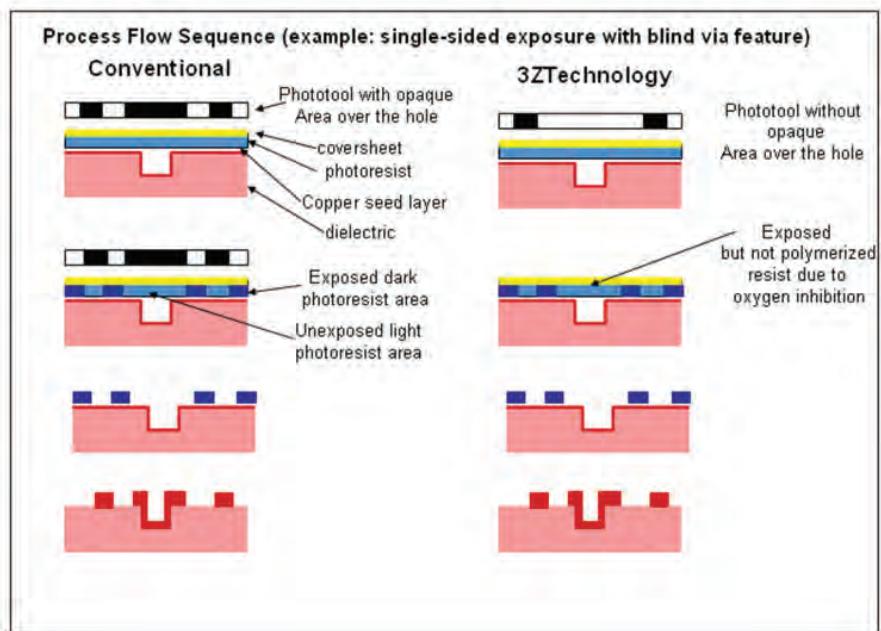


FIGURE 4: Comparison of 3Z Exposure with Conventional Exposure

that is practiced in IC fabrication. Another example is imprint technology, where a tool plate embosses circuit grooves and holes into a suitable dielectric substrate.[9]

Innalab's 3Z Technology

Innalab's 3Z Technology is a developed resist pattern for the annular ring that is always perfectly self-aligned with the hole, even if the line is not. Figure 4 shows that for a given degree of line misregistration, 3Z Technology may result in no hole break-out, whereas conventional exposure may cause hole break-out.[4]

3Z Technology takes advantage of the trapped oxygen in the hole by using suitable photoresists of a certain photosensitivity with which one can expose features on the board surface without polymerizing the resist tent over the hole and the adjacent halo of resist around the hole.

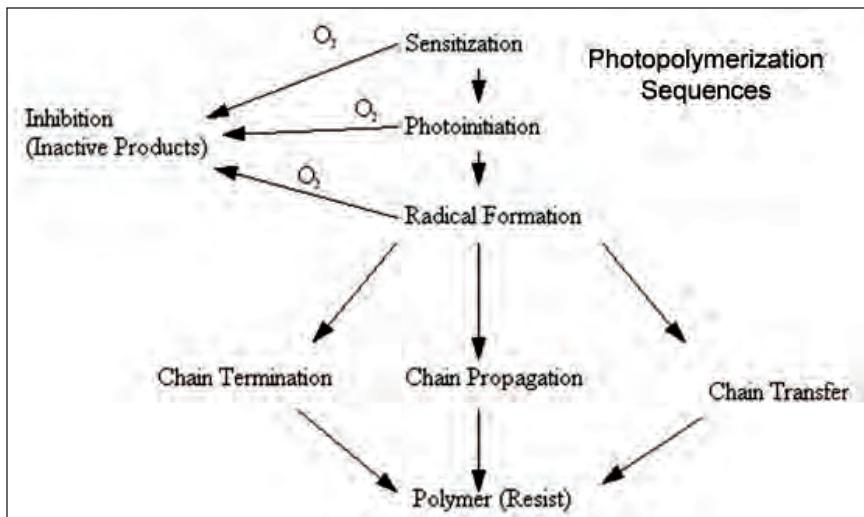


FIGURE 5: Photopolymerization sequences

Since oxygen is a potent radical scavenger, it will first react with the radicals formed by UV exposure. This will continue until all the oxygen that is dissolved in the resist is consumed. Only then will the chain polymerization begin. The polyester coversheet that covers the resist during exposure serves as a barrier to oxygen replenishment during exposure. Without it, higher exposure doses will be required to overcome the additional inhibition due to the re-supply of fresh oxygen. A special situation exists when the photoresist tents over a through-hole or blind via. The air trapped in the hole provides additional oxygen which can replenish the oxygen that is dissolved in the resist, given enough time for diffusion. This diffusion has been recognized as an issue in the tent and etch process, so that a slightly higher exposure dose in tent and etch applications is recommended than for other applications to assure good polymerization of the tent. If one waits some time to allow the oxygen in the hole to diffuse into the resist, then a second exposure will complete the polymerization of the surface features without causing polymerization of the

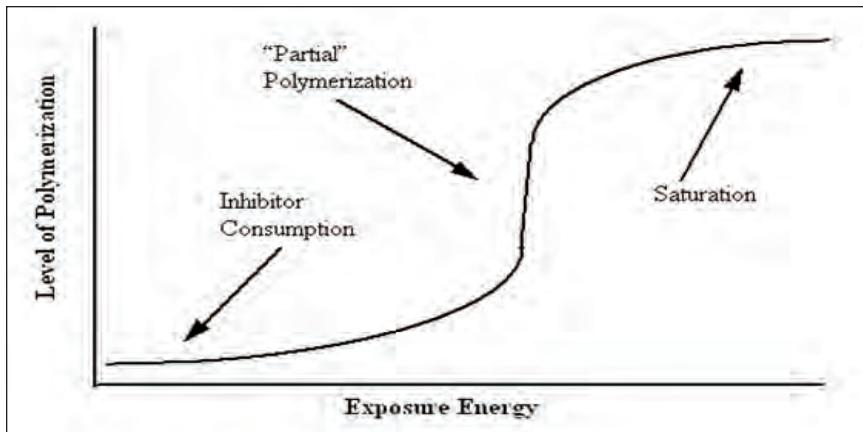


FIGURE 6: Exposure energy compared to level of polymerization

resist tent over the hole and around the hole rim. Figure 5 shows this photopolymerization process sequence taking advantage of the different levels of polymerization that different exposure energy provides (as seen in Figure 6). A 3Z phototool for pattern plate will have lines, but the lines don't end in pads because no pads are needed to block the light over and around the hole.

Another application is the formation of very high-aspect-ratio resist structures through double- or triple-lamination, exposure, and development of photoresist over a first exposed and developed resist layer. The developed openings in the first resist layer provide the trapped oxygen to inhibit polymerization of the second and third layers in the same position.

Developing

Developer Control Parameters

The control of photoresist aqueous development is of great importance to achieving high yields, resolution, good circuit line definition (side wall), and line uniformity. A myriad of critical equipment features and process variables, some

of them linked and interdependent, can confuse operators and engineers. Concentrations, water quality, temperature, spray pressure, break point (wash-off point), time in the developer, resist loading, pH, post-development rinsing, and drying parameters are just a few of these features and process variables.[12]

While all of these parameters can be important, and some are relatively easy to control within the required limits (e.g., temperature and time), the maintenance of the pertinent chemical concentrations within a desired range, both in batch and feed-and-bleed mode, is of particular interest and has spawned different schools of thought.

Control of Developer Chemistry

In principle, the control of the chemical composition of the developer solution is critical because aqueous, processable photoresists can overdevelop in aggressive chemistry. A chemical degradation of the exposed resist (in negative working formulations) or aqueous resists can underdevelop (incomplete cleaning of the channels) if the development chemistry is too diluted or depleted. The completion of development means the removal of unexposed resist traces from the bottom of the developed channel, which occurs in the end section of the development chamber after the bulk of the unexposed resist has been removed in the front section and the *breakpoint* has been reached. Too much time in the developer after the breakpoint can cause an attack on the exposed resist.

The developer chemistry is typically about 0.8-1.0% sodium (or potassium) carbonate. Fresh carbonate, when dissolved in water, is in equilibrium with small amounts of sodium bicarbonate. As carbonate gets consumed during

Fine-Line Imaging and Etching

the development process by solubilizing and neutralizing carboxylic acid groups in the resist formulation, the reaction products, bicarbonate, and resist component salts (*resist loading*), build up. The pH drops, the development rate slows down, and development may be less clean (danger of scum on the board). Resist suppliers may offer response curves for resist loading vs. pH, time-to-clean vs. temperature, time-to-clean vs. resist loading, and preferred conditions for breakpoint, loading, carbonate concentration, and temperature.

The initial make-up concentration of the developer solution from solid carbonate and water is typically verified by an acid/base titration or conductivity measurement. Should working strength solution be generated from carbonate concentrate solution (typically 25-45% potassium carbonate) and water, which is very popular in feed-and-bleed operations, the same analyses can be applied.

For batch replenishment, the chemical composition of the developer is normally not monitored directly. The developer conveyor speed may be adjusted initially to give a breakpoint at the low end of the recommended range, followed by monitoring the breakpoint during operation, and dumping the developer once the upper end of the recommended range has been reached. Empirically, this control experience can then be translated into a predetermined resist throughput per volume developer solution, and a panel count can signal the need for a dump.

In feed-and-bleed systems, one has to first choose how to mix concentrated carbonate and water to maintain a working strength solution in the developer. It is preferable to feed working strength solution to the developer sump. This is normally achieved by premixing concentrate and water in a large feed tank and monitoring the concentration. Another workable approach is to intermittently pump concentrate and

water into properly proportioned small overflow containers which empty simultaneously and feed the developer by gravity flow. A portion of the water used in the feed can be developer rinse water to conserve water. The bleed is normally controlled by a high level overflow. Carbonate concentrates especially tailored for developers are commercially available. They may feature foam control additives, complexing agents to maintain the cleanliness of pH probes and equipment, cleaners, and small additions of caustic.

Next, a chicken and egg argument arises with regard to the chemical parameter that truly matters in development and should trigger and cut off the feed. One practical approach is to select a desired pH (e.g., pH 10.6) to be maintained in the developer. This pH value can be dialed into a pH controlled feed-and-bleed system. The system may be set up to trigger feed at pH 10.5 and cut it off at pH 10.7. Developer conveyor speed is then set to maintain the recommended breakpoint while feeding working strength (e.g., one percent) carbonate replenishment. The resist supplier may have a recommended *resist loading* range and provide a resist-specific response curve of pH instead of loading. In all likelihood, such loading recommendations will be met if working strength solution is fed and the pH is maintained as described above. There may also be a recommendation with regard to the percentage of *active carbonate* to be present in the developer. This can be checked by an occasional acid/base titration of the developer solution to the bicarbonate and carbonic acid endpoints to verify the concentrations of *active* carbonate, *total carbonate*, and, by calculation, spent bicarbonate. There is some interference in these analyses of loaded solutions from the presence of resist and/or antifoam, but that has not kept generations of laboratory technicians from titrating anyway.

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The import topic of process and analytical controls will be addressed in future revisions of this Handbook.

Developer Sprays

The optimization of spray action in conveyorized modules has been approached in a variety of equipment designs, all having merits and shortcomings. There are fixed spray nozzle arrays, spray bar arrays that oscillate back and forth transverse to the machine direction, and stationary bars that pivot along a fixed axis, resulting in a spray pattern with oscillating angles.

The objective is to achieve a uniform spray pattern across the surface of the board and to have high-impact spray action assist the developer chemistry with good replenishment fluid dynamics and mechanical erosion of the resist. High surface velocity of the developer solution is desirable to reduce the thickness of the stationary liquid boundary layer. Spray pressure and nozzle type selection largely determine the spray impact (Figure 7). Direct fan nozzles yield the highest impact, cone nozzles give lower impact, and deflector fan

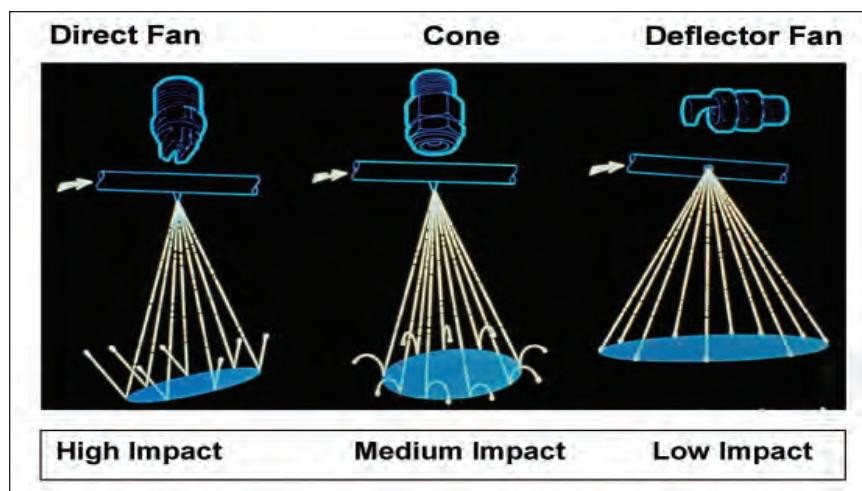


FIGURE 7: Spray impact of different types of spray nozzles.

nozzles provide even less. While direct fan nozzles appear to be the obvious choice, there are trade-offs that can favor the selection of cone nozzles. Fan nozzles have a very narrow spray footprint and it takes a large array of carefully arranged nozzles to achieve good coverage. Cone nozzles generate a larger spray footprint. They are spaced for maximum coverage and minimal overlap. Spray overlap is undesirable because spray impacts cancel each other out.

Interference with spray action and shadowing effects need to be minimized. Plastic clip-on guides for thin laminate are staggered. Guide wires are oscillated to randomize their shadowing effect. Conveyor wheels are staggered and solid wheels are replaced with wheels that feature thin spokes. Resist features that form during the development process can also shadow sprays and interfere with clean, complete development, which led to the concept of sprays that impact at different angles. This can be achieved by mounting nozzles at various angles or by angular oscillation of spray bars. Paying close attention to the developing chemistry and its control and providing the recommended process equipment design are critical to achieving clean blind vias and straight side walls of the through-holes.

Etching

The chemical and mechanical aspects of etching take on a renewed meaning with HDI. The fabricator must ensure excellent adhesion of the resist to the surface of the copper so that the action of the etching chemistry does not cause excessive undercut or lead to removal or lifting of the resist. There are several problem areas associated with etching, some interrelated, some independent (Figure 8). Benefit from process remedies may be seen in one or more of these problem areas. These problem areas will each be addressed.[13]

Etching Problems

- Undesirable lateral etching (etch undercut)
- Top to bottom variation due to puddling effect
- Etch variation due to obstructions in the way of the spray pattern
- Etch rate differences due to circuit pattern lay-out

FIGURE 8: Typical etching problems

Etch Undercut

Addressing etch undercut first (Figure 9), one must recognize that the wet etching of PWBs is isotropic. In other words, one sees a lateral attack on the copper traces as well as an attack on the copper in the z-axis direction. Even when equipment and process adjustments are implemented, the lateral undercut is not completely eliminated.

LP-Chemie's Impulse Process creates spray pulses of etchant droplets with high vertical impingement force onto the copper surface that easily penetrate an etch inhibitor

Reducing undesirable lateral etching (etch undercut)

- Use of pulsed sprays and banking agent (Impulse Process, L. P. Chemie, Germany)
- Use of low free acid normality etch chemistry
- Use of ferric chloride etchant (vs alkali or cupric chloride etch)
- Going to more favorable etch channel aspect ratio, by
 - Using thinner copper
 - Using thinner (liquid) resist in print & etch
 - Moving away from the traditional pannel plate/tent & etch process that requires thick resist to
 - Electrophoretically deposited (ED) resist (e.g. Nippon Paint, Kansai Paint), or
 - Laser ablatable immersion tin resist (Siemens), or
 - Laser ablatable (non-photodefinable) organic resist coating (Atotech)

FIGURE 9: Approaches to reduce lateral etching

layer (banking agent) at the bottom of the etch channel, but leave the inhibitor layer on the etch channel sidewalls largely undisturbed.[14] This technique results in enhanced downward etching (i.e., a more favorable etch factor) and higher etch speed. The pulses are generated mechanically by the rapid rotation of a coaxial pipe sleeve with slots around the spray bar. This process is combined with Pill's top side suction bar approach that addresses top-to-bottom etch non-uniformity due to puddling.[14]

It has been reported that controlling acid etchants at very low free acid normality improves the etch factor.[13] The findings are in line with earlier work that showed that by using NaCl instead of HCl as a source of chloride ions in acid etchers results in an improved etch factor by complexing copper salts and keeping them from precipitating.

Different etch chemistries result in slightly different etch factors. Alkaline etching typically yields a less favorable etch factor than acid etchant. Some studies show a better etch factor with ferric chloride than with cupric chloride, but results are not always conclusive.

Etch Non-Uniformity Across a Surface and Top-to-Bottom Non-Uniformity

The *puddling effect* is one cause of etch non-uniformity and poor etch factor. Most of the top-to-bottom etch variation stems from the puddling effect which causes a slower etch rate near the center of the top side of the panel due to liquid buildup, which is not the case on the bottom side because of the faster liquid run-off facilitated by gravity.

The use of suction bars, alternating with spray bars on the top side of the etcher as a means of removing the puddle by mimicking gravity on the panel top side has improved etch

Compensation for Puddling with Alternating Spray Bars and Suction Bars (Extraction System) (Source: Pill)

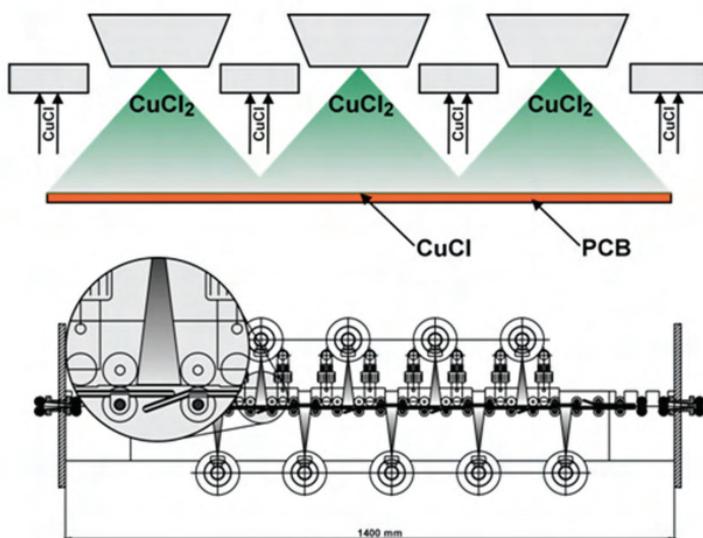


FIGURE 10: Illustration of an etchant extraction system (Courtesy of Pill)

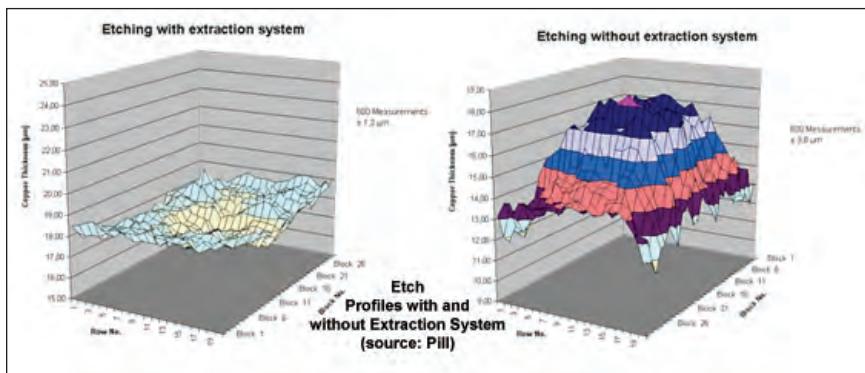


FIGURE 11: Effect of extraction system on etch uniformity (Courtesy of Pill)

uniformity significantly (Figures 10 and 11). [4]

Another technique to reduce the puddle effect is the use of a spray pressure profile, whereby the etchant stream enters the spray bar at the center, which is where the center of the board

Reducing etch variation due to obstructions to spray patterns (shadowing) by randomizing or avoiding obstructions

- use of “conveyorless” transport (edge grip, no wheels)
- use of spoked wheel (vs solid wheels)
- use of staggered wheel array
- randomize thin panel support guides (e.g. oscillating guy wires)

FIGURE 12: Reducing etch variation due to shadowing

travels. The spray pressure is highest at the center, tapering off at both ends of the spray bar. Similar results are achieved by timing the sprays on/off and synchronizing with the board movement in order to deliver more spraying action to the center of the board.

Figure 12 summarizes ways to minimize uneven shadowing of the board surface due to obstructions to the spray which can lead to uneven etching. Modern conveyorized etchers apply these techniques.[14]

Etch Spray Obstructions

Since conveyor wheels obstruct sprays, *conveyorless* transport systems have become popular. They are not really conveyorless, but most, or all of the wheels have either been replaced by traveling ledges supporting rigid boards on both edges, or edge grips for thinner panels that hold the panel under slight tension. If conveyor wheels are being used, they are spoked wheels, as opposed to solid wheels, which minimize the obstruction. The wheels are staggered to randomize the obstruction. If the etcher features support guides for thin panel transport, the guides are also randomized through the use of oscillating guide wires or other methods.[15]

Etching chemistry

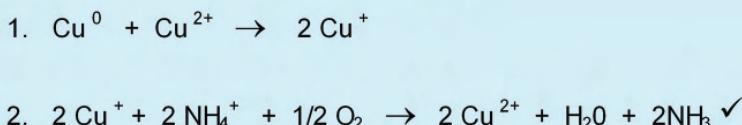
Alkaline Etching

Alkaline cupric chloride etchants are proprietary chemistries with several formulations designed to meet the needs of high productivity and fine-line work. These etchants are the preferred choice when tin or tin/lead plated metals are used as etch resist because they do not readily attack those metals while rapidly etching copper. All aqueous-processable photoresists are attacked to some degree by these etchants, but some can be successfully used with proper controls. Some photoresists have been designed to be more resistant to alkaline etchants. The dominant use of alkaline etchant is for outer-layers, but it is also used for inner-layer and double- and single-sided board manufacture.[16,17]

Basic Chemistry

The basic chemical reaction for alkaline cupric chloride chemistry (Figure 13) is the oxidation of copper metal by cupric ions to form cuprous ions. The equation is the same as

Oxidation/Regeneration Mechanism



Described as Tetramine / Diamine Complex

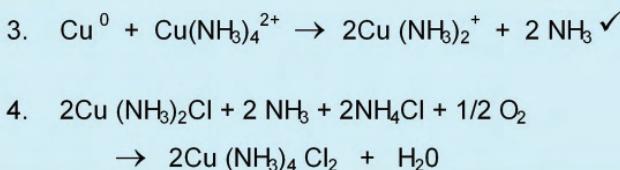


FIGURE 13: Chemistry of alkaline etching

for acid cupric chloride, in that cupric ion is the oxidant that attacks copper metal. However, it is different because it occurs in an alkaline environment in which both cuprous and cupric ions are complexed by ammonia.

An even greater difference is that in alkaline etchants, cuprous ions are rapidly oxidized by oxygen from air, so the oxidant is free. Where the oxygen regeneration reaction was too slow to be anything more than a nuisance for acid etchants, the air oxidation is fast enough to provide all the regeneration needed for alkaline etching. Ammonium chloride and ammonia in the solution are consumed as they complex and solubilize the copper ions formed during the oxidation of the copper metal and oxidation of the cuprous ions, so they must be replenished.

Etchant pH

The pH of the solution is vital to the control of solubility, etch rate, and undercut. The pH also has an important effect on photoresist performance. Lower pH typically favors a lower undercut (higher etch factor) and therefore a lower pH may be used in fine-line work. However, for a given alkaline etch system, the pH must be held above a minimum value (depending on copper concentration) to hold the copper salt in solution.

Higher pH values produce faster etch rates, and lower pH values produce slower etch rates. Therefore, alkaline etchants with high pH values are typically used in high productivity work. High pH is favored for higher copper solubility. High pH produces a larger undercut and can affect the performance of some photoresists, particularly aqueous resists. Some aqueous resists soften, and even strip, as a result of high pH in alkaline etching.

The ammonium hydroxide contained in replenisher solution supplies much of the base needed to maintain an alkaline pH (greater than pH 7.0), but ammonia additions are required to reach the pH ranges recommended.

Ammonia or ammonium hydroxide additions are usually made automatically by a pH-sensing control system. Since ammonium hydroxide contains water, a water loss/addition mass balance is necessary to assure that the added water does not reduce the chloride or copper content below their recommended values, notably with systems that are started daily, but in which panels are not run frequently. Evaporative loss of water also occurs, but its loss is far less than the water gained from ammonium hydroxide additions.

Ammonia gas works very well for pH control, since it contains no water to upset the system equilibrium, but it is more hazardous to use.

Copper Content

Copper concentration affects etch rate and etch factor. With some fine-line alkaline chemistries, higher copper concentration increases the etch rate within the operating range and increases the etch factor. Copper concentration above the recommendation for a given etch system will reduce the etch rate and can lead to sludging of copper salts. Once precipitation occurs, it takes so long to get the salts to re-dissolve that it is better to just dump the etchant and start over with fresh make-up solutions.

Using high copper content systems and operating at the upper limit of a system are favored for high productivity work, whereas low copper content systems at the lower end of recommended copper concentrations are often favored for fine-line work.

Copper content is controlled by monitoring the specific gravity of the solution using a Baumé controller. Since Baumé is also affected by chloride concentration, copper should be analyzed regularly by titration. A thiosulfate titration is often used for this. Replenisher is added to reduce the copper concentration. Should the copper content fall below the recommended range, and other chemicals are within their recommended ranges, the set point of the Baumé controller may be adjusted to obtain the goal copper concentration.

Chloride Content

Chloride addition is necessary for the etching process to proceed since the reaction products, cuprous chloride and cupric chloride, tie up and consume chloride. Unlike in acid cupric chloride etching, excess chloride does not serve the function of complexing and solubilizing the reaction products. Ammonia does the complexing in alkaline etching.

The recommended concentration of chloride is established by the vendor for each chemistry system and must be monitored closely. If the chloride concentration falls and the copper concentration rises, copper salts will sludge out. If the chloride concentration rises excessively, attack on solder or tin resists can occur.

Higher chloride concentration is required for high productivity and lower chloride concentration is often used for fine-line work. Chlorides also act as buffering agents. The principal buffer is ammonium chloride, and ammonium bicarbonate may be present for additional buffering action.

Chlorides are contained in the replenisher solution. Chloride concentration can be analyzed using the silver nitrate titration procedure in most etchant manufacturers' data sheets. Replenisher solution typically does not have exactly

the same chloride concentration as the etching solution. Alkaline etching is a very dynamic chemical system. The rates of water and ammonia evaporative losses, both in the replenisher and main etcher chambers, the amount of etcher use, particularly when ammonium hydroxide is used for pH control, and exhaust ventilation conditions all affect the equilibrium concentration of chloride in the etchant. As a result, the chloride concentration may gradually drift outside its recommended range.

Periodically, a chloride analysis should be performed. If too low, ammonium chloride salt can be added. If chloride drifts too high, and pH is controlled by ammonium hydroxide additions, it may be possible to bring it back into range by increasing ventilation, which will cause more ammonia evaporation, more frequent ammonium hydroxide additions, and a dilution effect from the water contained in ammonium hydroxide. Sometimes, if the pH is sufficiently high, water can be added directly to the solution to dilute chloride, but it should never be attempted unless recommended by the chemistry vendor.

Temperature Effect and Control

Etchant temperature affects the etch rate. A temperature rise of 10°F increases the etch rate by about 15 percent. The upper limit for temperature is usually dictated by the properties of the plastics from which etching equipment is built and seldom exceeds 130°F. Both heating and cooling are used to minimize variations in temperature. Temperature can affect ammonia usage and the control of pH because of the volatility of ammonia. Lower temperatures reduce ammonia losses to equipment exhaust ducts.

Banking Agents

Alkaline etchants sometimes contain proprietary banking agents and stabilizers that are used to influence the etch factor. These additives are present in both make-up chemistry and in replenishment chemistry. The theory is that banking agents reduce undercut by producing a protective film on the copper sidewalls, which reduces lateral attack as the etchant etches downward. However, there is very little published evidence that the effect is significant.

Oxygen Supply/Ventilation

Oxygen in the air is the oxidizer for cuprous ions in alkaline etchants. Equipment exhaust is necessary to provide the necessary air flow through the sprays in the etching chamber and to prevent ammonia fumes from entering the processing area. If there is an insufficient air supply, cuprous ions will not be completely oxidized to cupric ions, which will slow etching and reduce capacity. If the exhaust is too high, ammonia loss will reduce etch rate and copper solubility, possibly causing precipitation. Some alkaline etchers are designed for air sparging to assure a sufficient fresh supply of oxygen. Oxygen may also be introduced in a controlled way in an etchant regeneration loop connected with the etch chamber.[1] The proper balancing of ventilation airflow to exhaust ducts is absolutely critical because, if incorrectly set, ammonia attack can severely damage photoresists.

Conveyor Speed

Conveyor speed is set to obtain the desired residence time for the part and the desired etch result, whether it is conductor width, degree of undercut, a certain impedance value, or another desired attribute.

Determining the breakpoint is one method used to get a starting point for the correct conveyor speed. The breakpoint is that point in the etch chamber where the final bit of copper has just been etched off. It is expressed as a percentage of the total length of the etch chamber. An 80 to 85 percent breakpoint is typical, however, deliberate over-etching may be done at a 75 percent breakpoint. Excessive dwell time in the etcher can be critical for a metal etch resist because increased dwell time intensifies both resist attack and the galvanic cell reaction.[2]

Replenishment

Alkaline etchant replenishment differs from acid etchant replenishment. The cuprous ions generated during the alkaline etch process are oxidized back to cupric ions by the oxygen from air. Unlike the acid process, this is a very rapid oxidation process. Chemical replenishment is necessary to resupply other chemistry that is consumed by the process. Replenishment chemistry is supplied by etchant vendors and consists mostly of ammonium chloride (often referred to as *chloride* in alkaline etch terminology) and ammonium hydroxide. Ammonium bicarbonate is sometimes included as a buffer. The replenishment chemistry is unique for each chemistry system being used and must be matched with the system to maintain stable operation.

To control pH, ammonia additions as ammonia gas or aqueous ammonium hydroxide are automatically made. Because of the water present in ammonium hydroxide, special consideration must be given to its use.

Alkaline etch replenishment is controlled primarily by monitoring the specific gravity of the solution (also known as Baumé). Solution-specific gravity is proportional to the copper

and chloride concentrations. The specific gravity of etchant rises as copper is etched from panels causing a rise in copper concentration and as chloride concentration rises with water and/or ammonia evaporation. Controllers are available that sense the specific gravity or Baumé and automatically add replenisher solution when the density set point is exceeded. The excess volume of etchant created by the addition is simultaneously pumped out by means of a dual-bellows pump; one bellows adds replenisher at the same time as the second bellows removes an equal volume of etchant.

Replenisher (Figure 14) consists of a mixture of ammonium hydroxide, ammonium chloride, and perhaps ammonium bicarbonate and/or proprietary banking agents. Both ammonia and ammonium chloride are consumed during the etching of copper. Automatic replenisher additions, in conjunction with the pH control, keep the chemistry within the standard operating conditions under normal operation. However,

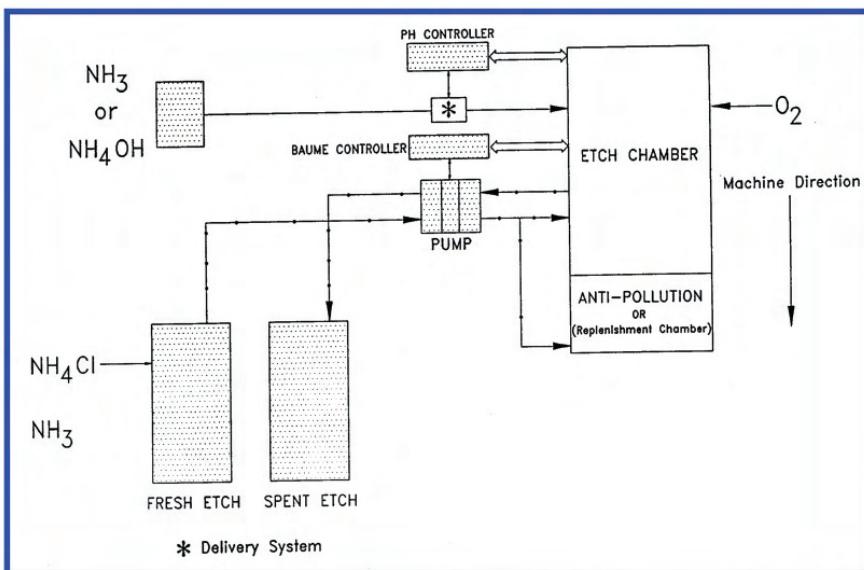


FIGURE 14: Alkaline etcher replenishment system (top view)

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regular analysis of the chemical constituents is necessary to ensure that each is within its specified range.

Replenisher addition methods have received special attention because both ammonia and ammonium chloride form chemical complexes with copper, and also because ammonia attacks aqueous resists.

The first stage rinse in an alkaline etcher is not a water rinse. It is a spray rinse chamber that recirculates replenisher chemistry. For alkaline etchers, replenisher is added to the rinse chamber, where it mixes and then cascades by overflow into the etcher sump. The spray rinse chamber is sometimes referred to as the *environmental control* chamber, based on the notion that its function helps conserve water and brings dragged-out chemicals back into the reaction chamber.

Additions of copper-free replenisher hold the copper level in this section to a minimum.

Under certain conditions, if replenisher is added only to this chamber, a substantial lag can occur between the time the replenisher is added to the replenishment chamber and the time the fresh chemistry overflows into the etcher sump where it is needed, which can cause process instability and variable etch speed. This usually happens only in systems that are used infrequently, where evaporation caused by ventilation often causes the level in the replenishment chamber to drop. In this case, additions must first refill this module before overflow into the etcher sump can occur, which delays delivery of chemistry to where it is needed to increase etch rate.

In such cases, the replenisher addition is sometimes split, sending part directly to the etcher sump and part to the replenisher. However, this practice will degrade performance of the anti-pollution (replenisher) chamber somewhat, because as the copper in this stage rises, more copper is carried into the

final rinse. Because this copper complexes with ammonia, it can complicate rinse water waste treatment.

Another reason to keep copper concentration in the replenishment rinse section low is that, as the level of copper rises, the rinse water begins to etch copper, further complicating matters. The replenisher rinse chamber can sometimes reach a very high pH because ammonia gas from the heated etcher sump can be absorbed from the vapor space by the replenisher recirculation sprays, which can greatly increase chemical attack on aqueous photoresists. The chemical attack can be prevented by properly balancing etcher exhaust ventilation.

Cupric Chloride Etching

Cupric chloride etching is a low cost and consistent technology designed to create fine-line patterns for print and etch and inner-layer details.[18]

Copper metal is oxidized by one cupric ion to produce two cuprous ions:



The Cu^{1+} ion is not soluble in water but it can be made soluble with the help of coordination ions which are ions that surround the Cu^{1+} atom by electrostatic attraction. The chloride ion, Cl^- , is an example of a coordination ion for Cu^{1+} . If one prepares a solution containing Cu^{2+} and Cl^- by dissolving cupric chloride in water, that solution should have the ability to etch copper metal because the Cu^{1+} ions are soluble in the solution, and the reaction can proceed.[1] In reality, the Cu^{1+} ions need a relatively large concentration of Cl^- in order for them to be soluble in water.

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The overall equation during etching is:

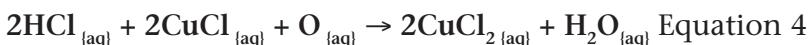


Regeneration

The cupric chloride etchant can be restored or regenerated to its original state by oxidizing the Cu^{1+} ions back to Cu^{2+} by adding an oxidizing agent. Common oxidizing agents used in the industry are *hydrogen peroxide*, *sodium chlorate*, dissolved *chlorine* and dissolved *oxygen*. In this discussion we will only concern ourselves with oxygen regeneration by dissolved air. The disadvantage of air regeneration compared to chemical regeneration is its slow speed due to the difficulty of dissolving sufficient quantities of air into solution. But air regeneration does have the advantage of being freely available and impossible to add in excess. The equation for regeneration by oxygen is:



You can see that H^+ is consumed in the above reaction, and so what better way can we provide hydrogen ions other than from hydrochloric acid? With excess hydrochloric acid in the mix, the chloride balance is always maintained and the solution grows as it consumes four ingredients during its lifetime. These include; copper metal, oxygen (from air), hydrochloric acid, and water. The overall equation during regeneration can be written as:



Parameter	Min	Max	Remarks
Free acid concentration (molarity)	1.0	3.5	HCl fuming increases Etch speed increases*
Specific gravity (g/cm ³)	1.220	1.380	Relatively stable etch rate across range
Temperature (°C)	0	40	HCl fuming increases. Etch speed increases*
Minimum bulk tank volume per board area (liters/cm ²)	0.016	-	Assuming 50% track coverage, double-sided, 36 µ m (one ounce) copper PCB
Maximum monovalent copper ion, Cu ¹⁺ (g/liter)	-	5	Color of drops on white surface should appear bright green to dark olive green Any signs of brown color indicate Cu ¹⁺ too high

* The temperature and acid molarity both contribute to HCl fuming. When the temperature is at the high end of the range, acid molarity should be reduced. When the temperature is at the low end, acid molarity can be increased. These two parameters are best determined through personal experience in your environment.

TABLE 3: Recommended bath operating parameters.

In practice, the concentrations of Cu²⁺, Cu¹⁺, and free acid affect the etching speed. In particular, the Cu¹⁺ ion has a large effect on etch rate. Cu¹⁺ has much lower solubility compared to Cu²⁺. Because it is generated directly at the surface of the copper, where the reaction is taking place, its presence will inhibit etching, therefore the Cu¹⁺ ions must be removed as quickly as possible from the copper surface in order to maximize etch speed. One way of achieving this is to maximize the solubility of Cu¹⁺ so it can quickly diffuse into

the bulk solution. Diffusion of Cu¹⁺ from the copper surface is increased by keeping concentrations in the bulk solution to a minimum.

Operating Parameters

Operating air regenerated cupric chloride etchant requires more attention to operating parameters than commonly used hobby etchants such as ferric chloride or ammonium persulfate. Etch speed will be impaired if bath parameters operate too far out of range. When etching is too slow, the benefits of using cupric chloride may be lost. To prove both the efficiency and cost-effectiveness of cupric chloride, regeneration systems must be utilized.

Etching to Achieve Finer Lines and Spaces

In general, the finest line/space in the market with the subtractive process seems to be around 50/50. There have been studies to determine how much finer line/space could be stretched with the process, using Surface Uniform Etching Process (SUEP) and thin dry film. SUEP had already been introduced as a process for fine-line/space forming. It is a process which reduces the surface copper foil thickness. The 3- to 5-micron copper obtained after SUEP is effective for making fine-lines by the conventional subtractive process consisting of panel plating, tenting, and etching.

The conventional *pattern plating* process, also called the *Plated Solder Stripping* process, has a thick-base copper of 20 microns, and uses plated solder as etching resist for the traces. Such thick-base copper makes traces smaller by etching after removal of the plating resist. Plated solder on traces requires an alkali etchant that has an inferior etching factor for base copper which can causes overhang on traces, which disturbs

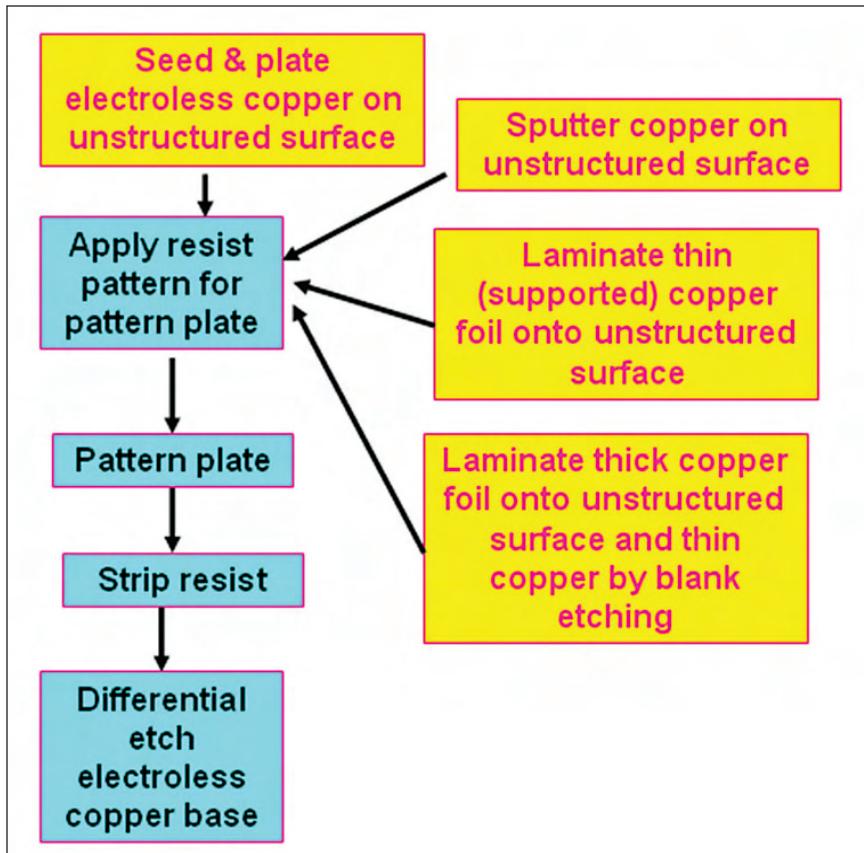


FIGURE 15: Semi-additive methods to reduce undercut and achieve higher circuit density

plating resist stripping. Therefore, the conventional pattern plating process should be improved to make finer lines/spaces. Ideally, a controlled surface etch process (CSE) can be employed to achieve finer lines and spaces for HDI designs. The CSE is a half-etch process which means it starts with one-half or one ounce foil and etches down to 9 microns or less. While this entails an additional etching step, the fabricator is able to reduce costs associated with ultra thin foils and the associated cost of handling such thin foils. The process flow for CSE is shown in Figure 15. The half-etch process is listed along with other semi-additive options.[19]

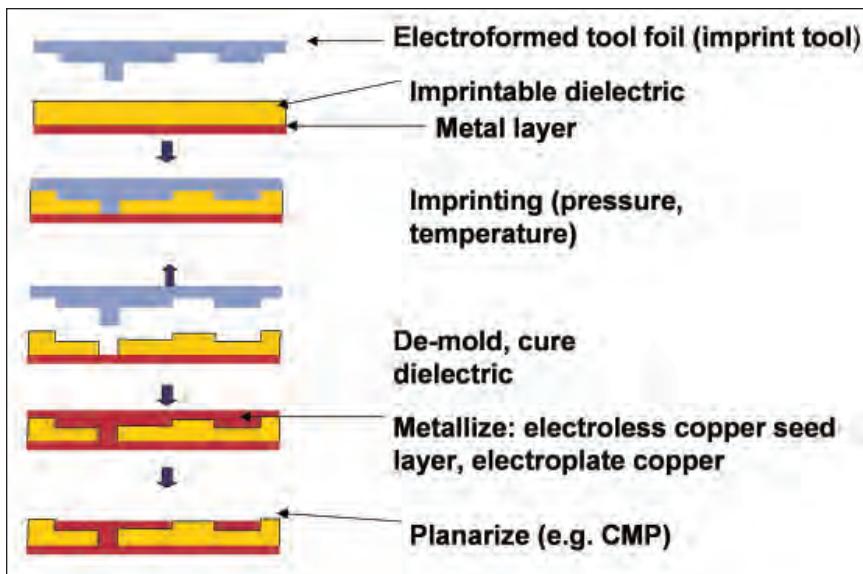


FIGURE 16: Principle of imprint technology (Courtesy of George Gregoire, Dimensional Imprint Technology, Inc.)

Raised vs. Recessed Circuits

There are two basic ways to form recessed copper features, the first of which have several variations on the theme. One concept consists of creating grooves and holes in a dielectric to define the dimensions of conductor traces and vias.

Grooves and holes may be formed by imprint technology (Figure 16), hot embossing, or laser ablation.[21] The other concept consists of forming circuit patterns *off-line* by pattern plating on a conductive layer (Figure 17), which could be a metal seed layer on a non-conductive board or film.[4] An example might be a polyester base sputtered with aluminum. Or the conductive layer could be a stainless steel plate.[5]

It is not clear at this time which of these approaches has the most merit and will eventually emerge as the technology leader, or if an altogether different circuitization method will prevail. It is, however, clear that a good number of

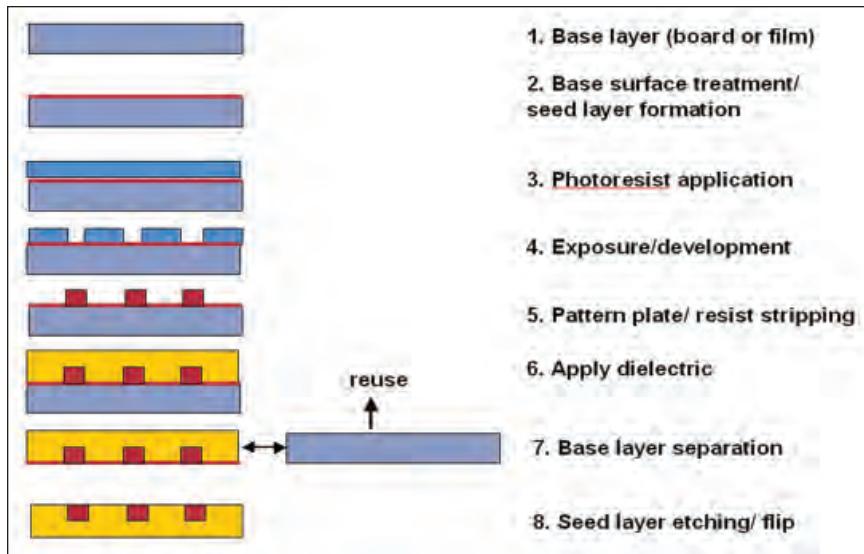


FIGURE 17: Illustration of a circuit transfer process (Courtesy of Ryoichi Watanabe, Samsung Electro Mechanics)[1]

progressive fabricators and OEMs are investigating these technologies.[20]

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Footnotes

• This material has been adapted from columns published in CircuiTree magazine from 2000 to 2007 and are provided by the author with his permission. Additional information on these topics can be found in: *Dry Film Photoresist Processing Technology*, a book by Karl H. Dietz PhD, published in Jan. 2001, Isle of Man, UK, 432 pages (www.elchempub.com) ISBN: 0 901150 39 8.

Fine-Line Imaging and Etching

Printed Circuit Board Applications



Electronic Chemicals

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- ENIG Processes
- Glicoat OSP Processes
- NICKELSOL EN
- Silver Guard Process
- Tin Guard Process

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- E-Prep Desmear Processes
- Shadow® Direct Metallization Process

Innerlayer Bonding Technology

- CO-BRA® Bond Oxide Alternative Processes
- Oxide/NPR Process

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- PC 600 Series DC & Pulse Copper Processes
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- Matte and Bright Tin Processes

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10

Electrodeposition and Solderable Finishes for HDI

By Michael Carano

Overview of the Electrodeposition Process

Copper Electrodeposition

A significant challenge to the HDI initiative is the ability to electrodeposit copper uniformly in blind vias. As aspect ratios of blind vias reach 1.0:1.0 and beyond, achieving minimum deposit thickness on the via wall and capture becomes increasingly difficult, regardless of the success of the metallization system. The challenge is to maintain good throwing power, without overplating the surface. And an even bigger challenge awaits the plater who must metallize PWBs with both blind and through-hole vias, which is particularly difficult as aspect ratios for through-holes and blind vias increase. With smaller diameter vias and thicker panels, the importance of higher throwing power, the high leveling acid copper electrodeposition process takes on added significance. In order for high-aspect-ratio vias to withstand multiple thermal cycles, the copper plating within the via must be uniform and have optimum physical properties. Additionally, the quality of the copper deposit depends, in part, on the performance of the metallization process previously discussed. However, the electrodeposition process must be optimized to minimize *dog-boning* and to provide a metallurgical structure

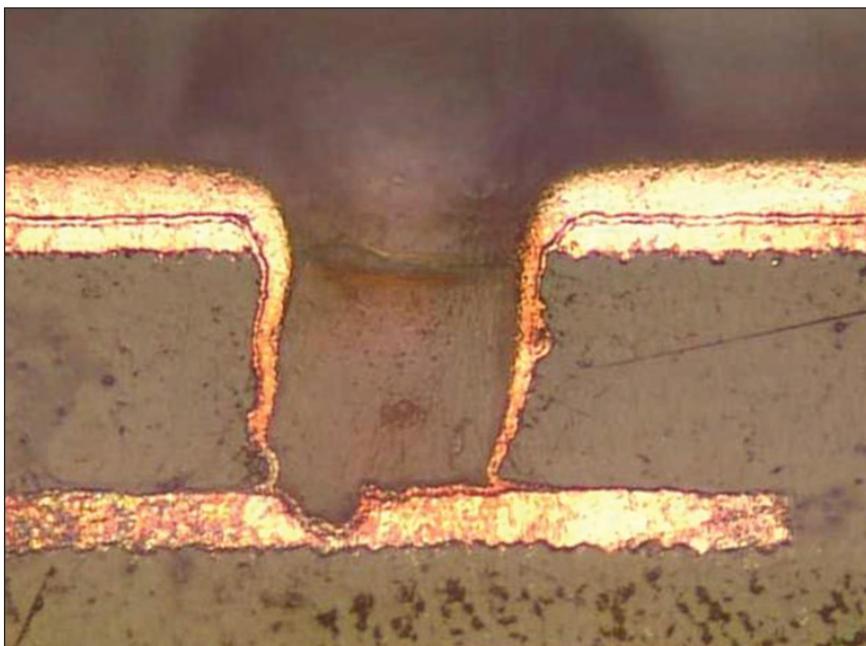


FIGURE 1: An example of dog-boning where there is more plated copper on the surface and tapering down into the via

of the copper deposit that is able to withstand the flexing and thermal excursions subjected to the PWB. Dog-boning is defined as a non-uniform thickness distribution inside the via or through-hole (Figure 1). This is of grave concern as the copper deposit must be of sufficient thickness to ensure reliability. Increasing the plating cycle time in order to plate more copper in the via only serves to exacerbate issues with surface non-uniformity.

Theory of Direct Current Plating

Conventional Direct Current (DC) plating is by far the most common and the oldest method of electroplating. In PCB manufacturing, the sulfuric acid copper bath is very popular. To influence the grain structure formation, grain refiners, wetting agents, and brighteners are added to the plain

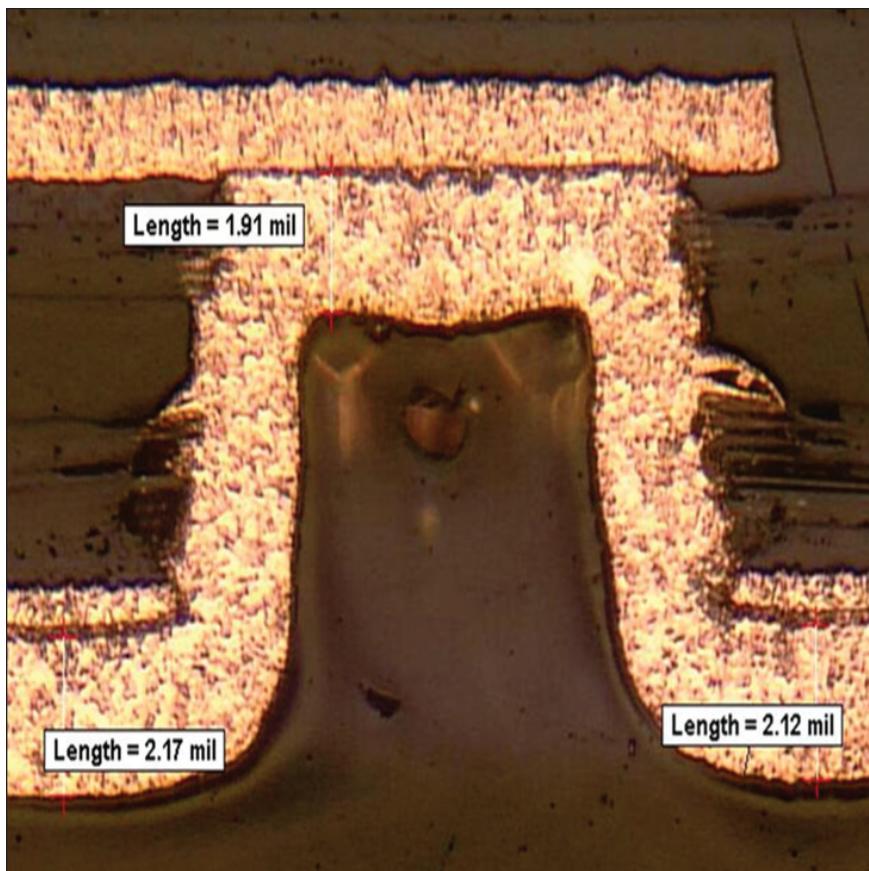
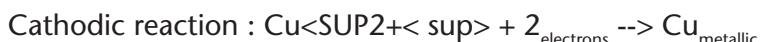


FIGURE 2: With proper plating parameters, excellent throwing power into small diameter blind vias is achievable.

electrolyte mixture of water, copper sulfate, and sulfuric acid. During electroplating, the copper ions are distracted from the solution. To maintain the copper ion concentration at a constant level, copper metal is dissolved in the electrolyte. Under influence of electric current, the following reactions take place:



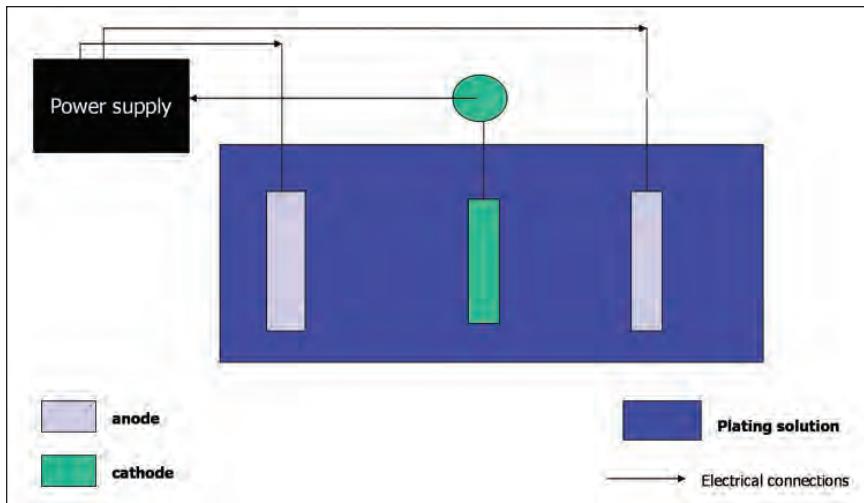


FIGURE 3: Schematic of a typical electroplating cell[1]

During the anodic reaction, some side effects are observed. In some cases, copper anode material is covered with an unknown layer. This layer is slightly soluble in sulfuric acid and is capable of blocking electrical current. The anode then becomes passive or is polarized. With the introduction of pulse-plating reversal equipment (presented later in this chapter), this polarizing property is used to improve the distribution of the electroplated metal. For a short time the current is reversed and the printed circuit board becomes temporarily anodic.

Mathematical Modeling of Plating Uniformity

There are a number of published studies on the subject of plating uniformity in through-holes.[2] Researchers developed models to test plating uniformity. With respect to plated through-holes, the models attempted to predict what influence key variables had on plating uniformity:

- Mass Transport
- Electrode Reactions
- Ohmic Resistance
- Circuitry Layout

One has to optimize the electrolytic copper process for plating on the surface and in the through-hole. Studies indicate that ohmic resistance tends to dominate the plating process with the higher aspect ratio through-holes. For example, ohmic resistance (or voltage drop) can be explained by the following model:

$$E = \frac{JL^2}{2Kd}$$

Where: E is the ohmic resistance
J is cathode current density
K is solution resistance
d is hole diameter
L is length of hole (board thickness)

As the model shows, the thickness of the panel or length of the hole influences the difficulty of plating by a squared term. In addition, an optimal balance between agitation on the PWB surface and solution movement in the holes was required to achieve a compromise between uniform plating distribution across the panel surface and excellent throwing power in the hole. The model developed by these scientists has been verified time and time again.[3] In solution, it is important to generate mixing to avoid localized reactions and non-uniformities. Plating rates are limited by mass transport. At the surface of the cathode, a boundary layer exists that slows the deposition to the surface. Uniformity of plating is important in order to reduce the thickness of this boundary layer.

Plating uniformity is a continual challenge for through-hole and microvia plating and is becoming more difficult with increasingly complex designs. It should be quite clear that

plating uniformity is closely influenced by solution chemistry and solution agitation conditions.

Options for Electrolytic Copper Deposition of High-Aspect-Ratio Vias

Complex designs and difficult-to-plate vias require careful thought and consideration in the electrolytic copper plating process. The fabricator has several options:

- Optimize process chemistry and cell design.
- Create longer plating cycle times by reducing cathode current density.
- Institute periodic pulse reverse plating.
- Implement Direct Energy Plating (DEP).

Even with a plating process with optimum throwing power, higher-aspect-ratio blind vias may exceed the performance capability of conventional acid copper plating processes. Some companies have resorted to electroplating the blind vias at less than 10 amps per square foot, in the hope that throwing power and overall distribution would be improved. However, plating times are extended in order to achieve the required plating thickness. Notwithstanding these measures, insufficient conductivity of the direct metallization coating and any other difficulties in desmear/surface preparation will lead to less than optimum plating thickness.

Direct Current vs. Periodic Pulse Reverse Plating (PPR)

An innovative solution to this problem is to change to electrodeposition process from DC plating to PPR. In the PPR process, the power supply will produce a forward cathodic current, alternating with short anodic currents. The anodic or

reverse current is typically of a very short duration or pulse. The cathodic current (forward) is typically of longer duration than the anodic current (reverse) applied. However, the reverse current typically is of greater current than the forward. PPR electroplating is the interruption and reversal of current in a bath, creating a periodic polarity change between the cathode and anode. In PPR, the forward (cathodic) plating current is disturbed and reciprocated (i.e., turned anodic) for a short time. The anodic (reverse) current causes certain molecules to drift. These additives are then attracted to the high current density areas and adsorbed on the PCB's surface. The adsorbed additive on the copper surface acts as an insulator. It will shield the current, temporarily preventing copper from being deposited during the forward pulse. This procedure is used to influence the throwing power, distribution, roughness, and other characteristics of the material during the plating process. This modified current is generally created by and delivered to the electroplating bath by the main power supply. Please note that the power supplies required for PPR plating are a considerable investment. The fabricator must carefully weigh the capital cost of the power supplies against the benefits gained. The use of PPR has shown that with an improvement in overall plating distribution and throwing power, actual plating cycle times are decreased when compared to direct (DC) current plating.

Direct Energy Plating (DEP)

A new technology has been developed to improve plating distribution. Surfct Technology (Tempe, Arizona) has introduced direct-energy plating (DEP). Instead of using mechanical methods, DEP uses vibrational energy that couples directly to the substrate. These energy modes do

more than bring about simple agitation. The waveforms can be programmed to create multiple effects: surface cleaning, contact welding, enhanced diffusion through high-aspect-ratio structures, removal of bubbles, or reduction of boundary layers for faster plating. Surflect's approach is to harness ultrasonic energy to affect kinetic energy in the plating solution. One mechanism to affect the kinetic energy of a fluid is vibration, and the means of generating this vibration is ultrasonic energy. Vibrations are waves traveling through the media. The typical frequency range of these transmissions is 0.5 kHz to 10 MHz. Depending on the frequency and modulation of the wave, it can travel in different modes, which include shear, longitudinal, and Rayleigh-Lamb waves. Each of these waves can have a different effect on the fluid.

Classic ultrasonic energy operates at one frequency and has a narrow pass band. The drawback to this approach is that cavitation tends to be large, different materials can be driven into resonance, and voids can be generated during deposition. Surflect's system utilizes a mixed-signal response to overcome the limitations of standard ultrasonic processes. By sweeping the output frequency and modulating the period of the cycle in the time domain (Figure 4), mixed modes can be created and wideband responses can be generated.

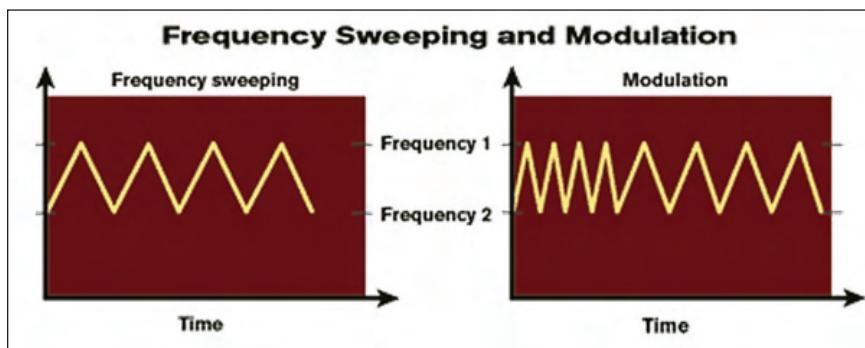


FIGURE 4: Model of frequency sweeping and modulation

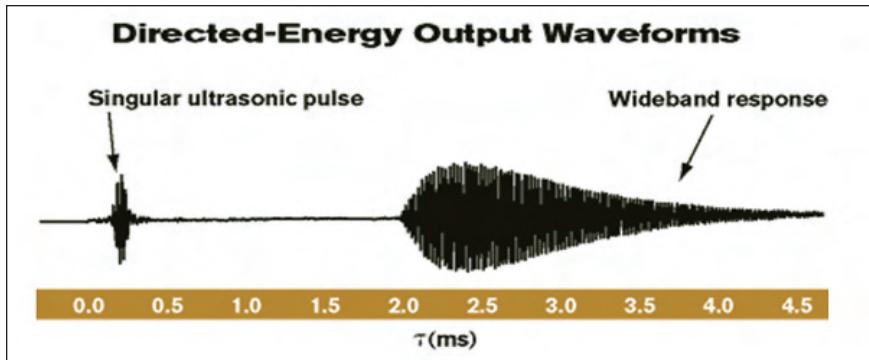


FIGURE 5: Illustration of directed-energy output waveforms[4]

Plating systems are composed of multiple materials with different resonances and responses. A broadband response that can couple to all materials of interest can be pre-programmed by sweeping the frequencies (Figure 5).

Panel Plating

Panel plating is the process by which the entire surface and vias are electroplated with copper, prior to laminating the photoresist. Ideally, a very thin copper foil should be used to start. This makes etching easier and more accurate. The method also obviates the need for an etch metal resist layer removal before solder-mask coating. Or as some fabricators prefer, the photoresist is laminated after the panel is fully plated to the required copper thickness. The resist is exposed, developed, and then the PWB is plated with the etch resist (usually tin, Electroless Nickel Immersion Gold, etc.)

Pattern Plating

Pattern plating is so named because only the circuit pattern and hole barrels are plated. Only the thin electroless copper layer or a conductive layer from the direct metallization process has been deposited in the through-holes and

microvias. Hole barrel copper, up to this point in the process, is very thin and it is far short of the typical 0.001-inch specification for copper thickness. The resist image is placed onto the PWB after the vias are made conductive. After exposure and developing, only the circuit lines and vias are exposed and able to be subsequently plated. None of the copper plated during this process is etched away, but rather, remains on the circuit and is part of the finished product. The copper is protected from the etchant by a metallic etch resist that is plated on during the next process step. The ordinary outer layer will have about 33% of the panel plated to a thickness of 1.5 mils of copper. This 1.5 mil target is to ensure a minimum thickness of 1 mil in the holes. The result is 0.6866 ounces of copper being plated per square foot of product run for a typical panel, not including the copper contained in the solution that is dragged with the panel.

Filling of Blind Vias

Filling of plated through-holes is not new to the PWB fabrication industry. For many years, end users required some or all via holes to be partially plugged with solder mask. This task was required in order to prevent solder from wicking through the holes (to the component side) during the assembly process and to create a vacuum for electrical test. Minimizing flux residue in the holes is another valid reason to undertake this operation. However, as PWB designs have evolved to more complex designs, partially filling has been replaced by full filling of blind vias, buried vias, and through-holes. In general, full or super-filling with plated copper is achievable with blind vias. And polymeric pastes, either non-conductive or conductive, are used to completely fill through-holes and blind vias. Figure 6 shows a filled blind via.

The key reasons for via filling are:

- to increase the density and frequency for PWBs;
- to minimize signal delays and avoid the effects of electron migration;
- to make a smooth surface layer and avoid indentations;
- to enhance the I/O number of package substrates;
- to avoid incomplete fill of microvia holes filled by dielectric or conductive materials;
- to solve the differences in coefficient of expansion of metal and resin;
- to improve fine-line design, via on via, and interconnect reliability.

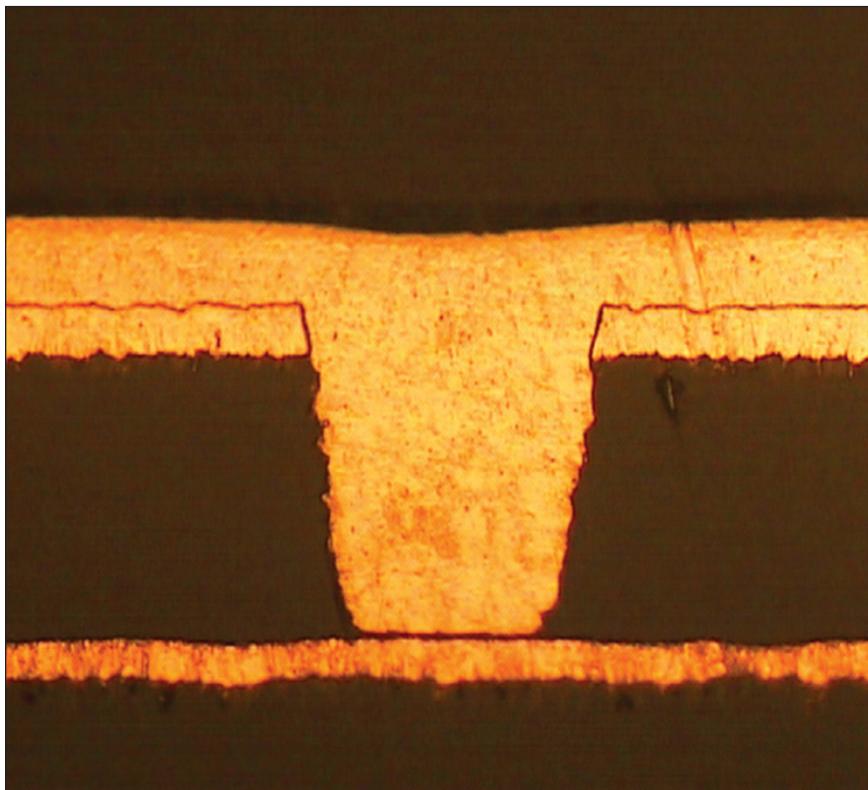


FIGURE 6: Example of a filled copper via

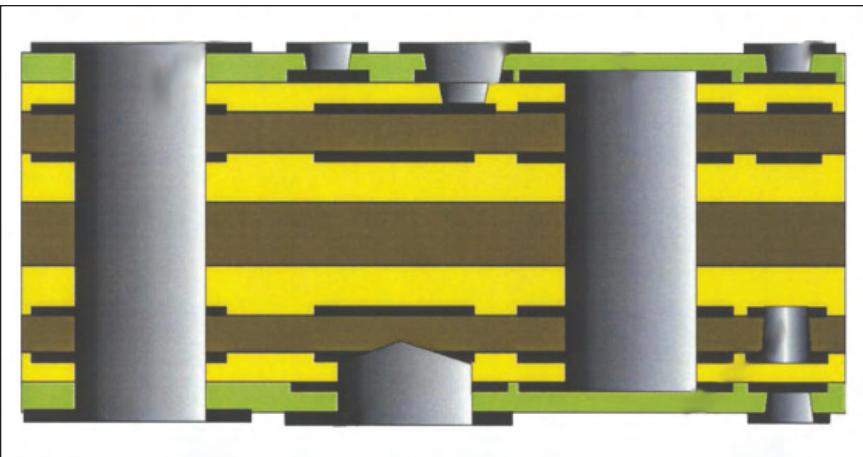


FIGURE 7: Typical mechanical drilled blind and buried vias compared to laser drilled blind and buried vias, drawn to scale

Electrodeposition of copper metal into vias has gained acceptance as a consistent means of achieving a solid copper via solution. Driven by high-density interconnect technology and the need for miniaturization, super-filling of microvias with copper plated metal relies on a thorough understanding of electroplating principles, cell design (including solution agitation and anode placement), and the functionality of organic addition agents. Fluid mechanics plays a very important role in determining the extent of filling power in a blind via. Since a typical circuit board design may include through-holes in addition to blind vias (Figure 7), the fabricator must consider mass transfer and ohmic resistances in addition to fluid flow. As aspect ratios increase, either due to increased PWB thickness or decreased via diameters, ohmic resistance increases. Increases in ohmic resistance negatively influence throwing power in the through-hole vias, which is considered a serious issue and will be addressed throughout this chapter.

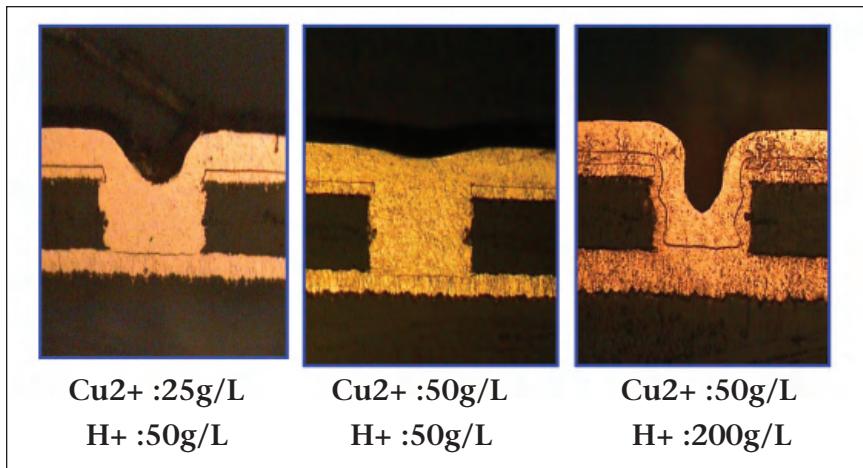
Discussion of Key Plating Parameters Involved in Super-filling

Acid copper baths used for plating of PWBs consist of copper sulfate, sulfuric acid, and chloride along with organic additives that function as brighteners, carriers, suppressors, and/or levelers. In general when we are plating PWBs we use high throw formulations to improve throwing power into small holes on thick panels. For proper filling of blind vias the fabricator must use formulations that are high filling solutions (Table 1), which means that they are good at filling the blind vias on the panel without resulting in plating folds and without leaving large depressions. These high filling solutions may or may not be good at providing sufficient copper thickness in high-aspect-ratio holes. There are three primary considerations to ensure good filling of blind vias.

1. Sulfuric acid to copper ratio - In high-aspect-ratio plating the sulfuric acid is typically 225 g/L and the copper concentration is 15 g/L, resulting in a ratio of acid to copper of 15:1. For super-filling solutions the acid and copper concentrations are each 50 g/L, giving a ratio of 1:1. The effect of varying the ratio is shown in Figure 8.

TABLE 1: Recommended electrolyte for super-filling

Item	Range	Consumption rate (ml/Amp.Hr)
CuSO ₄ .5H ₂ O	180 ~ 220 g/L	–
H ₂ SO ₄	2~ 4 %	–
Cl-	50 ~80 ppm	–
Leveler	2 ~5 ml/L	0.2~0.3
Grain refiner	2 ~5 ml/L	0.15~0.3
Carrier	10~20 ml/L	–
Current density	12~24 ASF, DC	–

**FIGURE 8:** Effect of varying sulfuric acid to copper ratios

2. Proper control of organic addition agents - Organic addition agents influence the mechanics of bottom-up filling (from the capture pad of the blind via), grain refinement of the deposit, overall leveling of micro-imperfections along the hole wall, and governance of the plating of copper on the surface of the via. See model of the reaction mechanism for the additive chemistry introduced earlier in this chapter.

If super-filling is not desired, then the high throw electrolyte formulation detailed in Table 2 works well for

TABLE 2: Details of high throw electrolyte formulation that works well for optimum throwing power in the blind vias and through-holes

Component	Range
Copper Sulfate	4½ – 8 oz/gal
Sulfuric Acid	30 –34 oz/gal
Chloride	70 - 90 ppm
Organic addition agent (brightener)	40-60 asf burn, 2A, 5 min
Carrier	> 1.2 %
Agitation	Eductors with 10" clearance and mechanical cathode

optimum throwing power in the blind vias and through-holes.

3. Agitation system - For super-filling of blind vias, a homogeneous mixing of the electrolyte is necessary to avoid over-plating of the surface while the via is being plated from the bottom up. The engineer may need to experiment with flow rates in order to optimize the super-filling process.

Solution agitation of the copper plating electrolyte may be accomplished with air agitation, eductors, solution impingement, or cathode bar movement. The main purposes of agitation are to eliminate solution stagnation and dispersal of reaction products, to increase deposition rates by mass transfer enhancement, and to dissipate heat at electrode/solution interfaces.

Air, as an agitator, suffers from some disadvantages, including a chemical oxidative action toward solution constituents, electrical resistance when present as a cloud or foam of bubbles, and lack of significant plating rate enhancement, despite several possible parameters for adjustment. The least appreciated characteristic of air is its resistivity, which can lead to an increase in electroplating power of 25 to 30 percent and become a significant electrical cost factor. Air also generates environmental pollution through its dispersion of air bubbles. These tiny bubbles can lodge into the through-holes and blind vias, leading to a reduction in plating thickness or voids.

Eductors are jets based on the Venturi Principle, whereby one volume is pumped and up to four volumes are drawn in by the pressure drop, making it a highly efficient jetting system, as seen in Figure 9. When fully submerged, no air is entrained. Eductor agitation overcomes several of the disadvantages associated with air agitation. Air bubbles and misting are eliminated. In addition, eductor agitation provides a more uniform mixing of the plating solution, which minimizes potential *dead spots* in the cell where air



FIGURE 9: Top view of a plating cell equipped with eductors

agitation is lacking. Educators provide more uniform agitation, better known as laminar flow. In contrast, air agitation provides a turbulent flow and may only promote mixing of the solution. For quality plating results, it is preferable to have interface agitation, where one interface agitation is directed more at the cathode diffusion layer. This helps to reduce the diffusion layer thickness, permitting the efficient delivery of

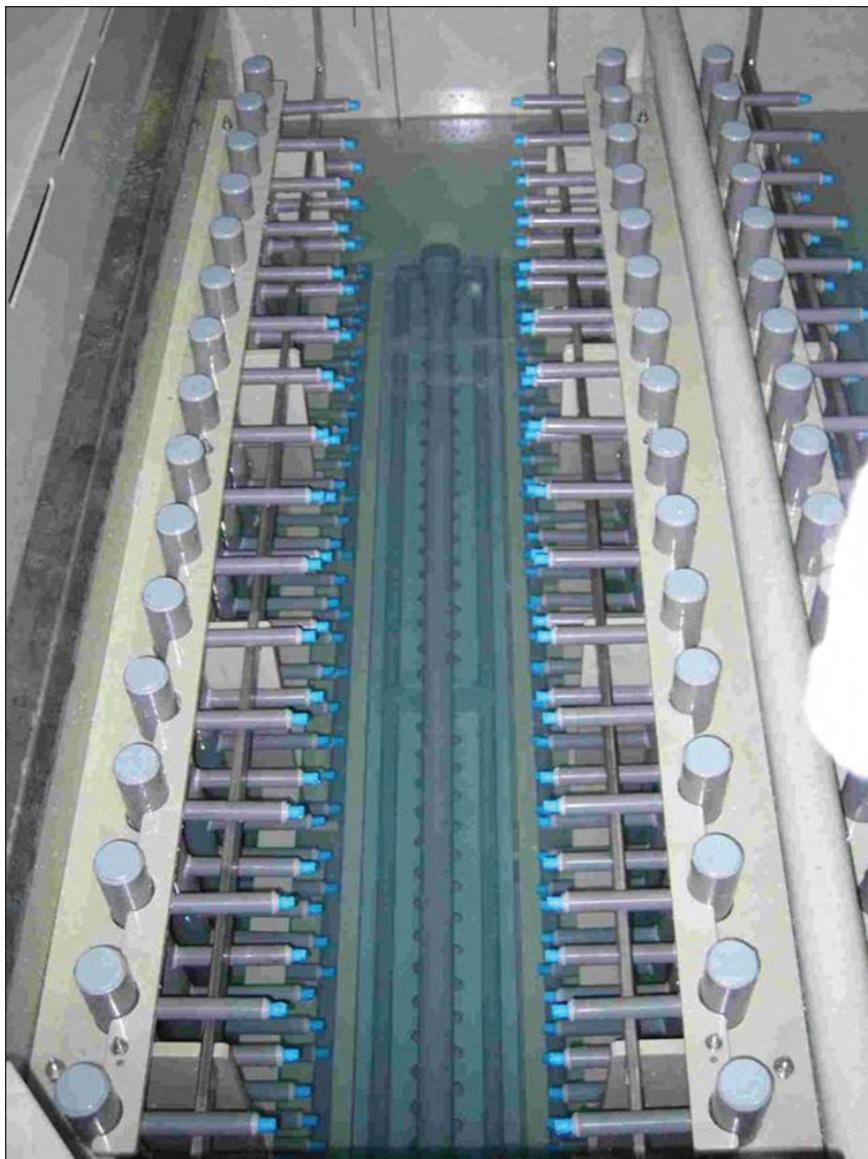


FIGURE 10: Top view of an actual plating cell using vertical impingement

additives and ions to the cathode surface.

An alternative to eductor agitation is the use of impingement. Figures 10 and 11 illustrate how the electrolyte is constantly pumped through a manifold system, through a set of vertical spray bars.

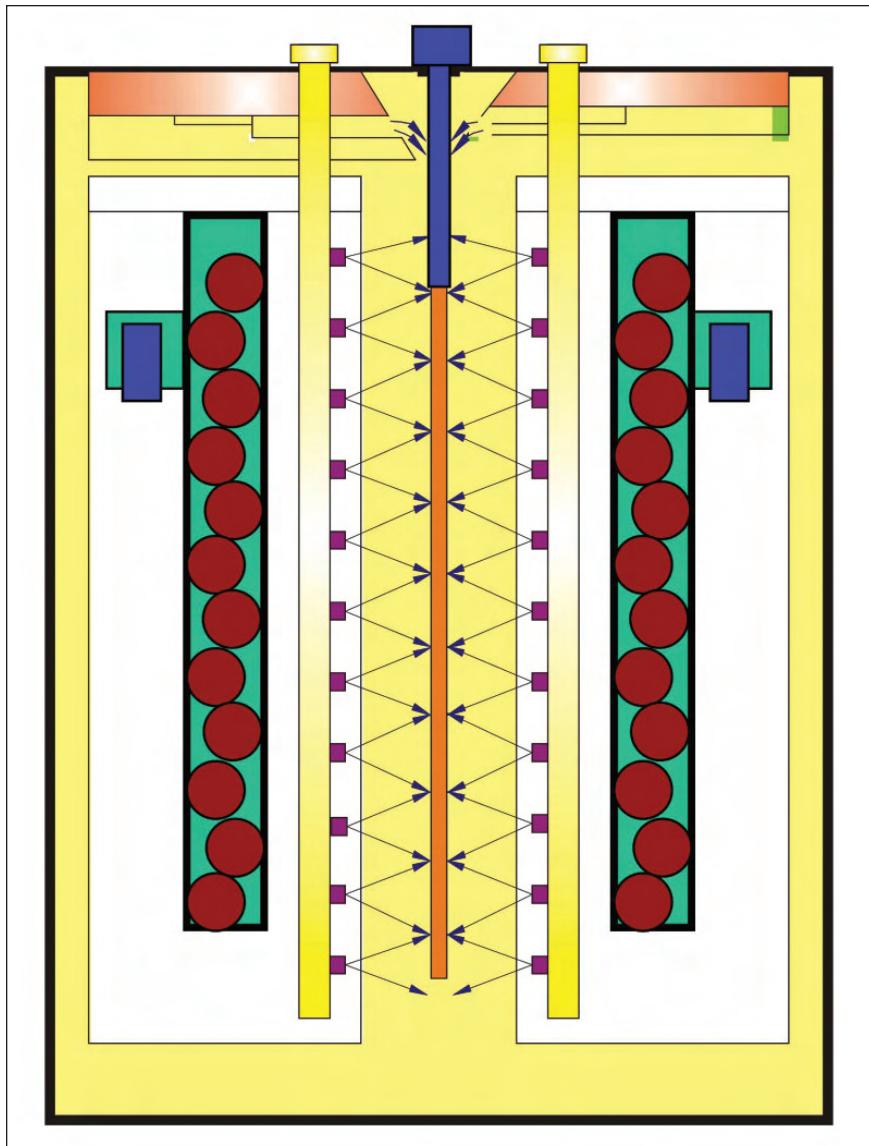


FIGURE 11: Schematic of cell-side view of above plating

Mechanism of Bottom-up Filling

Figure 12 depicts the reaction model of via filling plating. Each of the three organic addition agents plays a role in the quality of the fill. The brightener component is the smallest

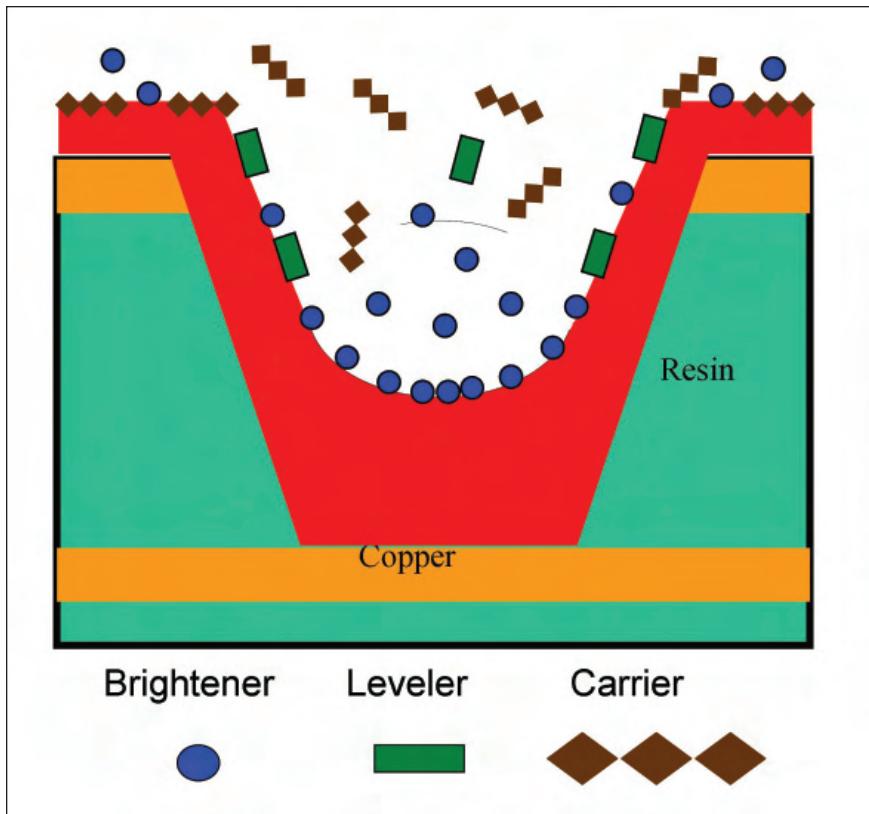


FIGURE 12: Schematic of bottom-up (super-filling) plating mechanism

in size, but has higher priority to adsorb on the via bottom and accelerate the deposit rate. The leveler adsorbs on the via corner and suppresses the deposit rate, which can prevent void product. The carrier is a high molecular weight polymer. It is designed to adsorb on the via surface easily and suppress the deposit rate. Combined with all of the component's functions, this causes the *bottom-up* mechanism.

Optimization of Process for Optimum Performance

There are several non-chemical factors that influence plating performance. Each of these factors are presented below.

Plating Cell Design

The plating cell design must, at the very least, be symmetrical with proper spacing between the anode and cathode. Six to eight inch spacing typically enables good throwing power. The bus bars that carry the current to the plating racks and anodes must be of sufficient size to minimize resistance in current flow. Resistance to current flow will reduce plating thickness and negatively impact optimum throwing power and plating distribution.

Proper Plating Cell Filtration

The need for filtration cannot be emphasized enough, especially when plating in through-holes and blind vias. Any void in the plating in the hole caused by small pieces of contaminant causes a reduction in the area available to carry the electric current. Rejects would also be caused when tin or tin-lead are used as a resist in the etching process, since any voids would allow etching in unwanted areas. Nickel and gold plating baths are also critical. If activated carbon powder is used to adsorb organic impurities, it may be added to a pre-coated surface or mixed with the solution in a treatment tank. Adsorption is quick, but the powdered carbon is difficult to remove from solution.

Flow rates are the only means of carrying solids to a filter or bringing fresh solution into contact with the particulate matter. The rate of flow is referred to as the turnover, i.e., total gallons pumped per hour in relation to the size of the tank. For example, 200 gal/h on a 100 gal tank is two turnovers per hour. Dirt holding capacity is essential and can be attained with throw-away paper, cartridges of different porosities, or filter surfaces coated with filter aid. Porosities of 100 microns down to less than one micron are typical. In practice, the

average plating solution is turned over once per hour. The recommended flow rates should provide at least two complete tank volume turnovers per hour. However, to achieve the ultimate in clarity, turnovers of up to ten times per hour may be necessary. Keep in mind that the initial flow rate is not the average flow rate. In other words, if one started at 1,000 gal/h and cleaned or replaced the filter when the flow was reduced to 200 gal/h, the actual average flow would probably be about 600 gal/h, depending upon the type of filter media used.

Anodes: Soluble vs. Insoluble

Via filling plating is very sensitive to equipment set-up, so great care should be taken. When using soluble anode, dissolution of anode may result in side reaction with additives.

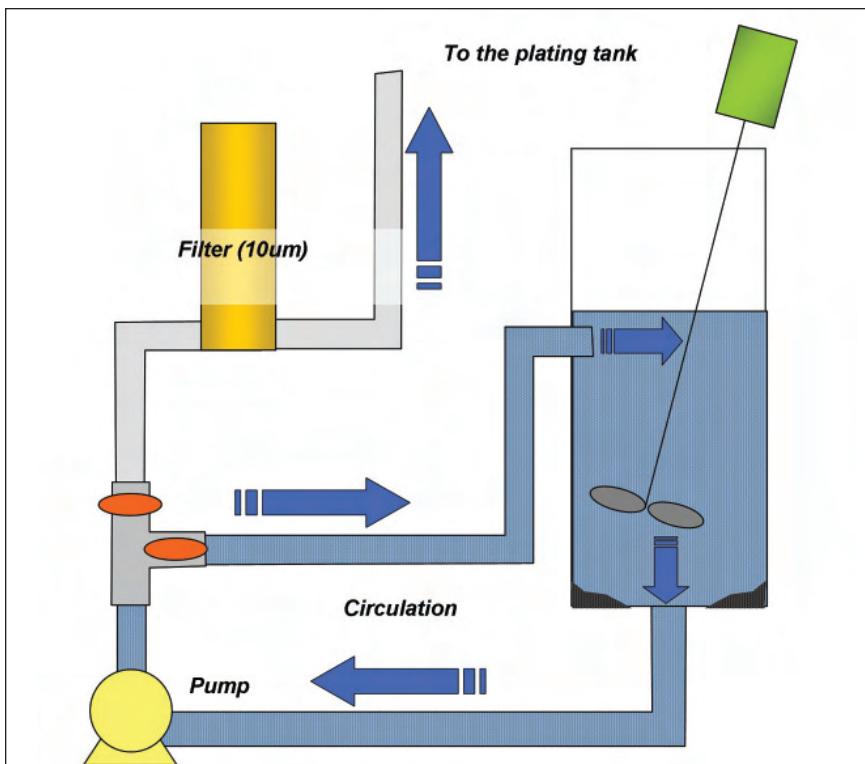


FIGURE 13: Copper feeder system (Courtesy of Rohm and Haas)

Use of insoluble anode, the electrolysis reaction of water, generates large quantities of oxygen, can result in excess consumption of organic additives and interference with plating at the cathode interface.

Recent data suggest that the quality of the via fill is enhanced through the use of insoluble anodes. With the use of insoluble anodes, the copper content must be replenished through the addition of copper oxide. In Figure 13, an example of a direct copper feeder system is shown. The copper oxide is added into the mixing tank and *digested*. The digested copper is then fed into the plating cell as needed.

Via Shape and Its Influence on Via Filling

The shape of the blind via prior to plating is critical for a proper via fill. A V-shaped via, as shown on the left in Figure 14, is ideal. When the via is more of a cup shape as shown on the far right, the uniformity of the fill is compromised.

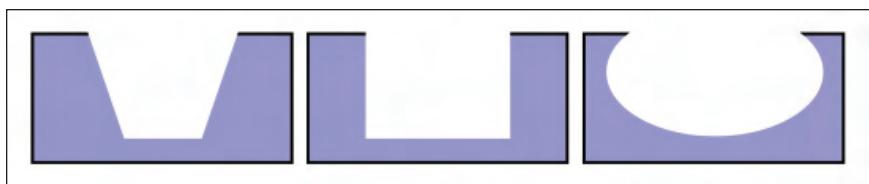


FIGURE 14: Via shape on the left is most suited for optimal filling

The High-Density Plating Challenge

As discussed previously, super-filling of blind vias requires an electrolyte formulation that is not ideal for plating high-aspect-ratio through-holes. Super-filling requires a higher copper concentration and lower acid content, which reduces the opportunity for optimal throwing power in plated through-holes. However, with improvements in solution agitation and organic addition agents, super-filling of blind

vias, while achieving reasonable throwing power in plated through-holes, is possible.

Board designs with blind vias and through-holes that do not require super-filling should be processed in a standard high throw electrolyte as discussed previously.

Tin Plating Etch Resist

The solder mask over bare copper technique is the primary method with practically every printed wiring board produced

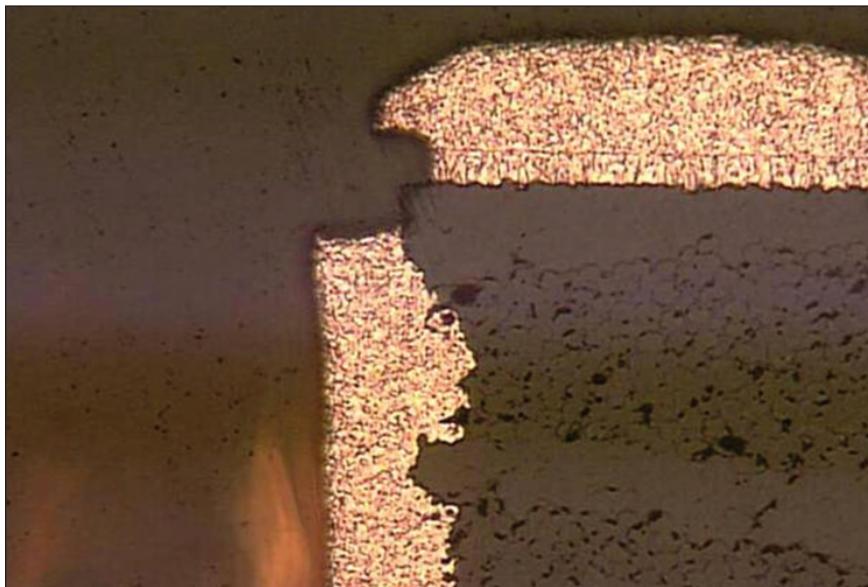


FIGURE 15: Etch out void on via corner caused by skip plating of the tin etch resist.

today. The tin plating step acts only as an etch-resistant over-plate. The critical factor with which to be concerned is ensuring a sufficient tin plating thickness on the surface and through the vias. This is necessary to protect the underlying copper from etch out voids (Figure 15).

Process Maintenance

- Carbon Treatment
- Analytical Controls

Analytical Controls

There is no substitute for tight control over the plating processes. While the Hull Cell method is purely qualitative, it does help the engineer keep close control over the acid copper and tin plating processes.

Dilution Hull Cell Technique

A blank copper plating solution should be prepared to approximate the bath to be tested. The copper sulfate and sulfuric acid concentrations should be within about ten percent of the concentration of the bath to be tested. The blank bath should be made up as follows:

Copper Sulfate	as test bath, ± 10%
Sulfuric Acid	as test bath, ± 10%
Chloride	40-60 ppm (1 mL of 10% HCl per Liter of blank)
Acid Copper Carrier	1% v/v

Hull Cell Panels

All Hull cells referred to below should be run for five minutes at two amps using an air agitated Hull cell and brass or copper panels. Figure 16 provides a reference for the general appearance of the resulting panels. To prevent false indications, temperatures and agitation should be similar for all tests.

- A.** Run a Hull cell on the “as is” test bath. If panel A shows excessive burn, it indicates that insufficient brightener is present, so go to B. If panel A shows an acceptable amount of burn, this indicates that the brightener concentration is at or above an acceptable concentration, so go to C.

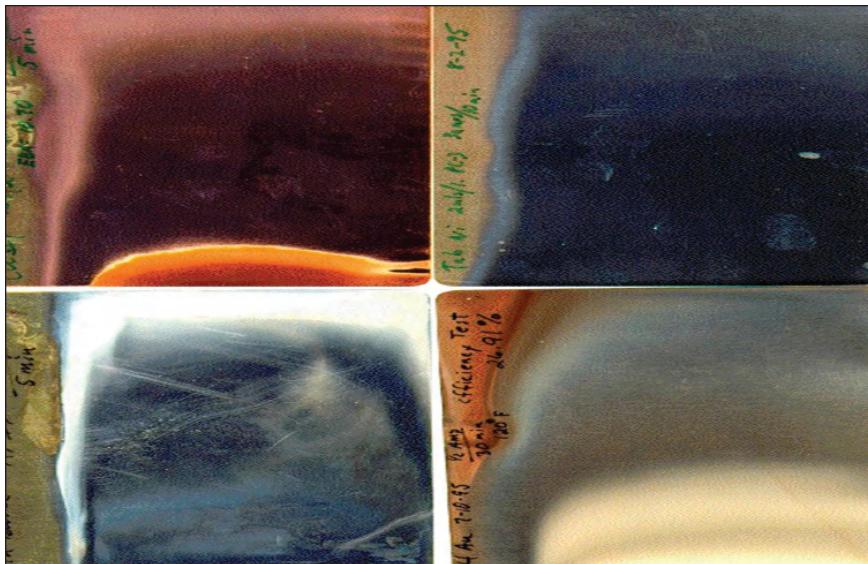


FIGURE 16: “As sampled” hull cells and hull cells plated with various metals (copper, nickel, tin, and gold)

- B.** Add .05% of the additive (0.134 mL in 267 ml) and run a second panel. An acceptable panel indicates the need for an equivalent addition of the additive to the working bath. A second .05% add can be made, if needed.
- C.** Add 133 ml of the sample bath to 133 ml of the blank bath (a 50% dilution) and run a Hull cell panel on the diluted sample. An increase in the burn over panel A indicates that the brightener is within the optimum range. No increase in burn over panel A indicates that excessive brightener is present.

Notes: If slightly broader control is acceptable, a 75% dilution can be used (67 ml of sample bath plus 200 ml of blank) in place of the 50% dilution.

When optimum leveling is needed, substitute a 30% dilution (187 ml of bath and 80 ml of blank) for the “as

sampled" panel and a 75% dilution (67 ml of bath and 200 ml of blank) for the 50% dilution.

In cases of high brightener, larger dilutions may be used to give an indication of the magnitude of the brightener overdose.

Electroanalytical Methods

Cyclic Voltametric Stripping (CVS) and Cyclic Pulse Voltametric Stripping (CPVS)

Acid copper electroplating baths used to form ultra-fine circuitry features on high-density semiconductor chips contain suppressor, anti-suppressor, and leveler additives that must be closely controlled in order to obtain acceptable copper deposits. CVS methods are available to measure the concentrations of the suppressor and anti-suppressor based on the effects of these additives on the copper electrodeposition rate. The CVS method uses measurements of the copper electrodeposition rate to determine the concentration of the leveler additive. The other two additives are included in the measurement solution at concentrations determined to provide the optimum compromise between minimal interference, high sensitivity, and good reproducibility for the leveler analysis. In this case, measurement precision is greatly improved compared to the precision provided by inclusion of the interfering additives in the measurement solution at their concentrations in the bath sample at the time of the analysis, which would be the standard analytical procedure.

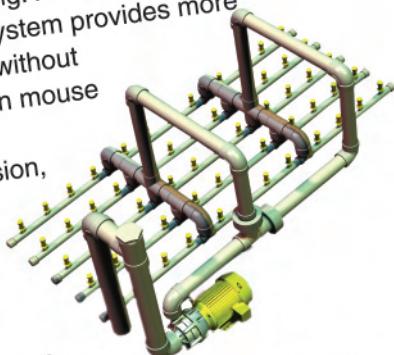
Analysis of baths is performed in an electrochemical cell using a three-electrode system, one of which is a platinum rotating disk electrode. During measurement, the potential of the platinum electrode is controlled by the instrument. The

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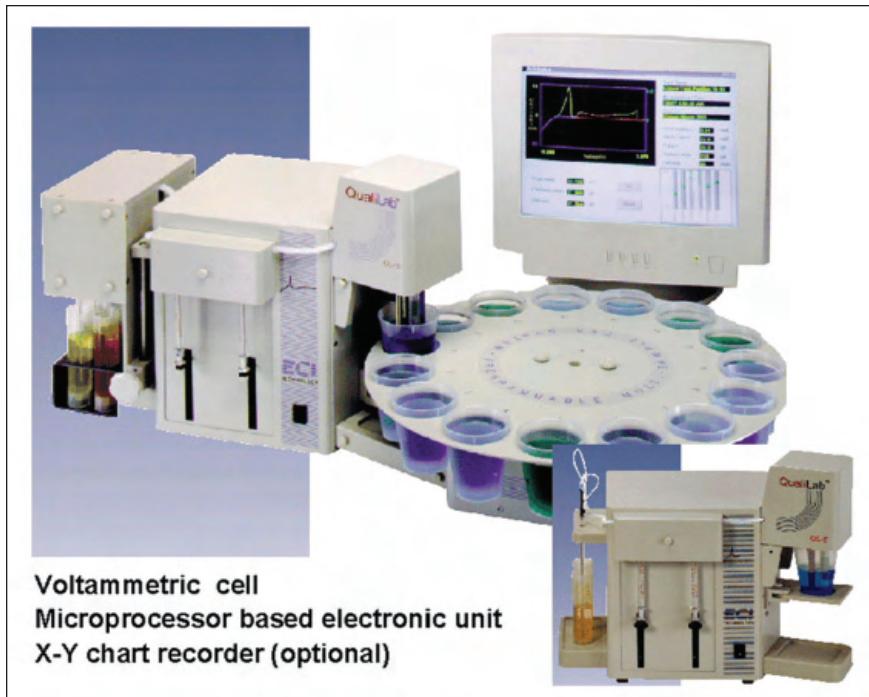


FIGURE 17: Voltammetric cell set-up

potential is scanned at a constant rate, back and forth between negative and positive voltage limits. A small amount of metal from the plating bath is alternately plated onto and stripped off the working electrode as the potential is changed. During the scan, the current at the working electrode is measured as a function of potential.

The activity of the additive will affect the plating rate of the metal onto the electrode. The plating rate is determined by calculating the charge required to strip the metal off the working electrode. The relationship between the stripping charge and the activity of the additives is used to quantitatively measure the additives and their components. Fresh additive, as supplied by the manufacturer, is used as a standard. The activity of the additive in the production bath is expressed as concentration (mL/L) of the fresh additive. The

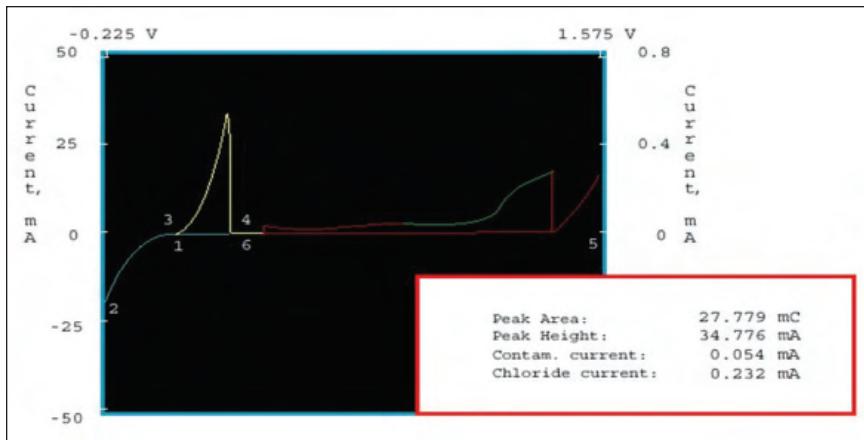


FIGURE 18: Actual voltamogram obtained during a CVS analysis

CVS unit performs the patented CVS analysis automatically (Figure 17).

An example of a voltamogram (plot of the measured current vs. applied potential) for an acid copper plating bath is shown in Figure 18.

The potential determines the electrochemical reaction that occurs. The potential is displayed on the X-axis with potentials becoming more positive from left to right. A positive-going potential is more strongly oxidizing, while a negative-going potential generates a more strongly reducing condition. Current is shown on the Y-axis. A positive current corresponds to an oxidation while a negative means a reduction. (Courtesy of www.ecitechnology.com)

Solder Mask Technology

HDI technology presents a variety of challenges for the fabricator. Among these challenges are solder mask definition, developing of the finer features, and concerns over leaving solder mask residue in the vias. Registration tolerances are also much tighter owing to the greater circuit density requirements.

TABLE 3: Solder mask registration and resolution challenges (units in μm)

	Now	Needed
Circuit Line & Space	50/75	40/40
Ball Pads	300	180
Mask Opening	380	220
Registration Accuracy	+/- 40	+/- 20
Mask Webs	120	80

In Table 3 the current capability and future needs for solder-mask attributes are listed.

Laser Direct Imaging (LDI)

In order to achieve circuit features and registration requirements, laser direct imaging (LDI) may be necessary. LDI is a process of imaging PCBs directly without the use of a phototool or mask. The exposure of the photo-sensitive resist is done using a laser beam that is scanned across the panel surface and switched on and off by means of a computer control system. The laser used in this process is often assumed to be in the UV spectrum, as this tends to suit most of the commonly available photoresists. However, systems exist that operate in both the visible and infrared spectra working with specially formulated photoresists. Papers have been written on both alternatives over the years, but it is the UV-based systems that interest most of the PCB manufacturers as they offer the opportunity to be a direct plug-in replacement for the *yellow room* environment. Consequently, the information in this chapter addresses UV laser systems.

There are a number of advantages that LDI has when compared to traditional UV methods. First, LDI eliminates

the need for phototools. There are costs savings associated with the elimination of the phototools, as well as phototool (print through) type defects. Registration is improved for several reasons. By eliminating the phototool, one eliminates temperature and humidity issues associated with film based tools. Also, alignment issues related to the movement of the tools during exposure are not an issue. The movement of conventional tools relates to the tendency for contact printers to run hot, causing the phototool to move.

Overview of Solderable Finishes

Introduction:

Surface finish is about connectivity. It is the surface to which the connection from the board to a device occurs. However, a surface finish used for solderability purposes only, is, at best, a compromise. In an ideal world the assembly engineer would receive bare copper PWBs for assembly. There would be no issues with flatness, product density, cleanliness, etc. However, this is not an ideal world. The ability of the assembly process to deal with oxidized copper as the solderable surface, with the flux activity used in today's assembly industry, is not there. The assembly engineer/designer needs to choose a surface finish that will meet or closely meet his product's needs while keeping in mind that in today's very cost sensitive environment, the choice of the surface finish may be heavily influenced by its per unit cost.

The first surface finishes were by-products of PWB manufacturing. SnPb as an etch resist subsequently reflowed and fused and became the surface finish of choice for many years. A mix of electrolytic nickel gold to plate the tabs for edge connectors was thrown in for good measure, directly

reflecting the technology of the components and assembly techniques of the time.

The introduction of SMT technology forced a change from the simple reflow SnPb surface finish to one that would meet the demands of the assembly industry. New designs required innovative solutions. Ball grid arrays, wire bonding pads, press fit, and contact switches were all outside the traditional realm of HASL and electrolytic nickel gold. In addition, environmental concerns are causing designers to focus on the elimination of lead. This will change HASL from a standard solder to a new lead-free HASL. A series of surface finishes emerged to fill these needs:

- **Organic Solderability Preservatives (OSP)**
- **Electroless Nickel/Immersion Gold (ENIG)**
- **Electroless Nickel/ Electroless Palladium/Immersion Gold (ENEPIG)**
- **Immersion Silver**
- **Immersion Tin**

Each one of these surface finishes offers connectivity solutions in some areas (Table 4). Only one, ENEPIG, is capable of meeting all the different assembly requirements. It is often referred to as the *Universal Finish*.

Organic Solderability Preservative (OSP)

Principle: Organic Solderability Preservatives are organic coatings that preserve the copper surface from oxidation until it is soldered. The two most widely used preservatives are both nitrogen bearing organic compounds. Benzotriazoles is one class and Imidazoles is the other. Both of these organic chemicals have the ability to complex with the exposed copper surface. In that respect they are copper-specific and do not

adsorb to the laminate or the solder-mask.

Benzotriazoles form a mono-molecular layer and protect the copper until it is exposed to a single thermal excursion at assembly. The coating will readily volatilize under reflow thermal conditions.

Imidazoles form a thicker coating and will survive multiple thermal excursions at assembly.

Process:

Process Step	Temp °F	Temp °C	Time/min*
Cleaner	95 - 140	35 - 60	4 - 6
Microetch	75 - 95	25 - 35	2 - 4
Conditioner	85 - 95	30 - 35	1 - 3
OSP	120 - 140	50 - 60	1 - 2

*For conveyorized equipment the dwell time must be reduced. Consult with equipment and chemical supplier.

Product: OSP has a thin layer of organic compound which coats the copper surface. The coating is as low as 100 Angstroms for benzotriazoles and as high as 4,000 Angstroms for imidazole-type preservatives. The coating is transparent and not easily discernable, making inspection difficult.

Assembly: At assembly the organic coating is readily dissolved into the screened paste or into the acidic flux. In either case, it leaves a clean active copper surface to which to solder. The solder then forms a copper/tin inter-metallic joint. Imidazoles may require a more aggressive flux after the first and second thermal excursions. Assemblers who use OSP are very familiar with the fluxing requirements for this finish.

Limitations: One of the biggest limitations is that the coating is difficult to inspect. OSP's organic coating is non-conductive. Benzotriazole, being a very thin coating, does not interfere with electrical test. Some imidazoles, on the other

hand, are thick enough to interfere with electrical test. Most shops that use these thicker coatings do their electrical test prior to OSP applications.

Electroless Nickel Immersion Gold (ENIG)

Principle: In the ENIG finish, a layer of electroless nickel with a thickness of 120 to 240 µins (3 to 6 microns) is deposited on the copper surface. This is followed by a thin coating (2 to 4 µins) of immersion gold. The nickel is a diffusion barrier to copper and is the surface to which the soldering occurs. The function of the immersion gold is to protect the nickel from oxidation or passivation during storage.

Process:

Process Step	Temp °F	Temp °C	Time/min
Cleaner	95 -140	35 - 60	4 - 6
Microetch	75 - 95	25 - 35	2 - 4
Catalyst	RT	RT	1 – 3
E Nickel	180 – 190	82 – 88	18 – 25
I Gold	180 - 190	82 - 88	6 - 12

The long dwell times needed for this process, make horizontal conveyorization impractical.

Applications: ENIG gives a flat co-planar surface. It is solderable, wire bondable, and is ideal as a switch-contacting surface.

ENIG has excellent solder wettability characteristics. The gold readily dissolves in the molten solder leaving a fresh nickel surface to form the solder joint. The amount of gold that dissolves in the solder is insignificant and will not cause solder joint embrittlement. The nickel forms a tin/nickel intermetallic joint.

ENIG is compatible with both aluminum and gold wire

bonding. However, the gold wire bonding is marginal and not recommended for this finish. Gold wire bonding requires more gold thickness than ENIG is capable of producing. Aluminum wire bonding works well on this surface as the aluminum wire will eventually form a bond with the underlying nickel.

ENIG is an ideal surface for soft pad contacts. These contact surfaces are needed for applications like telephones, pagers, and any device that requires frequent on/off switching. The hardness and thickness of the nickel lends itself well to this type of application.

Limitations: The process is relatively complex and requires good process control.

The electroless nickel bath operates at 180 to 190° F (82 to 88° C) and the dwell time usually exceeds 15 minutes.

Solder-mask compatibility must be taken into account here. Continuous replenishment is needed as nickel is plated out. Good process control is of particular importance to achieve the desired thickness and morphology of the nickel deposit.

The gold bath operates at similarly high temperatures. An eight to ten minute dwell time is adequate to deposit the required immersion gold thickness. Excessive dwell times and operating the bath out of the vendor's specifications are known to cause corrosion to the underlying nickel. If the corrosion is excessive, it can interfere with the functionality of the nickel surface.

Electroless Nickel/Electroless Palladium/ Immersion Gold (ENEPIG)

Principle: In this finish an electroless nickel layer of 120 to 240 μ ins (3 to 6 microns) is deposited on the copper surface, which is then coated with an electroless palladium layer of a thickness of 4 to 20 μ ins (0.1 to 0.5 microns) and

finally topped with immersion gold at 1 to 4 µins (0.02 to 0.1 microns). The electroless palladium layer prevents any probability of corrosion that may be caused by the immersion gold deposition reaction and creates an ideal surface for gold wire bonding. The gold layer caps the palladium and ensures that its catalytic activity is contained.

Process:

Process Step	Temp °F	Temp °C	Time/min
Cleaner	95 -140	35 - 60	4 - 6
Microetch	75 - 95	25 - 35	2 - 4
Catalyst	RT	RT	1 – 3
E Nickel	180 – 190	82 – 88	18 – 25
Catalyst	RT	RT	1 – 3
E Palladium	120 – 140	50 – 60	8 - 20
I Gold	180 - 190	82 - 88	6 - 12

Applications: ENEPIG gives a flat co-planar surface. ENEPIG is the universal surface finish. It is capable of functioning as the ENIG finish. In addition the electroless palladium at this thickness makes an ideal surface for gold wire bonding.

During soldering, the palladium and the gold both eventually dissolve in the solder and the joint forms a nickel/tin inter-metallic. During wire bonding the aluminum and the gold wires bond to the palladium surface. Palladium is a hard surface and is suitable for contact switching.

Limitations: The primary limitations for this finish are the additional cost of palladium and the added processing steps at the board shop.

Immersion Silver

Principle: Immersion silver deposits provide a thin

(5 to 15 µins or 0.1 to 0.4 microns), dense silver deposit incorporating an organic. The organic seals the surface and allows for extended shelf life. Silver offers a flat, extremely solderable surface that may be applied with high productivity in conveyorized equipment. The surface is also bondable for both aluminum and gold wire.

Process:

Process Step	Temp °F	Temp °C	Time/min*
Cleaner	95 -140	35 - 60	4 - 6
Microetch	75 - 95	25 - 35	2 - 4
Predip	RT	RT	0.5 – 1
I Silver	95 – 115	35 – 45	1 – 2

*For conveyorized equipment, the dwell time must be reduced. Consult with equipment and chemical supplier.

Application: Immersion silver is an ideal surface for soldering. During assembly the silver readily dissolves into the solder allowing the formation of copper/tin inter-metallic solder joints, similar to HASL and OSP. It offers the co-planarity that HASL lacks and it is also lead-free. Unlike OSP, it offers ease of inspection with no compromise in performance after the third thermal excursion. Immersion silver lends itself well to electrical test in the board shop. At this time the application of immersion silver as a contact surface for extended use remains to be demonstrated.

Limitations: The concern with silver has always been silver migration in electronic environments. This is due to the tendency of silver to form water-soluble salts when exposed to moisture and electrical bias.

Immersion silver, with the incorporation of organics, minimizes this phenomenon. In addition immersion silver, as a surface, does not survive the assembly process. After wire

bonding, the exposed silver is encapsulated and isolated from the environment.

Immersion Tin

Principle: Immersion tin became viable as a surface finish when two problems, namely grain size and copper/tin inter-metallics, were overcome. The deposit was engineered to be fine-grained and non-porous. A thick deposit of 40 µins or 1.0 micron was feasible, ensuring a copper-free tin surface. A new class of immersion tin processes do exactly that.

Process:

Process Step	Temp °F	Temp °C	Time/min*
Cleaner	95 - 140	35 - 60	4 - 6
Microetch	75 - 95	25 - 35	2 - 4
Predip	75 - 90	25 - 30	1 - 2
Tin	140 - 160	60 - 70	6 - 12

*For conveyorized equipment the dwell time must be reduced. Consult with equipment and chemical supplier.

Application: Immersion tin is a highly solderable surface and forms the standard copper/tin inter-metallic solder joint. Tin provides a dense uniform coating with superior hole wall lubricity. This characteristic makes it the choice for backplane panels that are assembled by Press Fit or Pin Insertion.

Limitations: The bath makeup entails the use of thiourea, which is banned in certain geographical locations for environmental reasons. During processing in the board shop, the primary by-product in the bath is copper thiourea. Waste treatment allowances must be made for the containment of the thiourea and its copper salt by-product.

The shelf life of the surface is limited (less than one year) due to the progression of the copper/tin inter-metallic until it

reaches the surface and renders the product non-solderable. The progression of this process could be accelerated under excessive temperature and humidity conditions.

Selective Electroless Nickel-Immersion Gold

Principle: Rather than plate the entire exposed circuitry with ENIG, some applications, such as cell phones, employ selective ENIG. The other finish would be an OSP. The traditional metal finish on cellular phone circuit boards has been ENIG. Thanks to excellent conductivity and scratch resistance on the touch pad and connecting areas, ENIG has served the mobile phone market well for many years. However, too many metal layers on a solder joint (or SAC alloy) weaken it, and reduce the reliability of the component. If you have heard the phrase that the cell phone failed the *drop test*, this means that the phone was deemed non-functioning due to the drop causing a fracture of the solder joint of a critical component or components.

In order to make the Selective ENIG process work, a highly specialized photoresist that is able to withstand the aggressive nature of the ENIG process must be utilized. The OSP that is subsequently utilized to coat the exposed copper vias and pads, must be compatible with nickel and gold and must meet certain specific requirements:

- Must maintain solderability and enable excellent solder joint strength of attached components
- Must not degrade the nickel
- Must not deposit on the gold

Application: The chemistry required for the Selective ENIG (SENIG) process is very similar to the ENIG and OSP described previously. However, there are a few critical

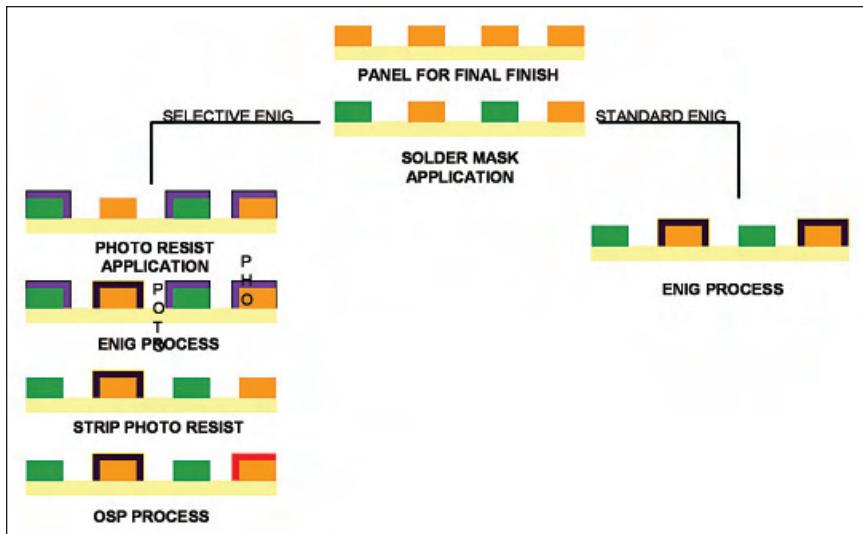


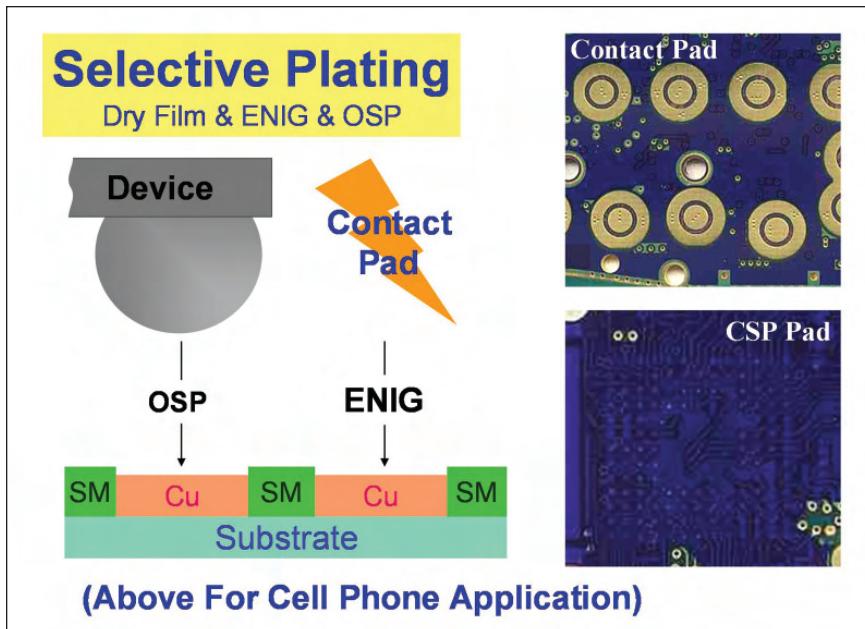
FIGURE 19: SENIG process flow

modifications. Modifications are made in the phosphorous content of the Ni to be more chemical corrosion resistant. The immersion gold is also modified to give a tighter, less porous deposit to better protect the underlying nickel during processing. The only other departure is the secondary imaging step to protect the pads and vias.

Limitations: The SENIG process (Figure 19) requires multiple processing steps and a specially formulated photoresist. The additional processing steps (i.e., a second resist lamination, expos, develop, and eventual resist stripping) may be cumbersome. However, the option of using a lead-free compatible OSP for the vias and pads provides significant benefits for both the cost structure and the solder joint, as seen in Figure 20

Hot Air Leveling

While Hot Air Leveling (HAL) has all but disappeared from the PCB scene, there remain pockets of fabricators who, for a

**FIGURE 20:** SENIG and OSP schematic

variety of reasons (customer requirements, military / aerospace, exemptions, etc.), continue to offer this process. The old adage, “nothing solders like solder” continues to pervade the industry. And HAL equipment and solder suppliers are offering lead-free hot air leveling (Figures 21 and 22). The unleaded versions include:

- Sn-0.3%Ag-0.7%Cu
- Sn-3%Ag-0.5%Cu
- Sn-0.7Cu + Ni

TABLE 4

ALLOY	MELTING POINT	PROCESS TEMPERATURE	PROCESS WINDOW
63/37 Sn/Pb	183° C	250° C (482)	67° C
Sn-0.7Cu+Ni	227° C	265° C (509)	38° C



FIGURE 21: Horizontal lead-free equipment

The latest versions include a nickel stabilized lead-free alloy. The main consideration when converting to lead-free hot air leveling is the melting point of the alloy (Table 4).



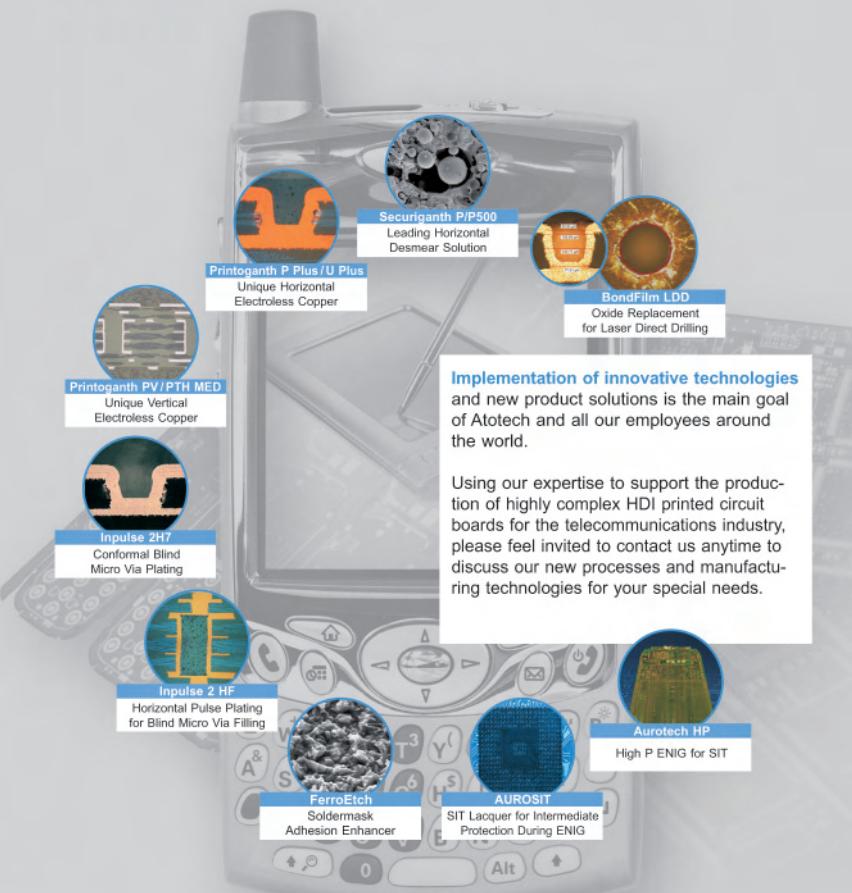
FIGURE 22:
Vertical hot air
leveling equipment
(Courtesy of Cemco)

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11

Electrical Test of High-Density Interconnects

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Introduction

HDI production yields are far from reaching 100% and a certain number of PCBs produced are necessarily faulty.

Since the addition of costly chips is the next assembly step, it is mandatory to have a final test, ideally just before shipping, to detect these faulty boards and to only deliver known good boards (KGB) to customers.

When you think about it, a PCB is nothing more than a complex cable with its main functionalities being electrical. It is therefore essential for the final test to be *electrically* performed.

Drivers for Electrical Test

There are several key factors that drive Electrical Test:

- Massive BGA/CSP/DCA technology adoption by the electronics industry → increasing density of interconnection → increasing density and number of test points
- Finer features → finer pitch capabilities for test systems and softer contact (or contactless) tests required
- Higher mix of products, smaller runs → higher impact of Non-Recurring Engineering (NRE) costs and more flexibility required for test systems

Electrical Test of High-Density Interconnects

- Buried passives → new test functionalities needing dedicated test systems

Let's illustrate these trends by a simple example (Figure 1). In the middle of the 1990s, complex HDI boards typically featured 300 I/Os / 16-mil peripheral pitch, on a 32 x 32 mm QFP footprint or 400 I/Os / 50-mil array pitch on a 25 x 25 mm BGA footprint. Today, complex HDI boards in production (such as IC package substrates and, in particular, FC-BGA or FC-CSP substrates) feature 15,000 I/Os / 150 µm array pitch, on a 20 x 20 mm footprint. This is 40 times more I/Os, just 13 years later, on a smaller footprint.

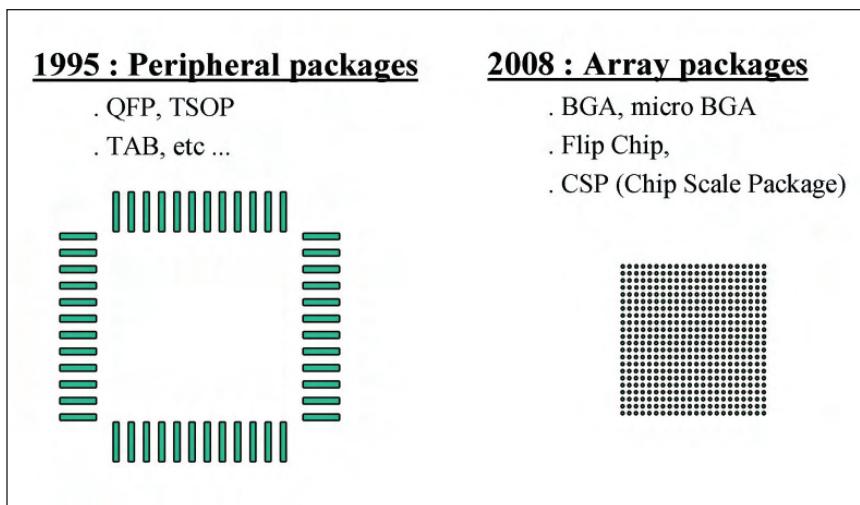


FIGURE 1: 1995 and 2008 footprints

Test costs are divided into two categories:

- NRE costs (data processing, fixturing)
- Operating costs (capital equipment, labor, insurance, real estate)

Fixturing (also called bed-of-nails or jigs) costs are drastically increasing, as an exponential function of board complexity, because of a number of trends (Figure 2).

The assembly industry has completed its migration from peripheral type packages (typically Quad Flat Packs or QFP) to array areas packages (typically Ball Grid Arrays or BGA). More than half of them have migrated from wire bonding to flip-chip interconnection. As a result, a non-linear increase of test point count occurs on fixtures, due to the corresponding increase of density.

There has been a decrease in the lifetime of products. Just a few years ago, the typical life of a product was two years. Today many cell phones have a life of less than six months. As a consequence, the relative cost of fixturing has dramatically increased in terms of the total area produced, because the fixture is paid off on fewer boards. Moreover, pin and probe costs become higher as they tend to become finer for more complex applications. Both of these trends severely impact test costs for one given part.

The inflation of test costs is also resulting because high volume production tester throughput is decreasing. Lower contact reliability due to the high complexity of the mechanical fixtures. Sometimes up to 20,000 pins are going through up to 40,000 holes. If only one hole fails, the contact can turn out to be unreliable and the test becomes uncertain, leading to retests and a significant decrease of throughput. As a consequence, smaller areas are tested per hour.

The capital-equipment cost of universal grid bed-of-nails-based equipment is increasing due to a higher number of test channels required to face higher densities. In summary, due to the explosion of fixturing costs, test costs are accelerating, while PCB selling prices are decreasing (Figure 2).

Electrical Test of High-Density Interconnects

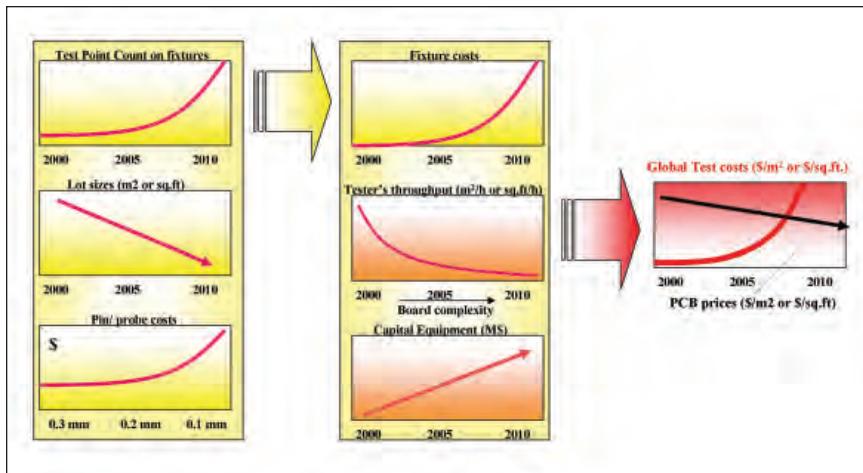


FIGURE 2: Fixture cost trends

What is Electrical Test Finding?

The goal of electrical test is to check that the complex cable (Figure 3) that is the PCB does not feature any opens, shorts, or leakage. It is necessary to access *all* its terminals (net ends), which are the footprint of the components to be assembled on the PCB later (Figure 4). If footprints feature dense and fine features, such as flip-chip areas, their test will require corresponding complexity.

Once boards under test can be probed in a reliable way (which is becoming more difficult), electrical test finds faults that give the test system measurements other than those programmed to be representative of a known good board. The

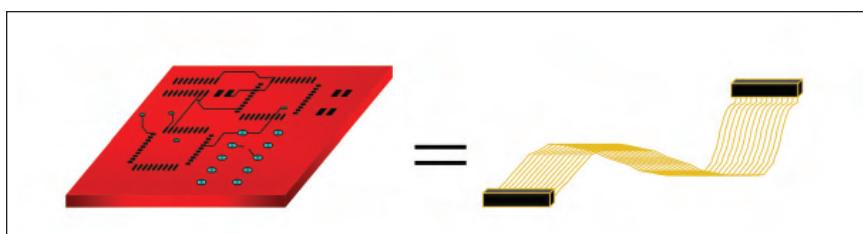


FIGURE 3: A PCB is nothing more than a complex cable

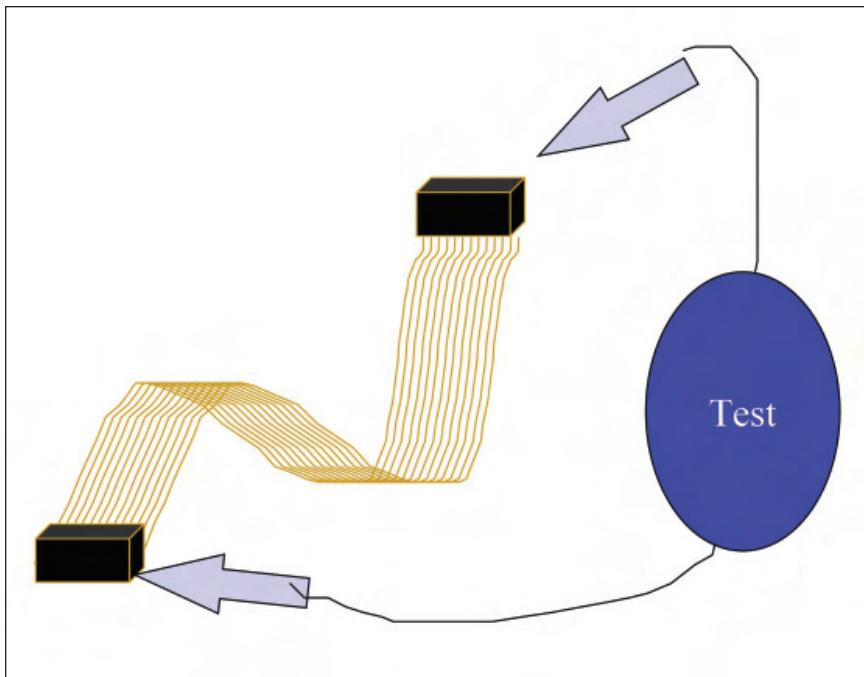


FIGURE 4: Testing a cable

faults measured may not necessarily impact the functionality of the substrate, but in most cases they will. The huge variety of substrate designs and applications make it difficult to make general statements about the end-result of a fault, especially if a certain fault type makes its way into a completely assembled end-product.

An electrical test investment will not ensure that all faults are found. The definition of *all faults* is too subjective. So far, electrical test systems cannot detect all faults related to annular rings, layer-to-layer registration, and other such defects that do not affect the test system-measurable interconnect.

Today's spectrum of generic faults detected by standard test equipment falls into three main categories: shorts, opens, and leakage (Figure 5).

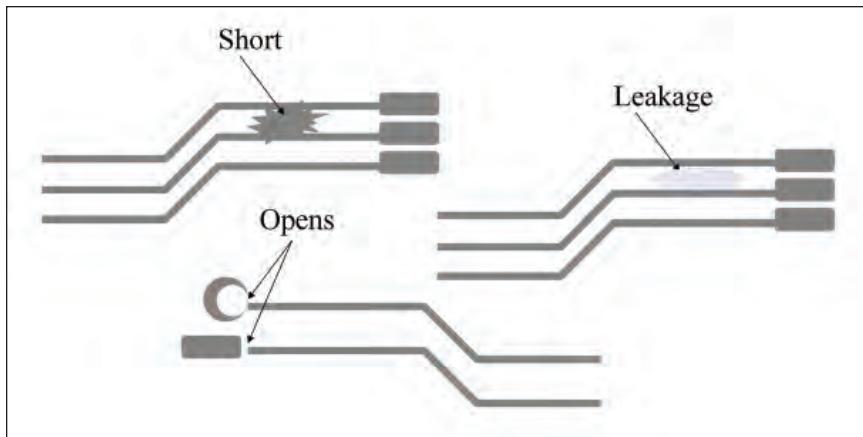


FIGURE 5: Opens, shorts and leakage.

Opens

An open is a discontinuity or non-connection within a network, so that the network is split or divided into two or more erroneous networks. Opens are produced in a variety of ways, including over-etching, under-plating, contamination, underexposure, and misregistration. The process for testing opens is called the continuity test. Depending on applications, the end user will ask for settings to be anywhere from a few hundred ohms to less than the one-ohm threshold.

It is important to mention that a 10-ohm threshold does not give more value than a 10-Kohm threshold. Trace resistance is usually much less than one ohm, while the contact resistance of a tester's probe can range from a few ohms to dozens of ohms. Only a 4-wire (Kelvin) measurement makes sense to set thresholds below 100 ohms, allowing one to disregard contact resistance from test results. When trace resistances are less than one ohm, 4-wire measurement only gives values for sub-ohm thresholds.

Shorts

A short is an erroneous connection between two or more networks, or isolated points, that should not be connected to each other. Shorts are produced in a variety of ways, including overexposure, under-etching, slivering, and solder leveling. There are many more sources for shorts, but these sources are most appropriate for a board fabrication discussion. Typically, the resistance of a frank short is a maximum of a few ohms. The process for testing shorts is called an isolation test. Depending on applications, the end user will ask for settings from a few Kohms up to more than a one-Mohm threshold.

Leakage

A leakage is a type of short, sometimes referred to as a high-resistance short, that is usually defined as a partial connection between two or more nets. The type of short exhibits a resistance value between the defined thresholds for acceptable continuity and acceptable isolation.

Common leakage sources are ionic contamination and moisture which are very closely related in the sense that both are contaminants and both exhibit conductive characteristics. Ionic contamination can occur at many stages in board fabrication (inner-layer, lamination, plating, solder mask, or manual handling) and is usually made up of metal salt deposits. Metal salts are typically conductive and may be widespread in a thin layer or on a circuit board. The resistive characteristic exhibited by this contamination can be a hard short, but is often a high-resistance short. With the addition of moisture, high-impedance short resistance will usually decrease, possibly deteriorating into a hard short. The nature of board materials is that they can absorb moisture easily. With a leakage path present on a board in operation, metal

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migration from one trace to another will further build the path into a hard short, which makes it important to find leakage faults before they make it into the end product.

The process for testing leakage is called a high-isolation test. Depending on applications, the end user will ask for settings from ten Mohms up to more than a 100-Mohm threshold. One Gigohm or more would be preferred, but it is rarely available on production testers.

Process feedback

The value of electrical test is not limited to detecting faulty boards. Combined with a statistical analysis of the defects, electrical test helps to optimize the production process. When it is observed that certain defects are repetitive, they can be identified as process related.

When is Electrical Test Required?

What products need to be tested? What percentage? When are substrates required to be tested? If the integrity of a given board is critical (military, aerospace, some automotive industry parts, which comprise a very small segment of the substrate manufacturing industry), then 100% test is mandatory, no matter what it costs (in theory).

In the majority of production processes, there is an acceptance that a certain number of boards shipped will be faulty. A substrate is required to be tested when overall test costs will account for less than the costs of no-test/scrap, combined at the following levels:

- bare substrates;
- assembly;
- field.

The added value of electrical test is simple. It saves money. The first area where money might be saved is on the factory floor. Testing provides feedback on the manufacturing process, helping to improve processes, increase yields, and decrease scrap. Testing also saves money on the assembly level every time an assembler does not mount components on faulty substrates (order of magnitude rule).

The corresponding test strategy will therefore depend on several variables:

- **Production cost of the board**
- **Test cost of the board (including repair)**
- **Process yield**
- **End-user requirements (how critical the substrate integrity is, cost of the final assembled product, and cost of components mounted on the substrate)**

It is important to note that the right test strategy should not be a decision made only by the substrate manufacturer. A choice should be made based on discussions between the fabricator and customer (OEM and/or EMS companies).

Let's consider some simple examples:

Single-sided consumer board (for example, remote control PCB)

- Production cost of the board: \$0.10
- Test cost per board: \$0.02 (20%)
- High yields: 99.9%
- Cost of components to be mounted, and assembled: \$5
- Critical substrate integrity: none

For this case, testing is not worthwhile. The process is under control, as indicated by the high yield. The cost of not

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testing is $0.1\% \times \$5 = \0.005 , while the cost of testing is $\$0.02$, four times the cost of not testing.

Six-layer buildup board (for example, cell phone)

- Production cost of the board: \$5
- Test cost per board : \$0.20 (4%)
- Low yields: 90%
- Cost of components to be mounted and assembled: \$20
- Critical substrate integrity: none

For this case, testing is worthwhile. With only 90% yields, the process requires adjustment. The cost of not testing is $10\% \times \$20 = \2 , while the cost of testing is $\$0.2$, ten times less than the cost of not testing.

Even if the test cost was twice the production cost of the board, it would, in theory, still be worth the cost. The reference here is not the production cost of the board, but the cost of the components to be mounted (with their assembly cost), and the bare substrate manufacturing yield. On the other hand, testing the same board at a much lower price would allow the systems house (OEM) to pay less while simultaneously increasing the fabricator's margin.

These examples illustrate the strategic border of electrical test, and its inherent value. End users and PCB fabricators agree on a threshold, which is typically measured in PPM (parts per million). End users accept PCB batches for which it can be proven, in the next assembly stages, that the number of faulty bare PCBs upon delivery did not exceed the number of PPM initially agreed upon.

The main goal of PCB fabricators is to define the right production and test strategies, in order to produce and test boards at the minimum price to make sure that the batches

delivered to end users do not exceed the PPM of faulty boards agreed upon (X) between the fabricator and the end user.

If Y is the production yield percentage, and E is the efficiency of Electrical Test to detect the number of bad boards as a percentage of total boards, then the fabricator has to make sure that :

$$(1-Y)(1-E) < X/10,000$$

If N is the number of good PCBs to be delivered to the end user, then what matters is how much it costs for producing and testing a batch of P boards ($P=N/Y$).

The PCB fabricator has to balance production and test costs, in order to reach the lowest possible cost for N boards, making sure that no more than X PPM are faulty boards among these N boards.

Please note that the efficiency of test equipment depends on the performance of the equipment itself (i.e., capability of detecting faults), as well as the list of test points (Netlist). If the Netlist is not defined to cover 100% of the possible defects, the test efficiency will rapidly decrease, regardless of the test equipment performance.

PCB manufacturers prefer to deal with relative test costs (percentage of the selling price of the board), rather than absolute test costs (dollar cost per square meter produced). They may accept spending more for testing more expensive boards. Just a decade ago, test costs rarely exceeded 1% of the selling price of the board. Today electrical testing can easily reach 5% of the selling price of an HDI substrate. Electrical test costs keep on increasing, while overall selling prices of PCBs keep on decreasing.

Top Three Parameters for Electrical Testing

An electrical test system will mainly be evaluated on its performance against three parameters:

1. **Fine-pitch and local density capability:** It should be able to probe very close attachment pads and dense designs, particularly array area package/flip-chip attachment pads.
2. **Low Cost of Ownership:**
 - a. High throughput (number of test points tested per second)
 - b. Low NRE/running costs because of shorter runs
 - c. Low Capital Equipment Expense – (Capex)
 - d. Fast setup capability and flexibility
3. **No mark**

It is also important to note that testing against data (Netlist downloaded into the tester) is an implicit requirement, which is actually standard for most new test equipment. Additionally, more and more passive / active components are embedded in HDI substrates. Dedicated test equipment is preferred to address corresponding tests, especially for capacitances and inductances. The same is true for Controlled Impedance tests.

Fine-Pitch and Local Density Capability

The pitch is the distance, center-to-center, between two traces to be tested (Figure 6).

On the most advanced IC package substrates, the array pitch can be less than 150 µm, center-to-center (typically 80 µm pad / 70 µm spacing). Some applications are currently [Y2008] designed with an array pitch of less than 100 µm and are anticipated to enter production within two years.

The density is the number of test points per unit of surface

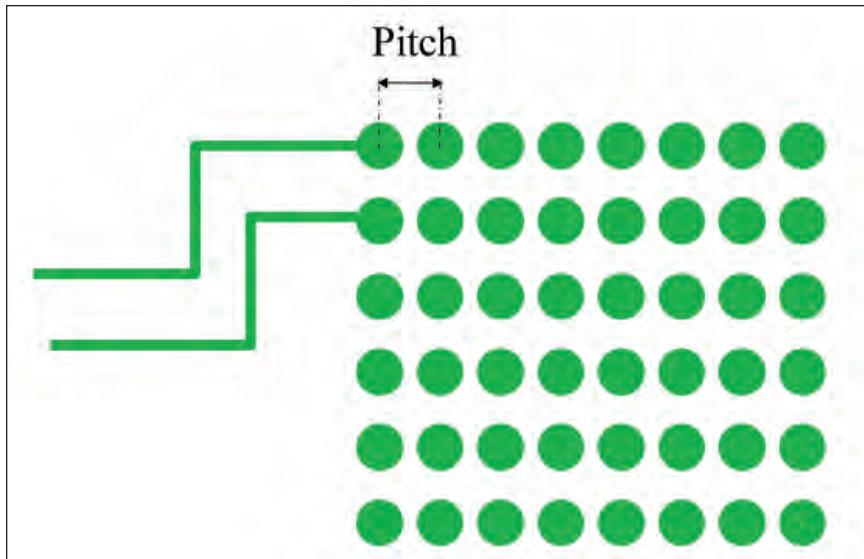


FIGURE 6: How pitch is measured

area. High-density substrates containing flip-chip arrays are very dense and extremely difficult/costly to probe using bed-of-nails/jigs. For example, a 1.27 mm pitch BGA offers a local density of 400 test points (TP) per square inch, which is the equivalent density of a high-density universal bed-of-nails grid. A 0.15 mm pitch FC area offers a local density of almost 30,000 TP per square inch, which is 75 times the equivalent density of a high-density universal bed-of-nails grid.

$$\text{Throughput} + \text{NRE/Running Costs} + \text{Capex} + \\ \text{Fast Setup Capability} = \text{Cost of Ownership}$$

- **Throughput:** Throughput refers to the productivity of the equipment. The faster a given board can be tested, the lower the cost, at least from a capital equipment point of view. The best parameter to quantify throughput is the number of test points per second the equipment is capable of testing. For instance, if a PCB has 1,000 test points, and the total time

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to fully test it (including opens, shorts, and leakage) is ten seconds, the throughput of the corresponding equipment will be measured as to 100 Test Points per second, or 100 TP/s.

Throughput is a very confusing parameter. It is highly linked to the test method used. For instance, the number of hits per second (number of times probes of the flying prober hit the board per second), often used to describe the throughput for flying probers, is not a throughput parameter. The only way to be objective is to use TP/s for a whole test.

- **NRE Costs:** NRE costs deal with fixturing/tooling costs (such as dedicated jigs/fixtures/bed-of-nails). Assuming a production cost of less than \$2,000 per board, a \$20,000 jig will be acceptable if it is paid off in testing one million boards (leading to a cost of \$0.02 per tested board), but will not be acceptable for testing 100 boards (leading to a cost of \$200 per tested board).

- **Running Costs:** Running costs are well known to PCB fabricators. They can include change pins/probes, engines of equipment, maintenance, etc. Running costs also include facility costs, such as power and air.

- **Capex:** Capex is a given amount of money that has to be paid when purchasing the equipment. The higher the Capex, the higher the hourly cost of the corresponding process, for the given lifetime of the equipment (typically five years).

- **Fast Setup Capability:** Most test equipment requires some setup time at the very beginning of the test of a new batch. It stops the equipment, thereby incurring a cost. Setup time must be as fast as possible, typically no more than a few minutes.

All these costs, in addition to the cost of real estate, operator, insurance, etc., lead to the concept of **Cost of Ownership** and the question of *what is the bottom line test cost of PCB?*

Because it is more accurate, we suggest using the unit of dollar cost/1,000 TP (how much it costs to test 1,000 test points), instead of referring to dollar cost/board (how much it costs per board).

Determining the bottom line test cost of a PCB is complex, because so many specific parameters have to be taken into account. The author of this chapter has developed a dedicated Cost Model, which addresses the main issues and parameters, in order to sense the range of test costs typically met in the industry. Figure 7 gives an estimation of the total test cost for 1,000 test points (Y axis), depending on the number of boards produced (X axis) for a given design, for an FC-BGA substrate, featuring 6,000 TP, for three test technologies.

The figure illustrates that flying probers (not using any fixtures at all) are not the cheapest solution for IC package substrates, regardless of the number of boards produced, hybrid probers are suited for small batches (less than 100,000

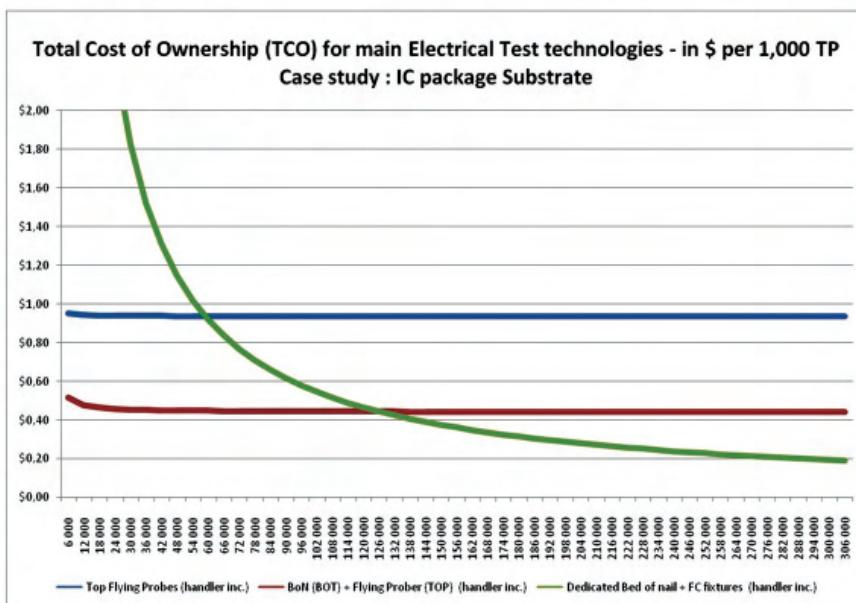


FIGURE 7: TCO for FC-BGA application

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boards produced), and dedicated bed-of-nails testers are suited for high volume.

In this example, for 125,000 boards produced, the total cost for testing a 6,000 TP FC-BGA is $\$0.40 \times 6 = \2.40 per substrate, which is very expensive compared to the price of \$6 to \$10 to the end user for this batch size. While the cost decreases with higher volume, using dedicated bed-of-nails, new test solutions are highly anticipated for small/medium batches of less than 200,000 pieces.

No Pad Damage

Figure 8 shows the impact of a pin on a test pad. At the present time no test technology can avoid marking test pads when testing complex HDI production, such as FC-BGA/FC-CSP. End users have been forced to accept it. End



FIGURE 8: Probe mark on a test pad

users generally accept marks if their overall size does not exceed 10% of the test pad area. However, as the test pad size decreases, while the test mark size is not in proportion, the time will come when the mark will exceed 50% of the test pad area, and as a consequence, will no longer be acceptable.

Electrical Test Requirements for HDI Production

Let's revisit our top three electrical test parameters, assigning some values for them today (Y2008), and five years from now (Y2013), for two main categories of applications.

Typical handset mother board (cell phone, PSP, etc.)

Minimum Pitch:

Today less than 0.3 mm, array

In five years, less than 0.2 mm, array

Cost of ownership : needs to go down

Marking:

Not an issue today

Still not a critical issue in five years

Typical IC package substrates (FC-BGA, FC-CSP, etc.)

Minimum Pitch:

Today less than 0.15 mm, array

In five years, less than 0.1 mm, array

Cost of ownership : needs to go down

Marking:

Not a critical issue today

A growing issue in the next five years

Ideal Profile for an HDI Substrate Electrical Tester

If we had to draw the lines of the ideal electrical test equipment for HDI substrates, it would be:

- 50 to 100 µm pitch capability (peripheral or arrays), for IC package substrate applications;
- no pad damage (off-contact, or very soft contact, still breaking oxidation layers or passivation when occurring);
- less than 10 Kohms continuity test, more than 10 Mohms isolation/leakage test;
- low cost of ownership, including:
 - fixtureless test technology for small/medium production (less than 200,000 boards), with a throughput of above 100 to 300 TP/s, depending on equipment price and running costs;
 - fixture allowed for high volume, if corresponding throughput is above 800 to 1200 TP/s, depending on equipment price, running costs, and fixture cost staying reasonable.

The HDI industry has several choices:

- Produce only in large volumes, in order to easily pay off expensive fixtures. However, the PCB industry does not control volumes. Only the market controls volumes, and the trend is actually to decrease the size of batches produced.
- Convince customers to pay for increasing test costs, which is never easy.

- Try to accelerate the emergence of low fixture cost technologies, with the ideal goal of fast fixtureless test technologies, provided that they can ensure high throughput (typically over 100 TP/s) and have fine pitch capabilities.

In other words, like imaging processes, tools/fixtures have to be eradicated in the next generation of equipment, except for very high volume manufacturing, where their cost may be justified because of their high throughput.

Electrical Test Technology Outlook

Bed-of-Nails Testers

What is an electrical bed-of-nails (universal grid or dedicated) electrical tester?

- One electronic part (several hundred electronic boards)
- One mechanical part (several ton press)
- One software part (fixture preparation and tester driving)
- One fixture part (bed-of-nails or dedicated) including from 1,000 to more than 20,000 test points

A new fixture is needed for every new kind of PCB to be tested. There are two different families of fixtures for bed-of-nails testers:

- Universal Grid Testers: fixtures are based on the use of *tilt* pins
- Wired or Dedicated Fixtures: time-consuming and expensive to build, but more reliable, faster and don't require a universal grid of electronic points, and much less expensive from a Capex point of view, because of the lower number of electronic tests point needed

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From an electronics point of view, universal grids and dedicated testers are very similar. They use modular electronic functions, called *electronic test points*, which are capable of reading or writing electrical stimuli (current, voltage) in order to check the interconnection between a given set of test points. The difference between the two bed-of-nails technologies lies in the fixturing method, which is to say that the electronics, or electronic test points, of the tester are physically interfaced with the PCB to be tested (the UUT).

Bed-of-Nails, Universal Grid-Based Testers

Universal grids or tilt pins fixture test systems are based on the use of a universal grid of electronic test points usually organized on a 2.54 mm down to 1.27 mm pitch array. They require the use of tilt pins fixtures as explained in Figure 9.

The cost of such fixtures starts from a few hundred dollars up to a few thousand. They are mainly used in Europe and in the USA:

Advantages:

- Relatively low fixture cost (compared with dedicated fixtures)
- Standard throughput of corresponding testers: between 500 and 1,000 TP/s, depending on complexity

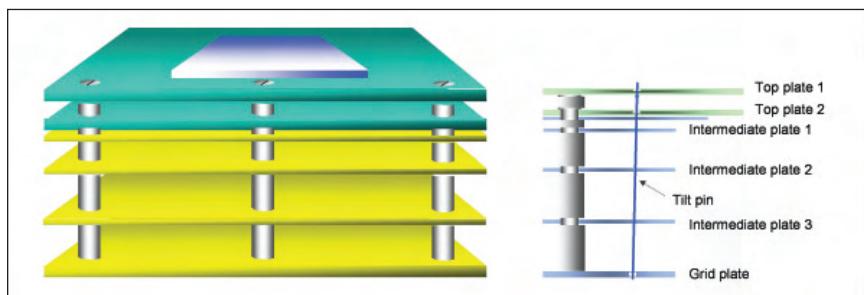


FIGURE 9: Universal grid bed-of-nails tilt pins fixture

Disadvantages:

- Pitch limited to 0.4 / 0.3 mm at an industrial level (if one wants to keep a reasonable throughput), for volume manufacturing
- Limited density capability with a practical limit of 0.5 mm pitch BGA or equivalent
- Less reliable for high volume throughput than dedicated testers
- Low throughput (< 500 TP/s) for advanced substrates, because of structural limits and reliability problems

A few years ago, quad density testers appeared on the market, with 1.27 mm pitch array. Priced between \$300,000 and \$800,000 (depending on total test point area on both sides), these testers cost a great deal more than dedicated systems. The reason for such high prices is the increase in density of the boards to be tested, and therefore the number of test points required on the grid. Ten years ago, the norm was 16,000 to 32,000 (total on both sides), and now it has expanded to more than 128,000 on quad density grids.

Bed-of-Nails Testers, Dedicated Fixtures

In the dedicated bed-of-nails fixture, the universal grid of contacts is replaced by connectors interfacing with the tester's electronics. The advantage lies in the fact that fewer electronic test points are required (the same number as the number of test points on the UUT), since their number is related mainly to the board density, not only to the dimensions of the board, (as would be the case for universal grid testers).

The main difference between dedicated and universal grids testers is that the electronic test points are not arranged in arrays, but are wired from an external box (the electronic

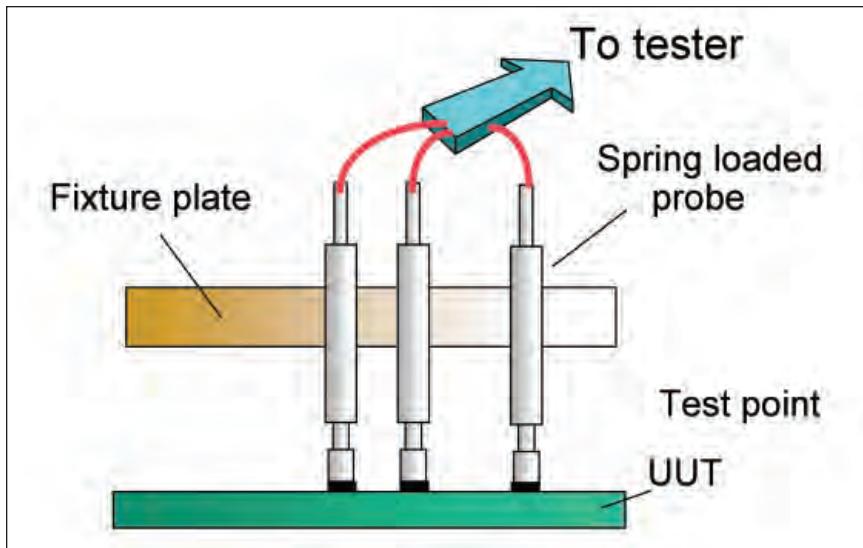


FIGURE 10: Dedicated bed-of-nails fixture principle

tester) to a dedicated fixture made of spring probes. This kind of fixture is more expensive, but generally more reliable for high volumes, and allows for higher productivity. In Asia and Japan, this kind of tester is in use by 90% of fabricators, because of the high volumes manufactured there.

Buckling Beam

For the most complex HDI applications, a fixturing technology called *buckling beam* (Figure 11), developed by IBM in the late 1970s and consisting of fixtures containing micro-wires, is used by the main players. The wires can be guided by the actuation of several plates down to fine pitches.

The buckling column (or buckling beam) problem was once investigated by a great Mathematician, named Euler. His investigations developed certain relationships that resulted in equations defining the bending or buckling of columns as a function of the loads placed on them. These mathematical relationships, when applied to spring wires, show that when

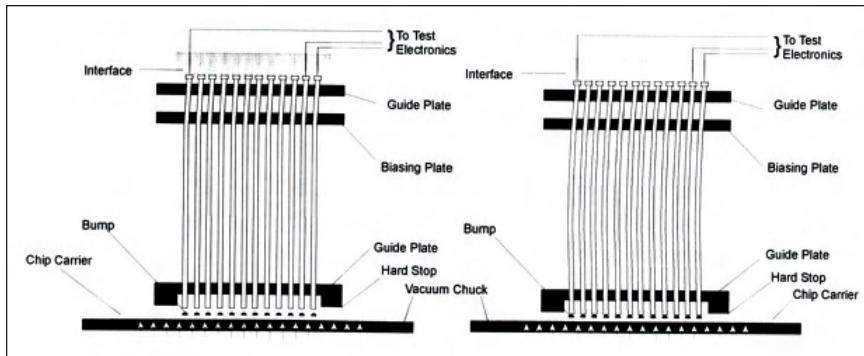


FIGURE 11: Buckling Beam Tester Principle

a force is placed on the end of a wire, the wire will bend and generate a spring force that is almost independent of the amount of displacement (or compliance) of the wire.

The force generated by a compression spring is a linear function of the amount of compression times the spring constant. In the case of buckling beam, most of the force generated by the buckling of the spring wire occurs during the start of the buckling action and is relatively independent of the amount of displacement (compliance). This factor has major significance in terms of touchdowns, contact force resistance, and scrub mark severity.

Scrub action is inherent in the design of the buckling beam. It is a controlled wiping action that is independent of overdrive. It is theoretically possible to achieve contact pitches as small as 150 microns, or less. Contact force is a function of the wire diameter. Therefore, if a high force is required (on the order of 25 grams), a wire diameter of 125 microns is normally used. If a lower contact force (10-12 grams) is acceptable or desirable, a wire diameter of 75 microns is used.

Advantages:

- Fine-pitch testing (down to 150 µm)

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- Reliable → High potential throughput (but severely limited by the number of electronic test points available for the test of HDI boards), typically 800 TP/s

Disadvantages:

- High fixture costs (between \$4,000 and \$70,000).
- Small size substrates only

Flying Probers

Flying probes (Figure 12), also known as moving probe systems or X-Y probers, are testers performing a *sequential* or semi-parallel access. A reduced number of points simultaneously contact the board to be tested, by a more or less consequent number of points, compared to bed-of-nail testers. A maximum of two to 16 probes simultaneously contact the board to be tested.

Flying probe testers are typically used to test prototypes. Their main advantage is that they do not use a fixture.

Mobile probes (at least two per side) move in (X,Y) to test point couples. For instance, the first probe sets a voltage, while the other one collects current. The system can then deduce the value for the measured resistance.

The flying prober is quite effective to test for opens (approximately 40 TP/s for dense HDI substrates) because they

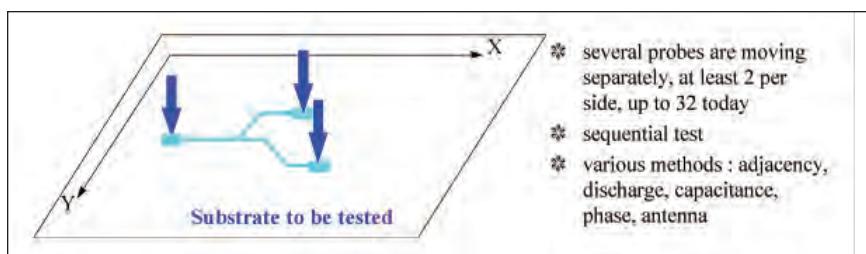


FIGURE 12: Flying Prober

are proportional to the number of connections. On the other hand, it is relatively slow for testing shorts, where insulation resistance must be measured between a connection and all the others, which implies a N^2 algorithm, where N is the number of networks. Some algorithms (adjacency method), using CAD data for statistically eliminating networks because of their distance compared to the network considered, make it possible to optimize the time taken, but slowness remains significant. It takes several minutes to test a board which has several thousand points.

Some other methods are also available, such as field measurement, discharge, capacitance, and phase difference. Taking advantage of alternative measurement methods gives a good idea of the isolation of a network, without having to access to all the networks to test the isolation of a single net. In this case, they perform the test by accessing each net only once, which avoids having to use adjacency.

Much more time is needed to test a unit area using flying probe testers, so they are generally dedicated to testing prototypes or small runs rather than high volumes. On the other hand, HDI boards are sometimes only testable by flying probers, because of their complexity (combination of fine-pitch and high-density):

- **Fine-pitch capabilities - flying probers are much better than tilt pin fixtures, 150 µm or less is OK**
- **Density capabilities - acceptable**
- **No fixture required**
- **Test time - from several minutes per board to more than one hour, depending on number of test points**

More and more, flying probes are using capacitance test methods or the equivalent, which makes the test a true parallel

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test, while not being a real resistance measurement test. This method is very effective for high TP count boards.

Advantages:

- Very effective for fine-pitch boards with a limit of between 100 and 150 μm
- No fixture needed

Disadvantages:

- Low throughput (typically 5 to 10 TP/s for complex HDI applications, such as IC package substrates)
- Pad damage still possible, even if much safer in this regard than bed-of-nails testers.

Flying probers are well-suited to small volumes of medium complex HDI substrates, such as handset PCBs. For leading edge HDI substrates, produced in small/medium volumes (such as FC-BGA / FC-CSP), hybrid probers are preferred over flying probers for cost of ownership reasons.

Hybrid Test Technology

Hybrid probers (Figure 13) are mainly dedicated to the test of small/medium volumes of IC package substrates, such as FC-BGA/FC-CSP. They combine two technologies:

- Dedicated bed-of-nails / jig technology, to probe the BGA land side of IC package substrates (typically a few hundred pins, 1.27 mm pitch), which is neither complex nor expensive
- Flying Prober (two probes max) for probing the flip-chip side, typically 180 μm pitch /5,000 TP

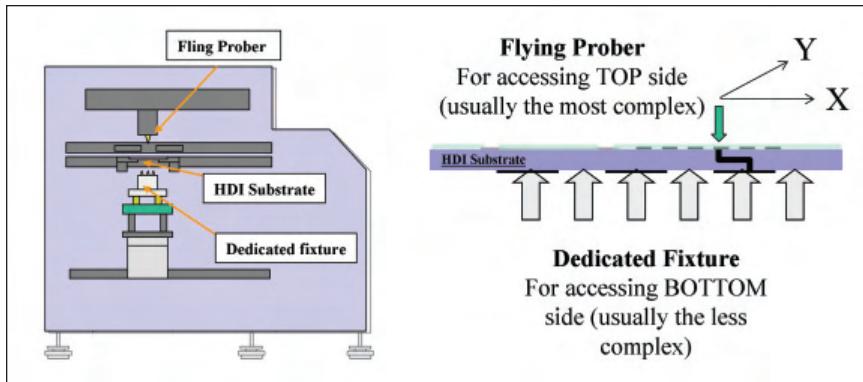


FIGURE 13: Hybrid test technology

Hybrid probers' throughput typically reaches 25 to 30 TP/s, compared to 5 to 10 TP/s for flying probers and 800 TP/s for bed-of-nails, for the same application.

Advantages:

- Efficient for special designs, in small volumes, such as IC package substrates.
- Higher throughput than Flying Probers, resulting in lower cost of ownership.

Disadvantages:

- Mainly dedicated to IC package substrate test
- Still requires a bed-of-nails for the bottom side, which tends to become more complex (pitch going down to 0.3 mm for FC-CSP applications) and features more and more I/Os

Sensor technology

Sensor technology (Figure 14) was mainly dedicated to the test of P-BGA (bonding attachment) IC package substrates. It combines two technologies:

Electrical Test of High-Density Interconnects

- Dedicated bed-of-nails / jig technology, to probe the BGA land side of IC package substrates (typically a few hundred pins, 1.27 mm pitch), which is neither complex nor expensive
- Capacitive coupling for probing the bonding side in a non-contact way

A capacitive sensor *senses* an alternative signal injected into a BGA land by the bottom bed-of-nails. If the signal is sensed on the bonding pad on the other side, it means that there is no open. Isolation can be tested by the bed-of-nails on the bottom side, because of the specific design of such substrates (two test point Nets; one on the bonding side, one on the BGA land side).

Advantages:

- Fine peripheral pitch testing (down to 80 µm)
- Fast

Disadvantages:

- Not compatible with an array of test points → not compatible with flip-chip designs
- Medium fixture costs

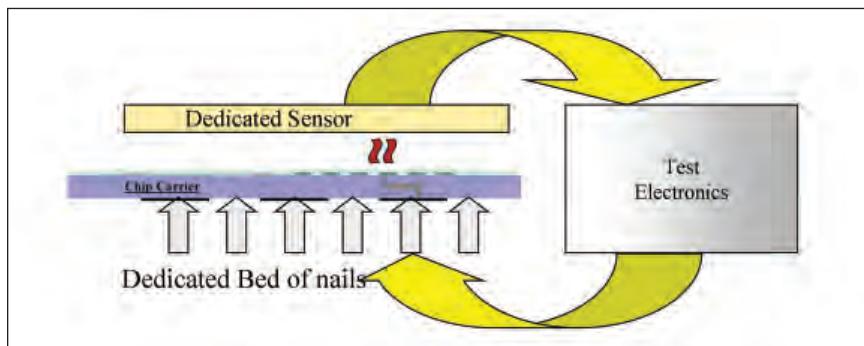


FIGURE 14: Sensor technology

Sensor technology has been progressively given up, as P-BGA production is progressively replaced by FC-BGA / FC-CSP.

Emerging Test Technologies

In the past, we have witnessed a few attempts to develop radically new test technology, mainly non-contact oriented. It is useful to mention:

Electron-Beam (E-Beam) Testers:

The focused electron beam can be positioned on different pads of the substrate using an electromagnetic deflection system which works similarly to the scanning beam in a CRT. In addition, the beam can be switched on and off by a blanking system in order to form charges and read pulses. A read pulse is formed by switching the beam on for a short time. During this time the beam generates secondary electrons at the location where it is positioned. The voltage contrast detected by collecting these secondary electrons allows for discrimination between charged and uncharged pads.

E-beam technology was originally developed by IBM in the late 1970s. So far, it is not available on the market. It has not become a fully operational product for PCB testing applications. Though development has never really stopped, there are two main sub-technologies that have met with positive results. These two technologies are known as the voltage contrast method and the switch grid potential method. Only the switch grid potential method seemed able to address PCB industry testing requirements.

E-Beam Switch Grid Potential Method: The corresponding test principle is very similar to capacitance

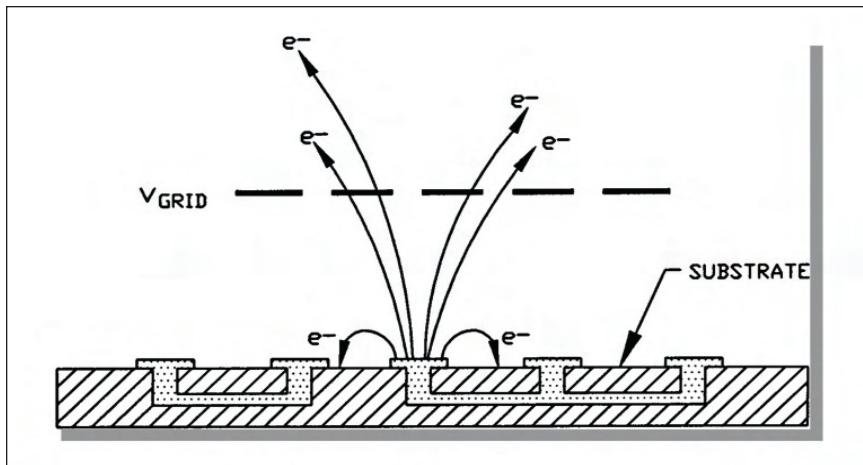


FIGURE 15: Switch grid potential method of testing uses an electron beam to change the charge on a net detecting its capacitance

measurement. The following are steps used in the switch grid potential method (Figure 15):

1. The test area is divided into sectors, for instance 2" x 2" each. The electron beam has to cover only an area of 2" x 2". The electron beam is used to scan over that surface and register the target. This takes into consideration misalignments caused by the changes in the positioning of the tested substrate (the X-Y stage, the shrinkage of nets, etc.)
2. The electron beam hits a pad while the extract grid is maintained at a positive potential (typically +10 volts). Because the beam is landing at one keV of energy and the secondary emission yield is greater than one, the pad will eventually reach an equilibrium more positive than the extract grid (typically 12 volts). While it lands on the same pad, the extract grid is switched to a negative potential (typically -10 volts). The pad will now charge negatively until, at equilibrium, it reaches a negative potential less negative than the extract grid potential (typically -8 volts). The speed with which the pad changes from one state to the other greatly depends upon

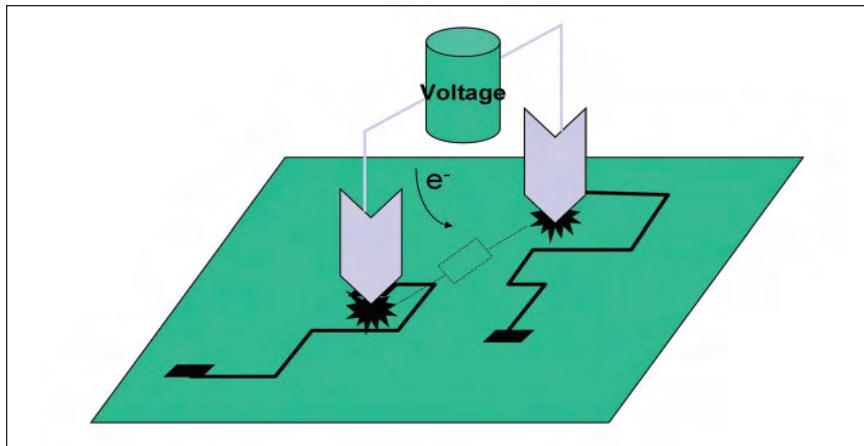


FIGURE 16: Short testing using the ignition of local plasma at two points on a substrate, close to two corresponding test points

the capacitance of its net. Any net that is open or shorted will have a substantially different capacitance than that of a corresponding defect-free net. Therefore, this measurement will show the presence of opens and shorts.

Plasma discharge: This technology deals with the ignition of a local plasma at two locations on a substrate, close to two corresponding test points (Figure 16). The plasma might be ignited by a laser beam or by a high-voltage discharge, which operates at normal temperature and pressure conditions. At this moment, the electrons of the inert gas (typically Argon) are released. Next, a voltage drop is applied between the two test points, allowing electrons to circulate and closing the electrical path with the resistance to be measured. The plasma probes are moving on an X-Y stage, like flying probe testers. Testing is made on the fly. Fixtureless plasma discharge probe testers are not capable of extremely fine-pitch testing (pitch typically has to be > 250 microns or 10 mils). Throughput is perhaps the most important issue that

Electrical Test of High-Density Interconnects

this technology has tried to addressed. Two companies were developing this technology; Exsight (Israel) and Probot (USA). Only Probot reached the market, but has sold small quantities of equipment.

Photo-electric effect: A first generation of equipment was developed in the late 1990s named Controlled Electron Migration. The concept was to try to take advantage of the photo-electric effect discovered by Einstein. Electrons can circulate from a metallic pad, illuminated by a UV light source, to a collecting plate biased at a suited voltage. Electrons are emitted and measured under the impulse of a high-frequency laser beam. This technology is non-contact and fixtureless (Figure 17). Ultra-fine-pitch testing was claimed to be potentially achieved using controlled electron migration (down to 75 microns). Not only is the method fixtureless, it is also contactless. Claimed throughput was relatively high. This project was stopped in the early 2000s.

Recently, a European company has developed a second generation of photo-electric tester, mainly dedicated to IC package testing. During the 2008 CPCA show, they announced

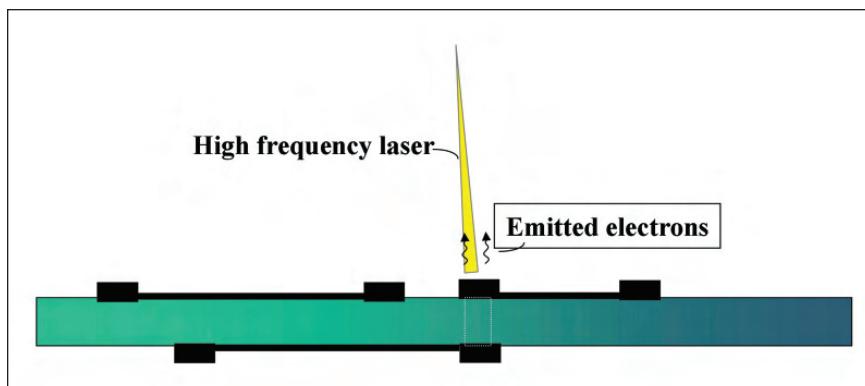


FIGURE 17: Non-contact, fixtureless photo-electric effect testing

that their Laser Direct Testing technology was now ready, and that they had already successfully passed sampling stages with major IC package substrate manufacturers. Based on the publications and interviews given by this company, they claim to have 100% non-contact technology able to probe fine-pitch designs (less than 100 µm array pitch) with higher throughput than hybrid probers. Laser Direct Testing would make a good challenge for testing high IC package substrates, if the manufacturer's statements are confirmed on the factory floor.

Conclusion

Testing HDI substrates is not easy. It requires a lot of know-how and expertise. Good test technologies are available, but new technologies being developed are expected to combine higher performance with lower cost of ownership. It is probably the segment of production where an intelligent strategy could save the most money and increase profitability the most.

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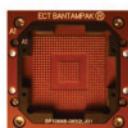


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12

Quality, Acceptability and Reliability

By Happy Holden — *Mentor Graphics*

Standards and References

The very nature of microvias' small size makes the acceptability criteria difficult to define. Most HDI Quality and Acceptability requirements are still OEM-defined. The IPC has IPC-6016 as part of the IPC-6011, the generic Qualification And Performance Specifications (6010 Series). These specifications only cover the buildup HDI layers and not the core, which is covered by its own IPC specifications.

IPC-6016 - Qualification and Performance Specification for High-Density Interconnect (HDI) Structures

IPC-6016 contains the general specifications for high-density substrates not already covered by other IPC documents, like IPC-6011, the generic PWB qualification and performance specifications. The acceptance criteria for HDI layers are organized into five slash sheet categories:

- Chip Carrier
- Hand-held
- High Performance
- Harsh Environment
- Portable

Quality, Acceptability and Reliability

The acceptability requirements are broken down into these 12 separate specifications:

- **Section 3.1:** General
- **Section 3.2:** Materials
- **Section 3.3:** Visual Examination
- **Section 3.4:** Dimensional Requirements
- **Section 3.5:** Conductor Definition
- **Section 3.6:** Structural Integrity
- **Section 3.7:** Other Tests
- **Section 3.8:** Solder Mask
- **Section 3.9:** Electrical Properties
- **Section 3.10:** Environmental Requirements
- **Section 3.11:** Special Requirements
- **Section 3.12:** Repair

Quality Control

Microvia Quality

Microvias are nearly impossible to inspect visually and extremely difficult to cross-section, which necessitates a more indirect approach to verification of proper fabrication. Proper microvias, as seen in Figure 1 (a-d), can be distinguished from defective microvias, as seen in Figure 2 (a-d), by using the Copyrighted CAT [1] coupons on production panel borders. These coupons are the same as those used in IPC-9151 and correlate to a statistically measured via-chain resistance and highly accelerated thermal-cycling tests (HATS).[2] The criteria for quality microvia production are no more than 50 defective microvias per million microvias and a covariance of the standard deviations of the daisy-chain Kelvin resistances of 5%.

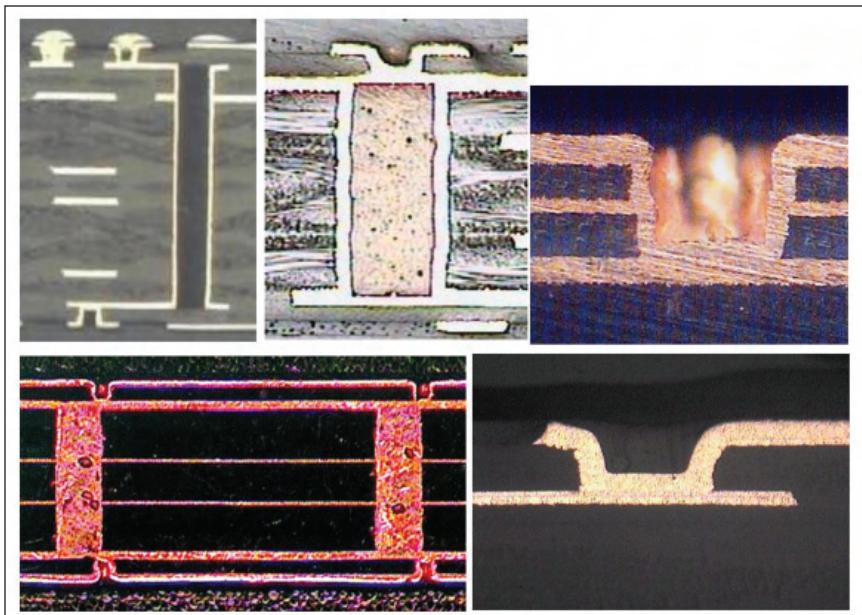


FIGURE 1: Five cross-sections of good microvias, showing the uniformity of the plating with no occlusions, voids, or skips

Via-In-Pad (VIP)

In a few cases, assemblers may have difficulty with the microvia-in-pad design approach.[3] Technical papers published by OEMs that have used microvias and VIP technology indicate that a finer-mesh solder-paste should be employed and that OSP, HASL, and Immersion Silver are the preferred final-finishes for the bare board. One alternative solution is to specify a *flat microvia pad*. There are four alternative methods to accomplish this, three of which are fabricator-controlled and add extra cost. The four *flat pad* filling processes are seen in Figures 3. The advantages of *flat and filled* microvias are ease of assembly and more copper to carry current and heat.

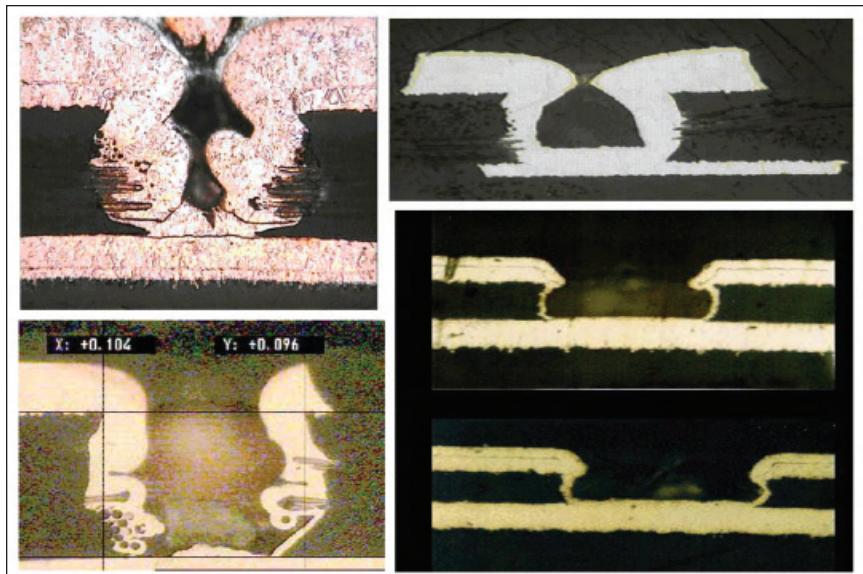


FIGURE 2: Four cross-sections of defective and rejected microvias[3]

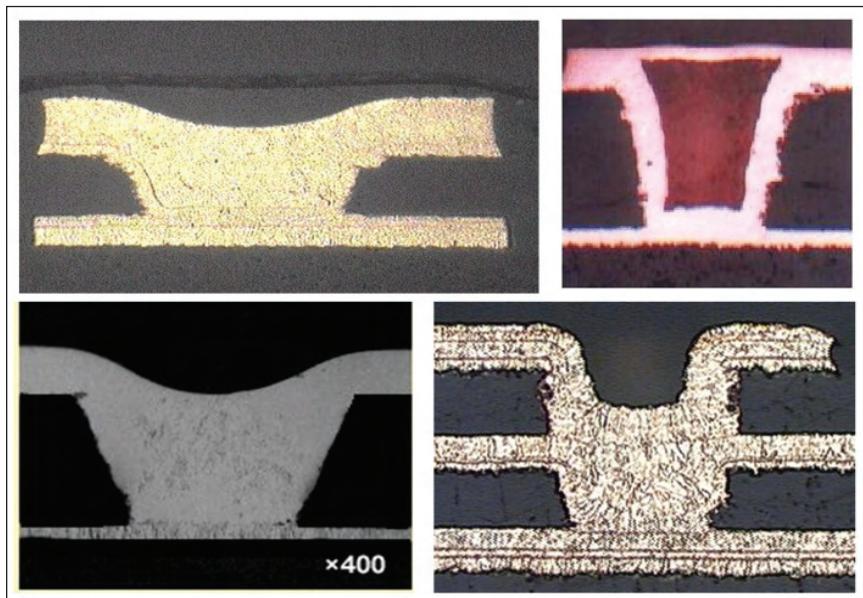


FIGURE 3: These four microvias are properly drilled, filled, metallized, and plated and show (a) surface plane flood (GND) designed with panel and pattern plating metallization; (b) microvia non-conductive fill and plating cap; (c) effect of specialized copper plating baths with normal DC plating; and (d) effect of pulse plating with periodic reversal but using normal copper plating baths on stacked blind vias.

Laser Drilling Quality

The quality of laser drilling of microvias illustrates the nature of the failure modes in microvias. Figure 4 shows the seven main quality criteria for laser microvias, along with the quality criteria specifications, measurement methods, sample sizes, and control limits.

Yields

PCB process lot yields, like other thermodynamically linked processes, do not follow normal manufacturing yields. As seen in Figure 5, the yields for a part number or groups of part numbers are grouped in the high 80s to 90% but have a long tail of lower yields. This is what is called a *gamma distribution*. It is not a *normal distribution*, as shown, because yields are not normal.

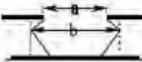
Item	Spec	Measurement	Sample Size	Control limit
1. Overhead	 Class A: $a / b \geq 0.95$ Class B: $a / b \geq 0.90, a / b < 0.95$ Class C: $a / b < 0.90$	Cross section inspected by microscope	1. first piece of Per Part 2. one of per 10 lots	$a / b = 0$ $a / b \leq 0.9$
2. Roughness	 Class A: $R \leq 0.1 \text{ mil}$ Class B: $R \geq 0.1, R \leq 0.5 \text{ mil}$ Class C: $R > 0.5 \text{ mil}$	Cross section inspected by microscope	1. first piece of Per Part 2. one of per 10 lots	$R = 0$ $R \leq 0.5 \text{ mil}$
3. Taper angle	 Class A: 5° Class B: 10° Class C: 15°	1. Cross section inspected by microscope 2. Z-check	1. first piece of Per Part 2. one of per 10 lots	$\theta = 0^\circ$ $\theta \leq 20^\circ$
4. Voids	 Class A: No Voids Class B: Voids	Cross section inspected by microscope	1. first piece of Per Part 2. one of per 10 lots	No Voids
5. Wicking	 Class A: $L \geq 0, L \leq 0.1 \text{ mil}$ Class B: $L > 0.1, L \leq 0.5 \text{ mil}$ Class C: $L > 0.5 \text{ mil}$	Cross section inspected by microscope	1. first piece of Per Part 2. one of per 10 lots	$L = 0$ $L \leq 0.5 \text{ mil}$
6. Resin remains	 Class A: $t \geq 0, t \leq 0.2 \text{ mil}$ Class B: $t > 0.2, t \leq 0.5 \text{ mil}$ Class C: $t > 0.5 \text{ mil}$	Cross section inspected by microscope	1. first piece of Per Part 2. one of per 10 lots	$t = 0$ $t \leq 0.5 \text{ mil}$
7. Cracks	 Class A: No Cracks Class B: Cracks	Cross section inspected by microscope	1. first piece of Per Part 2. one of per 10 lots	No Cracks

FIGURE 4: Seven main quality criteria for laser microvias, along with the quality criteria specifications, measurement methods, sample sizes, and control limits

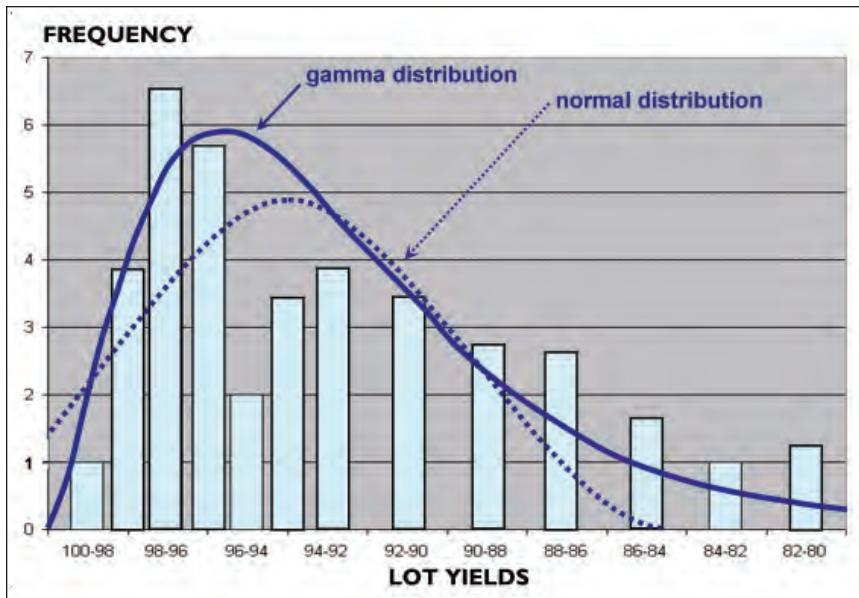


FIGURE 5: The lot yields for a part number or group of part numbers are grouped in the high 80s to 90% but have a long tail of lower yields. This is a gamma distribution and it is not a normal distribution.

The calculations of mean and standard deviation must be done differently. Using the normal mean and standard deviation results in yields over 100% or under 0% which is clearly not possible.

First Pass Yields

In Chapter 3 – Design of Advanced Printed Circuits, Equations 6 and 7 define first pass yield (FPY) and PCB producibility. To determine the constants A and B in Equation 7 of that chapter, any statistical software program [4] that has a model-based regression analysis function can be used. The model is shown in the equation below:

$$\text{Yield} = f[x] = 100 \div \text{EXP}\{\text{LOG}(\text{Complexity Index} \div \text{PARM[1]})^{\text{PARM[2]}}\}$$

Where: PARM [1] = A

PARM [2] = B

These are the Fabricator Capability Coefficients (FCC) Indexes

The first pass yield will follow the examples in Figure 6. Constant B determines the slope of the inflection of the yield curve and Constant A determines the x-axis point of the inflection.

Alternatively, any spreadsheet can be used to determine constants A and B. The [REGR] function in a spreadsheet program like Excel or Lotus 1-2-3 is often used. The [REGR] function is defined as: [=LINEST (known_Ys, known_Xs, TRUE, TRUE)]. To use this function, you must first put the FPY function into the form $Y=AX+B$. This is done by creating four columns:

- (1) Complexity Index that we will call X1
- (2) Yield called Y
- (3) $\{\log [\log (X1)]\}$
- (4) $\{\log [\ln (-Y/100)]\}$

Provide the regression function with column 4 as *known_Ys* and column 3 as *known_Xs*. The last four columns are the FCC fitted results and their errors using the given Complexity Index. From the sums, the average error is only 0.4% with a standard deviation of 4.4%.

The regression function will return ten values: *FIT* (slope and intercept); *sig-M* (slope and intercept); *r2*, *sig-B* (slope and intercept); *F,df* (slope and intercept); and *reg sum sq* (slope and intercept). The constant B is equal to the *FIT* (slope) and the constant A is $10^{[-FIT(\text{intercept})/FIT(\text{slope})]}$. The regression analysis of AVG ONLY is the fit when providing only the Average Yield rather than all of the data.

In order to calculate an array, remember to:

- **highlight the array on the spreadsheet;**
- **type the array formula, making sure the cursor is in the edit bar;**
- **press CTRL + SHIFT + ENTER.**

Figure 6 shows all the original data and the resulting FCC. High variability of closely spaced Complexity Indexed boards indicates poor process control or operator training. The variability in yield can often be explained by applying the classical *Learning Curve* mechanism, that is, the yield improves after a number of manufacturing runs.[5] If that is the case, then two FCCs need to be kept, one for *Early Runs* of a part and another for *Mature Parts*, after the learning curve has kicked in. High variability of a single part number (P/N) indicates poor process control, operator training, or a Complexity Factor not used in Chapter 3 - Equation 6, like HDI blind vias. In this case, a Z-Factor should be added to

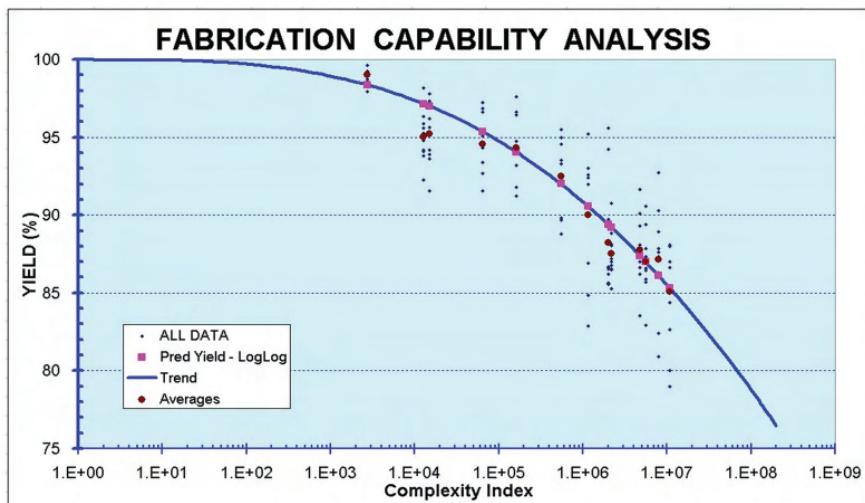


FIGURE 6: Yield predictions for the Fabrication Capability Coefficient curve and raw data of FPY from electrical test

Chapter 3 - Equation 6. This is a good justification for running Parametric Panels like PCQR².[6]

Statistical Methods

The Need For Statistical Tools

The discussion of quality and yields, including FPY, show how important yields are to HDI boards. Any loss goes to the bottom line. So what are some of the tools to help improve process yields? Process control comes to mind. Chemical processes have always been difficult to control in printed circuits. These uncontrolled factors can always creep into our processes.

All process control is a feedback loop of some sorts. Nevertheless, the element that I want to focus on is the *control* block, or more precisely, the *human decisions* that make up process control. Process Control and Process Automation will be two additional chapters addressed in future HDI Handbook Revisions.

Process Control

The first link in process control is the human link. The high level objectives are to:

- **reduce variations;**
- **increase first pass yields;**
- **reduce repair and rework;**
- **improve quality and reliability;**
- **improve workmanship.**

There are a variety of process control tools and methods that a person may have to work with:

- **Pareto Charts**
- **Cause and Effect Diagrams**
- **Multi-Vary**

Quality, Acceptability and Reliability

- Design of Experiments
- Process Optimization
- Control Charts
- Process Capability Indices (Cp, Cpk)
- PPM
- Six Sigma

Traditionally, statistical tools have been rather cumbersome and difficult to learn. I have good news for you! You can now get good statistics training from the WEB, and at a bargain price – *FREE!* Of particular importance for the engineer are the statistical tools, as seen in Figure 7.

The NIST/SEMTECH e-Handbook of Statistical Methods

I have just discovered a great statistics handbook on the Web. I was looking for Wiebull Reliability Plot information and the *SEMTECH/NIST e- Handbook of Statistical Methods*

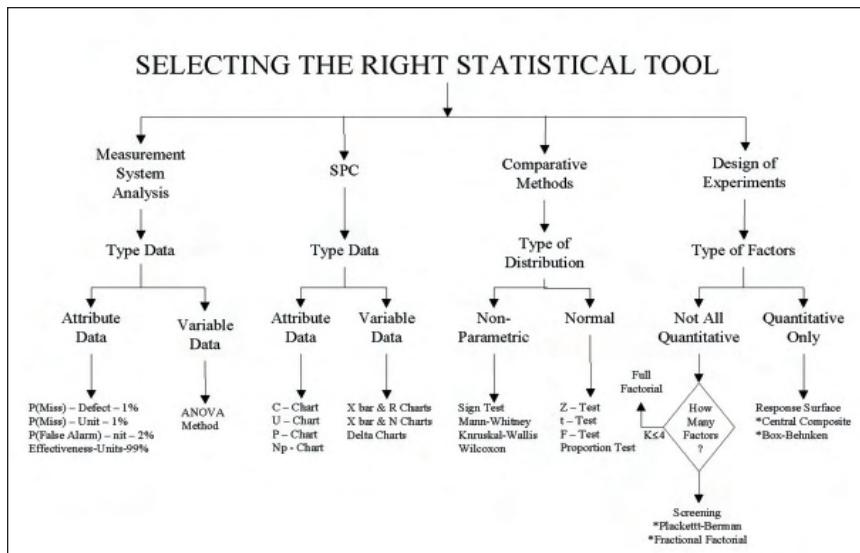


FIGURE 7: Four main techniques for selecting the right statistical tool for problem analysis

The HDI Handbook

(EHSM) popped up (www.itl.nist.gov/div898/handbook/). After playing with it for a while, I discovered that it was perfectly designed just for *process engineers*. The organization of the handbook follows the statistical tools that a process engineer would need to ferret out a problem, measure the extent of the problem, look for root causes, uncover how many factors are involved in the problem, postulate a solution, verify the solution, and then monitor the process to be sure the problem is gone and does not reappear. These eight stages are the main chapters of the EHSM and can be seen in Figure 8.

The usefulness of the EHSM comes from the experimental data sets it supplies (case studies). As you read the handbook, it encourages you to make statistical comparisons with its statistical tools. It does this by supplying a *complete statistical software program* for you to use! When used with the data sets

The screenshot shows the homepage of the NIST SEMATECH Engineering Statistics Handbook. The top navigation bar includes links for HOME, TOOLS & AIDS, SEARCH, and BACK/NEXT. Below the navigation is a header for "Engineering Statistics Handbook" with a URL link. A sidebar on the left contains sections for "HANDBOOK CHAPTERS" (listing 1-8), "HOW TO USE HANDBOOK", "TOOLS & AIDS" (which is circled in red), "SEARCH HANDBOOK", "DETAILED CONTENTS", "ACKNOWLEDGMENTS", "Select TOOLS & AIDS", "Select '10.Statistical Software'", and "Select 'Dataplot' to download". The main content area displays a table of contents for the "Handbook Chapters". The chapters are numbered 1 through 8, each with a list of sub-sections. The "TOOLS & AIDS" section is highlighted with a red circle.

Handbook Chapters	http://www.itl.nist.gov
1. Explore	2. Measurement Process Characterization
2. Measure	3. Production Process Characterization
3. Characterize	4. Process Modeling
4. Model	5. Process or Product Monitoring and Control
5. Improve	6. Assessing Product Reliability
6. Monitor	7. Product and Process Comparisons
7. Compare	8. Uncertainty Analysis
8. Reliability	1. Introduction
	2. Assumptions
	3. Techniques
	4. Case Studies
	1. Introduction
	2. Assumptions
	3. Data Collection
	4. Data Analysis
	5. Interpretation & Use
	6. Case Studies
	1. Introduction
	2. Comparisons: One Process
	3. Comparisons: Two Processes
	4. Comparisons: Three+ Processes
	1. Introduction
	2. Assumptions/Prerequisites
	3. Reliability Data Collection
	4. Reliability Data Analysis

FIGURE 8: TSEMTECH/NIST e-Handbook of Statistical Methods available over the Internet[4]

Quality, Acceptability and Reliability

supplied, it can then coach you through the interpretation of the results. You can then substitute your own data and look at the results. The *first we run the demo – then we run your problem* method is a very effective way to coach a person through the use of statistical tools.

To download DATAPLOT, simply click on TOOLS & AIDS and navigate from there. Or you can link from here directly to the *download page* (www.itl.nist.gov/div898/software/dataplot/). NIST has prepared versions of the software for most operating systems, including Windows, NT, LINUS, UNIX, MAC OS, etc. It is a bit large, but the download time is worth it.

Modern High Speed Processes

There are many processes with which to use these statistical tools such as the plating of HDI-Microvias. Figure 4 in Chapter 10 - *Electrodeposition and Solderable Finishes for HDI* shows a Parameter Influence Chart for a modern high-throw acid copper-plating bath. As key parameter characteristics go up, they have various effects on the characteristics of the copper plating. Of course, many of these parameters have interactive effects. This is where the statistical tools come into play.

Design Of Experiments

Design of Experiments or DOE is one of the most powerful and influential engineering tools for HDI yield improvements. *Experimentation* is the manipulation of controllable factors at different values to see their effect on some desired result. An engineer can use three Methods of Experimentation:

- Trial and Error
- One Factor at a Time
- Factorial Design

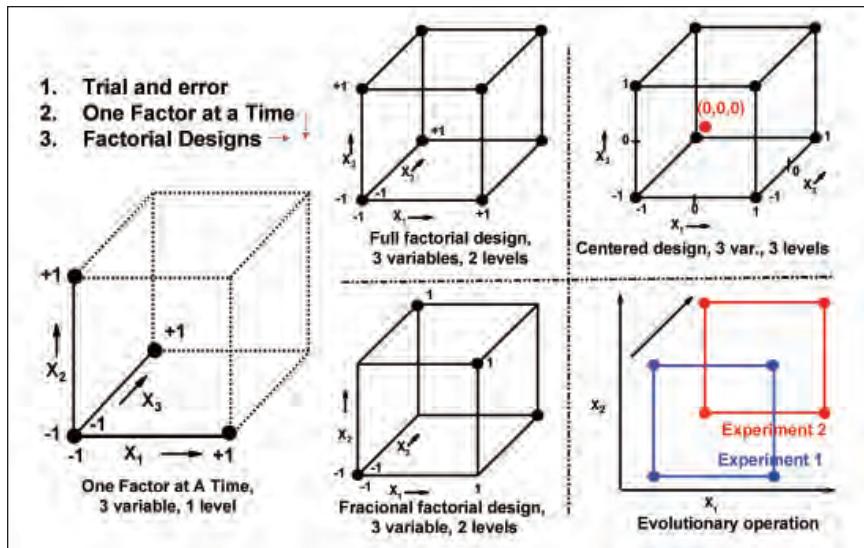


FIGURE 9: Design of Experiments (DOE) is much more comprehensive and effective than Trial and Error or One-Factor-at-a-Time methods. The DOE software can be found in The NIST/SEMATECH e-Handbook of Statistical Methods available over the Internet.

Figure 9 shows the One-Factor-at-a-Time and the Factorial Design methods of experimentation.

The next two figures show four different PCB process DOE results. The first, in Figure 10, is an experiment to minimize the shifting of inner-layers in multilayer lamination. The variables and levels were a full factorial design of three variables at two levels:

- Vented panel borders: with venting and without venting
- Tooling methods for lay-up: 1/4 inch holes and four centerline 1/8 inch slots
- Lamination pressure: 294 PSI and 344 PSI

The results are the image shift in microns. The lowest shift was 76 um using vented borders, 1/4 inch peripheral holes and the higher pressure. Analysis shows that the tooling method

Quality, Acceptability and Reliability

has the most positive effect on shifting and interacts with panel venting (V).

The second experiment in Figure 10 uses optimizing photoresist exposure, developing, and etching to provide the highest production yield. The variable and levels were a full factorial design of three variables at three levels (center point):

- **Exposure energy in mjoules: 70, 50, and 30**
- **Developer speed in inches per minute: 45, 40, and 35**
- **Etcher speed in inches per minute: 45, 40, and 35.**

The variables were chosen with the center point being the current production process: 50 mjoules, 40 in/min developer and 40 in/min etcher. The highest yield was 95% using slower developer speed, lower exposure intensity, and the slower etcher. Analysis shows that the developer speed has the greatest effect on yield and interacts with etcher speed.

The third experiment which is illustrated in Figure 11 is an experiment to find the highest hole quality in a multilayer board. The variables and levels were a Full Factorial Design of four variables at three levels:

Drill methods:	(-) resharpened 4-8 times	(0) resharpened <4 times	(+) new drills
Drill diameter:	(-) 0.008 in	(0) .014 in	(+) 0.020 in
In-feed rate:	(-) 30 in/min.	(0) 60 in/min	(+) 90 in/min
Construction:	(-) Std Foil-Lam	(0) Thick-prepreg with Foil-Lam	(+) Std Core-Lam.

The results of these analyses are the hole quality (rms roughness %) and maximum inner-layer mushrooming in microns.

The best quality was zero microns mushrooming and

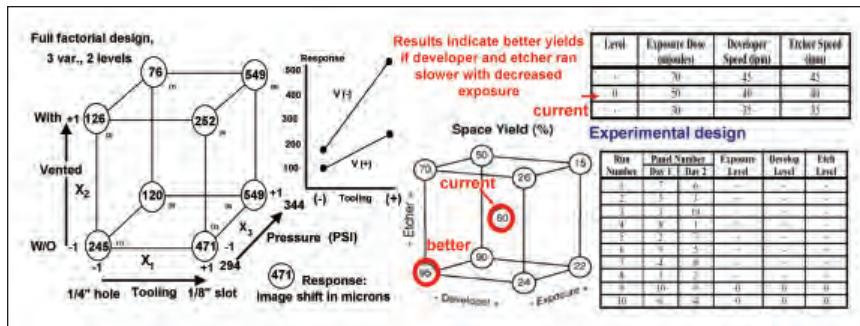


FIGURE 10: This illustrates two examples of Factorial Design of Experiments (DOE) in printed circuit manufacturing; minimizing inner-layer shifting during lamination (left) and optimizing yield in exposure, developing, and etch (right).

< 3% rms hole wall roughness using Construction (-), standard Foil-Lam, and a plane of any drill bits from 0.014" to 0.020" diameters with any appropriate in-feed rate. Analysis shows that the drill diameter has the best effect on hole wall roughness and interacts with drill in-feed rates and drill bit resharpening.

The fourth experiment in Figure 11 is to find the highest hole quality and to examine drilling productivity. The variables and levels were a Fractional Factorial design of three variables at two levels:

-
- | | | |
|------------------------|------------------|-------------------------|
| 1. Drill method: | (-) New drills | (+) Resharpened 6 times |
| 2. Stack height: | (-) 1 high | (+) 3 high |
| 3. Panel venting dams: | (-) No flow dams | (+) Full venting dams |
-

The results of these analyses are the hole quality (rms roughness %) and maximum inner-layer mushrooming in microns.

The best quality was < 4% rms hole wall roughness using a plane of new drill bits for stacks of one high with

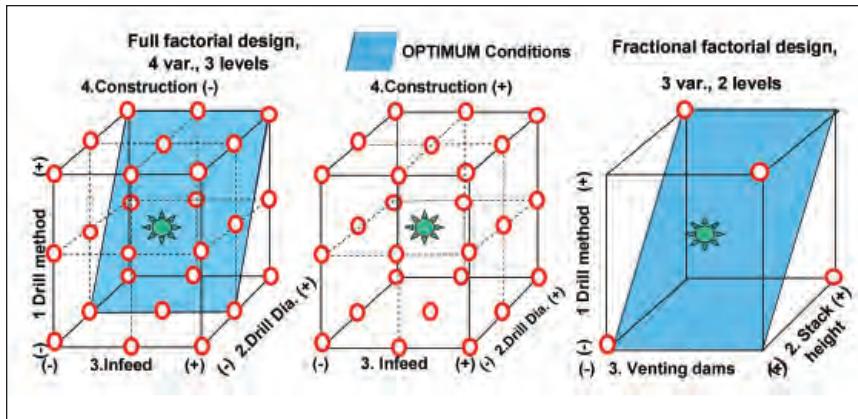


FIGURE 11: This illustrates two more examples of DOE for hole quality in multilayer boards, one conducted to optimize drilled hole quality (left), and a fractional factorial DOE to further optimize hole quality and production productivity (right).

any appropriate venting dams. Analysis shows that the old resharpened drills could be used with drill stacks of three high with a useable hole wall roughness, but they interact with drill in-feed rates.

Notice that this last experiment was a fractional factorial. The power of a scanning experiment using the fractional factorial methodology is that N number of variables can be reviewed with only $N+2$ experiments. This is useful to find main effects but not interaction, while later experiments will provide an examination of interactions and optimization.

Who Can Build HDI?

This is an interesting question. Because HDI can differ so much in its design rules and complexity, understanding if a fabricator is capable of building what you have designed is important. The best way to do this is to test the fabricator's capability.

Is The Fabricator Capable?

A test vehicle made up of various geometries is the best way to measure a fabricator's HDI capabilities. These geometries can be *parametric analysis and characterization coupons*. The IPC has these geometries, but there are two sets that have the unique capability to be electrically tested and provide quantitative feedback on fabrication capability.

Qualification Coupons

The best tools I know for analyzing fabricator capability are the many *parametric analysis and characterization coupons* available to you, which are part of the *quality assessment process*. Utilizing these processes provides reliability evaluations, end-product evaluations, work-in-process product evaluations, and process parameter evaluations. Here are six coupon systems that I will explain in more detail:

- Parametric Test System (PTS)
- Conductor Analysis Technology (CAT)
- Printed Circuit Quality and Relative Reliability (PCQR²)
- Others: PerfecTest
- Highly Accelerated Thermal Shock (HATS)
- Interconnect Stress Test (IST)
- Thermal Test Vehicles

Vendor Qualification

Selecting an HDI fabricator can be very challenging. One way to discover the HDI capabilities of PCB fabricators is the new IPC-9151 Capabilities Benchmarking Panel. It is provided in 2, 4, 6, 10, 12, 18, 24, and 36 layer structures with high- and low-density design rules, five thicknesses (for PCB and backplanes), and in a large panel size of 18" x 24" with various traces and spaces and via structures of blind and buried. The

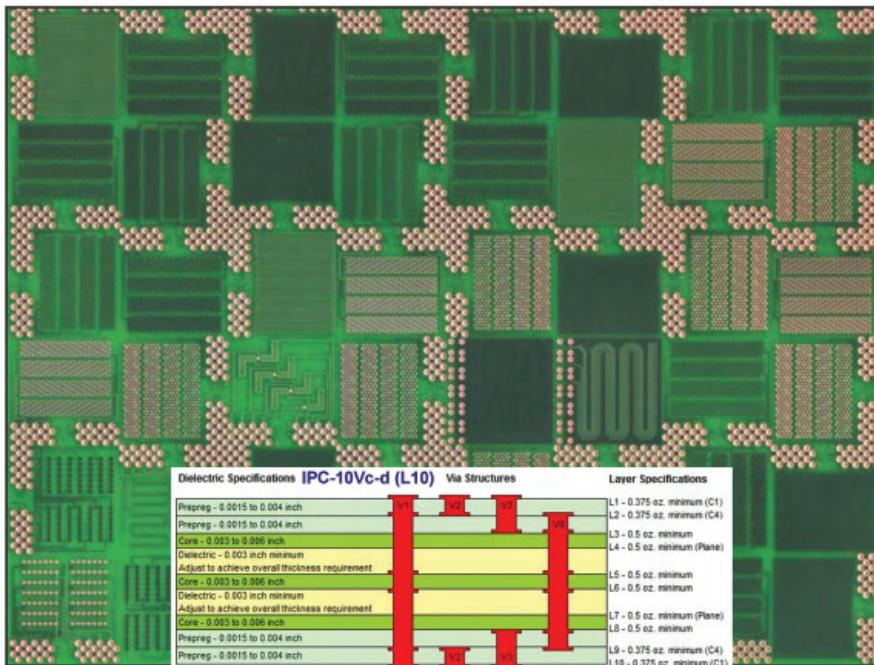


FIGURE 12: The new IPC-9151 Capability Benchmark (PCQR²) is an ideal way to evaluate which fabricators are capable of manufacturing HDI boards with high yields. The IPC-9151 has eight different layer counts, several design-rule variations from which to select, and various blind-buried via-structure combinations, including back-drilling. The Gerber artwork and sample report are all free to download at www.pcbquality.com.[2]

IPC Committee is planning other new Benchmarking Panels for substrates. A standardized multilayer panel can be seen in Figure 12.

The blind vias are optional, but provide significant data on the fabricator's HDI capabilities. Details, artwork, and a sample report are available on the IPC 9151 Website (http://www.pcbquality.com/CAT_Inc/HOME.html).

Other options include fabricating production boards and having them tested. Although fabricating and testing boards is convenient, most of the time this results in statistically nonsignificant results, that is, too few samples are evaluated

to provide for an interpretation that is statistically significant. The performance measured could be the result of hand-selecting the samples and not being statistically accurate in covering a range of capabilities.

Many times test vehicles are used for qualification and can be very accurate. Utilizing test vehicles is also the way reliability can be established. Later sections will discuss test vehicles and reliability testing results.

Why Is This Important?

With so many different part numbers running through your production, it is difficult to know how well your process is running, especially with regard to changing circuit production. One way that the IC manufacturers know that a process is running correctly is to measure specific coupons on a *parametric die* that is placed on each wafer and to have specific *parametric wafers*. Probe stations can be set up at specific process steps to probe these parametric dies to provide feedback as to whether the process is running within control bounds. Having a specific coupon that is sensitive to a specific process is like the proverbial canary-in-a-coal-mine. It signals a problem with the process *before* it hurts the product. The accumulation of these process effects, as well as the design, will be demonstrated at final test with the characteristic First Pass Yield (FPY). FPY models can be found in this book's Chapter 4 - Design of Advanced Printed Circuits. The next section's text and Figures 13 through 17 and 22 through 23 are from a column I wrote for CircuiTree in August, 2005 called "Passing The Test," printed here with permission.[6]

Parametric Test System

The *parametric test system* (PTS) was created by Hewlett-Packard's Printed Circuit Division in 1987 based on early H-P

coupons used in production since 1972. Those early coupons focused on inner-layer shifting, by using the copper on I/Ls shorting to a PTH, moiré patterns, and hole quality cross-sections. Additional influence came from a parametric printed circuit board used as a training and process vehicle for the first NanYa PCB Facility in Taiwan (circa 1983). This PCB had various design-rule technologies on it and provided feedback on how the process was improving.

The H-P PTS was a group of seven coupons that could be placed on production panels or used on parametric panels to provide a snapshot of the capability of the processes. The initial seven coupons (Figure 13) were designed to test:

- **outer-layer registration (a);**
- **inner-layer registration and shifting (b);**
- **conductors/pads open and shorts (c);**
- **plated through-hole and I/L conductors continuity (d);**
- **artwork defects (e);**
- **soldermask registration (f);**
- **etch factors (g).**

The coupons were all designed to be tested by facility continuity testers using a bed-of-nails open-short testing machine. In H-P's case, the tester was an ATG2000 grid tester. The tester's fault-file was captured by an H-P workstation and stored. Each coupon had a stored perfect response or netlist that was compared to the fault file and the opens and shorts were translated to dimensional shifts or other parametric data. The RS/1 statistics program was used to produce control charts, statistical reports, and historic data. The Gerber artwork files for these coupons can be downloaded from Happy Holden's Mentor BLOG, called *Happy's PCB INSIGHTS* at <http://communities.mentor.com/mgcx/blogs/pcbinsights>. The test

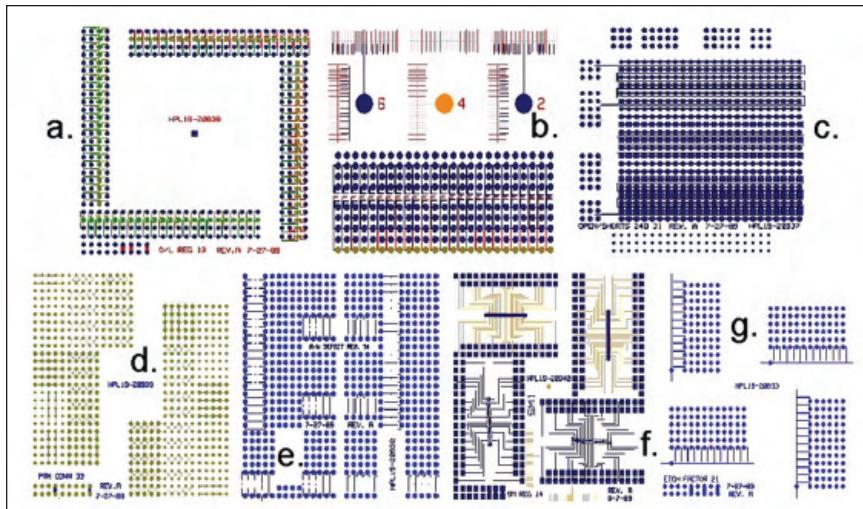


FIGURE 13: The seven coupons designed by H-P included: (a) outer-layer registration in 0.00025" increments; (b) inner-layer registration and shifting in 0.00025" increments including 0.1 mil x-ray vernier; (c) trace / trace / pad 'open and short' circuit on multiple layers; (d) plated through-hole continuity patterns including I/L connections at various angles to the PTH; (e) artwork defects analysis in 0.00025" increments; (f) etch factor analysis in 0.00025" increments.[7] The Gerber artwork files are available at <http://communities.mentor.com/mgcx/blogs/pcbinsights>

system can be seen in Figure 14a. Also seen in Figure 14 (b and c) are the small stand-alone coupon testers that operators used to check the process immediately as a confidence indicator. These home-built milliohm meters worked with a simple 1-ampere power brick, a 4-digit digital panel meter and a machined Plexiglas coupon holder with 8 spring-loaded gold pins wired to a 4-position rotary switch in a 4-wire Kelvin measurement scheme (Figure 15j).[7]

Conductor Analysis Technology

Conductor Analysis Technology (CAT) is the longest running available parametric coupon system. Born out of an NCMS program with Scandia National Laboratory, founders

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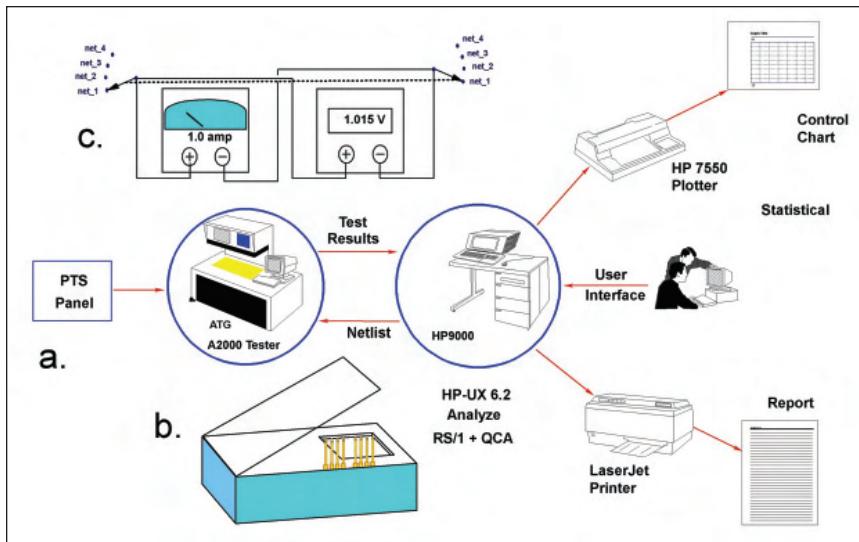


FIGURE 14: The illustrations here show: (a) H-P's PTS arrangement with a continuity tester; (b) coupon test fixture for individual coupons; (c) milliohm measurement using a 1-amp power supply and digital panel meter in a Kelvin 4-wire test configuration.

Tim Estes and Ron Rhodes bought the testing machine from Scandia and started CAT in 1994. Ron has written a column in CircuiTree called “Between the Conductors” about coupons and testing since 1998. You can find his back columns at the CAT web site: www.cat-test.info. Because of the length of availability, its thoroughness, and the wealth of publications, the CAT coupons are the most used and benchmarked. Six coupons, all 25.4 mm by 25.4 mm (1.0" x 1.0"), make up the primary sensors for CAT, seen in Figure 15 a-f:

- Drill overshoot (a)
- Conductor spacing (b)
- Solder mask registration (c)
- Via net daisy-chain (d)
- Impedance (e)
- Registration (f)

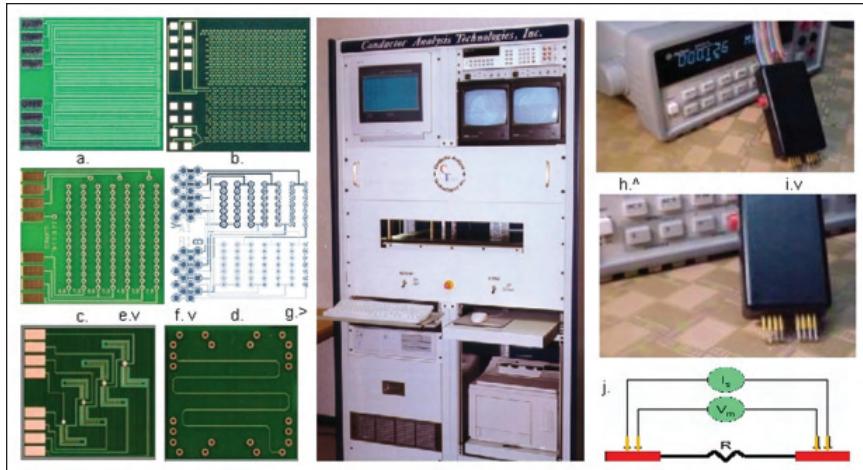


FIGURE 15: These pictures show Conductor Analysis Technology (CAT) including: (a) drill overshoot coupon; (b) conductor/spacing coupon; (c) solder mask registration coupon; (d) 4 via-nets daisy-chain coupon; (e) impedance coupon; (f) registration coupon; (g) sensitive AC chopped 4-wire micro-ohm test system; (h) portable coupon test system using Agilent 34401A meter; (i) close-up of coupon probes; and (j) current and voltage arrangement of the 4-wire Kelvin measurement configuration.[9]

The value of a parametric system such as CAT is its ability to capture the true capability of a process, procedure, machine, or materials. There are numerous features on each coupon so that they can be tailored to capture current capability. Complex as these features are, they cannot be inspected or sorted, so they truly represent what is going on. For novice users, the temptation is to inspect them to get perfect samples. This usually proves to be a futile activity, as some features are, by design, beyond our current capability.

Coupons that are customizable by CAT include conductor-spacing (1 to 20 mils), via diameter, via land, daisy-chain sequence, number of layers, registration sensitivity and layers, via structure (through, blind, buried, skip vias, stacked, sequentially laminated, etc), impedance type (single-ended, differential, edge-coupled, broadside,

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coplanar, etc.), and overall thickness, as well as placement and panel size. Some coupons were designed to be removed and put in small testers. I have been using these coupons since 1996 for vendor qualification, process improvement, and relative reliability.

The primary equipment for CAT is seen in Figure 15g, which was designed by Scandia and consisted of an alignment system, fixtures, and a bed-of-nails connected to a sensitive AC-chopped, 4-wire Kelvin resistance measurement system (Figure 15j) feeding a PC. To improve the impedance measurements, a robotic probe and measuring unit were added in 2001. A portable system was also designed so that readings could be made in production, using an Agilent 34401A voltmeter as seen in Figures 15h and 15i. The portable system has additional coupons from 0.33"x 3.0" to 0.5" x 2.0" to facilitate placing them on production panels, as well as software to automatically calculate responses. The Hong Kong Productivity Council erected a second testing facility using this equipment in Hong Kong in 2004.[8]

Process Capability, Quality and Relative Reliability

The popularity of CAT panels eventually led to their standardization by the IPC. The subcommittee, D-36, created standard parametric panels that became known as the IPC-9151 Process Capability, Quality and Relative Reliability or PCQR². The data from these Benchmarking Panels are kept in a database available by subscription from the IPC. Artwork and specifications for the benchmarking panels are available free to the industry at www.pcbquality.com. Figure 12 shows a typical PCQR² panel for the 10-layer benchmark (IPC-10VC-d). Another one is the 14-layer (IPC-14VB-D) Via Rigid Board Design (18" x 24") utilizing through-, blind, buried, and

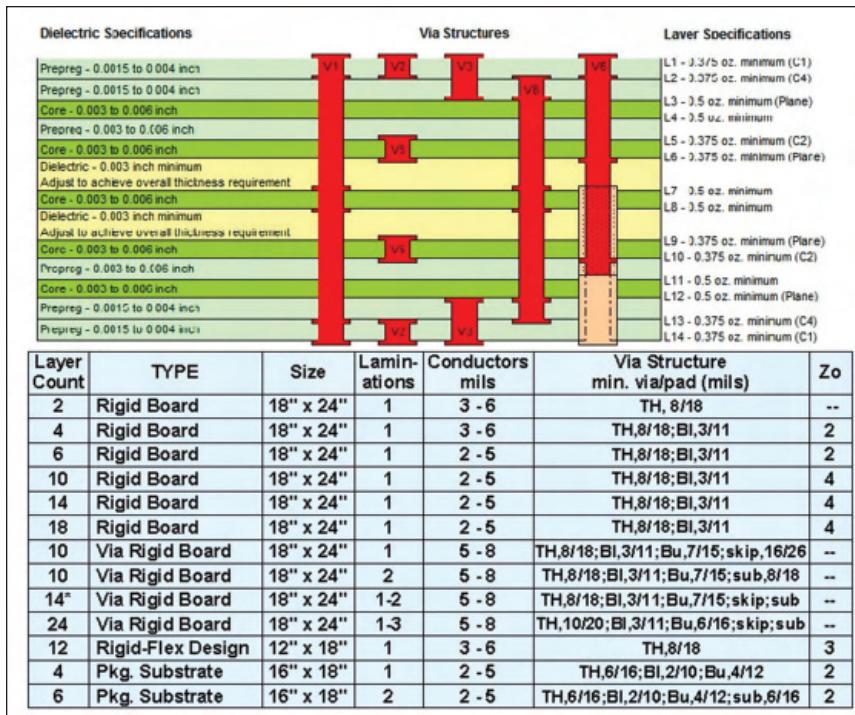


FIGURE 16: This PCQR² (artwork available) 14-layer Via Rigid Board is illustrated by cross-section showing thickness ranges and various through-hole, blind, buried, sub-composite, and back-drilled vias.[10]

subcomponent vias with two laminations (Figure 16). The table in Figure 16 shows the current list of available PCQR² panels.

Others: PerfecTest

PerfecTest came along in 1994 to address the problems in multilayer material movement and drill registration. The coupons (Figure 17a) are placed at the outer edges of the multilayer panel. The coupons work by detecting which plated through-holes have detected the movement of a particular I/L copper wedge. Figure 17b illustrates the 0.002" increments, from one mil to nine mils, that the coupon will detect in the X and Y axis. Coupons can be placed on every layer or

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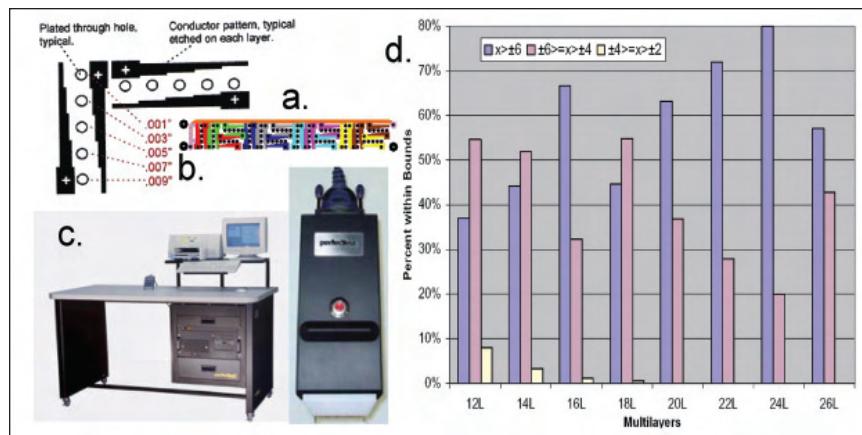


FIGURE 17: PerfecTest is a material movement and registration coupon system. The figure illustrates (a) coupons which are 0.2" x 1.73" and placed at the edges of production multilayer panels; (b) how it works by measuring the continuity of PTH versus the metal foil of specific layers; (c) the testing equipment including a close-up of the probe head; (d) data from one user in production of nearly 250,000 readings for 12- to 26-layer multilayers.[11]

just specific ones. Although no specific testing equipment is required, Figure 17c shows the PerfecTest unit equipped with analysis and data storage software. Illustrations and reports are available on their internet site at www.perfectest.com. Figure 17d is a summary of 250,000 coupon readings that we have collected in manufacturing over a six-month period.

Reliability Testing

Many coupon systems are used for reliability testing. They are incorporated into test vehicles that are then fabricated, subjected to various conditioning and stresses, and then evaluated for performance.

Test Vehicles

Figure 18 shows some of the test vehicles that mobile phone companies used during the 1990s to establish the

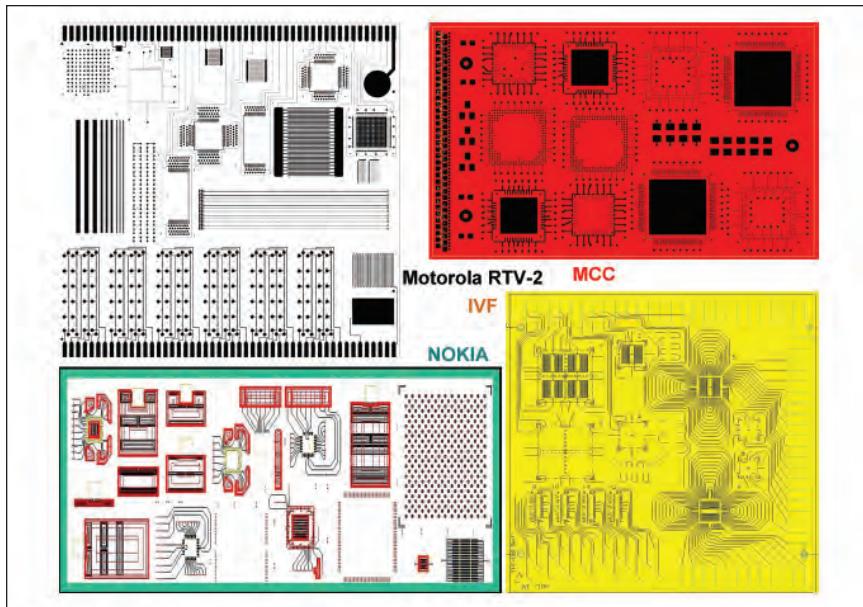


FIGURE 18: Four examples of reliability test vehicles used by mobile phone companies during the 1990s to establish HDI-microvia reliability of portable products reliability of HDI microvia structures. The RTV-2 from Motorola was the test vehicle used by the IPC for the October Project and for its ITRI-HDI reliability study.[12]

An example of a more recent Test Vehicle is seen in Figure 19. This panel contains four different daughter cards, all used to test various HDI reliability criteria:

- 4 duplicate Test ASIC “B” 1657 CCGA for solder-via structure and blind-buried via daisy-chain
- 4 duplicate Test ASIC “C” 1413 FCBGA for solder-via structure and blind-buried via daisy-chain
- 4 duplicate Multi-purpose board with seven coupons: solder spread, peel strength, CAF, ball shear, Tg by TMA, thermal stress, and Z-axis CTE by TMA
- 8-IST Coupon: 4 nets/coupon: plated through-hole net, buried via net, top microvia net, and bottom microvia net

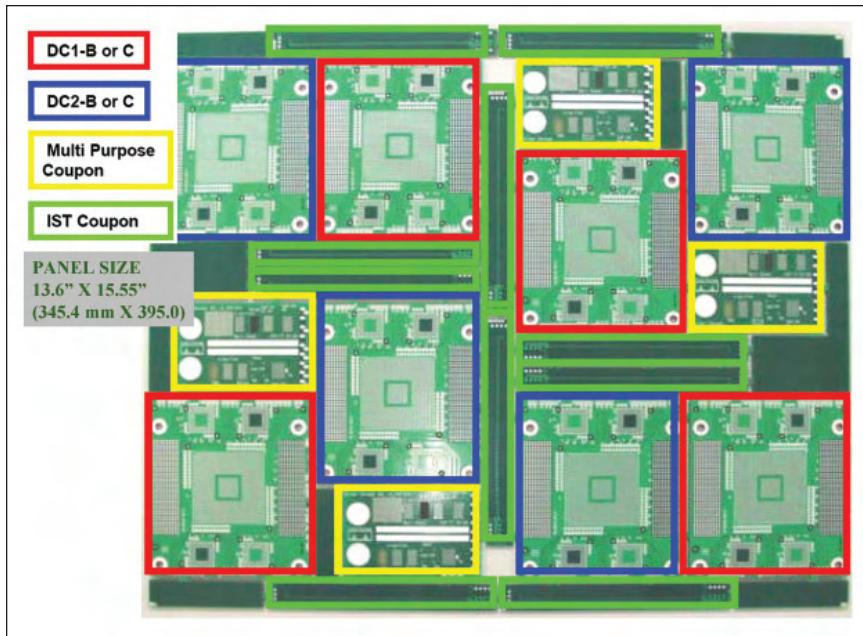


FIGURE 19: An example of a well thought out HDI reliability test vehicle of daisy-chain complex components, dense blind-via daisy-chains, multi-purpose coupons, and IST coupons[13]

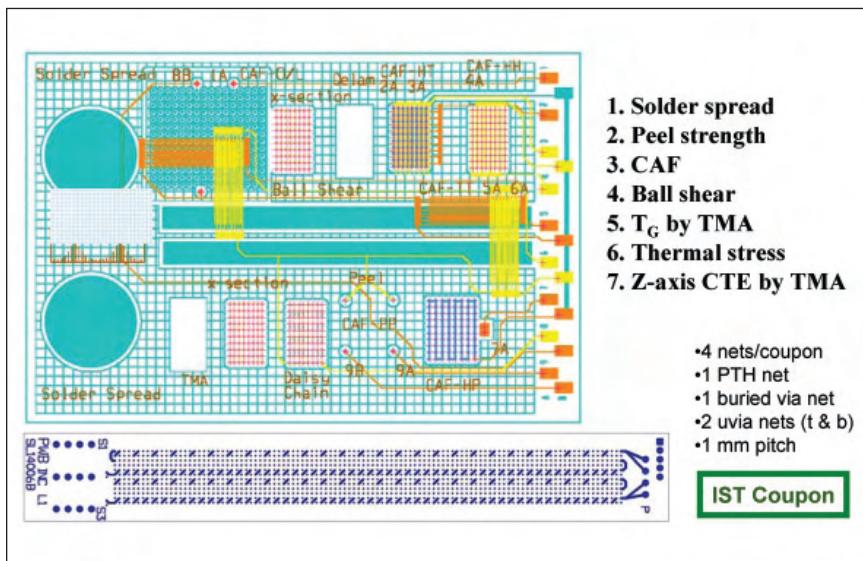


FIGURE 20: Multi-purpose coupon containing seven test structures and the IST coupon with four via structures.

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The results from this OEM's HDI testing were presented at PCDesign-WEST in 2003.[13] Some of the results are presented later in this chapter.

Typical reliability update procedures for a fabricator are shown in Table 1. This fabricator routinely conducts these tests:

- Temperature cycling
- Surface insulation resistance
- SEC
- High humidity
- Solderability
- Peel strength
- Thermal stress
- Tg
- High pot test

Test Item	Test Method/ Equipment	Criteria	Frequency	Capability	Layer Count
Temperature Cycling	125°C 30min. Room Temp. 10 min. -55°C 30 min. Room Temp. 10min	Hole Wall Resistance: <10% change before test <20% Change before test	4 pcs/month	100 Cycles <10% 1000 Cycles < 20%	Routine Test: 6L HLC Test: Random By R&D >12L
Surface Insulation Resistance	Pre Condition: 23°C, 50% RH, 3hr Test Condition: 35°C, 85%RH, 24hr	Insulation Resistance: After Black Oxide >10G Ohm After O/L Etch >10G Ohm After HASL > 3G Ohm	2 pcs/month	>10G Ohm >10G Ohm > 4G Ohm	Random Sample For O/L
SEC	Omega Meter 600 SMD 15 min. After Black Oxide, O/L etch, HASL	< 6.4 µg NaCl/Sqin	3 pcs/day	Average under 4ug/sqin	Finish Board
High Humidity	50°C, 95% RH, 7 days, 100V Bias	Resistance > 1 G Ohm	6 pcs/month	Pass	Routine Test: 6L
Solderability PTH Edge (SMD) Wetting Balance	Solder Pot Floating: 245°C, 4 sec.	No-dewetting	2 pcs/week	Pass	Finish Board
Peel Strength	IPC-TM-650 2.4.8.1	Trace to Laminate > 9 lb/in Hole > 10 kg/mm ²	2 pcs/month	>10 lb/in >11 kg/mm ²	Random Sample For O/L
Thermal Stress	288°C, 10 sec, Solder Float	No Delamination Hole Wall Inspection	10 pcs/week	Pass	For 2~18L Tooling Sample
Tg	D.S.C.	FR-4 > 120°C FR-4 Tetra > 130°C	2 pcs/day	> 125°C > 132°C	2~18L
High Pot Test	500 Volts, 1 min.	<1 mA Leakage	6 pcs/month	PASS	Min. spacing 4 mil dielectric thickness 4 mil

TABLE 1: Typical fabricator reliability testing program for HDI processes

Accelerated Reliability Test Coupons

Three coupon methods are typically used in reliability test vehicles:

- Accelerated Thermal Cycling (ATC)
- Highly Accelerated Thermal Shock (HATS)
- Interconnect Stress Test (IST)

Thermal Cycling Testing

Accelerated reliability testing using test coupons is about as old as PCBs are. The principle is to crowd a large number of holes into a small space and connect them in a chain, hence the name *daisy-chain*. The test board pictured in Figure 21 is typical of an HDI daisy-chain test vehicle. This board contains a number of different test structures for various test criteria. Most of the space is taken up with the HDI blind-via daisy-chains (Blocks A, B, C, E, and F) and the through-hole daisy-chain (Block D). Table 2 shows a summary of the test blocks and their criteria for qualification, using the TV in Figure 21. This is typical for the qualification of higher volume technology-intensive products like notebook computers and networking cards.

Highly Accelerated Thermal Shock

One of the results of the D-36 subcommittee's work on *Relative Reliability* was the creation of a highly accelerated thermal shock procedure. Developed by CAT and Microtek Labs, HATS, as it now is called, runs the PCQR² coupons through an air-to-air thermal cycle from -45°C to 145°C (-60°C to 160°C available) in a 30 second cycle (Figure 22a). The coupons are continuously monitored by a 4-wire data acquisition system connected to the test fixture (Figure 22b) to detect a 10% change in the resistance of the via-daisy-chains or

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Reliability Evaluation	Quantity	Settings / Conditions	Number of Cycles	Pre-processing	Measuring Method	Criteria to Pass
Cross Section	5 samples	Etch the section with solution of iron chloride or copper chloride		Measure plating thickness, hole diameter, and drilled diameter per hole diameter		
Hot-oil Test	500,000 BVH (~ 40 boards of Figure 20)	20C (20 sec) -260 C (10 sec)	40 cycles	Twice: IR reflow, or convection reflow peak 240C (10 sec)	4-wire Kelvin resistance measurement	Final measurement +/- 10% of initial
Vapor-phase Thermal Shock	500,000 BVH (~ 40 boards of Figure 20)	-65C (30 min) – room temp (5 min) – 125 C (30 min)	250 cycles	Twice: IR reflow, or convection reflow peak 240C (10 sec)	4-wire Kelvin resistance measurement	Final measurement +/- 10% of initial
Dielectric Reliability	5 samples	85C, 85% RH, 12 VDC	650 hours	Twice: IR reflow, or convection reflow peak 240C (10 sec)	Every 6 hrs take resistance measurement for 1 min	Dielectric resistance shall be 10^6 ohms or more
Drop Test	5 samples	Height of 1.0 meter	Drop freely for 5 cycles and measure the resistance of the daisy-chain		Final measurement +/- 10% of initial. No cracks and delamination	
Impedance	5 samples	TDR @ 1 GHz	Characteristic IMP of layers 1 and 3	none Twice: IR reflow, or convection reflow peak 240C (10 sec)	Calibrated TDR by ASTM/IPC	+/- 10%

TABLE 2: Description of the test blocks in Figure 21

500 cycles. The coupons can be various sizes from 0.5" x 1.0" to 1.0" x 2.0", as seen in Figures 22c, 22d and 22e. These are available free from the coupon generator software on their web site, www.hats-tester.com. A chamber load costs only \$4.50 per cycle (250 cycles minimum). The speed and efficiency of this system, has enticed many companies to purchase the unit.

Interconnect Stress Test

Interconnect Stress Test (IST) is the oldest and now most-used accelerated thermal via reliability system in the industry. Developed in 1989 by Digital Equipment of Canada, patented in 1994, and commercialized by PWB Interconnect Solutions in 1995, nearly 70 systems have been installed world-wide. Used by over 120 OEMs, EMSs, and PCB fabricators, it has six

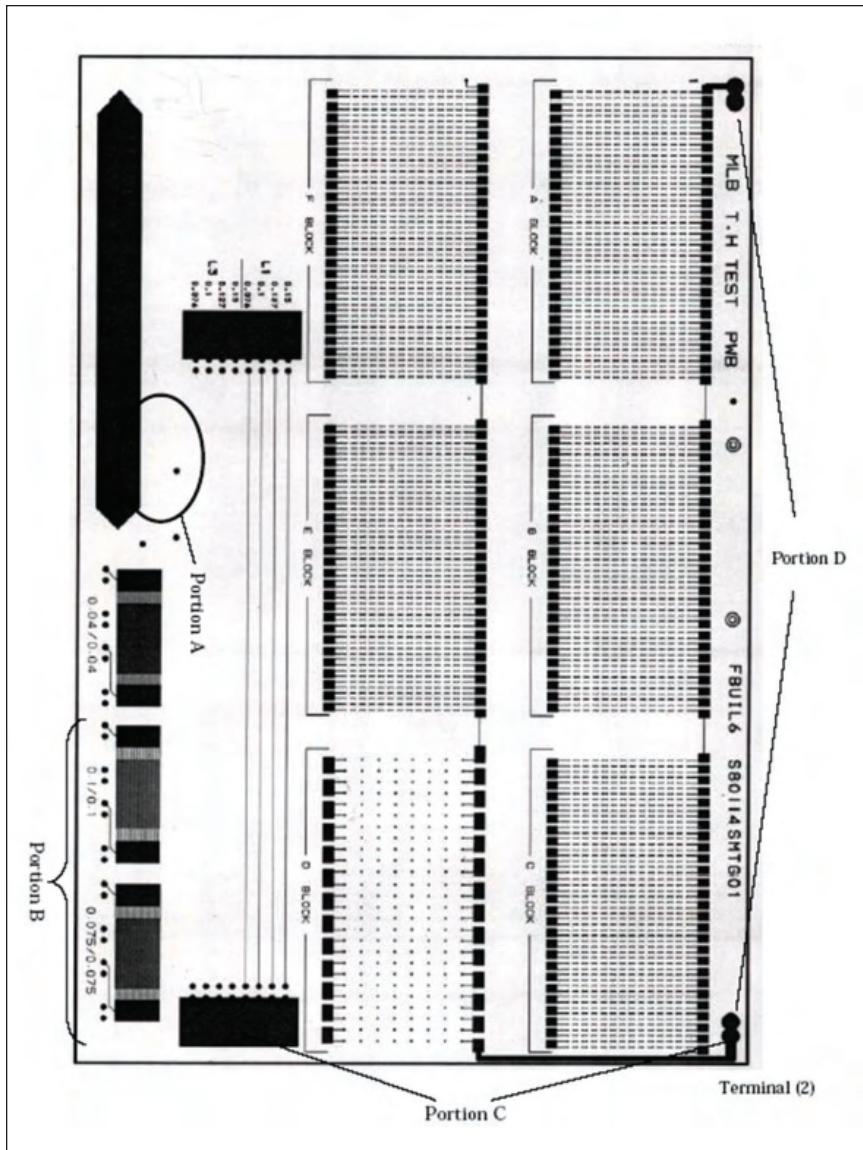


FIGURE 21: Typical of HDI thermal cycling reliability test vehicles, this vehicle contains five blind-via daisy-chains on each side of the board plus one through-hole daisy-chain, as well as other test structures for dielectric reliability, drop test, and impedance.

licensed Service Centers around the world and is standardized by the IPC-TM-650 Test Method 2.6.26 (the DC Current Induced Thermal Cycling Test).

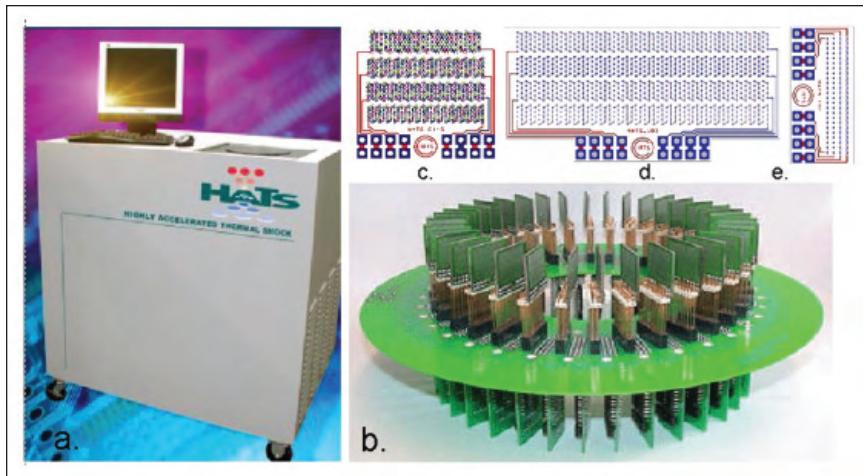


FIGURE 22, Highly Accelerated Thermal Shock or HATS is accomplished by the unit through generating refrigerated and heated air passing over the test fixture (a) that contains 36 test coupons (b) as shown in the 1.0" x 1.0" (c) or the 2.0" x 1.0" (d) or the 0.5" x 1.0" coupons (e). [14]

A typical coupon is seen in Figure 23a, which illustrates a coupon that we use for an IPC Class-III board. It has through-holes, blind microvias, and buried vias using a high Tg, low-loss laminate. Two of these coupons are built with every board, and until an approved number of IST cycles are passed, it is not assembled. Failure means a return to us for analysis.

The IST method measures changes in resistance of vias and internal layer connections as the holes are subjected to thermal cycling. The thermal cycling is produced by the application of a high current through the resistive internal layer connections of a specific group of holes, usually 200 daisy-chained vias, interconnecting through two adjacent layers, called the Power Circuit (Figure 23c). Switching the current on for three minutes creates heat to take the connections from room temperature to a designated higher temperature. Stopping the current and using forced-air cooling, the connections cool in two to three minutes (Figure 23f). Another group of

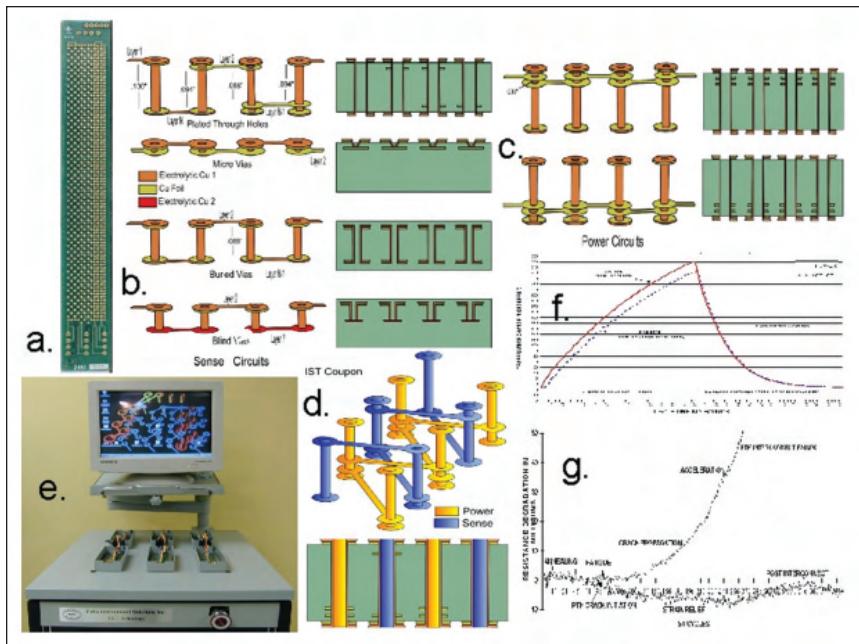


FIGURE 23, Interconnect Stress Test (IST) is a DC current induced thermal cycling test. This figure shows: (a) a typical 6" coupon; (b) a sense circuit daisy-chain; (c) a power circuit daisy-chain; (d) an isometric view of parallel and overlapping power and sense circuits; (e) IST power, data acquisition and fixturing test equipment; (f) a typical heating-cooling cycle; and (g) failure modes of thermally stressed interconnects.[15]

interconnects are the Sense Circuits and Power Circuits, which are two independent daisy-chains, interconnecting 500 vias through any two inner-layers at various levels (Figure 23b). An isometric view of the two sets of interconnects, running parallel to and sequentially overlapping, is seen in Figure 23d. The equipment providing the coupon fixturing, current, cooling, and resistance measurement is seen in Figure 23e.

An accelerated failure will occur because of the differential thermal expansion of the interconnect structure. Failure can occur in a number of locations (Figure 23g), and can be either a via crack, post separation, connection crack, or material delamination in a specific region within one or multiple

areas. Cycling continues until the specific rejection criterion is achieved or the required numbers of cycles are passed.

The IST Internet Site (www.pwbcorp.com) and its European licensee, Polar Instruments (www.polarinstruments.com), have extensive application data available, including standard designs of five and six inch coupons, for any number of layers, covering these structures:

GB400000A – Any 2-layer sequentially laminated

blind vias

GB400000B – Any 2-layer drilled blind vias

GC400000B – Any layer sequentially laminated

buried vias

GM400000B – Any 2-layer blind microvia

GP400000A – Any layer through-hole on PCB >

0.125 inches

GS400000A – Through-hole and blind vias > 4 layers,

sequentially laminated on PCB <=0.125 inches

GT408000B – Any layer through-hole on PCB >=0.125

inches on a 5-inch coupon

GT501000A – Any layer through-hole on PCB >=0.125

inches on a 6-inch coupon

Other Data

On July 15, 1997, the IPC's ITRI Consortium finished a comprehensive evaluation of the reliability of HDI vias and fabricators in North America. The report, titled "High-Density Printed Wiring Board-Microvia Evaluation," was assembled by the October Project team. The test vehicle used was contributed by Motorola as was their MRTV-2 multilayer (shown in Figure 18 and Figure 24). Three types of microvias were tested (laser drilled, plasma drilled, and photovia), from 15 submissions by nine companies at 11 sites. To understand

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what has happened to the North American fabrication market, only four of those 11 companies' sites are in business today! But the 160-page report clearly establishes the reliability of microvias.

The report is divided into two parts. The first part describes the test vehicle and the experimental plan, together with the complete reports from each company evaluating the submissions. The testing of the MRTV-2 boards was divided among four companies: Celestica, Delco, Motorola, and Nortel. The second part of the report contains reports, data, and photographs of microsections provided by each of the submitters. Table 3 shows a summary of the test results.

Table 4 shows a summary of the maximum microvia performance from the report which was based on 5-mil blind vias in 2-mil dielectrics.

In September 1997, ITRI designed a Chip Scale Package (CSP) for an assembly and reliability study at E&ET, ERC. The CSP test vehicle is an eight-layer board with blind vias in layers 1-2

Conditions	Industry Requirement	Laser Drilling	Photo Via	Plasma
1. Liquid-Liquid Shock: - 55°C to 125°C, cycle time of 5 min., 2000 cycles , Change of resistance <10 %	Motorola: 500 cycles	no failures	failures (opens)	no failures
2. High Temperature: 125°C, for 1000 hrs,	Bellcore: 500 hrs	Passed	Passed	Passed
3. Adhesion Test - Copper Peel Strength	IPC: 5 lbs/inch	Passed Min. 5.5 lbs Max: 12.2 lbs	Failed Min. 3.1 lbs Max: 14.0 lb	Passed Min. 8.0 lbs Max: 11.5 lbs
4. Dielectric Withstanding Voltage (0 to 5000 VDC applied, rate of 100volts/sec	IPC:500V/mil Bellcore: 1000 volts for 1 min	Passed >1500 V/mil	Passed >1500 V/mil	Passed >1500 V/mil
5. Min. Copper Thickness in Micro Via (mils)	Bellcore: Min. 0.7 mil	Passed 0.95	Passed 0.85	Passed 0.70
6. Dielectric Thickness (Micro via) mils	Bellcore: \geq 2.00 mil	\geq 1.8	< 1.80	\leq 1.80
7. Temp./Humidity: 85°C, 85%RH, 100 V Bias, 1000 hrs	Bellcore: 500 hrs	Passed	Passed	Passed

TABLE 3: ITRI summary test results from the 1997 October Project - Phase I, Round 2 Report on microvias[12]

<i>Conditions</i>	<i>Laser</i>	<i>Photo Via</i>	<i>Plasma</i>
1. Thermal Shock: - 55 ⁰ C to 125 ⁰ C, cycle time - 5 min,	3500 cycles	2000 cycles	3000 cycles
2. Temperature Cycling: 0-125 ⁰ C, cycle time - 21 min.	> 1000 hrs	> 1000 hrs	> 1000 hrs
3. Temperature Cycling: Air-Air - 40 ⁰ C to 125 ⁰ C, cycle time: 21 min.	>1200cycles	1000 cycles	NA
4. Temp./Humidity: 85 ⁰ C, 85%RH, 5 VDC Bias, 1000 hrs.	2400 Hours	2104 Hours	2000 Hours
5. Solder Float Test at 288 ⁰ C, 10 sec, X 10 ,	Passed	Passed	Passed

TABLE 4: ITRI summary test results from the 1997 October Project - Phase I, Round 2 Report on maximum microvia performance.[12]

and 7-8. The size of the board is 13.95" x 7.73" with an overall thickness of 60 ± 10 mils. This test vehicle evaluated blind via formation by two different methods, mechanical drilling (sequential lamination) and laser drilling (microvia). The mechanical drill is 8 mils with a capture land of 14 mils, and the laser drill is 4 mils with a capture land of 12 mils. The line width and spacing is 3/3 mils. The materials used on these boards were FR4 Core Laminate and Pre-preg, Raw Laminate, Taiyo PSR 4000 soldermask, and Kester Organic Solder Preservative (OSP) as the surface finish. The boards were fabricated by NanYa PCB and Compeq of Taiwan. The CSP eight-layer had reliability tests performed at E&ET, Princeton, NJ.

The test conditions for thermal cycling were 0 - 100⁰ C and - 40⁰ C to + 125⁰ C. Ten sets of coupons were selected, cross-sectioned at the center of the plated through-holes and blind-via holes. The cross-sections were examined for plating integrity, copper thickness, and dielectric thickness. Results are summarized in Table 5 and the test vehicle is seen in Figure 24.

Another HDI and CSP Reliability Characterization Project was conducted by the High-Density Packaging (HDP) User Group International in March of 2000. Figure 25 shows the resultant Wiebull graph on the performance of the fine-pitch

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CSPs and HDI boards. The HDI boards were made in IBM's and H-P's in-house HDI PCB fabrication facilities.

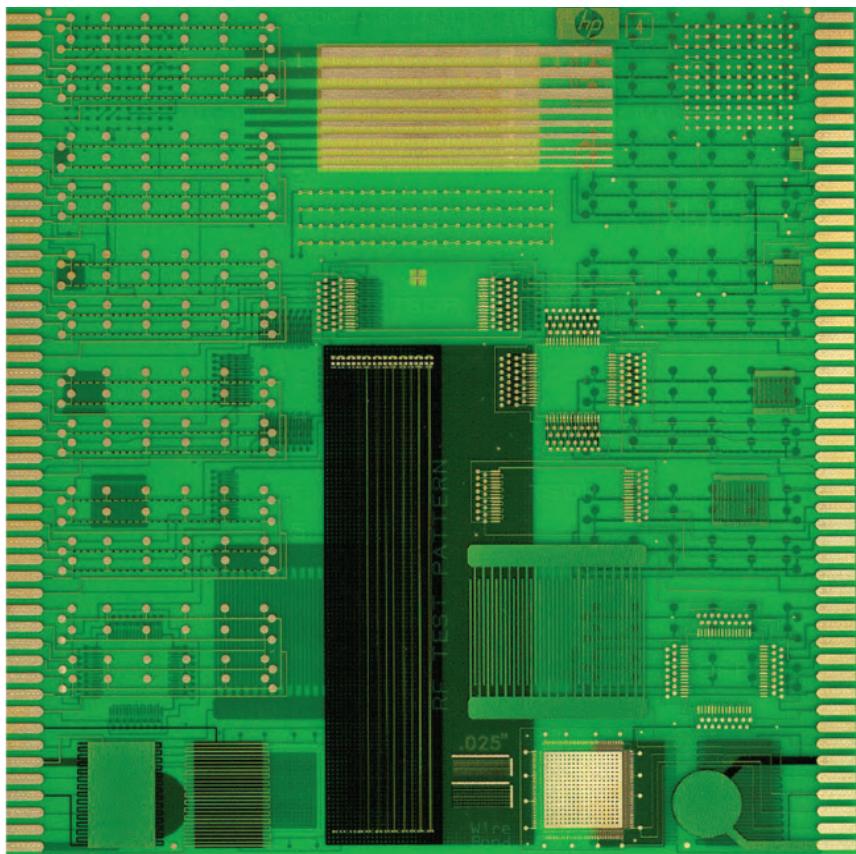


FIGURE 24: MRTV-2 test vehicle used by the IPC-ITRI for various microvia reliability test programs

Attributes	Sequential Lamination	Laser Drilling
Blind Via Drill Size	8 mil	4 mil
Blind Via Capture Land Size	14 mil	12 mil
Plated Through Hole Cu thickness	1.335 mil	1.4135 mil
Copper Thickness in Blind via	1.363 mil	1.493 mil
Blind Via Cu - Cu Dielectric Thickness	6 mil	1.8 mil
High Temperature: 0 - 100 °C, Total Cycle time: 21 minutes with daisy chain	- 5000 cycles (Blind via) - No failures	- 5000 cycles (Blind via) - No failures
Thermal Stress: -40 to +125 °C, Total Cycle time: 21 minutes with daisy chain	- 1264 cycles (Blind via) - PTH failure at 3200 cycles	- 1264 cycles (Blind via) - PTH failure at 600 cycles

TABLE 5: ITRI summary test results from the 1997 October Project

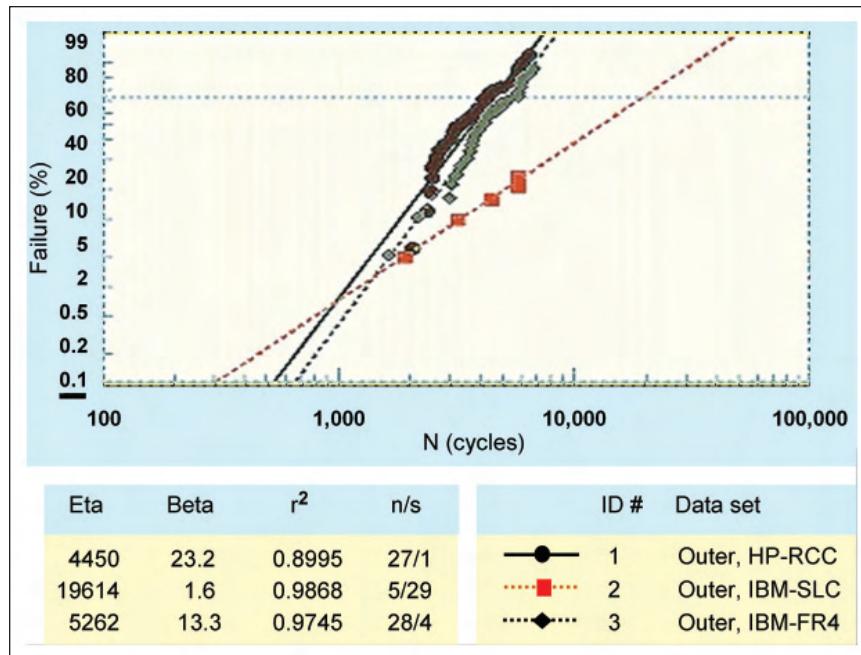


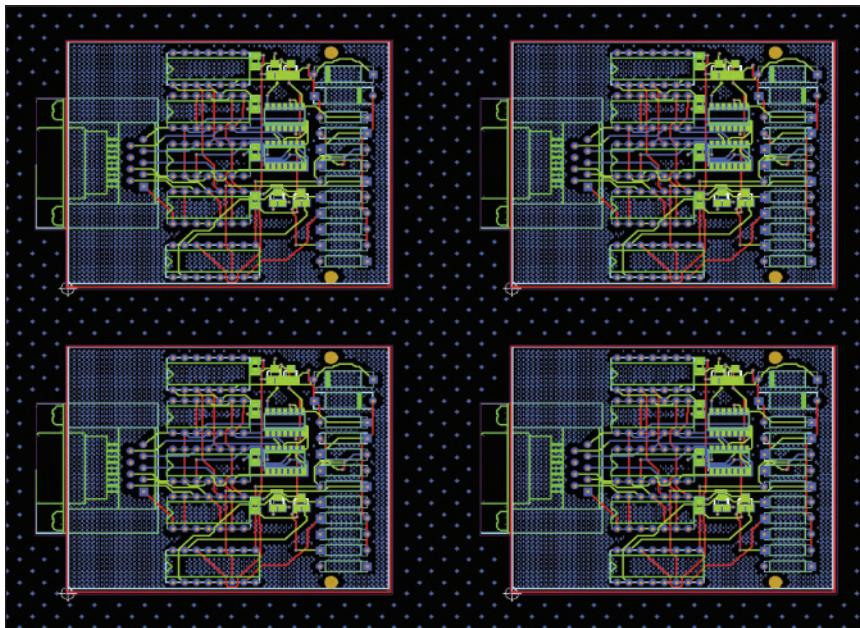
FIGURE 25: HDPUG results of testing fine-pitch CSPs on HDI boards[16]

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13

Assembly and Test Processes for HDI

By **Mark Laing — Mentor Graphics**
and **Matt Wuensch — Mentor Graphics**

Introduction

When implementing HDI printed circuit boards in manufacturing there are many considerations to account for, particularly with assembly, test, and inspection processes. Certain characteristics of the HDI circuit board, such as the lack of externally exposed vias and limited real estate for proper test pads, significantly limit physical access in order to perform automated electrical test. Therefore one of the more important questions with regard to successful HDI implementation is, “How do I test my products?” Fortunately, various solutions exist in the marketplace that can assist with identifying and implementing the right test strategy for HDI PCBs. They can provide valuable information on test accessibility and test strategy trade-offs. We will discuss how existing test coverage can be determined and how this knowledge can be used to develop an overall test and inspection strategy that limits duplicate coverage and minimizes escapes.

Defect Detection Equipment

Before considering any specific test and inspection strategy and its associated Design-for-Test (DFT) measures, it is necessary to consider the types of process verification

Assembly and Test Processes for HDI

equipment available. References are provided that give more detail on the different types of test and inspection equipment. However, the main types of equipment will be introduced and discussed. There are two types of defect detection equipment: structural inspection and electrical test machines. There are four main categories of structural inspection: Paste Automated Optical Inspection (AOI); pre-reflow AOI; post-reflow AOI; and Automated X-Ray Inspection (AXI). Considering electrical test, there are four main types of defect detection equipment: In-circuit Test (ICT); flying probe test (FPT); boundary scan test (BST); and manufacturing defects analysis (MDA). Functional test systems are primarily for product verification as opposed to defect detection. Although they are used for the latter, the poor fault diagnostics makes them more suited to confirming product performance than process verification.

With HDI PCBs, implementing a single test or one piece of inspection equipment may not produce acceptable results. For example, due to the lack of bed-of-nails access resulting in a reduction in coverage on MDA and ICT machines, combined with longer test times at FPT, there may not be a sufficiently thorough electrical test strategy that is effective for higher production volume HDI products. Obscured solder joints, longer inspection times for AXI, and lack of electrical verification for both AOI and AXI machines create issues for an inspection-only process verification strategy. The solution is to be able to implement a process verification strategy that is a combination of electrical test and structural inspection machines depending on the topology of the circuit board, the PCB application, and production volumes.

Given the reduced availability of traditional ICT test points in HDI applications, all possible avenues should be pursued to achieve the necessary quality and cost goals. Techniques

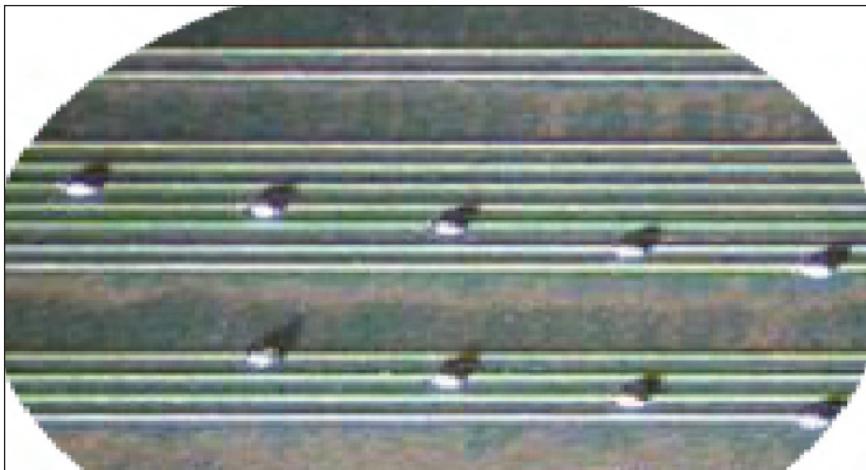


FIGURE 1: Agilent Bead Probe Technology

such as Bead Probe from Agilent Technologies, the ability to incorporate small dots (called *beads*) of solder that are applied to traces, can be used to increase ICT access. External traces that require test points have a small section of the trace exposed through the solder mask layer, enabling a diamond-shaped solder ball to be deposited. Once reflowed, the bead, which needs to be only four mils in diameter, deforms under the pressure of a flat ICT test probe creating an electrical connection between the tester and the PCB. Studies have shown that such a small test point, which is several times smaller than traditional test points, is both reliable and has a negligible effect on high frequency signals. More details, including papers and studies on this technique, can be obtained from Agilent Technologies.

In a number of cases, a reasonable level of bed-of-nails access may be available, provided that it is intelligently designed into the layout of the board. For example, a PCB may not have the real estate to incorporate 100% net accessibility, but 75% of the nets could be made bed-of-nails accessible. The

question is, which nets should make up this 75% access so that the best overall coverage can be attained?

With reductions in accessibility on many of today's HDI PCBs, employing a process verification strategy using multiple electrical test and structural inspection machines can keep production yields at acceptable levels. In order to achieve maximum process verification effectiveness, other Design-for-Test practices should be employed to optimize the overall coverage by taking advantage of the capabilities of different electrical test and structural inspection solutions.

Defect Spectrum

Having an accurate understanding of the defect spectrum of the specific manufacturing assembly process is the key to creating an electrical test and structural inspection strategy capable of delivering the necessary manufacturing quality targets for HDI technology PCBs. Given the restricted ICT access of HDI PCBs, it is important to understand the defect spectrum of the line that is being used to assemble the board. When traditional ICT access is limited, knowing the probability of the defect spectrum can go a long way toward applying the right mix of electrical test and structural inspection methods. Although this approach is equally valid for standard PCB technology, it is very important for HDI boards given the lack of electrical test access. Typical defect spectrums of PCB manufacturing processes will be a mix of structural- and electrical-related defects. For example, if a manufacturing line had a typical defect spectrum (as defined in the following table), to get the most robust process verification capabilities, a combination of electrical test and structural inspection methodologies would need to be employed in order to ensure correct manufacturing of the HDI PCB.

Defect	Defect Type	Probability of Occurrence
Bad Part	Electrical	15%
Wrong Part	Electrical	5%
Misoriented Part	Electrical	5%
Missing Part	Structural/Electrical	15%
Misaligned Part	Structural	15%
Solder Open	Structural/Electrical	30%
Solder Short	Structural/Electrical	10%
Solder Unreliable	Structural	5%

Coupled with the distribution of the different types of defects, component Defects Per Million Opportunities (DPMO) figures can be used to get an accurate predictive yield estimate for the HDI board under evaluation. By applying different test strategies and being able to detect these defects, it is possible to determine which test strategy will deliver the required quality goals on the HDI product.

Utilizing Multiple Test and Inspection Machines

Most electrical test or structural inspection strategies are implemented using a single test or inspection machine on a line for process defect detection. Possibly an AOI machine is used for structural inspection or, if electrical test is required, an ICT machine. However, it is unlikely that multiple test and inspection machines will be used, largely due to cost and line beat rate goals. Given the unique requirements for HDI, implementing an effective test and inspection strategy may require multiple defect detection machines to deliver the quality and cost targets. Knowing which combination of machines to use and how they need to be combined is the key.

Assembly and Test Processes for HDI

In developing a test and inspection strategy, manufacturers understand that no machine can deliver 100% coverage. The major issue with HDI boards is that electrical test machines, one of the staples for PCB manufacturers, will deliver significantly reduced coverage than what is needed due to the reduced bed-of-nails access or sub-optimal boundary scan device availability. Cost pressures are always important. The correlation between the benefit of adding a test or inspection machine and the cost of that machine must be weighed. Another other aspect is the impact on line beat rate to see if the addition of the machine will impact the speed at which the line can assemble PCBs. See Figure 2 for a high level comparison of various test and inspection machines' ability to deliver on cost, speed, and coverage.

For high volumes, adopting a combination of ICT, Boundary Scan, and AOI may deliver the right balance of cost, speed, and coverage. For lower volumes, Flying Probe, Boundary Scan, and AXI may be the right combination. For

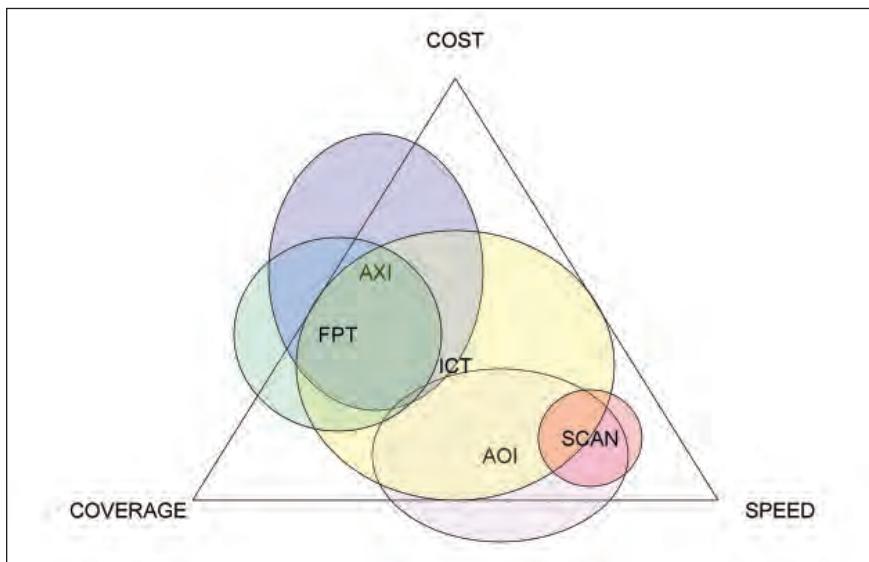


FIGURE 2: Cost, Speed, and Coverage Test and Inspection Comparisons

higher coverage and medium volumes, a combination of ICT with Boundary Scan and AXI may be the right combination. It is difficult to recommend different strategies when there are so many variables that need to be assessed before a final combination can be determined. The following section describes in more detail how to make those assessments and what tools are available to help automate this process.

Defects Per Board and Yield

It is possible to estimate a PCB's final yield using historical DPMO data for both the processes used to manufacture the PCB and the components specified on the Bill Of Materials (BOM). DPMO is a normalized assessment of the defects generated in the PCB manufacturing process. The estimated PCB Defects Per Board is the sum of all the individual DPMO numbers associated with all the components fitted to the board, divided by one million.

The DPMO values for each component may consist of an element that is associated with the component and another part that is associated with each pin of the component. Alternatively, there may just be an overall figure that considers the total DPMO contribution of the component.

For example, working with a PCB with 1,000 components that each have an average DPMO of 250, the total DPMO for this board will be 250,000. To obtain the Defects Per Board, this figure would be divided by 1,000,000. Statistically, for every four boards that are built, one board will have a fault on it. Statistics can be employed to convert this to yield. This is an estimate of the final yield for the PCB.

$$\text{Yield} = e^{-\text{Defects per Board}}$$

In this example, the result is $e^{-0.25}$ or 78%.

Assembly and Test Processes for HDI

Employing a targeted test and inspection strategy on our PCB, we can expect to improve that yield significantly. This simple calculation gives an initial insight into potential yields that can be expected for an HDI PCB given a specific assembly process. In order to assess the impact of a test and inspection strategy on this yield, it is necessary to break down the component DPMO numbers by the percentages in the previous table, which gives the individual DPMO allocated to each type of defect that could occur. If the capability of each piece of test and inspection to detect the defects listed in this matrix is cross-linked to the individual DPMO numbers, the benefit of the specific equipment can be assessed.

For example, if we assume an AOI machine has a 90% ability to detect structural defects, the following analysis can be gleaned for a component with a DPMO value of 250.

Applying this result to our 1,000 component board would produce a final board DPMO value of 81,250 instead of the

Defect	Probability to occur	DPMO contribution	AOI Detection capability	Final DPMO
Bad Part	15%	37.5	0%	37.5
Wrong Part	5%	12.5	0%	12.5
Misoriented Part	5%	12.5	0%	12.5
Missing Part	15%	37.5	90%	3.75
Misaligned Part	15%	37.5	90%	3.75
Solder Open	30%	75	90%	7.5
Solder Short	10%	25	90%	2.5
Solder Unreliable	5%	12.5	90%	1.25
	100%	250		81.25

value of 250,000 that would result without the AOI machine. This would equate to a final yield of 92% instead of 78%. Using the same process, but including ICT with Boundary Scan, would improve these figures even more, showing the advantage of a combined structural and electrical test strategy. The net result of the combined electrical test and structural inspection strategy is a reduction in the number of process escapes.

Automating the Process

Although the described analysis may seem daunting, there are resources available that can automate this analysis. It is possible to approximate these results with a spreadsheet application such as Microsoft Excel. However, as the component count of a board increases, the complexity of calculating defect rates and allocating DPMO becomes increasingly harder.

The *National Electronics Manufacturing Initiative* (NEMI) offers an Excel-based Test Strategy Cost Model that automates a number of the necessary calculations for yield, defect, and cost analysis of PCBs.

ASTER Technologies markets a product called *TestWay* that provides significant benefits over standard Excel spreadsheets. *TestWay* can especially help with electrical analysis on schematic data, which is important for correct design layout on HDI boards.

A product from *Teradyne*, called *Strategist*, can provide defect analysis and yield estimates for printed circuit boards depending on the electrical test and structural inspection methods employed.

The major boundary scan companies, such as Goepel, Asset Intertech, JTAG Technologies and Corelis, have their

own solutions that can analyze test coverage of boundary scan boards. This provides a significant source of analysis on nets that does not require physical test access prior to the layout being started.

Electrical DFT analysis provided by the above products can be combined with such products as Mentor Graphics' CAMCAD Professional that provides physical DFT analysis to get the most out of the limited ICT access of HDI boards.

Improving Testability at Design Time

Trying to improve testability coverage once a board has completed the layout processes will usually result in a suboptimal solution. Incorporating Design-for-Test options during the product design and layout phases can improve the overall testability of the HDI board significantly with little or no overhead in the PCB. Electrical test decisions can make or break an HDI test strategy, so this analysis should be performed as early as possible in the design process, ideally when the schematic is being reviewed and prior to any physical layout beginning. At this time, layout has not started, so all aspects of test and inspection can be incorporated, or at least reviewed, in the context of the other design constraints.

Boundary Scan is defined as an IEEE standard 1149. There are a number of sections to this standard such as 1149.1, which details digital boundary scan. In this part of the standard, the Test Access Port (TAP) describes a set of four or five scan pins that are used to control and program the boundary scan device. In the case of four pins, they are labeled Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK), and Test Mode Select (TMS). There is an optional fifth pin called

Test Reset (TRST) that can be incorporated. Boundary Scan support can provide a wealth of opportunities for increasing testability coverage, provided that the Test Access Port (TAP) is configured correctly. Although this discussion does not go into the detail of boundary scan analysis, references to other materials are provided at the end of the chapter. Some high level descriptions are included for completeness.

Most of the time the various boundary scan parts are correctly chained together, specifically, a connector to the first TDI, TDO to subsequent TDI pins, and ultimately a TDO pin that also goes to an edge connector. Then TMS, TCK, and the optional TRST pins are all connected together in parallel (Figure 3).

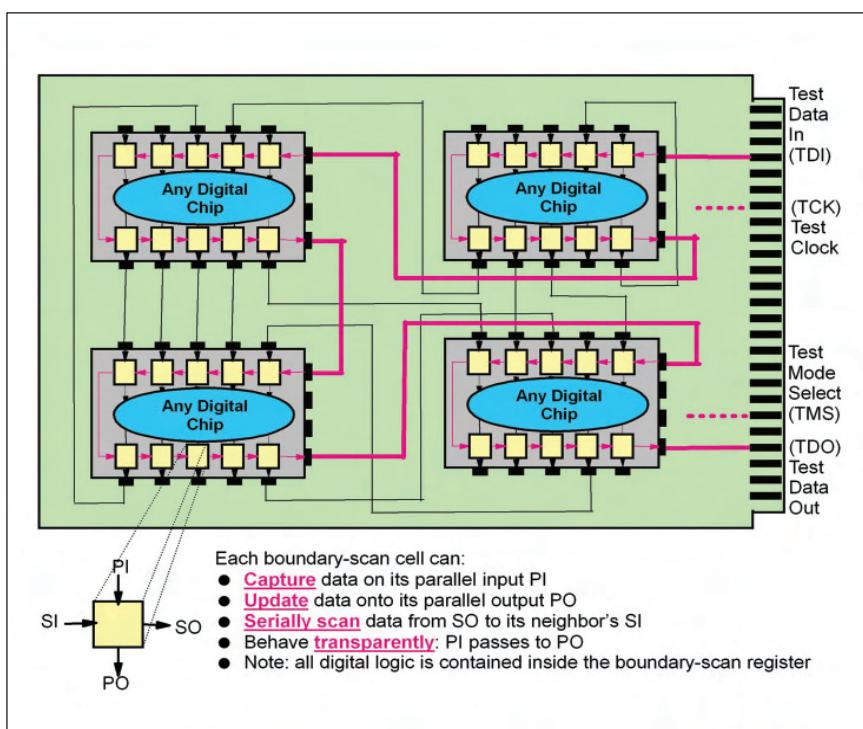


FIGURE 3: Daisy-chaining of boundary scan parts

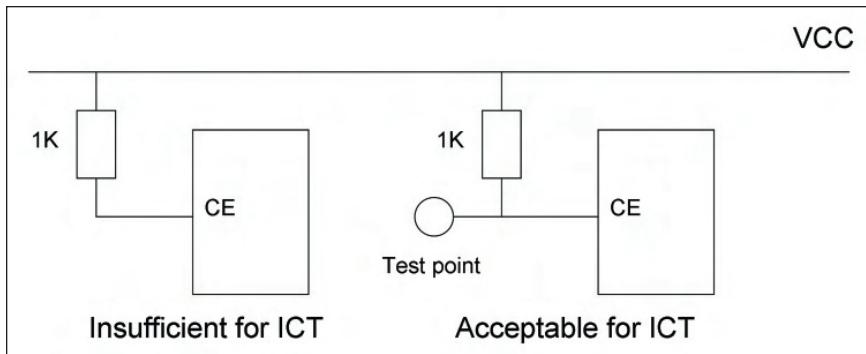


FIGURE 4: Addition of test point to reduce noise during testing

Tristateable Integrated Circuits (ICs) provide a mechanism to disable clocks. Using separate pull-up or pull-down resistors can significantly reduce noise during the test phase and can also eliminate the need for back-driving components to a required state (Figure 4). However, adding pull-up or pull-down resistors alone is insufficient since it does not allow the state of the pin to be controlled without an additional test point on the net between the resistor and IC pin. Disabling on-board clocks allows much lower test frequencies, which result in more reliable tests and a reduction in the number of false failures. Incorporating tristateable buffers or resistor pairs in feedback loops can also increase the testability of the board by making tests run more reliably with less noise.

In an HDI PCB application where boundary scan components are available on the board, there may be unused cells that can be routed to these nets instead of having to place a physical test point. The boundary scan cells act as virtual test points, but without the overhead of a bed-of-nails fixture probe. The aspect of boundary scan capability that can be overlooked is the ability to employ boundary scan cells on pins that are unused in the final design intent. Typically, these pins have a full read and write boundary scan cell on

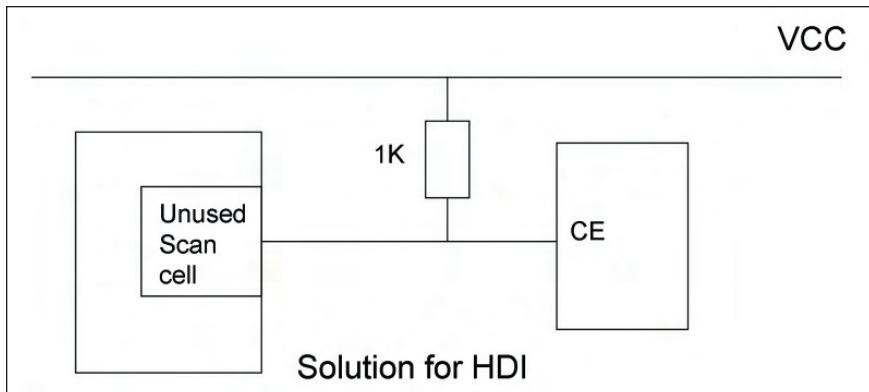


FIGURE 5: Connection of unused boundary scan cell to active net

them and can be used for complete driver/sensor testing of an active net on the board without the overhead of placing a test point on the layout. It is not unusual to be able to assign a significant number of nets that require access to their own unused pins purely for testing purposes. Once connected in the schematic, boundary scan analysis tools can utilize these cells to test for shorts, opens, and component faults. This scenario can be particularly useful in breaking up the testing of a non-boundary scan cluster into smaller clusters that help to confirm good boards while improving the diagnosis of bad boards.

If a digital net has a bi-directional boundary scan cell associated with it, any short in this net can be detected with any other accessible net. If all digital pins have either drive and/or sense capability on the net, the pins can be additionally tested for stuck-at faults and open pin defects. In this scenario, a bed-of-nails probe does not increase test coverage of this net, so it does not require a probe to be assigned. As a result, the test point can be saved.

If non-boundary scan components lie between boundary scan parts, it may be possible to perform some form of cluster

test of the non-boundary scan parts using the boundary scan cells. Depending on the complexity of the cluster being tested, diagnostic resolution may be reduced, but passing the test would confirm that the circuitry is performing correctly. Additional diagnosis may be required in the event that the test fails.

Bundled components such as resistor arrays, diode arrays, and multiple element gates, such as 7400s, can be tested using a sampling technique. Adding test access to one element of the component for electrical verification can ensure that the correct value or functional gate is connected to the board. The addition of AOI or AXI to inspect all the joints on the component ensures that all the pins are electrically connected to the PCB, giving a high level of confidence in the component with significantly reduced test point requirements.

Summary

There is no doubt that HDI printed circuit boards are pushing the boundaries of existing test and inspection technologies. However there are solutions to many of these issues, provided that good DFT practices are used early in the design process so that they can be incorporated into the final layout.

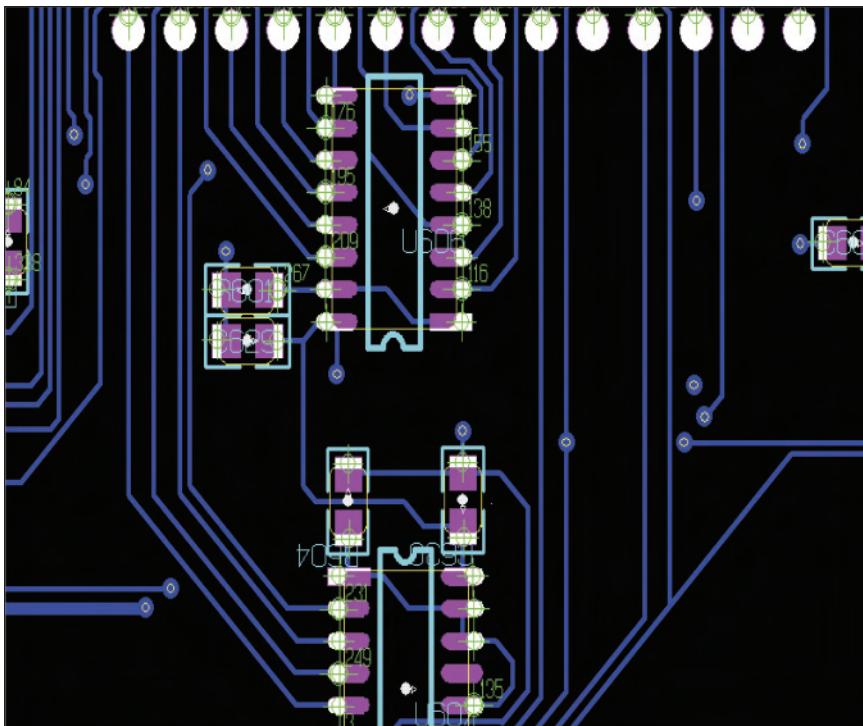
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14

Embedded Components

By Happy Holden and Per Viklund —
Mentor Graphics

Standards and References

Embedded passives (EP) offer many advantages over the use of discretes. However, the performance requirements, range of resistor and capacitor values, and product size targets dictate when it is best to implement these passives as embedded or discrete. This chapter will introduce the various materials and manufacturing techniques used to create embedded passives. It will also, through the use of test cases, show the cost, performance, and size trade-off parameters and indicate when and how to best utilize this emerging technology.

Any discussion on embedded components (EC) should start with notes to references on standards. The IPC has a new document, *IPC-2316 - Design Guide for Embedded Passive Device Printed Boards, published in March 2007*. This 44-page document contains 8 sections:

1. Scope
2. Applicable Documents
3. General Introduction
4. Embedded Resistors
5. Embedded Capacitors
6. Inductors
7. References
8. IPC Published Papers

Embedded Components

It provides details about EP materials, design, and manufacturing processes. The Reference section has over 34 references that can help you, including some that go back to 1955. There are also references to IPC published papers and conferences.

Introduction

One of the largest categories in electrical components is discrete passives. Historically, these existed long before active devices and have been mounted on the outside of printed circuits boards, either with through-hole leads or with terminations all on a single side (surface mount) with the interconnection traces embedded on the inside or outside of the board. Increasing density of components has created a competition for this valuable surface real estate and new technology has been developed to embed electrical components inside the board. The earliest of these was in the 1970s when resistors were first used on military and spacecraft. These resistors were made by etching a pattern on a sheet of resistive material and then connecting them with the rest of the circuit through the standard multilayer process. Inter-plane dielectric layers between power and ground have been used since the early 1980s to reduce power supply noise, but only since the 1990s to replace decoupling capacitors. Etching of copper coils to replace inductors has been used since the early 1960s. Assembly techniques have expanded to include the ability to place very small, discrete surface mount technology (SMT) passive components inside the board which permits the normal multilayer board pressing operation to encapsulate these “placed” components. SMT now includes active devices, like transistors and integrated circuits, similar to the original buried IC-MCM technology developed by GE

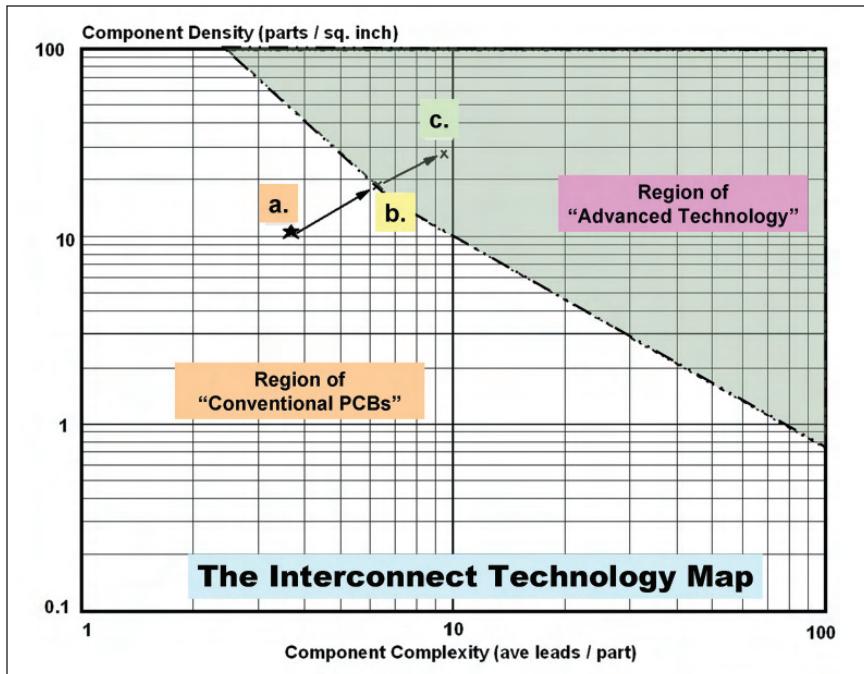


FIGURE 1: The Interconnect Technology Map shows the effect of component density on PCB technologies. The “Region of Advanced Technologies” includes densities that will require microvias and embedded passives. (Courtesy of *Printed Circuits Handbook-5th Edition*, Coombs, McGraw-Hill, 2001, p. 1.5)

Federal Systems in 1997. The effect of increased density and discretes can be seen in Figure 1. Point (a) is a lower-density PCB that has enough room for SMT land patterns, traces, and via-holes. Point (b) is the maximum number of components that will fit on a through-hole PCB. Point (c) is in the region of advanced printed circuit technologies like microvias and embedded passives, where there is not enough room for all the components and vias.

The Ultimate Embedded Component Substrate

The semiconductor roadmap shows ever-decreasing gate geometry. Portable consumer products need to provide more

Embedded Components

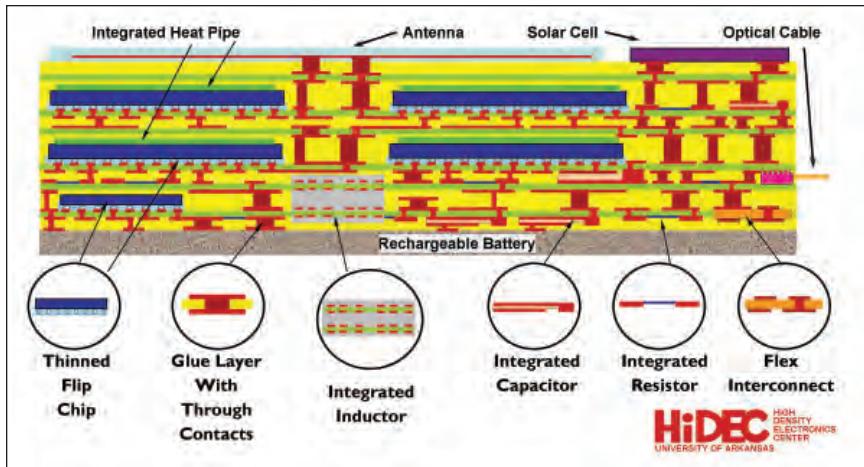


FIGURE 2: Cross section of a future multilayer board showing the use of all types of embedded components, both passive and active (Courtesy of HiDEC-Univ. of Arkansas)

functionality. These two trends will increase PCB density, but at the same time, decrease the size and weight of products. The result is projected by HiDEC (University of Arkansas) to be a fully-integrated substrate that provides all of these functions, as shown in Figure 2; battery, antenna, solar cell recharging, optical inputs, sensors, integrated cooling, flex connections, active ICs and transistors, inductors, capacitors, and resistors.

Alternative Applications and Trade-offs

There are a number of alternatives for solving the problem of higher component density and better high-frequency electrical performance. In addition to embedding components, there are now smaller SMT components that can be assembled onto inner-layers of a multilayer. Several factors must be considered when deciding whether to use embedded components or not. Use of discrete components whether on the surface or placed inside the board involves incremental costs. However, the trade-off is that the cost of fabricating one formed embedded component is about the same as that of

forming an entire layer of those components. Another factor to consider is that surface mount components can have the same size and shape for widely different electrical values. Widely differing electrical values may require more than one layer of embedded materials.

Smaller SMT Components

New smaller SMT components have been introduced. As seen in Figure 3, these are 0101 (0.4 x 0.4 x 0.4 mm) and the smaller, 01-005 (0.4 x 0.2 x 0.2 mm). These components can be mounted on the surface or inside the multilayer board. They are small enough to be attached to the traces of inner-layers and then encapsulated by the prepreg during lamination.

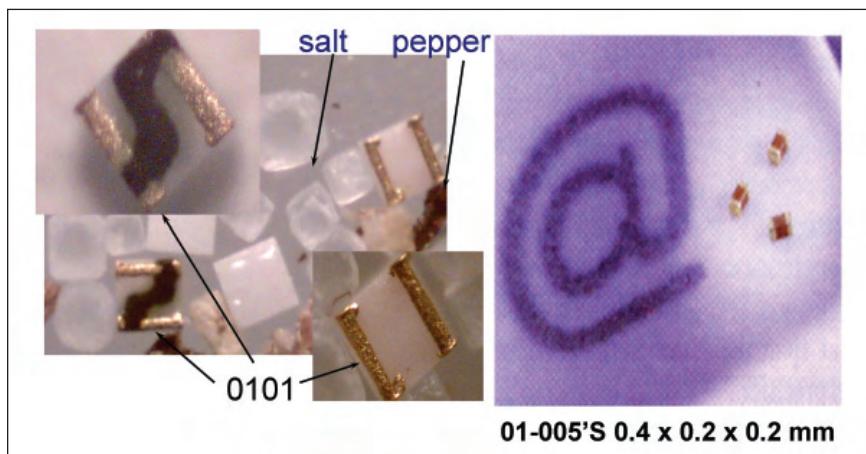


FIGURE 3: New smaller SMT resistors and capacitors in 0101 and 01-005 form size

Stacking Components

A new trend is also developing that allows assembly to stack discrete components. This is quite common for stacking IC dies and then using three-dimensional wire-bonding. But 3-D stacking of discretes involves special soldering processes.

Embedded Components: Advantages and Disadvantages

There are several advantages to embedding components inside the board:

- Reduction in board area (enabler) - The surface area saved by moving components inside the board can result in a smaller board. Reduction in board size can result in more boards per panel.
- Increase in functionality, higher density (enabler) – Additional functionality and density can be achieved by adding more components to the inside of the board.
- Improvement in performance (enabler) - By embedding components, shorter interconnect lengths (lower inductance) and smaller terminations (also lower inductance) allow for higher speeds with lower noise.
- Elimination of solder joints - Any embedded component will eliminate the SMT solder joint which will potentially improve the reliability of the assembly, especially for the higher temperature lead-free solders.
- Improvement in total assembled costs - System cost is the key. The higher board prices from materials, process, and test are often offset by a lower bill-of-materials purchased, assembly costs, and even smaller board size.

There are also disadvantages to embedding components:

- Quality can be affected. In particular, meeting tolerances can be more difficult.
- Trimming embedded resistors is slow and expensive.
- The design is “parametric” where designers size components.
- Certain technologies are not capable of duplicating discrete components, especially capacitors ($>100 \text{ nF/cm}^2$).

- Sheet materials come in only limited ranges.
- The cost of prototypes can be high.
- Sheet resistors cost the same whether one or thousands are made.
- Test tools are expensive.
- Rework is not possible inside the board.
- Screen printed components require additional capital investment.

Cost Trade-Offs

EDA tools will help decide what components can be embedded but will not calculate the cost trade-offs. The fixed costs for embedding components depend on the materials selected, their fabrication and test costs, and the number of EPs designed for the board. This is a traded-off against the variable cost of discretes and their assembly costs. The more EP that can be buried, the better the trade-offs will be, ignoring any size reduction (Figure 4).

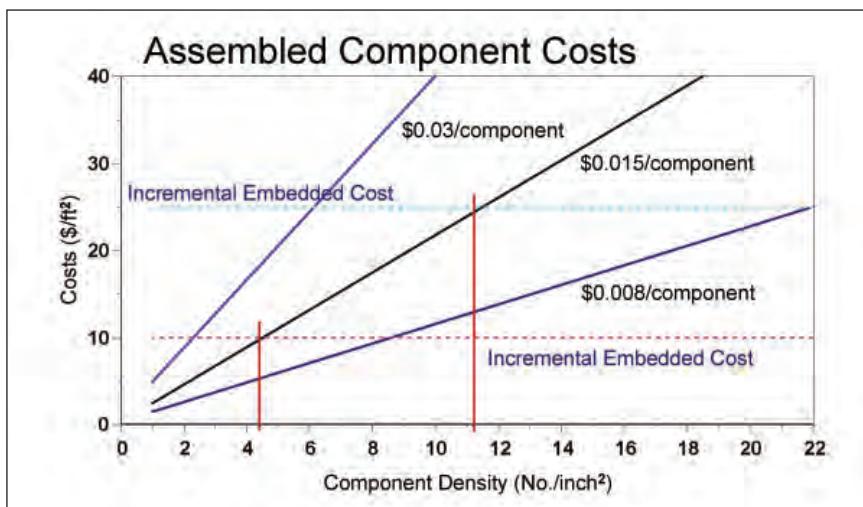


FIGURE 4: Embedded formed components trade-off between subtractive and additive EP technologies, their density, and conventional surface mounting (Courtesy of Richard Hartley, PCDesign-West, 2005)

Example

A simple example best illustrates the trade-off advantages of embedded components. A case study performed and reported by Richard Hartley deals with a telecom board

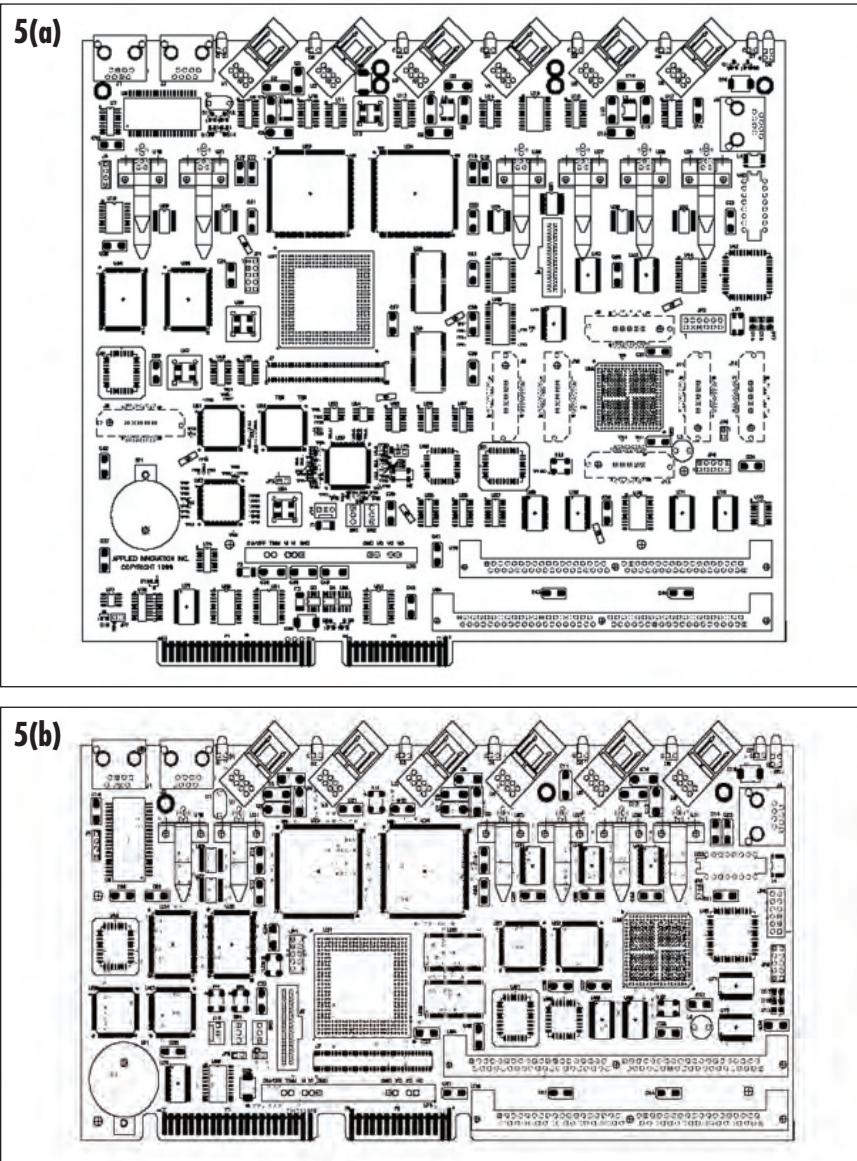


FIGURE 5: Examples of EP (a) Original 10-L SMT board (9.0" X 10.25") and; (b) Smaller version (5.2"X 10.25") (Courtesy of Richard Hartley, PCDesign-West, 2005)

of unusual size for a production panel.[1] The “Alflex Concentrator Card” from Applied Innovation was initially 9.0” x 10.25” and a 10-layer board. This could only fit 4-up on a 21” x 24” fabrication panel. The original board can be seen in Figure 5(a) and the final version in Figure 5(b). The characteristics of this board were:

- 9.0” X 10.25,” 10-layers, FR-4, 0.062” thick;
- 1,279 total SMT components on both sides;
- 746 resistors;
- 363 capacitors;
- 88 ICs;
- 83 transistors, diodes, inductors, and connectors.

Redesign Solution

- Selected 500 ohm/square thin-film laminate
- Length:Width aspect ratio of 1:10 to 24.8:1 gave resistor values ranging from 50 ohms to 12.4 K ohms. All EP resistors were placed on the Power Plane Layer.
- 579 resistors were embedded corresponding to 10.1/sq in
- The space savings allowed the board to have a reduced dimension of 5.2” X 10.25” and be placed 6-Up on an 18” x 24” production panel.

Cost Savings

• Production Panel Cost	Original: \$378	EP Board: \$325
• Boards per Panel	4	6
• Cost of Embedded Resistors	--	per panel: \$ 96
• Cost per Board	\$95	\$70
• Cost Savings – Bare Board	--	\$25
• Cost Savings – Components (579 x \$.03)	--	\$17
• Total Cost Savings	--	\$42

Embedded Components

Lower cost will result from a smaller choice of board fabricators for the EP board and engineering change orders (ECOs) will require design (artwork) changes.

Materials

The embedded passive materials come as bulk sheet resistances, additive screen printed pastes, additive plated thin-films, deposited dielectrics as capacitors, materials that can form capacitors, or materials that can be roller-coated or inkjet printed onto the inner-layers of a board as capacitors.

Resistors

Resistors, discrete or formed, are actually very poor conductors when compared to copper. Their function is to restrict the flow of electricity in a circuit. The common compositions of resistors include metal oxides, carbon particles, or small conductive particles separated widely by an organic polymer. Conventionally, the value of a resistor is rated in ohms (Ω). For embedded resistors, the materials are classified by their ohms per square ($\Omega / \text{sq.}$). Table 1 shows the five main types of EP resistor technologies. The actual range of resistance values is shown in Table 2. Seven decades of resistance ohms per square ($\Omega / \text{sq.}$) are available on the market. The middle three technologies; screen printed PTF, ceramic thick-film (CTF), and additive plating, are additive and

PROCESS	TECHNOLOGY
Photoprint (Sheet resistor material)	Thin-film etch (NiCr, NiP, NiCrAlSi, Pt)
Screen or stencil print	Polymer thick-film addition (PTF)
	Ceramic thick-film addition (Cermet)
Plating	Selective addition
Inkjetting	Selective addition
Photoimageable	Photopolymer (filled)

TABLE 1: Embedded formed resistor supplier types

Resistance in Ohms/square	10	100	250	1k	10k	100k	1m
Photoprint (NiCr, NiP)	X	X	X				
Photoprint (NiCrAlSi)				X			
Photoprint (Pt)		X	X	X	X		
Screen or stencil print (PTF)	X	X	X	X	X	X	X
Screen or stencil print (Cermet)	X	X	X	X	X	X	X
Plating (NiP)	X	X	X				
Inkjetting	X	X	X	X	X		
Photoimageable discrete	X	X	X	X	X		

TABLE 2: Embedded formed resistor ranges

can be modified or mixed to have any intermediate value of ohms per square.

Resistor Fabrication Process

The EP resistor fabrication process, as shown in Figure 6, consists of a series of process steps:

1. Starting with the copper clad material, apply photoresist using artwork that defines the resistor and terminals, expose the photoresist, and develop the image.
2. Etch the copper foil and resistive layer with cupric chloride etching solution or other approved etchant.
3. Strip the photoresist.
4. Apply photoresist using artwork that defines the resistor only, expose the photoresist, and develop the image.
5. Selectively remove the copper over the resistors using an ammoniacal etchant.
6. Strip the photoresist.

Capacitors

Capacitors are needed in a great range of values. Capacitors can be conventional discrete or a whole capacitance sheet may be used for distributed capacitance. Distributed capacitance is

Embedded Components

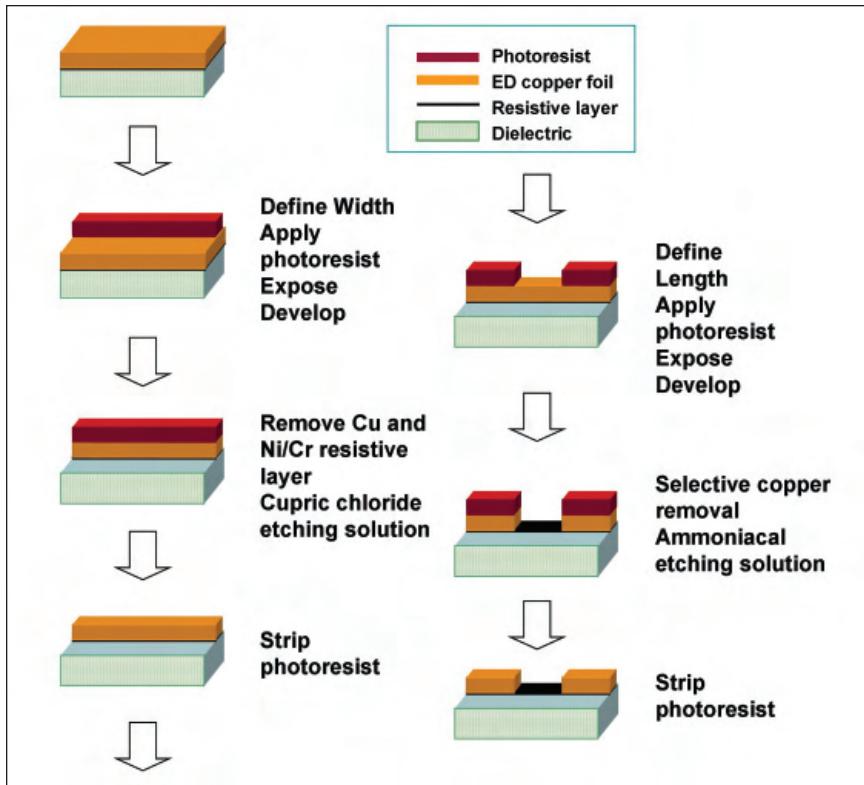


FIGURE 6: Embedded resistor manufacturing process

the storage of energy between the power and ground layers by employing a dielectric. This is Faraday's Law which indicates that capacitance is inversely proportional to the distance between the two parallel planes and proportional to the material's dielectric constant. In addition to offering a method of storing energy for fast-switching components, distributed capacitance will also couple power to ground and provide lower power supply impedance. Noise on the power bus can be attenuated in this way. The various technologies for EP capacitors are shown in Table 3.

Table 4 outlines the various capacitances available which can be used for individual buried capacitors or for the bulk distributed capacitance.

PROCESS	TECHNOLOGY
Photoprinting on etched copper planes (Sheet capacitor material)	FR-4/glass, copper clad laminate Polyimide (unfilled) copper clad Polyimide (filled) copper clad Proprietary dielectric (filled) copper clad Epoxy (filled) copper clad
Screen or stencil printing	Polymer thick-film addition (PTF) Ceramic thick-film addition (Cermet)
Inkjetting	Selective addition
Photoimaging	Photopolymer (filled)
Emerging	Sol gel formation

TABLE 3: Embedded formed capacitor supplier types

TECHNOLOGY	DIELECTRIC CONSTANT	THICKNESS (microns)	Capacitance per sq cm area
FR-4, copper clad laminate	4.4	50	78 pF
		24	155 pF
		16	250 pF
		12	300 pF
		8	480 pF
Epoxy (filled) copper clad	10	12	700 pF
		16	850 pF
		30	1700 pF
		3.5	122 pF
Polyimide (unfilled) copper clad	3.2	12.5	250 pF
Polyimide (filled) copper clad	10	25	350 pF
Proprietary dielectric (filled) copper clad laminate	22	8	3000 pF
Polymer thick-film	35	12	3000 pF
Ceramic thick-film	35,1500-2000	25	23nF, 93 nF
Photopolymer (filled)	22	11	1500 pF
Sol gel formation	150	0.5	150-300 nF

TABLE 4: Embedded formed capacitor technologies

Capacitor Fabrication Process

The EP capacitor fabrication process is similar to the EP resistor fabrication process. Normally, embedded formed polymer capacitors are made from purchased sheet dielectrics clad with copper foil. It is difficult for the board fabricator

Embedded Components

to apply a liquid dielectric precisely to laminate, but one photolithographic capacitor formation technique has been developed. Unneeded dielectric is removed with a developer solution similar to liquid photoimageable solder mask.

Advanced Materials

Research and development are continuing on EP materials. New materials available today include two-resistance cores and resistance-capacitance cores. One of these is illustrated in Figure 7. Chapter 5 – Materials for HDI has more details on these materials.

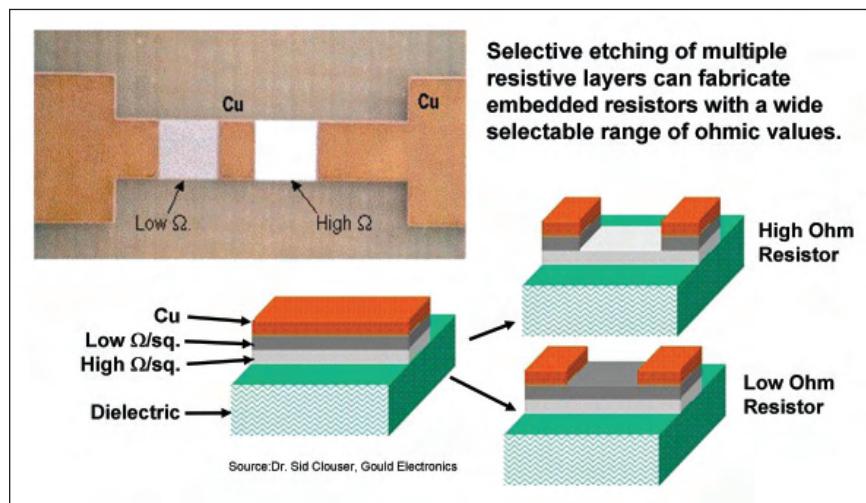


FIGURE 7: Embedded formed resistors' ranges (Courtesy of Sid Clouser, TICER Technologies)

Active Integrated Circuit Fabrication

Manufacturing of formed embedded active devices was first developed in 1995 for the military and was labeled *chips-first*. The ICs were placed along with discrete components and then the substrate was fabricated over the components. Laser drilling interconnected the IC chips and components to the

substrate wiring. This technology was later trademarked HDI. Polymer semiconductor radio frequency identification (RFID) tags are one example of HDI technology in use.

Embedded Actives

3-D Embedded Actives (EA) is rapidly evolving as the next technology to improve functionality and performance while maintaining a compact form-factor. EA will play a major role in all of these 3-D schemes. EA will not only improve density but will enhance electrical performance by reducing signal integrity noise and stabilizing the power distribution.

EA adds significant complexity to the design and, with that, a significant risk for failure unless tools and processes

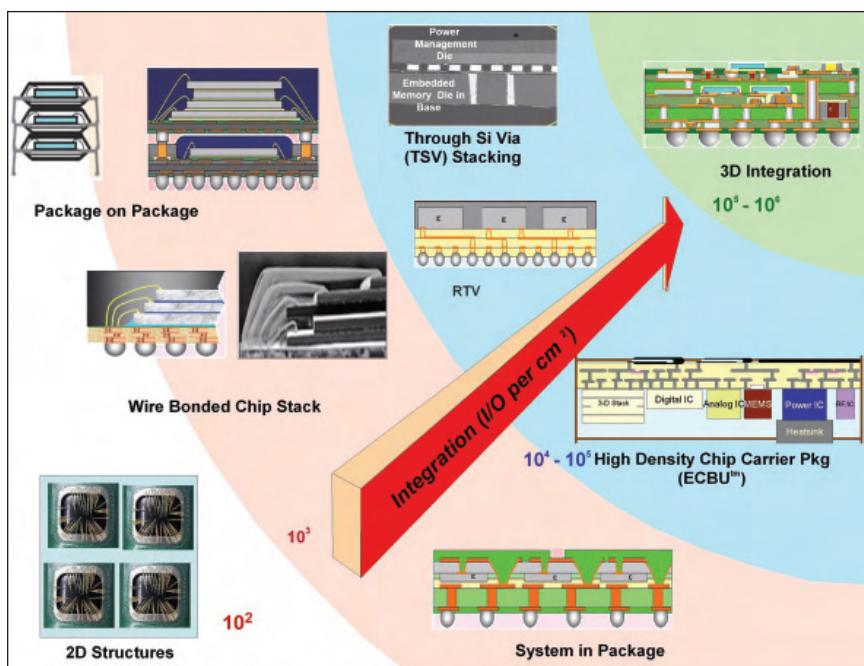


FIGURE 8: The waves of increasing interconnect density show the effect of 2-D to 3-D stacking technologies. System-in-Package (SiP), Package-on-Package (PoP), Through-Silicon Vias (TSV), Reverse Thru Via (RTV) and High-density Chip Carriers (EBCU) are leading to true 3-D package integration.

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can help manage the complexity. Until recently no such tools existed and all EA design was performed completely by hand or somewhat assisted by custom scripts. Although the technology has existed since the early 1990s, it has just now become more widespread. One reason the technology has not been adopted more universally is the lack of methods and tools to manage the design complexity.

The effect of increased interconnect density can be seen in Figure 8 which shows that the rapid increase in connections per square centimeter, from 10^2 to nearly 10^6 , has created waves of more and more complex 3-D packaging, as a function of different stacking architectures.

Alternatives, Applications, and Trade-offs

There are a number of alternatives for solving the problems of higher component interconnect density and better high-frequency electrical performance. In addition to embedding

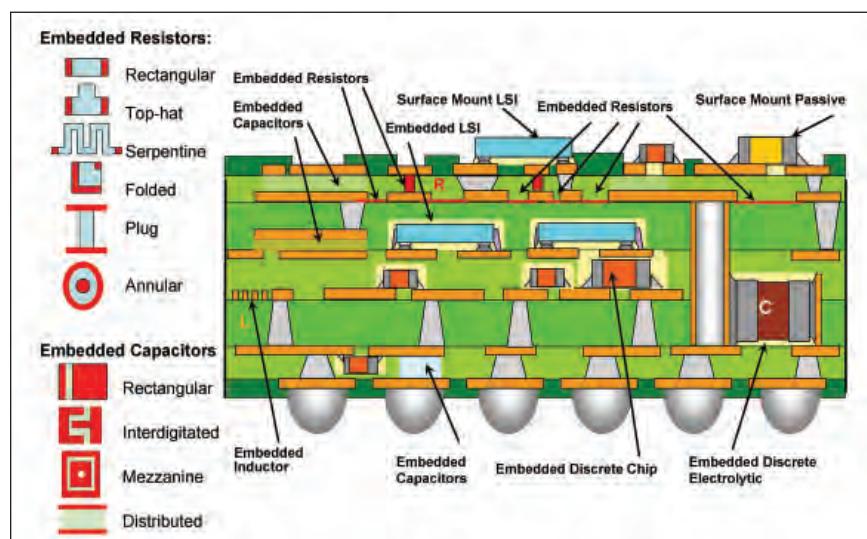


FIGURE 9: This cross section of a future 3-D package shows the use of all types of embedded components, passive and active, formed and discrete, assembled. The six forms of embedded resistors and four capacitors are diagrammed.

components, there are now smaller SMT components that can be assembled onto inner-layers of a package. Widely differing electrical values may require more than one layer of embedded materials.

Typical Applications

Figure 9 shows a hypothetical 3-D embedded active. It shows the use of all types of embedded components, passive and active, formed and discrete, when fully assembled. The six forms of embedded resistors and four capacitors are diagrammed.

Resistors:

- Rectangular
- Top-hat
- Serpentine
- Folded
- Plug
- Annular

Inductors:

- Serpentine
- Spiral
- Interleaved
- Interdigitated

Capacitors:

- Rectangular
- Interdigitated
- Mezzanine
- Distributed (for power supply impedance and replacement of decoupling caps)

With the addition of embedded coils and inductors, the use of 3-D EAs creates quite an opportunity for increased component and interconnect density.

Various 3-D Embedded Active Schemes

There are two main categories of 3-D EA schemes; stacked die and stacked packages. Stacked die are involved in System-on-Chip (SoC) with or without Through-Silicon-Vias (TSV)[2] and System-in-Package (SiP). Stacked packages are Package-on-Package (PoP)[3] and, in a way, Verdant's new OCCAM Process.[4] These are all discussed in Chapter 16 – Advanced Packaging and System-in-Packages.

EA is a growing application that has at least six variants:

- Redistributed Chip Packaging (RCP) – Freescale [5]
- Bumpless Buildup Layer (BBUL) – Intel [6]
- Embedded Chip (IEC) – Fraunhofer IZM [7]
- Integrated Module Buildup (IMB) – Imbera [8]
- Embedded Chip Buildup (ECBU) – GE [9]
- OCCAM Process – Verdant Electronics [4]

Applications

Why all this activity? Printed circuit boards (PCBs) have been too slow to miniaturize and poor in their electrical performance. By mounting a memory chip using TSV on a processor chip, a 1,000-fold increase in speed is possible while gaining a 100-order decreased magnitude in power consumption. As you can see in Figure 8, the driving force is an increase in interconnect integration. Conventional 2-D structures gave us ~100 I/Os per cm^2 (645 I/Os per sq in). Stacking packages with wire bonding or flip-chip has raised that to 1,000 I/Os per cm^2 . But various 3-D high-density direct connect schemes provide 10,000 to 100,000 I/O per cm^2 . Ultimately, full 3-D integration will provide up to one million I/Os per cm^2 . The lowly TH PCB now delivers around 20 I/Os per cm^2 (120 I/Os per sq in). Even high-density HDI can usually only serve up to 105 I/Os per cm^2 (660 I/Os per sq in).

in) which is why the OCCAM Process has surfaced. As a direct HDI connect to components without soldering, it can support the need for I/O connections up into the thousands of I/O per cm^2 (6,450 I/Os per sq in). Figure 10 shows the six 3-D EA technologies described below.

In an embedded chip fabrication approach, bare chips are located under or within the interconnect structure that is used to fan the chip pads out to the package or carrier I/O pads. These can be found in single-chip, chip-scale, and BGA carrier versions, in multichip System-in-Package (SIP) versions, and in 3-D stacked versions.

Redistributed Chip Packaging (RCP) – Freescale:

RCP is a direct connection technology of the *chips-first* variety. The substrate is eliminated and the components have the package built or integrated around the assembly or die using semiconductor processes rather than standard substrate types of processes. This provides higher densities while reducing the foot-print and any soldering or wire-bonding requirements. It uses a photodefinition polyimide dielectric to form vias rather than laser ablation as seen in Figure 10a.[5]

Bumpless Buildup Layer (BBUL) – Intel:

A number of embedded chip approaches start by molding the bare chips into a carrier. Dielectric layers are formed over the chip face using liquid dispensed polymeric dielectrics and vias to chip pads formed through the polymer using either photodefinition or laser ablation. The surface vias are metallized and patterned to form the first interconnect layer and to make a direct metallurgical connection to the chip pads. Additional interconnect layers are added by repeating these steps. The Intel Bumpless Buildup Layer (BBUL)

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embedded chip technology targeting high-end microprocessors is typical, as seen in Figure 10b.[6]

Embedded Chip in Polymer (ECP) – Fraunhofer IZM:

The embedded chip structure along with a thinned chip (~20mm) are placed on a PC substrate and overlaid with a buildup interconnect structure, as seen in Figure 10c.[7]

Integrated Module Buildup (IMB) – Imbera: Based on the embedded 3-D work of the University of Helsinki, IMB places thinned chips into cavities in the PC board prior to encapsulation. After encapsulation of the chips and other components, microvias are formed to connect the chip pads and components, as seen in Figure 10d.[8]

Embedded Chip Buildup (ECBU) – GE: Another embedded chip approach was developed by GE Central Research for multichip applications. ECBU has been applied to

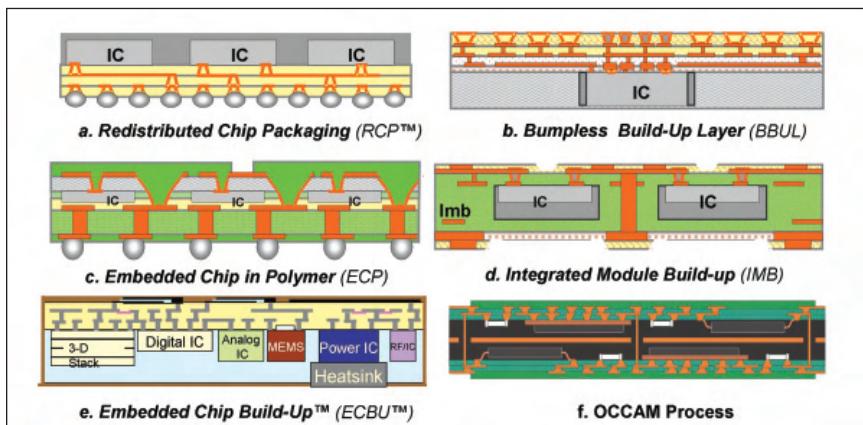


FIGURE 10: Various 3-D EA technologies include: (a) Redistributed Chip Packaging; (b) Bumpless Buildup Layers; (c) Embedded Chip in Polymer; (d) Integrated Module Buildup; (e) Embedded Chip Buildup; (f) The OCCAM Process from Verdant Electronics. The direct connection for the board is built over the components resulting in the elimination of solder and the need for SMT land patterns.

both chip scale and BGA carrier applications with embedded passives, as seen in Figure 10e.[9]

OCCAM Process - Verdant: The OCCAM Process from Verdant Electronics, seen in Figure 10f, is a *components-first* technology rather than a *chips-first* technology. The direct connection for the board is built over the components, eliminating solder and SMT land patterns. The resulting density is much higher, interconnect complexity is reduced, solder joint reliability is a non-issue, and cost is lower.[4]

Performance

Power Supply Noise

The electrical performance of EP resistors and capacitors is nearly identical to their discrete SMT counterparts. Distributed capacitance works much differently than decoupling capacitors; although both can serve the same function. EP components' performance is enhanced if the buried components are connected using blind vias instead of through-hole vias due to the lower series inductance of the blind vias.

The noise profile curve shown in Figure 11 on the 1.5V power distribution compares a 3-mil FR-4 core separating power and ground to the new 7-micron ceramic materials separating power and ground. The TV is a Hewlett-Packard MIPS R14K processor daughter card operating at 550 MHz with 9 secondary cache SRAM's @ 275 MHz.

Summary of Test on Board Noise Levels:[10]

- Typical board with PWR/GND not coupled: +18 dB
- H-P Test Board with 3-mil FR-4 and no HF bypass capacitors: +6.8 dB

- H-P Test Board with 3-mil FR-4 and 4 HF bypass capacitors: +0.0 dB
- H-P Test Board with 8-um ceramic and no HF bypass capacitors: -.6.5 dB
- H-P Test Board with 8-um ceramic and 4 HF bypass capacitors: -7.1 dB
- A reduction of ~ 14 dB with the use of ultra-thin power-ground core
- A reduction of ~25 dB compared to no power-ground coupling

All of the capacitor technologies outlined in Table 4 are suitable for this function.

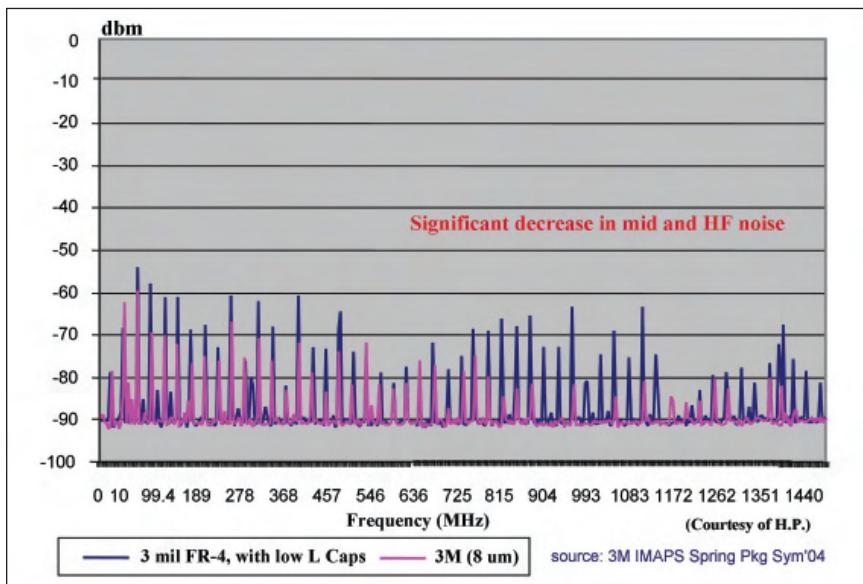


FIGURE 11: Power bus (1.5V) noise vs. frequency using ceramic dielectric instead of 3-mil FR-4 (Courtesy of 3M IMAPS Pkg Sym'04)[10]

Power Supply Impedance

Any embedded capacitor materials, when not used as individual capacitors, can serve as energy storage and

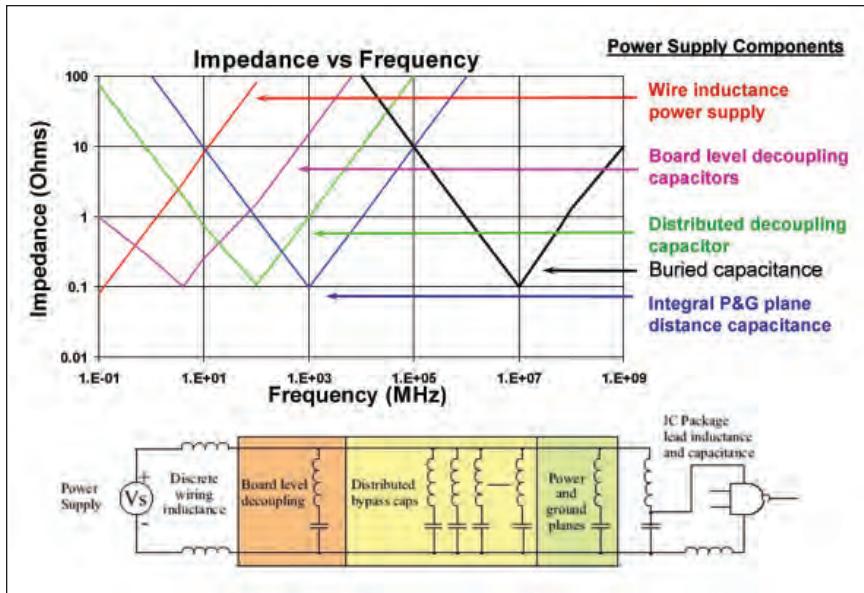


FIGURE 12: The impedance profile of the power distribution network (PDN) is affected by the inductances and capacitances of each component in the PDN, but changes with frequency.

decoupling for the power supply network which is covered in Chapter 4 – Electrical Performance; Figure 15. The materials and their performance are detailed in Chapter 5 – Materials for HDI. Copper plane pours can be employed for power and ground, with appropriate vias connecting to those assigned planes. The resulting capacitance will reduce the PDN's high-frequency impedance as seen in Figure 12.

Design

Introduction

Embedded Passives (EP) as a technology is nothing new. It is a technology from the 1970s that, for various reasons, has been used predominantly in military and aerospace applications. The market drivers of today have shifted the

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center of gravity from these low volume, ultra-advanced military/aerospace boards into huge volume, low-cost, consumer electronics. Still the adaptation has, until now, not been widespread and one reason is the lack of design tools.

Designing with EPs adds significant complexity and thereby also risk of failure. In the traditional design methodology, all phases of EP design were made by hand and sometimes assisted by custom scripts. In this section, we will look at the EP design process and how design tools can help manage the complexity and mitigate the risks. We will limit the discussion to resistors but the principles are very similar for embedded capacitors.

Start Early

The biggest visible impact of EP is the board design phase. However, to be successful with EP, design must start much earlier, instead of during layout. In fact, EP impacts every step, from early planning to product shipping. Recognizing this fact is the first step toward success.

In the design process, a surface mounted component can easily be changed into an embedded passive. So why is it important to start early? There are several reasons. First, The EP board or substrate design has to be targeted toward a specific board shop and be set up to their process rules. Once designed to these rules, retargeting to another supplier is difficult. Therefore, selection of board manufacturer has to be one of the first steps.

Secondly, the circuit design will also impact the EP design. For example, in circuit design the absolute component value is seldom as critical as the relationship between components in the circuit. EPs without trimming will have a tolerance of around 15 to 20 percent, but most circuit designers would

object and demand higher accuracy. However, if two resistors are used in a voltage or current divider application, the ratio between the two is much more critical than the actual nominal component value. Some EP materials and processes can handle the ratios on the same board within 3 to 10 percent because all components are manufactured in the same manufacturing step. This correlated tolerance is more important and if a circuit designer, just by old habit, picks 1 percent E96 standard value resistors from the corporate database, unnecessary requirements are put on the EP design with added cost as a consequence. Instead, the designer should enter the actually desired component value and the actually required correlated tolerance.

Finally, manufacturing and test of the boards also impact how EPs are designed. For example, if the resistors are to be laser trimmed, then several factors need to be considered during EP design. First, the type of probing needs to be determined. For low volume applications, flying probe testing can be optimal. The prime concern is to make sure the probes have access to the resistor but don't obscure the view of the laser.

For large volume applications, fixed probing is almost always used. All probes make contact at the same time and we need to ensure that none of the probes obscure the view of the laser. It is also important to remember that a typical laser trimmer has a scan lens window of around 80x80 mm. Unless all EPs are to be trimmed to fit inside that window, multiple probe cards will be needed. The only way to achieve these goals is to co-design the probe card with the EP design.

Process Parameters

As already mentioned, a board manufacturer has to be selected early. A manufacturer who has already had

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experience with the EP materials you intend to use, and who can supply you with the needed process parameters, is typically a good choice. There are a multitude of parameters you need to obtain from manufacturers and if they can't supply you with them, one can have doubts about their previous experience with EPs. Parameters you should demand depend on the type of resistors in use.

Parameters for thick-film resistors and additive thin-film include:

- printing/plating thickness;
- pad size: side extend, minimum pad width, overlap;
- over-sizing overglaze (protective coating);
- minimum resistor body width*;
- untrimmed tolerance capabilities;
- trim factor (percentage of nominal resistance value to design in order to allow margin for trimming);
- minimum resistor width remaining after trimming;
- restrictions on how resistors can be rotated;
- resistance matrix for each material;
- ohms per square values at various resistor width and length dimensions.

** It is preferred to have different widths for different tolerance requirements. The larger a resistor is, the less impact manufacturing variances will have on the nominal value. In addition, if laser trimming is required, the resistor needs to be large enough for trimming.*

For all additive processes, the pad parameters can have a profound impact on tolerance. As the resistor material is added in a separate process step, it will have some misalignment with the pad pattern. Depending on how the pad parameters are set up, this misalignment can result in differences in contact area

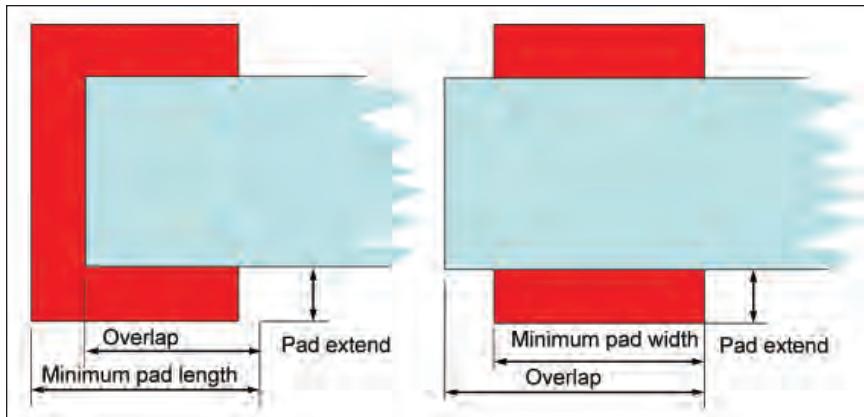


FIGURE 13: The terminals on an EP must be larger than the component by an overlap equal to the maximum manufacturing registration tolerances.

between the pad and the resistive material.

Figure 13 is an example of a pad set-up that allows for some misregistration without changing the contact area. The downside is added size. It is clear that a left-to-right or up-and-down shift less than the overlap will have zero impact on material overlap. For thin-film subtractive technologies, we have other requirements grounded in a much different manufacturing process:

Parameters for thin-film resistors (subtractive technology) include:

- **pad size: side extend, minimum pad width and overlap;**
- **over-sizing the resistor definition mask;**
- **minimum resistor body width***;
- **untrimmed tolerance capabilities;**
- **trim factor (percentage of nominal resistance value to design in order to allow margin for trimming);**
- **minimum resistor width remaining after trimming;**
- **restrictions as to how resistors can be rotated, if any.**

* It is preferred to have different widths for different

tolerance requirements. The larger a resistor is, the less impact manufacturing variances will have on the nominal value. In addition, if laser trimming is required, the resistor needs to be large enough for trimming.

In both cases, we strive to have small resistors, but the impact is typically on tolerance. The smaller the resistor is, the larger impact the manufacturing variances will have on tolerance.

For thin-film subtractive processes the over-sizing of the resistor definition mask is critical. In a separate process step, the mask is applied and everything overlapped by this mask will turn into a resistor as copper is etched away exposing the thin-film material beneath. If this mask overlaps a trace, the trace becomes a resistor and the circuit will fail. Likewise, if

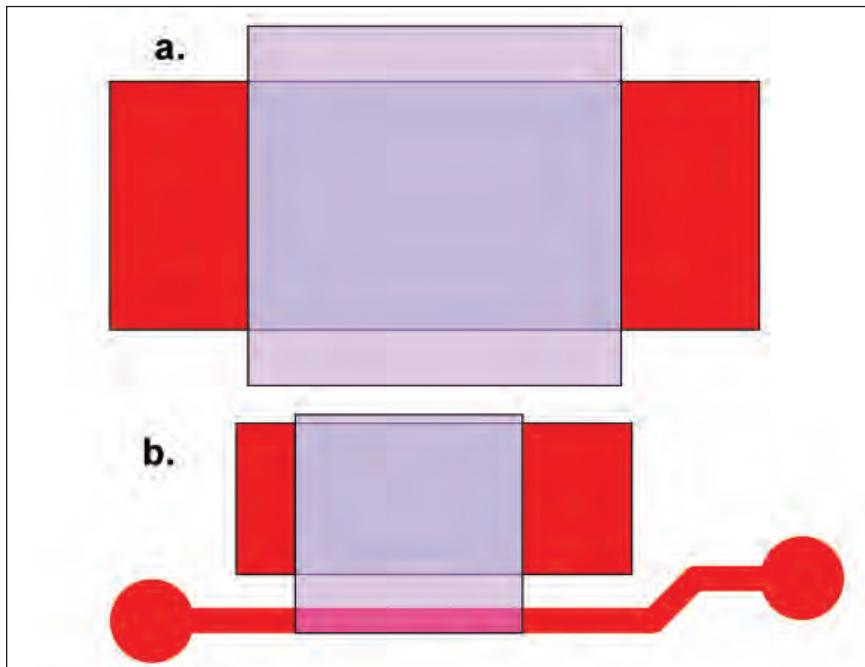


FIGURE 14: The actual component mask must be overized in the counter-direction to the trace (a), but not so much that it shorts to adjacent tracks or objects (b).

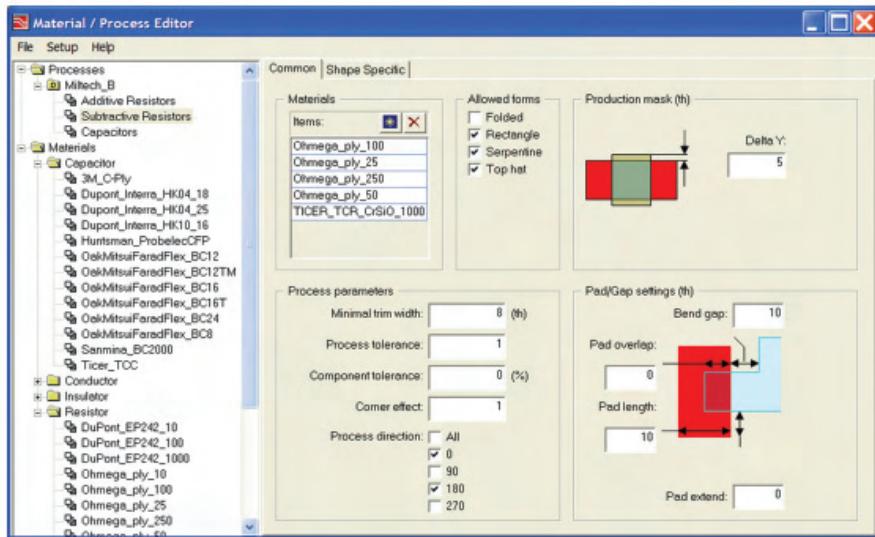


FIGURE 15: An EDA Tool's "Material and Process Editor" menu to capture the process manufacturing details for a subtractive resistor process[11]

the mask shifts in manufacturing so that part of the resistor body is not overlapped, a sliver of copper will remain making the resistor zero-ohm. Because the shift can vary slightly from panel to panel, you risk getting some boards testing OK where the margin is virtually zero, which can lead to long term reliability issues.

The mask must be over-sized by an amount equal to the worst possible manufacturing shift. The design rules in layout need to be set to check mask to other design objects with an amount equal to half the over-size to prevent the mask from overlapping neighboring design objects.

As seen in Figure 14a, the mask is only over-sized sideways. As the mask shifts left-to-right, it will eat up part of one of the pads but give back an equal amount to the other pad, keeping the resistance unchanged.

Figure 14b shows a shifted mask and how it has overlapped a routed trace causing a failure.

Manage the Manufacturing Process Data

Since the manufacturing parameters have a profound impact on the dimensions of a resistor to be generated, we must carefully capture, verify, and manage these data. In an EA Tool, this is done in the “Material and Process Editor” (Figure 15). Typically this is a database where multiple manufacturing processes can be set up and managed.

Manage Material Parameters

Having the process parameters under control, the next step is to collect data for the embedded passive materials you are considering. There are many different materials available and what is right for one design can be a bad fit for another. Consequently, you need multiple materials so we can investigate which materials and which processes will give the best results for a particular design. Manufacturers typically don’t have experience with all materials, so this can become a selection criterion for manufacturer.

In some EDA Tools, the material parameters are managed in the “Material and Process Editor.” The parameters differ between thin-film and thick-film processes. For example, for thin-film, the ohm/square of the material is static regardless of resistor size. For thick-film materials, several parameters together impact the ohm/square as a variable that is a function of resistor width and length. This means that for a 100-ohm thin-film material, you typically simply enter 100 as the resistance value while for thick-film, you need a matrix of resistance values for different lengths and widths of the finished resistor. The resistor synthesis tool needs to interpolate this in the resistance table.

Another critical parameter is power handling. A typically sized EP can handle around 100 mW. This is not accurate

enough for design. We need data from the material supplier on power handling which needs to be taken into account in the resistor synthesis. Thick-film resistors typically have a fixed mW/mm² or mW/mil². Thin-film materials are more complex. The manufacturers have conducted extensive tests and plotted power handling curves. As a designer you can use these curves to determine a specific mW/mm² for a given size resistor. As a service to the designer, the material suppliers typically publish curve fitting equations (such as the equation below) to allow you to calculate the power handling of a resistor.

$$P=45.9*((L*W)^{-0.87})/1000 \text{ [mW/mil}^2\text{]}$$

(where: P= power handling, L= length, W= width)

Once the manufacturing and material parameters are entered and validated, these data rarely change significantly, so the place to store these data is in a library.

Planning and *What if?*

With all parameters set up, the next step is to run some planning calculations on the design. The design doesn't have to be 100 percent complete. The minimum requirement is to have all the resistors and their properties, such as nominal value, tolerance, and power rating.

Knowing these properties, we can, for example, filter out all resistors with a tolerance we can't achieve (in case we want to avoid trimming). For each available material, we can also calculate the hypothetical dimensions of a resistor of each value and compare these dimensions to what we think is reasonable. For example, you probably don't want a 10-mil wide resistor 10 inches long or a 1-inch wide resistor

Embedded Components

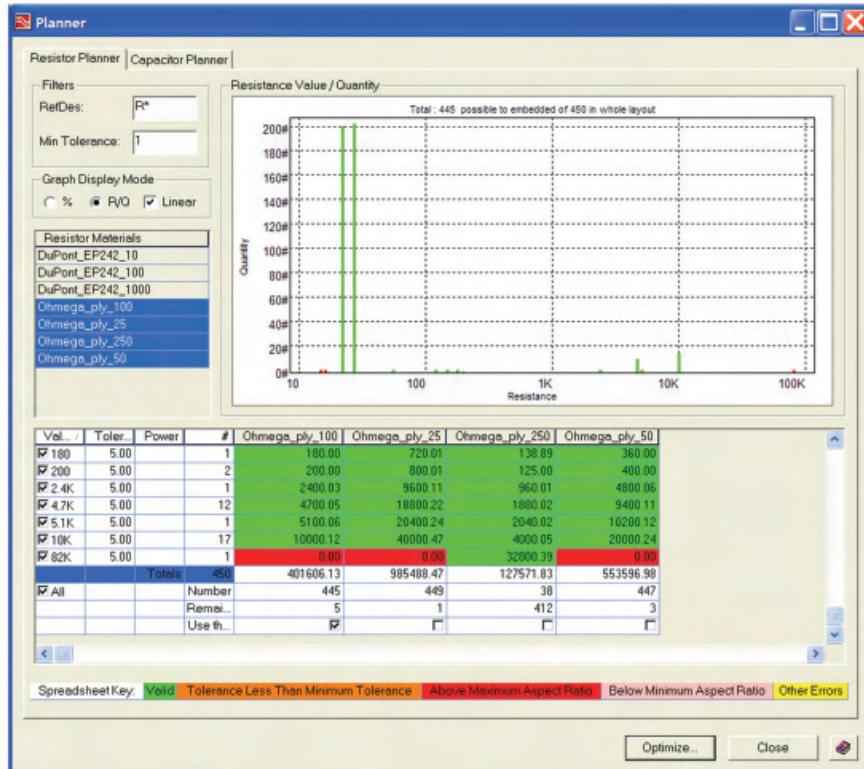


FIGURE 16: An EDA Tool's EP Planning menu to select components suited for embedding and EP materials to accomplish that task, along with resulting size[11]

10 mils long. The ratio between length and width is called the aspect ratio. 10 mils wide and 10 inches long is an aspect ratio of $10,000/10 = 1,000$. 1 inch wide and 10 mils long is an aspect ratio of $10/1,000 = 0.01$. For rectangular resistors, typical acceptable aspect ratios are between 0.2 and 15.

Based on whether a resistor falls within or outside of the acceptable aspect ratio, we can flag it as good or bad for each material. We can also calculate the actual resistor size so we can sum up the total component area. With these parameters, we can see which components can be embedded, which material(s) give the best result, and the total board area these embedded parts will occupy.

In some EDA Tools, this is done automatically in the “Embedded Passive Planner.” Figure 16 shows a typical analysis scenario for this design. Using the Ohmega Ply 100 ohm/sq material will allow you to embed 445 resistors leaving five as surface mount devices. Total part area is 401,606 mil² ~0.4in². We can also see that if we had picked the 25 ohm per sq material, we could have embedded four more resistors but at the cost of more than twice the component area (905,400 mil² versus 40,606 mil²). The outcome of the analysis is a selection of resistors to embed and a selection of the material(s) we will use. These data will be used in the next step of the design flow.

Resistor Synthesis

With the embeddable resistors selected and the right material(s) chosen, the synthesis tool can automatically generate the components. This was traditionally a manual and seriously error prone process. The synthesis can generate resistors in different forms (in order top to bottom in Figure 17):

- **Rectangle – most common**
- **Top-hat – has extended trimmable range**
- **Serpentine – to create high ohm resistors with low ohm materials**
- **Folded – to create low ohm resistors with high ohm materials**
- **Plug – to bridge layers**
- **Annular – donut around the via**

For the resistor, for each material, and for each selected form, the synthesizer calculates one alternative. For four materials and four forms, that is 4x4=16 versions of each

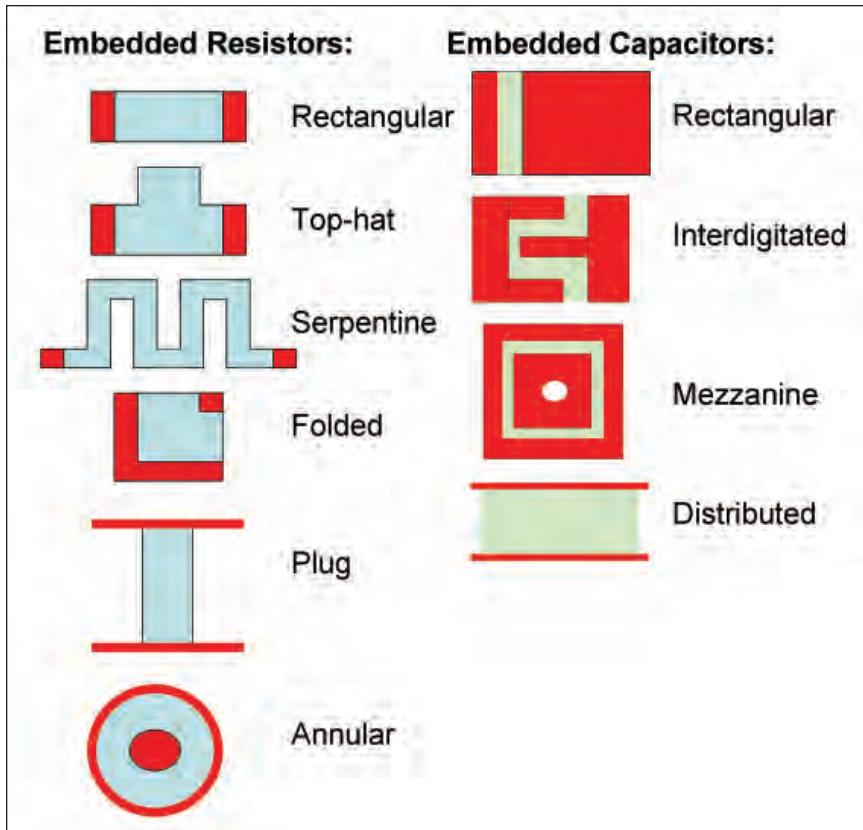


FIGURE 17: Six types of embedded resistors that can be designed for EP along with four types of embedded capacitors

resistor. They are all technically correct, as the synthesis keeps track of all rules and limitations, meaning:

- they all have the correct nominal resistance;
- they all are large enough to handle the power;
- they all follow the manufacturing parameters;
- they are all large enough to meet tolerance requirements.

However, depending upon the application, one is typically a better fit than the others. For example, size is always a concern and the number of materials is another. We can let the optimizer function of the synthesis tool optimize the

design by selecting the variants that will give the smallest total component area and the fewest required embedded passive materials.

Place and Route

From this point on, the EP is a component as any other. It needs to be placed and routed. However, as we place EPs in inner-layers, the tactics for placement are different. We need to place them so they don't block vias and routing. The design rule system needs to monitor all resistor pieces relative to other design objects during both place and route to ensure correct design.

Manufacturing Data

There are additional manufacturing data requirements when dealing with EP. We need artwork for each step in the manufacturing process. The artwork may be different for thin-film and thick-film. For thin-film subtractive process for each EP layer, we need:

- one film of all traces, vias, pins, and the resistor bodies;
- one separate film of the resistor definition mask.

For thick-film we need:

- one film of all traces vias and pins;
- one film of all EP resistor pins, each of which needs plating to accept the resistive ink;
- one film of EP resistor bodies, separate for each ink;
- one film of EP resistor overglaze mask, if used.

Today, many companies use ODB++ data for board manufacturing. However, ODB++ does not support the concepts of embedded resistors. It assumes that all

Embedded Components

components are either on the top or bottom layer. This causes assembly violations in the CAM check stations to a point where real errors could be obscured. The combined resistor bodies and traces, vias, and pin layer will act as a short circuit making a net check of the manufacturing data impossible. Still, ODB++ can be used to generate the artwork as long as these limitations are considered. Because of these issues, many still use Extended Gerber (RS-274-X) data format for embedded passive artwork.

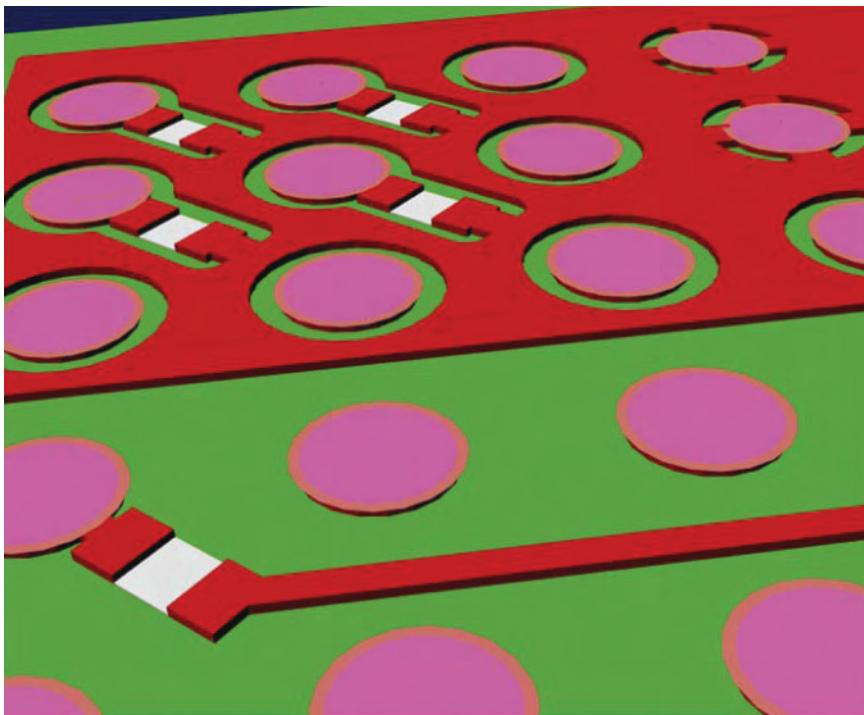
Test

When we receive a standard printed circuit board from a manufacturer, we expect it to be correct and we expect the board manufacturer to verify that the boards are good. When we use EP technology, we not only expect the board to be good but now we have transferred the responsibility for hundreds or thousands of resistors to the board manufacturer. They must all be within specified limits. To give the board manufacturer a fair chance to trim and test the boards, we need to deliver sufficient test data. Consider that the board panels, before lamination, will be tested and possibly trimmed. We need a data format where the resistor pads or other probe locations are included, as well as all resistor properties, such as nominal value, tolerance, power rating, and trimmable range.

Today, the typical format of choice is the IPC-D-356-A or IPC-D-356-B. These are extensions of the classic IPC-D-356 format but now with the extension of supporting parts on any layer and with all component properties included. Finally, as mentioned in the introduction, co-designing the probe card with the EP board is desirable to ensure testability and trimmability.

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Advanced HDI Structures and Next Generation Technologies

By Happy Holden — *Mentor Graphics*

Advanced HDI Fabrication Processes

The four basic and original HDI processes are laser drilled laminate (FinstrateTM) and flexible materials (MicrowiringTM), photodielectrics with SLCTM [1,2], and plasma-etching polyimide (DycostrateTM). These and the other 18 HDI processes have been integrated into standard printed circuit manufacturing flows. There is no standard way to organize these processes, but the method of Interconnect Via Hole (IVH) formulation is the most unique characteristic of each process and will be used for this purpose.

The purpose of this chapter is to examine a variety of advanced HDI fabrication processes that have evolved over time. IVH formation is just one element of fabricating HDI wiring boards and although the laser drilling method is the most popular, a number of other methods for defining IVH have taken root. Two important factors are the various dielectric materials available and the methods of metallization. Fabrication of HDI wiring boards with microvia holes involves many new processes not common to conventional board fabrication. Therefore, additional emphasis will be placed upon these new fabrication processes that are common to other microvia technologies.

Definitions of HDI Process Factors

Figure 1 shows that the HDI technologies in use today are made up of four factors: via stack-up, dielectric materials, methods of IVH formation, and methods of metallization of z-axis via connections. In recent years, 14 different advanced HDI processes have been used.

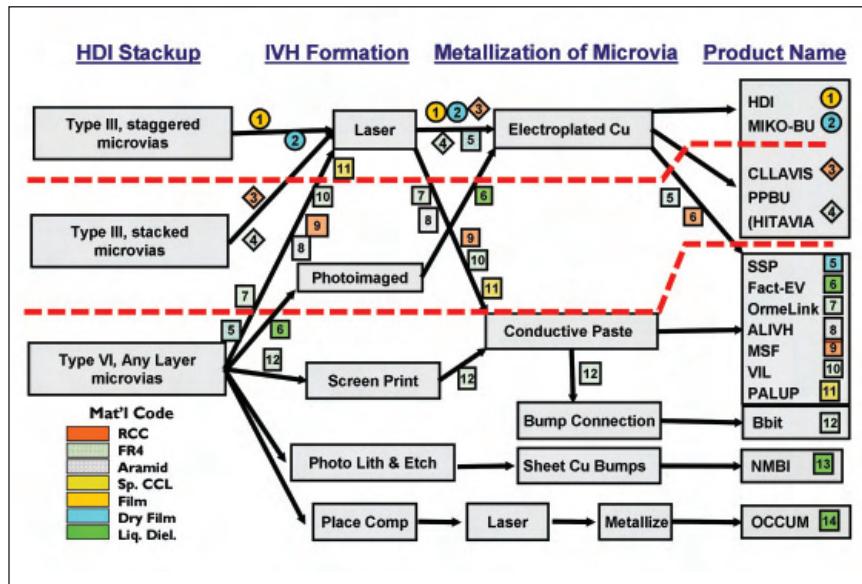


FIGURE 1: The HDI technologies in use today are made up of four important factors: microvia stack-up architecture, dielectric materials, methods of IVH formation, and methods of metallization of z-axis via connections. In recent years, 14 different HDI processes have been developed.

HDI Type III Using Staggered Microvias

As seen in Figure 1, most advanced HDI processes utilize a laser drill via generation technique. This process was first used by IBM in the late 1970s to drill small holes in G-10 laminate for buried vias in mainframe computer boards for its 370 computer. There are two advanced HDI processes using a Type III staggered via structure: High-Density Interconnect and Meiko-BU.

High-Density Interconnect (HDI)

The HDI process developed by General Electric is the one that is most similar to integrated circuit (IC) processes. This process is what is called *chips-first*, as the assembly is done before the substrate is completed and the IC bonding is direct to the substrate. It does not use flip-chip or wire bonding, but can utilize unmodified chips directly. A number of buildup layers and very fine geometries are possible. There are obvious advantages to making multichip modules and using standard chips. The materials and bonding technologies have proven to be very reliable and suitable for military applications. The disadvantage is that the maximum panel size if sputtering is used instead of common electroless metallization. Future use of Physical Vapor Deposition (PVD)/Chemical Vapor Deposition (CVD) metallization may make this process more cost-effective.

Structure

The circuit structure of HDI consists of common conventional flex circuits or more advanced microvia flex structures that are purchased for this process. The polyimide film usually has 25 or 50 microns of adhesive. The laser ablates away the polyimide to produce blind and through-vias. The through-vias are stopped by the aluminum bonding pads of the integrated circuits. By doing this, integrated circuits designed for

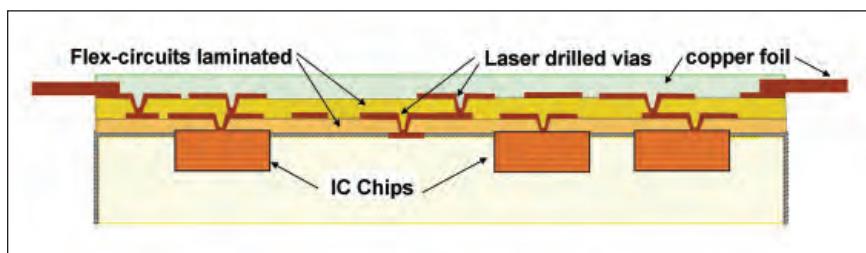


FIGURE 2: Structure for HDI multilayer substrate with laser blind vias and direct connection to ICs

wire bonding can be directly attached. Figure 2 shows a typical HDI structure.

Manufacturing Process

The process starts with a finished single-sided, double-sided, or multilayer polyimide flex circuit. An adhesive is applied to the flex circuit. All the ICs and components are bonded to the polyimide film layer-pair flex circuitry and cured. The assembly is turned over and a laser drills down through the flex circuitry to make blind and through-vias while opening up the bonding pads on the IC chip. Gold, under-bump metallurgy, or C4 bumps are not required. The panel goes through tungsten sputtering to metallize the vias and seed the top layer. The circuit pattern can be applied, plated, and then etched to complete the circuit.[3,4] The process is diagrammed in Figure 3.

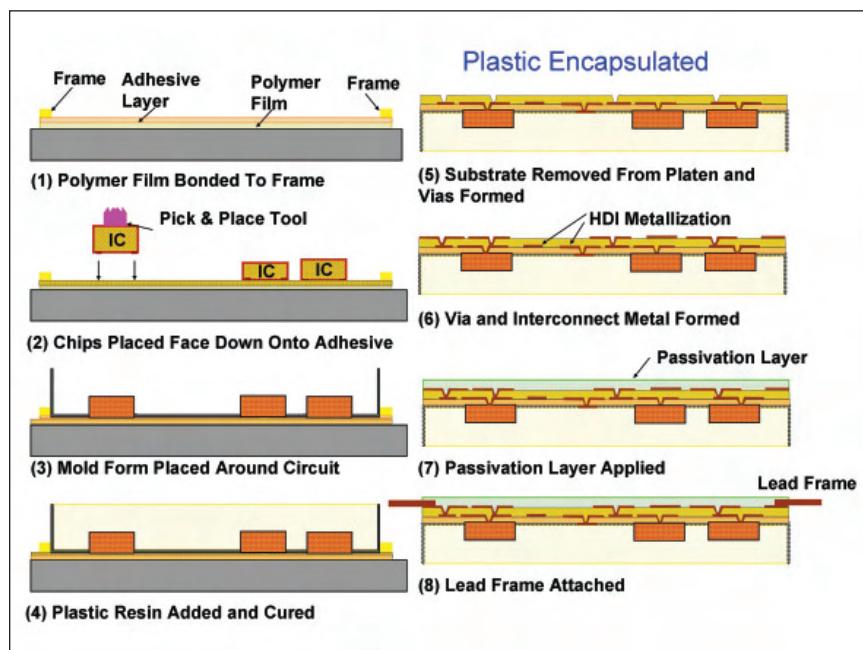


FIGURE 3: Manufacturing sequence for the HDI multilayer substrate with laser blind vias

Meiko-BU

Meiko Circuits of Japan takes a photoresist and coats it onto a stainless steel panel which starts the process of producing buildup structures in a remarkable way. One advantage of this process is that surface geometries are not determined by etching or full additive metallization. In addition, the vias are under the surface lands and the circuits are all flush with the dielectric, permitting the elimination of solder masks. On the negative side, this is a more expensive process that involves carriers.

Structure

Figure 4 shows the structure of Meiko's buildup circuits, which are called carrier-formed because a stainless steel carrier serves as the base for the photodielectric, even though they are laser drilled to form the vias. The resulting structure is similar to other HDIs. The core is still a rigid board and the buildup layers are special films or liquid resins.

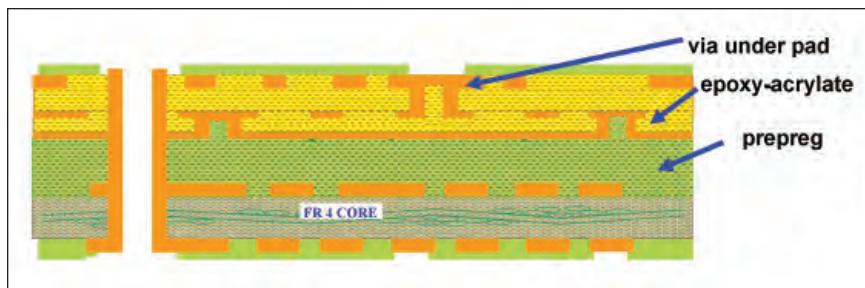


FIGURE 4: Carrier-formed circuit multilayer structure

Manufacturing Process

The manufacturing process (see Figure 5) starts by taking a photoresist and coating it onto a stainless steel panel. The surface pattern is exposed and developed in the photoresist. First gold, then nickel, and finally copper are plated on the panel.

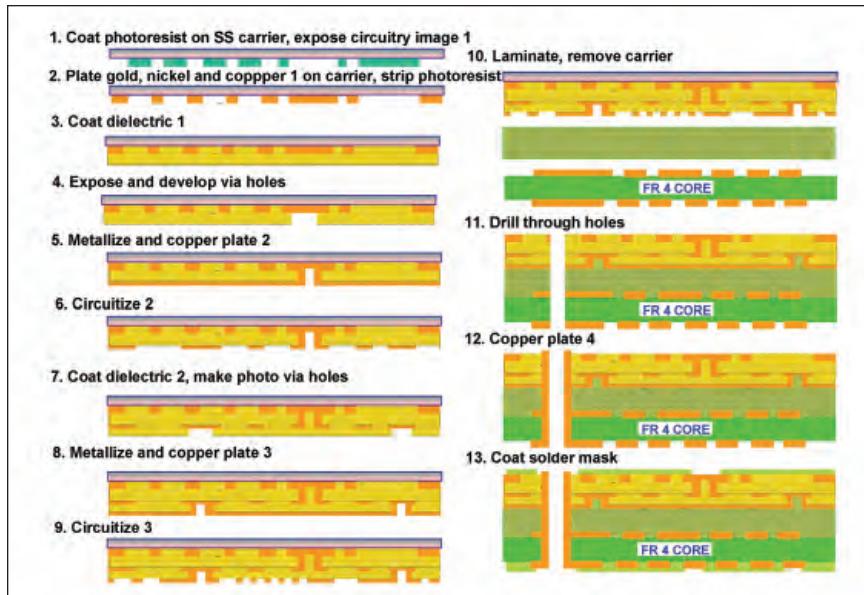


FIGURE 5: Fabrication process for carrier-formed circuit multilayer substrate

When the resist is stripped, the PID is applied over the entire panel and via holes are laser drilled in the dielectric. Once metallized and plated, photoresists can define the circuitry by etching. The process can be repeated until the circuitry is complete or can be laminated to FR-4 materials as rigidizers.[5,6]

HDI Type III Using Stacked Microvias

A further density evolution in advanced HDI is stacking of the IVHs. Most advanced HDI processes have stacked microvias, but the distinction here is that this is produced as an IPC Type III, sequential buildup processes. Three HDI structures use this process: CLLAVIS, PPBU, and HITAVIA.

CLLAVIS

The CLLAVIS buildup technology is marketed by CMK of Japan. The laser drilled microvia technology is the most common of HDI processes. The cross-sectional view in Figure 6

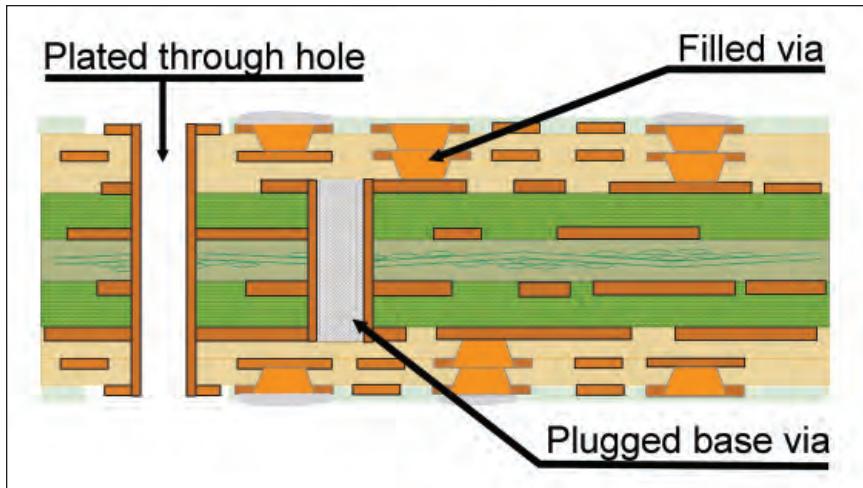


FIGURE 6: A typical high-density CLLAVIS

shows the filled, buried vias in the multilayer core, as well as the optional filled microvias that can be stacked. This structure is also available with the simpler, unfilled staggered microvias.

Manufacturing Process

The CLLAVIS manufacturing process is outlined in Figure 8 and is identical to most of the laser via-buildup technologies used.

Prepreg Buildup

The Prepreg Buildup (PPBU), from CMK, is a standard sequential lamination process using laser drilled vias similar to those in the CLLAVIS process. The diagrams in Figure 7 show two of the structures, a standard 2+4+2 buildup and an advanced 3+2+3 stacked buildup.

HITAVIA

The Hitachi HITAVIA technology (Hitachy Any-layer Via) is the only HDI process developed for use with conventional

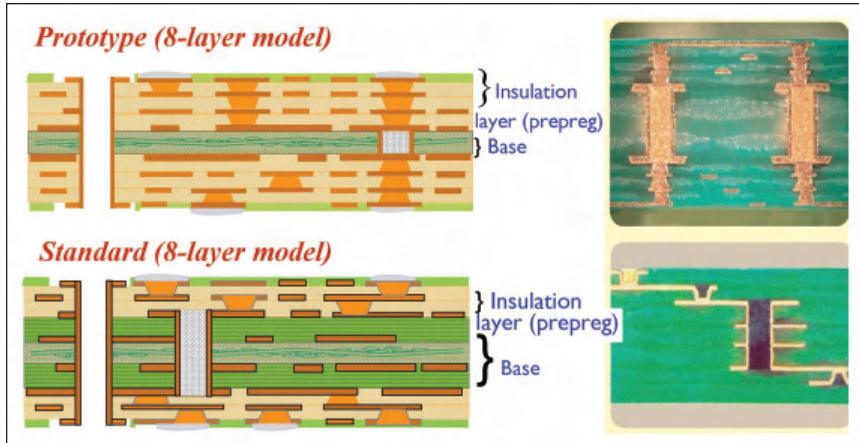


FIGURE 7: A typical high-density PPBU board

mechanical drilling as well as laser drilling. It utilizes RCC or prepreg materials that are mechanically drilled and sequentially laminated after the vias are filled with conventional electroless copper and copper plating. The typical manufacturing sequence for this HDI technology is similar to that of CLLAVIS and PPBU (Figure 8).[7]

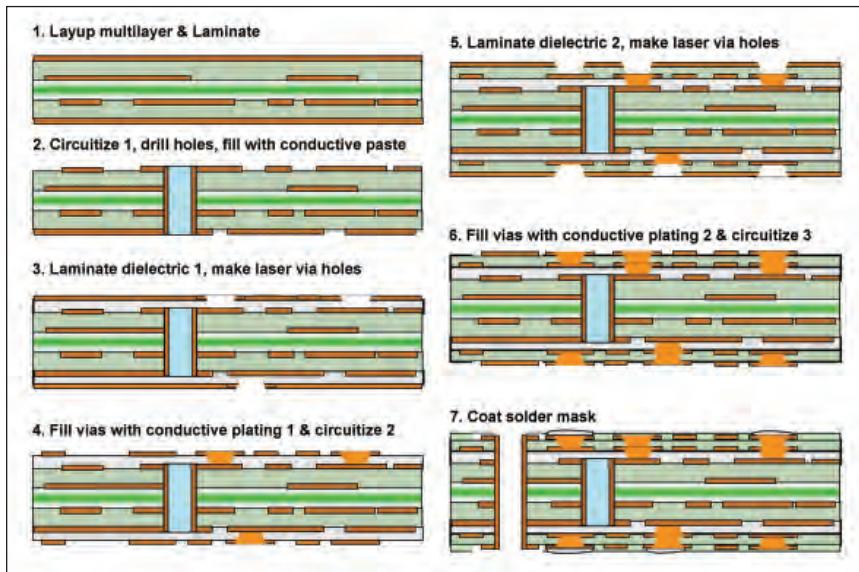


FIGURE 8: Typical manufacturing process for CLLAVIS, PPBU, and HITAVIA boards

HDI Type VI, Any-Layer Vias Using Stacked Microvias

The ultimate in HDI density is the IPC Type VI structure utilizing an *any-layer IVH* architecture. (For more discussion on this, see Chapter 3 - Design Of Advanced Printed Circuits.) Ten advanced HDI structures are of this type:[8,9,10,11]

- SSP
- OrmeLink
- MSF
- PALUP
- NMBI
- FACT-EV
- ALIVH
- VIL
- Bbi
- OCCAM

SSP

The SSP technology was developed by Ibiden of Japan. It used standard FR-4, copper plating and laser drilling and can be seen in Figure 9. SSP technology's additional step is the application of a thin adhesive to each finished, single-sided, bump-plated core. The process sequence is described below and illustrated in Figure 10:

- Start with single-sided, copper-clad laminate.
- Laser drill from the non-copper side.

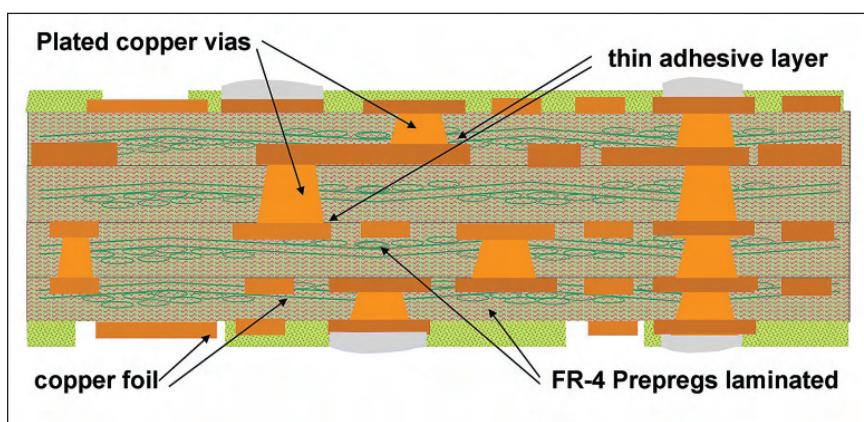


FIGURE 9: Typical SSP board

- Desmear laser holes and run through the electroless copper process.
- Plate up bumps on the clad side.
- Image and circuitize the copper side.
- Apply a thin adhesive to the unclad side.

Repeat these steps for the remaining cores of the multi-layer and then follow the remaining steps:

- Lay up the finished cores with copper foil.
- Vacuum laminate with finished layers.
- Image and circuitize the outer layers
- Coat the solder mask and finish.

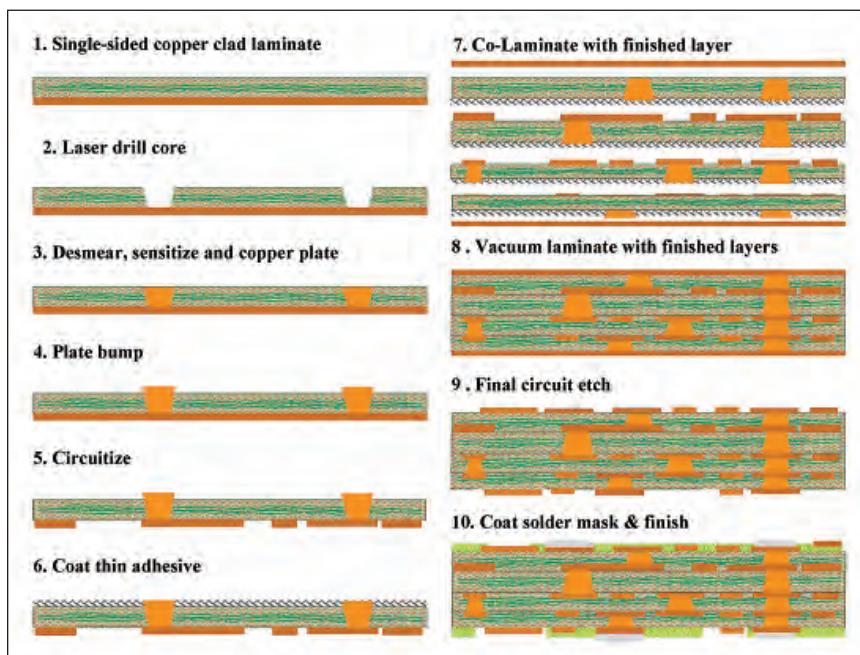


FIGURE 10: Typical manufacturing process for SSP boards

FACT-EV

Fuji Kiko Advanced Chemical Technology-Etched Via Post (FACT-EV) is from Fuji Kiko of Japan. As with the SSP process,

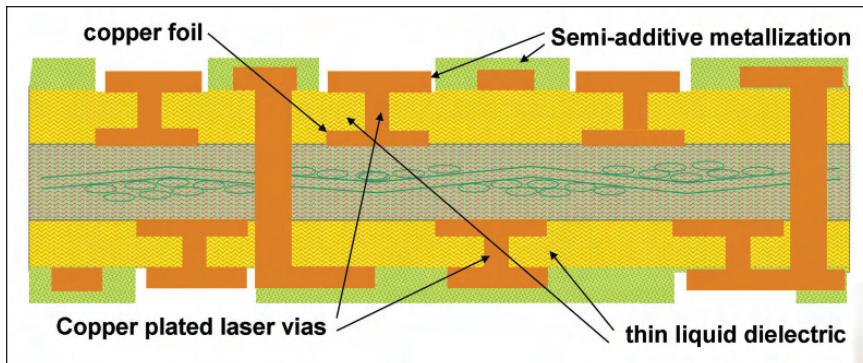


FIGURE 11: Typical FACT-EV board

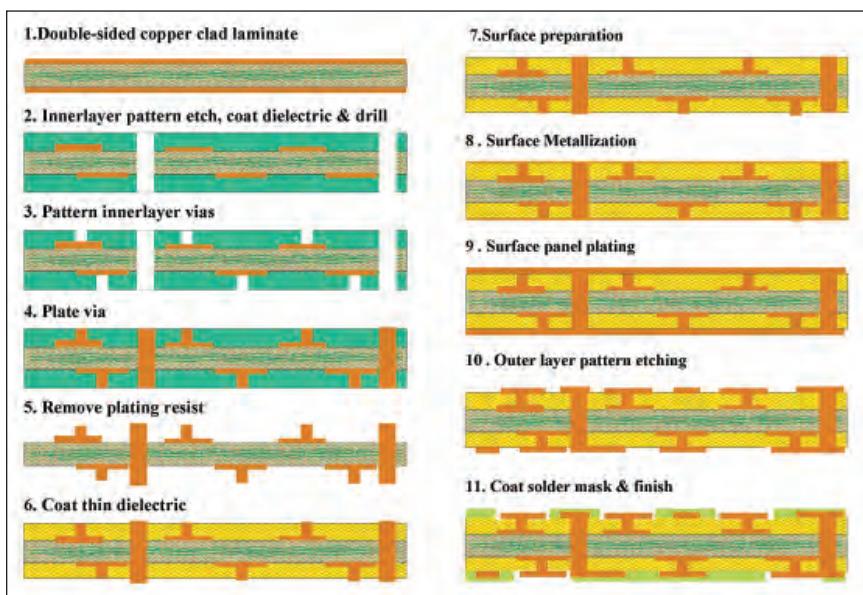


FIGURE 12: Typical FACT-EV manufacturing process (Courtesy of Ormet Technology)

the via is a solid-plated copper post (Figure 11). In this case, the process uses standard dry-film photoresist to define the posts and a thin-liquid dielectric to coat the plated posts. Unlike SSP, however, the process is sequential and each two sets of layers are processed on the prior layers (Figure 12).

Solid Conductive Via Fill

The next group of HDI technologies all utilize metallic copper pastes or a solid sheet of metal to form the via connections. Table 1 presents alternatives to copper plating for forming IVH connections.

TABLE 1: Alternative HDI Technologies utilizing filled, solid IVH

Fabricator	Trade Name	IVH Process	Metalлизation
Dyconex	DYCOre	Copper etching	Etched copper bumps
Ormet	OrmeLink	Laser, plasma, or photodielectric	Cu/Sn organo-metallic
Matsushita Electronics	ALIVH	Laser	Copper particles in epoxy
Toshiba	Bbit	Insulation displacement	Silver/epoxy paste
Parelec	PARMOD	Drill, laser, or photodielectric	Metallo-organic decomposition, Cu or Ag
Namics	Unimec	Punch, drill	Silver, palladium, and copper particle pastes
North Corp.	NMBI NMTI (Neo-Manhattan)	Image and etch	Etched copper bump
Denso	PALUP	Laser	Cu organo-metallic
Shinko	MSF	Laser	Conductive paste
Victor	VIL	Laser	Silver/epoxy paste

OrmeLink

CTS' co-lamination process and Ormet's transient liquid phase sintering (TLPS) process, OrmeLink, are similar to ALIVH's conductive copper paste process in that they are via pastes of copper-tin organometallic matrix that sinter into a solid metallurgical via. CTS' process is called ViaPly. Past users, in addition to Sheldahl, include Litronics, now called

Allied-Signal Substrates, in Costa Mesa, California. Up to four layer-pairs have been connected (eight metal layers) using OrmeLink.

Structure

The Ormet structure is made up of polyimide or FR-4 layer-pairs. Different materials can be mixed if a rigid core or heat spreader is required. The conductive paste is a TLPS ink of copper-tin. The structure is shown in Figure 13. Figure 14 shows the cross sections of two finished circuits with laser-via polyimide layer-pairs, with TLPS solid metallurgical vias connecting the layer-pairs and FR-4 inner-layer cores with buried TLPS vias.

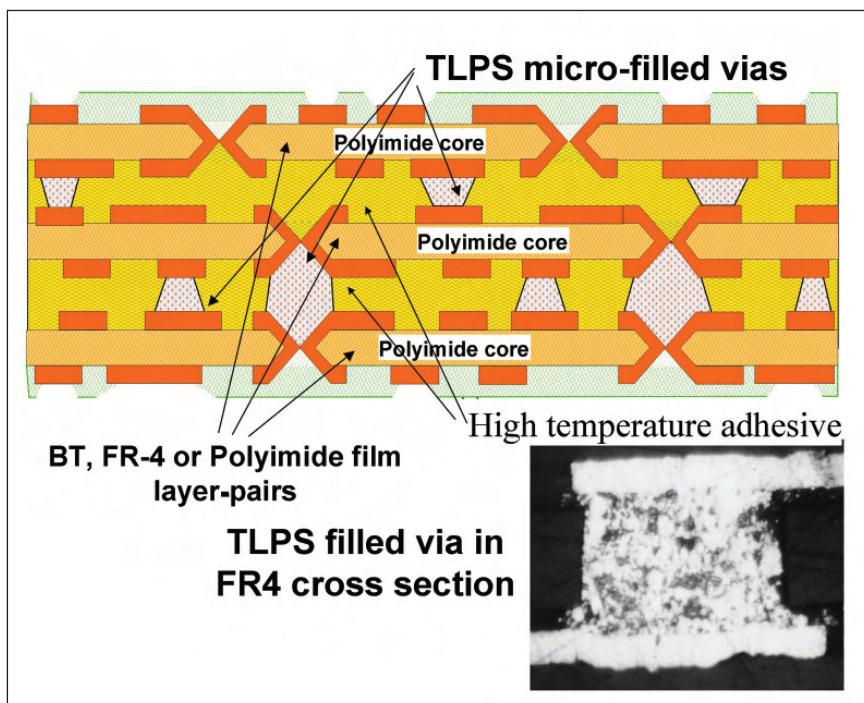


FIGURE 13: This illustrates the co-lamination (OrmeLink) multilayer structure with examples of TLPS cross sections of three layer-pairs with laser-vias filled with TLPS paste vias and buried vias for FR-4 inner-layers.

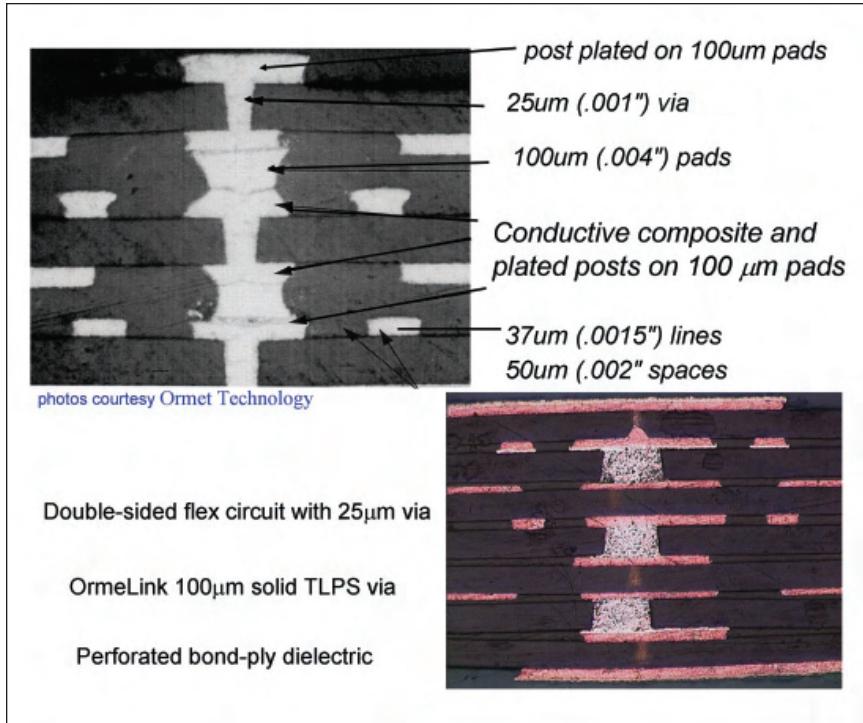


FIGURE 14: OrmeLink TLPS sintered conductive pastes used to connect layer-pairs in multilayer substrates

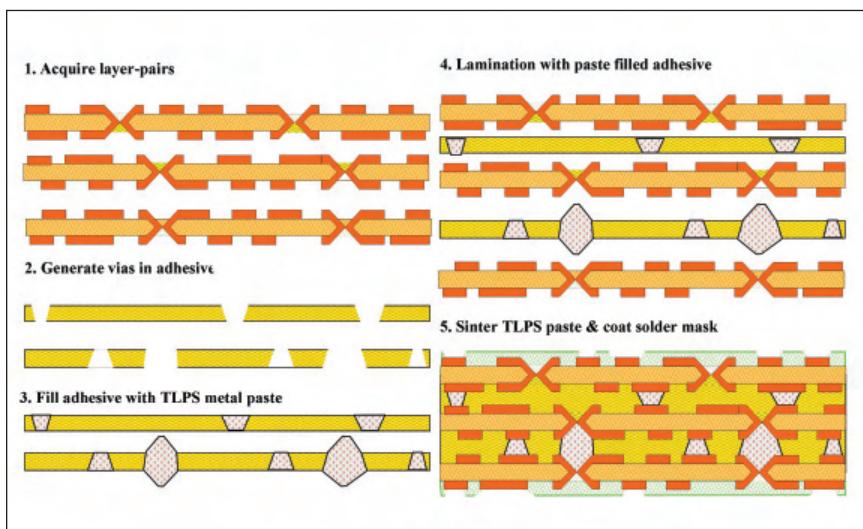


FIGURE 15: OrmeLink multilayer substrate fabrication process

Manufacturing Process

The manufacturing process is shown in Figure 15. The microvias are lasered or punched in the polyimide adhesive and then filled with the TLPS paste. The structure can now take layer-pairs from any other HDIS process (such as Sheldahl's) and turn them into a multilayer structure through sintering. The conductive pastes have to be sintered in a condensing vapor of fluorocarbon at 215° C for 2 minutes. The structure is then postured by baking for 40 minutes at 175° C. Table 2 details the process.

TABLE 2: Properties and Curing Processes for the Ormet Type of TLPS Conductive Pastes

Property	Curing Process
Ormet 2005 Series Ink	Specification and processing parameter
Electrical Conductivity	Bulk 4.0×10^{-3} Ohms-cm Sheet resistance 10.0×10^{-3} Ohms/sq in
Adhesion (Tensile Pull) on various materials	
FR-4 ($T_g = 125^\circ C$)	1,300 psi (minimum)
Copper	2,921 psi (average)
Printability	230 stainless steel wire mesh and emulsion Thickness of 7.5 μm Sintered thickness 28–38 μm 200 μm traces on 400 μm pitch
Cure Cycle	
	30 minute drying at 85° C 2 minute vapor cure at 215° C 40 minute post-cure at 175° C

ALIVH

The Any Layer Interstitial Via Hole (ALIVH) process has been in development for many years by Matsushita Components of Osaka, Japan. The novel process eliminates additive

metallization and plating, but defines features by subtractive etching of the copper foil. However, the buildup process is not sequential. It uses layer-pairs and aramid-epoxy prepreg with copper-paste vias that can be laminated at one time into a three-dimensional structure. Six to 14 layers have been laminated in this way. CMK (the fourth largest PCB maker in the world) and other Japanese firms have licensed the ALIVH process.[12,13]

Structure

Figure 16 shows the structure and cross sections for an ALIVH product. The PCB consists of laser produced blind vias. The core material is an epoxy-aramid laminate. The man-made aramid filaments are ideal to be cut with a CO₂ or UV laser. If DuPont Kevlar filaments are added, then the resulting material will have a very low coefficient of thermal expansion (CTE), which is useful for mounting ceramic packages and for direct attachment of flip-chip integrated circuits. The structure can be as simple as a two-sided PCB or as complex as a many-layered PCB. The vias consist of a copper-epoxy paste that con-

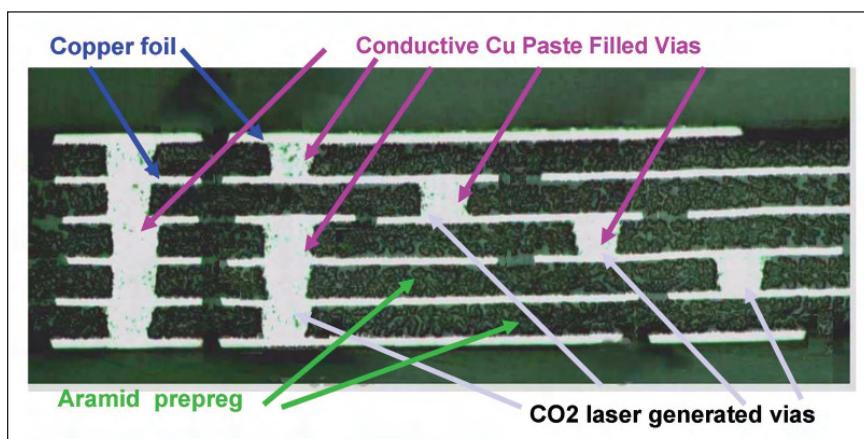


FIGURE 16: Parallel-bonded solid via structure of the ALIVH multilayer with cross sections of examples

ncts the top and bottom copper foil. If used as a prepreg layer without copper, the vias connect the various ALIVH layer-pairs into a multilayer structure. This is not a sequential buildup process, but rather a parallel buildup process.

Manufacturing Process

The ALIVH process is shown in Figure 17. The process starts with an epoxy-aramid B-stage prepreg. The laser cutting of holes can proceed very rapidly. The material is then printed with a conductive paste of copper and epoxy to fill these holes. Copper foil is applied and the structure is laminated to attach the foil and cure the prepreg and conductive pastes that serve as vias. The sheet of material is imaged and etched to provide the various circuits. Registration is less critical because the vias are now under the surface lands. Several of these two-sided layer-pairs can be produced, inspected, and tested. The two-sided

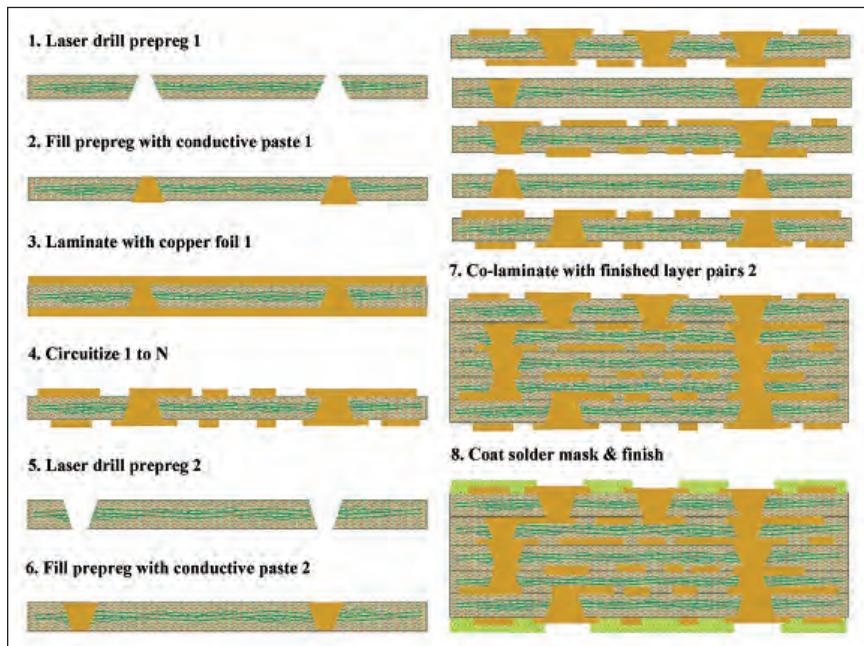


FIGURE 17: ALIVH manufacturing sequence for a multilayer substrate

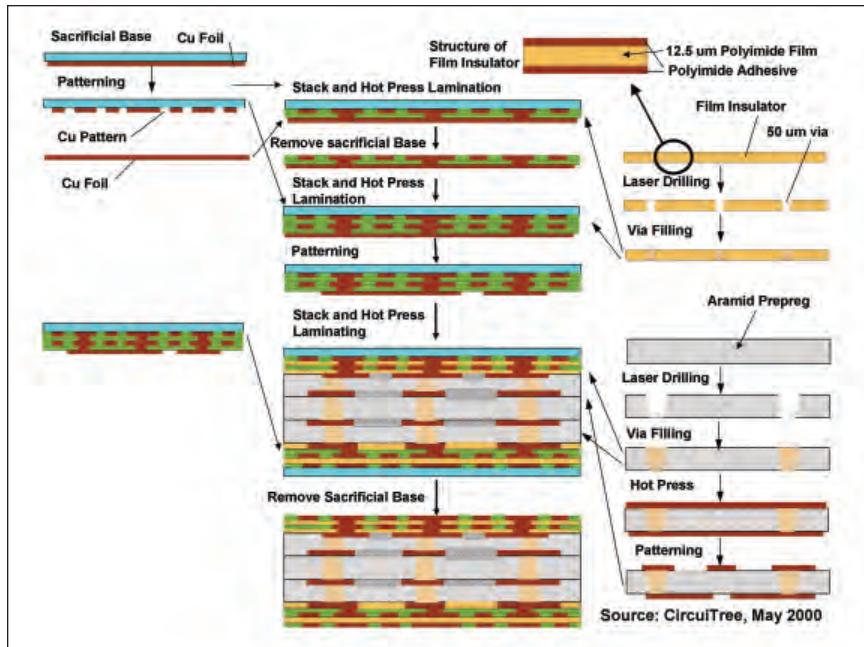


FIGURE 18: ALIVH-FB manufacturing process for a multilayer substrate (Illustration courtesy of CircuiTree)

structures can then have additional single layers of B-stage/conductive paste layers with foil laminated to one or both sides, or the B-stage/conductive paste layers can be used to attach a number of layer-pairs in one parallel lamination. The outside is imaged, etched, and completed as a normal PCB.

An advanced manufacturing process results in a product known as ALIVH-FB which has a fine-line, tight via structure suitable for wire-bonding and flip-chip substrates, as shown in Figure 18. The manufacturing process for each microvia technology begins with a base core, which may be a simple double-sided board carrying power and ground planes or a multilayer board carrying some signal pattern in addition to power and ground planes. The core usually has PTHs, which become BVHs, and is often called an active core.

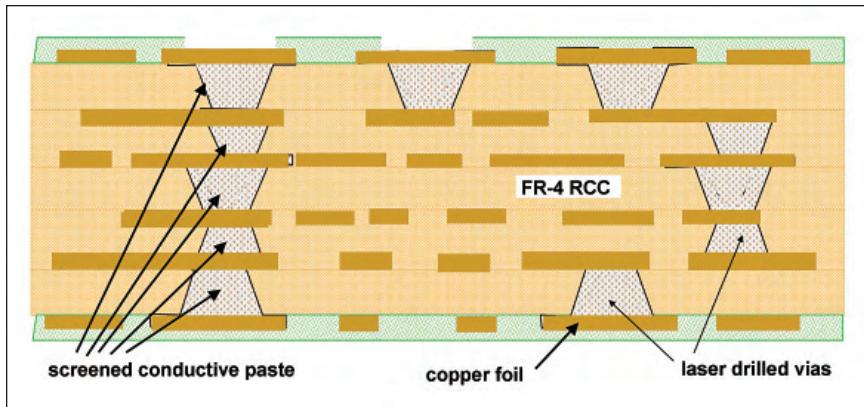


FIGURE 19: MSF multilayer substrate structure[14]

In fabricating a base core with a pattern, manufacturers usually panel-plate the core panel and create the pattern through a dry-film tenting process. Some makers seem to prefer pattern plating. The choice depends on the fabricator's familiarity with these processes. After the pattern is formed, dielectric material is laminated over the core (in the case of prepreg, with copper foil) and the holes can be filled with resins, depending on the plated hole diameter and the thickness of the core. It is generally agreed upon that when the diameter of plated holes is equal to or less than 0.3 mm and the core thickness is equal to or less than 0.6 mm, the holes can be filled effectively by the lamination process (although the resin thickness of 80 μm is preferred in the case of RCC).

When the diameter and thickness conditions are not met, it is necessary to fill the holes using a separate process. A screening process does this from one side of the panel with a polyester screen that has an oversized hole pattern. After filling the holes and curing the resin completely, it is important that the resin be flush with the surface on the core.

MSF

Shinko of Japan developed the MSF HDI technology. It utilizes laser drilled RCC materials and vias filled with a conductive paste. After testing, these are laminated into the parallel buildup structure. Figure 19 shows the typical stack-up for the MSF HDI technology.[15]

Victor Interconnected Layers

The Victor Interconnected Layers (VIL) HDI technology was developed by Victor of Japan. It utilizes FR-4 prepreg materials that are laser drilled and sequentially laminated after the vias are filled with a conductive paste. Figure 20 shows the typical structure for the VIL technology.[16]

Manufacturing Process

The MSF and VIL have similar manufacturing sequences for a multilayer substrate.

Patterned Prepreg Layup Process

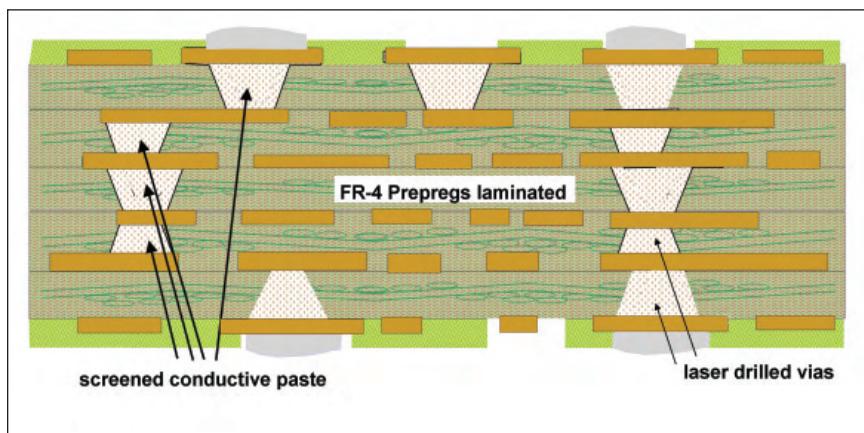


FIGURE 20: VIL multilayer substrate structure

Patterned Prepreg Layup Process (PALAP) is a process that was developed by a consortium comprised of the Japanese firms Denso, Wako Corporation, Airex, Kyosha, Noda Screen,

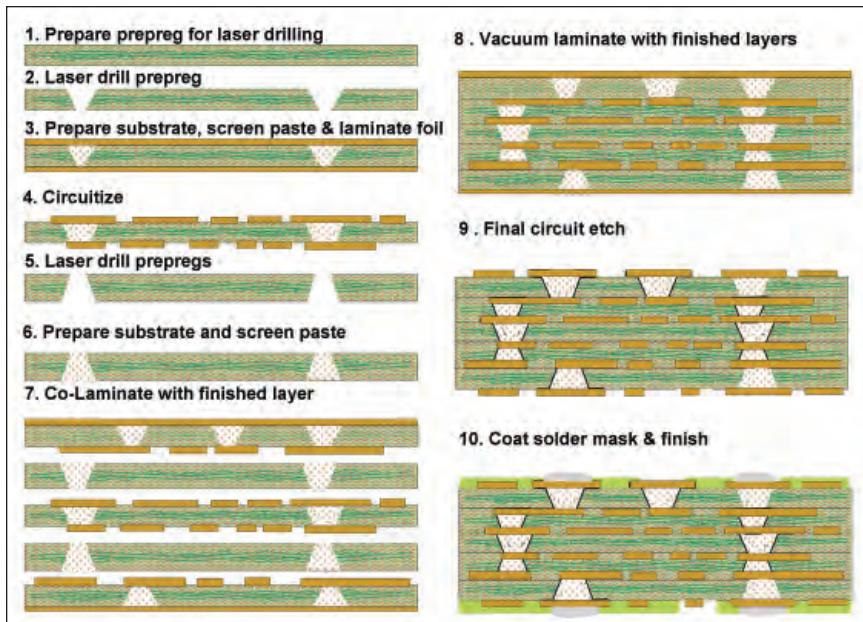


FIGURE 21: MSF and VIL manufacturing sequences for a multilayer substrate

and O.K. Print. Originally, the process started with copper-clad laminates (CCL), but now it utilizes thermoplastics like poly-ether-ether ketone (PEEK) resins or a new plastic called PAL-CLAD. PAL-CLAD is characterized by the electrical properties and heat resistance of BIAC, a recyclable thermoplastic resin film produced by Japan Gore-Tex, Inc (See Figure 22).[17]

Manufacturing Process

The single-lamination process compares favorably to conventional PCB processing, where lamination, curing, and wiring patterns are repeated layer after layer. PALUP boards can be multilayered by pressing together all thermoplastic resin layers, each having wiring patterns, as shown in Figure 23. This significantly improves quality, lowers costs, and shortens delivery times. PALAP boards also offer high interconnecting reliability by adopting metallic paste for filling vias, and have

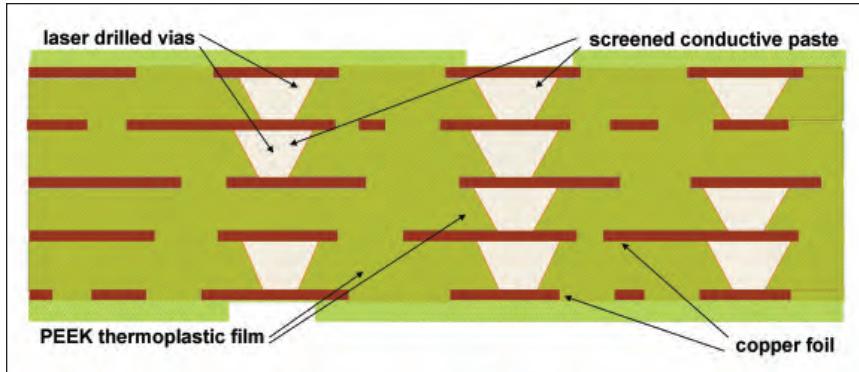


FIGURE 22: PALAP multilayer substrate structure

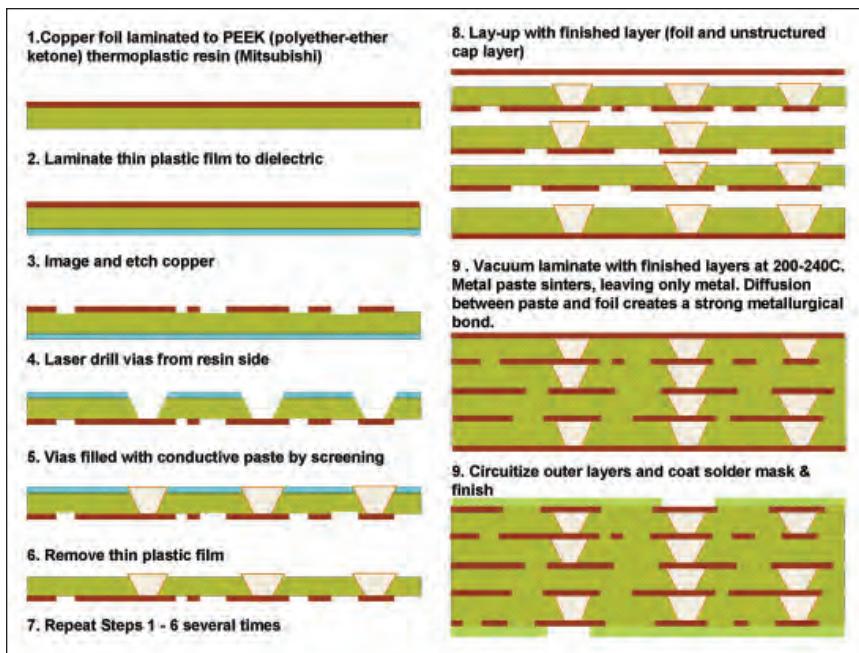


FIGURE 23: PALAP manufacturing sequence for a multilayer substrate

excellent high-frequency properties due to a low dielectric constant.

PALAP boards are fabricated giving due consideration to the environment. *Environmental correctness* is one of the major issues requiring action in the area of electronics products,

including those used in information technology and automobiles. Because PALAP boards use thermoplastic resin as their base material, they enable material recycling in which only the resin is separated and reused.

Buried Bump Interconnect Technology

Toshiba has developed a new process referred to as Buried Bump Interconnection Technology (Bbit). Bbit employs a conductive paste to replace via drilling, additive metallization, and via plating. The process has the advantage that hole-producing equipment is not required. Instead, a screened silver-epoxy paste is cured to be pointed, like a thumbtack. The paste displaces the glass and epoxy during lamination to connect to the copper on the opposite side of the prepreg. The mass via-generation techniques, the simplification of metallization, and the fact that no drilling equipment is required, make Bbit potentially very inexpensive. Currently, the design rules and features are for consumer products, but future uses include simple plastic ball grid arrays (PBGAs).[18,19]

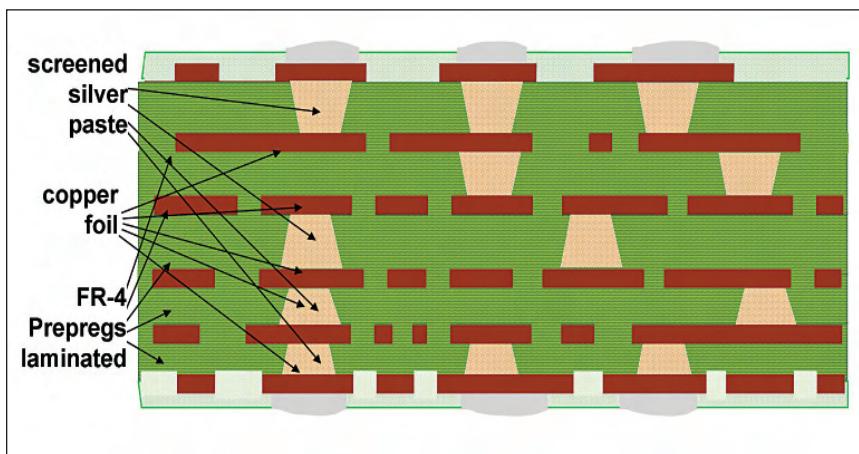


FIGURE 24: Structure of the Bbit substrate

Structure

The Bbit structure appears similar to the structure of other PCBs employing conductive paste vias. As shown in Figure 24, the Bbit structure is similar to ALIVH. The difference is that the Bbit structure uses standard FR-4 materials and a novel way to produce a via.

Manufacturing Process

A silver ink is screened on copper foil in the locations where vias are required. Copper is used in the manufacture of standard FR-4 laminate. The silver paste thumbtack-like obstruction forces itself through the glass cloth during lamination to connect itself to the copper foil on the other side of the laminate and to cure the prepreg. The sheet of material is imaged and etched to provide the various circuits. Registration is less critical because the vias are now under the surface lands.

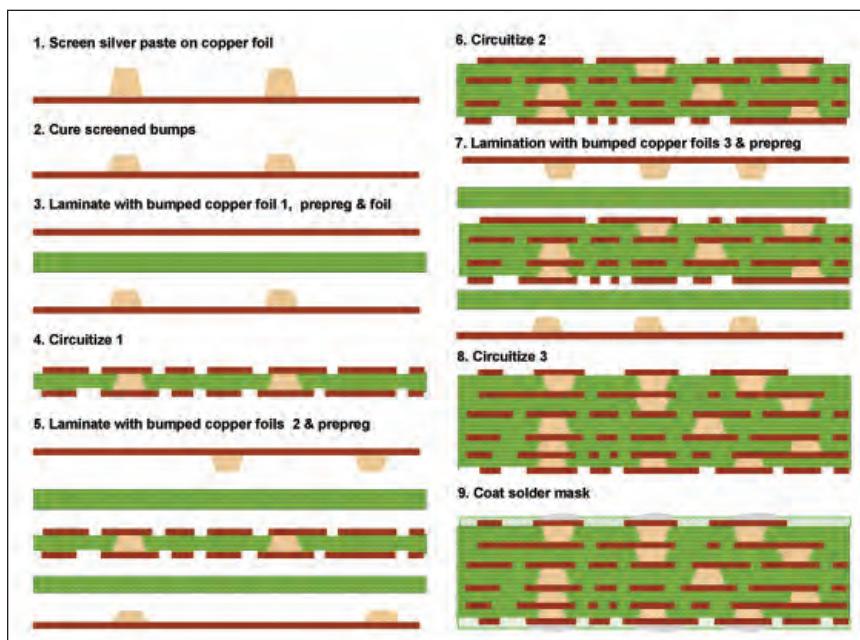


FIGURE 25: Manufacturing process for Bbit boards

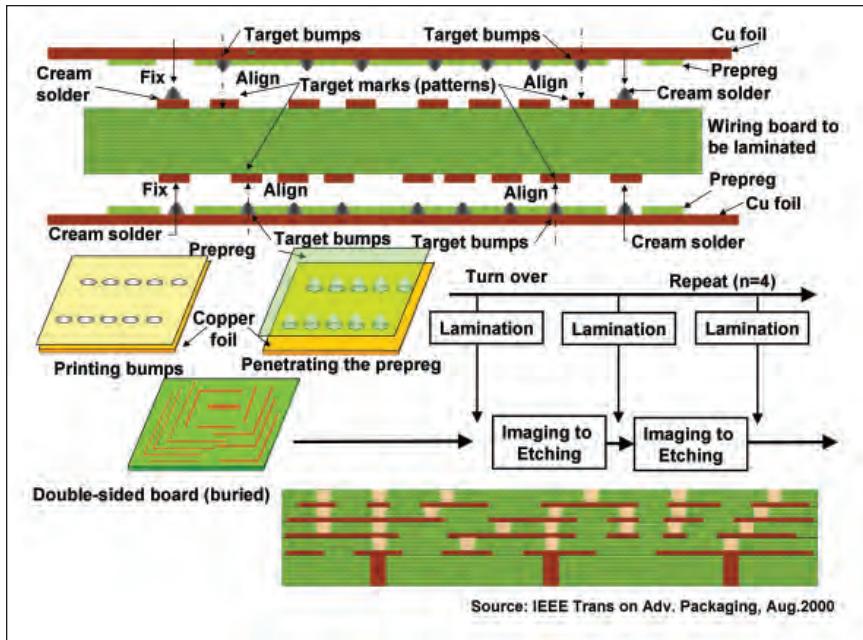


FIGURE 26: Manufacturing process for fine-pitch Bbit substrates

Several of these two-sided layer-pairs can be produced, inspected, and tested. The two-sided structures can then have additional single layers of B-stage/conductive paste layers with foil laminated to one or both sides. Alternatively, B-stage/conductive paste layers can be used to attach a number of layer-pairs in one parallel lamination. The outside is imaged, etched, and completed as a normal PCB. This process is seen in Figure 25.

A newer Bbit process has been defined to manufacture wire-bonding and flip-chip substrates. In the Bbit process (shown in Figure 26), the prepreg is laser drilled so that smaller cream Ag solder can be used to bond to the copper.

Neo-Manhattan Bump Interconnect

The Neo-Manhattan Bump Interconnect (NMBI) technology is one of the newest Japanese HDI technologies. It might be considered a *third-generation* HDI technology since tech-

nologies such as ALIVH are considered second-generation HDI technology. NMBI was pioneered by North Corporation of Japan and further refined by Tessera in the USA.

Structure

Figure 27 shows the structure of an NMBI substrate, along with a scanning electron microscope (SEM) of the etched-metal bumps that make up NMBI's via interconnects. Figure 28 shows the density advantage of having land-less vias.

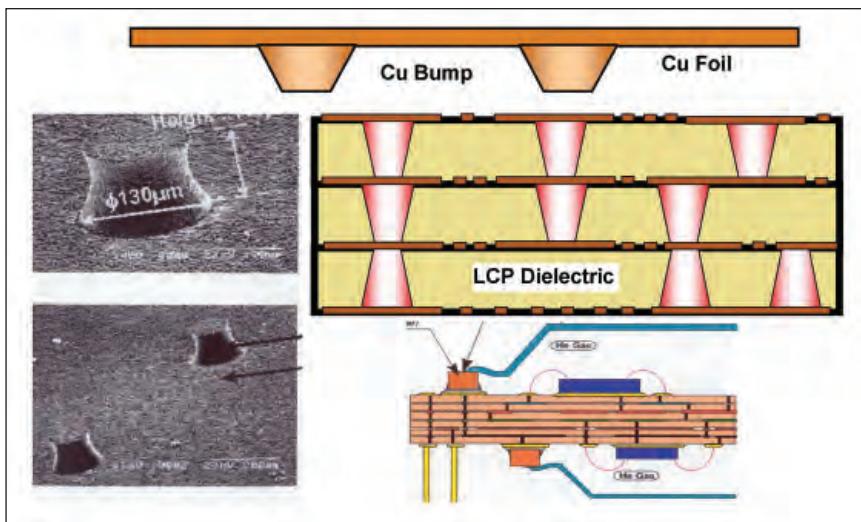


FIGURE 27: Neo-Manhattan Bump Interconnect structure

Manufacturing Process

The manufacturing process for NMBI is unusual in that it does not drill the via connections. Instead, a new material is employed that consists of two different coppers of differing thicknesses that are bonded together. The thicker copper is imaged and etched to form the interconnect vias which are then filled with a film or liquid dielectric. They are bonded to copper foil and cured. The copper foils are then imaged and etched to circuitize the layer-pair. The layer-pairs can be tested

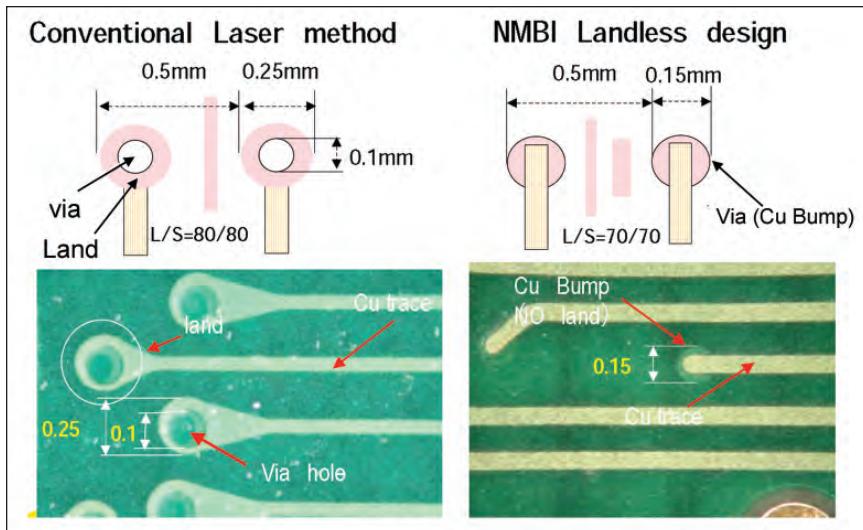


FIGURE 28: Conventional plated TH vias and lands compared to NMBI 'land-less' constructions

and later be stacked with uncured NMBI structures to form the final multilayer. Like the second-generation ALIVH HDI structure, an NMBI structure allows the connection of any layer to any other layer. This manufacturing process is shown in Figure 29.

The OCCAM Process

The OCCAM Process is a new idea from inventor Joe Fjelstad of Verdant Electronics. It was briefly mentioned in Chapter 14 - *Embedded Components*. Unlike other HDI processes, the OCCAM Process is quite a radical departure from HDI in that the components are assembled first and then the OCCAM board is fabricated over them, eliminating the need for soldering. The interconnect is made directly to the component lead by laser drilling and direct metallization, which facilitates very high-density wiring since SMT land patterns are not required. (Remember, no soldering.) High-density component placement and wiring allows other innovations like the layer-pair

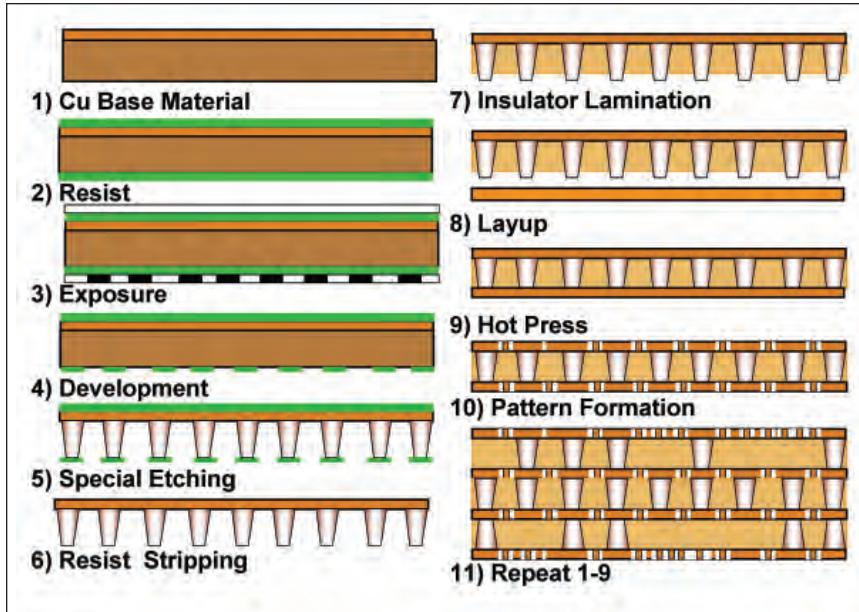


FIGURE 29: Manufacturing process for the NMBI substrates

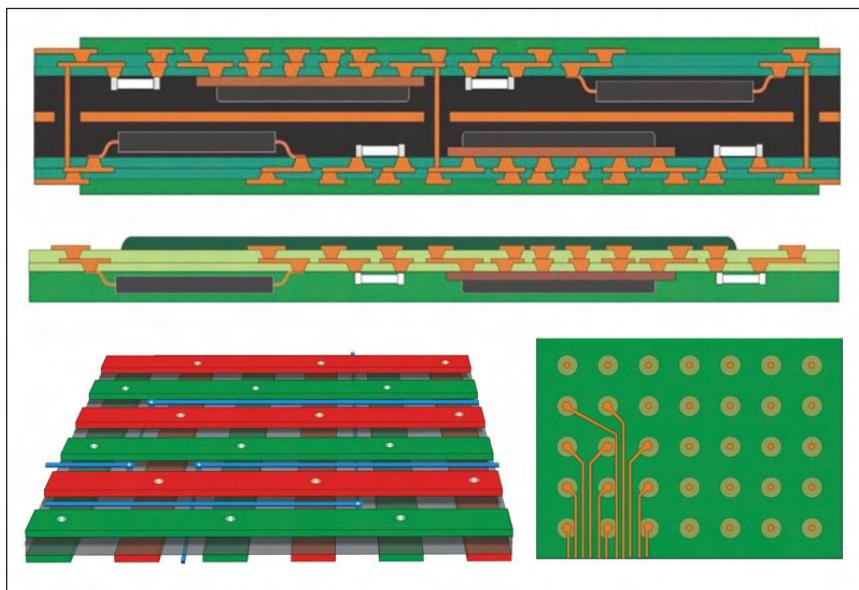


FIGURE 30: The OCCAM Process was invented to eliminate soldering and increase component density. Shown here are two OCCAM structures, along with the Power Mesh power delivery architecture and an illustration of higher density wiring because there are no solder land patterns. (Courtesy of Verdant Electronics)

Power Mesh Architecture for power delivery.[9] These can be seen in Figure 30.

Manufacturing Process

Like the GE HDI process that started this chapter, the OCCAM Process is a packaged chips-first type of process. Unlike the HDI process, this process uses finished, packaged, and tested components. The manufacturing process is shown in Figure 31.

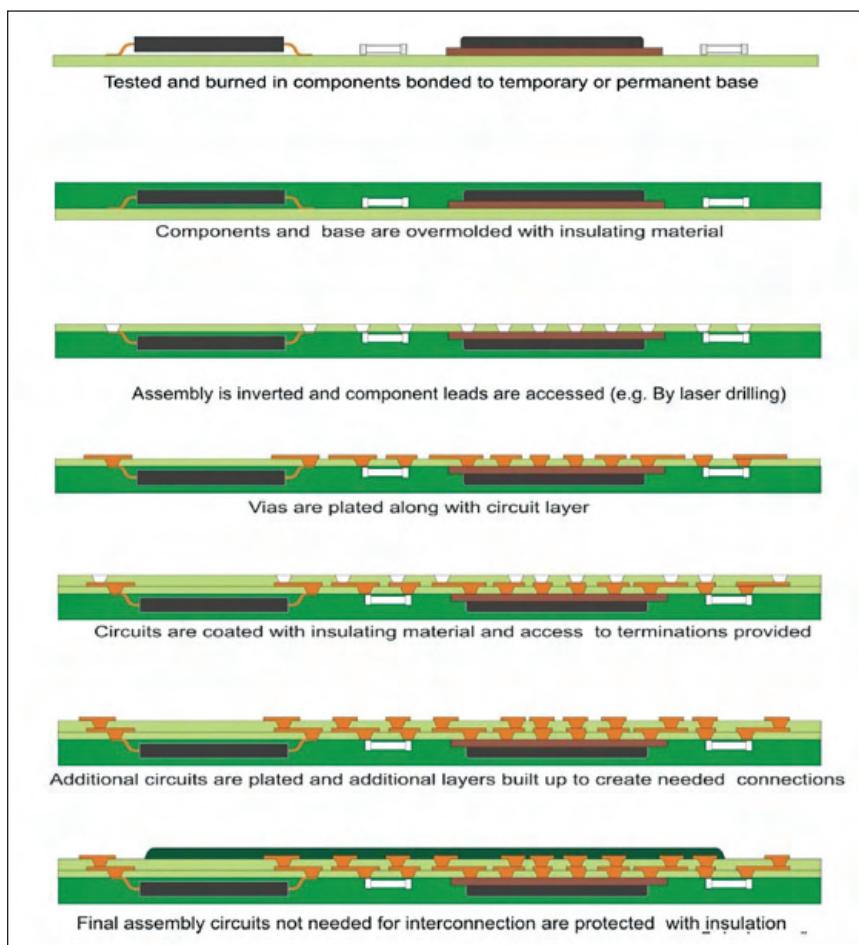


FIGURE 31: The OCCAM Process starts with the components and then builds the interconnects over the components. (Courtesy of Verdant Electronics)

Next-Generation HDI Processes

HDI and microvias provide a big boost in density due to miniaturization. Next generation HDI technologies will continue to evolve and become smaller, following integrated circuit cell geometries. The next revolution will be in optical wiring. Currently, optical networking ties together continents and cities, providing the backbone of modern worldwide networking. There is fierce market competition over what technology will provide *the last mile* on connectivity? Optical wiring is competing for that market.

Printed Optical Waveguides

Although electrical signals can be multiplexed on a single 100-micron wire or trace, many individual laser wavelengths can each carry many multiplexed signals on a single 100-micron waveguide, resulting in a 10,000-fold increase in information handling which is not influenced by magnetic and electrical fields such as electronic signals. Optical conduits can now

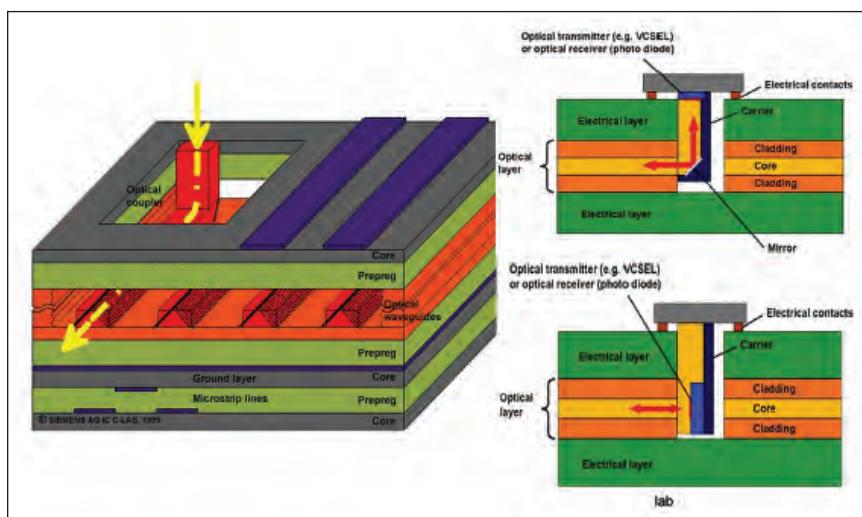


FIGURE 32: Structure of a printed optical waveguide (Courtesy of Siemens C-Lab) [23-27]

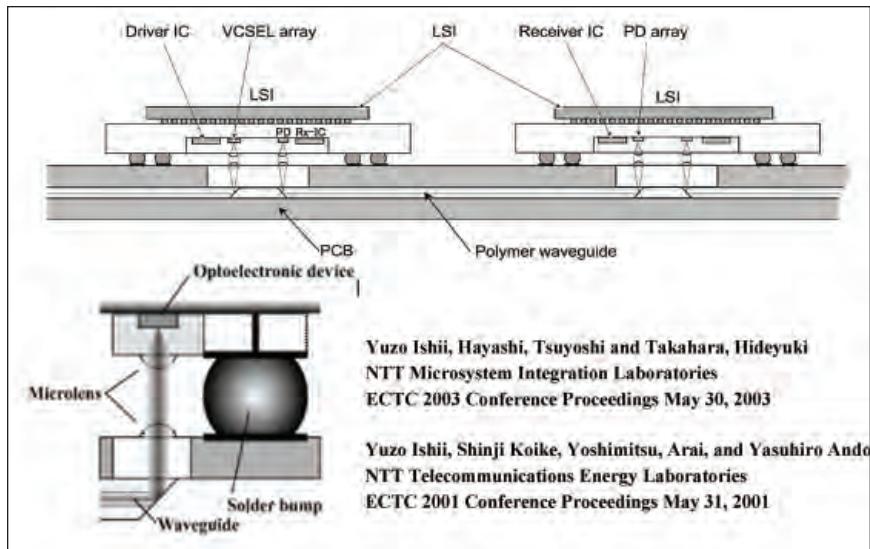


FIGURE 33: NTT waveguide-on-board concept with OptoBump packages (Courtesy of NTT-Lab)

be mass-produced on printed circuits as polymer optical waveguides, as shown in Figure 32. Much like when the industry transitioned from single-point soldering by individual wires to printed circuits, single-point fiber-optical cabling can now have low-cost printed waveguides.

Structures

Optical waveguide structures are shown in Figure 33. The transmitter package provides the multiplexed laser signal source through vertical cavity surface emitting laser (VCSEL) arrays into mirrors at the optical polymer waveguide level. The receiver package uses mirrors to direct the laser signal up into photodiode arrays.

Components

Figure 34 shows what the transmitter BGA packages will look like, whereas Figure 35 shows what the receiver BGA

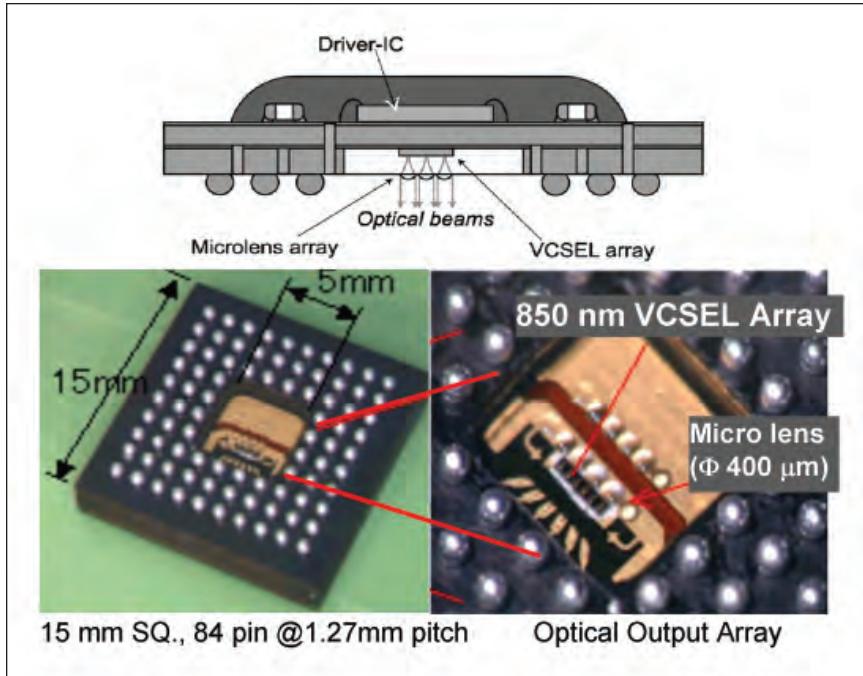


FIGURE 34: NTT chip-to-chip optical interconnection, transmitter (Tx), and details of the optical output array (Courtesy of NTT-Lab)

package with micro-mirrors, VCSEL, and photo-receptor sensors may look like.

The optical materials being considered for integrated waveguides are currently polymers. Polymers have a number of advantages:

Stable — Polymers offer high thermal stability and long-term photostability. Bellcore Telecordia compliance (i.e., 1209, 1221) tested for less than 600 hours at 85°C/85 relative humidity (RH), solder temperature >230°C, and degradation temperature >350°C.

Well-established — A huge body of data has been gathered on polymers over the last 100 years, including all the popular photoresists.

Useful — Polymers have unique properties (such as su-

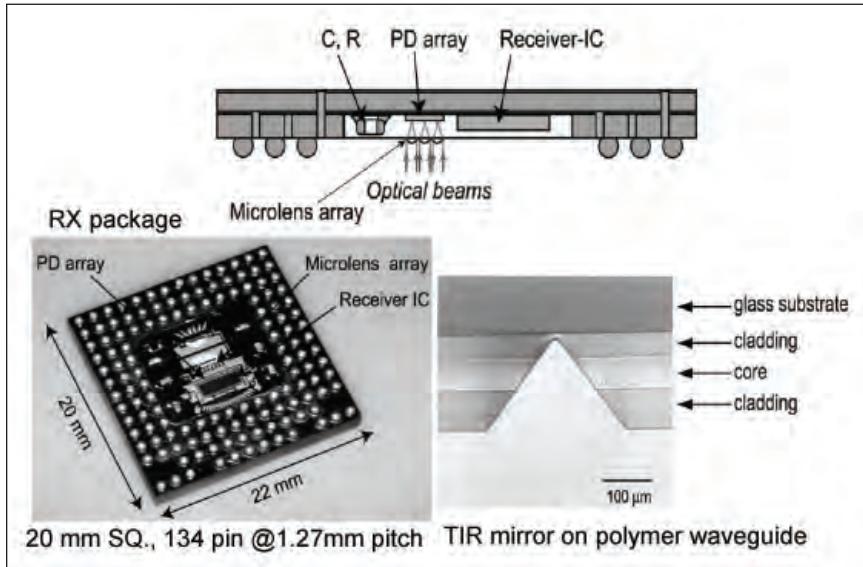


FIGURE 35: NTT chip-to-chip optical receiver (Rx) module and mounting schemes for the VCSEL, mirrors, and photo-receptors (Courtesy of NTT-Lab)

perior bend radii, modulus, and index tuning) that cannot be found anywhere else. These properties include unique processing options such as photolithographic, reactive ion etching (RIE), direct laser writing, molding, and printing.

Polymers also have a number of disadvantages:

Unstable — Many polymers have low thermal stability (POF below 80°C) with photodegradation (laser dyes < days) and are sensitive to delamination, moisture, and chemicals.

Unknown — New materials require new processes, equipment, and experience.

Useless — Some polymers have POF losses of 20 dB/km, whereas optical glass is <0.1 dB/km. The packaging cost of polymers represents 80% of the cost of devices.

Candidate materials are acrylates, halogenated acrylates, cyclobutenes, polyimides, and polysiloxane. Table 3 lists many of the most popular materials. The optical losses of the

TABLE 3: Polymers for Optical Waveguides and Candidate Materials

Manufacturer	Polymer Type	Patterning Techniques	Waveguide Optical Loss (dB/cm)		
			840 nm	1300 nm	1550 nm
Allied Signal	Halogenated Acrylate	Lithographic, RIE Laser	0.01	0.03	0.07
	Acrylate	Lithographic, RIE Laser	0.02	0.2	0.5
Dow Chemical	Benzocyclobutene	RIE	0.8	1.5	
	Perfluorocyclobutene	RIE	0.01	0.02	0.03
DuPont	Acrylate (Polyguide)	Lithographic	0.2	0.6	
	Teflon AF	RIE			
Amoco	Fluorinated polyimide	Lithographic		0.4	1.0
BF Goodrich	Polynorbornenes	Lithographic	0.18		
Gen Electric	Polyetherimide	RIE, Laser	0.24		
JDSU	Acrylate	RIE			
Terahertz	Acrylate	Lithographic	0.03	0.4	0.8
NTT	Halogenated Acrylate	RIE	0.02	0.07	1.7
	Polysiloxane	RIE	0.17	0.43	
Asahi	Cytop	RIE		0.3	
Nippon Paint	Polysilane-photosensitive	Lithographic Photo bleaching	0.1	0.06–0.2	0.04–0.9

polymers (dB/cm) are in the lower wavelengths near 840 nm.[21,22,23]

Manufacturing Process

The manufacturing process for polymer optical waveguides is similar to using a liquid photoresist. Roller coating or meniscus coating of the liquid polymer is all that is required to apply the optical polymer to a standard inner-layer. After drying, the optical polymer is exposed through standard photo masks and developed. After a final curing, the optimal polymers are laminated into standard multilayers with prepgs. Figure 36 shows

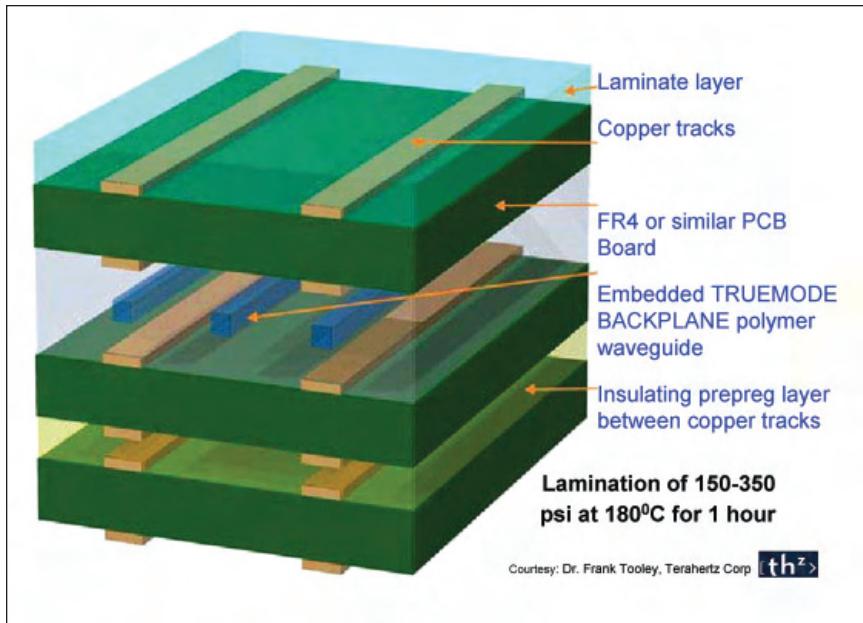


FIGURE 36: Optical waveguide stack-up in a conventional multilayer prior to lamination (Courtesy of Terahertz Corporation)

the lay-up of the TRUEMODE optical polymer from Terahertz Corporation.

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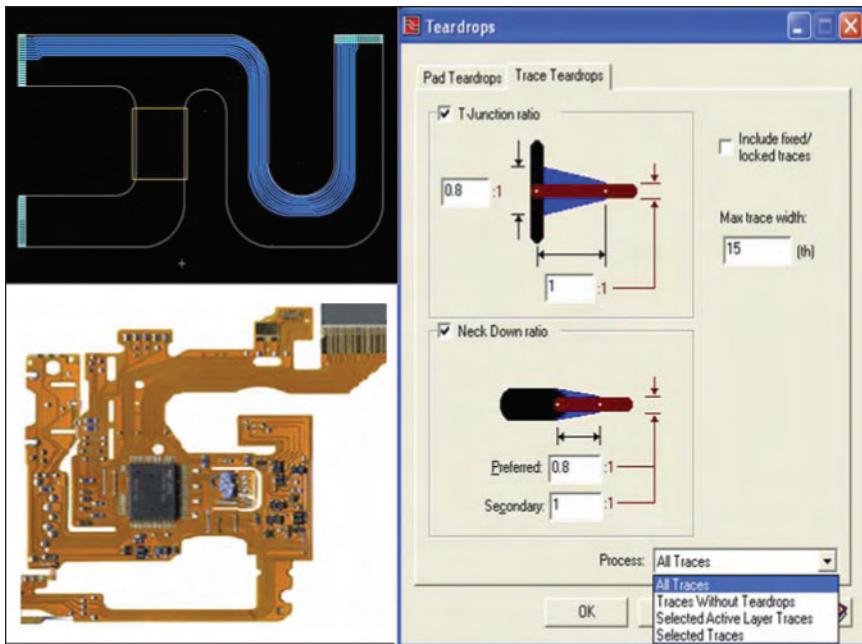
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16

Advanced Packaging and System-in-Packages

By Per Viklund — *Mentor Graphics*

Introduction

Silicon packaging of dies by wire bonding and flip-chip is the foundation of packaging. Traditional silicon packaging is evolving to 3-D/stacked dies and multiple-components as in System-in-Package (SiP). Current trends leading to a higher level of 3-D integration create big challenges for design tools, methodologies, and the individual designer. In Chapter 1, it is stated: The design and the manufacture of

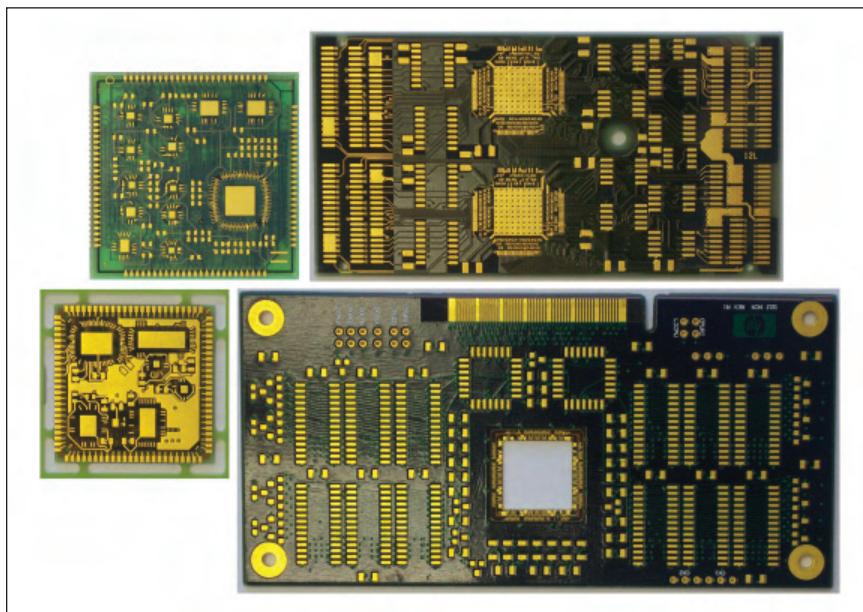


FIGURE 1: Advanced packaging is being used on PCBs and to package bare silicon.

these interconnections have evolved into a separate discipline called *electronic packaging*.

What then is Advanced Packaging? Advanced packaging is the term that is rather carelessly used for the design of chip-packages. I say carelessly, because today all of the techniques and technologies first used in chip packaging are being used on printed circuit boards in order to increase function/area ratio and/or performance.

Our focus is to introduce the advanced technologies used in advanced packaging, whether the purpose is to design a chip-package or a printed circuit board (PCB).

MCM, Hybrid, SiP, SoP: Nomenclature

There are many acronyms and buzzwords in the world of advanced packaging. Abbreviations and acronyms are used frequently and often with different meanings. We will list some of the more common abbreviations and take a look at what they really mean. You will see that some are just variations on a theme and that the boundaries are often fuzzy. It is not the intention to present a complete glossary, but to explain the terms needed to follow this chapter.

Multi Chip Module (MCM)

Multi Chip Module (MCM) is a package technology where multiple dies are combined in a single package. MCMs were first used in the 1970s. There are a few subtypes based on what type of substrate technology is used:

- **MCM-L:** L stands for Laminate. MCM-L uses a classic laminated PCB as substrate.
- **MCM-C:** C stands for Ceramic. MCM-C (Figure 1) uses a ceramic substrate such as Low Temperature Co-fired Ceramic (LTCC).

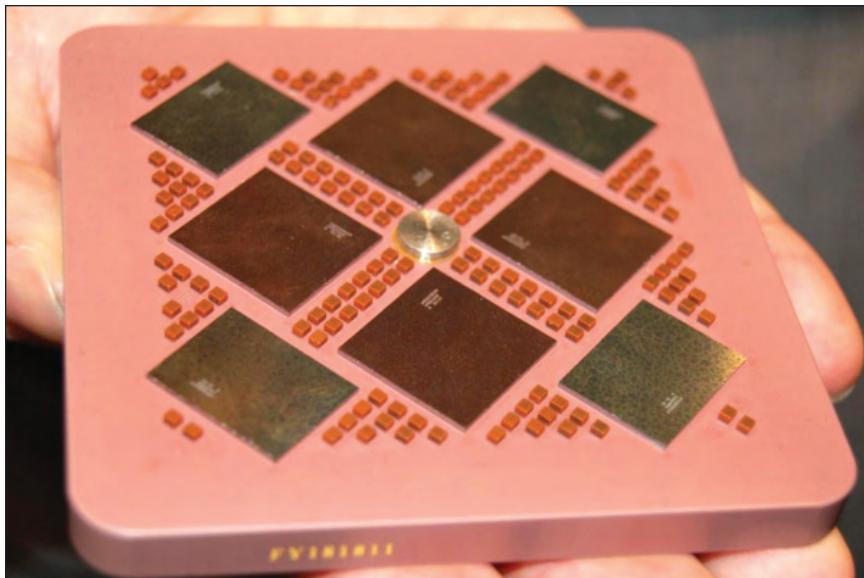


FIGURE 2: IBM Power5 CPU using MCM-C technology as a 95x95 mm module[1]

- **MCM-D:** D stands for Deposited. The substrate pattern is deposited using a metal deposition vacuum sputter and a thin-film structure, which means high cost, but very high wiring density.

Some MCMs contain passive components as well as a mix of analog and digital functions. The boundary between MCM and SiP (if there has ever been a boundary) becomes fuzzy. Die attach can be by wire bonding or flip-chip.

Hybrid

Hybrids started under several different names. Around 1950 there was a program named “Project Tinkertoy” driven by the US National Bureau of Standards to promote the development of dense circuit assemblies containing multiple transistors and passive parts on a ceramic substrate. The technology was expensive but some came into high volume production with

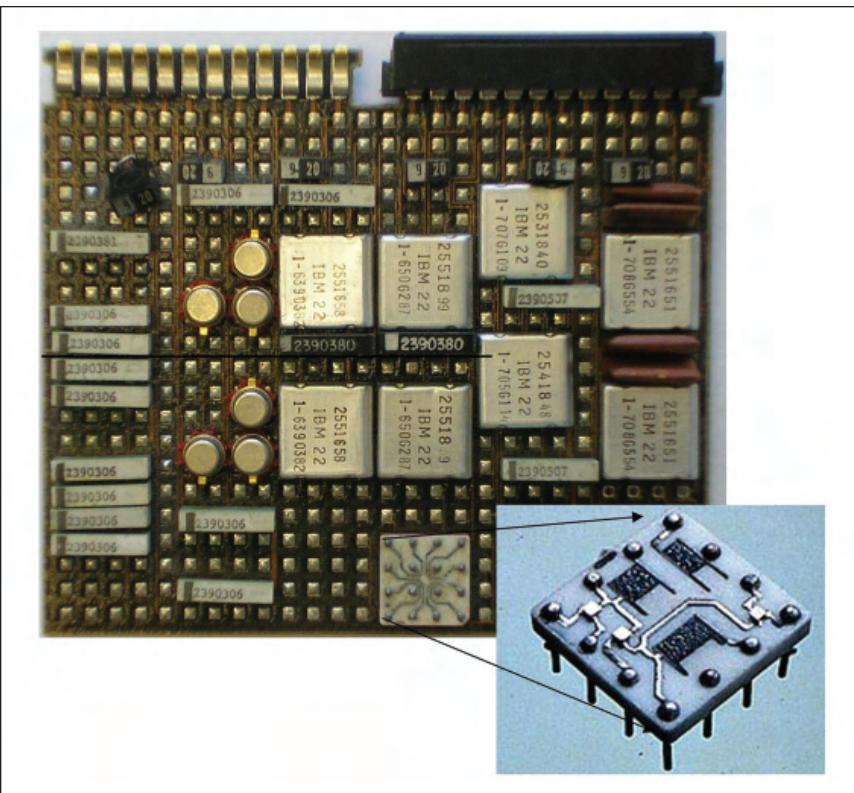


FIGURE 3: SLT modules (0.5 inch square) for IBM's System/360 computers back in the mid-1960s utilizing ceramic hybrids

the development of Solid Logic Technology (SLT) modules for IBM's System/360 computers back in the mid 1960s (Figure 3).

SLT is still used for applications of high power modules, high temperature resistance, and for RF modules. There are many sub-types based on the substrate technology, such as Low Temperature Co-fired Ceramic (LTCC) and High Temperature Co-fired Ceramic (HTCC).

During manufacturing, a tape-based material is used and processed once to form holes, cavities, and conductors. The entire "sandwich" is baked (sintered) to form a homogenous substrate. DuPont's Green Tape is a common material for

LTCC. HTCC is sintered at around 1,500 degrees C while LTCC is sintered at around 875 degrees C. At the higher temperatures of HTCC, the conductors have to be made of tungsten or molybdenum which are not ideal conductors. At the lower temperatures of LTCC, the conductor material can be gold or silver which are much better conductors. During the sintering process, the material will shrink. This shrinkage can be significant and therefore the fabrication artwork has to be scaled to compensate for the shrinkage.

System-in-Package

System-in-Package (SiP) is a chip-package containing more than one die combined with passive components. Some may argue that these passive parts have to be classic discrete parts, while others claim that integral embedded passives also belong to SiP technology. It is common for ICs to use different technologies such as digital signal processing, RF microwave amplifiers, and radio circuits.

In System on Chip (SoC), a single large-scale multi-technology chip is packaged as a complete system. The advantage of SiP is that custom ASICs can be combined with standard components, such as memory chips, into a very flexible system. The design time and total cost is reduced, but at the cost of a somewhat lower function/area density. Above all, the risks in the design process are lower as the building blocks are less complex.

System on Package (SoP)

System on Package (SoP) originates from the Georgia Institute of Technology (Georgia Tech) under the lead of Dr. Rau R. Tummala. SoP is a package or module with more than one die in combination with thin-film-based embedded

passives. Some would argue that an SoP is identical to an SiP because they have certain elements in common. However, for a true SoP, the substrate is built up using organic buildup technologies similar to those used in the IC industry, while an SiP can use a laminated substrate. In fact, Dr. Tummala considers SiP to be a subset of SoP.

Package on Package (PoP)

Package on Package (PoP) is a technology to stack BGA packages in order to increase function/area. The PoP package itself can be a SoC, SoP, SiP, or any other type of package technology.

The basic BGA package has BGA balls on the bottom surface and BGA pads on the upper surface as shown in Figure 4. Another BGA can be soldered on top of this lower component. Stacking can be two to six parts high or even more. The most common PoP applications would only stack two parts high. To connect the upper parts, one connects to the lower-most part and internal connections in this part lead the signal to the upper surface pins.

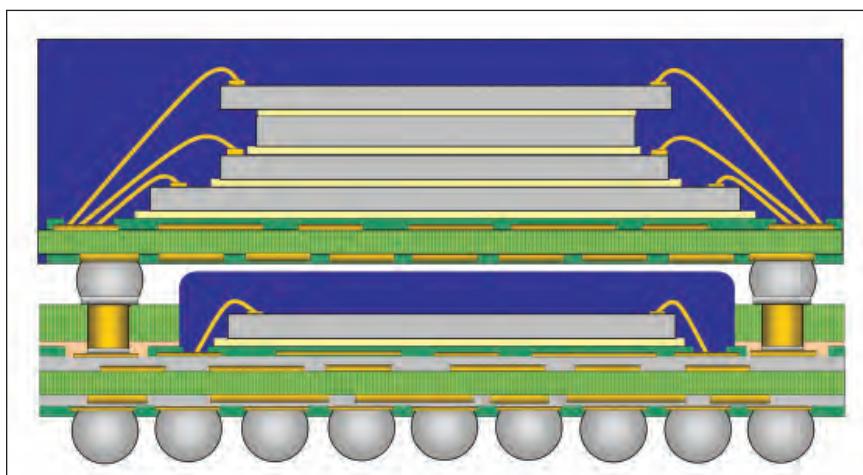


FIGURE 4: Stacking of packaged parts with PoP technology

Through Silicon Via (TSV)

Through Silicon Via (TSV) is a technology to stack dies and interconnect them with via holes right through the silicon. It is similar to PoP but now with bare dies. A multitude of technologies to create TSVs have been developed.

Wafer Level Package (WLP)

Wafer Level Package (WLP) is a single die with the BGA bumps applied directly to the wafer surface yielding a package with almost the same size as the die. WLPs are sometimes called Wafer Level Chip Scale Packages (WL-CSP). Typically the bumps are applied before the dies are singulated (separated from the wafer), hence the name Wafer Level.

Chip Scale Package (CSP)

Chip Scale Package (CSP) is defined in IPC standard J-STD-012 as a single die package where the size of the package is a maximum of 1.2 times the size of the bare die.

Flip-Chip

Flip-chip is a method to connect a die to the substrate. Rather than wire bonding, a flip-chip uses a bump grid pattern

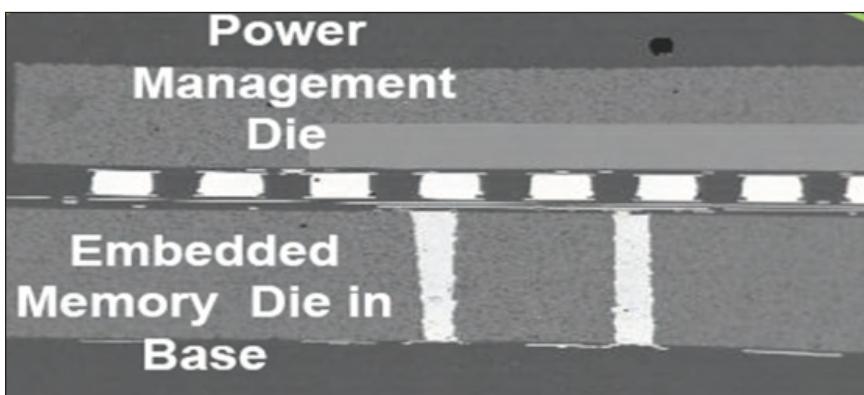


FIGURE 5: TSV used to directly integrate two separate dies

similar to a BGA. The connection can be either a reflow solder joint, a thermo sonic bond, or Anisotropic Conductive Film (ACF), which is an environmentally-friendly epoxy-based technology.

The site www.flipchips.com provides a wealth of information spanning from overview to detailed tutorials.

Controlled Collapse Chip Connection (C4)

Controlled Collapse Chip Connection (C4) is a flip-chip technology developed by IBM. The flip-chip bumps are made of solder. When they melt, they collapse and become shaped by the surface tension of the melted metal, hence the term controlled collapse.

Controlled Collapse Chip Carrier Connection (C5)

C5 has the same technology as C4, but the connection is not made directly to the chip. The connection is made to some form of chip carrier such as a chip-package.

Redistribution Layer (RDL)

The I/O locations on a chip core are usually at a dense pitch and offset from the practical package pattern grids the flip-chip bumps are placed on. Therefore, a connection is needed from the I/O bump to the chip core I/O. This connection is made as a metal layer on the chip. It is called a Redistribution Layer because it redistributes the I/O locations. The same term is used for the routing that connects the I/O cell for wire bonding to the chip core I/O location.

3-D Packaging

3-D packaging is a general concept that simply means the assembly of parts in a vertical direction (typically by stacking

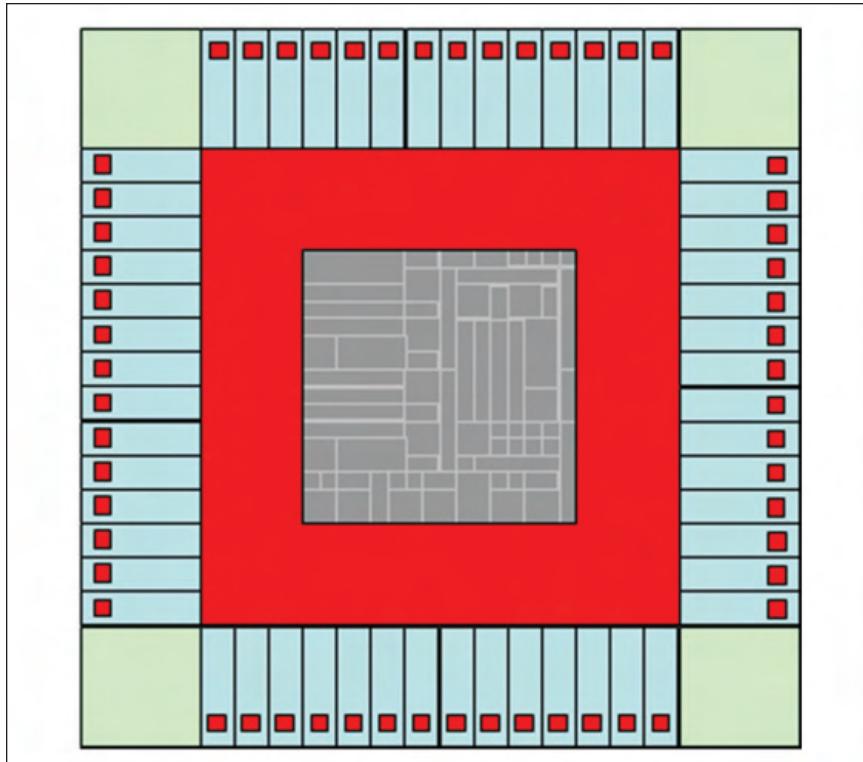


FIGURE 6: Sketch of a pad-limited design with the wasted die area in red

bare dies). An MCM, an SiP, or an SoP can all utilize 3-D packaging.

Pad-Limited Design

In a pad-limited design the number of I/Os are plenty with respect to core size. This means that when all I/O cells are placed, the area inside the I/O ring is larger than the chip core which results in wasted die area (Figure 6). The wasted area drives up the design cost so various techniques are usually applied in order to better utilize the die area.

Core Limited Design

In a core limited chip design, when placed close together

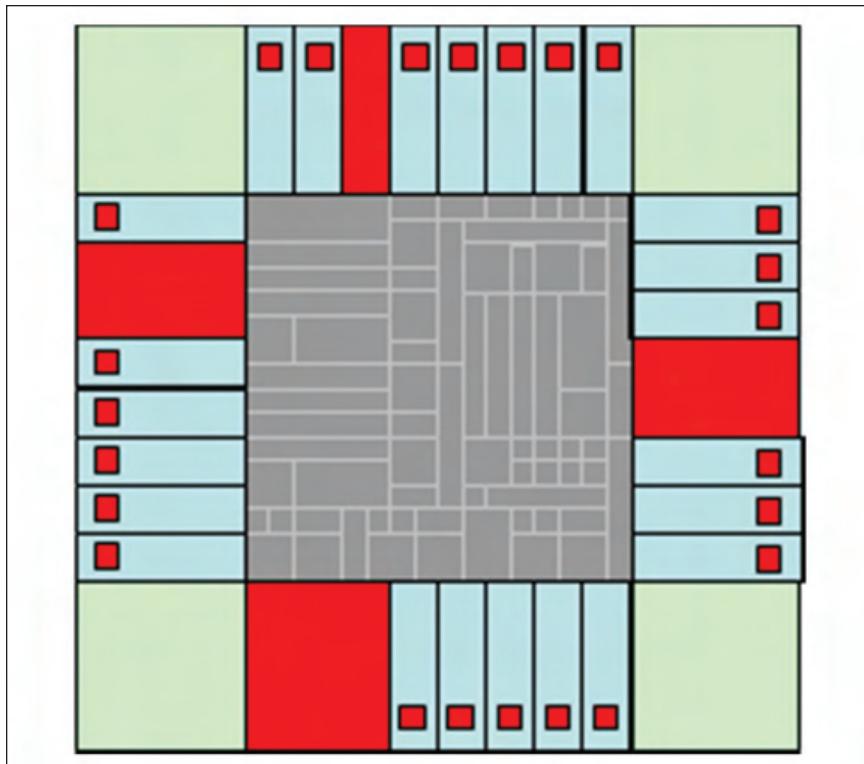


FIGURE 7: Sketch of a core limited design with the wasted die areas shown in red

around the perimeter of the core, the I/O cells will not entirely fill the available space.

These gaps are typically filled with special filler cells since gaps in the I/O ring can cause breaks in the power and ground rings.

Chip-Package-Board Co-design

When a chip is going to be connected to a package and the package in turn is going to be connected to a board, it becomes interesting to design the chip I/O and power/ground system and the package pin out so that the total system performance is maximized. Routability of signals and power/ground on

both package and board are optimized. With few I/Os this process could be managed manually and this is still widespread today with the aid of extremely large spreadsheet files, home-brewed ASCII formats, proprietary scripts and programs. Having several hundred or even thousands of interconnects, it is no longer practical to do this optimization by hand.

It is even more important to be able to change the chip design. Any investigation of what I/O drive strength is needed, where the I/O cell should be located, or how the power/ground system should be laid out has to be done while the chip is still in design, before the place and route process of the chip I/O system, and above all before tape-out. Changes to a nearly completed chip are extremely costly. The combination of design challenges has led to a computer-aided process called chip-package-board co-design, which has a number of applications and components.

Virtual Prototyping

The key to co-design is to be able to make changes very early in the design process while the cost of change is low and the freedom of choice is the largest. Unless we have some data about our design, it is difficult to make any educated decisions. Actual design data probably does not exist. For example, the chip may not have been designed and the package and the board are not even started. We still need to evaluate different scenarios and let the outcome of our analysis guide our design activities.

Virtual prototyping allows us to use estimated, or even “guesstimated,” input in the analysis. The output may not be very precise but in many cases it can still give us a great deal of information that will help us design a better system.

Let us take for example a system that we know will have one ASIC, use two of the shelf memory dies in one package,

and will place this package on a board with a known bus system such as PCI Express. We know that the ASIC will have approximately 200 I/Os and we expect about the same number of power/ground connections. We also know that we are going to use an I/O library where the I/O cells are 90x180 um in size. With this data, we can mock up the ASIC I/O and power/ground system and create a dummy die part.

Using the dummy part and the off-the-shelf memory parts, we can make a mock-up package and place it on a mock-up board. This will tell us a number of things about our design. Knowing the size of the I/O placement and the available size for the chip core will help us decide between wire bonding and flip-chip. We can investigate this for one or multiple rows of I/O cells and for area array I/O (flip-chip) configurations.

We will also be able to make a preliminary package selection since we now know the approximate size of the dies and the number of pins we need. We can even do some early package power network prototyping with a Power Integrity (PI) tool. In addition we can do some preliminary investigations on the required I/O drive strengths. Driving with the least strength possible is significant in order to keep overall power consumption down. With a mock-up PCB we can even investigate practical signal allocations to the package.

It is crucial to have this knowledge early, because until the chip has passed place and route and before the package is designed, the cost of change is extremely low. On the other hand, if the chip has passed the tape-out stage, any change, whether small or large, will come at an astronomical cost.

The transition from Virtual Prototyping to actual design should be gradual. If the design starts 100% virtual, actual design data is then used to replace virtual data as it becomes available. For example, VHDL or Verilog source files from the

The HDI Handbook

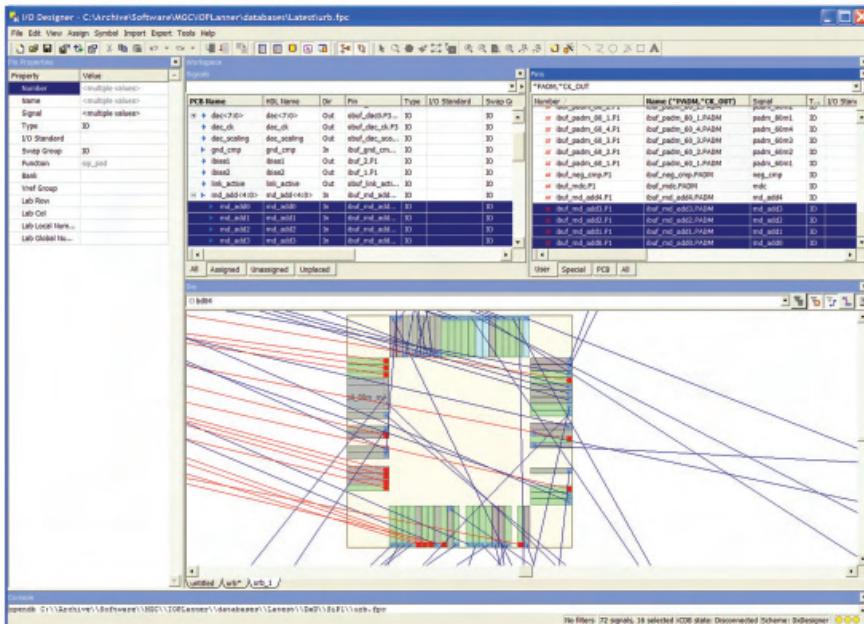


FIGURE 8: A chip-package-board co-design tool shows how a mix of virtual and actual design data is used to form the basis for early design decisions.

chip design can be used to create an actual package signal list and LEF or Open Access data for the selected I/O library can be imported to replace the virtual I/O cells with real ones (Figure 8). The virtual data can be used for early decisions and trade-offs, while the gradual introduction of real design data lets the design converge toward an optimum for chip, package, and even PCB at the same time.

Power Grid Design

Power grid design is all about making sure that when the package is placed on a board, the circuitry in the package is getting the power it needs with sufficient quality for safe operation. Special Power Integrity tools are typically used to help design a functional power delivery system (Figure 9). These tools can operate in a virtual prototyping fashion to

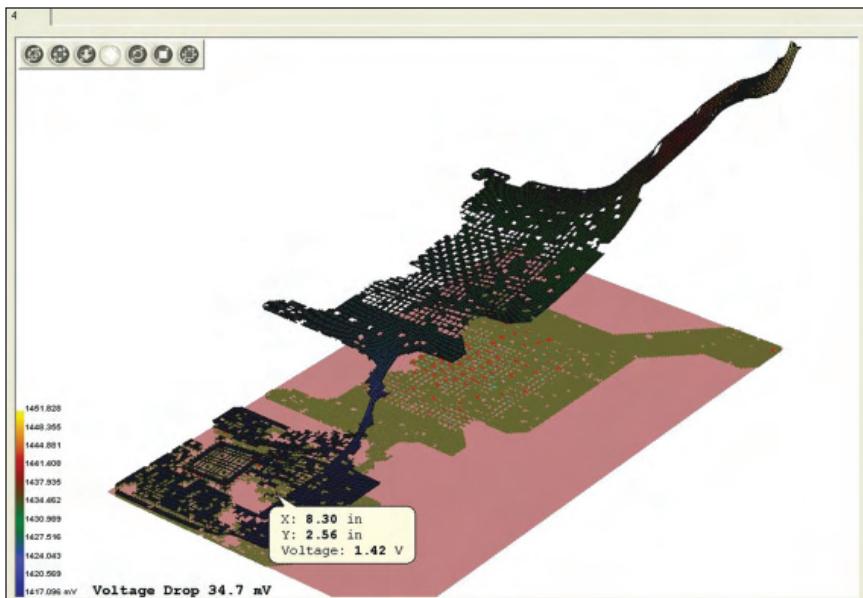


FIGURE 9: Analysis result of a power/ground system

let you pre-plan your power grid. They can also be used in a detailed analysis and verification mode to validate your actual implementation before manufacturing.

There are many factors to consider in power grid design:

I/O activity: The more signal activity there is, the higher the power consumption will be for that I/O system.

Chip core activity: The faster the core is operating, the more energy is needed. In the power grid design you need to ensure that enough energy is fed to the core to sustain its operation.

Voltage levels, logic thresholds, and noise margins:

Low voltage systems help reduce power consumption and are key to avoiding ASIC meltdown of dense designs. Unfortunately, this means that the logic thresholds and noise margins become smaller which also means that the requirements for a noise free power/ground system become stronger.

Power ground plane configuration and decoupling:

The way the power and ground planes are arranged in the substrate stack-up has a profound impact on power integrity. If there is a single power plane, if it is fractioned to support multiple voltages, or if the power is supplied through routing rather than using planes, power integrity will be affected.

The plane must be able to deliver a large enough electrical charge in a short enough time to support the logic transitions at a specified speed. Power can be regarded as a signal propagating down a transmission line. It will have a finite signal speed as will the charge on the ground plane, meaning that only the charge stored close to a circuit can be used to support a logic transition.

Using a distributed capacitance plane, only the plane very near to a power/ground pin will be useful. The locally stored charge can be increased by adding decoupling capacitors. In doing so, one must take great care to connect the capacitor in a low inductance fashion.

Wire bond parasitics: Wire bonds have some amount of inductance. Delivering power/ground over wire bonds means that this inductance will try to oppose the charge delivery to the circuit. There are various techniques to mitigate this effect and they are all based on lowering the combined inductance.

If you connect two inductors in parallel, the combined inductance becomes half that of a single wire. Three wires give one third the inductance of a single wire and four wires give one fourth the inductance of a single wire. By using several power/ground cells to the circuit and to wire bond each with more than one wire, the power system will perform better.

Non-ideal power/ground from the board: The power and ground planes are never ideal. They usually possess more

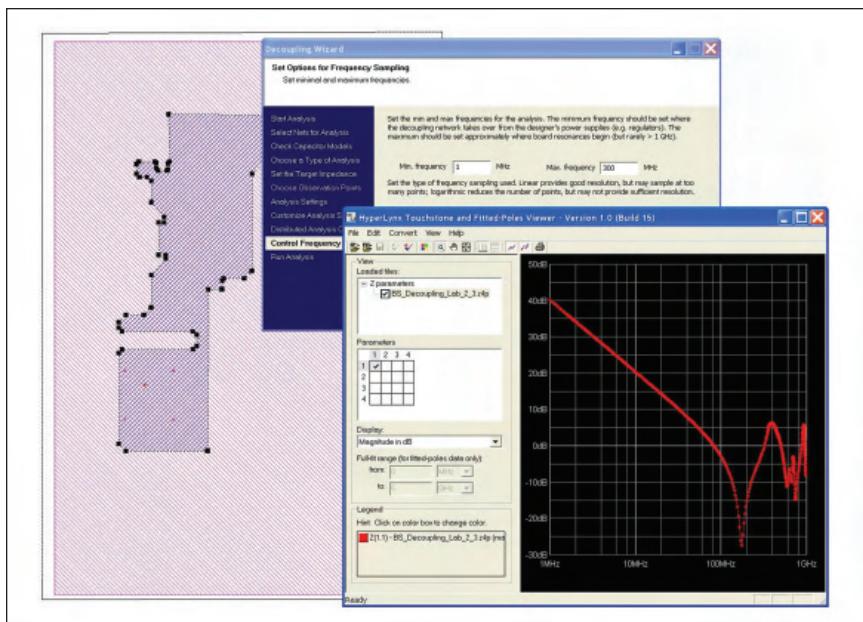


FIGURE 10: Special design tools help with early planning of the power grid.

or less inductance that will oppose when the circuit tries to draw current from it. It is the responsibility of the substrate and board designers to make sure that features that fracture the power/ground planes are not placed in the way of the power delivery or return paths.

Power/Ground cell placement – adding more cells:

The actual number of power/ground cells and their placement are prerequisites for correct power grid design. Using actual or estimated power consumption per I/O cell, the designer can estimate the required number of cells and also their placement. To really know if the number of cells is correct and if the placement is optimal, a real Power Integrity analysis is required.

With all of the above to consider, it is vital to start the planning and design of the power delivery network early. Special virtual prototyping tools exist to help with this task

(Figure 10). This way we can create an outline for the power system and analyze its behavior before we are too far into the design process.

Package Selection Criteria

Traditionally, package selection, or even package design as a whole, was a post-process after-chip design. Today it is widely recognized that package design including package type/model selection has to be an integrated part of the design flow.

The package is an added cost and it generally impacts performance in a negative manner. Performance-wise, the ideal would be no package at all but then the cost is added to handle bare dies and for various reasons, the industry still prefers to use packaged parts. Consequently, we need to choose packaging technology and a package type/model that helps preserve the chip performance and has the lowest cost.

New package technology is constantly being developed, so the best advice is to stay in close contact with package providers and make use of their expertise in selecting the proper package. There are several factors to consider:

- Will the package handle the package substrate size I need?
- Will the package have enough pins to cover both my I/Os and my power/ground requirements? Here it is important to remember that you may require more power/ground pins than you initially thought in order to achieve acceptable power integrity.
- Will the package be able to handle chip to package pin interconnects with the high-speed or RF performance I need?

Package Ball-Out Optimization

Package Ball-Out Optimization refers to allocating signal names to the BGA balls of a BGA package. The term is also generally used for non-BGA style packages. The ball-out should be driven from board connectivity. As the package is placed on a board, its I/Os have to be routed to adjacent components on the PCB. When using FPGAs it is a common practice to optimize the I/O locations so that the signals can be routed on the PCB with shorter line lengths and fewer via holes in order to make the PCB more routable and to maintain high signal integrity. For FPGAs this I/O optimization is achieved by altering the software of the FPGA while keeping in mind the various rules for how the I/Os can be legally organized.

Using package ball-out optimization, we are dealing with a package that can, in theory, assign the signals to pins any way we like without changing software. The reality is that there are many rules governing how the signals can be arranged:

- Keep core power and core ground to the center of the BGA pin array.
- Keep differential pairs together.
- Assign an I/O ground pin for each differential pair.
- Keep busses together.
- Keep digital signals away from analog signals.
- Keep RF signals away from all other signals.

The rules will vary with each application, but there are always multiple rules and frequently the rules conflict, which leads to a painful and lengthy arbitration process trying to narrow down a ball-out solution that best fits the given rule set (Figure 11).

The package ball-out process must be driven from the board connectivity. Many times the board does not exist at

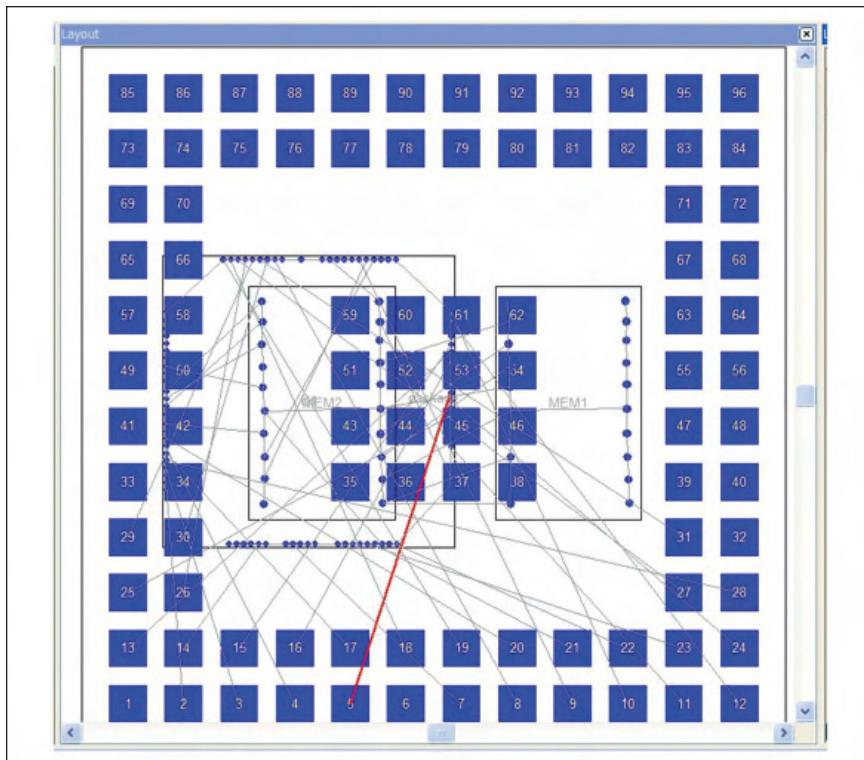


FIGURE 11: There are many package ball-out rules and they often contradict each other. Package-board co-design tools let you optimize the pin-out against all rules simultaneously.

the time of package design, whether the package is designed to be an off-the-shelf or in-house product. In both these cases it is usually possible to make some educated assumptions about what circuitry will be placed around the package being designed. With this knowledge, one can build a board mock-up that is a fair representation of a generic application for the package. This mock-up should then be used to optimize the signal, power, and ground assignments for the package. To put the importance of this step in some perspective, trying to assign package pins without considering the board will always lead to added cost and decreased performance for every single board designed with this package.

As in the case of FPGAs, the process is extremely hard to manage by hand so special I/O design or chip-package-board co-design tools must be used to reach an optimal solution in a reasonable time. The signal assignments will have a profound impact on the routing between the package pins and the silicon so we need to make this part of the I/O optimization before optimizing the chip I/O placement.

Silicon I/O Placement and Optimization

Silicon I/O placement and optimization involves selecting I/O cells from the chosen I/O cell libraries and placing them either as an I/O ring around the chip core or distributed over the many I/O and power/ground cells. Co-design tools will automatically place the I/O cells according to the design rules and will use simple initial placement rules such as placing the I/O on the chip side that puts it closest to the core function it serves. An approximated number of power and ground cells are also placed early on. There are many rules of thumb and a common approximation is to give each I/O cell a power number. For example, 5 for an input; 15 for an output and so on. We can then sum up these numbers in the actual I/O placement and, from experience, use statements like, “need one power and one ground cell for every sum of 55.” Later in the flow, the required number is calculated and/or simulated.

After the initial placement we need to optimize the placement by relocating the I/O cells considering the full system connectivity. This is called unraveling. Once an optimal configuration is found, the new proposed I/O design will be written back to the chip design tools where it will be carefully scrutinized by the chip design team. The chip design team will have opinions regarding some I/O cell and power/ground locations and propose changes that are written to the

co-design tool. The process is repeated until chip, package, and PCB engineers are satisfied and the chip can go to place and route.

3-D Integration

The available design area is not likely to increase over time. To increase function/area density we have only two paths:

- Reduce ASIC feature size to fit more on the same die size.
- Use 3-D stacking to grow circuits in Z-axis.

Chip Stacking

Stacking dies is, in principle, easy. Just stack them and glue them together. In reality it is a little more difficult. We need to be able to access the connections of each die either for wire bonding or for other types of chip connect. In addition, we need to consider the thermal effects of several dies in a very tight space. Even the local area hot spots of each chip core need to be considered to avoid exactly overlapping these. Thermal analysis tools may be required to safely assess a stacking configuration.

Interposer Design

An interposer is placed between two stacked dies and can be anything from a solid piece of metal or plastic to a routed substrate to map connectivity from the upper die to the lower one. The latter is often used in technology isolation where a fine-pitch device is mapped to a lower pitch to be assembled on a PCB of coarser technology than would be needed if the fine-pitch device was placed directly on the PCB.

We will only cover the case where the interposer is a mechanical aid between two dies, but it is important to

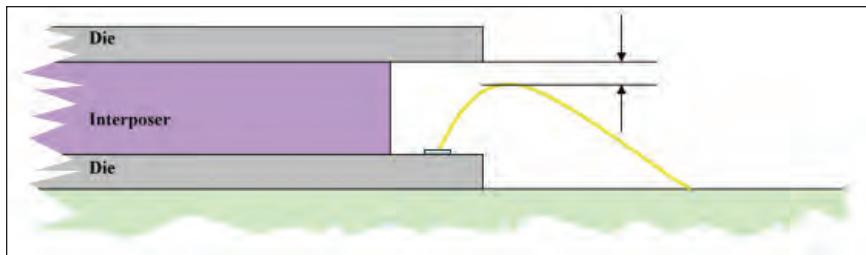


FIGURE 12: The interposer provides the required bond loop-to-die clearance.

remember that the same term is used for both types and often in similar contexts. The interposer's purpose can be to act as a thermal spreader and/or to yield sufficient upper die spacing to make room for the wire bond (Figure 12) and finally to give the upper die sufficient mechanical strength to sustain wire bonding to it.

In this case, the actual wire bonding overhang is measured from the chip die pin opening center to the edge of the interposer. Ideally, this overhang is small but it typically needs to be large enough to allow wire bonding on the die beneath (Figure 13). The thicker the die, the more overhang can be tolerated, as the bond tool can put more force on the die pad before the deflection becomes too large for the bonding process or breaks the die.

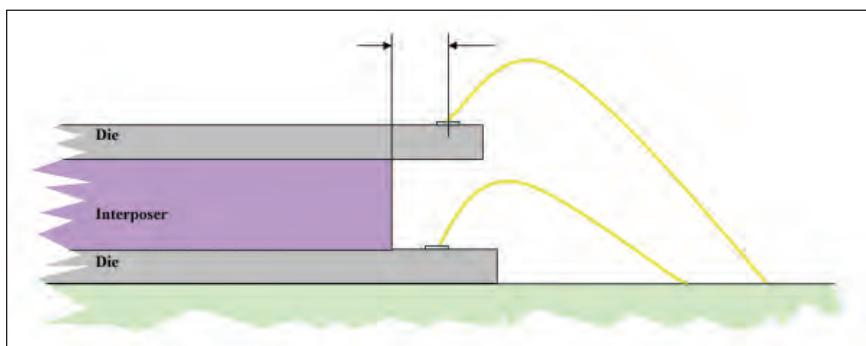


FIGURE 13: In this configuration, the interposer gives the upper die the required strength to sustain wire bonding.

Package on Package (PoP)

In PoP, two or more already packaged components (where one or more surely can be a multi-die package) are stacked and solder pads on the top surface of a lower level package let you solder another package on top (Figure 4). PoP is interesting because it increases function/area density and allows a wide range of flexibility. For example, using a signal processor as the bottom package and various memory packages as the upper parts is an easy way to configure with more or less memory.

To connect from the board to one of the upper part pins, one needs to connect to a pin on the bottom part and rely on internal connections of that bottom part from the board to the upper pins. It is critical to have a neutral schematic, meaning, each part is represented with its true pin naming and any mapping for connection through a bottom level part has to be done at board design level. The reason is that in the design flow, it is common to change the PoP stacking configuration during the design process and making complex modifications to the schematic each time is not feasible.

PoP is becoming increasingly popular, especially among the cell phone handset and consumer electronics industry, due to its flexibility and increased function/area ratio. This has led to a JEDEC standard pin out to make off the shelf parts for PoP assembly possible.

For chip-package-board co-design, PoP adds yet another level of complexity as the package ball-out now covers both the bottom level and upper level pin outs.

In the assembly process there are two options. The complete stack can be built separately and assembled onto the board as one unit. Alternatively, the bottom level part can be assembled to the board first, solder paste dispensed to the

upper level pins, and the second part can be assembled on top of the first.

Thermal concerns

Obviously, the tighter we integrate active parts, the more heat we have the potential to generate. If we don't let the heat out, the circuit may overheat. Directly stacking dies on top of each other results in an almost homogenous piece of silicon with a power dissipation equal to the sum of each die's power dissipation. Other stacking methods, such as PoP, are faced with similar thermal issues. Unless taken into account, thermal issues can cause the design to fail. It is therefore vital to investigate the thermal effects as part of the process of finding the optimal stacking configuration for a design.

It is important to note that for large dies, the power dissipation is typically not even across the chip surface; and for all dies, the power dissipation is dependent on the chip operation and, in some cases, software.

The lowermost die has the advantage of possibly using thermal spreading techniques, improving thermal conductivity from chip to substrate, and increasing metal content in the substrate to help dissipate the heat. The uppermost die could have a heat sink attached. To help even out the temperature between multiple dies, it is common to place a thermally conductive interposer between the dies. In order to get a detailed understanding of the thermal effects one must either build and measure it or use a 3-D thermal analysis tool.

Signal Integrity Concerns

Stacking dies also introduces the risk of cross talk from signals on one die over to the next. If both dies are in-house designs, this can be taken into account and the die rotations

and spacings, as well as the RDL routing, can be made so that signal integrity is secured. With off-the-shelf dies, this is not at all trivial since manufacturers don't reveal the inner content of their dies.

Wire Bonding

Introduction

Wire bonding is the process of connecting a die pin to another die pin or to the substrate with a thin metal wire. The metal is typically very pure gold and is often referred to as 4N wire. Diameters can vary between 15 um and 250 um. The wire is welded to the chip pin and to the substrate pin. There are different technologies used to create the weld, or bond as it is called.

In *Thermo Compression Bonding*, the surface is heated to 300 degrees C or more. The wire is then pressed to the surface at high pressure, up to 10,000 lbs/sq in. Expressed over the surface of a bond wire, this means about 25 grams or close to an ounce of force per wire bond. Thermo compression is typically only used for wedge bonding described below.

In *Ultrasonic bonding*, the wire and the chip are rubbed against each other causing the roughness of the metal surfaces to be ground flat which causes a bond between the atoms. The rubbing energy is created using ultrasonic vibrations. Ultrasonic bonding can be done at room temperature.

Thermosonic bonding is a very common method. Both thermal energy and ultrasonic energy are used to form the bond. Pre-heating is at around 150 degrees C. The surfaces to be bonded must be clean and free from contamination. Several processes exist to clean the surface to be bonded.

The wire bonding pitch can be very narrow and since the

capabilities are changing rapidly, we will not discuss what is considered mainstream or leading edge today. The actual production volume of practical pitch has been, and is still, closely following the ITRS pitch requirement roadmap. Around 35 um pitch is considered possible today.

The tool on the wire bonder machine that moves the wire and creates the bond is called a *capillary*. There are many shapes and sizes available in order to fit every possible bond job. During substrate design, it is vital to keep in mind the movements of the capillary and its size to avoid interference with surrounding objects. A wire bond takes about 200-600 milliseconds and costs around \$0.01 per wire

Ball Bond

There are several types of bonds named after their main characteristic. A ball bond is started by melting the tip of the bond wire so that a tiny drop or ball is formed. The ball is then bonded to the chip or the substrate (Figure 14). The ball

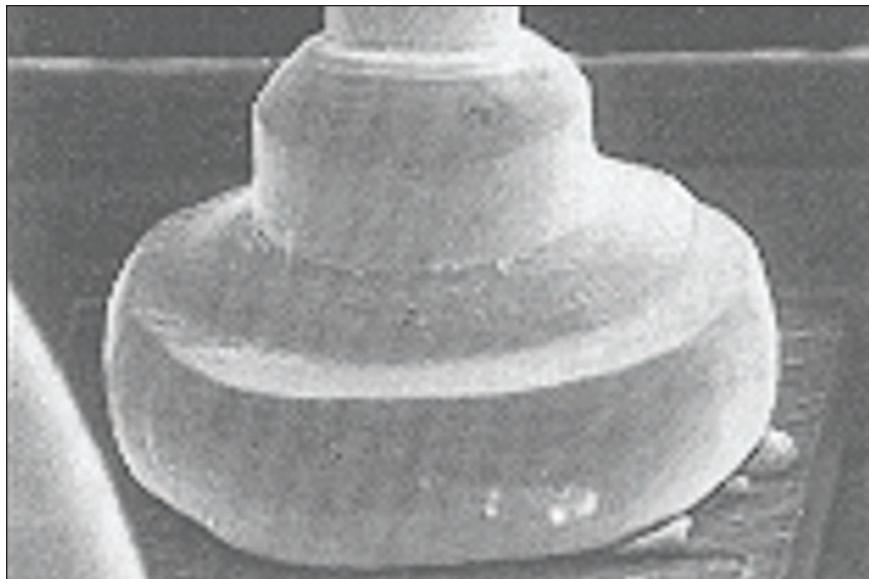


FIGURE 14: Detail of a typical ball bond[2]

formed is usually made by ionizing the gap between a high tension electrode and the wire tip causing an electric arc which melts the wire. This is called Free Air Ball (FAB).

The opposite end is always wedge bonded. Therefore, the typical bond starts with a ball bond and ends with a wedge bond, which is called a ball-wedge bond.

Wedge Bond

In wedge bonding there is no ball-forming. A special capillary tool is used to form a wedge-like bond (Figure 15) that typically has a lower loop profile than the ball bond. It is possible to have a wedge in both the starting point and the end point. This is called a wedge-wedge bond.

Ribbon Bond

For high power and RF, it is possible to bond with a tape shaped wire called a ribbon or strip bond. Its advantages are higher current carrying capacity, lower inductance, and exceptionally low loop height.

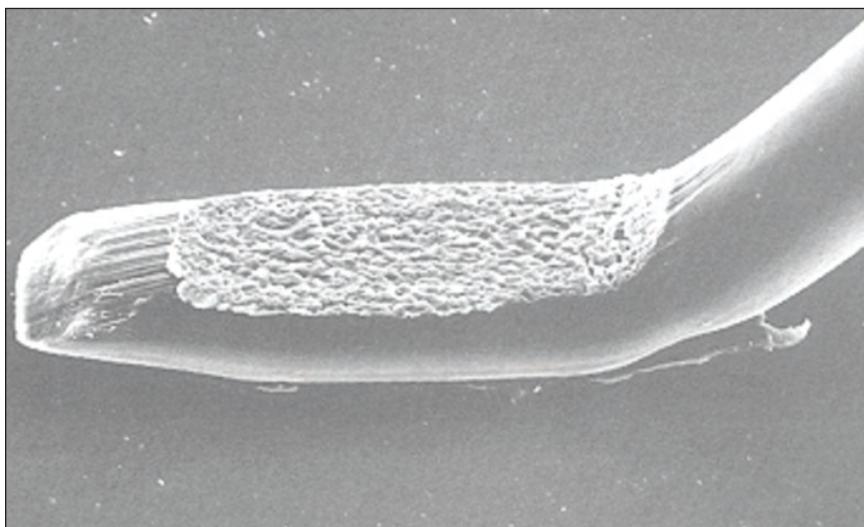


FIGURE 15: Detail of a wedge bond[2]

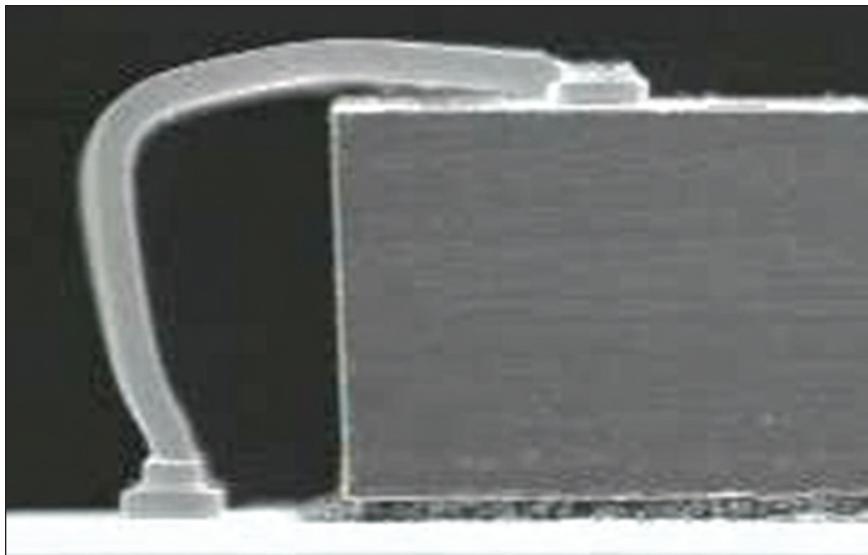


FIGURE 16: A reverse (or loop back) stand off bonding has ultra low height over the chip. The stand off gives enough added height for the wire to clear just the chip edge.[3]

Stand Off Bonding

Stand off technology is the process of raising the bond location in order to have an extremely low profile bond loop. There is some confusion about what stitch bonding is. Some equate it with stand off bonding while others think that it is a multihop bonding. Stitch bonding starts in one point and sequentially visits more than one target point without cutting the wire in between. Our focus will be on stand off bonding.

A stand off bond is chosen for its extremely low profile bond loop. The process is started by first adding a wedge or a ball bond to the pin, then cutting the wire and starting a new bond at the opposite end, and finishing the bond on top of the first created wedge or ball. This results in a bond loop that can pass a chip edge with very little clearance to yield a low total height. The cost is in the additional time it takes to create the stand off before the actual bonding.

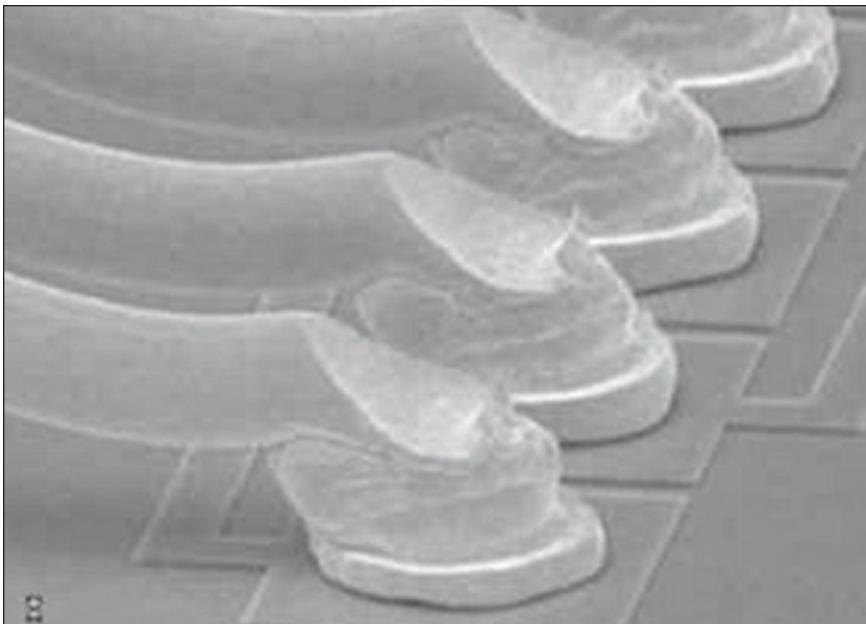


FIGURE 17: Detail of a ball stand off showing how the ball stand off makes the wedge bond start higher up[3]

Chip to Chip Bonding

If a connection is to be made from one die to another, we can wire bond down to the substrate and then route on the substrate between the bond pads or we can put a wire bond directly between the two dies.

A short wire directly between the two dies has superior electrical performance and saves substrate real estate, so this is the preferred configuration. The design tool needs to recognize the direct chip-to-chip connectivity and must be able to validate signal integrity. Analysis tools for signal and power integrity must support extraction of this type of interconnect. There is nothing to prevent you from attaching more than one wire to the same pin on the die and/or on the substrate, as long as there is space enough to reach the bond position with the capillary.

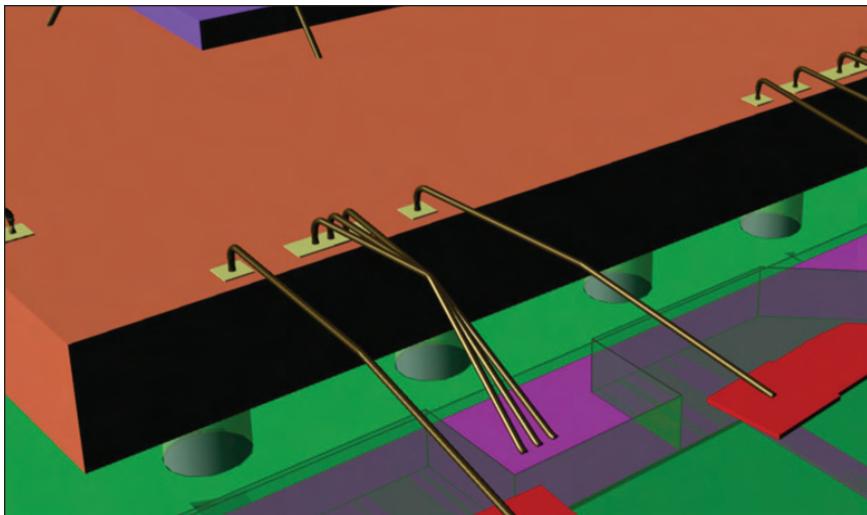


FIGURE 18: Crossing the wires during multi-wire bonding gives increased mechanical strength.

Multi-Wire Bonding

Some interconnects to a die might need a higher current capacity than what you can provide using a single wire. It is expensive manufacturing-wise to wire bond isolated pins using different wire diameters because it entails an extra process step. The alternative is to add multiple wires in parallel positions between the same die pin and the same bond pad. This is common for power and ground connections.

Another benefit of multi-wire bonding is that parallel wires means less total inductance (three parallel inductors equal one-third the inductance of a single inductor of the same value), which is desirable for ground and power connections.

Bonding of Special Components

Wire bonding is not only used to connect a chip die pin to the substrate pin. It can be used for many purposes. If a design is to be wire bonded, the extra cost of adding a few more wire bonds is very low and we can make use of that fact. Rather

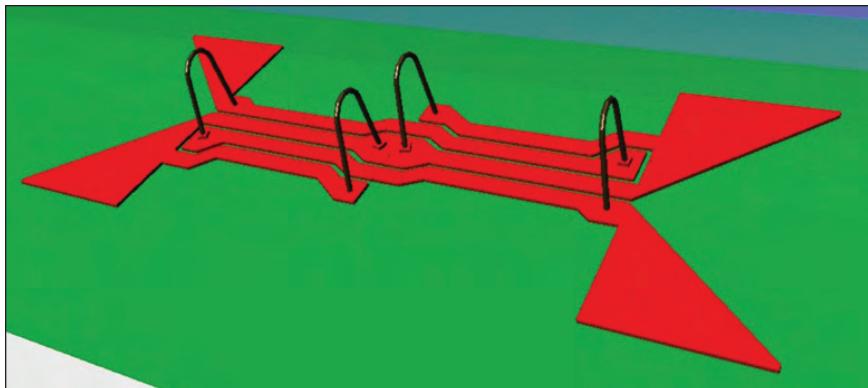


FIGURE 19: 3-D image of a microwave “Lange coupler” with wire bonded stubs

than inserting a via hole, a wire bond jumper can be used when a signal needs to jump over another signal trace.

Test Bridge

Sometimes a circuit is designed so that by breaking or inserting a jumper, the circuit can be put in a specific test mode. A wire bond can be used as that jumper.

Configuration Jumper

As for the test bridge, a wire bond can be used as a configuration jumper, configuring the circuit by inserting one or several wire bond jumpers.

RF Shape Bonding

Some planar RF shapes need to have their stubs tied together. Rather than using vias and bridging the stubs on a separate layer, wire bonds can be used.

I/O cell placement considerations

I/O cells are placed where they are close to the chip core function they serve. There are several other requirements

to keep in mind, many of which are mechanical and driven by wire bond yield. Although the cells should be placed in a specific order, we typically have to change the cell spacing as we get closer to the die edge. Assuming we can wire bond at 50 um die pin pitch, we will typically find that for the last 10 to 20 I/O cells, we have to gradually increase the spacing to maintain the yield. The reason is that the closer to the end we come, the larger the angle between the bond wire and chip will become and eventually the angle is so large that the wires overlap the next die pin making it impossible to wire bond (Figure 20). Increasing the spacing helps minimize the issue.

Exactly how to increase the pitch, whether step-by-step in a few steps or as a seamless gradient increase, and by what amount is almost like religion, with each person steadfast in his beliefs. Typically, corporations have developed proprietary rules based on trial and error.

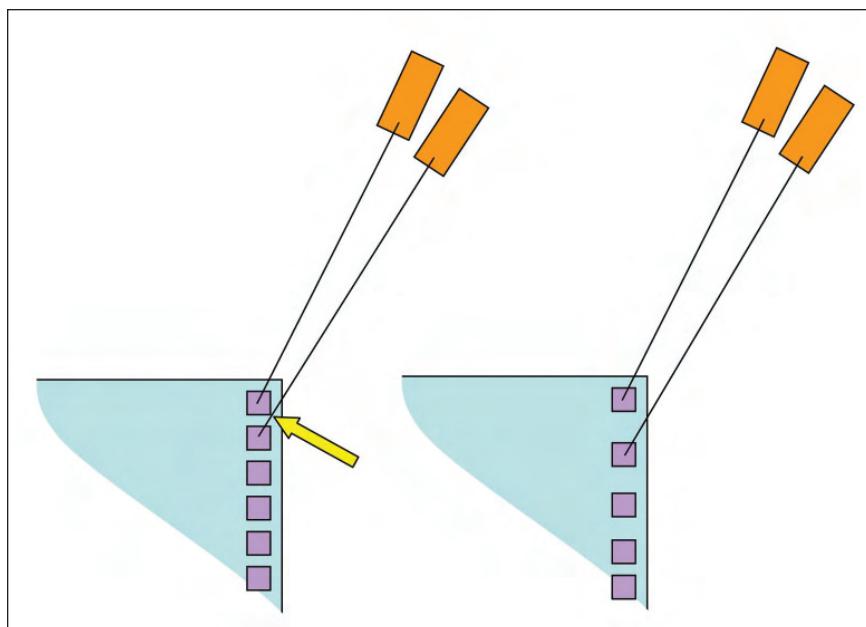


FIGURE 20: With constant I/O cell pitch, we may see yield issues that are easily overcome by gradually extending the I/O cell pitch at the corners of the die.

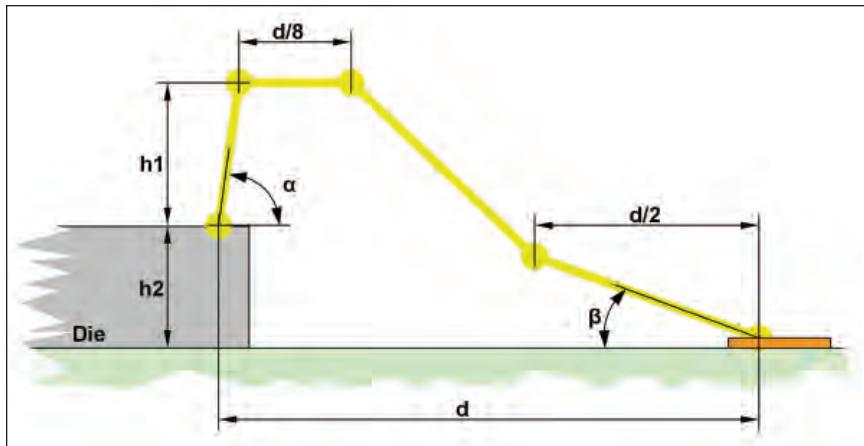


FIGURE 21: Jedec JESD59 five-point model

3-D Wire Loop Considerations

The design of the wire loop profile can be anything from a simple Jedec 4 point loop to a highly complex custom loop bending in all 3-D planes. There is a JEDEC/EIA standard on wire bond loop profiles: EIA/JESD59 which uses a 2-dimensional four or five point approximation (Figure 21). This model is still the most common in design and analysis tools, but we need to consider that the standard is more than

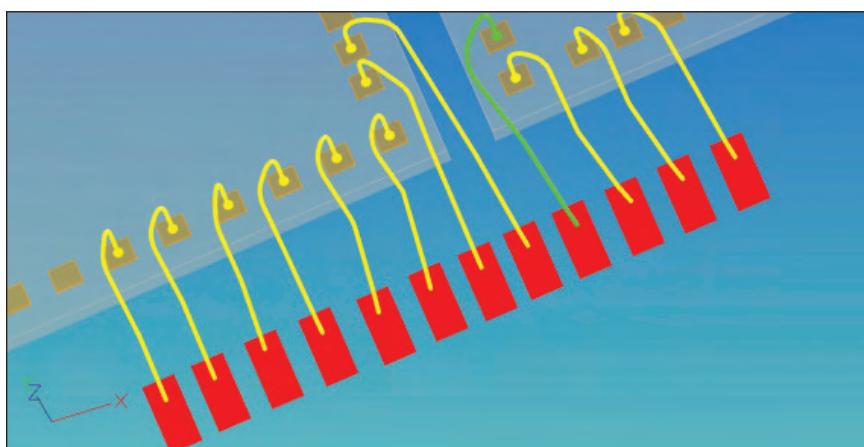


FIGURE 22: With a model that can bend in the 3-D planes, density can be significantly increased.

ten years old and the requirements of today are very poorly supported.

Rather than a 2-D side projection loop with a fixed number of points, the industry needs a model that supports bending in all three 3-D planes (top, side, and end projection) leading to a fully flexible n-point model where the distance between any points can be a straight line, an arc, or a spline. A good example is seen in Figure 22, where a wire is bent in 3-D space to increase density. This means bending the wire not only in the side view projection but also from the top view projection and end view projection. This is something the JESD59 and other side projection models cannot support.

Flip-Chip

Introduction

Flip-chip is not a new technique. IBM patented its C4 process in the early 1960s. The SLT modules used in its System 360 mainframes used C4 technology. Thermally and electrically, flip-chip technology is excellent, but for various reasons, wire bonding is still a very common bonding technology. The main drivers for flip-chip today are high pin count devices in combination with ultra-high-speed digital technology.

Flip-chip Bonding

The attachment of the flip-chip to the substrate is called Flip-Chip Bonding. There are several methods in use. One method is similar to the reflow soldering of a BGA circuit. A tin alloy paste is applied and melted using IR heat. As the tin melts, its surface tension will help center the die bumps to the substrate pads.

Another interesting technology which is gaining popularity is to use Anisotropic Conductive Bonding, or Anisotropic Conductive Film (ACF), which is an epoxy-based film that only conducts current in Z-axis. The film can be applied over the surface without making contact between the bumps, but still provide Z-axis connection from die bump to substrate pads.

Flip-Chip vs. Wire Bond Selection

Wire bonding is still the most common connection method. It is cheap, fast, and well-known, but when the number of input/output/power/ground pins becomes large enough, it will not be possible to place the I/O cells in a ring around the chip core. Another driver is signal performance. A bond wire does have some parasitic elements, as does the flip-chip interconnect, but the latter are much smaller and therefore capable of sustaining a faster digital throughput. Consequently, flip-chip bonding is used when the signal performance requirements are in the extreme or when the number of I/Os and power/ground connections are very high. The exact number depends on several factors. The size of the I/O cell is one major factor.

Let's look at an example. A sample TSMC 0.13 um I/O library has the cell size of 35 x 246 um. If we assume a single row of I/O cells, 1,000 cells will form an available core area of 8.7 x 8.7 mm and a total die size of 9.2 mm. Assuming dual rings of I/O cells, the core area becomes 4.4 x 4.4 mm and the die area 5.4 x 5.4 mm. It now becomes a matter of deciding if a core area of 4.4 mm will suffice for this design or if a die area of 9.2 x 9.2 becomes a costly waste. The alternative would be to use flip-chip I/Os distributed over the chip core surface. A chip-package-board co-design tool with virtual prototyping capabilities will help you do these calculations and trade-offs.

Bump Matrix, Routability, and RDL Routing

Each power/ground location from the chip core and each I/O interface of the chip core needs to be connected to the flip-chip bumps. In case of signals, an I/O buffer cell is required. The bumps are typically placed in a regular or a staggered matrix pattern. Sometimes they are fully populated, but often individual bumps are left out and sometimes channels of bumps are left out. The pattern does not have to be regular. If, for some reason, it is desired to have a specific custom pattern, then that is possible.

The power/ground connection can be made as one of two main types. Place the bumps aligned with the chip power/ground grid and metallize the bump directly to the power grid, or route from the chip core to the bump.

Signals are always routed. The I/O buffer cells can be of different configurations. The simplest case is when I/O cells are placed around the perimeter of the chip core like wire bonding. However, with flip-chip we have the option to use area array I/O, meaning that the I/O cells are places in the chip core close to the core function they serve. In both cases, a metal route has to be made from the chip core function to the I/O cell and another metal connection from the I/O cell to the flip-chip bump for that signal. It is better in terms of signal performance to use area array I/O as the connection from I/O cell to chip. We call these routes Redistribution Layer Routing (RDL). RDL is an additional metal layer on the chip, so chip design rules apply. RDL routing can be done by the chip design tool or the package design tool. Both environments typically have the required tool support to perform the RDL routing. Some are using chip design tools and some are using package design tools to create the RDL routing, which then needs to go to chip manufacturing.

RDL routing is typically a single layer route. It is possible to place the I/O cells and place the bump positions so that the RDL routing cannot be completed within the design rules. It is therefore a task within chip-package co-design to place the I/O cells so that 100% routability can be guaranteed.

BGA Substrate Routing

Introduction

It is hard to give a general description of package routing. There are many substrate technologies such as classic laminated, sequential buildup, thin-film buildup, silicon core BCB dielectric buildup, etc. They are all different in ways that impact the interconnect strategy, mostly due to different via hole formation capabilities. Still, many considerations and techniques are the same for all substrate technologies.

For general signal routing, we differ between single chip-packages and multichip-packages. SiP and other multichip-packages can be viewed as small, but typically very dense. PCBs. Serious package engineers don't like the fact that a powerful PCB auto router will make excellent results on this type of design and a more interactive approach will use the exact same strategies as for a dense PCB, identifying signal paths and route without a specific layer direction bias.

The success rate is heavily dependant on the break-out/break-in routing described below and how well the chip-package has been co-designed. Clearly, if all signals are on the wrong side of the die or if differential pair of signals have not been kept together, it will become difficult to route to specifications at the package level.

Single chip-packages are different. Here, a typically large,

high pin count chip is centered in the package and all signals escape radially out from the chip area to a blind/buried via structure reaching down to the appropriate BGA pin.

Package “Break-In” Routing

When a large BGA is placed on a PCB, the designer needs to do a break-out operation to provide for all signals to escape the BGA area with as few layers as possible in a way that makes sense with respect to power and signal integrity. In packaging, the problem is exactly reversed, hence the challenge of break-in routing.

For a single chip-package, the challenge is to escape all chip connections and eventually connect to the package pins.

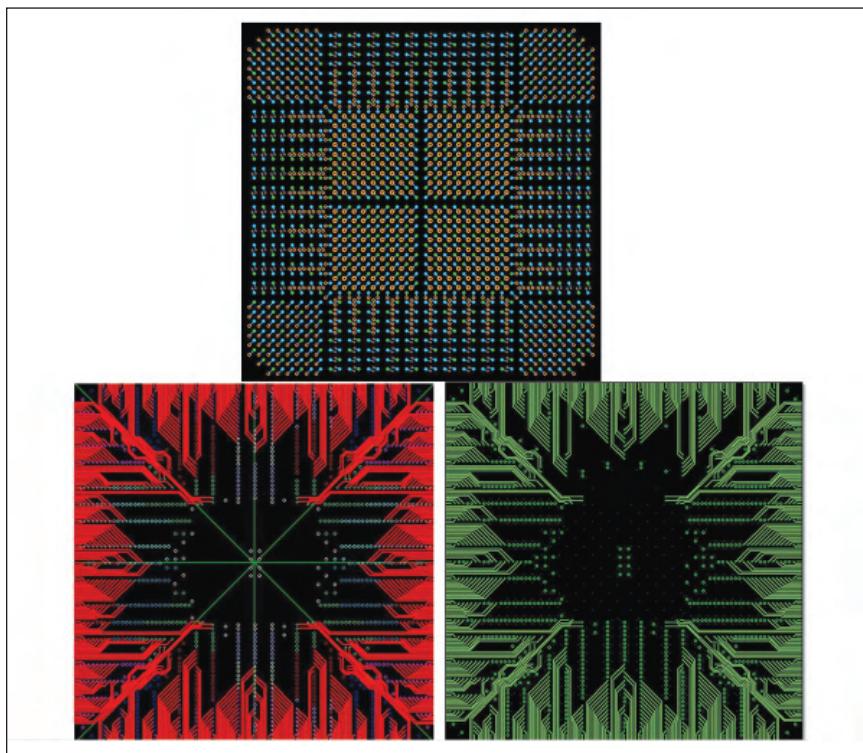


FIGURE 23: Break-out routing of high pin count pin matrix created in Mentor Graphics' Expedition tool

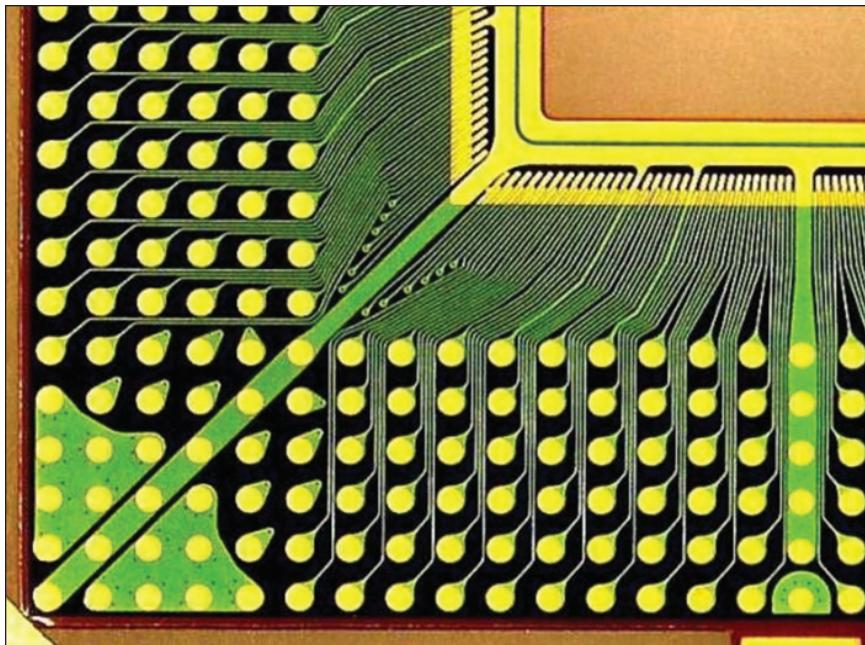


FIGURE 24: Break-out routing of wire-bonded die

Whether the chip is wire bonded or flip-chip or the package is BGA or another type, the basic objective is the same.

A flip-chip is, in this respect, a tiny BGA and to escape, sufficiently narrow trace widths and small micro vias have to be used. This is identical to BGA break-out routing in a PCB (Figure 23), just with smaller dimensions. Just as for PCB, differential pairs and bus signals have to be kept together and power/ground needs special attention. Routing the entire package with this narrow trace width will have yield and cost implications, so typically, once the die is escaped, the trace widths and gaps are increased.

When a die is wire bonded, the bond pads are typically placed in a manner that optimizes wire bonding yield assuming the routing is a less difficult issue. This leads to radial fan-out routing which has to be applied to escape the dense bond pad pattern (Figure 24).

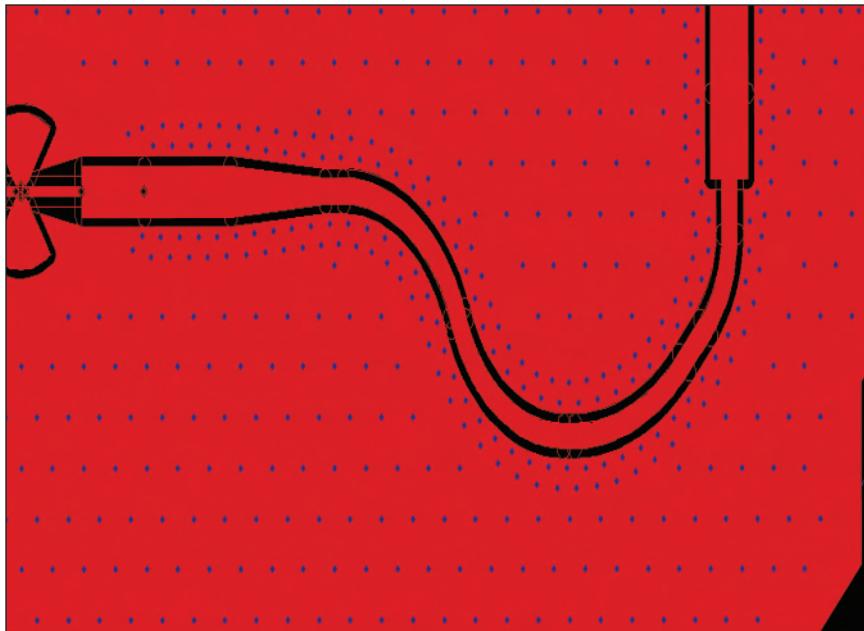
Advanced Packaging and System-in-Packages

Upon closer inspection of a dense multi-die package, one will see that each die poses a different break-out or break-in challenge. A strategy has to be decided upon for each die considering the interconnects between the dies. Once the break-out and fan-out have been applied this type of package is routed as described above.

This chapter provides a detailed overview of Advanced Packaging and System-in-Packages. For more information and details on the principles and solutions, I would recommend reading *BGA Breakouts and Routing: Effective Design Methods for Very Large BGAs* by Charles Pfeil. Many of the same principles mentioned in this book on PCB design apply to package design.

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Basic%20Info.htm](http://nepp.nasa.gov/wirebond/Basic%20Info.htm)
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