```
.ORIG x2000
-------------------------------------
Instruction Count : 0
PC                : 0x2000
CCs: N = 0  Z = 1  P = 0
Registers:
0: 0x0000
1: 0x0000
2: 0x0000
3: 0x0000
4: 0x0000
5: 0x0000
6: 0x0000
7: 0x0000


AND R0,R0,x0
-------------------------------------
Instruction Count : 1
PC                : 0x2001
CCs: N = 0  Z = 1  P = 0
Registers:
0: 0x0000
1: 0x0000
2: 0x0000
3: 0x0000
4: 0x0000
5: 0x0000
6: 0x0000
7: 0x0000


AND R1,R1,x0
-------------------------------------
Instruction Count : 2
PC                : 0x2002
CCs: N = 0  Z = 1  P = 0
Registers:
0: 0x0000
1: 0x0000
2: 0x0000
3: 0x0000
4: 0x0000
5: 0x0000
6: 0x0000
7: 0x0000


ADD R0,R0,x-7
-------------------------------------
Instruction Count : 3
PC                : 0x2003
CCs: N = 1  Z = 0  P = 0
Registers:
```

```
0: 0xfff9
1: 0x0000
2: 0x0000
3: 0x0000
4: 0x0000
5: 0x0000
6: 0x0000
7: 0x0000


ADD R1,R1,x4
-------------------------------------
Instruction Count : 4
PC                : 0x2004
CCs: N = 0  Z = 0  P = 1
Registers:
0: 0xfff9
1: 0x0004
2: 0x0000
3: 0x0000
4: 0x0000
5: 0x0000
6: 0x0000
7: 0x0000


LOOP ADD R0,R1,R0
-------------------------------------
Instruction Count : 5
PC                : 0x2005
CCs: N = 1  Z = 0  P = 0
Registers:
0: 0xfffd
1: 0x0004
2: 0x0000
3: 0x0000
4: 0x0000
5: 0x0000
6: 0x0000
7: 0x0000


BRn LOOP
-------------------------------------
Instruction Count : 6
PC                : 0x2004
CCs: N = 1  Z = 0  P = 0
Registers:
0: 0xfffd
1: 0x0004
2: 0x0000
3: 0x0000
4: 0x0000
5: 0x0000
```

```
6: 0x0000
7: 0x0000


LOOP ADD R0,R1,R0
-------------------------------------
Instruction Count : 7
PC                : 0x2005
CCs: N = 0  Z = 0  P = 1
Registers:
0: 0x0001
1: 0x0004
2: 0x0000
3: 0x0000
4: 0x0000
5: 0x0000
6: 0x0000
7: 0x0000


BRn LOOP
-------------------------------------
Instruction Count : 8
PC                : 0x2006
CCs: N = 0  Z = 0  P = 1
Registers:
0: 0x0001
1: 0x0004
2: 0x0000
3: 0x0000
4: 0x0000
5: 0x0000
6: 0x0000
7: 0x0000


AND R1,R1,R0
-------------------------------------
Instruction Count : 9
PC                : 0x2007
CCs: N = 0  Z = 1  P = 0
Registers:
0: 0x0001
1: 0x0000
2: 0x0000
3: 0x0000
4: 0x0000
5: 0x0000
6: 0x0000
7: 0x0000


NOT R1,R1
-------------------------------------
```

```
Instruction Count : 10
PC                : 0x2008
CCs: N = 1  Z = 0  P = 0
Registers:
0: 0x0001
1: 0xffff
2: 0x0000
3: 0x0000
4: 0x0000
5: 0x0000
6: 0x0000
7: 0x0000


LEA R3,x20
-----------------------------------
Instruction Count : 11
PC                : 0x2009
CCs: N = 1  Z = 0  P = 0
Registers:
0: 0x0001
1: 0xffff
2: 0x0000
3: 0x2029
4: 0x0000
5: 0x0000
6: 0x0000
7: 0x0000


LEA R4,x20
-----------------------------------
Instruction Count : 12
PC                : 0x200a
CCs: N = 1  Z = 0  P = 0
Registers:
0: 0x0001
1: 0xffff
2: 0x0000
3: 0x2029
4: 0x202a
5: 0x0000
6: 0x0000
7: 0x0000


ST R3,x-4
Memory content [0x2000..0x2020] :
-----------------------------------
 0x2000 (8192) : 0x5020
 0x2001 (8193) : 0x5260
 0x2002 (8194) : 0x1039
 0x2003 (8195) : 0x1264
 0x2004 (8196) : 0x1040
```

```
 0x2005 (8197) : 0x9fe
 0x2006 (8198) : 0x5240
 0x2007 (8199) : 0x2029
 0x2008 (8200) : 0xe620
 0x2009 (8201) : 0xe820
 0x200a (8202) : 0x37fc
 0x200b (8203) : 0xb9fb
 0x200c (8204) : 0xabfa
 0x200d (8205) : 0x2df9
 0x200e (8206) : 0x6180
 0x200f (8207) : 0x7141
 0x2010 (8208) : 0x5260
 0x2011 (8209) : 0xe402
 0x2012 (8210) : 0x4080
 0x2013 (8211) : 0xf025
 0x2014 (8212) : 0x1267
 0x2015 (8213) : 0xc1c0
 0x2016 (8214) : 0x00
 0x2017 (8215) : 0x00
 0x2018 (8216) : 0x00
 0x2019 (8217) : 0x00
 0x201a (8218) : 0x00
 0x201b (8219) : 0x00
 0x201c (8220) : 0x00
 0x201d (8221) : 0x00
 0x201e (8222) : 0x00
 0x201f (8223) : 0x00
 0x2020 (8224) : 0x00


STI R4,x-5
-----------------------------------
 0x2028 (8232) : 0x00
 0x2029 (8233) : 0x202a
 0x202a (8234) : 0x00
 0x202b (8235) : 0x00
 0x202c (8236) : 0x00


LDI R5,x-6
-----------------------------------
Instruction Count : 15
PC                : 0x200d
CCs: N = 0  Z = 0  P = 1
Registers:
0: 0x0001
1: 0xffff
2: 0x0000
3: 0x2029
4: 0x202a
5: 0x202a
6: 0x0000
7: 0x0000
```

```
LD R6,x-7
-------------------------------------
Instruction Count : 16
PC                : 0x200e
CCs: N = 0  Z = 0  P = 1
Registers:
0: 0x0001
1: 0xffff
2: 0x0000
3: 0x2029
4: 0x202a
5: 0x202a
6: 0x2029
7: 0x0000


LDR R0,R6,x0
-------------------------------------
Instruction Count : 17
PC                : 0x200f
CCs: N = 0  Z = 0  P = 1
Registers:
0: 0x202a
1: 0xffff
2: 0x0000
3: 0x2029
4: 0x202a
5: 0x202a
6: 0x2029
7: 0x0000


STR R0,R5,x1
-------------------------------------
 0x2028 (8232) : 0x00
 0x2029 (8233) : 0x202a
 0x202a (8234) : 0x00
 0x202b (8235) : 0x202a
 0x202c (8236) : 0x00


AND R1,R1,x0
-------------------------------------
Instruction Count : 19
PC                : 0x2011
CCs: N = 0  Z = 1  P = 0
Registers:
0: 0x202a
1: 0x0000
2: 0x0000
3: 0x2029
4: 0x202a
5: 0x202a
```

```
6: 0x2029
7: 0x0000


LEA R2,x2
-------------------------------------
Instruction Count : 20
PC                : 0x2012
CCs: N = 0  Z = 1  P = 0
Registers:
0: 0x202a
1: 0x0000
2: 0x2014
3: 0x2029
4: 0x202a
5: 0x202a
6: 0x2029
7: 0x0000


JSRR R2
-------------------------------------
Instruction Count : 21
PC                : 0x2014
CCs: N = 0  Z = 1  P = 0
Registers:
0: 0x202a
1: 0x0000
2: 0x2014
3: 0x2029
4: 0x202a
5: 0x202a
6: 0x2029
7: 0x2013


ADD R1,R1,x7
-------------------------------------
Instruction Count : 22
PC                : 0x2015
CCs: N = 0  Z = 0  P = 1
Registers:
0: 0x202a
1: 0x0007
2: 0x2014
3: 0x2029
4: 0x202a
5: 0x202a
6: 0x2029
7: 0x2013


RET
-------------------------------------
```

```
Instruction Count : 23
PC                : 0x2013
CCs: N = 0  Z = 0  P = 1
Registers:
0: 0x202a
1: 0x0007
2: 0x2014
3: 0x2029
4: 0x202a
5: 0x202a
6: 0x2029
7: 0x2013


HALT
------------------------------------
Instruction Count : 24
PC                : 0x0000
CCs: N = 0  Z = 0  P = 1
Registers:
0: 0x202a
1: 0x0007
2: 0x2014
3: 0x2029
4: 0x202a
5: 0x202a
6: 0x2029
7: 0x2013
```