EW-2 Project-1
Audio Amplifier (Table No. 24)

Snehil Sanjog
2023102051
snehil.sanjog@students.iiit.ac.in

Vedant Tejas
2023112018
vedant.tejas@research.iiit.ac.in

***Abstract*—The aim of the project is to build an audio amplifier with the following specifications:**

- **Supply Voltage = -5 to 5 V**
- **Input small signal voltage = 10-20 mV peak-to-peak**
- **Gain = $G_1 \times G_2 \geq 500$ (Pre-amp and Gain stage)**
- **Frequency = Audible Range (20 Hz to 20 kHz)**
- **Power $\geq$ 1.5 W**
- **Filter should not attenuate the input signal**
- **Power Amplifier should not provide voltage gain**
- **Load = 10 Ω**

This document presents a detailed study and implementation of an Audio Amplifier. The project involves designing, simulating, and testing an amplifier circuit for enhanced audio signal amplification. Key parameters such as gain, efficiency, and distortion are analyzed.

I. Introduction

Audio amplifiers play a vital role in various applications, including sound systems, musical instruments, and broadcasting. This project aims to design an efficient and cost-effective amplifier while ensuring reliable performance.

II. Stages of the Audio Amplifier

A. Pre-Amplifier Stage

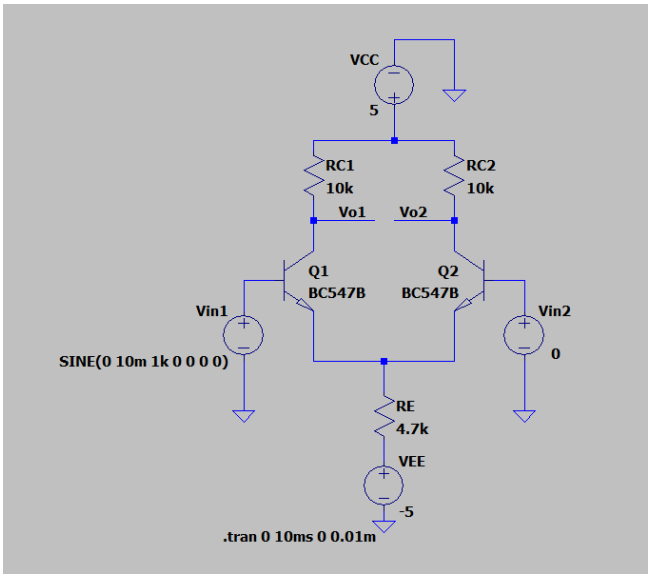

Fig. 1: Basic Pre-Amplifier LTSpice

1) Functionality: The pre-amplifier stage is designed to provide initial signal amplification while improving the signal-to-noise ratio (SNR). A high Common Mode Rejection Ratio (CMRR) is desirable for minimizing noise.

To prevent excessive current draw from the microphone, the input impedance should be sufficiently high. The common-emitter differential amplifier is an ideal choice due to its high input impedance, low output impedance, and effective noise performance.

2) AC Analysis: From AC analysis, we found that

$$\frac{V_o}{V_{in}} \propto \frac{R_C}{R_E}$$

$$\text{gain} = k \times \frac{R_C}{R_E}$$

By keeping $R_C = R_E$, we get $k \approx 18$. So for $R_C = 2R_E$, hence:

$$\text{gain} = 36$$

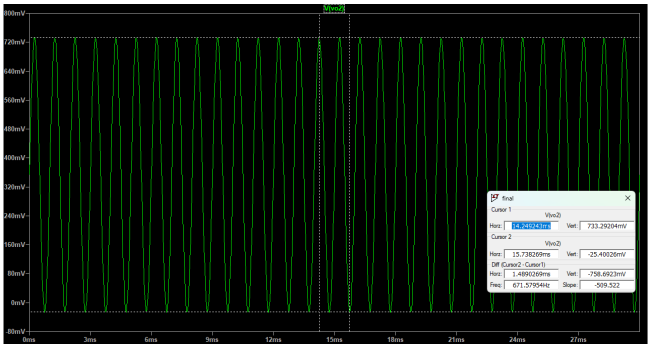

Fig. 2: Simulated Plot from LTSpice

3) Result Plots and Verification: From the simulation results:

- **Collector current**: $I_C \approx 0.457mA$.
- **Transconductance**: $g_m = \frac{I_C}{V_T} \approx 0.01764$ S.
- **Output amplitude** (green trace): $\approx 733.292mV_{pp}$.
- **Amplitude gain**: $A_v = \frac{733.29204 \text{ mV}}{20 \text{ mV}} \approx 36.664$.

The common mode output was obtained when an 20mV peak-to-peak input was given.

$$\text{Common Mode Gain} = \frac{2.936mV}{20mV} = 0.147$$

Thus, we can calculate the CMRR from the known equation:

$$\text{CMRR} = 20\log\left(\frac{A_d}{A_c}\right) = 20\log\left(\frac{36.664}{0.147}\right) = 47.93$$

We get **Experimental gain**: $A_v = \frac{810mV}{20mV} \approx 40.5$.

a) Comparison: Table V presents a comparison of theoretical, simulation, and hardware values.

TABLE I: Comparison of Theoretical, Simulation, and Hardware Values

Parameter	Theoretical Value	Simulation Value	Hardware Value
Gain (A_v)	36	36.664	40.5
I_C	0.450mA	0.457mA	0.460mA

The results show that the theoretical, simulation, and hardware values are in close agreement, confirming the validity of our design.

B. Gain Stage

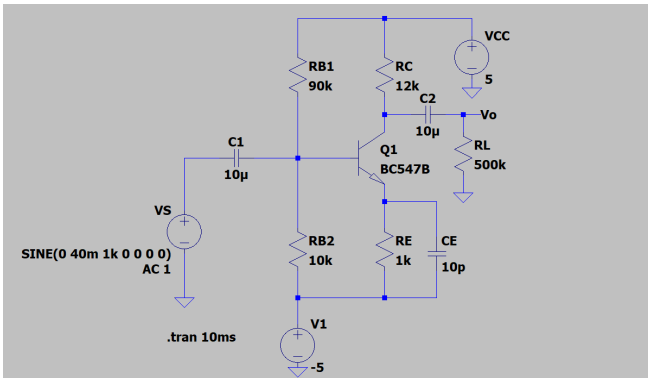

Fig. 3: Circuit Diagram for Common Emitter Amplifier

1) Working: The Common-Emitter (CE) amplifier we have used in this stage has a high input impedance and provides high voltage and current gain. The input capacitor C_1 blocks the DC components of the input signal while allowing AC signals to pass and also introduces a low-frequency pole in the system. The capacitor C_2 blocks DC current from flowing to ground and serves as an AC coupling capacitor to the filtering stage. Bias resistors R_{B1} and R_{B2} form a voltage divider with respect to V_{CC} to properly bias the transistor (Base-Emitter junction in forward bias and Base-Collector junction in reverse bias). To independently control AC gain and DC bias, we use the resistors R_{E2} and R_{E1}, where the latter is AC short circuited by a bypass capacitor.

2) DC Analysis: We use the following equations for DC analysis:

$$V_B = \frac{R_{B2}V_{CC}}{(R_{B1}+R_{B2})}$$

$$I_E = \frac{(V_B - V_{BE}) + V_{CC}}{R_{E1}+R_{E2}}$$

$$I_C = \frac{\beta}{\beta+1} I_E \approx I_E$$

$$V_{out} = V_{CC} - I_C R_C$$

We can stop here to analyse the working of the gain stage. The output voltage is at the collector, thus, the collector voltage will swing by the amplitude of the amplified signal. We always want the npn-BJT to operate in **active** mode, where the base-collector junction is reverse biased, and base-emitter junction is forward biased.

Assuming a swing of ± 4 Volts at the collector, we chose to give a DC bias of 0.5V at the collector and -3.2V at the base. Thus, we obtain the ratio:

$$\frac{R_{B1}}{R_{B2}} \approx 9$$

3) AC analysis: The small signal diagram is given below:

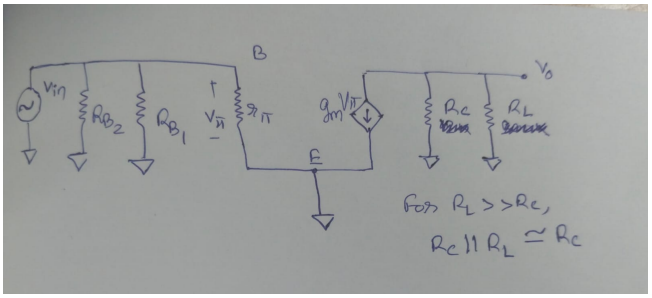

Fig. 4: Gain Stage Small signal model

The capacitors are shorted and DC sources are grounded.

$$V_\pi = V_{in}$$

$$V_{out} = -g_m v_\pi (R_C || R_L) \approx -g_m v_\pi R_C = -g_m v_{in} R_C$$

$$\text{gain} = \frac{V_{out}}{V_{in}} = -g_m R_C$$

4) Component Selection: We can summarise the calculated constraints so far as follows:

- R_{B1} and R_{B2} are set such that we get proper swings at V_{out}
- Output impedance R_C must be low (Impedance matching)
- R_E must remain relatively small to ensure high enough gain can be attained.

It is possible to take the liberty to allow R_C to be large in view of the high input impedance of the filter stage, but we decided to use intermediate values to optimize all parameters.

a) Emitter Current: Using the base-emitter voltage drop $V_{BE} \approx 0.7V$, we can approximate the emitter voltage:

$$V_E = V_B - V_{BE} = -4V - 0.7V = -4.7V$$

Applying Ohm's law to find emitter current:

$$I_E = \frac{V_E + V_{CC}}{R_E}$$

We chose to set the emitter resistance as $R_E = 1k\Omega$

$$I_E = \frac{377mV}{1k} = 377\mu A$$

b) Biasing Resistors: The base voltage is equal to:

$$V_B = V_{CC}\left(\frac{R_{B2} - R_{B1}}{R_{B1} + R_{B2}}\right)$$

The ratio R_{B1}/R_{B2} must equal 9. We chose

$$R_{B1} = 90k\Omega, \quad R_{B2} = 10k\Omega, \quad V_{CC} = 5V$$

$$V_B = 5\left(\frac{10000 - 90000}{10000 + 90000}\right) \approx -3.2V$$

$R_{B1}||R_{B2} = 9k\Omega$, so we satisfy

c) Collector Current: Since $I_C \approx I_E$ (assuming β is large):

$$I_C = 377\mu A$$

d) Transconductance:

$$g_m = \frac{I_C}{V_T}, \quad V_T \approx 26mV$$

$$g_m = \frac{377\mu A}{26mV} = 0.0145$$

e) Gain Calculation: From the gain equation:

$$\text{gain} = -g_m R_C \approx 11.2$$

f) Input coupling capacitor: The coupling capacitor blocks the input DC offset, but also create a CR high pass filter with the biasing resistors, with cutoff frequency:

$$f_{cutoff} = \frac{1}{2\pi RC}$$

The higher cutoff frequency will come from the smaller resistance, so plugging in $C_1 = 10\mu F$ and $R = 10k\Omega$:

$$f_{cutoff} = \frac{1}{2\pi \times 10 \times 10^3 \times 100 \times 10^{-6}} = 1.59Hz$$

The high pass filter will not attenuate any of the frequencies in the 20Hz - 20kHz range.

g) Final Component Values:

- $R_{B1} = 90k\Omega$
- $R_{B2} = 10k\Omega$
- $R_C = 12k\Omega$
- $R_E = 1k\Omega$
- $C_1 = 100\mu F$
- $C_2 = 10pF$

5) Result Plots and Verification: To validate our design, we performed SPICE simulations and hardware testing. The results are presented below.

a) SPICE Simulation: The LTSpice simulation output for the Gain Stage circuit is shown in Figure 5

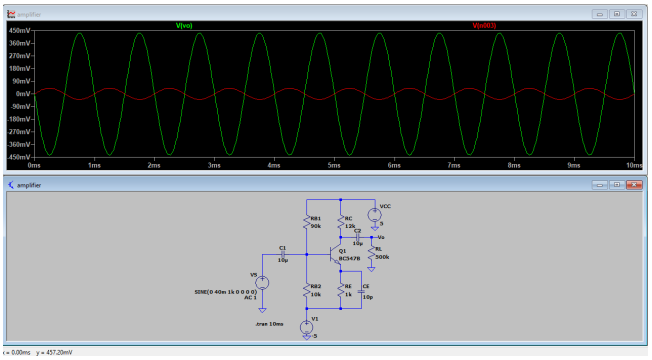

Fig. 5: Gain stage Circuit Simulation Output

From the simulation results for input 80mV peak to peak at 1kHz for the first two stages:

- **Output amplitude** : $\approx 900mV_{pp}$.
- **Voltage gain**: $A_v = \frac{900 \text{ mV}}{80 \text{ mV}} \approx 11.25$.

b) Hardware Output: From hardware, we get approx gain of 11 which is very close to our simulated gain.

c) Comparison: Table V presents a comparison of theoretical, simulation, and hardware values.

$$\text{simulated gain} = 36.667 \times 11.25 = 412.503$$

TABLE II: Comparison of Theoretical, Simulation, and Hardware Values After first 2 stages

Parameter	Theoretical Value	Simulation Value	Hardware Value
Gain (A_v)	405	412.503	440

C. Active Band-Pass Filter Analysis

We have implemented a first order Band Pass filter The observations showcased at the end of this stage.

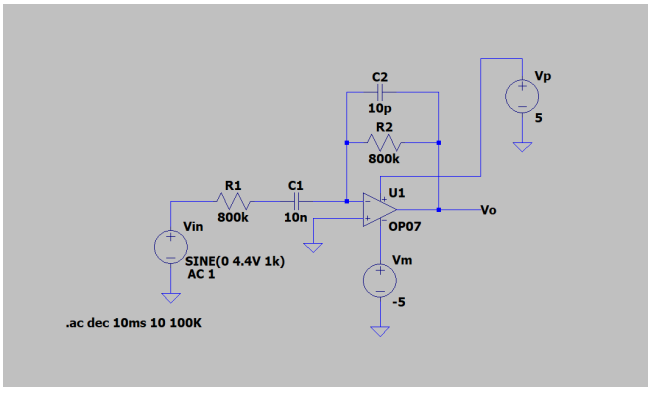

Fig. 6: Band Pass Filter Circuit in LTSpice

1) Working of the Active Band-Pass Filter: The active band-pass filter is implemented to remove unwanted noise and DC components while allowing a specific frequency range to pass. This is essential for ensuring signal integrity in the system.

- The high-pass section (R_1C_1) blocks low-frequency signals, including DC.

- The low-pass section (R_2C_2) attenuates high-frequency signals.
- The operational amplifier allows an implementation without inductors, and doesn't require impedance matching

2) Theoretical Analysis: The impedances in the circuit are given by:

$$Z_1 = R_1 + \frac{1}{j\omega C_1}$$

$$Z_2 = \frac{R_2}{1 + j\omega R_2 C_2}$$

Applying Kirchhoff's Current Law (KCL) at the inverting node:

$$\frac{V_- - V_{in}}{Z_1} + \frac{V_- - V_{out}}{Z_2} = 0$$

Since the op-amp is ideal with infinite gain, the inverting input is virtually grounded, i.e., $V_- \approx 0$, giving:

$$\frac{-V_{in}}{Z_1} + \frac{-V_{out}}{Z_2} = 0$$

Solving for gain:

$$\frac{V_{out}}{V_{in}} = -\frac{Z_2}{Z_1} = \frac{-j\omega R_2 C_1}{(1 + j\omega R_2 C_2)(1 + j\omega R_1 C_1)}$$

a) Frequency Response Analysis: We first note that (R_1, C_1) forms a high pass filter and (R_2, C_2) forms a low pass filter, therefore $R_1C_1 >> R_2C_2$.

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{R_2 C_1 \omega}{\sqrt{(R_2C_2\omega)^2 + 1} \cdot \sqrt{(R_1C_1\omega)^2 + 1}}$$

For different frequency ranges:

- When $\omega \ll \frac{1}{R_1C_1}$ (low frequencies, including DC), attenuation occurs due to the high-pass effect:

$$\left|\frac{V_{out}}{V_{in}}\right| \approx R_2 C_1 \omega$$

- When $\omega \gg \frac{1}{R_2C_2}$ (high frequencies), attenuation occurs due to the low-pass effect:

$$\left|\frac{V_{out}}{V_{in}}\right| \approx \frac{1}{R_1 C_2 \omega}$$

- In the midband range $\frac{1}{R_1C_1} \ll \omega \ll \frac{1}{R_2C_2}$, the gain simplifies to:

$$\boxed{\left|\frac{V_{out}}{V_{in}}\right| \approx \frac{R_2}{R_1}}$$

If $R_1 = R_2$, we achieve midband unity gain, which is desired in the 20Hz to 20kHz range.

b) Phase Response Analysis:

$$\angle\frac{V_{out}}{V_{in}} = -\frac{\pi}{2} - \left(\tan^{-1}(R_2C_2\omega) + \tan^{-1}(R_1C_1\omega)\right)$$

For different frequency regions:

- When $\omega \ll \frac{1}{R_1C_1}$, the phase shift is approximately $-\frac{\pi}{2}$ radians.
- When $\omega \gg \frac{1}{R_2C_2}$, the phase shift is approximately $-\frac{3\pi}{2}$ radians.
- In the midband region, phase shift approaches $-180°$.

It is apparent that the bandpass filter causes a phase offset, and shows inverting behaviour for midband frequencies.

3) Component Selection Based on Cutoff Frequencies: The cutoff frequency of the high-pass section is determined by R_1 and C_1, while the cutoff frequency of the low-pass section is determined by R_2 and C_2. Given the design requirements:

- The high-pass filter should have a cutoff frequency of $f_L = 20$ Hz.
- The low-pass filter should have a cutoff frequency of $f_H = 20$ kHz.

We chose the resistance values to both be equal to $800k\Omega$ which has the advantage of providing a high input impedance, and convenient capacitance values at the cutoff frequencies. The equality of resistances, as mentioned before ensures unity gain in the midband and attenuation of other frequencies.

a) Calculation of C_1 for the High-Pass Filter:: The cutoff frequency for a high-pass filter is given by:

$$f_L = \frac{1}{2\pi R_1 C_1}$$

Rearranging for C_1:

$$C_1 = \frac{1}{2\pi R_1 f_L}$$

Substituting $R_1 = 800$ kΩ and $f_L = 20$ Hz:

$$C_1 = \frac{1}{2\pi(800 \times 10^3)(20)}$$

$$C_1 \approx 10 \text{ nF}$$

b) Calculation of C_2 for the Low-Pass Filter:: The cutoff frequency for a low-pass filter is given by:

$$f_H = \frac{1}{2\pi R_2 C_2}$$

Rearranging for C_2:

$$C_2 = \frac{1}{2\pi R_2 f_H}$$

Substituting $R_2 = 800$ kΩ and $f_H = 20$ kHz:

$$C_2 = \frac{1}{2\pi(750 \times 10^3)(20 \times 10^3)}$$

$$C_2 \approx 10 \text{ pF}$$

Component	Value Chosen
R_1	800kΩ
R_2	800kΩ
C_1	10nF
C_2	10pF

TABLE III: Calculated Component Values

c) Observations:

- The band-pass filter successfully removes unwanted noise and DC components.
- The midband gain is consistent with the theoretical prediction.
- The phase response confirms the expected transitions between different frequency regions.

4) Result Plots and Verification: After passing the signal through the filter stage, we obtain the following output:

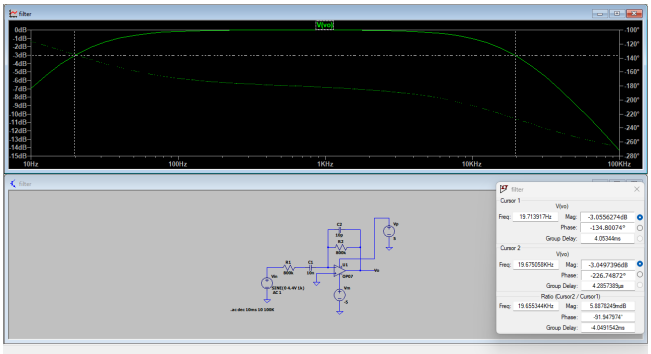

Fig. 7: Bode plot of the filter stage (LTSpice simulation)

From the Bode plot shown in **Fig 7**, we observe that the lower cutoff frequency at $F_L = 20$ Hz and the upper cutoff frequency at $F_H = 20$ kHz has a magnitude of **-3db dB**. While the mid-range has 0dB which means unity gain. In hardware, we also get similar results.

D. Power Amplifier: Class AB Amplifier Design

1) Importance of a Power Amplifier: A power amplifier is essential as the final stage in an audio amplification system, since the preceding stages lack the capability to deliver the high current required for driving low-impedance loads. For instance, delivering a 4V amplitude signal to a 10Ω speaker necessitates a current of 400mA, which is beyond the capacity of a standard operational amplifier or conventional transistor. To meet this requirement, we employ the **power transistors** TIP31A and TIP32A.

2) Operating Principle: The power amplification stage is realized using a **Class AB amplifier**, which provides a balance between the efficiency of Class B amplifiers and the low distortion characteristics of Class A amplifiers.

In the circuit, coupling capacitors are used to block any DC offset. (The high-pass CR filters have a cutoff frequency of approximately 1.59Hz, ensuring minimal signal loss). Diodes are employed to establish a voltage separation of about $1.4V$ between the base terminals of the NPN and PNP transistors. By appropriately selecting resistor values (as detailed in the following section), bias voltages of approximately $0.7V$ at the NPN base and $-0.7V$ at the PNP base are achieved. Consequently, during the positive half-cycle of the input, the NPN power transistor conducts the necessary high current, while during the negative half-cycle, the PNP transistor takes over.

The diode arrangement effectively mitigates **crossover distortion** by ensuring that both transistors are not simultaneously in the active region.

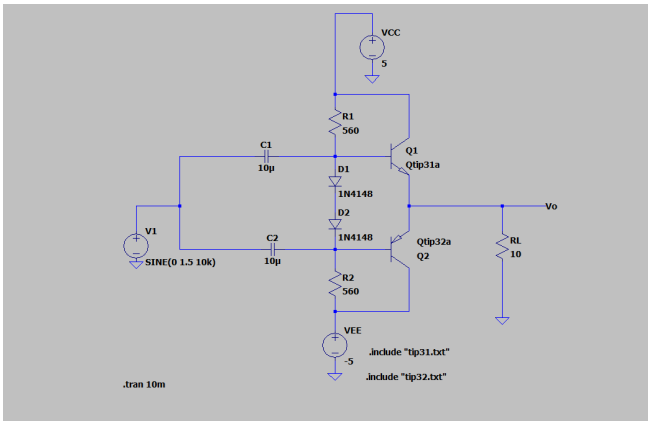

Fig. 8: Class AB Power Amplifier LTSpice Circuit

3) DC Biasing Analysis: To establish proper transistor biasing, the voltage drop across the base-emitter junctions of the complementary NPN and PNP transistors is typically assumed to be:

$$|V_{BE}| \approx 0.7V$$

Since there are two junctions (one for each transistor), the total bias voltage required is:

$$V_{B1} - V_{B2} \approx 1.4V$$

Assuming equal resistors $R_1 = R_2$ and a power supply voltage of $V_{CC} = \pm 5V$, we estimate the voltage drop across each resistor:

$$V_{R1} = V_{R2} = 4.3V$$

Using the 1/10th approximation:

$$I_{base} \approx 0.1 \times I_{branch}$$

where $\beta \approx 100$ for TIP series transistors. Through the AC analysis we will see the significance of the bias resistance values.

4) AC Analysis: Applying Kirchhoff's Current Law (KCL) at the emitters:

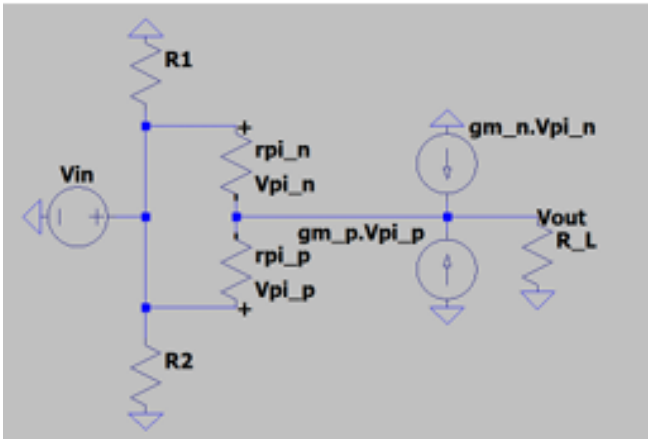

Fig. 9: Power Amp Small Signal model

$$\frac{V_{\pi n}}{r_{\pi N}} + \frac{V_{\pi p}}{r_{\pi P}} + g_{mN}V_{\pi n} + g_{mP}V_{\pi p} = \frac{V_{out}}{R_L}$$

We will use the notation

$$x = \frac{1}{r_{\pi N}} + \frac{1}{r_{\pi P}} + g_{mN} + g_{mP}$$

Now using $V_{in} - V_{out} = V_{\pi n} = V_{\pi p}$:

$$V_{in}(x) = V_{out}(x + \frac{1}{R_L})$$

5) Gain Calculation: The full gain expression is:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{\left(\frac{1}{r_{\pi N}} + \frac{1}{r_{\pi P}} + g_{mN} + g_{mP}\right)}{\left(\frac{1}{r_{\pi N}} + \frac{1}{r_{\pi P}} + g_{mN} + g_{mP} + \frac{1}{R_L}\right)}$$

To minimize attenuation, it is clear that we would like $x >> \frac{1}{R_L}$. Since $\frac{1}{r_\pi} = \frac{g_m}{\beta}$ these terms are less significant in x. Thus, we would like to have a high value of g_m which translates to a significant DC collector current I_C in both transistors.

We can also solve for the input impedance V_{in}/I_{in} using the KCL:

$$I_{in} = \frac{V_{in}}{R_{bias1}} + \frac{V_{in}}{R_{bias2}} + \frac{V_{in} - V_{out}}{r_{\pi N}} + \frac{V_{in} - V_{out}}{r_{\pi P}}$$

Moving forward we will use BJT matching to assume $r_\pi = r_{\pi N} = r_{\pi P}$ and $g_m = g_{mN} = g_{mP}$. We have also assumed equal bias resistances, which gives:

$$I_{in} = \frac{2V_{in}}{R_{bias}} + \frac{2(V_{in} - V_{out})}{r_\pi}$$

Using the gain equation, we can rewrite $V_{in} - V_{out}$ in terms of V_{in}:

$$\frac{2(V_{in} - V_{out})}{r_\pi} = \frac{2V_{in}}{2R_L(\beta + 1) + r_\pi}$$

Plugging this into the previous equation, we obtain the input impedance:

$$R_{in} = \left(\frac{R_{bias}}{2}\right) || \left(R_L(\beta + 1) + \frac{r_\pi}{2}\right)$$

Using the 1/10th approximation for I_B:

$$\text{branch current} \approx \frac{4.3}{R_{bias}}$$

$$I_C \approx \beta I_B$$

So we have to negotiate with the following tradeoffs:

- R_{bias} should be small to ensure attenuation is reduced, and
- R_{bias} should be sufficiently high to ensure the power amplifier's input impedance is high enough, to ensure excessive current is not drawn from the previous stage(s).

Continuously reducing the bias resistance (say less than 500Ω) will eventually result in clipping of the output from the previous stage - for example, the UA741 has an output current cap of $\approx 25mA$ after which clipping occurs. Therefore, we chose a bias resistance of 560Ω which when substituted into the relevant equations gives:

$$\text{branch current} \approx \frac{4.3V}{560\Omega} = 7.68mA$$

$$I_C \approx 100I_B = 100 \times 0.1 \times 7.68mA = 76.8mA$$

Now the value of transconductance will be roughly:

$$g_m = \frac{I_C}{V_T} = \frac{76.8mA}{26mV} = 2.954S$$

Using $\beta = 100$ and the transconductance we can approximate r_π:

$$r_\pi \approx \frac{\beta}{g_m} = \frac{100}{2.954} = 33.85\Omega$$

Thus, we can approximate the gain (for a 10Ω load) to be:

$$\frac{V_{out}}{V_{in}} \approx \frac{2.954 + 2.954 + 0.02954 + 0.02954}{2.954 + 2.954 + 0.02954 + 0.02954 + 0.1} = 0.98$$

Plugging in to the equation for input impedance, using the value of load = 10Ω:

$$R_{in} = 560\Omega || \left(10(100 + 1) + 16.92\right)\Omega$$

Thus, we have:

$$R_{in} \approx \frac{560 \times 1026.92}{560 + 1026.92} = 364\Omega$$

which is in perfect accordance with our LTSpice simulation result. So, for a 4V amplitude input signal, less than 12mA current would be pulled from the previous stage (but 400mA is delivered to the load!), ensuring stable operation.

6) Component Selection: A summary of the chosen values is given below:

Component	Value Chosen
R_1	560Ω
R_2	560Ω
R_L	10Ω (Speaker)
C_1	10μF
C_2	10μF

TABLE IV: Chosen Component Values

7) Results and Verification: The final output of our circuit has been obtained and analyzed through both simulation and hardware implementation.

The LTSpice simulation of the power amplifier provided the following output:

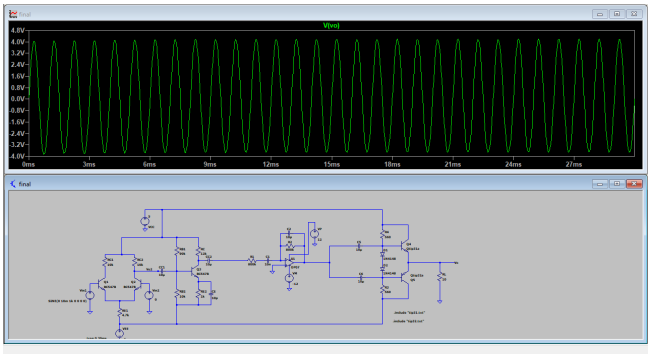

Fig. 10: Final Output in LTSpice

From the simulation, the output voltage is observed to be 7.89 V. Given the input voltage of 20 mV, the simulated voltage gain is:

$$A_v = \frac{7.89V}{20mV} = 394.5$$

The final output obtained from the hardware implementation at 2 kHz is shown below:

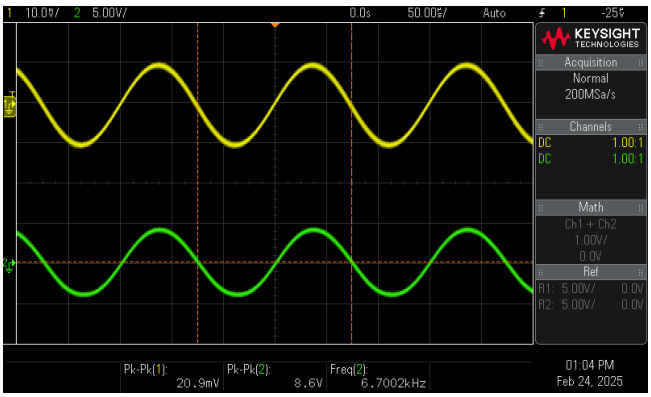

Fig. 11: Final Output on Hardware at 2 kHz

The measured output voltage at 2 kHz is 8.2 V, leading to a voltage gain of:

$$A_v = \frac{8.6V}{20mV} = 430$$

The following is the frequency response analysis:

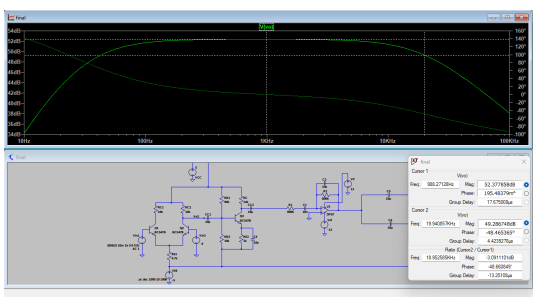

Fig. 12: Bode Plot from LTSpice Simulation

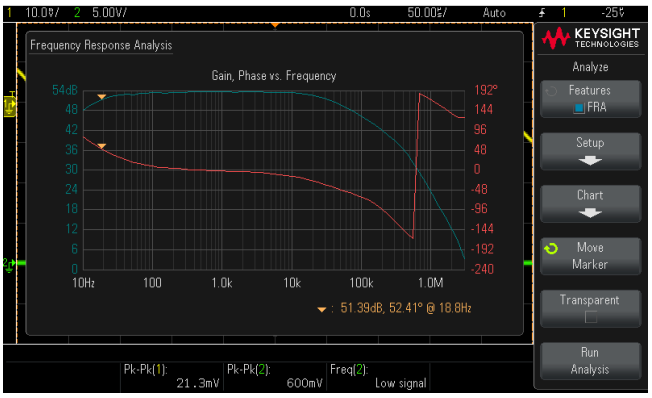

Fig. 13: FRA Hardware Output

The peak FRA gain was measured at 54 dB. At boundary frequencies:

- At $F_L = 20$ Hz, the gain is 51.59 dB, approximately -3 dB from the peak.
- At $F_H = 20$ kHz, the gain is 51.32 dB, approximately -3 dB from the peak.

These values indicate the expected attenuation at low and high-frequency limits.

The Total Harmonic Distortion (THD) analysis at 5 kHz shows harmonic peaks at the following frequencies:

- First peak at 5 kHz

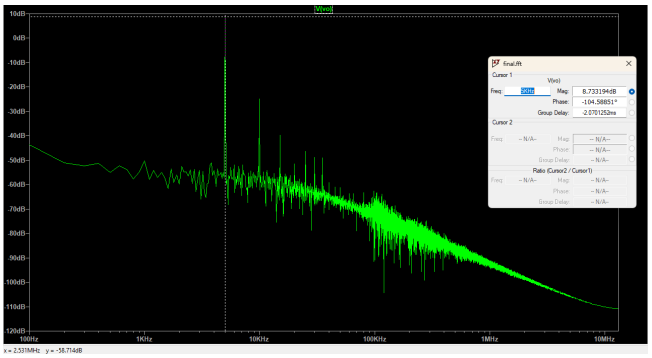

Fig. 14: THD First Peak at 5 kHz

- Second peak at 10 kHz

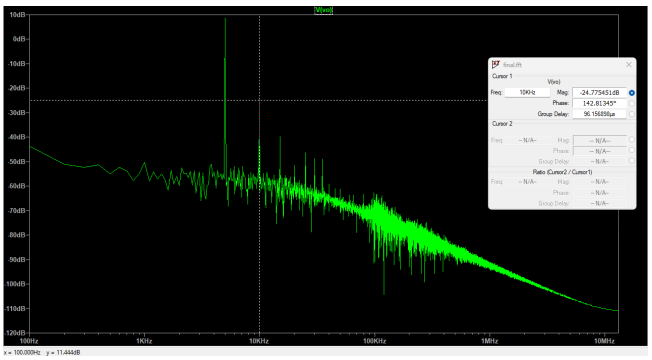

Fig. 15: THD Second Peak at 10 kHz

- Third peak at 15 kHz

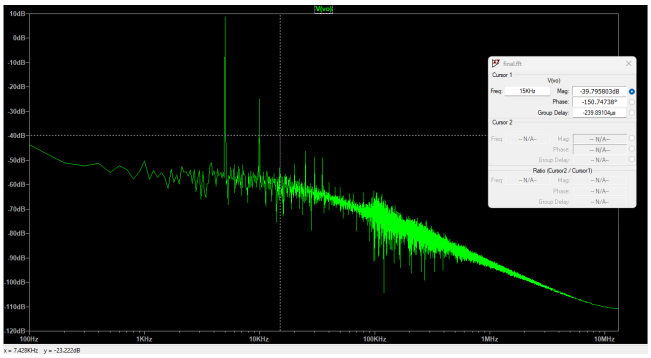

Fig. 16: THD Third Peak at 15 kHz

- Fourth peak at 20 kHz

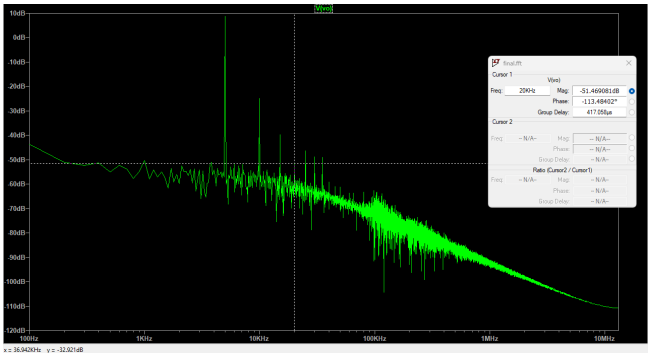

Fig. 17: THD Fourth Peak at 20 kHz

These harmonic peaks indicate the presence of distortion components in the output signal.

Parameter	Simulation	Hardware
Output Voltage at 2 kHz (V)	7.89	8.6
Voltage Gain	394.5	430
Peak FRA Gain (dB)	52.67	54
Gain at $F_L = 20$ Hz (dB)	49.70	51.59
Gain at $F_H = 20$ kHz (dB)	49.28	51.32

TABLE V: Comparison of Simulation and Hardware Results

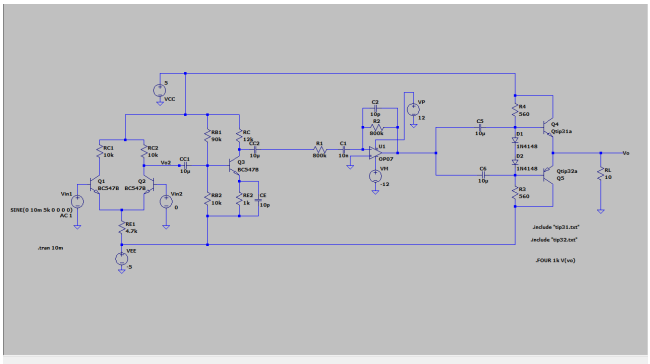

Fig. 18: Full circuit LT-Spice

III. Conclusion

This project successfully demonstrates the design and implementation of an audio amplifier with improved gain and efficiency.

Here are some working videos on hardware with one explaining the hardware and other playing music from mobile on amplifier.

- Working of Hardware
- Music on Audio Amplifier