COM219 HW4

Q1 (16 points) Quiz in class.

Q2 (20 points) In a 'CPU - two cache - memory' system the caches are connected in series (one after the other with L2 located between L1 and the main memory and L1 between L2 and the CPU. L2 is larger but slower than L1). During a CPU memory reference, first the L1 cache is searched and the result is returned to the CPU if found. Otherwise, if the item is not found, then the L2 cache is searched. Finally, the content is fetched from main memory if the reference is not found in L2. The hit ratios for L1 and L2 are 0.8 and 0.9 respectively. If the L1 access time is half of L2 and the L2 access time is one fifth that of the main memory access time, find the improvement the two cache system brings over the CPU-memory system without L1 and L2. More precisely, find the ratio of the access time of the main memory to the combined CPU-two cache-memory system described above.

Q3 (20 points) As manager of an IT department you need to evaluate a range of storage options for data storage on your servers. You have 12 drives of size 8 TB each and you plan to utilize all of them in one of the following configurations given below.

RAID 0, RAID 1, RAID 1+0 (where 0 splits drives into two groups of RAID 1),
RAID 100 (two symmetric groups of RAID 1+0),
RAID 5, RAID 6, RAID 6+0 (two symmetric groups of RAID 6)

Provide a table where the configurations are rows and the parts (a) through (c) below are the columns. Show all reasoning and calculations.

a) For each configuration, calculate the total effective disk size (excluding any indexing overhead). Explain your reasoning.
b) If each drive costs $100, calculate the per TB cost of usable (effective) data storage (not including redundancy) for the given configurations.
c) Find how many drive failures each system can tolerate. Provide your answer for the worst case.

Q4 (22 points) We would like to design and implement a digital circuit using logic gates. The circuit will check whether the 4-bit pure binary input number is an even number between 8 and 14, inclusive. That is, the circuit will have 4 inputs, $\mathbf{M=m_3m_2m_1m_0}$, and one output, **f**. The output will be 1 when the above condition holds and 0 otherwise. Derive the 4-variable truth table for **f** and then

a) Write the Boolean expression for **f** by finding the AND term for each row that is a 1 and combining them with ORs.
b) Draw the circuit diagram for the expression in part (a) using inverters, AND and OR gates (AND and OR gates with any number of inputs are permitted).
c) Simplify the expression in (a) using algebraic manipulation and draw the corresponding logic circuit.

Q5 (22 points) For each of the following functions:

a) **f = xy'z + xyz' + x'y' + xz'** (3 variables: **x,y,z**)
b) **f = x'yz + y'z'w + x' (y'z' +y'zw') + y'zw** (4 variables: **w,x,y,z**)
   i. Find the truth table.
   ii. Simplify the function through algebraic manipulation.
   iii. Make another column in the truth table and fill the column using the simplified expression to verify that it is equal to the column you found in part (i).