COM219 HW2

Q1 (15%) Quiz in class.

Q2 (15%) We would like to find the rate at which machine code instructions can be executed in a given CPU system like the one shown below for a program that resides in main memory. The CPU doesn't have a pipeline and therefore all operations are conducted sequentially.

Assume this CPU recognizes two types of instructions.

Type A: is a register-to-register instruction and it takes 10 clock cycles to execute, once the instruction is fetched into the instruction register (IR). It does not take any operands.

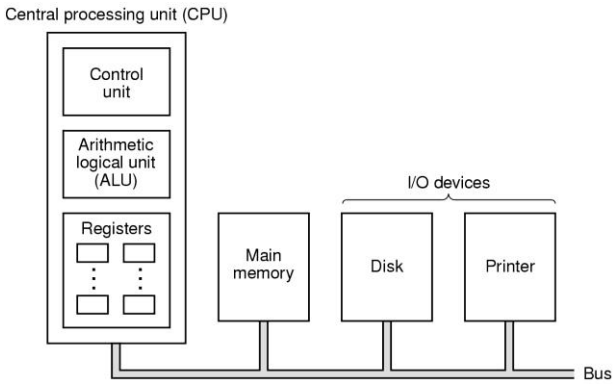
Type B: is a memory read/write instruction. This operation reads/writes the content (data) of a register from/to main memory at an address given in the program as an operand to this instruction. It takes 100 clock cycles once both the instruction and the operand have been fetched.

Since fetching an instruction is similar to a memory read/write operation it takes the same time as the read/write of a type B instruction to fetch an instruction from main memory into IR (100 cycles). Same applies for fetching an operand.

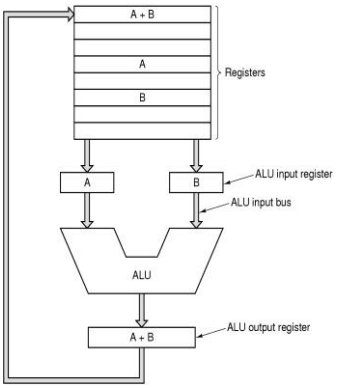
According to the fetch-decode-execute cycle, to execute a type A instruction, the CPU fetches the instruction (pointed to by PC) into IR, decodes it, and performs the operation (e.g. C=A+B). A type B instruction is executed by performing the following steps: fetch instruction into IR, decode instruction, fetch the operand from main memory, and then read/write content of a register from/to main memory. Assume decode time is negligible for both types of instructions.

Assume a typical program has 20 percent of memory read/write instructions (type B) and the rest are register-to-register instructions (type A).

a) Find the average instruction execution time on this CPU system. Give your answer in clock cycles.
b) Find the average time it takes to execute an instruction (t_1 in the multi-level example) if the clock frequency is 1 Mhz.
c) Find the instruction execution rate in part b (in instructions per second).
d) Find the processor bandwidth (the rate at which instructions are executed – instructions per second) if the clock frequency is 20 Mhz.
e) Find the program completion time of a 5 million-instruction program (at level 1 – machine code) in part d. Give your answer in seconds.



Q3 (15%) Consider the data path of a CPU on the right. With this configuration a register-to-register operation (e.g. C=A+B) takes 3 clock cycles; i.e. a fixed amount of time regardless of the complexity of the ALU operation. In the first cycle data is loaded into the ALU input registers from the main registers. For all registers the loading operation takes a maximum of 4 ns (nanoseconds). The ALU can compute any one of the 6 types of operations at a time. These take 7, 3, 9 10, 3, 12 ns each to produce the result at the output of the ALU. At the end of the ALU operation the data will be ready and in the second cycle the data is written into the ALU output register. Note that in this architecture every ALU operation needs to be completed in a single clock cycle. In the third cycle the value in the output register is written back to the destination (main) register(s).



a) Find the maximum clock frequency and bandwidth in MIPS that this microprocessor can handle for repetitive register-to-register operations if all operations are performed without any overlap between instructions (assume no wait time for fetching instructions). Note that the clock frequency will remain constant once set for operation and the cycle time will be the same for all clock cycles.
b) Repeat part (a) if the data path operates in a pipelined fashion, i.e. all units are kept busy. In any given cycle, the input, output and the destination registers are being loaded, and the ALU is performing an operation for the corresponding instruction. Assume there are no register read/write conflicts and instructions can be executed in order with a new instruction starting every clock cycle.
c) Find the program completion time of a one million instruction program separately for parts (a) and (b). Assume the instructions are readily available in IR and no extra time is spent to fetch them from memory.

Q4 (20%) Complete the following table for the given systems. Redraw the table onto your answer sheet; show all work and your reasoning below the table. Indicate which system is the fastest in terms of program completion time. Assume that execution is sequential and there is no branching in the programs being run. Also assume that an instruction is issued so as to maximize the resource utilization in the pipelined systems below.

System	Description	Cycle Time	Clock Frequency	Instruction Completion Time	Processor Bandwidth
A	No pipeline; instruction latency 20 ns, cycle time 5 ns				
B	No pipeline; instruction completion time 25 ns, clock frequency 250 MHz.				
C	7-stage pipeline, instruction completion time 35 ns				
D	Pipelined design, instruction completion time 10 ns, clock frequency 1 GHz.				
E	5-stage pipeline, cycle time 5 ns				
F	4-stage pipeline, processor bandwidth 250 MIPS.				

Q5 (15 points) The following 8-bit binary numbers are given (k=8). You can think of each of these as a number already written into an 8-bit register. Complete the table below according to the representations listed to interpret the given binary numbers. E.g. if the given binary number is 1001 (k=4) the pure binary interpretation would be 9, the two's complement would be -7, and BCD would be 9. Show all calculations and reasoning.

	01101011	**10011001**
Pure Binary	(Base-10 number)	(Base-10 number)
Sign-magnitude	(Signed Base-10 number)	(Signed Base-10 number)
Two's Complement	(Signed Base-10 number)	(Signed Base-10 number)
Excess 128	(Signed Base-10 number)	(Signed Base-10 number)
BCD	(2 BCD digits)	(2 BCD digits)
Hexadecimal	(2 Hex digits)	(2 Hex digits)

Q6 (20 points) Find the values of numbers given in the leftmost column if their corresponding binary numbers are interpreted with the representation given in the rightmost column. k designates the number bits used in the representations; it is the same in the original and the new representation. For each number, first find the binary number and write it in the middle column. Assume that for each row the number on the left is written into a register with the given representation (producing the middle column) and then the same binary number is read and interpreted with the representation on the right. Note that in the right column you will be using signed base-10 numbers for the values of pure binary, two's complement, excess-x and sign-magnitude representations.

Original Number	**Binary Number in Register**	**Value as interpreted with the new representation**
13 (pure binary, k=4) < Example >	1101	Two's Complement => -3 Excess-8 => 5 BCD => undefined Hexadecimal => D Sign-magnitude => -5

Original Number	**Binary Number in Register**	**Value as interpreted with the new representation**
11 (Pure Binary, k=4)		Excess-8
-14 (Sign-magnitude, k=5)		Two's Complement
68 (Pure Binary, k=6)		Two's Complement
-27 (Two's Complement, k=6)		Pure Binary
-76 (Two's Complement, k=8)		2-digit Hexadecimal
72 (interpret as 2-digit BCD)		Sign-magnitude
6DH (interpret as 2-digit Hex)		Excess-128