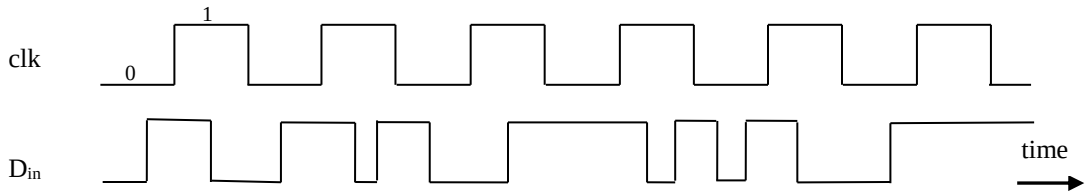
COM219 HW6

Q1 (25 points) Answers to the questions at the end of this homework will replace Quiz 6. It requires you to read Section 4.1 in the textbook, perhaps several times, and answer the questions. Note that as we discuss the Mic-1 architecture in class we will be providing answers to most of these questions. Work in groups of three (read the text before your meeting, discuss, and provide one write-up with names of all participants)

Q2 (25 points)

a) The signal D_{in} is connected to the D input of a D flip-flop given in Figure 3-25. It changes over time as shown below together with the clk signal that is connected to the clock input of the same D flip-flop. Draw the corresponding output Q over time. Redraw the two signals given below on your answer sheet and draw your answer below them so that their times correspond. The clock frequency is 100 Hz and Q=0 initially.



b) Redesign the pulse generator in Fig. 3-24 such that it produces a narrow pulse on the rising edge as well as on the falling edge of its input. You may use any type of two-input logic gate and inverters.

c) Replace the pulse generator in part (a) with the one you designed in part (b) and repeat part (a).

Q3 (25 points) These problems will serve as a refresher for memory calculations you will need for the next problem. Explain your reasoning for the following:

a) Assume that the 4 x 3 memory given in the text book is available in a single chip. How many of these chips are needed to implement a 16x12 memory system? What is the total number of D FFs used for this memory system?

b) Find the number of cells in a memory chip that has capacity of 32 Kilobits and is organized as 16-bit cells. How many address and data pins does this memory chip have?

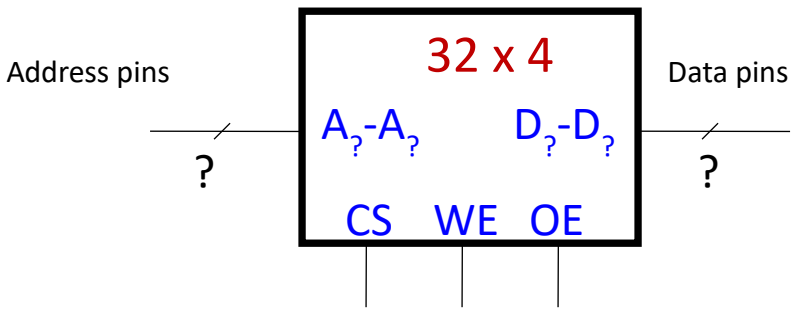
c) Find the size of the address space (in locations) of a CPU system with 24-bit address and 32-bit data bus.

d) Find the size of maximum addressable memory (maximum capacity) of a CPU system with 20-bit address and 16-bit data bus (in bytes).

e) How many 32Kx8 chips are required to completely fill the address range 30000H – BFFFFH with physical memory? CPU system has 20-bit address and 16-bit data bus.

Q4 (25 points) In this question you will design a 128x8 memory chip using 32x4 memory chips and decoders. Then, you will connect it to a CPU.

a) Find the number of address and data pins for the 32x4 memory chip shown below and redraw it with proper labels and indices. What is the capacity of this chip in bytes?



b) Design a 128x8 chip using as many 32x4 chips as necessary. Indicate inputs and outputs of all chips clearly. 2-to-4 and 3-to-8 decoders are available (each has a single active high enable). You may ignore the WE and OE connections. What is the capacity of this chip in bytes?

c) Now connect the new 128x8 chip to a CPU with a 12-bit address bus (A_0-A_{11}) and an 8-bit data bus (D_0-D_7) such that it appears at the address starting from 080H. You may use decoders, or any standard gates with any number of inputs for address decoding (apply full decoding). Give the address range of this chip in Hex. Use the 128x8 as a block with clearly labeled pins - no need to show the internal details.

d) If we were to fill the entire address space with the 128x8 chips, how many would we need? What would be the capacity of this system in bytes?

Quiz replacement: Carefully read Section 4.1 describing the Mic-1 architecture and study the hardware diagram.

a) Explain the function of the data path. How does it work?
b) What do the following register names stand for? SP, TOS, LV, CPP, and H.
c) Is it possible to add the contents of the registers SP and LV in one clock cycle?
d) How many cycles does it take to add the content of H and OPC and write back to OPC?
e) How many bits does each register hold (except MBR)? How about MBR?
f) Can multiple registers drive the B bus? How/Why?
g) Can the data on the C bus be written into multiple registers in the same clock cycle?
h) What do the N and Z outputs of the ALU represent?
i) The ALU doesn't have a subtractor, how does it do subtraction (e.g. B-A)?
j) What are the two functions of the shifter?
k) Explain how the MDR and MAR registers work as a pair.
l) Explain how the MBR and PC registers work as a pair.
m) Explain the process of sign extension while MBR is being copied onto the B bus.
n) Describe the functions of MPC and MIR.
o) What is the function of the 'next address' field in the MIR instruction format?
p) Explain the function of the JAM bits.
q) Explain the function of WRITE, READ and FETCH bits.