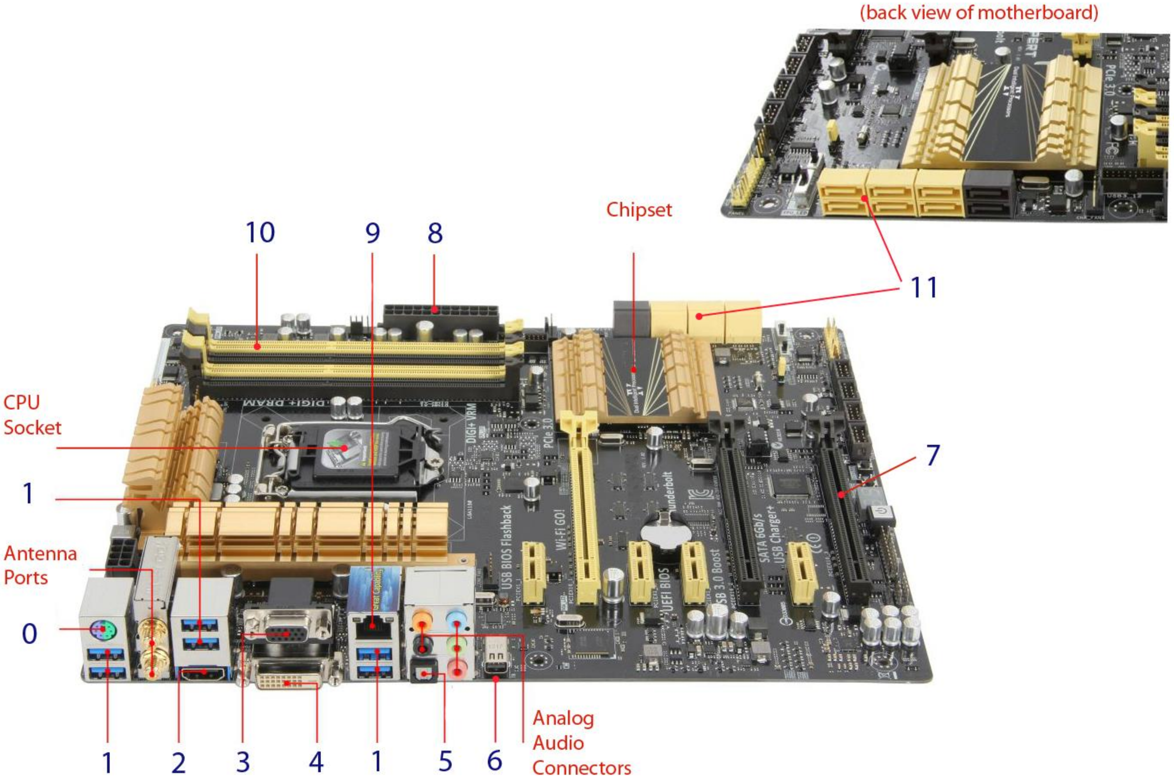
COM219 HW1

Q1 (15%) Quiz in class.

Q2 (15%) Identify the numbered connectors on the motherboard given below. Conduct research online to find the names and functions of these connectors. Provide a table with three columns similar to the one below on your answer sheet.

Connector Number	Name of Connector	Function
X (not shown in figure)	USB-C port	USB-C is used for charging, transferring data and display connections, it's a 24-pin connector which is distinguished by its two-fold rotationally-symmetrical connector
1		
2		
…	…	…



Q3 (20%) We have a 6-level computer and would like to execute a sequential 500,000-instruction program (**M**) made up of level-6 instructions. The following table gives the relationship between the numbers of instructions at different levels.

Level **(*n*)**	**Average number of instructions at the level below that implement one instruction at this level (i_n)**
6	3
5	2
4	4
3	2
2	3
1	-

Assume that the instructions at level 1 are of 3 separate types (**A**, **B** and **C**) and their execution times differ based on the type of instruction (i.e. register-to-register, register-to-memory etc.) In a typical program like the one being executed, 25 percent of the instructions are of type **A**, 45 percent of the instructions are of type **B** and the remaining are of type **C**. Each type **A** instruction takes 44 ns (nanoseconds), type **B** instruction takes 40 ns and type **C** instruction takes 20 ns to execute. Find the

a) number of level-1 instructions for each level-6 instruction.
b) average instruction execution time at level 1 (**t_1**).
c) average instruction execution time for each level-4 instruction (**t_4**).
d) average instruction execution time for each level-6 instruction (**t_6**).
e) program completion time for the given program (**T_{prog}**).
f) ratio of the new program completion time to that of the old, if an improvement is made to the translation method from level 2 to level 1 such that each instruction at level 2 is now translated to 2 instructions at level 1 (instead of 3) without changing the power of the instructions.

Q4 (15%) We have a multi-level computer which has hardware at level 1 and identical levels of translation at all levels above it. Each level has **W** times more powerful instructions compared to the level below it. An instruction being **W** times as powerful means that optimally sequenced **W** instructions at level **n-1** do the same work of one instruction at level **n**. In practice, the optimal translation from a level to the one below it is hard to achieve. Therefore, we will assume that an instruction at level **n** is translated into **S** instructions at level **n-1**, where **S** > **W**. Assuming we have 6 levels in this multi-level computer find the ratio of the time it takes to execute a program at level 6 to the time it takes an optimal sequence of instructions to do the same work at level 1. Assume all instruction types at one level take the same amount of time to execute. Generalize your answer to **N** levels.

Q5 (15%) Consider the hardware organization diagram discussed in class. Conduct research online to identify the component class (e.g. Motherboard, power supply, CPU, RAM, chipset, disk, sound card, graphics, card, network) of the following chips/devices. Reproduce the table below on your answer sheet (print or write) and fill the two right-hand columns.

Chip/Device	**Component Class**	**Approximate Price**
ASUS WS C422 SAGE/10G LGA2066 ECC DDR4 M.2 U		
AMD Radeon Pro WX 9100 - 4096 Stream Processors, 16GB vRAM		
Intel Core i7 i7-7700K - Quad Core, 4.2GHz		
MSI MEG X570 AMD SATA 6Gb/ USB 3.2		
Intel Core i9-7980XE X-Series 2.6 GHz 18-Core LGA 2066		
Cisco 32GB DDR4-2666-MHZ RDIMM PC4-21300 DUAL		
NVIDIA QUADRO RTX 8000		
AMD Ryzen Threadripper 1920X 12-Cores, Socket sTR4, 3.5GHz		
Intel 10PK OPTANE 800P SERIES INT 120GB		
Intel C246, 14 USB Ports, 24 PCI Express Lanes		(skip)
Corsair CX Series CX450M 450 Watt ATX		
Kingston 16GB DDR4, 2133MHz DIMM - KVR21R15D4/16		
AMD Phenom II X2 560		
NVIDIA Tesla K80 24GB GDDR5 CUDA Cores		
Creative Sound Blaster Z Series ZXR		
Seagate 1TB SATA 7.2K RPM 6GBPS 2.5IN		

Q6 (20%)

a) We would like to understand how the choice of doubling time in Moore's Law affects the increase in the estimated number of transistors that fit on a fixed-size chip. We have discussed the fact that the book quotes the doubling time as 18 months whereas it is commonly quoted as 2 years. Assume that at year 0, 8000 transistors fit on a chip with area A. Calculate the number of transistors on a chip of size 12A for year 0 and then every four years for the next 20 years, first using a two-year doubling time and then using 18 months. Print out the associated semi-logarithmic graph sheet (or edit the given image), mark the points on the graph and draw the curves/lines that represent the ideal relationship between time and number of transistors on a chip of size 12A. Draw the graphs for the two-year and 18-month relationships on the same sheet and clearly label them.

b) Assuming that the shape of a transistor is square, find the ratio of one side of the transistor at the end of 30 years to that at year 0. Calculate separately for a doubling time of two years and 18 months.