BPU Question 1

Considering a 2-bit saturating counter BHT of 1K entries; and assuming that the processor executes the following code fragment, determine the BHT final state and calculate the misprediction ratio in the presented case. The BPU initial state is indicated in the table.

General assumptions:
- R10 is the main loop control register and is initialized to 100
- R3 and R7 are reference values set to 1
- R2 is the input register
  - the input value is the incremental sequence of integer numbers starting from 0 (in the first iteration) to 99 (during the last iteration)

Address	Instruction	BHT (2-bit)	Prediction	misP. counter
0x0000	L0: …	0	NT	
…	; *Reading input values*	0	NT	
0x0010	AND R1, R2, R3	0	NT	
0x0014	BEQZ R1, L1	0	NT	
0x0018	…	0	NT	
0x001C	L1: XOR R4, R1, R7	0	NT	
0x0020	BEQZ R4, L2	0	NT	
0x0024	…	0	NT	
0x0028	L2: …	0	NT	
0x002C	DADDI R10, R10, #-1	0	NT	
0x0030	BNEZ R10, L0	0	NT	
0x0038	…	0	NT	

BPU Question 2

Considering a (2,2) correlating predictor of 1K entries; and assuming that the processor executes the following code fragment, determine the BPU final state and calculate the misprediction in the presented case. The BPU initial state is indicated in the table.

General assumptions:
- R10 is the main loop control register and is initialized to 100
- R3 and R7 are reference values set to 1
- R2 is the input register
  - o the input values are the integer numbers from 0 to 99

Address	Instruction	2-bit predictors				2-bit shift register	misP. counter
		00	01	10	11		
0x0000	L0: …	0	0	0	0	00	
…	; Reading input values	0	0	0	0		
0x0010	AND R1, R2, R3	0	0	0	0		
0x0014	BEQZ R1, L1	0	0	0	0		
0x0018	…	0	0	0	0		
0x001C	L1: XOR R4, R1, R7	0	0	0	0		
0x0020	BEQZ R4, L2	0	0	0	0		
0x0024	…	0	0	0	0		
0x0028	L2: …	0	0	0	0		
0x002C	DADDI R10, R10, #-1	0	0	0	0		
0x0030	BNEZ R10, L0	0	0	0	0		
0x0038	…	0	0	0	0		