ULTIMATE ELECTRONICS: PRACTICAL CIRCUIT DESIGN AND ANALYSIS

7.2

Op-Amp Voltage Buffer

An op-amp voltage buffer mirrors a voltage from a high-impedance input to a low-impedance output.

A **voltage buffer**, also known as a **voltage follower**, or a **unity gain amplifier**, is an amplifier with a gain of 1. It's one of the simplest possible op-amp circuits with closed-loop feedback.

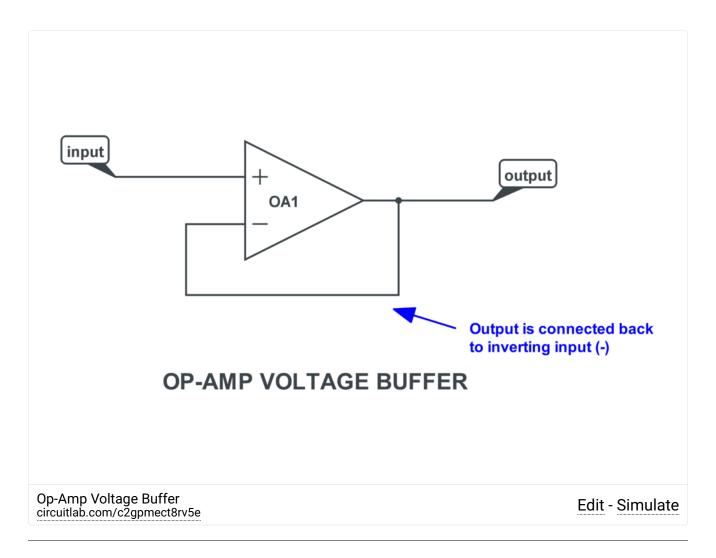
Even though a gain of 1 doesn't give any voltage amplification, a buffer is extremely useful because it prevents one stage's input impedance from loading the prior stage's output impedance, which causes undesirable loss of signal transfer. We covered this concept extensively in the Maximum Signal Transfer and Minimizing Interstage Loading section.

A voltage gain of 1 means that if the input voltage goes up by ΔV , then the output voltage is also designed to go up by the same ΔV .

An op-amp can be configured as a voltage buffer by:

- 1. Connecting the input signal to the non-inverting (+) input, and
- 2. Connecting the output directly back to the inverting input (-) with a wire

as shown below:



Intuitive Model

We mentioned in the <u>Ideal Op-Amp</u> section that the op-amp will change its output voltage until the two inputs are the same. We now have the first opportunity to see how that works because this circuit has closed-loop feedback from the op-amp's output back to one of its inputs. Let's build up a qualitative, intuitive model first before we work out the math.

In this case, we can slow down time and imagine what happens if we take a <u>steady-state</u> situation and then suddenly change the input voltage:

- 1. Suppose the input voltage is suddenly higher than the output.
- 2. The op-amp will see a higher voltage on its non-inverting input than its inverting input $(V_+ > V_-)$, and so the output voltage will start to increase.
- 3. The circuit is configured so that this increased output voltage loops back from the output, through the wire connecting the output to the inverting input.
- 4. The voltage at the inverting input increases.

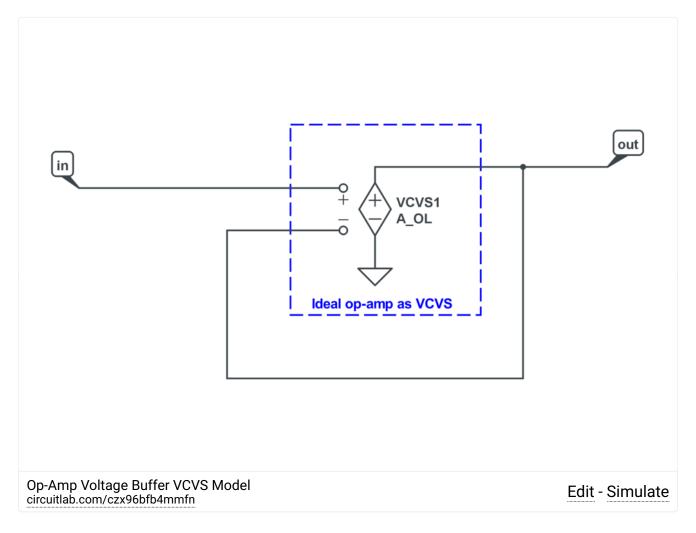
5. Once the inverting input voltage rises to meet the non-inverting input voltage, the output will stop increasing.

Solving the Equations

The voltage buffer circuit is connected so that:

$$V_+ = V_{
m in} \ V_- = V_{
m out}$$

From the ideal op-amp modeled as a VCVS, our buffer circuit looks like this:



The voltage-controlled voltage source gives us one additional equation:

$$V_{
m out} = A_{
m OL}ig(V_+ - V_-ig)$$

This is an example of <u>Dependent Source Feedback</u> because there's a connection from the output back to one of the inputs.

We can substitute in the V_+ and V_- above to find an equation that connects $V_{\rm out}$ to $V_{\rm in}$, and solve algebraically:

$$egin{aligned} V_{ ext{out}} &= A_{ ext{OL}}ig(V_+ - V_-ig) \ V_{ ext{out}} &= A_{ ext{OL}}ig(V_{ ext{in}} - V_{ ext{out}}ig) \ V_{ ext{out}} &= A_{ ext{OL}}V_{ ext{in}} - A_{ ext{OL}}V_{ ext{out}} \ V_{ ext{out}}ig(1 + A_{ ext{OL}}ig) &= A_{ ext{OL}}V_{ ext{in}} \ V_{ ext{out}} &= ig(rac{A_{ ext{OL}}}{1 + A_{ ext{OL}}}ig)V_{ ext{in}} \end{aligned}$$

Because the ideal op-amp assumes $A_{\mathrm{OL}}
ightarrow \infty$, we can take the limit:

$$\lim_{A_{\rm OL}\to\infty}\big(\frac{A_{\rm OL}}{1+A_{\rm OL}}\big)=1$$

so we simply have:

$$V_{
m out} = V_{
m in}$$

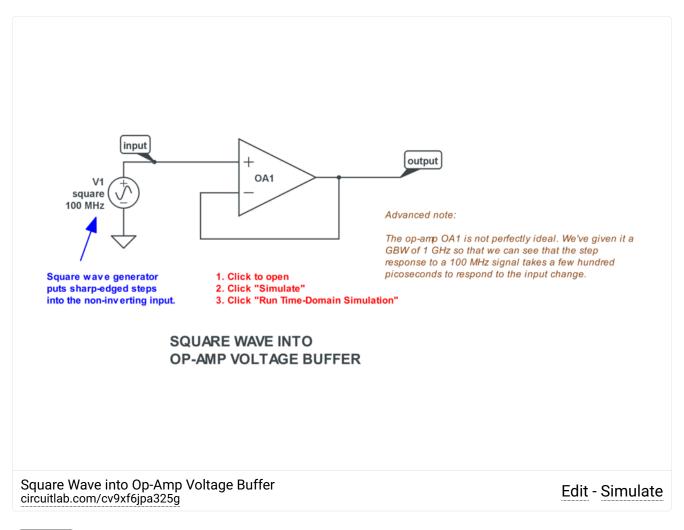
as expected for a voltage follower.

Even in non-ideal op-amps, because $A_{\rm OL}\gg 1$, this is an excellent approximation.

Step Response Time

In a truly ideal op-amp, with infinite gain and bandwidth and slew rate, the process described in the intuitive model happens instantaneously.

In the real world, op-amps have a finite gain-bandwidth product, so the intuitive model process happens more literally over a finite period of time. We can simulate this by using an op-amp that has finite gain-bandwidth product of 1 GHz, and passing in a 100 MHz square wave input signal:

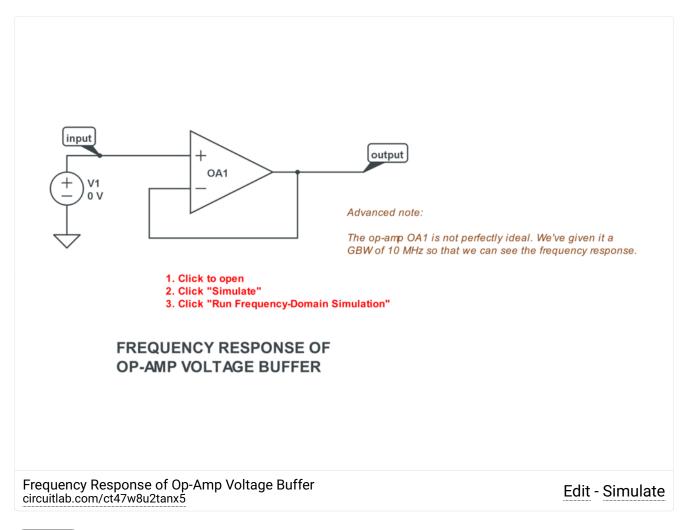


Click to open and simulate the circuit above. How long does it take for the output to respond after the input changes?

Frequency Response

With an ideal op-amp, the voltage buffer would have a perfectly flat frequency response, with a gain of 1 out to unlimited frequency.

In a real-world op-amp with a finite gain-bandwidth product, the voltage buffer configuration has a closed-loop gain of 1, so the bandwidth is equal to the gain-bandwidth product. Try this simulation with a 10 MHz GBW op-amp and observe that the gain is flat until reaching a corner at 10 MHz:



Click to open and simulate the circuit above. What's the <u>-3 dB frequency</u>? Double-click OA1, adjust the A_OL, and re-run the simulation: does the Bode plot change? Next, do the same for GBW.

As shown by this circuit simulation, the -3 dB knee in the frequency response curve happens at the gain-bandwidth product (GBW) of the op-amp.

For practical purposes, this means that we can assume that a real-world op-amp voltage buffer will do its job well for signals with a frequency much lower than the GBW of the opamp. (As a rule of thumb, let's say you're reasonably safe if $f_{\rm signal} < \frac{1}{10} {\rm GBW}$.) For signals at frequencies at or above the GBW, the op-amp won't be able to respond fast enough to copy the signal from input to output. The GBW is listed on an op-amp's datasheet, so you may be able to solve this problem by simply buying a faster op-amp.

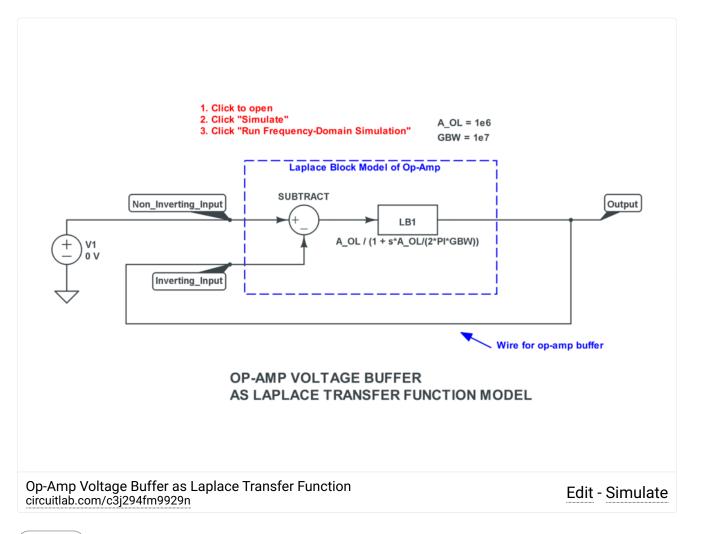
We'll now calculate the frequency response algebraically using the Laplace transform.

Laplace Transfer Function

As shown in the <u>Ideal Op-Amp</u> section, we can model the open-loop transfer function of the ideal op-amp (with finite GBW and A_OL) in the Laplace domain as:

$$H(s) = rac{A_{
m OL}}{1 + s ig(rac{A_{
m OL}}{2\pi {
m GBW}}ig)}$$

In fact, CircuitLab makes it easy to simulate this Laplace transform in the closed-loop feedback configuration, by simply removing the op-amp OA1 from our circuit above, and replacing it with the voltage subtraction and the Laplace transfer function:



Olick to open and simulate the circuit above. Observe that the frequency reponse of this Laplace Block model is identical to the frequency response shown for the op-amp circuit shown above. (Note that V1 is our input source, and in frequency domain simulations, the DC value 0 V shown on the schematic doesn't matter at all. For the purposes of constructing the Bode plot, V1 is treated as an AC signal source with amplitude 1 and phase 0. See the CircuitLab documentation on Frequency-Domain Simulation for more details.)

The simulation shows that with a wire providing closed-loop feedback from the output back

to the inverting input, the huge open-loop gain is tamed, yielding a closed-loop gain of 1, out until the GBW limit is reached.

We can show this algebraically as well. The op-amp is defined by the transfer function:

$$V_{
m out}(s) = ig(V_+(s) - V_-(s)ig)H(s)$$

And as we did at the beginning of this section, we can substitute in $V_+(s)=V_{\rm in}(s)$ and $V_-(s)=V_{\rm out}(s)$ to find:

$$egin{aligned} V_{ ext{out}}(s) &= ig(V_+(s) - V_-(s)ig)H(s) \ V_{ ext{out}}(s) &= ig(V_{ ext{in}}(s) - V_{ ext{out}}(s)ig)H(s) \ ig(1 + H(s)ig)V_{ ext{out}}(s) &= H(s)V_{ ext{in}}(s) \ \hline rac{V_{ ext{out}}(s)}{V_{ ext{in}}(s)} &= rac{H(s)}{ig(1 + H(s)ig)} \end{aligned}$$

This fraction $\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)}$ gives us the overall closed-loop response of the op-amp voltage buffer circuit. Let's plug in H(s) and simplify algebraically:

$$egin{aligned} rac{V_{
m out}(s)}{V_{
m in}(s)} &= rac{H(s)}{1 + H(s)} \ rac{A_{
m OL}}{1 + s \left(rac{A_{
m OL}}{2\pi
m GBW}
ight)} \ rac{V_{
m out}(s)}{1 + s \left(rac{A_{
m OL}}{2\pi
m GBW}
ight)} \ rac{V_{
m out}(s)}{V_{
m in}(s)} &= rac{A_{
m OL}}{1 + s \left(rac{A_{
m OL}}{2\pi
m GBW}
ight)} + A_{
m OL} \ rac{V_{
m out}(s)}{V_{
m in}(s)} &= rac{1}{(1 + rac{1}{A_{
m OL}}) + s \left(rac{1}{2\pi
m GBW}
ight)} \end{aligned}$$

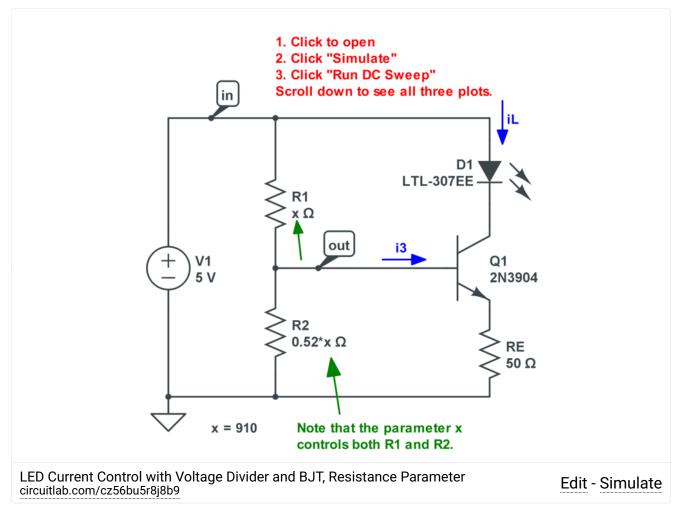
Since $A_{
m OL}\gg 1$, we can ${
m \underline{approximate}}\ 1+{1\over A_{
m OL}}pprox 1$. This gives us:

$$rac{V_{
m out}(s)}{V_{
m in}(s)} = rac{1}{1+sig(rac{1}{2\pi {
m GBW}}ig)}$$

As expected, since we're configuring the op-amp in a closed-loop configuration with a gain of 1, this closed-loop transfer function is simply the transfer function of a low-pass filter with a cutoff frequency of $f_c = \text{GBW}$.

Example: Buffering a Voltage Divider

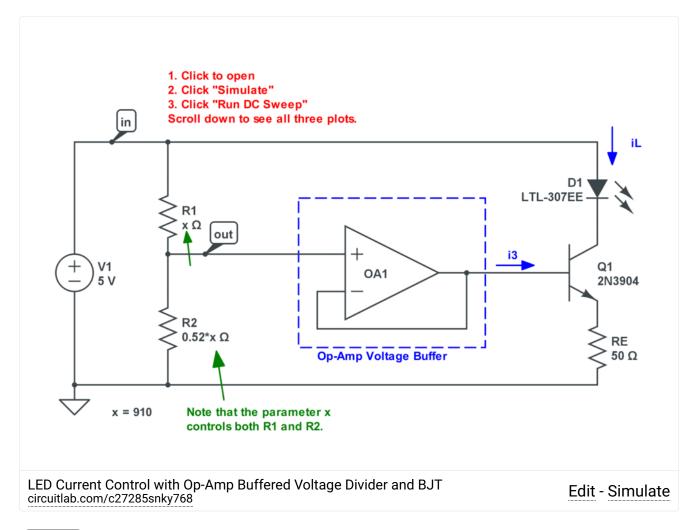
Let's revisit our <u>LED</u> Current Controller <u>Example</u> from the <u>Voltage Dividers</u> section. In this example, we used a voltage divider (R1 and R2) to set the voltage of an NPN BJT's base terminal:



Exercise Click to open and simulate the circuit above. How do $V_{
m out}$ and i_L change as we increase the resistance parameter x ?

The problem we explored in that section was how to choose the value of the the voltage divider resistors, given that we knew we wanted a fixed ratio 100:52 between R1 and R2. If we made the resistances too small, they wastefully consumed a lot of power, even more than the LED we were intending to control. If we made the resistances too big, they would not be able to handle the increased load from the base current into Q1, and the voltage would drop far below what we predicted. In that section, we used the simulator to find a sweet spot between those two effects.

But now that we have op-amps at our disposal, one easy application of the op-amp voltage buffer is to buffer the voltage divider, simply inserting the buffer between the voltage divider and Q1's base:



Click to open and simulate the circuit above. Now that we've added a buffer, how do V_{out} and i_L change as we increase the resistance parameter x?

As is quickly evident from the flat DC Sweep simulations, this lets us use much larger resistance values for R1 and R2 (therefore reducing power consumption in the voltage divider) without having any change in LED current!

In the real world, there is a tradeoff to this approach. By adding the op-amp voltage buffer, we win from the reduced power consumption in R1 and R2, but we lose a bit by adding the new power consumption of the op-amp's own quiescent current. We also slightly increased the cost and space required by adding a component. But in many cases, the math works out that this is a winning trade!

Most importantly, the buffer allows us to isolate different sections of the design: the design choices of R1+R2 are now much more independent from the design choices of Q1+RE. This alone can be a huge win by making the engineer's life easier and in making the design more robust to component manufacturing variations.

(Advanced readers note: this is not the best way to use an op-amp and BJT as a precision current source. There's a better way, covered in a later section!)

What's Next

We've used an op-amp to build a voltage buffer with voltage gain $A_v=1$. In the next few sections, we'll look at alternative configurations:

- $A_v \leq 1$: Op-Amp Voltage Reference
- ullet $A_v \geq 1$: Op-Amp Non-Inverting Amplifier
- ullet $A_v \leq 0$: Op-Amp Inverting Amplifier

Let's start by putting the buffer to good use as an Op-Amp Voltage Reference.

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