Design of the Signal Generator for ISS-Bioreactor

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This technical report is prepared to document the design of the signal generator circuit for the ISS-Bioreactor project at Boise State University.

1. INTRODUCTION

We design an input PWM filter to create the desired $0-10$V sine wave at 90Hz that the controller expects from a carrier PWM signal at a carrier frequency 36.6kHz.

This technical report builds the final design up over a few major steps. For the impatient reader, the theoretical analysis, its implementation, and the full blown-up schematic of the final design are provided in Section 2.3, Section 3, and Figure 8 of the Appendix A, respectively.

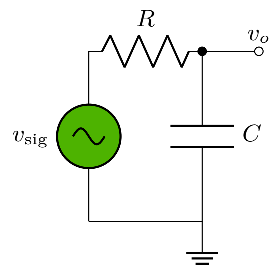

FIG. 1: A first-order low-pass filter circuit.

2. THEORETICAL ANALYSIS

We perform basic PWM filter design to generate the driving $0 - 10$V sine wave for the Physik Instrumente (PI)'s piezoelectric actuator [3].

2.1. Basic Lowpass Filter Design

Consider the first-order filter sketched in Figure 1 with a sinusoidal driving voltage. The current i over the capacitor is $i = C\frac{\mathrm{d}v_o}{\mathrm{d}t}$. KVL around the circuit gives

$$RC\frac{\mathrm{d}v_o}{\mathrm{d}t} + v_o = v_{\text{sig}} = A\cos(\omega t) \tag{1}$$

This differential equation has the transfer function

$$G(s) = \frac{1}{RCs + 1}.$$

The steady-state solution of the differential equation (1) is obtained as

$$\begin{aligned} v_o(t) &= A\,|G(j\omega)|\cos(\omega t + \angle G(j\omega)) \\ &= \frac{A}{\sqrt{1 + \omega^2 R^2 C^2}}\cos(\omega t - \arctan(\omega RC)) \end{aligned} \tag{2}$$

Since we do not want our signal to be attenuated by the low-pass filter, we must choose the values of R and C such that $\omega RC \ll 1$ or $2\pi RC \ll {}^1/_f$.

Unfortunately, our actual input from the microcontroller is not a pure sine wave, rather a PWM signal. Therefore, we also need the value of $2\pi RC$ to be large so that it attenuates the high frequencies present in the PWM signal. This requirement is difficult to achieve with just a first-order low-pass filter, leading us to design a second-order low-pass filter in the next subsections.

2.2. Second-Order LPF Design

The second-order filter is implemented in the first part of the circuit presented in Figure 2. The second part of this circuit amplifies the sine wave extracted from its PWM modulation from $0-3.3$V to $0-10$V. We analyze the circuit so as to figure out the values of the various resistances and capacitances.

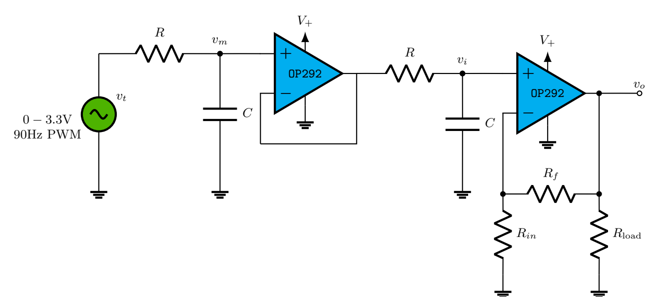

FIG. 2: The signal generator circuit.

We start by analyzing how the input voltage, v_i, to the non-inverting amplifier, responds to Teensy-generated PWM voltage, v_t. This is a $0 - 3.3$V PWM signal to be filtered to extract the modulated sine wave. Thanks to the buffer op-amp, the transfer function from the Teensy input v_t to the input v_i to the non-inverting amplifier op-amp is given by

$$H(s) = \frac{V_i(s)}{V_t(s)} = \frac{1}{R^2C^2s^2 + 2RCs + 1}. \tag{3}$$

This is a fully-damped transfer function with poles at $s_{1,2} = -{}^1/_{RC}$. In other words, the cut-off frequency of this filter is at $f = \frac{1}{2\pi RC}$ with a roll-off of 40dB per decade. Contrast this to the first-order filter of

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the previous subsection where the roll-off was 20dB per decade. The greater roll-off rate allows us be able to select $2\pi RC \ll 1/f$ while simultaneously achieving excellent high-frequency attenuation.

Our desired signal is a 90Hz sinusoidal. We do not want to lose this signal, i.e., we want our transfer function $H(s)$ to approximately have a unity gain at this frequency. We set $2\pi RC \leq 1/900$ or $RC \leq 1.768 \times 10^{-4}\Omega\,\mathrm{F}$ to satisfy this requirement. Using some standard values of the resistance $R = 47\mathrm{k}\Omega$ and the capacitance $C = 1\mathrm{nF}$, we obtain $RC = 4.7\times10^{-5}\Omega\,\mathrm{F}$, meeting the specification. The attenuation at Teensy's PWM carrier frequency of 36.6kHz is found by

$$20\log_{10}\{|H(j2\pi 36600)|\} = -55.163\,\mathrm{dB}.$$

Lastly, we want to amplify the input voltage v_i thrice in order to hit the $0-10$V mark. The gain of the non-inverting amplifier is $k = 1 + R_f/R_{in}$. We choose $R_f = 2\mathrm{k}\Omega$ and $R_{in} = 1\mathrm{k}\Omega$ to achieve $k = 3$. The high gain bandwidth product of the `OP292` op-amp is read from its datasheet to be GBP = 4MHz. Hence the transfer function from the input voltage v_i to the output voltage v_o that will be applied to the PI controller is approximately given by

$$\frac{V_o(s)}{V_i(s)} = \frac{k}{\frac{k}{2\pi\mathrm{GBP}}s + 1} \approx \frac{3}{1.194\times10^{-7}s + 1},$$

which will have a firm unity gain at our desired oscillation frequency of 90Hz.

2.3. Sallen-Key Architecture

Another well-known architecture that works well for this sort of problem is the Sallen-Key low-pass filter, which replaces the two RC+buffer combination whose output enters the amplifier op-amp, as shown in Figure 3. The blown-up full schematic of signal generator circuit may be found in Figure 8 of the appendix.

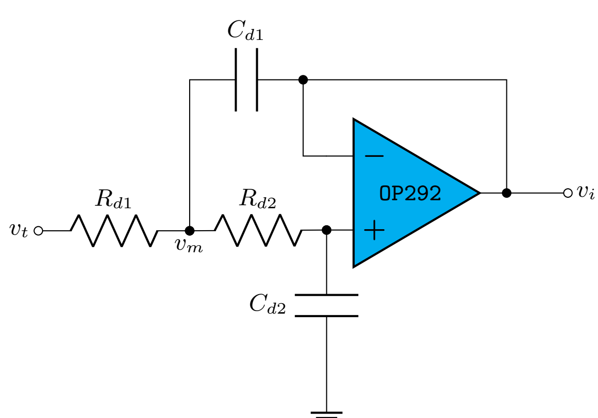

FIG. 3: Sallen Key (second-order) low-pass filter.

We find the governing equations of this circuit. Assume an ideal op-amp model so that both of the inputs of the op-amp have potential v_i. Let the current i flowing over R_{d1} split into i_1 and i_2, the former flowing into C_{d1} and the latter into C_{d2} through R_{d2}. KCL gives

$$\begin{aligned} i &= i_1 + i_2 = \frac{1}{R_{d1}}(v_t - v_m), \\ i_1 &= C_1\frac{\mathrm{d}(v_m - v_i)}{\mathrm{d}t}, \\ i_2 &= C_2\frac{\mathrm{d}v_i}{\mathrm{d}t}. \end{aligned}$$

KVL around the bottom loop ($v_m - v_o - \mathrm{gnd}$) gives $v_m = R_{d2}i_2 + v_i = R_{d2}C_{d2}\frac{\mathrm{d}v_i}{\mathrm{d}t} + v_i$. Plugging this into the second equation gives $i_1 = R_{d2}C_{d1}C_{d2}\frac{\mathrm{d}^2 v_i}{\mathrm{d}t^2}$. Combined with the first and third equations, this yields

$$R_{d1}R_{d2}C_{d1}C_{d2}\ddot{v}_i + (R_{d1} + R_{d2})C_{d2}\dot{v}_i + v_i = v_t. \quad (4)$$

We will take $R_{d1} = R_{d2} = R_d$ and $C_{d1} = C_{d2} = C_d$ so that the transfer function for this linear differential equation is observed to coincide with that of equation (3) of Section 2.2:

$$H(s) = \frac{V_i(s)}{V_t(s)} = \frac{1}{R_d^2C_d^2s^2 + 2R_dC_ds + 1}.$$

Therefore, all the analysis that follows equation (3) goes through for the Sallen-Key architecture as well. Theory, simulation and experiments show that some good values for the resistances R_d and the capacitances C_d are $R_d = 47\mathrm{k}\Omega$ and $C_d = 1\mathrm{nF}$, with a cutoff frequency of $f \approx 3386$Hz. There is a range of resistance and capacitance values that work well around these nominal values.

Remark 1. *This is the filter to be implemented in the final design.*

3. RESULTS

We provide extensive simulation and experimental data and their interpretation, supporting that the proposed analog signal generator works as intended.

3.1. Simulation

We perform a realistic simulation with a second-order low-pass filter we came up with in Section 2.2. One of the important aspects of this design is the selection of the op-amp. In order to keep the common-mode voltage at 0V we choose the op-amps as CMOS type. One such op-amp is `OP292` [2], which is used in this simulation.

The PWM signal generated by Teensy [4] is simulated exactly with a carrier frequency of 36.6kHz modulating the signal

$$V_{\mathrm{pwm}} = 3.3/2 + 3.3/2\sin(2\pi 90t).$$

Finally, the impedance of the load (PI's controller) is read off from its datasheet and inserted as a 100kΩ resistance. The circuit that is simulated using LTSpice [1] is presented in Figure 4.

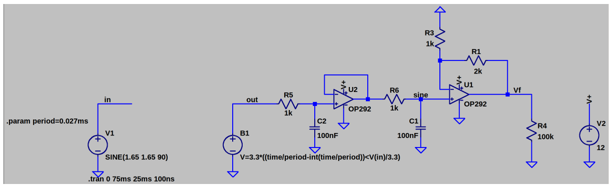

FIG. 4: The signal generator circuit in LTSpice

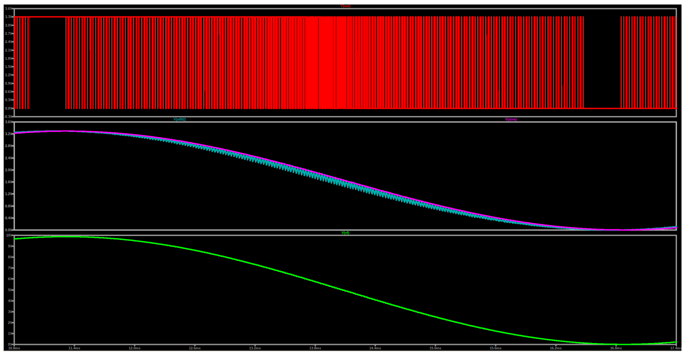

FIG. 5: The response from the simulation for one full period.

The simulation generates the relevant voltage responses, provided in Figure 5. The top plot shows the PWM signal generated by Teensy modulating a sine-wave at 90Hz frequency. The individual plots in the middle show the output of the first (cyan) and the second (purple) RC low-pass filters (v_f and v_i, respectively) that extract the modulated signal from its PWM representation. Finally, the last plot shows the amplified signal (gain = 3) through the op-amp `OP292`. This signal is ready to be sent to the PI controller.

The performance of the Sallen-Key architecture from Section 2.3 is shown in Figure 6, where the values for the resistances were taken to be $R_d = 68\text{k}\Omega$ and capacitances to be $C_d = 1\text{nF}$. Even though the performance of the Sallen-Key filter of Section 2.3 looks very similar to the RC+buffer filter of Secton 2.2 in simulation, in the experiments the Sallen-Key filter outperforms significantly. We will implement this filter in our final design.

3.2. Experiment

The design is implemented on a simple setup on my table top by lighting two red LEDs, first one using the filtered PWM and the second using the amplified signal, both obtained using the circuit in Section 2.3.

Figure 7 shows the response of the second-order Sallen-Key LPF observed through an oscilloscope. This is the output of the signal generator in response to the Teensy generated 90Hz $0-3.3$V PWM signal modulating the desired sine wave. This response is satisfactory and should drive the PI controller without any issues.

4. DISCUSSION AND CONCLUSIONS

A sine wave is modulated using a $0-3.3$V PWM output of a Teensy 4.1 microcontroller at a carrier frequency of 36.6kHz. We presented to second-order lowpass filters to extract the modulated signal from its PWM representation: (i) RC+buffer configuration, (ii) Sallen-Key architecture. We have shown that in simulation both perform similarly, however in experimentation the Sallen-Key filter performs significantly better. We have decided to use this filter in our final design on the bioreactor.

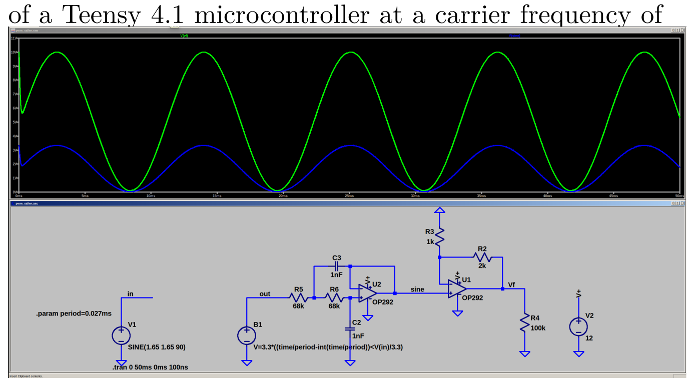

FIG. 6: The response of the Sallen-Key architecture.

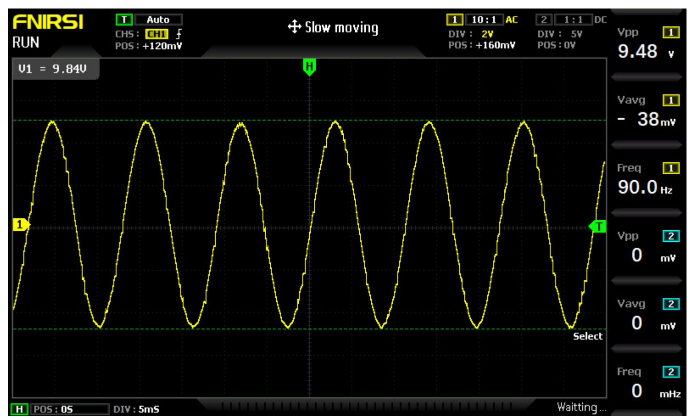

FIG. 7: The response of the second-order Sallen-Key filter.

5. ACKNOWLEDGMENT

The author thanks Drs. John Chiasson and Vishal Saxena of Electrical and Computer Engineering at Boise State University and University of Delaware, respectively, for their invaluable insights into the practical implementation of the signal generator.

[1] Analog Devices. LTSpice, . URL https://www.analog.com/en/design-center/

design-tools-and-calculators/ltspice-simulator.html.

[2] Analog Devices. OP 292, . URL https://www.analog.com/en/products/op292.html.

[3] Physik Instrumente. E-610. URL https://www.physikinstrumente.com/en/products/controllers-and-drivers/nanopositioning-piezo-controllers/e-610-piezo-amplifier-controller-601000.

[4] PJRC. Teensy. URL https://www.pjrc.com/teensy/.

Appendix A: Full Circuit Drawing of the Final Design

The final signal generator circuit schematic is presented in Figure 8. The potentaial v_t denotes the $0-3.3$V PWM signal modulating a 90Hz sinusoidal wave at a carrier frequency of 36.6kHz. The potential v_o denotes the $0-10$V analog 90Hz sine-wave signal ready to be sent to the Physik Instrumente controller as its reference input.

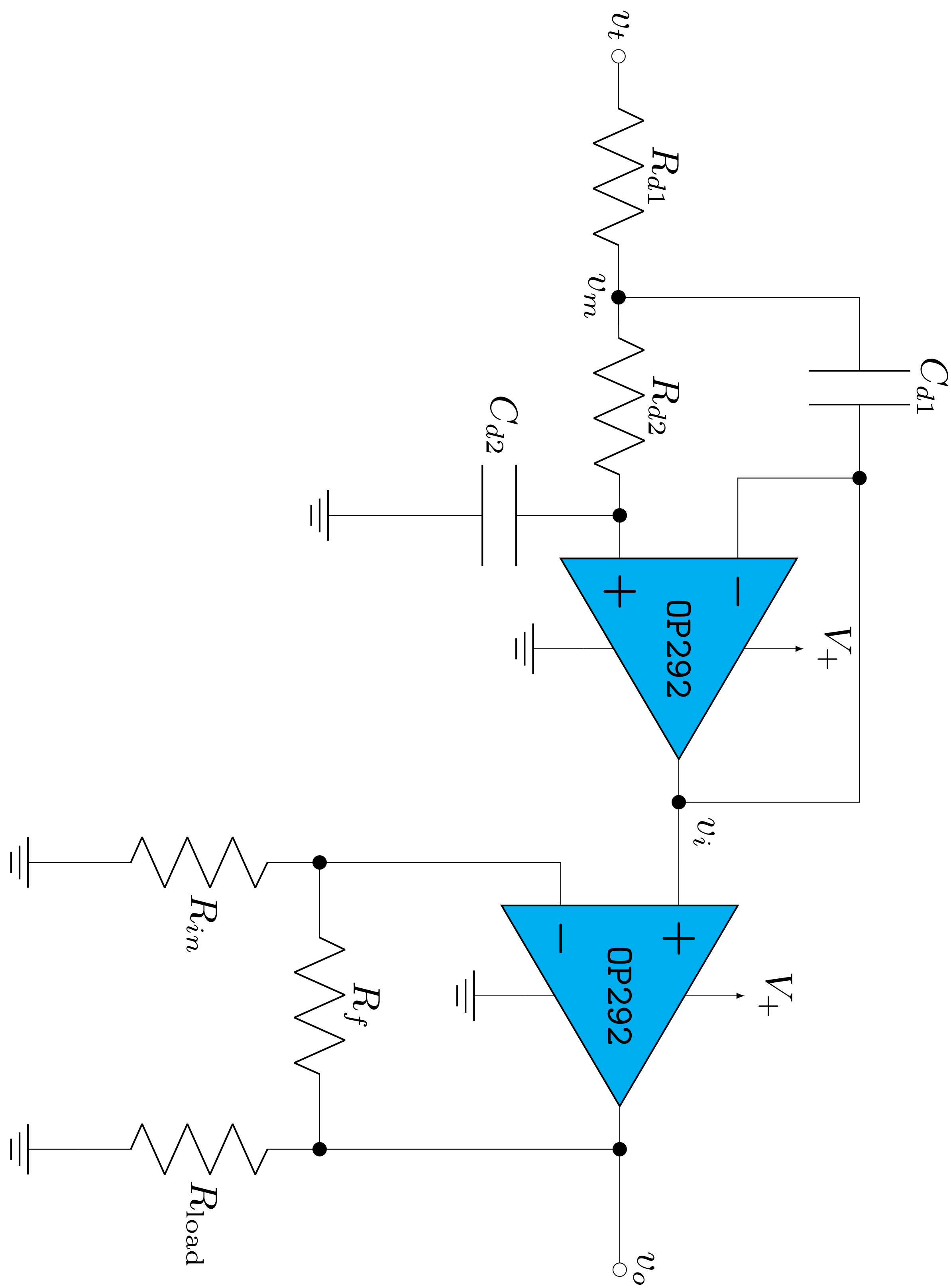

FIG. 8: The final signal generator circuit design.