7.5

Op-Amp Inverting Amplifier

An op-amp circuit forming a voltage amplifier with negative gain set by the ratio of two resistors.

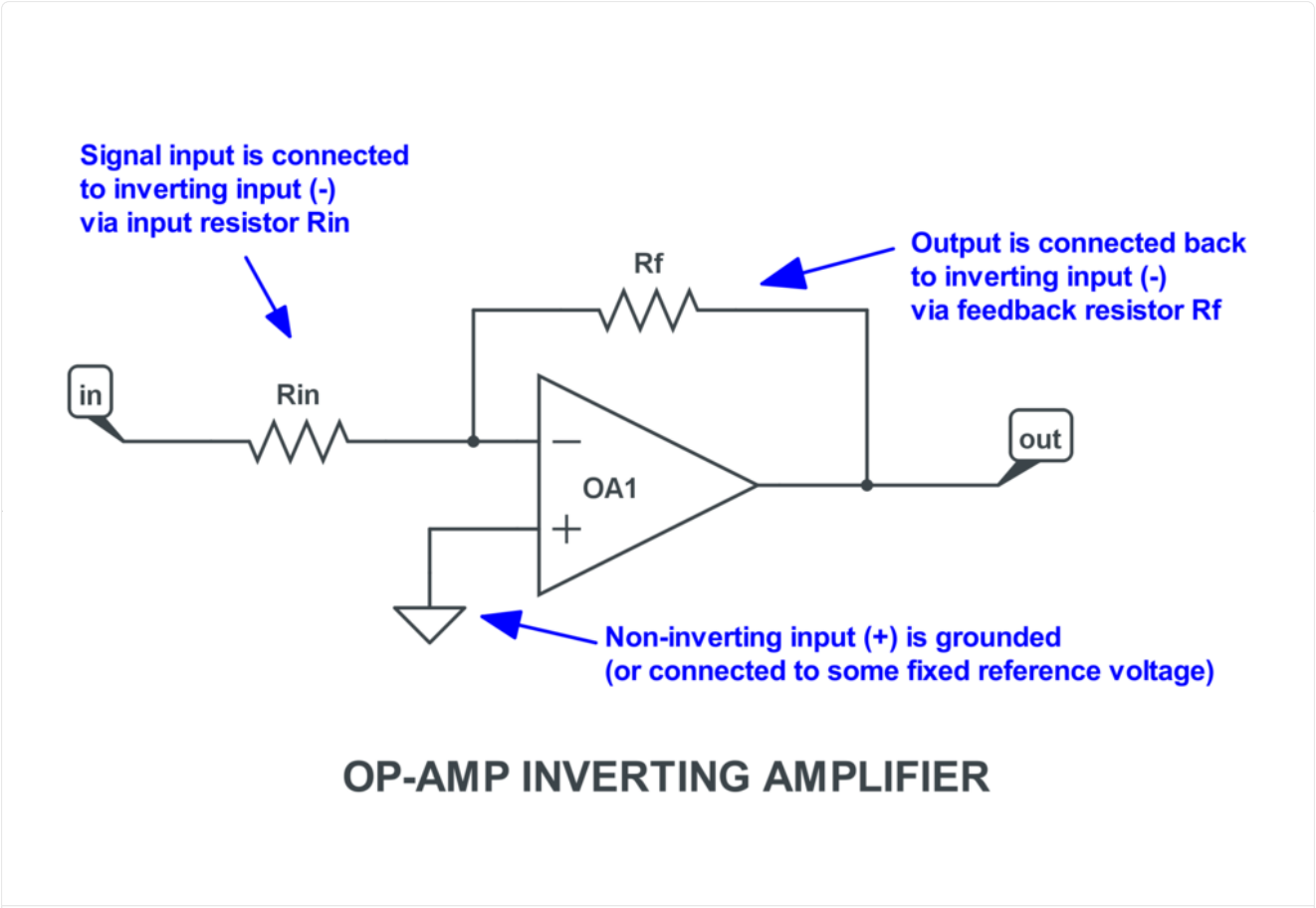
In previous sections, we used two resistors plus an ideal op-amp to make a non-inverting amplifier, with $A_v \geq 1$. We also showed how to rearrange those two resistors to create an op-amp voltage reference with $0 \leq A_v \leq 1$. Now, we'll take care of the negative gain values: we will rearrange the two resistors and create an **inverting amplifier**, where the signal becomes inverted: $A_v \leq 0$.

A voltage gain of A_v means that if the input voltage goes up by ΔV , then the output is designed to go up by $A_v \Delta V$. As the name implies, for an inverting amplifier, **the gain is always negative** $A_v \leq 0$. When the input goes up, the output goes down.

An op-amp can be configured as an inverting amplifier by:

1. Connecting a resistor R_{in} between the signal source and the op-amp's inverting (-) input, and
2. Connecting a resistor R_{f} from the op-amp's output back to the inverting (-) input, and
3. Connecting the op-amp's non-inverting (+) input to ground (or another fixed reference voltage)

This amplifier has voltage gain $A_v = -\frac{R_{\text{f}}}{R_{\text{in}}}$ as shown below:



Op-Amp Inverting Amplifier
circuitlab.com/cbrb4w7egr83k

Edit - Simulate

We'll call our **design gain** k :

$$k = \frac{R_{\mathrm{f}}}{R_{\mathrm{in}}}$$

which is the ratio of the two resistances. For clarity we'll leave the minus sign out of this, so

$$A_v = -k$$

Next we'll show several ways to understand why the gain is $-\frac{R_{\mathrm{f}}}{R_{\mathrm{in}}}$.

Intuitive Model

The ideal op-amp changes its output until the two inputs are equal. No current ever flows into the inputs of an ideal op-amp, so the only way to make the inputs equal is by changing the output and relying on an external feedback network.

By applying Kirchhoff's Current Law at the inverting input node, the current through R_{in} must therefore be equal to the current through R_{f} . By Ohm's Law, if the two resistors carry the

same current, then their voltage drops will be proportional to the ratio of their resistances.

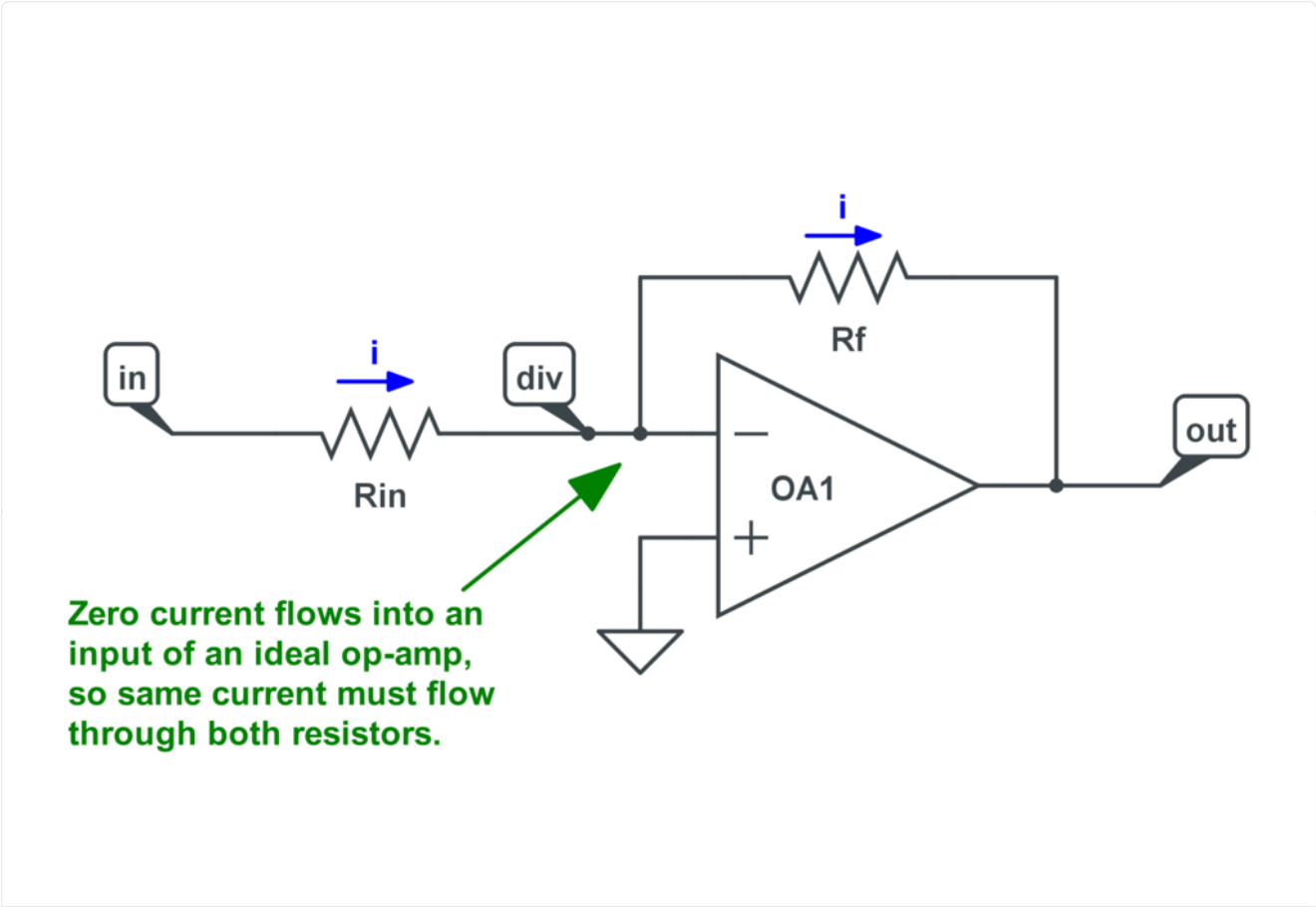
When all is operating properly, the op-amp output will be whatever is needed to hold the inverting input's voltage at zero, to equal the grounded non-inverting input. This effect means that the op-amp's inverting input node is called a **virtual ground**. A virtual ground means that the node is effectively held at a fixed voltage, but this happens via feedback, rather than being directly connected to ground itself.

Because of the virtual ground at the inverting input, we know the voltage drop across the resistor R_{in} is just $V_{\text{in}} - 0$. This tells us the voltage drop across R_{in} , which is directly proportional to the drop across R_{f} . And again due to the virtual ground, the voltage drop across R_{f} is just $0 - V_{\text{out}}$, so we know our output voltage.

Suppose $R_{\text{in}} = R_{\text{f}}$, and we then apply $V_{\text{in}} = 1\ \text{V}$. After the feedback loop settles, some amount of current will pass through both resistors, such that the voltage drops across each resistor are equal. One volt is dropped from V_{in} to the non-inverting input, and equally, one more volt is dropped from the non-inverting input to V_{out} , yielding $V_{\text{out}} = -1\ \text{V}$.

Solving the Equations

As we did with the non-inverting amplifier, let's label the inverting input node V_{div} so we can see how the circuit operates with feedback:



Op-Amp Inverting Amplifier - Labeled Inverting Input
circuitlab.com/c576qm3vwjhtp

Edit - Simulate

Ohm's Law gives us two equations for two voltage drops:

$$V_{\text{in}} - V_{\text{div}} = iR_{\text{in}}$$
$$V_{\text{div}} - V_{\text{out}} = iR_{\text{f}}$$

We can combine these two equations, eliminating the current i :

$$\frac{V_{\text{in}} - V_{\text{div}}}{R_{\text{in}}} = \frac{V_{\text{div}} - V_{\text{out}}}{R_{\text{f}}}$$

The ideal op-amp gives us one more equation, ensuring its two inputs to be equal:

$$V_{\text{div}} = 0$$

Substituting into the earlier equation, we find:

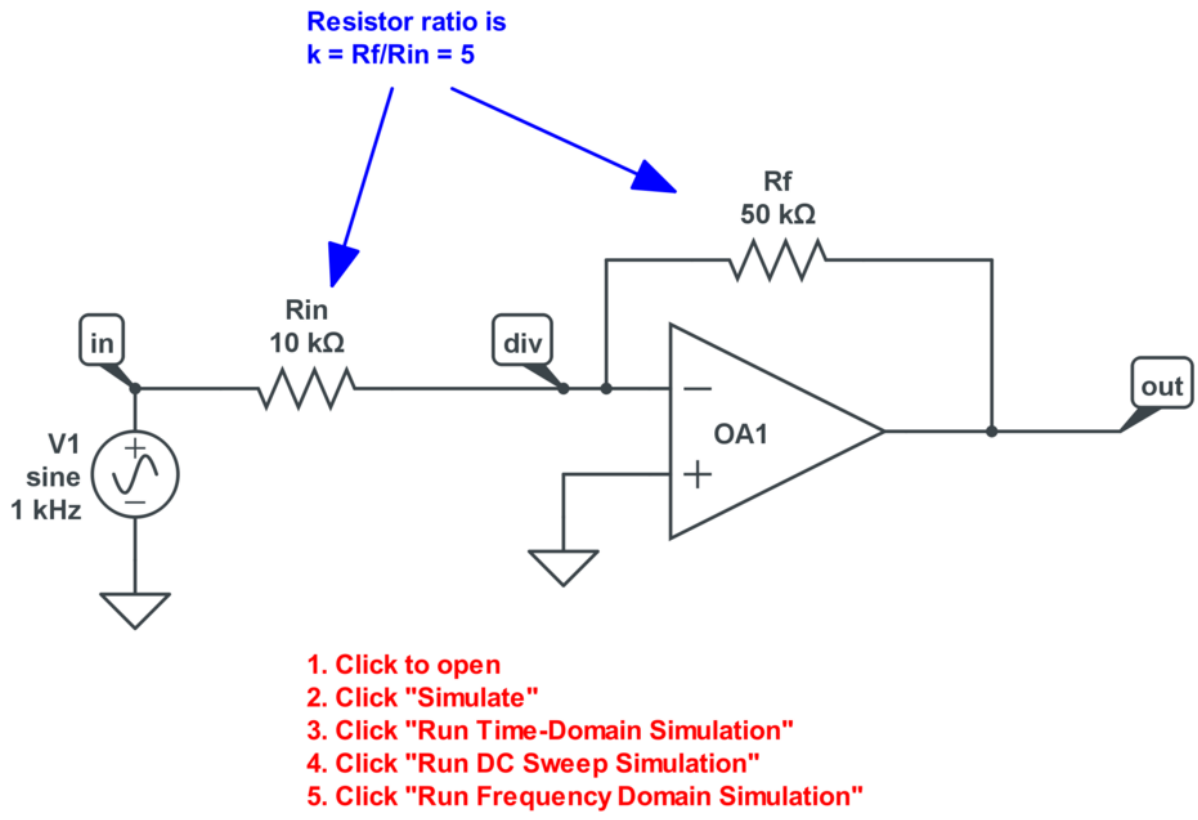
$$\frac{V_{\text{in}} - 0}{R_{\text{in}}} = \frac{0 - V_{\text{out}}}{R_{\text{f}}}$$
$$\frac{V_{\text{in}}}{R_{\text{in}}} = -\frac{V_{\text{out}}}{R_{\text{f}}}$$
$$A_v = \frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R_{\text{f}}}{R_{\text{in}}}$$

The voltage gain A_v is simply the negative ratio of the resistances, $-\frac{R_\text{f}}{R_\text{in}} = -k$. If $R_\text{f} > R_\text{in}$, then (in absolute value terms) the output amplitude will be larger than the input. This makes sense because the same current causes a larger voltage drop.

In any case, the gain will be negative, but any value $A_v \leq 0$ can be achieved with this arrangement. In contrast to the non-inverting amplifier, there is no inherent limitation as to whether the absolute signal magnitude gets larger or smaller in an inverting amplifier.

Example: Gain of -5 Amplifier

We can make a gain-of-negative-5 amplifier by setting the resistor ratio to $k = 5$. For example:



Op-amp Inverting Amplifier - Gain of -5 Example
circuitlab.com/c23xfs3587jd8 Edit - Simulate

Exercise Click to open and simulate the circuit above. What is the relationship between input and output sine waves?

The gain of the circuit shown is:

$$A_v = \frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R_{\text{f}}}{R_{\text{in}}} = -\frac{50\ \text{k}\Omega}{10\ \text{k}\Omega} = -5$$

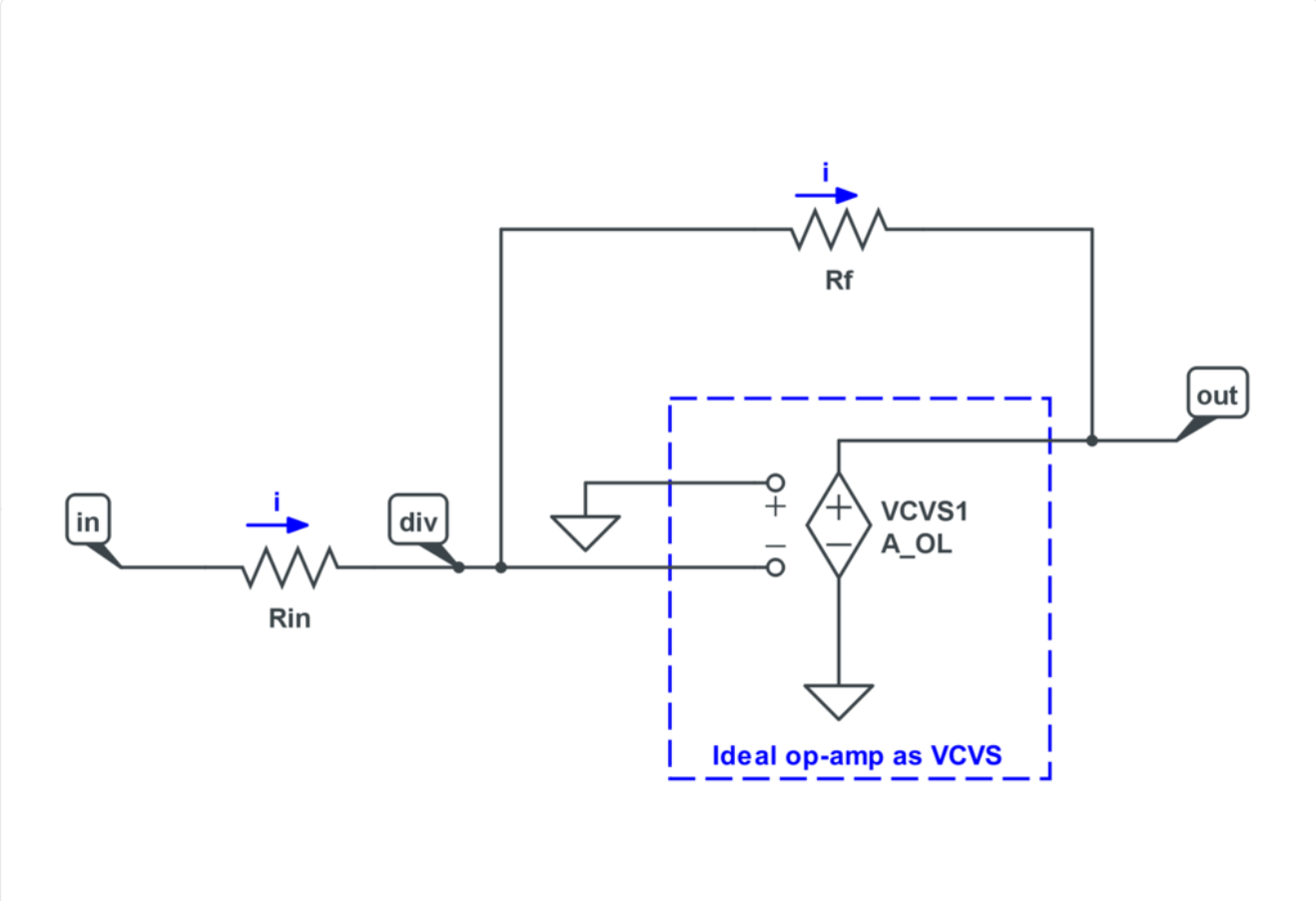
And the relationship between input and output is simply:

$$V_{\text{out}} = -5 \cdot V_{\text{in}}$$

VCVS Model

Instead of simply *assuming* that the op-amp closes the loop and makes its inputs equal as specified, let's look at the mechanism behind it. This reveals crucial limitations of the inverting amplifier.

We can model the op-amp as a voltage-controlled voltage source (VCVS) (as we did in The Ideal Op-Amp and earlier op-amp sections solving the voltage buffer, voltage reference, and non-inverting amplifier) to allow us to perform a more detailed analysis of how the inverting amplifier works:



Op-Amp Inverting Amplifier VCVS Model
circuitlab.com/c5kgdge4xjgq7

Edit - Simulate

The VCVS gives us one equation, an output proportional to the difference in its inputs

multipled by the open-loop gain A_{OL} :

$$V_{\text{out}} = A_{\text{OL}}\big(0 - V_{\text{div}}\big)$$
$$V_{\text{out}} = -A_{\text{OL}}V_{\text{div}}$$

Our Ohm's Law-derived ratio still applies as well:

$$\frac{V_{\text{in}} - V_{\text{div}}}{R_{\text{in}}} = \frac{V_{\text{div}} - V_{\text{out}}}{R_{\text{f}}}$$

We can combine this with the VCVS equation to eliminate $V_{\text{div}} = -\frac{1}{A_{\text{OL}}}V_{\text{out}}$ and solve for a relationship purely between input and output:

$$\begin{aligned}
\frac{V_{\text{in}} + \frac{1}{A_{\text{OL}}}V_{\text{out}}}{R_{\text{in}}} &= \frac{-\frac{1}{A_{\text{OL}}}V_{\text{out}} - V_{\text{out}}}{R_{\text{f}}} \\
\frac{1}{R_{\text{in}}}V_{\text{in}} &= -\Big(\frac{1}{R_{\text{f}}}(1 + \frac{1}{A_{\text{OL}}}) + \frac{1}{R_{\text{in}}A_{\text{OL}}}\Big)V_{\text{out}} \\
\frac{V_{\text{out}}}{V_{\text{in}}} &= -\frac{1}{R_{\text{in}}\big(\frac{1}{R_{\text{f}}}(1 + \frac{1}{A_{\text{OL}}}) + \frac{1}{R_{\text{in}}A_{\text{OL}}}\big)} \\
\frac{V_{\text{out}}}{V_{\text{in}}} &= -\frac{1}{R_{\text{in}}\frac{1}{R_{\text{f}}R_{\text{in}}A_{\text{OL}}}\big(R_{\text{in}}A_{\text{OL}}(1 + \frac{1}{A_{\text{OL}}}) + R_{\text{f}}\big)} \\
\frac{V_{\text{out}}}{V_{\text{in}}} &= -\frac{R_{\text{f}}A_{\text{OL}}}{R_{\text{in}}(A_{\text{OL}} + 1) + R_{\text{f}}}
\end{aligned}$$

For an ideal op-amp we take the limit $A_{\text{OL}} \to \infty$. In the denominator, this causes the insignificant terms $R_{\text{in}} + R_{\text{f}}$ to drop away, leaving us with:

$$A_v = \frac{V_{\text{out}}}{V_{\text{in}}} \approx -\frac{R_{\text{f}}}{R_{\text{in}}} = -k$$

This is the same gain we found earlier.

Maximum Gain

Is there a **maximum gain** we can get from an inverting amplifier? Note that when we took the limit $A_{\text{OL}} \to \infty$, the algebraic approximation we made in the denominator only holds because we assumed $R_{\text{in}}A_{\text{OL}} \gg R_{\text{in}} + R_{\text{f}}$. Let's take a closer look at this. We can clean up that assumption a bit:

$$\begin{aligned} R_{\text{in}} A_{\text{OL}} &\gg R_{\text{in}} + R_{\text{f}} \\ A_{\text{OL}} &\gg \frac{R_{\text{in}} + R_{\text{f}}}{R_{\text{in}}} \\ A_{\text{OL}} &\gg 1 + \frac{R_{\text{f}}}{R_{\text{in}}} \\ A_{\text{OL}} &\gg 1 + k \end{aligned}$$

This tells us that our gain assumption holds only if one plus our design gain (the resistor ratio k) is much smaller than the open-loop gain of the op-amp.

We can find the maximum gain algebraically by rewinding to the last equation just before we took the limit $A_{\text{OL}} \to \infty$:

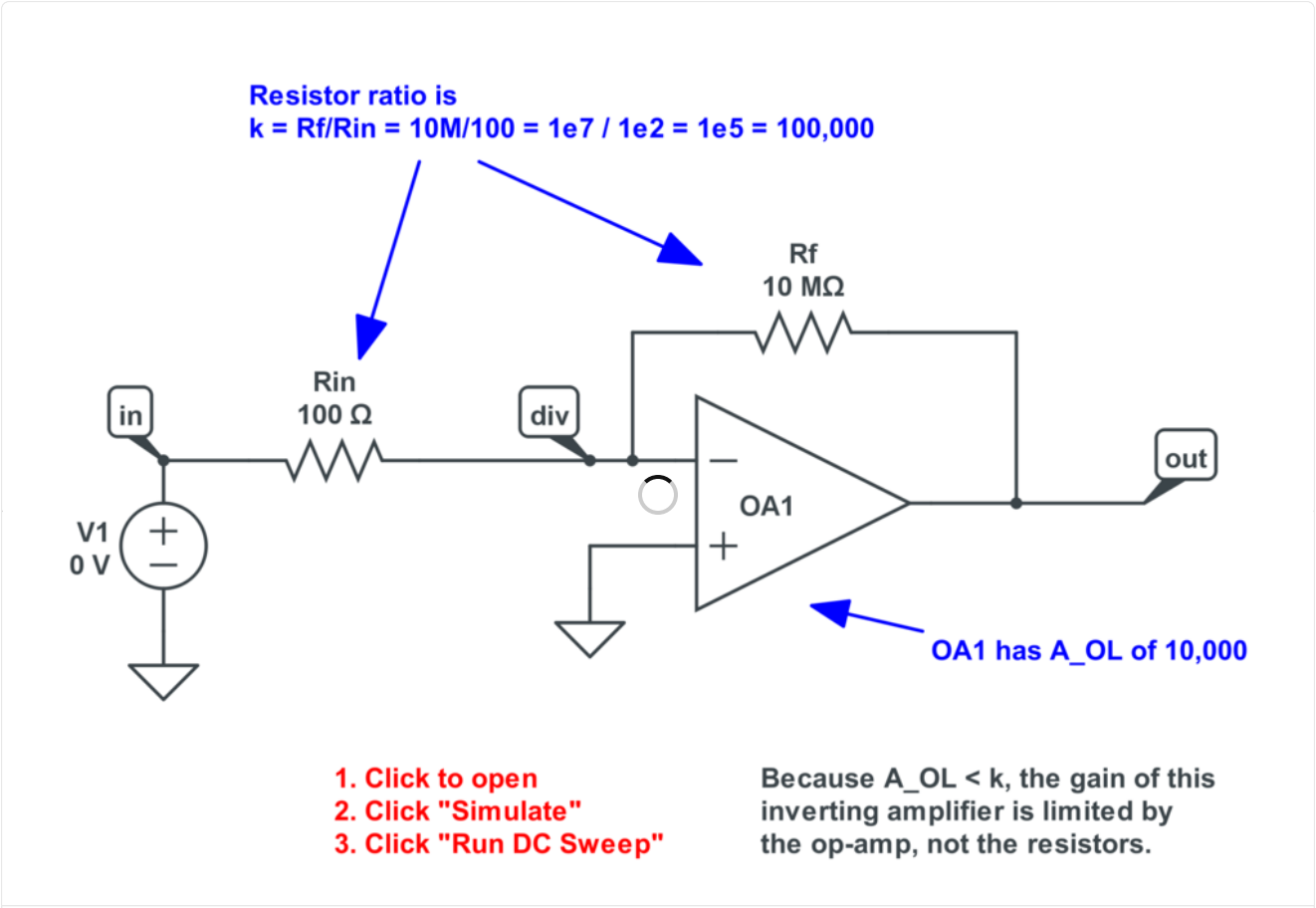
$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R_{\text{f}} A_{\text{OL}}}{R_{\text{in}}(A_{\text{OL}} + 1) + R_{\text{f}}}$$

This time, let's make a different assumption. Let's assume the opposite condition is true: now, let's assume the design gain $k = \frac{R_{\text{f}}}{R_{\text{in}}}$ is now much *larger* than the op-amp's open-loop gain, $(k \gg A_{\text{OL}})$ and see what happens:

$$\begin{aligned} \frac{V_{\text{out}}}{V_{\text{in}}} &= -\frac{R_{\text{f}} A_{\text{OL}}}{R_{\text{in}}(A_{\text{OL}} + 1) + R_{\text{f}}} \\ \frac{V_{\text{out}}}{V_{\text{in}}} &= -\frac{\frac{R_{\text{f}}}{R_{\text{in}}} A_{\text{OL}}}{(A_{\text{OL}} + 1) + \frac{R_{\text{f}}}{R_{\text{in}}}} \\ \frac{V_{\text{out}}}{V_{\text{in}}} &= -\frac{k A_{\text{OL}}}{(A_{\text{OL}} + 1) + k} \\ \frac{V_{\text{out}}}{V_{\text{in}}} &\approx -\frac{k A_{\text{OL}}}{k} \\ \frac{V_{\text{out}}}{V_{\text{in}}} &\approx -A_{\text{OL}} \end{aligned}$$

If we use an op-amp with finite open-loop gain, as all real-world op-amps have, then our ability to build an inverting amplifier is limited to approximately the (negative) open-loop gain of the op-amp.

This is demonstrated through simulation here:



Op-Amp Inverting Amplifier - Limited by Open-Loop Gain
circuitlab.com/ctjm6t325a9he

Edit - Simulate

Exercise Click to open and simulate the circuit above. On the DC Sweep plot, what is the slope of the line for V_{out} (y-axis) vs. V_{in} (x-axis)?

We can't use an op-amp with $A_{\text{OL}} = 10^4$ to make an inverting amplifier with $k = 10^5$ (a gain of $A_v = -10^5$). If we truly needed this much gain, we need to either find an op-amp with higher open-loop gain, or split the amplification up into multiple stages. Something similar happened in the math for the non-inverting amplifier.

Input Impedance

It's important to understand the input and output impedance of amplifier stages to maximize signal transfer and minimize interstage loading.

When we examined the non-inverting amplifier in the previous section, we didn't talk about input impedance because the input source is connected directly to an op-amp input. No current flows into an op-amp input, so the input impedance of the non-inverting amplifier is infinite.

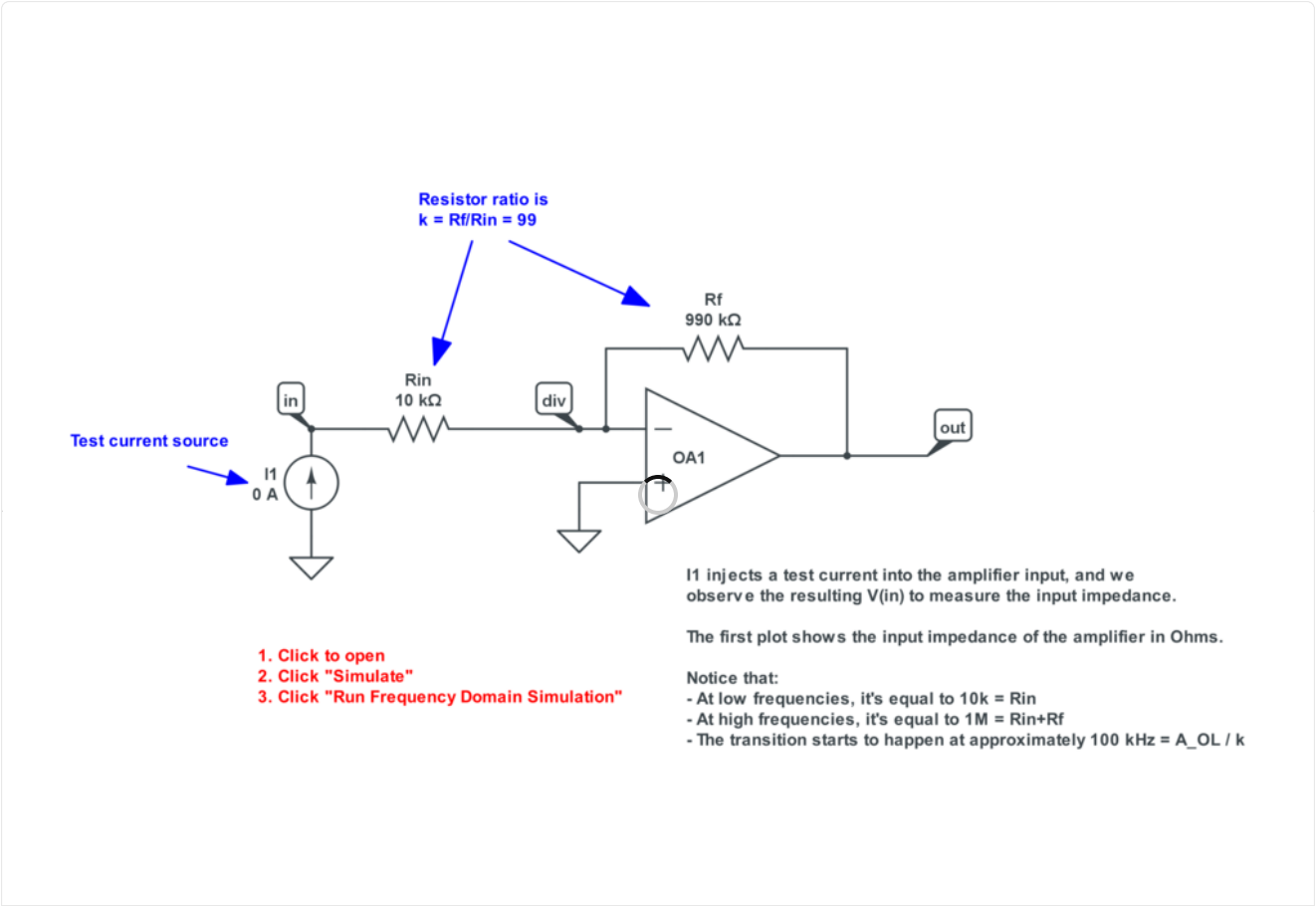
However, one hugely significant difference between the inverting amplifier and the non-inverting amplifier is that **the inverting amplifier has finite input impedance**. This is significant because if the previous stage has finite output impedance, then you'll lose some signal connecting these two stages.

One way to avoid this is to add an op-amp voltage buffer just before the inverting amplifier. This comes at a cost of an extra op-amp and extra power consumption, but it does mean that the behavior of our circuit is no longer dependent on the previous stage's output impedance.

Quantitatively, just how big is the input impedance?

- If we're measuring at frequencies slow enough that the op-amp has time to close the feedback loop and keep the inverting input as a virtual ground, then we only see R_{in} when looking into the overall circuit's input in the Thevenin Equivalent Circuit sense.
- If we're measuring at frequencies faster than that, the op-amp hasn't had time to keep its inverting input voltage fixed. Instead, the op-amp's output could be considered fixed, because at high frequencies, it doesn't have time to change voltage. In this case, we'll see $R_{\text{in}} + R_{\text{f}}$ looking into the overall circuit's input. (We'd also add the op-amp output impedance, but we'll ignore this for now.)

We can demonstrate that the input impedance is R_{in} for low frequencies and $R_{\text{in}} + R_{\text{f}}$ for high frequencies through a simple input impedance simulation:



Op-Amp Inverting Amplifier - Input Impedance Simulation
circuitlab.com/c7gvkuez25b24 Edit - Simulate

Exercise Click to open and simulate the circuit above. Observe the transition between two flat input impedances. What are the levels of the two flat sections? When does the transition start to happen?

In this circuit, I1 is a test current source, set to 0 at DC but used as an AC signal source for small-signal frequency-domain analysis. We can look at the magnitude and phase of the resulting voltage at V_{in} and this gives us a complex impedance for each frequency.

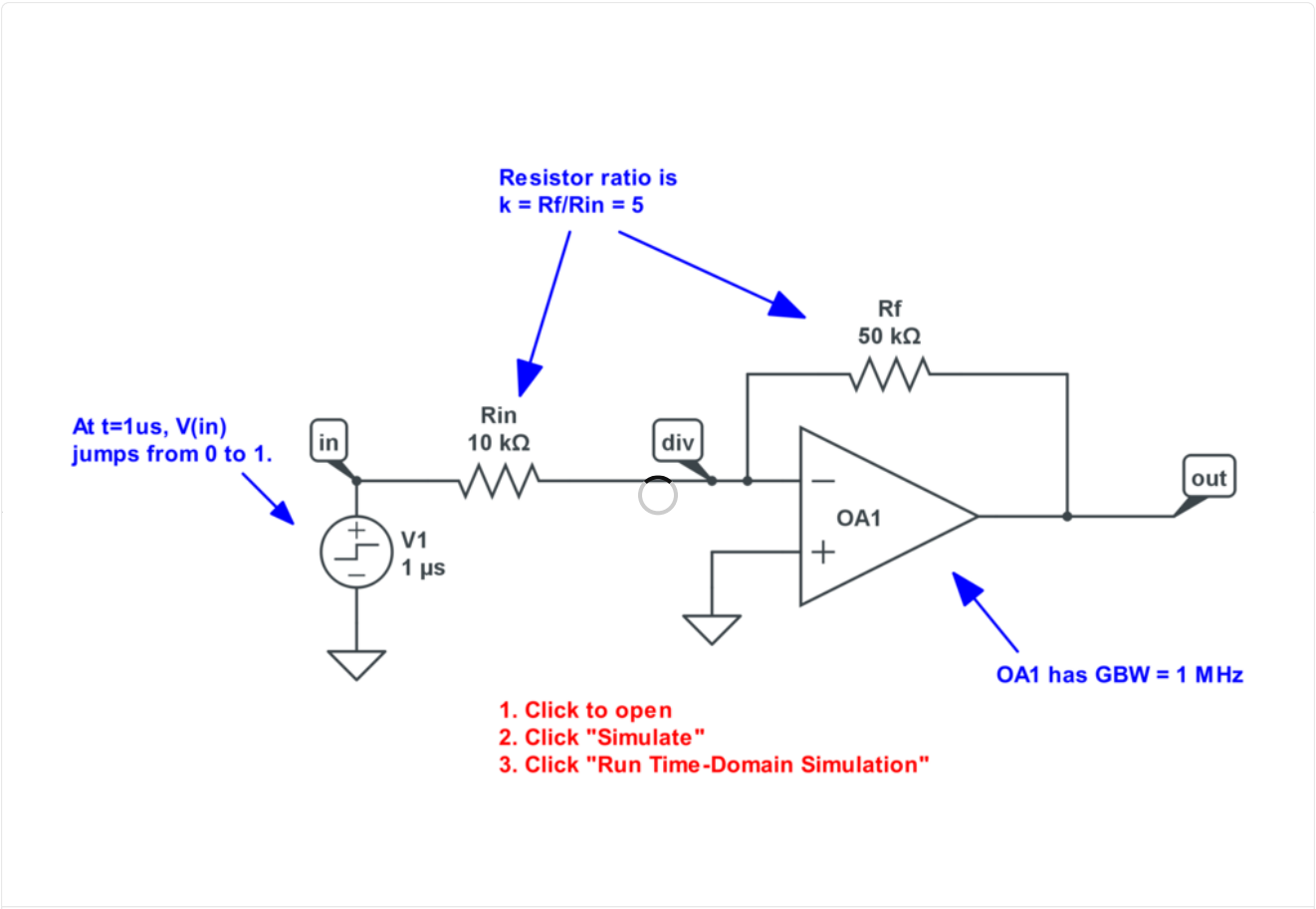
The input impedance of the inverting amplifier configuration is quite unusual, but it's useful to see how easy it is to understand and simulate for two reasons:

- The input impedance of the inverting amplifier affects your choice of absolute resistor values, discussed later in this section.
- Other more complex circuits will have different input or output impedance behavior, and it's easier to start by learning how to analyze and design around a simple case like this one.

Step Response

The input impedance's transition between not-yet-virtual-ground at high frequencies to virtual ground at low frequencies hints at the inverting amplifier's interesting **step response** as it restabilizes. Observing the step response, whether through an oscilloscope or a simulation, helps show that the **"virtual ground" is an illusion of feedback that only applies at low frequencies**.

Let's put a unit voltage step into our gain-of-negative-five inverting amplifier:



Op-Amp Inverting Amplifier - Step Response
circuitlab.com/c5493kmczatef

Edit - Simulate

Exercise Click to open and simulate the circuit above. The most interesting trace to look at is V_{div} .

Immediately after the step from 0 to 1 in V_{in} , the op-amp hasn't had time to respond yet, so $V_{\text{out}} = 0$ as it was before the step. This leaves R_{in} and R_{f} to form a voltage divider, causing $V_{\text{div}} = V_{\text{in}} \cdot \frac{50\ \text{k}\Omega}{10\ \text{k}\Omega + 50\ \text{k}\Omega} = \frac{5}{6} \approx 0.833\ \text{V}$.

After the step, the op-amp observes a difference in its inputs and begins reducing its output

voltage until the inputs are equal again.

This does not happen instantaneously. We've configured the op-amp in the simulation to have a gain-bandwidth product of $\mathrm{GBW} = 1\ \mathrm{MHz}$, and you can observe that it takes several microseconds for the op-amp to settle to within a few percent of its final output value. (Microseconds may sound short, but it's a long time in electronics: if the signal you care about is changing fast enough, you're in trouble!)

As an exercise: replace the step voltage source V1 with a square wave source. See what happens as you drive the inverting amplifier at various frequencies from $1\ \mathrm{kHz}$ to $1\ \mathrm{MHz}$. (You'll have to adjust the simulation stop time and time step proportionally to get a good view as you change the input frequency.)

If you drive the inverting amplifier so fast that it doesn't have time to close the feedback loop and bring the virtual ground node back to where it belongs, then the amplifier won't do what we've intended. **If you are relying on a virtual ground, you have to be patient.** Unlike a real ground, a virtual ground is only a low-impedance point when you move slowly.

Frequency Response and the Gain-Bandwidth Product

Just as with the non-inverting amplifier configuration, our op-amp's open-loop gain drops at high frequencies, limiting the effective bandwidth of the amplifier.

As we did for the non-inverting amplifier, we'll replace the op-amp's gain A_{OL} with $G(s)$, the complete expression for the open-loop ideal op-amp Laplace transfer function:

$$G(s) = \frac{A_{\mathrm{OL}}}{1 + s\left(\frac{A_{\mathrm{OL}}}{2\pi \mathrm{GBW}}\right)}$$

This expression includes the open-loop gain A_{OL} which covers DC and low frequencies, and it includes a low-pass filter which drops off following the gain-bandwidth product GBW.

We can substitute this into our inverting amplifier VCVS model, inserting $G(s)$ in place of the DC-only A_{OL}:

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = -\frac{R_{\text{f}}G(s)}{R_{\text{in}}(G(s)+1)+R_{\text{f}}}$$

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = -\frac{R_{\text{f}}\frac{A_{\text{OL}}}{1+s\left(\frac{A_{\text{OL}}}{2\pi\text{GBW}}\right)}}{R_{\text{in}}\left(\frac{A_{\text{OL}}}{1+s\left(\frac{A_{\text{OL}}}{2\pi\text{GBW}}\right)}+1\right)+R_{\text{f}}}$$

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = -\frac{R_{\text{f}}A_{\text{OL}}}{R_{\text{in}}\left(A_{\text{OL}}+1+s\left(\frac{A_{\text{OL}}}{2\pi\text{GBW}}\right)\right)+R_{\text{f}}\left(1+s\left(\frac{A_{\text{OL}}}{2\pi\text{GBW}}\right)\right)}$$

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = -\frac{R_{\text{f}}A_{\text{OL}}}{\left(R_{\text{in}}A_{\text{OL}}+R_{\text{in}}+R_{\text{f}}\right)+s\left(\frac{A_{\text{OL}}(R_{\text{in}}+R_{\text{f}})}{2\pi\text{GBW}}\right)}$$

In the denominator, let's use the fact that $R_{\text{in}}A_{\text{OL}} \gg (R_{\text{in}}+R_{\text{f}})$ to simplify. This will enable us to start substituting in the design gain $k = \frac{R_{\text{f}}}{R_{\text{in}}}$ for simplification as well:

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} \approx -\frac{R_{\text{f}}A_{\text{OL}}}{R_{\text{in}}A_{\text{OL}}+s\left(\frac{A_{\text{OL}}(R_{\text{in}}+R_{\text{f}})}{2\pi\text{GBW}}\right)}$$

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} \approx -\frac{R_{\text{f}}}{R_{\text{in}}+s\left(\frac{R_{\text{in}}+R_{\text{f}}}{2\pi\text{GBW}}\right)}$$

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} \approx -\frac{k}{1+s\left(\frac{R_{\text{in}}+R_{\text{f}}}{2\pi\text{GBW}R_{\text{in}}}\right)}$$

To simplify this denominator, we can observe that $\frac{R_{\text{f}}+R_{\text{in}}}{R_{\text{in}}} = k+1$:

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} \approx -\frac{k}{1+s\left(\frac{k+1}{2\pi\text{GBW}}\right)}$$

This overall transfer function consists of a gain $-k$ at DC and low frequencies, multiplied by a one-pole low-pass filter. Following the same method we solved in detail in the previous section, the corner frequency can be found by determining where the imaginary part of the denominator is equal in magnitude to the real part. (Review that section to see us work through the almost-identical math.)

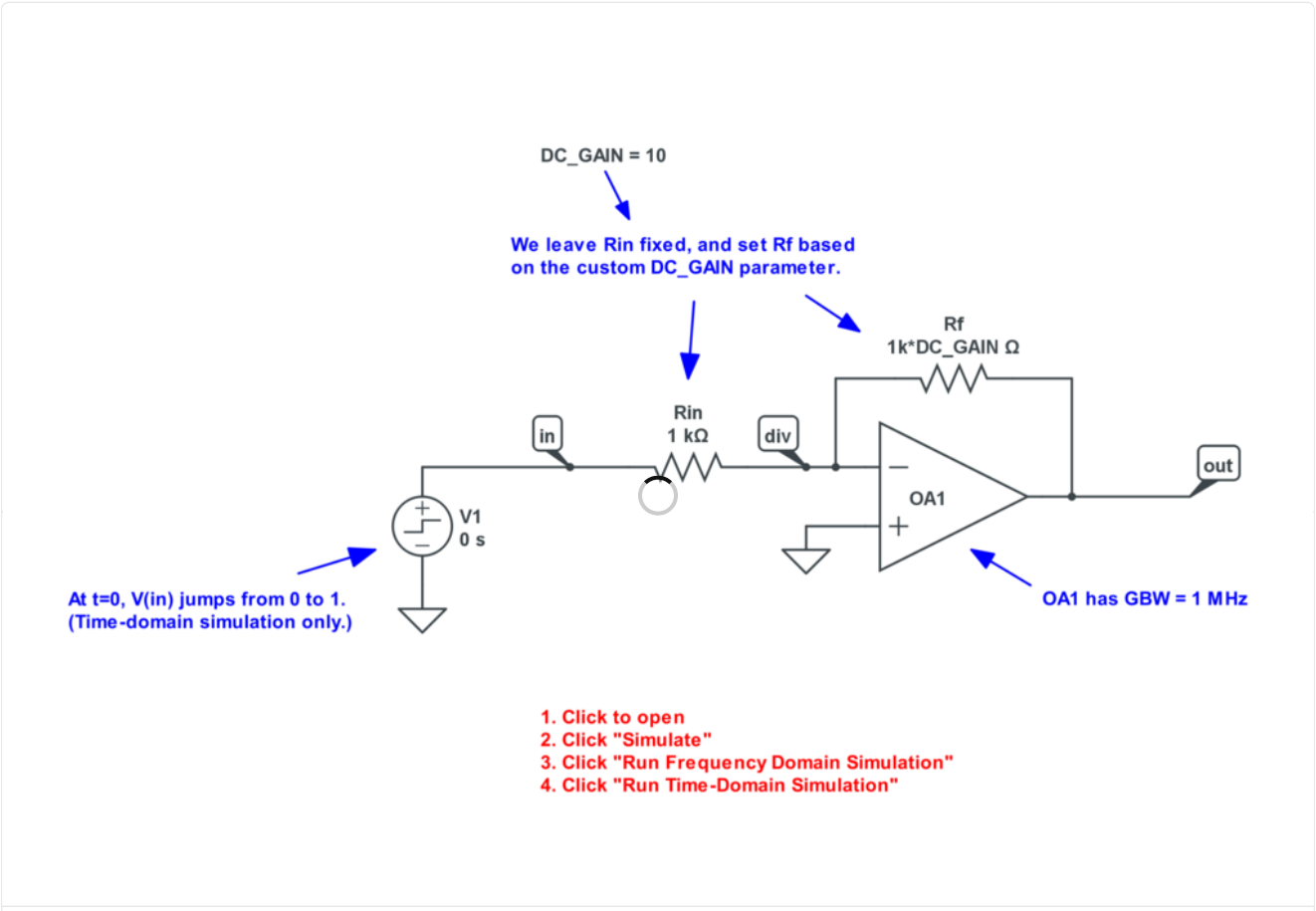
The result is that the amplifier's closed-loop corner frequency f_c is:

$$f_c = \frac{\text{GBW}}{k+1}$$

This is almost identical to the corner frequency we found for the non-inverting amplifier, which had $f_c = \frac{\text{GBW}}{k}$. The modification of the denominator to $k+1$ is significantly different only at low values of gain.

- If the gain $k = 10$ and the $\text{GBW} = 10^6\ \text{Hz}$, then
  $f_c = \frac{10^6\ \text{Hz}}{10+1} = 9.1 \times 10^4\ \text{Hz} = 91\ \text{kHz} \approx 100\ \text{kHz}$
- If the gain $k = 100$ and the $\text{GBW} = 10^6\ \text{Hz}$, then
  $f_c = \frac{10^6\ \text{Hz}}{100+1} = 9.9 \times 10^3\ \text{Hz} = 9.9\ \text{kHz} \approx 10\ \text{kHz}$
- If the gain $k = 1000$ and the $\text{GBW} = 10^6\ \text{Hz}$, then
  $f_c = \frac{10^6\ \text{Hz}}{1000+1} = 9.99 \times 10^2\ \text{Hz} = 999\ \text{Hz} \approx 1\ \text{kHz}$

We can demonstrate this easily in a simulation where we take an op-amp with $\text{GBW} = 1\ \text{MHz}$ and configure it as an inverting amplifier with various levels of gain:



Op-Amp Inverting Amplifier - Gain vs. Bandwidth Tradeoff
circuitlab.com/cm5yf4gjyqf4t

Edit - Simulate

Exercise Click to open and simulate the circuit above. We've asked the simulator to re-run this circuit for DC_GAIN = 1, 10, 100, 1000, 10000, and 100000. Try the frequency domain simulation. As we step up the gain by a factor of 10 each time (plotted on a decibel log scale y-axis, so they're plotted evenly spaced $+20\ \mathrm{dB}$ steps), what happens to the $-3\ \mathrm{dB}$ corner frequency of the amplifier's response?

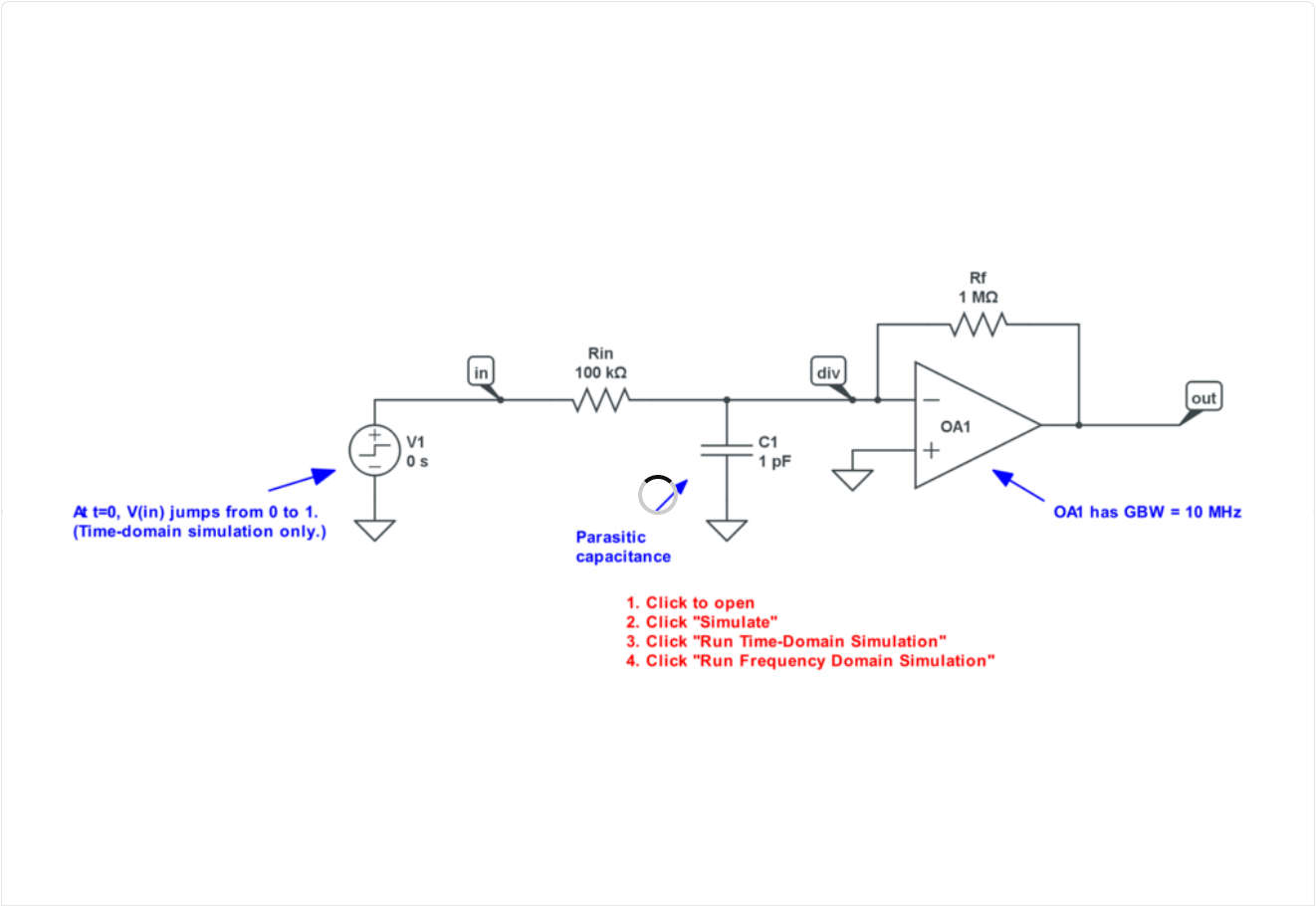
Again, the gain-bandwidth product is not magic. It's simply a way of saying that as we ask the amplifier to do more amplification, it takes longer to get there! **There is a direct tradeoff between amplification and bandwidth (frequency)**, and it's captured as the **gain-bandwidth product (GBW)**.

If you need more gain or more bandwidth than the op-amp's gain-bandwidth product allows, the solutions are the same as already discussed for the non-inverting amplifier, so we won't repeat them here.

Stability and Compensation

Just as we discussed on the non-inverting amplifier, there is parasitic capacitance everywhere, and we have to be most concerned about it at high-impedance nodes like V_{div} .

Let's see what happens to the step response of a gain-of-negative-10 amplifier with various levels of parasitic capacitance:



Op-Amp Inverting Amplifier - Instability due to Parasitic Capacitance
circuitlab.com/c8x5srsmhd6zg Edit - Simulate

Exercise Click to open and simulate the circuit above. How much parasitic capacitance does it take to start seeing **overshoot** in the step response? How about **ringing**?

As the simulation demonstrates, it takes just picofarads of unintentional capacitance to cause serious overshoot or ringing. Both of these are usually undesired because they distort the signal that's passing through.

It isn't just the step response that is compromised. If you run the frequency-domain simulation, you'll see that overshoot and ringing correspond to peaking in the magnitude plot of the frequency response: some small range of frequencies are amplified by *more* than our design gain because of unintented resonant behavior.

As an exercise, add `,500p` to the end of the custom sweep list for C1.C. Increase the simulation stop time to `40u`. What happens to the step response? This demonstrates why this issue is called **instability**, because the op-amp is very nearly unstable and prone to oscillating indefinitely.

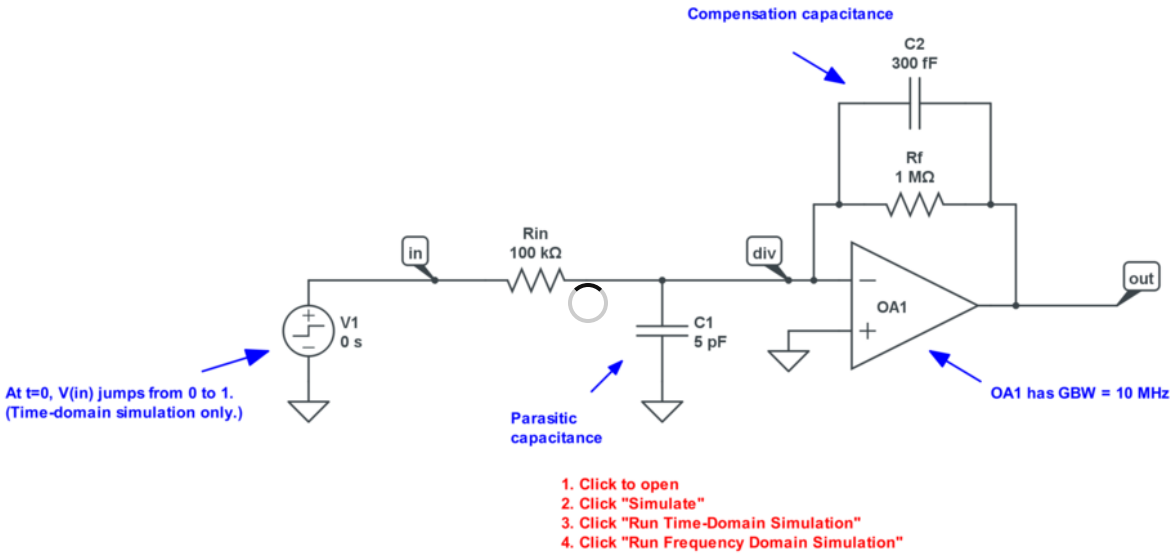
As another exercise, try making both resistors smaller by a factor of 0.1. Does this help or hurt?

As another exercise, try changing the GBW of the op-amp.

As discussed on non-inverting amplifiers, there are a few ways of mitigating this stability problem:

1. Layout the physical circuit to reduce parasitic capacitance.
2. Use smaller resistances. (For the same capacitance, this pushes the effect of the capacitor out to higher frequencies.) This comes at a cost of increased power consumption and greater sensitivity to the input source impedance.
3. Use a slower op-amp (lower GBW). This comes at a cost of slower responses in exchange for stability.
4. Compensation.

Compensation means modifying the circuit slightly by adding components that counteract the undesired parasitic effects. We demonstrated feed-forward compensation in detail on the non-inverting amplifier. We can do something similar for the inverting amplifier, adding a capacitor C_2 in parallel with R_f :



Op-Amp Inverting Amplifier - Compensation Capacitor
circuitlab.com/cdr6eey9rx4hn

Edit - Simulate

Exercise Click to open and simulate the circuit above. The simulator is set to try a range of different values for C2. Which value gives the best step response (little ringing or overshoot)? What happens if C2 is much larger or much smaller than that?

We can't give a general formula for the size of the compensation capacitor. It depends on too many factors, including the resistances, the gain-bandwidth product, and the parasitic capacitance. That's why we use simulation to determine the best value.

In this particular case, with parasitic capacitance $C_1 = 5\ \text{pF}$, it looks like we get the best step response somewhere in the neighborhood of $C_2 \approx 0.3 \pm 0.05\ \text{pF}$. If C2 is much smaller than that, it doesn't do enough and we still get ringing and overshoot. If C2 is much larger than that, we eliminate ringing, but it also slows down the step response considerably.

Somewhere around 0.3 pF is optimal, but this is a *tiny* amount of capacitance. It may even be present unintentionally due to parasitic capacitance in your physical circuit, simply from the PCB traces of the output and inverting input being in close proximity. At high frequencies, tiny amounts of capacitance matter, and if your op-amp is fast enough (high GBW), you're dealing

with high frequencies whether your signal needs them or not!

One reason that only a tiny capacitance is required here is because the two ends of the compensation capacitor are connected to voltages that are naturally moving in opposite directions: as V_{div} rises, V_{out} falls because of the op-amp. This means that even a small voltage change at the high-impedance side actually drives a large voltage change across the capacitor. This is called the **Miller effect**.

This can be hard to understand, but to a first order, we can think about the parasitic capacitance C_1 as adding charge stored at the inverting input node V_{div} . To increase V_{div} by $+\Delta V$, we need to store charge $\Delta Q_1 = C_1 \Delta V$. It takes time for this charge storage to happen, which is what causes the ringing and oscillation in the first place. (This is discussed in greater detail in the corresponding non-inverting amplifier section.)

To some degree, we can think of the compensation capacitor C_2 as trying to cancel out or *remove* that charge so that the circuit behaves overall more like the one without any parasitic capacitance. When V_{in} rises by $+\Delta V_{\text{in}}$, then *eventually* V_{out} changes by $-k\Delta V_{\text{in}}$, which requires charge $\Delta Q_2 = kC_2 \Delta V_{\text{in}}$ to flow into the capacitor. Note that the capacitance is multiplied by the gain, $C_{\text{eff}} = kC_2$. This is the **Miller multiplication** effect at work!

A lot of transient behavior is hidden in the word “eventually” as the op-amp circuit settles to its new steady-state, but at a high level:

- Parasitic capacitance C_1 makes the step response *worse* by requiring *more charge storage* at the high impedance node V_{div} .
- Compensation capacitor C_2 *improves* the shape of the step response by *more rapidly removing charge* from this node.

Compensation is advanced analog magic, but it’s important if you care about building high-performance analog circuits. If you design op-amp circuits and find you have oscillation, overshoot, or ringing, remember this section and revisit it. You’ll find other compensation methods in the literature as well. My overall advice would be to pay special attention to high-impedance nodes and simulate step responses to quickly see the effects of parasitics and compensation.

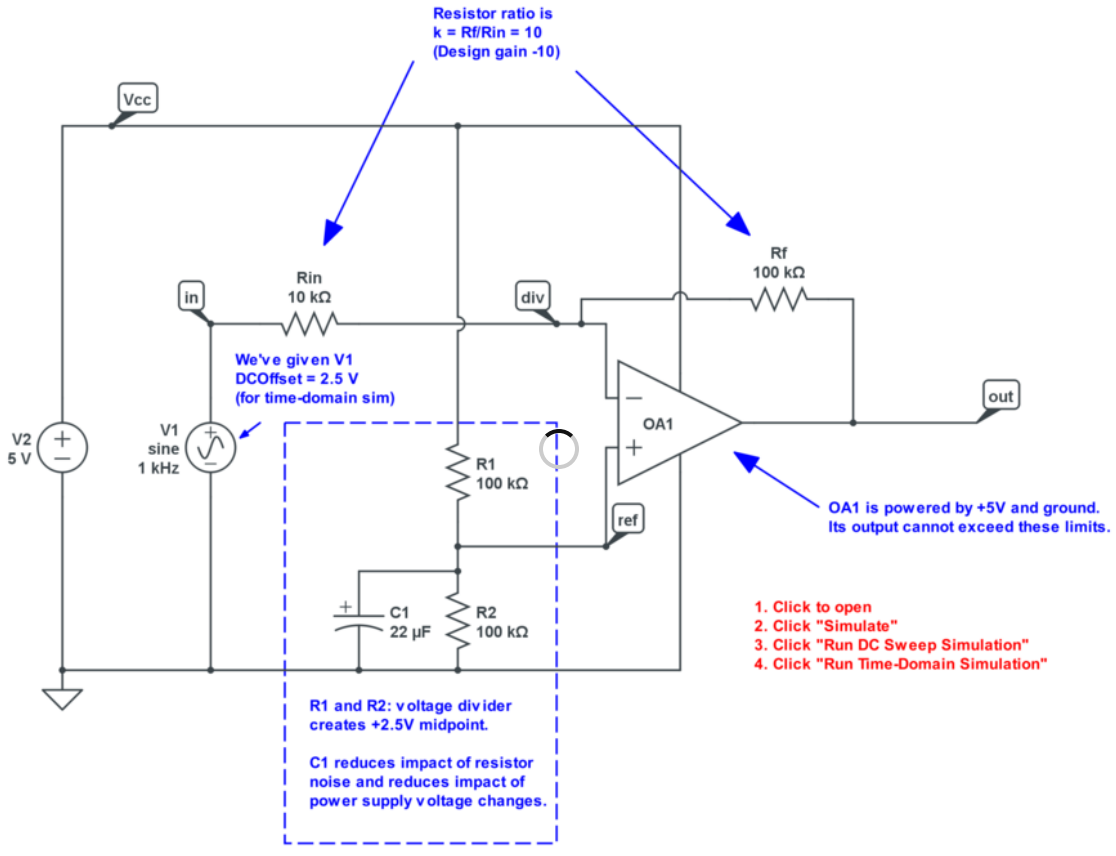
Offsetting the Virtual Ground

All of the examples show the op-amp's non-inverting input (+) connected to ground, but it's quite common for it to be connected to a different DC voltage V_{ref} instead.

One common case is in **single supply** systems, where we have a positive power rail but no negative one. In that case, you may wish to have everything be relative to a midpoint between ground and the positive rail, in order to maximize the available range symmetric around this new reference midpoint. The midpoint itself could be generated by a voltage divider or by an op-amp voltage reference.

Since the midpoint is connected to the op-amp's non-inverting input and is otherwise unloaded, it's not necessary to have a particularly low impedance source. However, adding a **decoupling capacitor** can help reduce resistor noise and improve **power supply rejection**.

An example of a 5V single-supply circuit with a gain-of-negative-10 amplifier anchored at the midpoint is shown here:



Op-Amp Inverting Amplifier - Single-Supply
circuitlab.com/c65s8x3e2je9e

Edit - Simulate

Exercise Click to open and simulate the circuit above. Run the DC Sweep simulation and

observe three piecewise-linear segments. Does this shape match your expectation?

(If you run the time-domain simulation, note that we've given V1 a DC offset of 2.5V. We'll talk about this under AC Coupling just below.)

A ground is always an arbitrary choice of a voltage. Moving the non-inverting input's voltage only changes our equations slightly. Now, we have:

$$V_{\text{out}} = V_{\text{ref}} - k\big(V_{\text{in}} - V_{\text{ref}}\big)$$

If $V_{\text{ref}} = 0$ as we assumed when the non-inverting input was grounded, this simplifies to the same equation we had above:

$$\begin{aligned} V_{\text{out}} &= 0 - k\big(V_{\text{in}} - 0\big) \\ V_{\text{out}} &= -kV_{\text{in}} \\ \frac{V_{\text{out}}}{V_{\text{in}}} &= -k \end{aligned}$$

When $V_{\text{ref}} \neq 0$, it no longer makes sense to look at the large-signal ratio $\frac{V_{\text{out}}}{V_{\text{in}}}$. Instead, we can look at changes, where $\frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} = -k$ still applies.

In the circuit above, we've used a resistive voltage divider to create $V_{\text{ref}} = 2.5\ \text{V}$.

We've also added a capacitor $C_1 = 22\ \mu\text{F}$. In combination with the voltage divider resistors, this forms an RC high-pass filter with a time constant of $\tau = (R_1 // R_2)C_1 = 50\ \text{k}\Omega \cdot 22\ \mu\text{F} = 1.1\ \text{s}$. (If it isn't clear why to considers the resistors in *parallel*, review the Thevenin Equivalent of the Voltage Divider.) This time constant is quite long. It corresponds to a cutoff frequency of $f_c = \frac{1}{2\pi\tau} \approx 0.14Hz$. Short-duration (high-frequency) noise from the resistors, or high-frequency noise from the power supply itself, is substantially reduced by adding the capacitor.

If you run the time-domain simulation, you'll see that we've configured the function generator source V1 to produce a small sine wave centered around the midpoint. This is configured by V1's `DCOffset` parameter. You can try changing it to see the effect that the DC offset has on the output.

As an exercise: what happens if you increase the amplitude of signal source V1? How big can it be before you experience clipping of the output signal due to the op-amp's limited power supply range?

AC Coupling

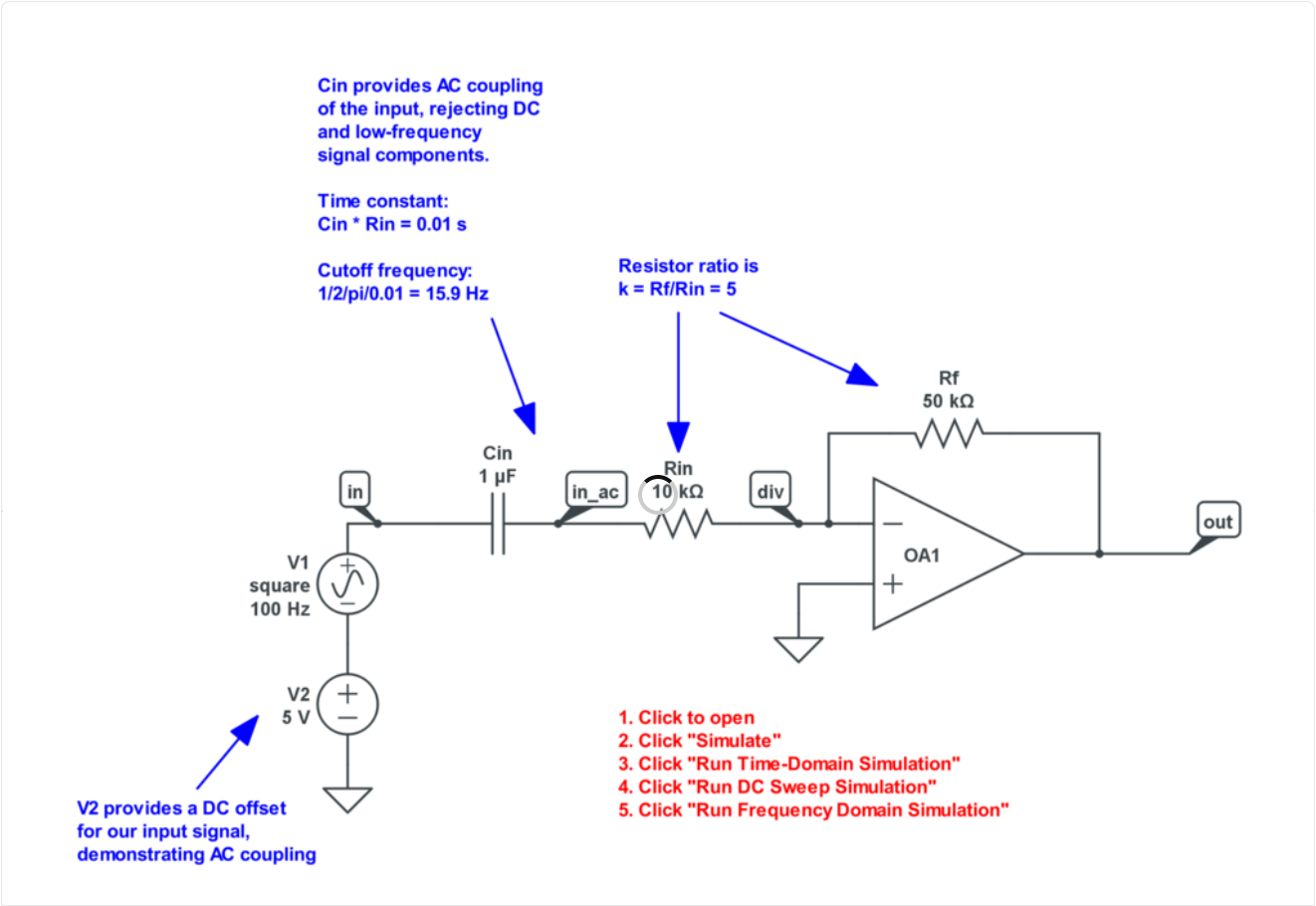
We can add a capacitor C_{in} in series with R_{in} . (The order does not matter.)

For a system at DC steady state, no current can flow through a capacitor because the flow of current would cause charge to accumulate, causing a change in voltage, which is disallowed at DC.

To see this mathematically, note that the capacitor equation $Q = CV$ implies $\frac{dV}{dt} = \frac{1}{C}\frac{dQ}{dt} = \frac{1}{C}i_C(t)$, and since $\frac{d}{dt} = 0$ at DC steady state, we must have $i_C(t) = 0$.

At DC, one plate of the capacitor is driven by the DC value of the signal input. The other plate is connected to the virtual ground V_{div} through the resistor R_{in} , but there is no DC current and so no voltage drop across R_{in} . Effectively, the capacitor charges up to perfectly cancel out the DC level of V_{in} .

If we now allow the input signal to change, an instantaneous step input change ΔV_{in} creates an equal instantaneous change $\Delta V_{\text{in\_ac}}$, because the voltage drop across the capacitor can't change without time to charge or discharge it. Input signals that change fast enough are allowed to pass through the capacitor, while slow signals are diminished.



Op-Amp Inverting Amplifier - AC Coupling
circuitlab.com/cf6ypt432etz2 Edit - Simulate

Exercise Click to open and simulate the circuit above. The results may surprise you!

The input capacitor C_{in} forms an RC high-pass filter, where the resistance is equal to the input impedance of the amplifier. As discussed earlier, the input impedance of the inverting amplifier is quite interesting, but for frequencies where the op-amp maintains the virtual ground, the input impedance is simply equal to R_{in} .

In the circuit shown here, we have an RC time constant $\tau = C_{\text{in}}R_{\text{in}} = 1\ \mu\text{F} \cdot 10\ \text{k}\Omega = 0.01\ \text{s}$. This corresponds to a high-pass filter cutoff frequency of $f_c = \frac{1}{2\pi\tau} \approx 15.9\ \text{Hz}$.

Qualitatively, the behavior of the capacitor looks very different for low-frequency and high-frequency changes in V_{in} :

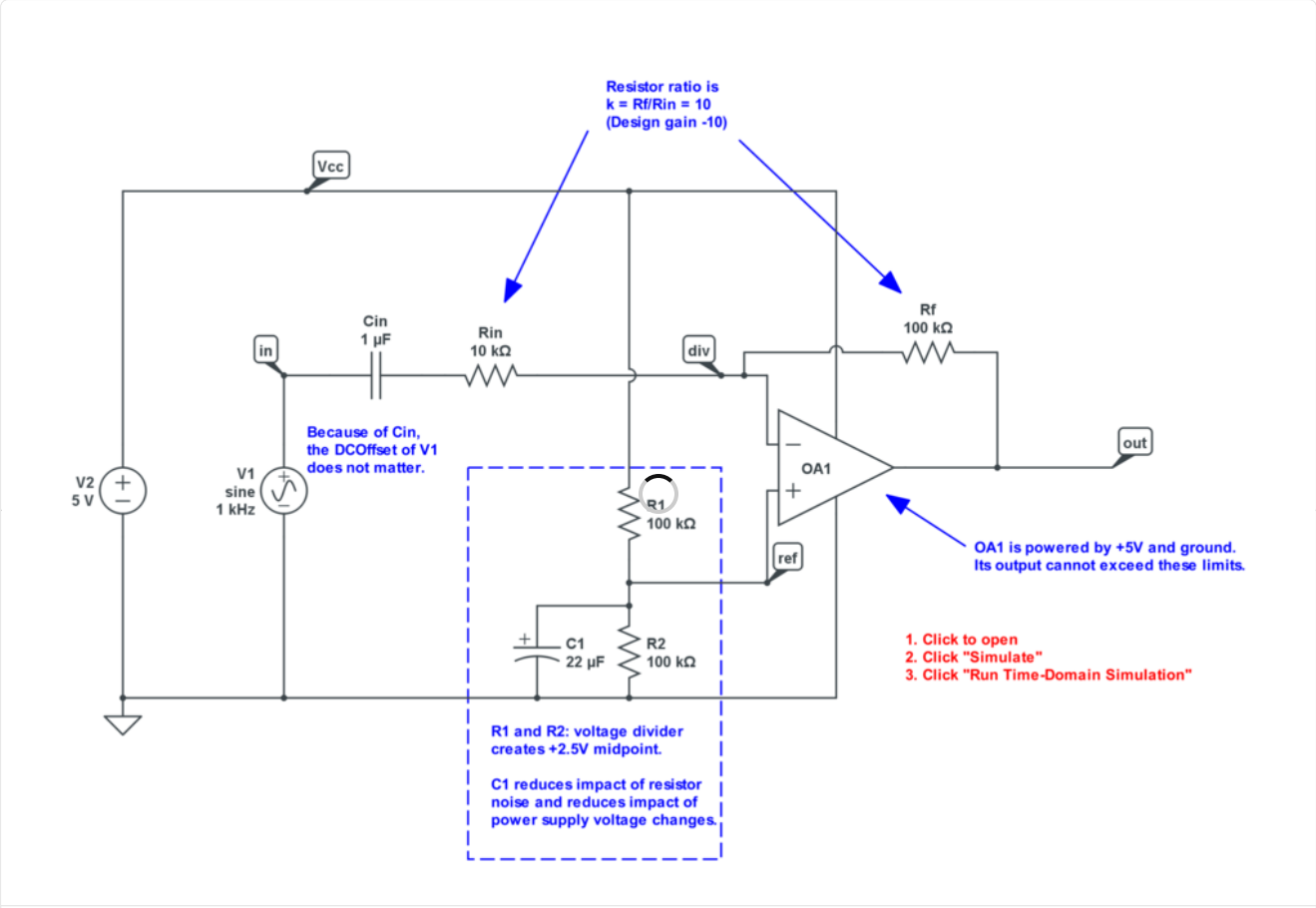
- $f \ll f_c$: Signals much slower than f_c will be **absorbed by changes in voltage across the capacitor**, having little to no effect on $V_{\text{in\_ac}}$.
- $f \gg f_c$: Signals much faster than f_c will be **copied almost 1:1 across the capacitor**, changing $V_{\text{in\_ac}}$. They're too fast to cause the capacitor to charge or discharge much.

AC coupling is a useful technique when the signal you care about isn't carried in the DC signal. Any DC signal offset, especially when joining multiple circuits together, can be problematic. It's especially troublesome if we're trying to use large gain values. It's possible that a large gain (thousands or higher) multiplied by even a few millivolts of unintented DC offset could cause our system to saturate purely from the offset.

As an exercise, run the frequency domain simulation and inspect the Bode plot of the circuit above. What happens if you change $C_{\text{in}} = 0.1\ \mu\text{F}$ and re-run the simulation? You can also use the "Sweep Parameter" mode on `Cin.C` and set it to custom values `0.1u,1u` to have the simulator run it for both values to make it easier to compare the two plots.

As another exercise, change the frequency of V1 and run the time-domain simulation to see what happens to the signal as it passes through the amplifier. (As you adjust the frequency, you should also adjust the simulation stop time and time step to get a good picture of what's going on.)

AC coupling can also be combined with the offset virtual ground shown above. The result looks something like this:



Op-Amp Inverting Amplifier - Single-Supply, AC Coupled
circuitlab.com/cws5ghw72yj3d

Edit - Simulate

Exercise Click to open and simulate the circuit above. What's the relationship between input and output sinusoids in terms of scale and offset?

As an exercise, try removing C_{in} and replacing it with a wire. What happens to the output signal?

If we remove the capacitor and replace it with a wire, the output signal is a flat line at $V_{\text{out}} = 5\ \text{V}$, regardless of input signal variations. The amplifier no longer works, and instead stays completely saturated at the positive output rail. This is a bad amplifier design!

AC coupling is tremendously useful in connecting subcircuits together while avoiding saturation due to DC offsets.

Choosing Resistor Values

Most of the concerns about choosing the correct absolute resistor values for R_{in} and R_{f} are the same as the corresponding discussion on the non-inverting amplifier, so we won't repeat

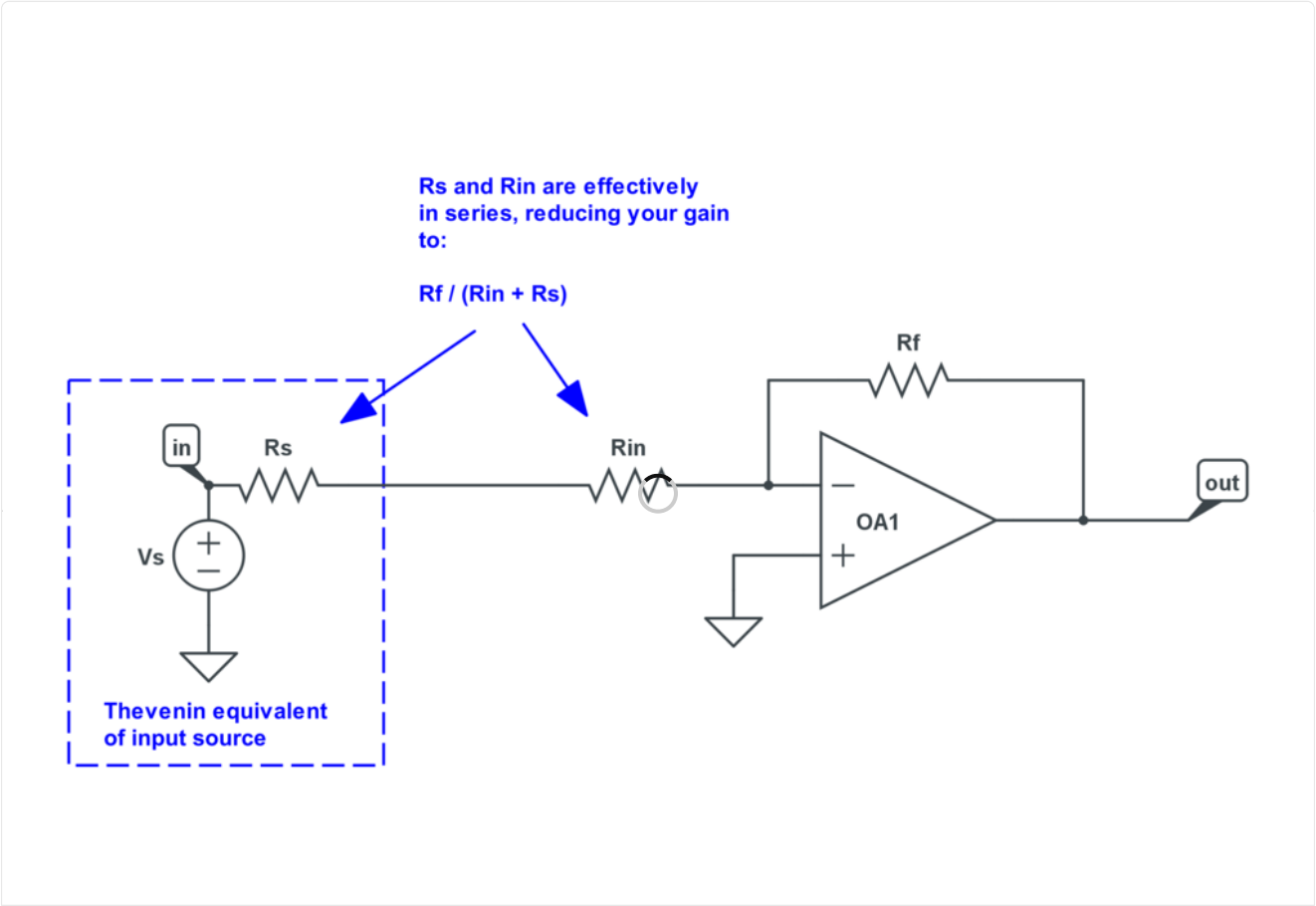
those discussions here. If resistances are too high, noise and stability are concerns. If resistances are too low, output impedance and power consumption are concerns.

The inverting amplifier has one additional concern, however. As discussed earlier, the input impedance of the inverting amplifier configuration is R_{in} at low frequencies.

If you are driving the inverting amplifier with a low-impedance source $R_{\text{s}} \ll R_{\text{in}}$, you're fine.

If you're driving it with a relatively high-impedance source $R_s \gg R_{\text{in}}$, you'll lose most of your signal due to interstage loading.

Another way of thinking about it is that the true design gain is $\frac{R_{\text{f}}}{R_{\text{in}}+R_{\text{s}}}$, where R_{in} and R_{s} appear in series because they are! **Any nonzero source impedance R_{s} lowers the effective gain of the inverting amplifier.** Here's what it looks like:



Op-Amp Inverting Amplifier with Thevenin Equivalent Source Input
circuitlab.com/c5q537vb823cn

Edit - Simulate

$R_{\text{in}} + R_{\text{s}}$ add because they're indistinguishable from the perspective of the circuit. Equivalently, that is to say that the current flowing through R_{f} is the source voltage V_{s} divided by the total resistance between the source voltage and the virtual ground point, $i = \frac{V_{\text{s}}}{R_{\text{s}}+R_{\text{in}}}$.

We have to be careful about what we're calling the source voltage, but this relabeling of V_{in} to be the unloaded open-circuit voltage of the previous stage is a more common way to think about connecting together multiple stages in a signal chain.

To minimize this unintended loss of amplification, you may:

- design with a non-inverting amplifier instead (infinite input impedance)
- add an additional op-amp voltage buffer to provide a low-impedance output to drive the inverting amplifier
- increase R_{in} and R_{f} until $R_{\text{s}} \ll R_{\text{in}}$, at the cost of the stability and noise concerns discussed above.

What's Next

The inverting amplifier takes a voltage input, but if we drop the resistor R_{in} , it's now a useful current-to-voltage converter called an Op-Amp Transimpedance Amplifier, which is a common building block of many other op-amp circuits.

Robbins, Michael F. **Ultimate Electronics: Practical Circuit Design and Analysis.** CircuitLab, Inc., 2021, ultimateelectronicsbook.com. Accessed 07 Apr 2023. (Copyright © 2021 CircuitLab, Inc.)