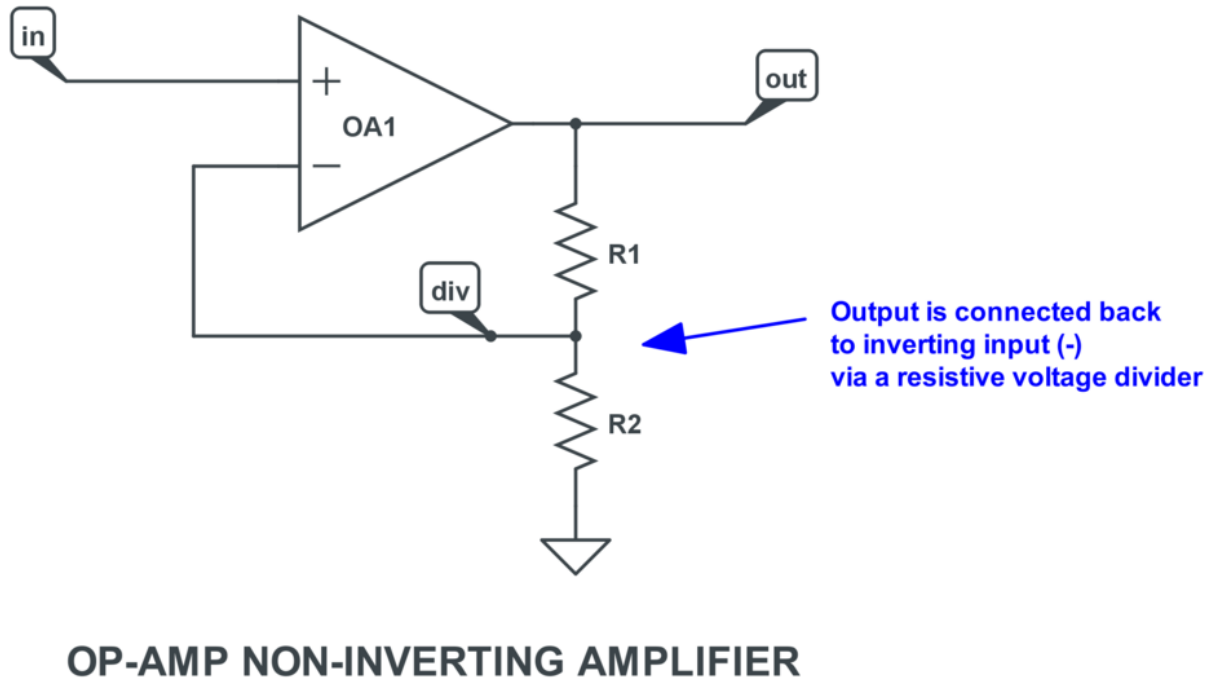
7.4

Op-Amp Non-Inverting Amplifier

An op-amp circuit forming a voltage amplifier, using negative feedback to multiply an input signal by a positive gain set by two resistors.

In previous sections, we showed that by adding one wire to an ideal op-amp, we could create a gain-of-1 op-amp voltage buffer using closed-loop feedback. In this section, we'll show how we can add two resistors to make a **non-inverting amplifier** and choose our desired level of voltage gain, amplifying the voltage signal by $A_v \geq 1$.

Specifically, we can connect a resistive voltage divider to the op-amp's output, and then connect the middle terminal of that voltage divider back to the op-amp's inverting input:



Op-Amp Non-Inverting Amplifier
circuitlab.com/c4wnat6ynz2ek

Edit - Simulate

As discussed in the Voltage Dividers section, the resistors R1 and R2 make an intermediate

voltage point which is proportional to the output, but scaled *smaller* by a ratio determined by the resistor values.

This intermediate voltage V_{div} is then connected via a wire back to the op-amp's inverting (-) input.

Conceptually, the op-amp adjusts its output voltage until its two inputs are equal. The only way to have the op-amp's two inputs be equal is if the output is scaled proportionally *larger* in a way that cancels out the downscaling of the voltage divider.

Solving the Equations

R1 and R2 form an voltage divider, which we can assume is unloaded because the op-amp has zero input current. This gives us one equation:

$$V_{\text{div}} = \left(\frac{R_2}{R_1 + R_2}\right) V_{\text{out}} = f V_{\text{out}}$$

where $f = \frac{R_2}{R_1 + R_2}$ is the voltage divider fraction.

For convenience, let's define the reciprocal of the voltage divider fraction to be our design gain k :

$$k = \frac{1}{f} = \frac{R_1 + R_2}{R_2}$$

The ideal op-amp changes its output until the two inputs are equal. *When all is operating properly,* this gives us an equation:

$$V_{\text{in}} = V_{\text{div}}$$

We can combine these two equations to find a relationship between input and output:

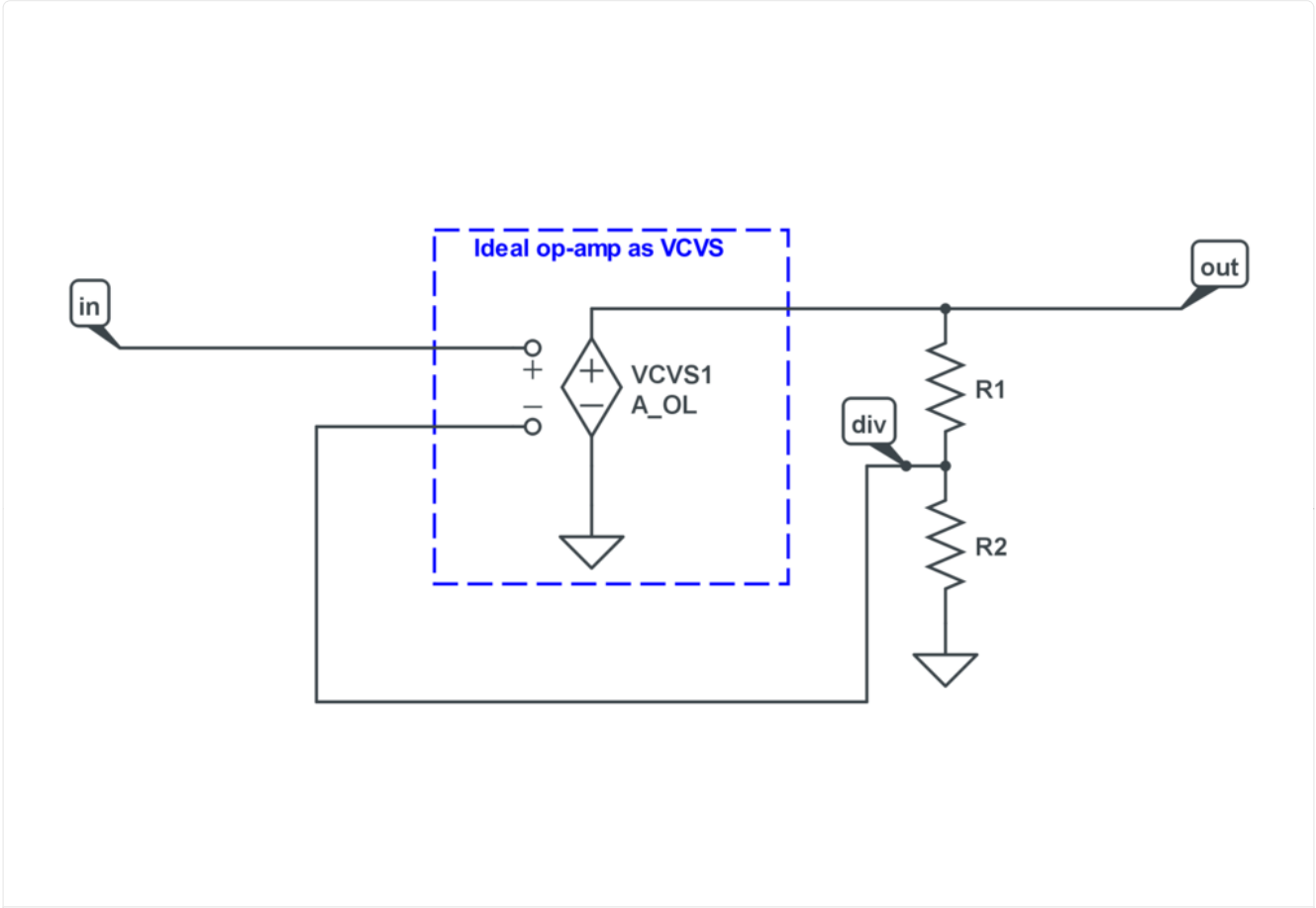
$$\begin{aligned} V_{\text{in}} &= f V_{\text{out}} \\ V_{\text{out}} &= \frac{1}{f} V_{\text{in}} \\ A_v = \frac{V_{\text{out}}}{V_{\text{in}}} &= \frac{1}{f} = k \end{aligned}$$

As the voltage divider can only produce a fraction $0 \leq f \leq 1$, the signal is amplified by a voltage gain:

$$A_v = \frac{1}{f} = k \geq 1$$

VCVS Model

We can model the op-amp as a voltage-controlled voltage source (VCVS) as we did in earlier op-amp sections to allow us to perform a more detailed analysis:



Op-Amp Non-Inverting Amplifier VCVS Model
circuitlab.com/cq3ssz7y3pkpj

Edit - Simulate

The VCVS gives us one equation:

$$V_{\text{out}} = A_{\text{OL}}\left(V_{\text{in}} - V_{\text{div}}\right)$$

The voltage divider continues to be unloaded so we can still substitute in our voltage divider fraction $V_{\text{div}} = fV_{\text{out}}$ and simplify:

$$\begin{aligned} V_{\text{out}} &= A_{\text{OL}}\left(V_{\text{in}} - fV_{\text{out}}\right) \\ V_{\text{out}} &= A_{\text{OL}}V_{\text{in}} - A_{\text{OL}}fV_{\text{out}} \\ V_{\text{out}}\left(1 + A_{\text{OL}}f\right) &= A_{\text{OL}}V_{\text{in}} \\ \frac{V_{\text{out}}}{V_{\text{in}}} &= \frac{A_{\text{OL}}}{1 + A_{\text{OL}}f} \end{aligned}$$

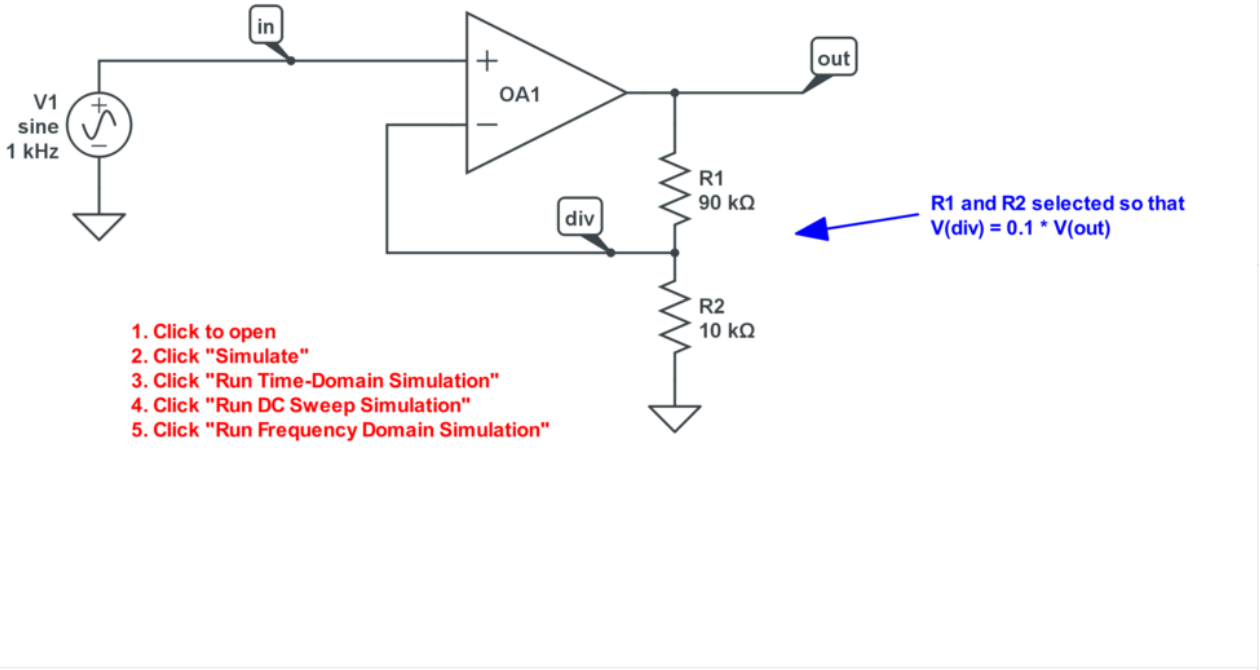
For an ideal op-amp we take the limit $A_{\text{OL}} \to \infty$, producing cancellation in the numerator and denominator:

$$A_v = \frac{V_{\text{out}}}{V_{\text{in}}} \approx \frac{1}{f} = k$$

Again, since $0 \leq f \leq 1$, therefore $k \geq 1$, so this circuit produces an amplification $A_v \geq 1$.

Example: Gain of 10 Amplifier

We can make a gain-of-10 amplifier by setting the voltage divider to have a fraction of $f = \frac{1}{10}$. For example:



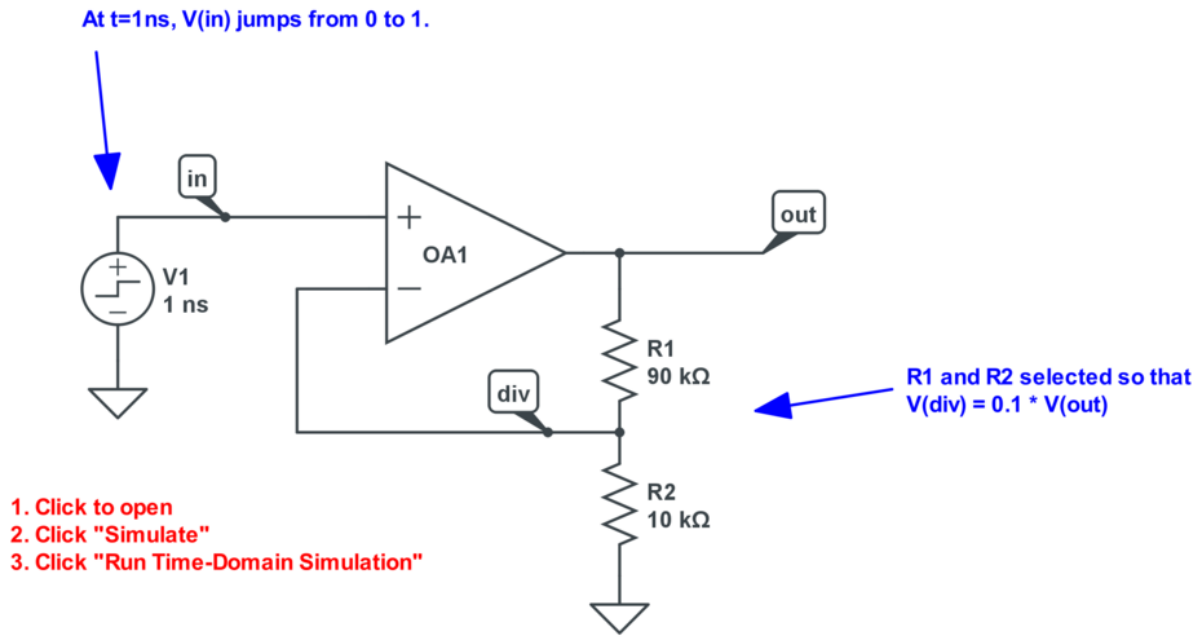
Op-Amp Non-Inverting Amplifier Gain of 10 Example
circuitlab.com/cnm6354nkc2jm

Edit - Simulate

Exercise Click to open and simulate the circuit above. What's the amplitude of the output compared to the input? Can you change R1 to make this amplifier have a gain of 20 instead?

Conceptually, imagine that we start with all voltages at zero. Then suddenly, we change the input to be 1 volt. The op-amp sees a large difference between its non-inverting (+) input at 1 volt, and its inverting (-) output at 0 volts, so (as discussed in the ideal op-amp section) the output begins to rise. When the output reaches 1 volt, the inverting output still sees only 0.1 volt, so the output continues rising. Only when the output rises to 10 volts does the voltage divider yield 1 volt at the inverting input, stopping the further rise of the output.

We can actually examine that happening by looking at the **step response**:



Op-Amp Non-Inverting Amplifier Gain of 10 Step Response
circuitlab.com/c9xykgb57wstt Edit - Simulate

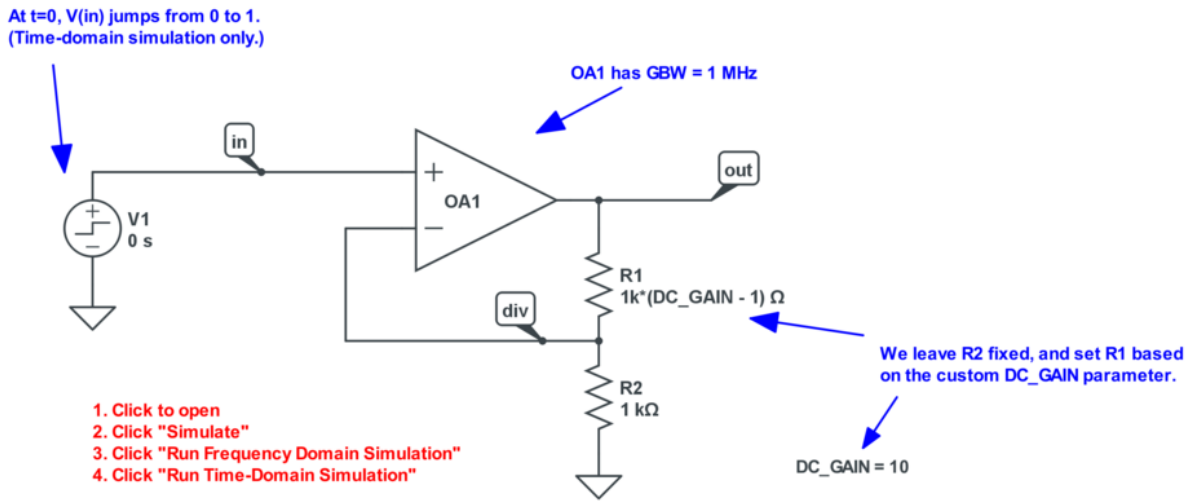
Exercise Click to open and simulate the circuit above. Which trace corresponds to the op-amp's non-inverting input? Which corresponds to the inverting input? What happens if you increase the amplification to 100 and re-run the simulation? (Hint: you may have to change the simulation stop time!)

To draw this out in time, we've used an op-amp with a finite gain-bandwidth product $\mathrm{GBW} = 1\ \mathrm{GHz}$. (A truly ideal op-amp would have $\mathrm{GBW} = \infty$.) The result shows that it takes a few nanoseconds for the op-amp to "close the loop" and bring its two inputs into balance.

Frequency Response and the Gain-Bandwidth Product

In earlier sections we talked about real op-amps having a finite gain-bandwidth product (GBW). At that point it wasn't entirely clear why we'd multiply (product) a unitless amplification (gain) and a bandwidth (in Hz), but the non-inverting amplifier will make it clear.

This is easiest to see with a simulation example where we take an op-amp with $\mathrm{GBW} = 1\ \mathrm{MHz}$ and configure it as a non-inverting amplifier with various levels of gain:



Op-Amp Non-Inverting Amplifier - Gain vs. Bandwidth Tradeoff
circuitlab.com/c2v2mwrd2t966 Edit - Simulate

Exercise Click to open and simulate the circuit above. We've asked the simulator to re-run this circuit for DC_GAIN = 1, 10, 100, 1000, 10000, and 100000. As we step up the gain by a factor of 10 each time (plotted on a decibel log scale y-axis, so they're plotted evenly spaced $+20\ \mathrm{dB}$ steps), what happens to the $-3\ \mathrm{dB}$ corner frequency of the amplifier's response?

This simulation makes it clear that as we ask the amplifier to do more amplification, it gets slower!

You can confirm this by running the time-domain simulation and looking at how much time it takes for the output to settle to within, say, 5% of its final value. You'll see that each time we design the circuit with 10X higher gain, it also takes 10X as long to settle.

This happens because our op-amp's gain isn't A_{OL} at high frequencies; it decreases at higher frequencies. As shown previously, the open-loop ideal op-amp Laplace transfer function is:

$$G(s) = \frac{A_{\mathrm{OL}}}{1 + s\left(\frac{A_{\mathrm{OL}}}{2\pi \mathrm{GBW}}\right)}$$

This expression includes the open-loop gain A_{OL} which covers DC and low frequencies, and it

drops off following the gain-bandwidth product GBW . We can substitute this into our non-inverting amplifier model, inserting $G(s)$ in place of the DC-only A_{OL} :

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}(s) = \frac{G(s)}{1 + G(s)f}$$

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}(s) = \frac{\frac{A_{\mathrm{OL}}}{1+s\left(\frac{A_{\mathrm{OL}}}{2\pi\mathrm{GBW}}\right)}}{1 + f\frac{A_{\mathrm{OL}}}{1+s\left(\frac{A_{\mathrm{OL}}}{2\pi\mathrm{GBW}}\right)}}$$

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}(s) = \frac{A_{\mathrm{OL}}}{1 + s\left(\frac{A_{\mathrm{OL}}}{2\pi\mathrm{GBW}}\right) + fA_{\mathrm{OL}}}$$

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}(s) = \frac{1}{\left(f + \frac{1}{A_{\mathrm{OL}}}\right) + s\left(\frac{1}{2\pi\mathrm{GBW}}\right)}$$

This tells us the complex frequency response of the non-inverting amplifier for a sine wave input of frequency $s = j\omega = j2\pi f_s$.

(Note the potential for confusion here: we're using f to refer to the unitless voltage divider fraction, and f_s to refer to the signal frequency in Hz.)

If we look at this expression only at DC, then $s = 0$ so:

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}(s = 0) = \frac{1}{f + \frac{1}{A_{\mathrm{OL}}}} \qquad (\text{at DC})$$

If you multiply numerator and denominator by A_{OL} you'll see this is identical to the $\frac{A_{\mathrm{OL}}}{1+fA_{\mathrm{OL}}}$ expression we found earlier in this section. And similarly, since $\frac{1}{A_{\mathrm{OL}}} \ll f$, we can ignore the $\frac{1}{A_{\mathrm{OL}}}$ term. (Observe that if we try to use the voltage divider to choose a closed-loop gain that is similar to or greater than the op-amp's open-loop gain, then this approximation won't hold, and the amplifier will not work as you intended, even at DC.)

Let's use this simplification to replace $\left(f + \frac{1}{A_{\mathrm{OL}}}\right) \approx f$ in the denominator, and place this back into our earlier expression:

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}(s) = \frac{1}{f + s\left(\frac{1}{2\pi\mathrm{GBW}}\right)}$$

And now, instead of referring to the voltage divider fraction $0 \leq f \leq 1$, let's refer to its reciprocal, the design voltage gain $k = \frac{1}{f}$. Multiplying numerator and denominator by k :

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = \frac{k}{1 + s\left(\frac{k}{2\pi \text{GBW}}\right)}$$

This closed-loop transfer function can be decomposed into the product of a gain k and a one-pole low-pass filter $\frac{1}{1+s\left(\frac{k}{2\pi \text{GBW}}\right)}$.

We can find the corner frequency of the low-pass filter by determining where the imaginary part of the denominator is equal in magnitude to the real part:

$$\begin{aligned}
|1| &= |s\left(\frac{k}{2\pi \text{GBW}}\right)| \\
|1| &= |j\omega_c\left(\frac{k}{2\pi \text{GBW}}\right)| \\
1 &= \omega_c\left(\frac{k}{2\pi \text{GBW}}\right) \\
1 &= 2\pi f_c\left(\frac{k}{2\pi \text{GBW}}\right) \\
1 &= f_c\left(\frac{k}{\text{GBW}}\right) \\
f_c &= \frac{\text{GBW}}{k}
\end{aligned}$$

This last equation tells us that the amplifier's closed-loop corner frequency f_c is equal to the gain-bandwidth product divided by the gain:

- If the gain $k = 10$ and the $\text{GBW} = 10^6 \text{ Hz}$, then $f_c = \frac{10^6 \text{ Hz}}{10} = 10^5 \text{ Hz}$.
- If the gain $k = 100$ and the $\text{GBW} = 10^6 \text{ Hz}$, then $f_c = \frac{10^6 \text{ Hz}}{100} = 10^4 \text{ Hz}$.
- If the gain $k = 1000$ and the $\text{GBW} = 10^6 \text{ Hz}$, then $f_c = \frac{10^6 \text{ Hz}}{1000} = 10^3 \text{ Hz}$.

For a given op-amp (i.e. a fixed gain-bandwidth product), the closed-loop corner frequency gets lower as you ask it to do more amplification. **There is a direct tradeoff between amplifier performance in terms of amplification, and performance in terms of bandwidth.**

This is not merely theoretical. You are likely to run into this problem in real-world op-amp design! For example, if you need a gain of 1000, and you simultaneously need to handle signals of 10^5 Hz, you have a few options:

- *Use a faster op-amp.* Buy an op-amp with a higher GBW.
- *Split your overall gain into multiple stages.* Use two or three of the slower op-amps, perhaps doing only a gain of 10 at a time, allowing you to achieve higher corner frequencies in each stage.

The limited frequency response also manifests as a slower step response in the time domain.

Simulate the circuit above and see how long it takes to settle to its final value after an input step for different gain configurations.

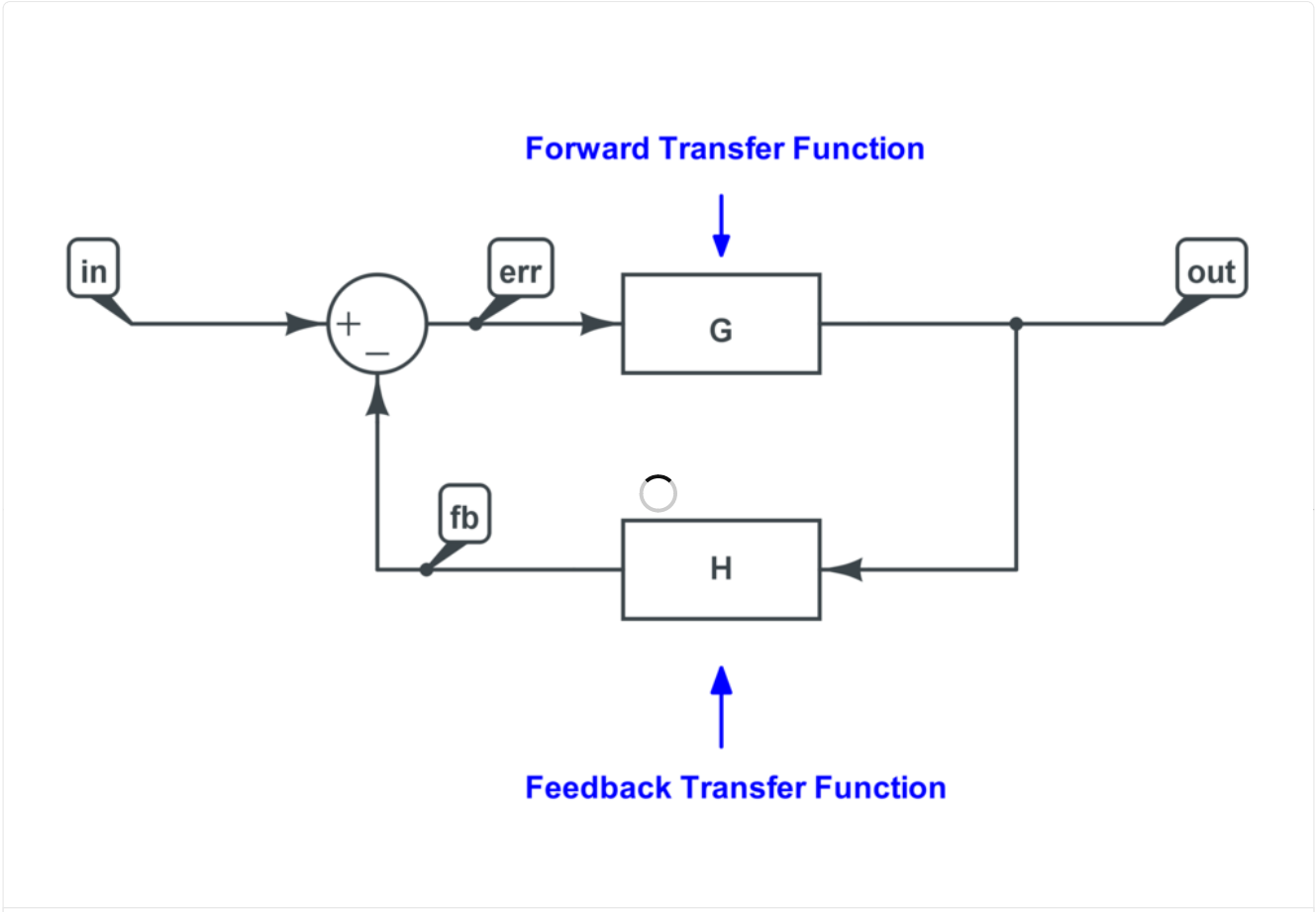
Closed-Loop Feedback and Inverse Behavior in the Feedback Path

Notice that the voltage divider makes the output signal *smaller* by some fraction $0 \leq f \leq 1$, while the overall effect of the closed-loop circuit actually makes the output *larger* than the input by $k = \frac{1}{f} \geq 1$.

This is actually a simple case of a common but confusing concept in feedback systems: a modification in the feedback path (such as multiplication by f) generally causes the *inverse* or *reciprocal* effect (such as multiplication by $\frac{1}{f}$) to the whole system after closed-loop feedback is applied. That's a big idea and can be hard to grasp in general, but the non-inverting amplifier illustrates the concept in the simplest way possible.

For readers familiar with transfer functions: this is equivalent to saying that the feedback transfer function ends up in the *denominator* of the closed-loop response.

In a general way, we can look at a feedback system with a **forward transfer function** G and a **feedback transfer function** H as depicted here:



Closed-Loop Transfer Function Block Diagram
circuitlab.com/c42n7tesuxm2d

Edit - Simulate

For simplicity, consider these multipliers G and H to be constants, performing multiplicative scalings of their input.

Our block diagram has four labeled nodes for the input, output, error, and feedback terms.

The three block diagram elements (one subtraction and two transfer function multiplications) let us build a system of three equations:

$$\begin{aligned} V_{\text{err}} &= V_{\text{in}} - V_{\text{fb}} \\ V_{\text{fb}} &= H \cdot V_{\text{out}} \\ V_{\text{out}} &= G \cdot V_{\text{err}} \end{aligned}$$

We'd like to find a closed-loop relationship between input and output, without the V_{err} or V_{fb} terms. We can combine the above equations, substituting V_{fb} and V_{err} to find:

$$\begin{aligned} V_{\text{out}} &= G \cdot \left(V_{\text{in}} - H \cdot V_{\text{out}}\right) \\ V_{\text{out}} &= G \cdot V_{\text{in}} - GH \cdot V_{\text{out}} \\ V_{\text{out}}(1 + GH) &= G \cdot V_{\text{in}} \\ \frac{V_{\text{out}}}{V_{\text{in}}} &= \frac{G}{1 + GH} \end{aligned}$$

This last equation is the **closed-loop transfer function**, and it relates the input to the output, after considering the effects of the feedback loop. It's a general result that is quite useful!

A particularly interesting case is to consider what happens when $|GH| \gg 1$. In this case, we can approximate that $1 + GH \approx GH$ in the denominator, in which case the equation simplifies:

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx \frac{G}{GH} = \frac{1}{H} \quad \left(\text{if } |GH| \gg 1\right)$$

This is a remarkable result: if the magnitude of the **loop gain** $|GH|$ is large compared to 1, then the foward transfer function G actually cancels out of the closed-loop result, and the closed-loop response is determined only by the reciprocal of the feedback transfer function, $\frac{1}{H}$.

In the case of the op-amp non-inverting amplifier at DC, the forward transfer function $G = A_{\text{OL}}$, the open-loop gain of the op-amp. The feedback transfer function $H = f$, the voltage divider fraction, as only a fraction of the output is fed back to the input.

Since typical values for $A_{\text{OL}} \gg 100000$ and the fraction $0 \leq f \leq 1$, the product $|GH| = |fA_{\text{OL}}| \gg 1$ for all but very tiny values of f. (We'll ignore this range of very small f values, as they represent a condition where we're attempting to design a non-inverting amplifier that has closed-loop gain larger than the open-loop gain of the amplifier, which won't work!) So the closed-loop gain is just:

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx \frac{1}{f} = k$$

When we care about the response of systems with frequency-dependent behavior, such as when we analyzed the gain-bandwidth tradeoff above, we can still apply the Laplace-domain to the same general closed-loop result:

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{G(s)}{1 + G(s)H(s)}$$

Choosing Resistor Values

So far, we've only considered the *ratio* of resistor values in our resistive divider, as that's what determines our gain. (We can even use a potentiometer to make an adjustable-gain amplifier.)

But how should we choose the *absolute* resistor values? If we want to design an amplifier with a gain of $A_v = 10$, why should we pick $\left(R_1 = 90\ \text{k}\Omega, R_2 = 10\ \text{k}\Omega\right)$ instead of $\left(R_1 = 9\ \Omega, R_2 = 1\Omega\right)$, even though both produce the same voltage divider ratio?

The answers are similar to the tradeoffs discussed in the Voltage Dividers section. There are

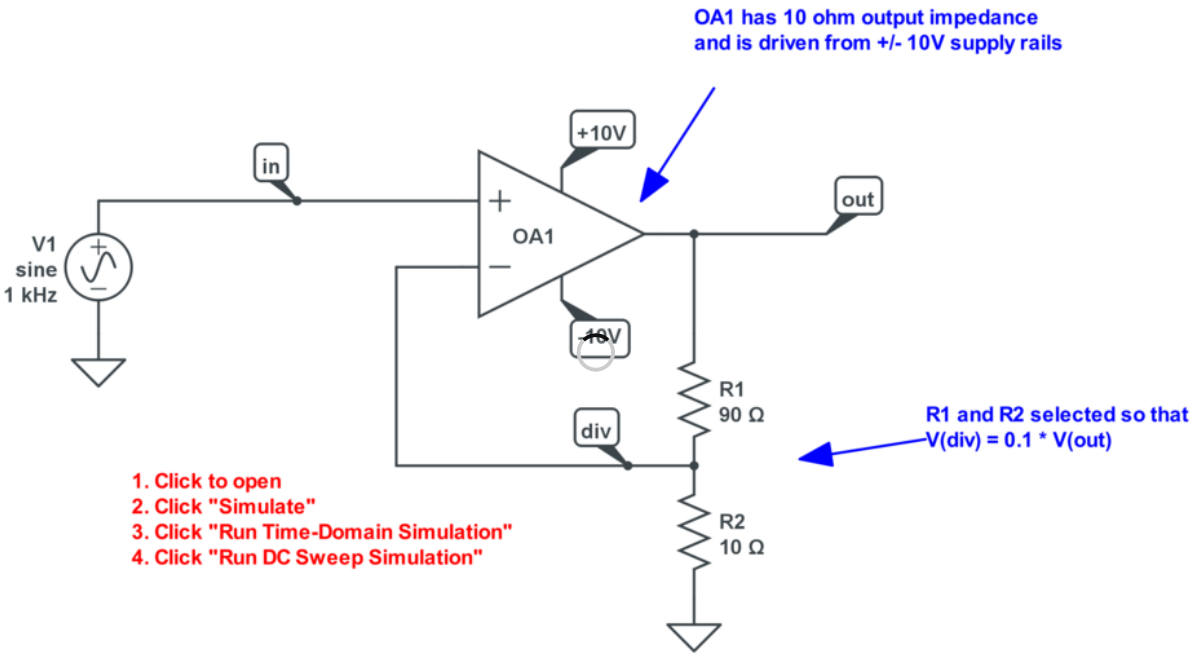
concerns and drawbacks on either extreme:

Resistances Too Low

If the resistances are much too small:

- **Excessive power consumption.** Power dissipation in the resistors becomes significant, possibly leading to overheating in the resistors or even in the op-amp itself.
- **Output impedance and supply rail limits.** Real op-amps have nonzero output impedance. Their ability to drive large currents is especially compromised near the supply rails. You may find that the output range is compromised when using too-small resistors.

Here's a simulation showing the latter problem:



Op-Amp Non-Inverting Amplifier - Clipping due to Output Impedance
circuitlab.com/c2xqt2ju44bm7 Edit - Simulate

Exercise Click to open and simulate the circuit above. The 1V-amplitude sine wave is amplified by $k = 10$, which should fit within the 10V supply rails. However, this op-amp has an output impedance $R_O = 10\ \Omega$, which limits its ability to drive its output near the rails. What does the resulting signal look like? What happens if you change R1 and R2 to both be 2x smaller or larger?

Note that this problem is exacerbated further if the op-amp's output is loaded. As an exercise, add a load resistance to the output and see how the signal changes.

These problems cause nonlinear **clipping**, which destroys information and causes distortion for all later signal stages.

Resistances Too High

If the resistances are too large:

- **Excessive noise.** Resistor voltage noise increases as resistance increases.
- **Loading error due to op-amp input current.** While the ideal op-amp has zero input current, real op-amps typically have some small current into their inputs. If the voltage divider resistors are too large, this can cause an unwanted voltage drop, resulting in an unwanted offset.
- **Stability problems.** Parasitic capacitances have a larger effect at high-impedance nodes. With high-gain feedback this becomes especially dangerous. We'll discuss this next.

In typical design, it's typical to pick values in the range:

$$1\ \mathrm{k\Omega} \leq \left(R_1 + R_2\right) \leq 1\ \mathrm{M\Omega}$$

This is a very wide range already, so don't be surprised if you see some op-amp designs outside of it, but you should double-check if they might be prone to one or more of the issues above.

Feedback Input Capacitance and Stability Issues

What happens if there is some unintentional but unavoidable parasitic capacitance in the feedback path? Let's model this as a capacitor between the inverting input and ground. Conceptually, we can follow the ideal op-amp adjusting its output up or down based on the immediate difference in its inputs:

1. A voltage step input on the non-inverting terminal causes the op-amp's output to start rising and rising.
2. The output rising starts to send current through the voltage divider. But because of the capacitance, the rising output doesn't immediately propogate back to the inverting input.
3. The capacitor takes time to charge, and it can only charge through the resistors. This takes time.
4. As a result, the op-amp's output keeps rising and rising. If the capacitance is large enough, the op-amp's output keeps rising well past the point where it should settle out, because the

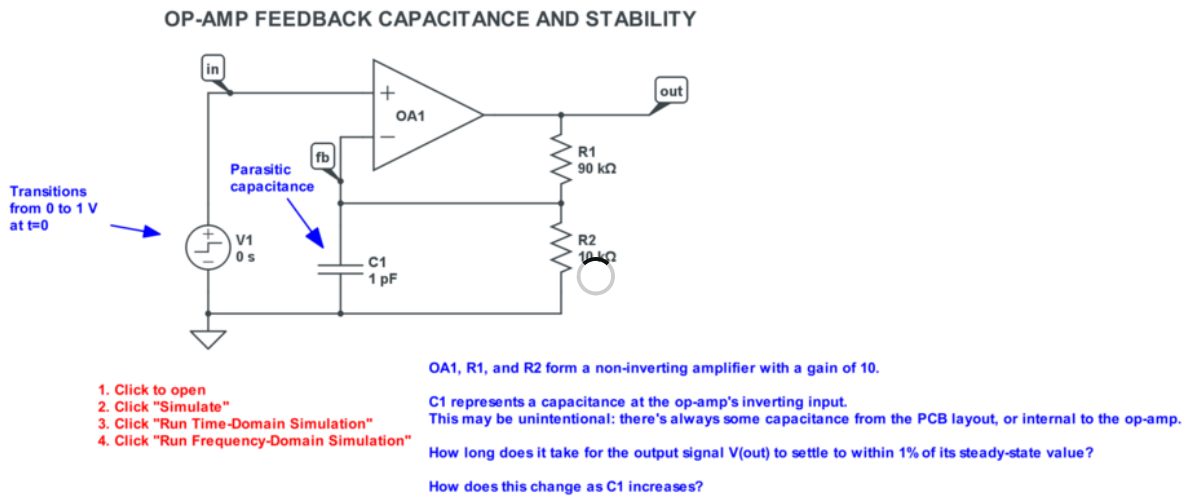
capacitor is still charging. This is called **overshoot**.

5. Eventually, the capacitor charges up to the point where it matches and even exceeds the non-inverting input voltage. At this point, the op-amp starts reducing its output.
6. However, since the output is still higher than the steady-state point, the capacitor is still being charged, higher and higher, causing further overshoot!
7. Eventually, the output falls enough that it causes the capacitor to start discharging.
8. The oscillations (also called **ringing**) eventually settle out to the steady-state point, where the capacitor is neither being charged nor discharged by the output.

We effectively have two slow things chasing each other:

1. The op-amp and it's limited gain-bandwidth product, and
2. The RC circuit formed by the voltage divider plus the capacitance.

In this simulation, you can see that when the parasitic capacitance C1 is large enough, the capacitor voltage continues rising well past where it's supposed to, out of phase with the peak in the output voltage:



Op-Amp Non-Inverting Amplifier Feedback Parasitic Capacitiance Stability Issues
circuitlab.com/ctahy46huss23 Edit - Simulate

Exercise Click to open and simulate the circuit above. How does even a few picofarads of parasitic capacitance affect the step response?

As an exercise, try making R1 and R2 both be 10x larger. What happens now?

Does anything change if C1 is connected between the two op-amp inputs, rather than from the inverting input to ground? Why or why not?

Parasitic capacitance is a real problem in high-speed amplifiers, and issues with feedback loop stability is one of them. We call it **stability** because in the extreme cases, it's possible for this to become **unstable** and oscillate forever, never settling to the final value. (You can approach this in the simulator by making C1 very large. In the simulator it will eventually settle out, but in the real world, it may actually oscillate forever because of additional delay imposed by the speed of light, if nothing else!)

There are multiple ways to mitigate this problem:

1. Layout the physical circuit to reduce parasitic capacitance.
2. Use smaller resistances.
3. Use a *slower* op-amp (lower GBW), and accept slower responses in exchange for stability.
4. Add a feed-forward compensation capacitor, as we'll show next.

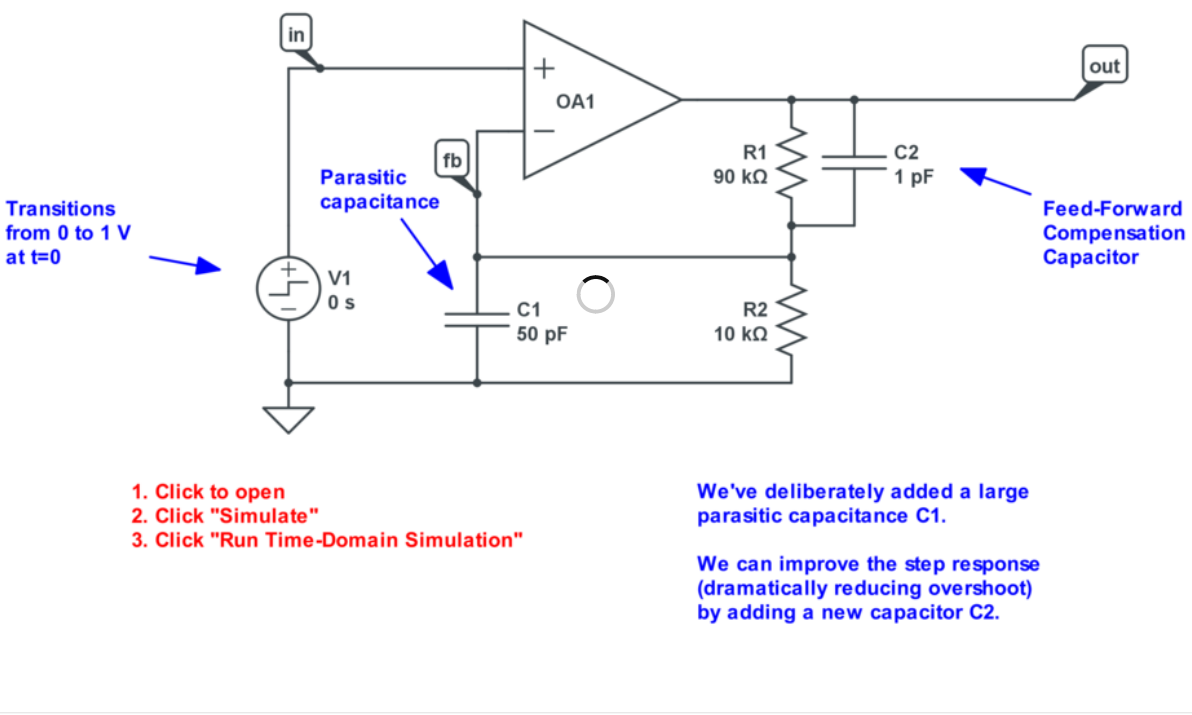
Op-Amp Compensation

The last option for mitigating our stability problem is worth demonstrating briefly. We can add a small **feed-forward compensation capacitor** C2 in parallel with R1.

(Remember that C1 is not a capacitor component that we buy and install in our circuit, but is instead just a parasitic capacitance that arises from the circuit layout. In contrast, C2 is a deliberately-added capacitor, though parasitics may contribute to it as well.)

This added capacitor actually helps because it helps push the increase in output voltage directly from the output into the parasitic capacitance C1, without the delay in waiting for C1 to charge through R1.

The choice of value for C2 is complicated and involves the design gain of the amplifier, the op-amp's gain-bandwidth product, the resistances involved, and the value of the parasitic capacitance. Nonetheless, it's possible to pick by simulation or experimentation. Here's an example where we test out different compensation capacitor values:



Op-Amp Non-Inverting Amplifier - Feed-Forward Compensation Capacitor
circuitlab.com/c9wqubpx4g4g5 Edit - Simulate

Exercise Click to open and simulate the circuit above. What's the best capacitance to choose for C2 in this situation?

- If the compensation capacitance is too low (or zero), we'll have instability and overshoot in the step response.
- If the compensation capacitance is too high, it will slow down the amplifier step response too much.
- But there's a Goldilocks zone in the middle (around $5 - 6\ \mathrm{pF}$ in this example), where the step response is very nice, despite a large parasitic capacitance.

Adding compensation capacitors is on the more advanced end of analog magic, but with an understanding of why stability problems occur and how they might be corrected, you may be able to use simulation and experimentation to solve them when they happen.

What's Next

As you may have guessed from the "non-inverting" name, there's also an Op-Amp Inverting

Amplifier configuration, which we'll explore next.
