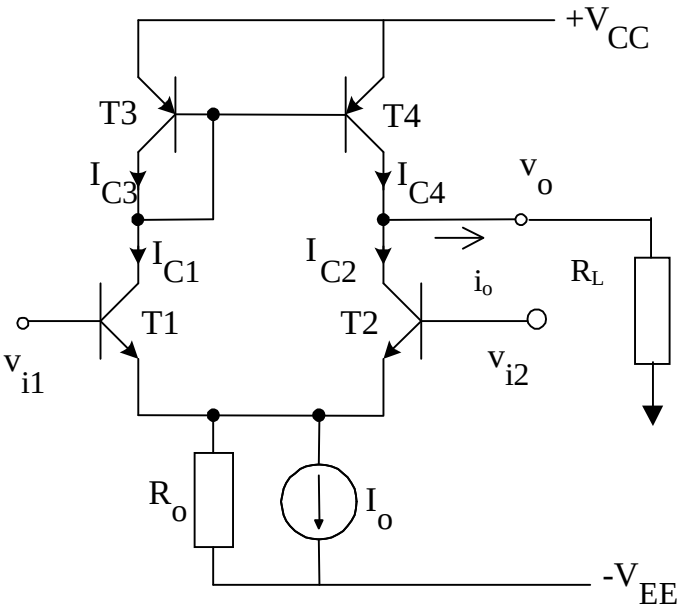
Differential amplifier with active loads – explanation of operation and summary of analysis

Now address the problem of achieving a large load resistor, R_C for high gain without upsetting d.c. conditions. Consider the circuit below where the collector resistors have been replaced by a current mirror:



We investigate the operation by first considering the inputs grounded (d.c. operation). Current mirror action in T_3 and T_4 means that $I_{C3} = I_{C4}$ always. Also, assuming base currents are negligible, $I_{C3} = I_{C1}$. With grounded inputs and assuming perfectly matched transistors, $I_{C1} = I_{C2} \approx I_o/2$. Hence $i_o = 0$ (as $I_{C4} = I_{C1}$) . With a differential signal applied such that v_{i1} is going more positive and v_{i2} is going less positive, I_{C1} (= I_{C3}) will rise and hence so will the current I_{C4} , by current mirror action. However, I_{C2} will fall hence

$$i_o = I_{C4} - I_{C2} = I_{C1} - I_{C2}$$
$$= g_m v_{i1} - g_m v_{i2} = g_m (v_{i1} - v_{i2}) = g_m v_{id} \text{ (as '} I_C = g_m v_{in}\text{')}$$

the configuration is thus best thought of as a *transconductance* amplifier:

$$G_m = \frac{i_o}{v_{id}}$$

Voltage gain

Recall that for the voltage gain of a diff. amp. with resistors R_C, the differential voltage gain was $g_m R_C$. As the 'R_C' is now the *dynamic* resistance 'looking up' into the collectors of the current mirror. We might 'guess' that the voltage gain now becomes

$$A_{Vd} = g_m (r_{ce4} \,//\, r_{ce2} // R_L)$$
$$\sim g_m (r_{ce4} \,//\, r_{ce2}) \text{ if } R_L \text{ is very big (infinity say)}$$

Voltage gain is thus large without the need for a very large (area consuming) discrete resistor.

Exercise: Assuming that the guess is correct, show that A_{Vd} can be expressed in terms of the Early voltages (V_{An}, V_{Ap}):

$$A_{Vd} = \frac{1}{V_T}\frac{V_{An}V_{Ap}}{V_{An}+V_{Ap}}$$ [recall that $g_m = I_C/V_T$ and $r_{ce} = V_A/I_C$]

Solution

The output resistance of $T_2 = V_{An}/I_C$
The output resistance of $T_4 = V_{Ap}/I_C$

Without R_L we have $A_{Vd} = g_m\left(r_{ce2} // r_{ce4}\right) = \frac{I_C}{V_T}\frac{\frac{V_{An}}{I_C}\frac{V_{Ap}}{I_C}}{\frac{V_{An}}{I_C}+\frac{V_{Ap}}{I_C}} = \frac{1}{V_T}\frac{V_{An}V_{Ap}}{V_{An}+V_{Ap}}$ as required

Note that:-

1. We have assumed above that the amplifier is driving an infinitely large resistance load R_L. In reality, the 'load' resistance would be $R_L // r_{ce2} // r_{ce4} \rightarrow R_L$ (if $R_L << r_{ce}$) and the high gain can therefore be severely reduced by the loading of the following stage. However, we could ensure a high resistance for the following stage by making it an emitter follower (high input resistance) and thus high voltage gain could be realised.

2. The d.c. output voltage level is a 'V_{BE}(on)' drop less than the supply rail V_{CC}. Thus the d.c. output voltage is (V_{CC} − 0.7 V). This implies that only a very small (a.c.) voltage swing is allowed at v_o. However, it must be recalled that in the main purpose of achieving very high gain amplifiers is to 'trade' the gain for feedback to stabilise and enhance the overall performance (input and output resistance etc.). Thus a large amount of negative feedback is generally used and this tends to make $v_{in1} \rightarrow v_{in2}$. (See 2nd semester notes on feedback.)

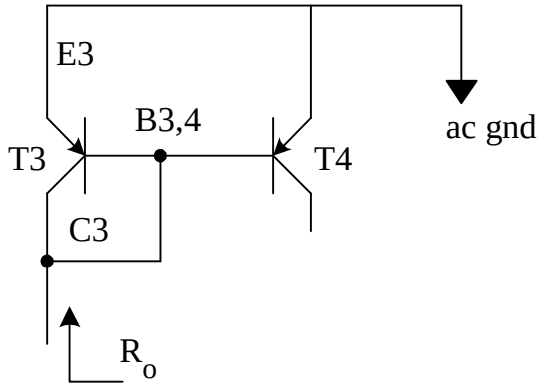
3. Both high transconductance (gain) and high input resistance are required and this constitutes a design trade-off. (See earlier notes for ways of increasing input resistance.)

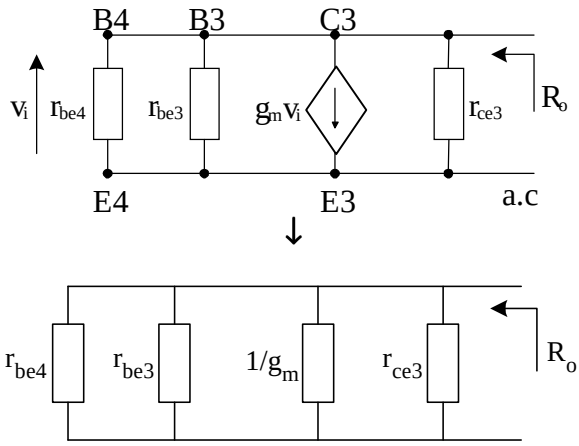
4. greatly improved common mode rejection because of the large dynamic resistance of the current source I_o

5. the current mirror effectively provides the 'subtraction' of the outputs so the output can be taken single ended.

a.c. analysis – more rigorous analysis

We will derive the expression for gain again, by considering the a.c. equivalent circuit. We seek an equivalent circuit for the current mirror load: what 'resistance' is seen looking up into the current mirror?

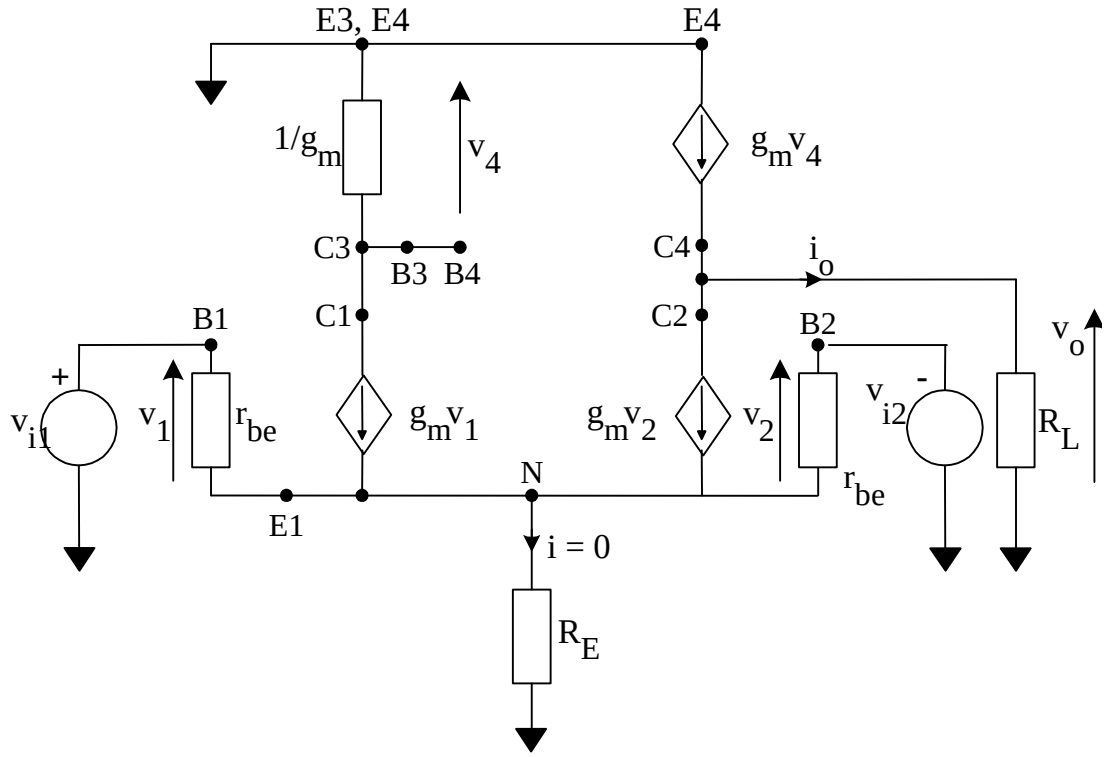




The following approximation can again be made (see Widlar CM notes)

$$R_o = r_{be4} // r_{be3} // \frac{1}{g_m} // r_{ce3} \approx \frac{1}{g_m}$$

Now construct the equivalent circuit for differential mode (ignoring the r_{ce} 's for simplicity)



Note that the voltage drop across the $1/g_m$ load is $v_4 = (g_m v_1) \times 1/g_m = v_1$

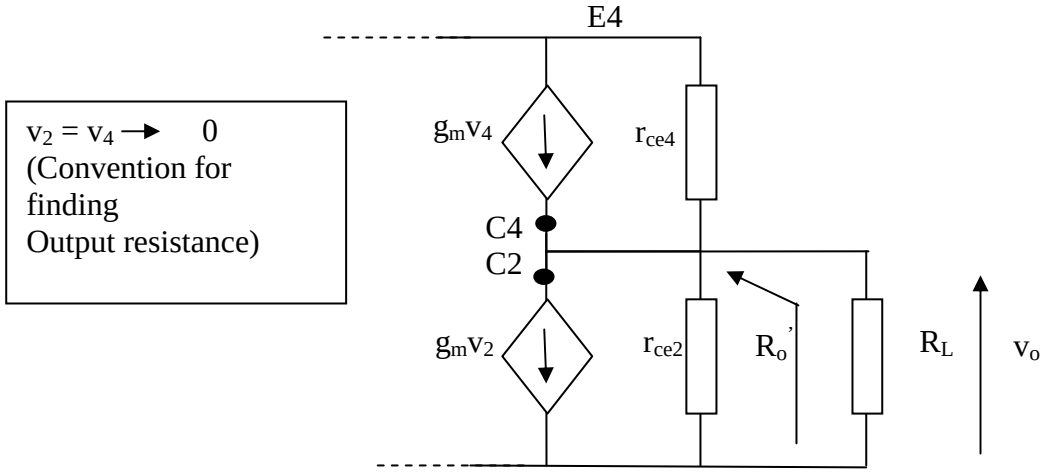
So write: $i_o = g_m(v_4 - v_2) = g_m(v_1 - v_2) = g_m v_{id}$; ie, $i_o = g_m v_{id}$

So $v_o = g_m v_{id} R_L$

$\therefore$ $A_{vd} = g_m R_L$ (single ended voltage gain)

$v_{i1} = i_i r_{be}$; $v_{i2} = -i_i r_{be}$ so $v_{id} = i_i r_{be} - (-i_i r_{be})$ and **Diff. input resistance**, $R_{id} = \frac{v_{id}}{i_i} = 2r_{be}$

Include the effect of r_{ce}'s



As v_2 and v_4 are set to zero (by convention for finding output resistance, the a.c. load is by inspection, $R_o' = r_{ce4}//r_{ce2}$ and $R_o = r_{ce4}//r_{ce2}//R_L$

So without R_L $A_{Vd} = g_m (r_{ce4} // r_{ce2})$ - VERY HIGH
But with R_L, $A_{Vd} = g_m (r_{ce4} // r_{ce2} // R_L)$

and if $R_L << r_{ce4} // r_{ce2}$, then $A_{Vd} \sim g_m R_L$ - VOLTAGE GAIN MUCH REDUCED if R_L small

→ **so ensure that the differential amplifier with active loads is not fed into a low impedance stage.**

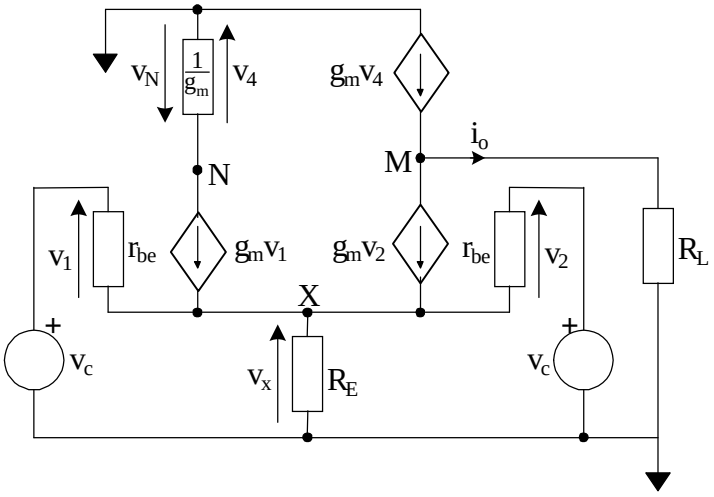
Common Mode Gain

Currents in left and right- hand sides of the circuit are the same (by CM action), so

$i_o = 0$

$v_o = 0$

$A_{vc} = 0$



Note that $g_m v_1 = g_m v_2$ - also, $v_4 = v_1$ (see previous page); hence $i_o = 0$ and $v_o = 0$; $A_{cm} = 0$!

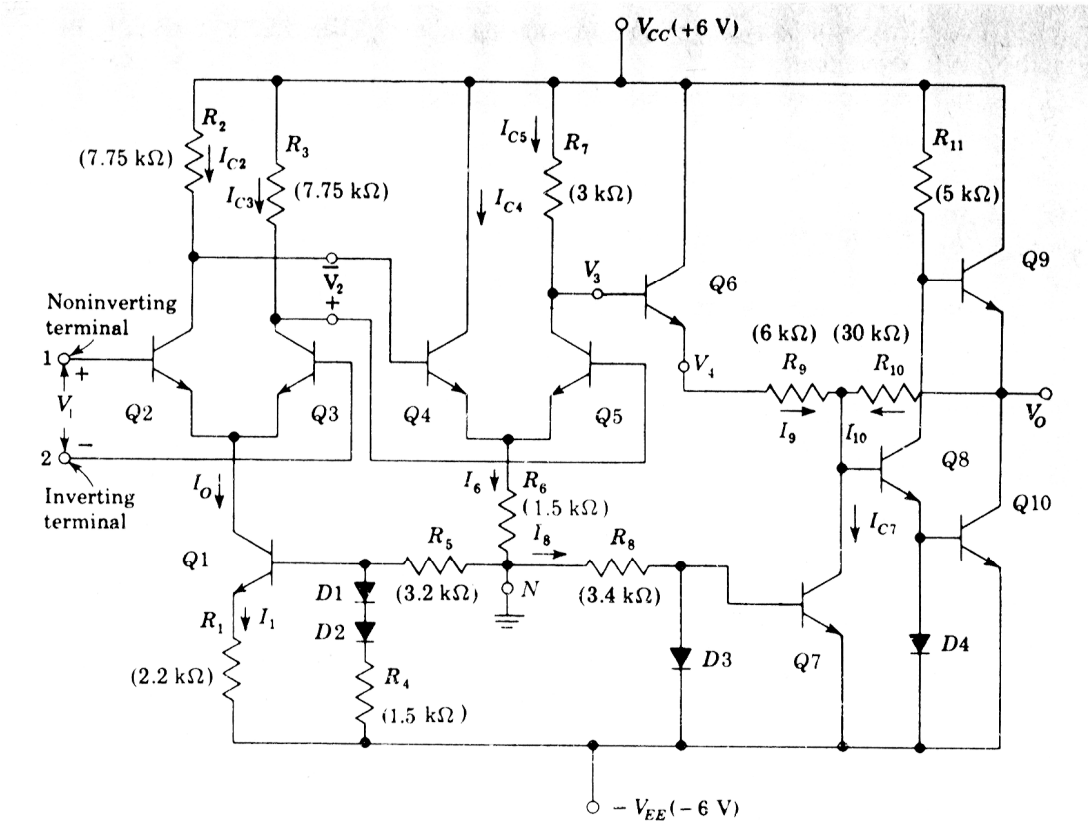
Conclusion: By the use of active loads and a current source, we have achieved the objective of both high gain and large CMRR. We have 'de-coupled' the a.c. and d.c. roles of the biasing components.

We are now in a position to analyse a 'real' operational amplifier using our knowledge of d.c. biasing techniques, a.c. equivalent circuits and multi-stage amplifiers (see Ex.2).

Exercises

1. Consider a common-emitter amplifier with a current mirror load. Work out an expression for the voltage gain in terms of the Early voltages.
2.

2. The figure below shows an early operational amplifier (Motorola MC1530).
All transistors are out of saturation, therefore base currents can be neglected. Note also that the diodes D_1 - D_4 are formed by transistors with the base and collector terminals connected together.



I. Identify the circuit building blocks that make up the amplifier.

II. Calculate the following <u>d.c. currents and voltages</u> (applied a.c. voltages at inputs 1 and 2 are both zero).

(i) Voltage at the base of Q_1, (ii) hence I_1, I_O and $I_{C2} = I_{C3}$, (iii) voltage at base of Q_4, (iv) $I_{C4} = I_{C5}$, (v) V_3, V_4, (vi) I_8 hence I_{C7} (Hint: what is the circuit configuration formed by R_8, D_3 and Q_7?), (vii) voltage at base of Q_8, (viii) I_9, (ix) I_{10}, (x) V_O

III. Assuming $\beta_o = 100$ for all transistors:

(xi) calculate the gain of the first stage $A_{V1} = v_2 / v_1$ (Load is 7.75k in parallel with the input resistance of Diff. Amp. formed by Q_4,Q_5 : r_{be4}).

(xii) find the gain of the second stage, $A_{V2} = v_3/v_2$

(xiii) hence find the overall gain of the amplifier, $A_V = v_o/v_1$. (Hint: the gain of the final stage is set by the ratio of resistors R_{10}, R_9)