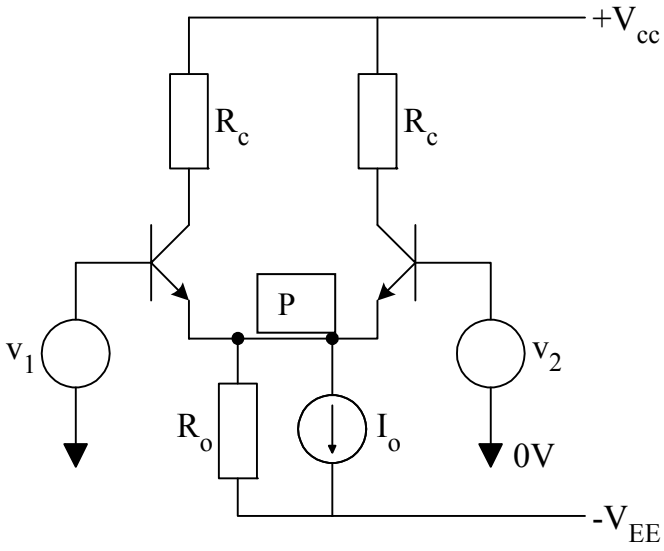
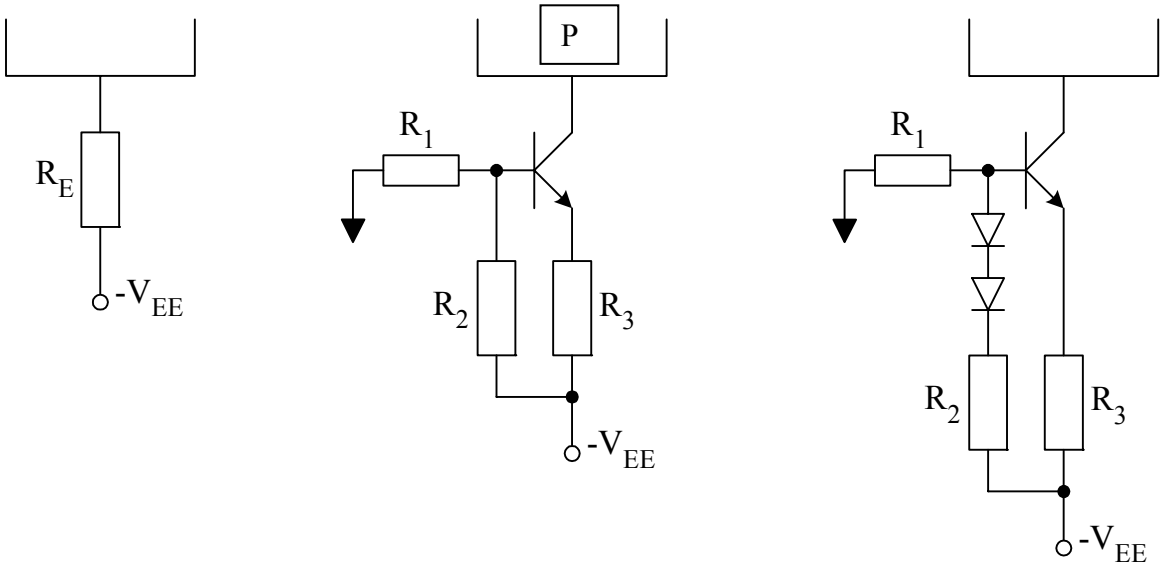
Differential Amplifier with Constant Current Source Biasing

We seek an improved current source and the general case is shown below, where I_o is an ideal current source and R_o represents non-ideality.



Three forms are shown below. The first (R_E) has been considered already.



For the second, we analyse by assuming that the base current is negligible (zero). R_1 and R_2 form a potential divider so the voltage on the base of the transistor is

$$V_B \sim -V_{EE}\frac{R_1}{R_1+R_2}$$

so the emitter current (and hence bias current) is $$I_E = \frac{(|V_B| - V_{BE}) - |V_{EE}|}{R_3} \sim I_C = I_o$$

Thus I_o can be set by R_3. What about the effective resistance looking into the current source (R_o)?

Considering the output characteristic of a transistor, the dynamic resistance is very high (flat characteristic). We could perform a small signal analysis (try it if you want!) and this would show that the R_o is $> 10\ r_{ce}$ typically, where r_{ce} is the output resistance of a transistor. Why is it increased with this circuit? Consider a slight increase in voltage at P. This implies a very slight increase in I_C due to the Early effect and hence I_E. The increase in I_E causes a slight increase in the emitter voltage and hence a slightly smaller V_{BE} for the transistor which in turn causes I_C to decrease. That is to say, the resistor R_E provides 'feedback' and prevents I_C and hence I_O rising. This is the physical effect that gives rise to very large R_o.

We turn now to the 3rd circuit. Again we ignore the base current and assume 0.7 V is dropped across each forward biased diode. The net voltage across the resistors is therefore (V_{EE} – 1.4 V) and the voltage at the base node is

$$V_B \sim -\left(|V_{EE}| - 1.4\right)\frac{R_1}{R_1 + R_2}$$

The emitter voltage is then $V_E \sim -\left(|V_{EE}| - 1.4\right)\frac{R_1}{R_1 + R_2} - V_{BE}$

And the emitter current is $I_E = \frac{\left(|V_{EE}| - |V_B|\right)}{R_3} \sim I_C = I_o$

Why have the diodes been introduced into the base bias circuit? The answer is, to provide temperature compensation. (see notes in lecture for further details)

Temperature dependence and compensation

Consider the diode equation (note it's the same form as that of the collector current), written in two forms as below.

$$I_d = I_S(T)\exp\left(\frac{qV_d}{kT}\right) \qquad V_d = \frac{kT}{q}\ell n\left(\frac{I_d}{I_S(T)}\right)$$

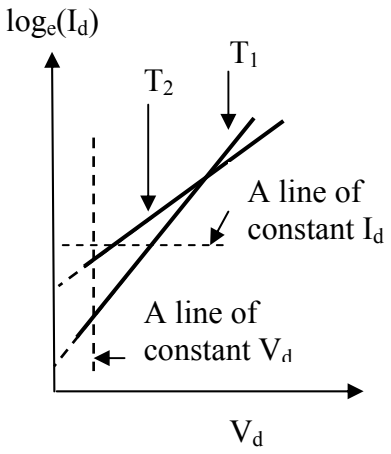
Note that $I_S(T) \sim \exp\left(-\frac{qE_g}{kT}\right)$ where E_g is the bandgap of silicon. Both terms on the RHS of the equation for I_C are strongly temperature dependent.

Now consider an experiment where the diode is heated from a temperature T_1 to T_2. The current is plotted on $\log_e$ – linear scales for the two cases and is sketched below.

Note that the pre-exponential term increases and the gradient (slope) of the line decreases.

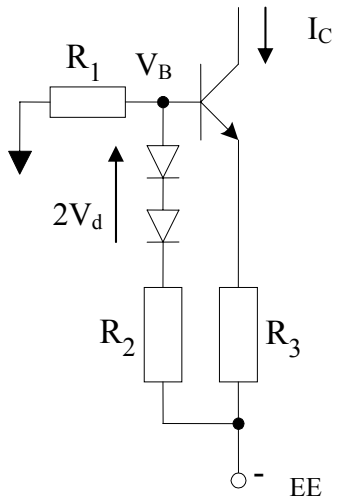
Consider a line of constant I_d. The voltage across the diode, V_d is smaller for the same current at higher temperature.

Now consider a line of constant V_d. The current through the diode is higher for the higher temperature.



Thus we have one variable increasing with increasing temperature (the current through the diode) and another decreasing as temperature increases, the voltage across the diode.

Looking again at the temperature compensated current source, it is now possible to see how it works. If the temperature of the circuit increases, the I_C of the transistor will tend to increase, but the voltage drop across the diodes in the base bias arrangement ($2V_d$), tends to decrease, This drop causes the voltage at V_B to drop hence the V_{BE} of the transistor becomes smaller and this prevents the I_C rising very much!

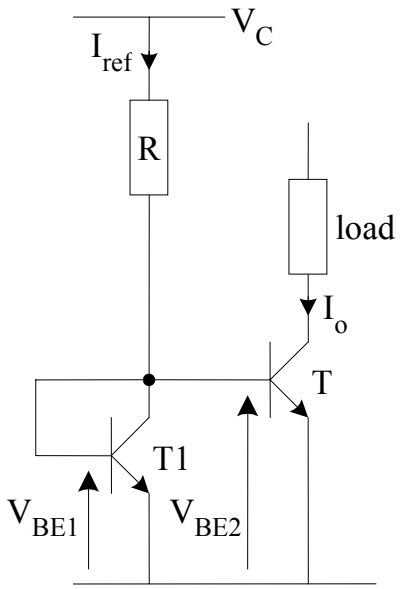


We have found phenomena with differing temperature coefficients and arranged that they 'fight' each other, resulting in very small temperature variation of the current overall.

Further biasing techniques: Current mirrors

This is a very useful circuit to create a temperature compensated current source. It is widely used in integrated circuit designs, because all the transistors are produced at the same time in the same piece of silicon – hence it easy to produce matched transistors that also share the same thermal environment. These are key requirements for the circuit to operate effectively.

Consider the simple current mirror circuit shown below, where 'load' could be the differential amplifier.



Notice that the $V_{BE1} = V_{BE2}$ (= V_{BE}) and so if the transistors are identical, the collector currents must be the same also ($I_{C1} = I_{C2} = I_O$) . Hence

$$I_{ref} = I_{C1} + 2I_B = I_C + 2\frac{I_C}{\beta}$$

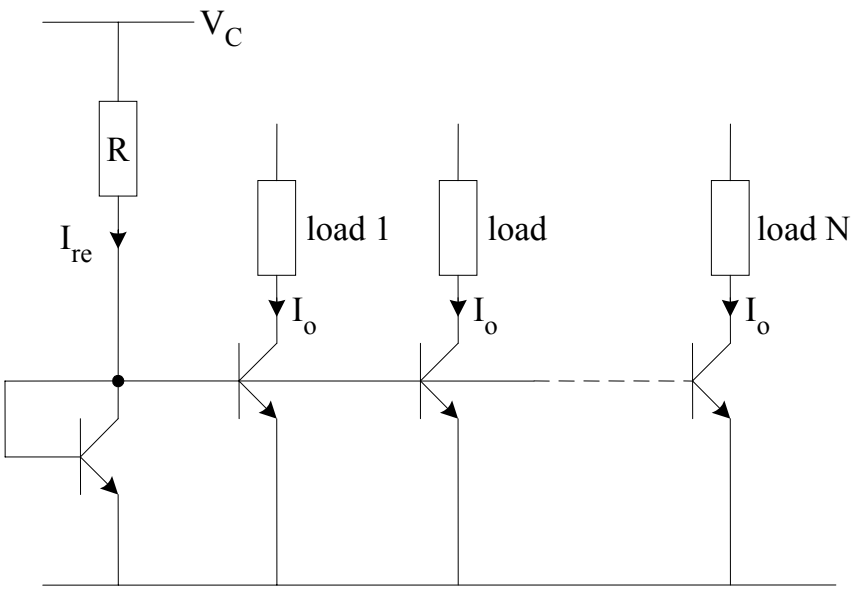
i.e. $$I_{ref} = I_O + 2\frac{I_O}{\beta}$$

$$I_o = \frac{I_{ref}}{1 + 2/\beta} \approx I_{ref}$$

where $$I_{ref} = \frac{V_{CC} - V_{BE}}{R}$$

Thus I_{ref} is set by choosing R and this current is 'mirrored' in T_2 to provide I_O. The advantage of this form of current source becomes apparent from the circuit below where it is seen that a number of current sources can be created to provide bias in different parts of a more complex circuit.

Current Repeater



$$I_{ref} = \frac{V_{CC} - V_{BE}}{R}$$

it's easy to show that

$$I_o = \frac{I_{ref}}{1 + (N+1)/\beta}$$

Problem is that the same current is produced in each load and usually, different bias currents will be required. It is possible to scale the currents by making the transistors with different areas as

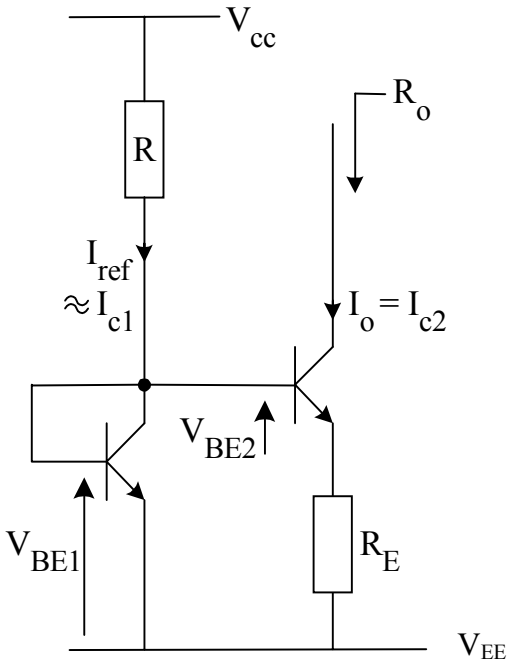
$$I_{C1} = I_{S1} \exp\left(\frac{V_{BE}}{V_T}\right) \qquad I_{C2} = I_{S2} \exp\left(\frac{V_{BE}}{V_T}\right)$$

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{S1}}{I_{S2}} = n \quad \text{so} \qquad I_o = n\, I_{ref}$$

small values of 'n' can be produced this way but bias currents may differ by factors of ten and more so the transistors would have be very large. A better way to scale the bias currents is to use a 'Widlar' current mirror.

Widlar current mirror

The circuit is shown opposite. Ignoring base currents:



$$V_{BE1} = V_{BE2} + I_o R_E$$

$$I_o R_E = V_{BE1} - V_{BE2}$$

$$I_{C1} = I_S \exp\left(\frac{V_{BE1}}{V_T}\right) \sim I_{ref}$$

$$I_{C2} = I_S \exp\left(\frac{V_{BE2}}{V_T}\right) \sim I_o$$

hence

$$V_{BE1} = V_T \ell n\left(\frac{I_{ref}}{I_S}\right)$$

$$V_{BE2} = V_T \ell n\left(\frac{I_O}{I_S}\right)$$

and $\boxed{R_E I_O = V_T \ell n\left(\frac{I_{ref}}{I_O}\right)}$.

This is the basic design equation. We can set different currents in current repeaters by incorporating different emitter resistors (R_E)

Exercise: Find values for R, R_E to give a bias current of I_o = 0.1mA. (assume $V_{RE} \sim 4V_T$= 0.1V for stability).
Given: V_{CC} = 5V, V_{EE} = -5V, transistors have current gains $\beta = \beta_o = 100$ and V_A = 150V.
What will be the value of I_{ref}? Comment on your answer.

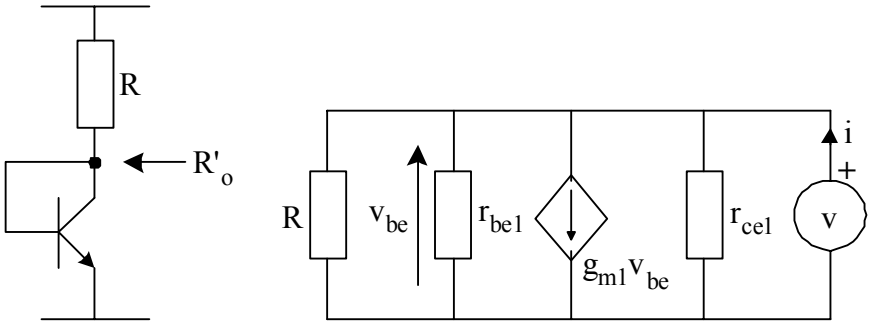
Solution: see lecture: **Ans:** R = 1.7kΩ and R_E = 1kΩ. I_{ref} = 5.5mA.

NOTE also: g_{m1} = (40 *x* 5.5mA) = 220 mA/V,
g_{m2} = (40 *x* 0.1 mA) = 4 mA/V,
$r_{ce2} = V_A/0.1\text{mA} = 150/0.1\text{mA} = 1.5\text{M}\Omega$

Now we work out an expression for the ac resistance, R_o and hence find a numerical value for R_o.

We will now perform an ac analysis of the CM using the values we have obtained above
a.c. analysis – to find the output resistance (R_o) of our current source

It is convenient to split the circuit into two to simplify the analysis. Consider:



Note that the dependent current source, $g_{m1}v_{be1} = g_{m1}v$ as $v_{be1} = v$!

So we have a current source of $g_{m1}v$ with a voltage 'v' across it – from ohms law this is equivalent to a resistor of value $1/g_{m1}$.

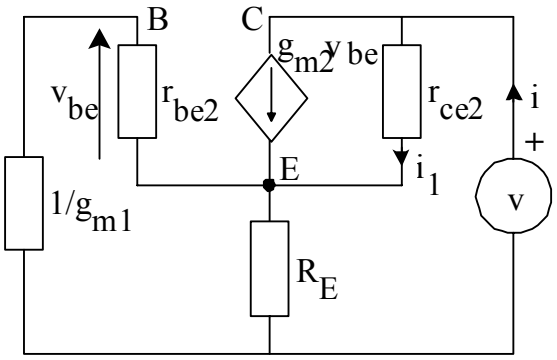
We can see that $$\boxed{R_o' = R // r_{be1} // r_{ce1} // \frac{1}{g_{m1}} \approx \frac{1}{g_{m1}}}$$

Justify approximation: $g_{m1} = 40 x I_{ref} = 40 x 5.46mA \sim 218mA/V$; R = 1.7k

$$\frac{1}{g_{m1}} = \frac{1}{218m} \sim 5\Omega ; \; r_{be1} \sim \frac{\beta_o}{g_{m1}} = \frac{100}{218x10^{-3}} \sim 460\Omega ; \; r_{ce} \sim \frac{V_A}{I_{ref}} = \frac{150}{5.5x10^{-3}} = 28k\Omega$$

Clearly 5Ω will dominate the parallel connections! and $R_o' \approx \frac{1}{g_{m1}}$

Incorporating this into the second part of the circuit we get the ac equivalent circuit below. Again, we apply a voltage source to force a current, *i,* into the output of our current source. The aim then is to find $\boldsymbol{R_o = v/i}$



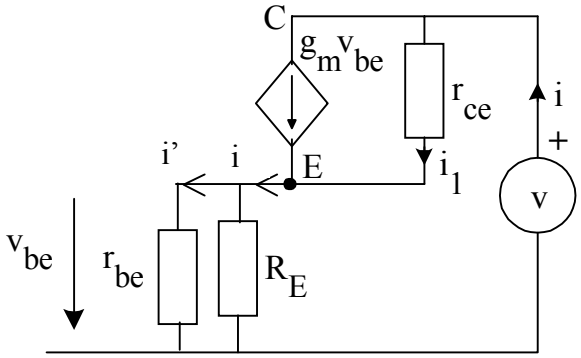
Can we make a further approximation?

$1/g_{m1} \sim 5\text{ohms}$ and

$$r_{be2} = \frac{\beta_o}{g_{m2}} = \frac{100}{40xI_o} = \frac{100}{40x0.1mA} = 25k\Omega$$

So $r_{be2} >> 1/g_{m1}$!

The schematic circuit is re-drawn below on the right. We have managed to reduce the original circuit to quite a simple one. We drop the subscript '2' for simplicity.



Now we can write

$$i = g_m v_{be} + \frac{v - (-v_{be})}{r_{ce}} \qquad (1)$$

$$i = \left(g_m + \frac{1}{r_{ce}}\right)v_{be} + \frac{v}{r_{ce}}$$

Need to find v_{be}: consider current division at 'E'

$i' = i\dfrac{R_E}{r_{be}+R_E} = -\dfrac{v_{be}}{r_{be}}$ (note V-drop across r_{be}) - and this can be re-arranged: $v_{be} = -iR_E // r_{be}$

substitute $v_{be} = -iR_E // r_{be}$ into Eqn.1 to get: $i = -\left(g_m + \dfrac{1}{r_{ce}}\right)iR_E // r_{be} + \dfrac{v}{r_{ce}}$

$$R_O = \frac{v}{i} = r_{ce}\left[1 + \left(g_m + \frac{1}{r_{ce}}\right)R_E // r_{be}\right]$$ …complicated expression!

But we can also say $\mathbf{g_{m2} >> 1/r_{ce2}}$ (4m >> 0.1m/150~ 10^{-6}) giving $R_O \sim r_{ce}\left[1 + \dfrac{R_E r_{be} g_m}{R_E + r_{be}}\right]$

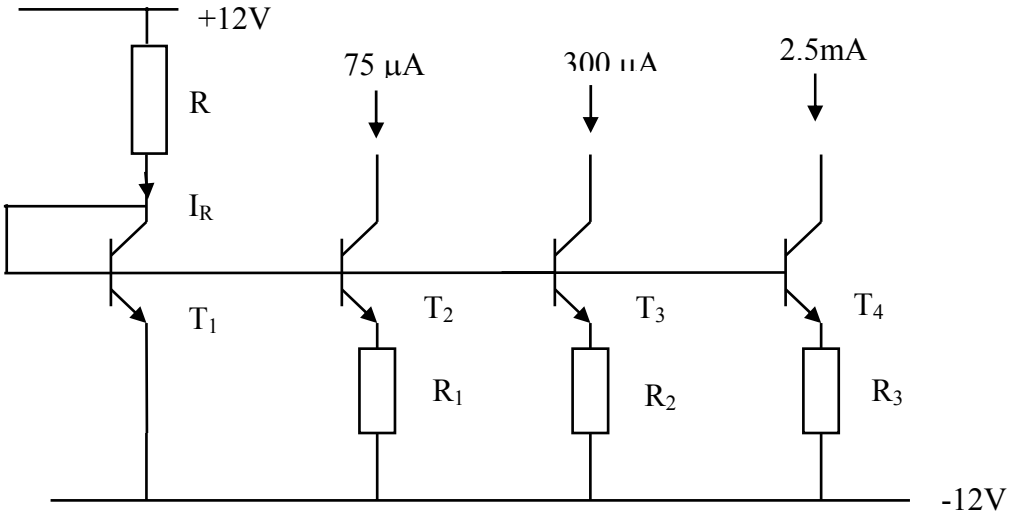
Finally if $\mathbf{R_E << r_{be2}}$ (1k < 25k)

OUTPUT RESISTANCE IS SIMPLY $R_O \sim r_{ce}\left[1 + g_m R_E\right]$

Now $R_E g_m = \dfrac{R_E I_O}{V_T}$ and $R_E I_O$ is the voltage drop across R_E. We see therefore that we require at least a few thermal volts (25mV) across R_E to 'multiply up' the transistor output resistance r_{ce} to give a large R_o for our current source.

Example: (January 1999)

An operational amplifier comprises three stages with bias requirements of 75 μA, 300 μA and 2.5 mA. Sketch the circuit and design the current mirror arrangement to provide these bias currents. Assume power supplies of ± 12V, identical transistors with Early voltages, V_A = 100 V, V_T =25 mV and V_{BE} = 0.7V. Take $r_{ce} = V_A/I_C$.



Choose $\mathbf{I_R = 2.5mA}$ then $R_3 = 0$ (simple current mirror) and

$$R = \frac{V_{CC} - (-V_{EE} + V_{BE})}{I_R} = \frac{V_{CC} + |V_{EE}| - V_{BE})}{I_R} = \frac{24 - 0.7}{2.5.10^{-3}} = 9.3k\Omega$$

$$R_1 = \frac{V_T}{I_{O1}} \ell n\left(\frac{I_R}{I_{O1}}\right) = \frac{25.10^{-3}}{75.10^{-6}} \ell n\left(\frac{2.5.10^{-3}}{75.10^{-6}}\right) = 1.17k\Omega$$

$$R_2 = \frac{V_T}{I_{O2}} \ell n\left(\frac{I_R}{I_{O2}}\right) = \frac{25.10^{-3}}{300.10^{-6}} \ell n\left(\frac{2.5.10^{-3}}{300.10^{-6}}\right) = 177\Omega$$

Estimate the a.c. resistance looking into each of the three bias stages. State carefully any approximations used in your estimation. Comment on the values you obtain.

Output resistances : First work out transistor transconductances and output resistances:

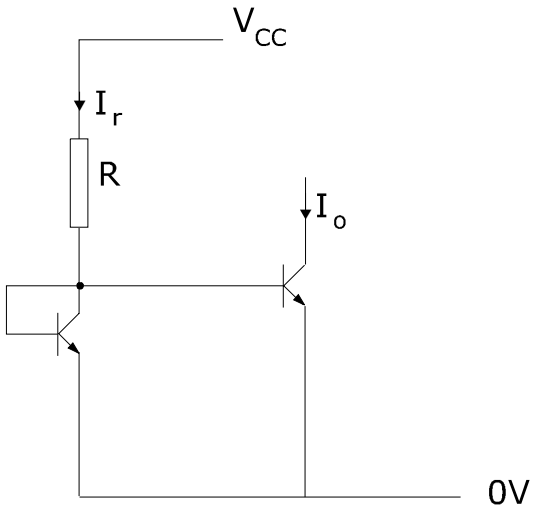
$g_{m1} = 40\ I_R = 40\ x\ 2.5$ mA = 100 mS,
$g_{m2} = 40\ I_{o1} = 40\ x\ 75$ uA = 3 mS, $r_{ce2} = 100/75$ uA = 1.3 MΩ
$g_{m3} = 40\ I_{o2} = 40\ x\ 300$ uA = 12 mS, $r_{ce3} = 100/300$ uA = 333 kΩ
$g_{m4} = 40\ I_R = 40\ x\ 2.5$ mA = 100 mS, $r_{ce4} = 100/2.5$ mA = 40 kΩ

Assume that the 'loading' effect of adjacent stages is negligible: the resistance from the collector/base of T_1 (taken alone) to ground is $1/g_{m1} = 1/1\ \Omega$ and this is much less than a.c. resistance from other bases to ground (appear in parallel). Therefore:

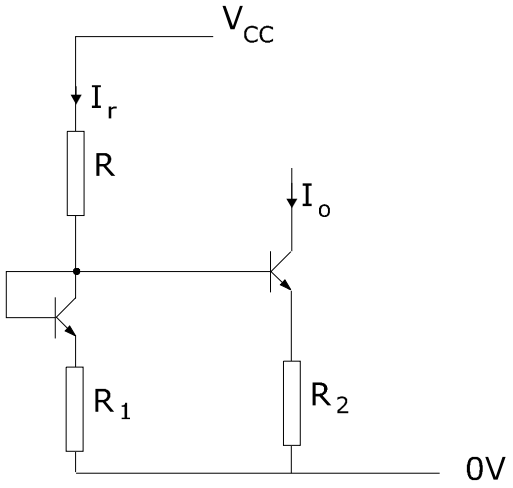
$$R_{o2} \sim r_{ce2}\left[1 + g_{m2}.R_1\right] = 1.3.10^6\left[1 + 3.10^{-3}1.17.10^3\right] = 5.86M\Omega$$
$$R_{o3} \sim r_{ce3}\left[1 + g_{m3}.R_2\right] = 333.10^3\left[1 + 12.10^{-3}.177\right] = 1.04M\Omega$$
$$R_{o4} \sim r_{ce4}\left[1 + g_{m4}.0\right] = 40.10^3 = 40k\Omega$$

Exercises

The bias current I_o in the current mirror in the figure below is required to be 10 μA. The maximum emitter area ratio for the two transistors is 5. Which transistor should have the larger area and what is the value of R required? Explain why the circuit is unsatisfactory for an IC design. V_{CC} = 30 V.



It is proposed instead to use the circuit in the figure below, in which the transistors are identical.



Show that:

$$\frac{I_o R_2}{I_E R_1} - 1 \approx \frac{V_T}{I_r R_1} \ln \frac{I_r}{I_o}$$

where $V_T = kT/q$. Assume negligible base currents. If I_r = 1 mA select values for R, R_1 and R_2 to achieve I_o = 10 μA. Resistor values should be less than 50 kΩ. Assume V_T = 25 mV.