Electronic circuits and systems
ELEC271

Part 3
The Differential amplifier – I

Another important circuit building block

How does it work and what does it do?

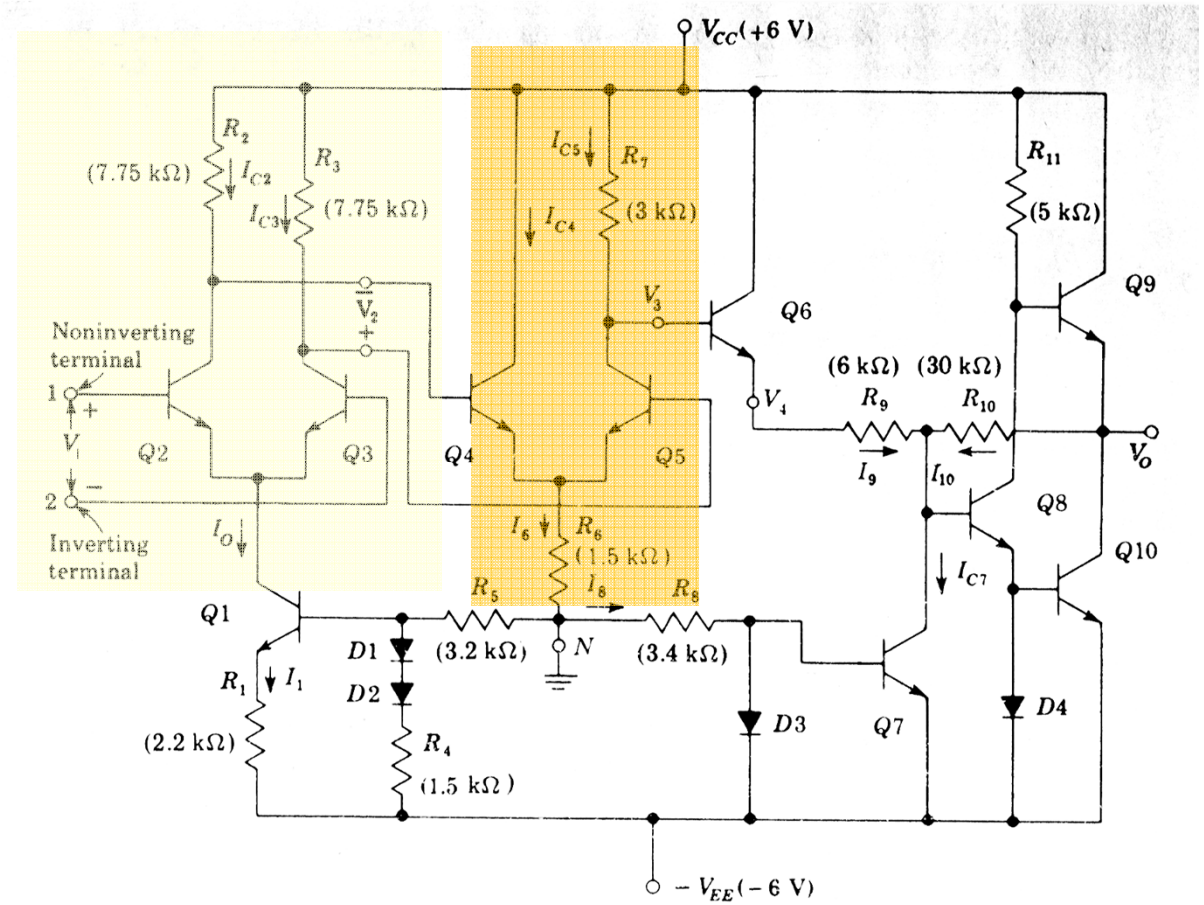
How to analyse?

How to design it?

A target for week 4…

By about week 4 we will be able to:

- Identify circuit ‘building blocks’
- Perform a dc analysis to estimate all currents and voltages
- Perform an ac analysis to estimate gain of amplifier



Motorola MC1350 operational amplifier

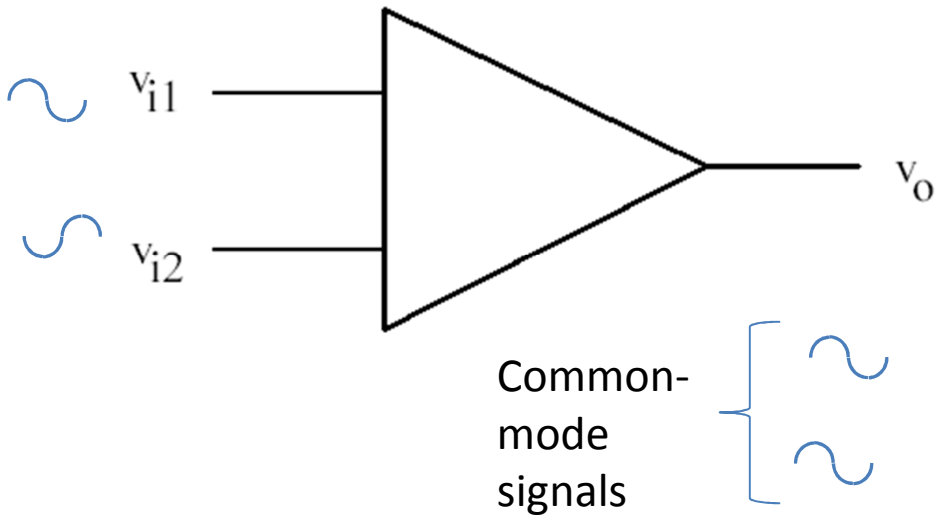
Differential amplifier principles

- amplifies the difference between two signals.

Ideally:-

$$v_o = A_d(v_{i1} - v_{i2})$$

Note that signals that are common mode (CM), that is same phase, will not affect v_o.



Reality:-

Amplifer **will** amplify CM signals. We define:

Differential mode $v_{id} \equiv (v_{i1} - v_{i2})$ (1)

Common mode $v_{ic} \equiv \frac{1}{2}(v_{i1} + v_{i2})$ (2)

Why the factor ½?

Principles (contd)

$$v_{id} \equiv (v_{i1} - v_{i2})$$
$$v_{ic} \equiv \frac{1}{2}(v_{i1} + v_{i2})$$

Why the factor ½?

Consider:- v_{i1} = + 50 μV, v_{i2} = - 50 μV (No CM signal) compared to v_{i1} = 1050 μV, v_{i2} = 950 μV (**CM signal of 1000 μV**)

Corresponding DM and CM inputs are

v_{id} = + 100 μV and v_{id} = + 100 μV

v_{ic} = 0 V v_{ic} = 1000 μV

without the factor ½, the common mode for the second case would be considered incorrectly as 2000 μV: the average value of CM input must be used.

What is this 'common mode' signal? It is unwanted noise and interference that will be picked up on the two input pins of the amplifer - usually same in phase and magnitude.

Common-mode rejection ratio

This is a figure of merit for the amplifier which tells us how good it is at rejecting the unwanted signal (CM) relative to the one we want to amplify (DM).

First express output as a linear combination of the two inputs:

$$v_o = A_1 v_{i1} + A_2 v_{i2} \qquad (3)$$

Voltage amplification factor of input 1 with input 2 grounded

Voltage amplification factor of input 2 with input 1 grounded

[(1) + (2)] →

[(1) – (2)] →

Then, from Eqn.s 1,2:

$$v_{i1} = \frac{1}{2} v_{id} + v_{ic} \qquad v_{i2} = -\frac{1}{2} v_{id} + v_{ic}$$

Substitute in Eqn.3 to get

$$v_o = A_d v_{id} + A_c v_{ic} \qquad (4)$$

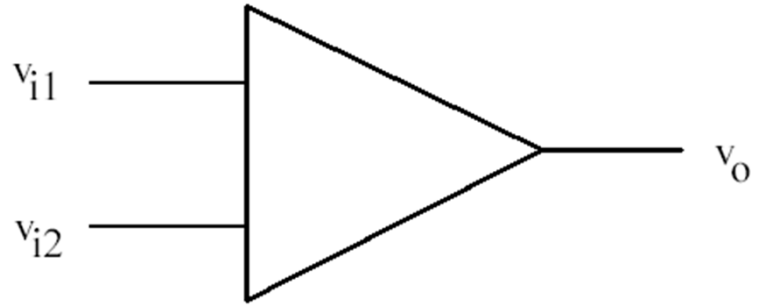
$$v_{id} \equiv (v_{i1} - v_{i2})$$

$$v_{ic} \equiv \frac{1}{2}(v_{i1} + v_{i2})$$

where $A_d \equiv \frac{1}{2}(A_1 - A_2)$ $\qquad A_c \equiv (A_1 + A_2)$

Interpretation

$$v_o = A_d v_{id} + A_c v_{ic}$$



Want $A_d >> 1$, $A_c \rightarrow 0$ for a good diff. amp. Define:

$$CMRR = \rho = \left| \frac{A_d}{A_c} \right|$$

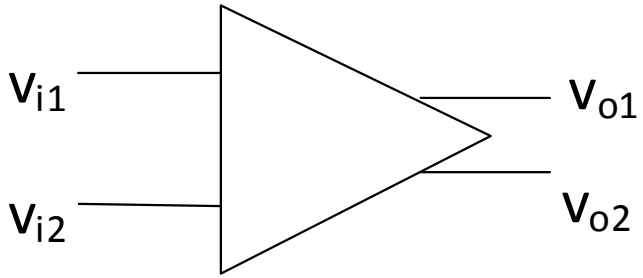
so Eqn 4 becomes $$v_o = A_d v_{id} \left(1 + \frac{1}{\rho} \frac{v_{ic}}{v_{id}} \right)$$ $$v_o \sim A_d v_{id}$$

want ρ large. Examples of commercial op-amps:

741	ρ = 70 – 90 dB	(3,000 to 30,000)
OP07	ρ = 94 – 106 dB	(50,000 to 200,000)

Sometimes there are two outputs

Convention is therefore



Inputs

$$v_{i1} = \frac{v_{id}}{2} + v_{ic}$$

$$v_{i2} = -\frac{v_{id}}{2} + v_{ic}$$

Outputs

$$v_{o1} = \frac{v_{od}}{2} + v_{oc} \qquad \left(= A_d \frac{v_{id}}{2} + A_c v_{ic}\right)$$

$$v_{o2} = -\frac{v_{od}}{2} + v_{oc} \qquad \left(= -A_d \frac{v_{id}}{2} + A_c v_{ic}\right)$$

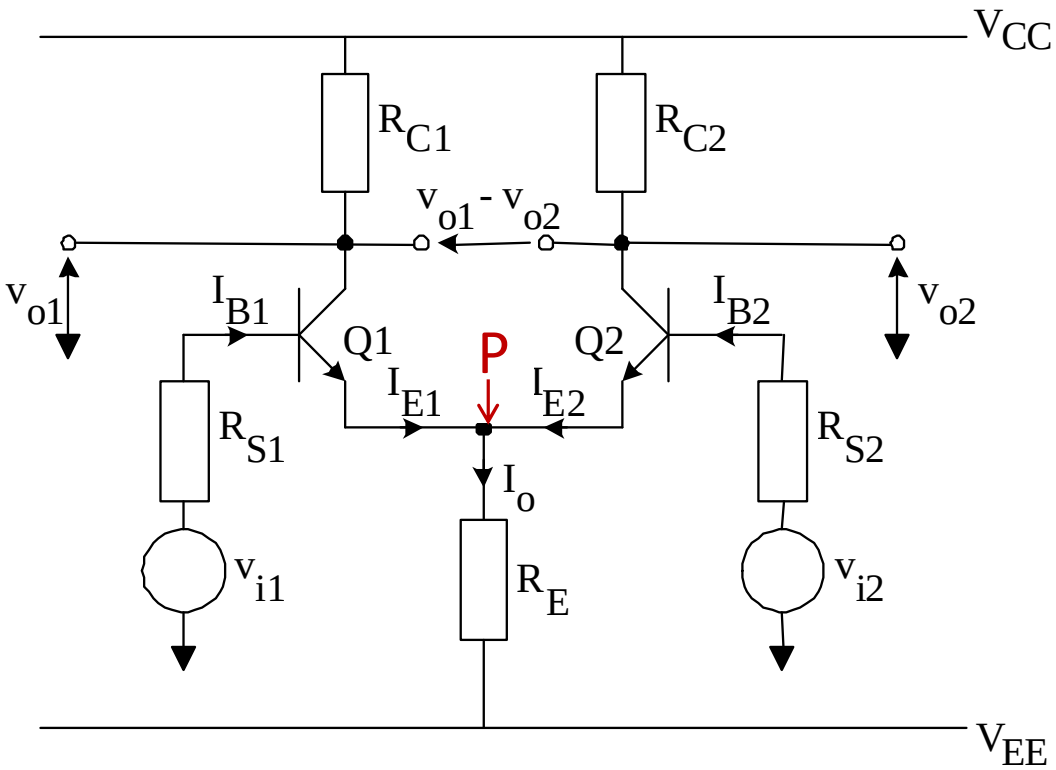
Diff. mode gain: $$A_d = \frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} = \frac{v_{od}}{v_{id}}$$

Common mode gain $$A_c = \frac{v_{o1} + v_{o2}}{v_{i1} + v_{i2}} = \frac{v_{oc}}{v_{ic}}$$

$$CMRR = \rho = \left|\frac{A_d}{A_c}\right|$$

We now consider a real circuit.

The differential amplifier
(or 'long-tail pair', or emitter-coupled amplifier)



Question:
Why are split supply rails used?

d.c. conditions
($v_{i1} = v_{i2} = 0$).
Neg. supply rail biases
Q1,2 on
- R_E sets the current.
- Assume that the transistors do not saturate
-small I_B causes little voltage drop so that the base of Q1, 2 ~ 0 V.
= Point P will be at ~ – 0.7 V
due to the forward biased B/E

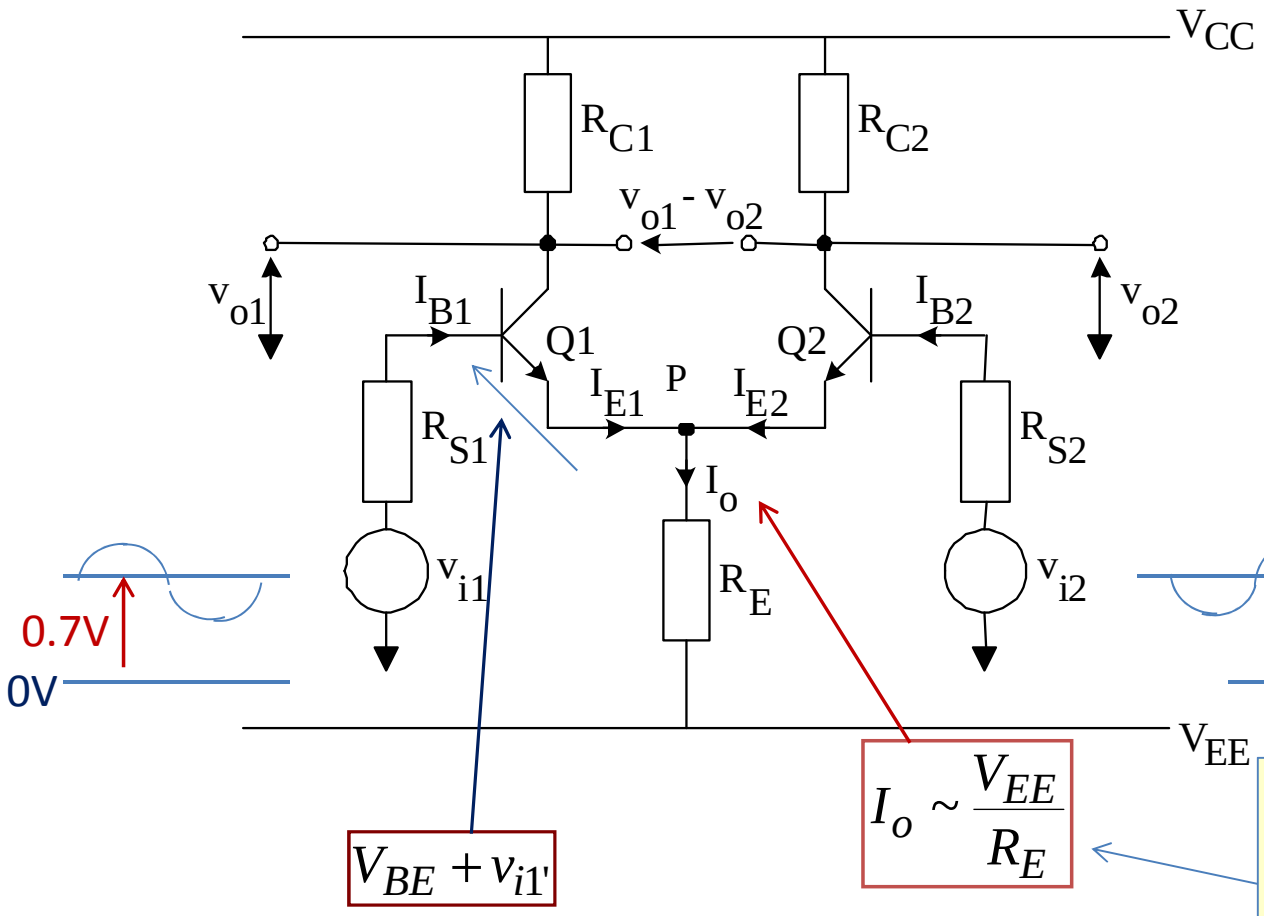
$$I_o \approx \frac{|V_{EE}| - 0.7}{R_E}$$

R_E and V_{EE} constitute a simple current source

Response to **ac signals: Diff. mode**

Consider the application of test sine waves to the inputs,

RECALL: $I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$



I_{C1} ↑ so v_{o1} ↓

I_{C2} ↓so v_{o2} ↑

o/p is $(v_{o1} - v_{o2})$

AC signal

DC bias

0.7V

0V

0.7V

0V

$V_{BE} + v_{i1}$

$I_o \sim \frac{V_{EE}}{R_E}$

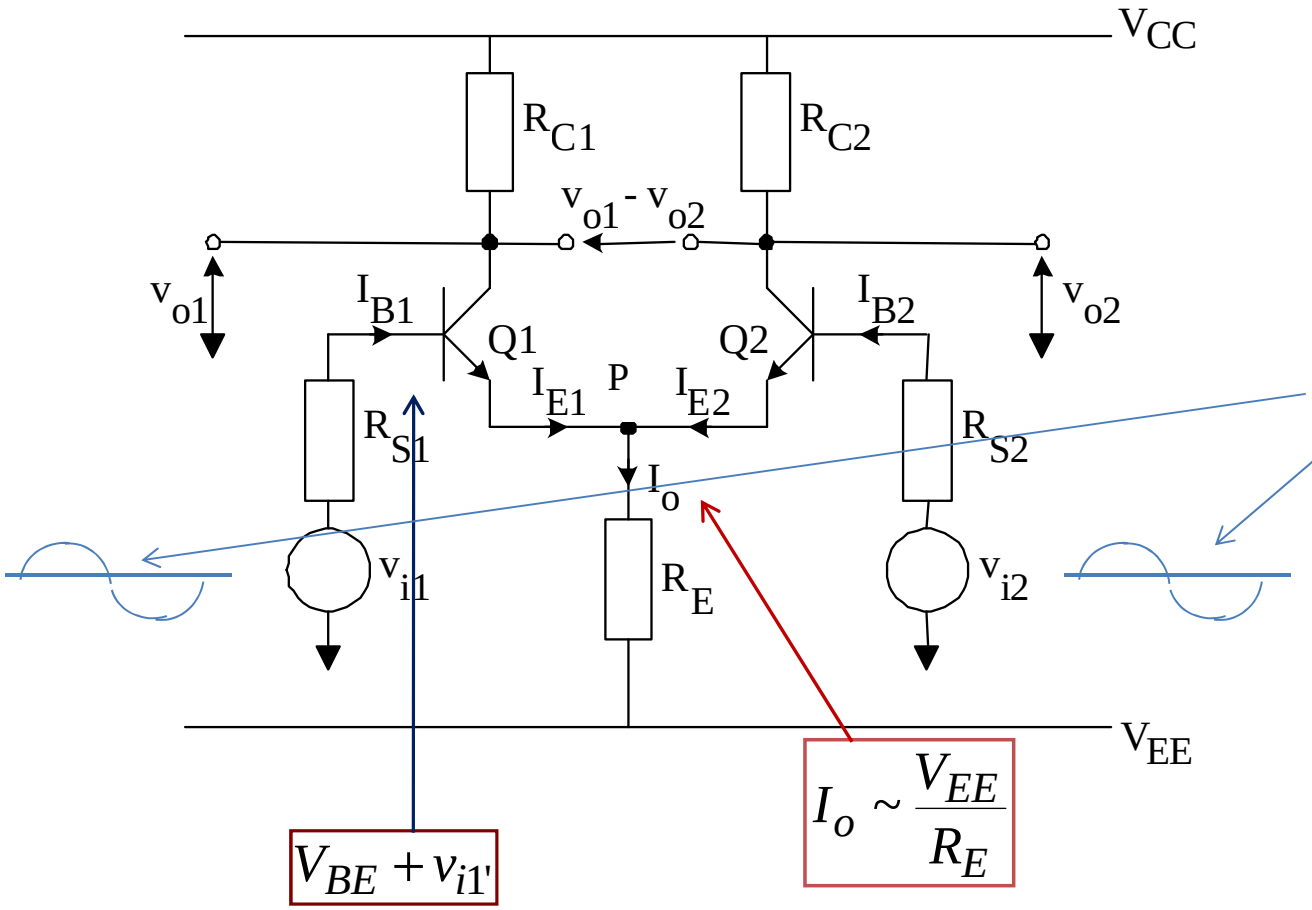
A simple DC current source! For biasing

$I_C = I_S \exp\left(\frac{V_{BE} + v_{i1}}{V_T}\right)$

Response to **ac signals: Common mode**

Consider the application of test sine waves to the inputs,

RECALL: $I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$



Same signals both sides!

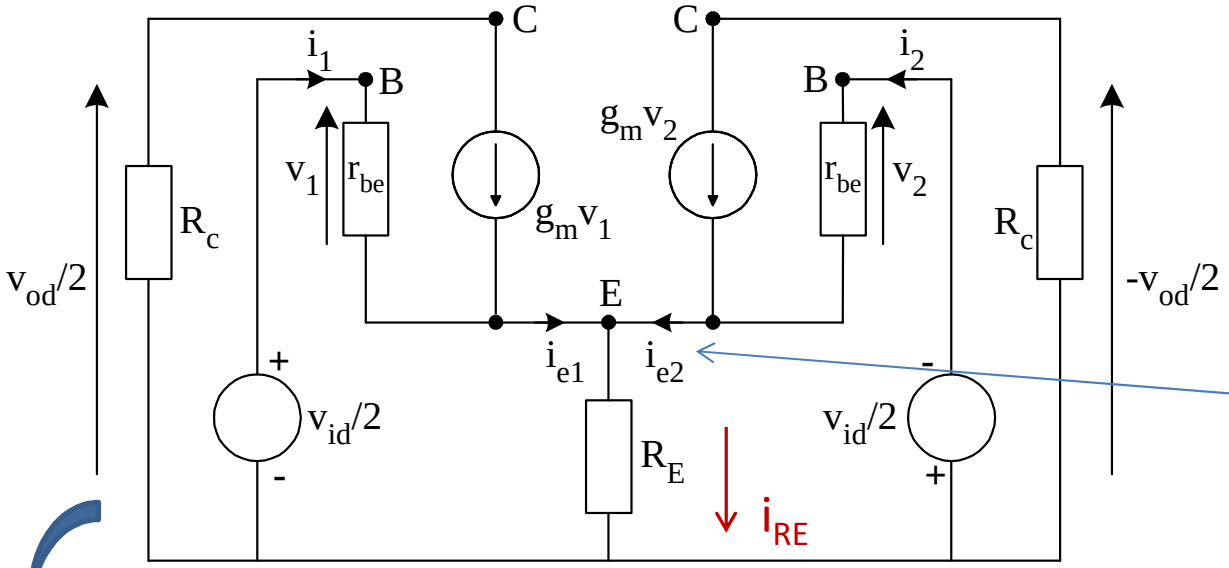
I_{C1} ↑ so v_{o1} ↓

I_{C2} ↑ so v_{o2} ↓

$(v_{o1} - v_{o2}) = 0$!

Small-signal analysis

Differential inputs

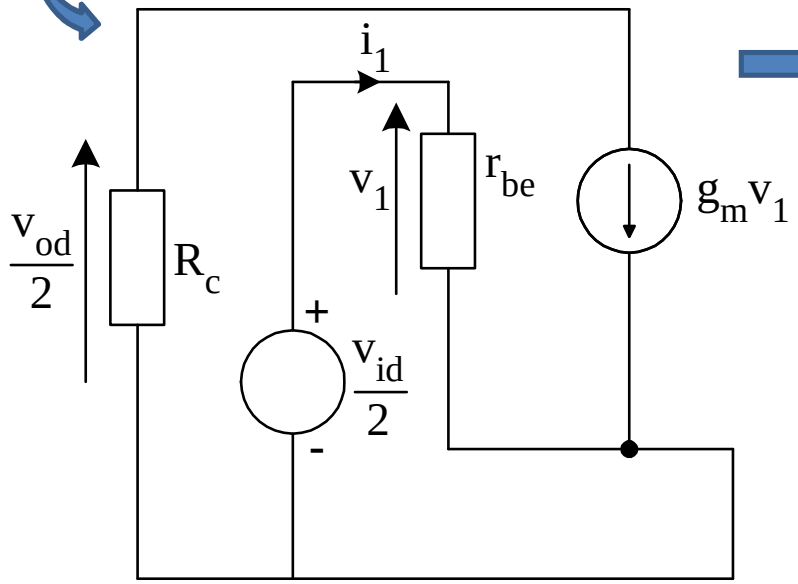


Assuming identical Q's

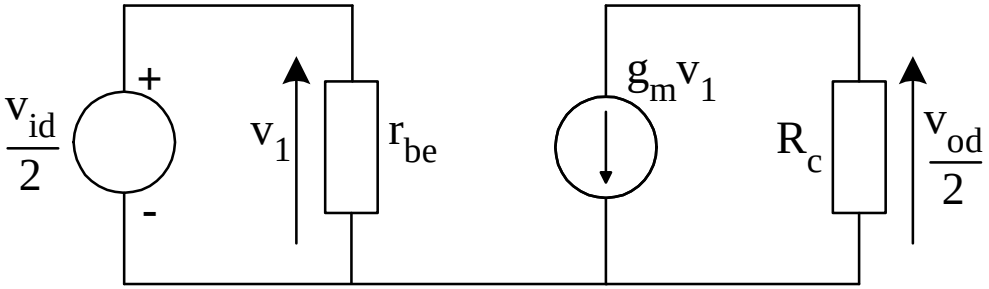
$i_{e1} = - i_{e2}$!

So i_{RE} = doesn't change!

It's an 'ac ground'



Just consider one side of the circuit



$$i(R_C) = -g_m v_1$$

$$\frac{v_{od}}{2R_C} = -g_m \frac{v_{id}}{2}$$

$$A_d \equiv \frac{v_{od}}{v_{id}} = -g_m R_C$$

$$A_d = -40\left(\frac{I_o}{2}\right)R_C$$

Interpretation

$$A_d = -20 I_o R_C$$

- we have assumed $R_{C1} = R_{C2} = R_C$ (see exercise 1.b at the end of the handout for another case).
- **Thus a higher bias current leads to a higher voltage gain.**
- **Taking the output single ended gives**:

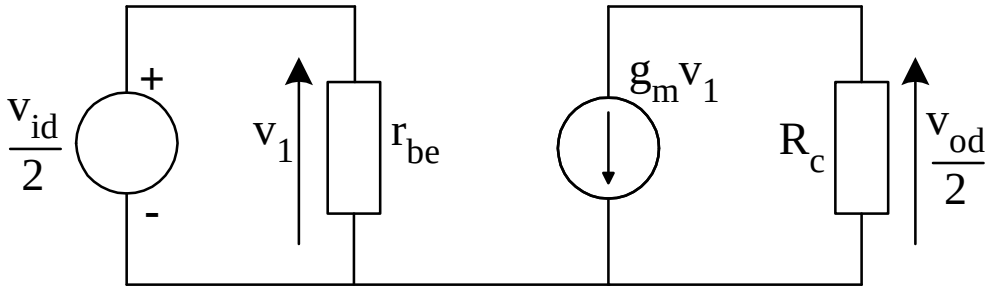
$$\begin{cases} A_{d1} = \dfrac{v_{o1}}{v_{i1} - v_{i2}} = -g_m \dfrac{R_{C1}}{2} \\ A_{d2} = \dfrac{v_{o2}}{v_{i1} - v_{i2}} = +g_m \dfrac{R_{C2}}{2} \end{cases}$$

- Note for single ended output, the gains are exactly half the voltage gain of double ended output or simple common emitter amplifier (why?).
- **Thus the voltage gain can be increased by increasing the value of collector resistor.**
- However, there is considerable constraint because of the need to avoid saturation in the transistors. This will lead us to use an 'active load' (see later lecture).

Design issues

The 'differential' input resistance of the D-M configuration is given approximately by:

$$R_{id} = \frac{v_{id}}{i_i} = \frac{2v_1}{i_i} = 2r_{be}$$



$$R_{id} = 2r_{be} = 2\frac{\beta_o}{g_m} = 2\frac{\beta_o}{40I_C} = \frac{\beta_o}{10I_o}$$

thus the operating current must be chosen small to increase the input resistance.

$$R_{id} = \frac{\beta_o}{10I_o} \qquad \textbf{(Eqn. 1)}$$

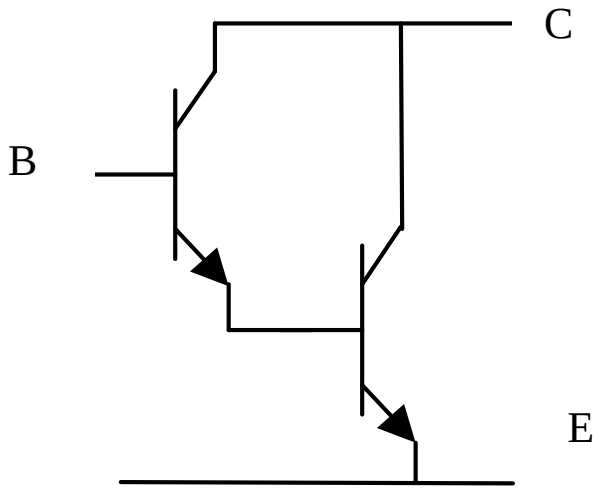
BUT want bias, I_c large for high gain!!

$$A_d = -20I_oR_C \qquad \textbf{(Eqn.2)}$$

$\Rightarrow$ We have an engineering trade-off as I_o must be large for high voltage gain (Eqn.2) and small for large input resistance (Eqn. 1).

Alternatively, R_{id} can be increased by the following methods

1. Use Darlington transistors on the input



Effectively: $\beta_o \rightarrow \beta_o^2$

$r_{be} \rightarrow \beta_o^2/g_m$

Large increase in input resistance

2. Use super gain transistors

Very narrow base transistors – enhances collector current
typically $\beta_o \sim 5{,}000$

For $I_C = 1\mu A$, $\mathbf{r_{be}} = \beta_o/g_m = 5{,}000/40 \times 1\mu A = \mathbf{125\ M\Omega}$

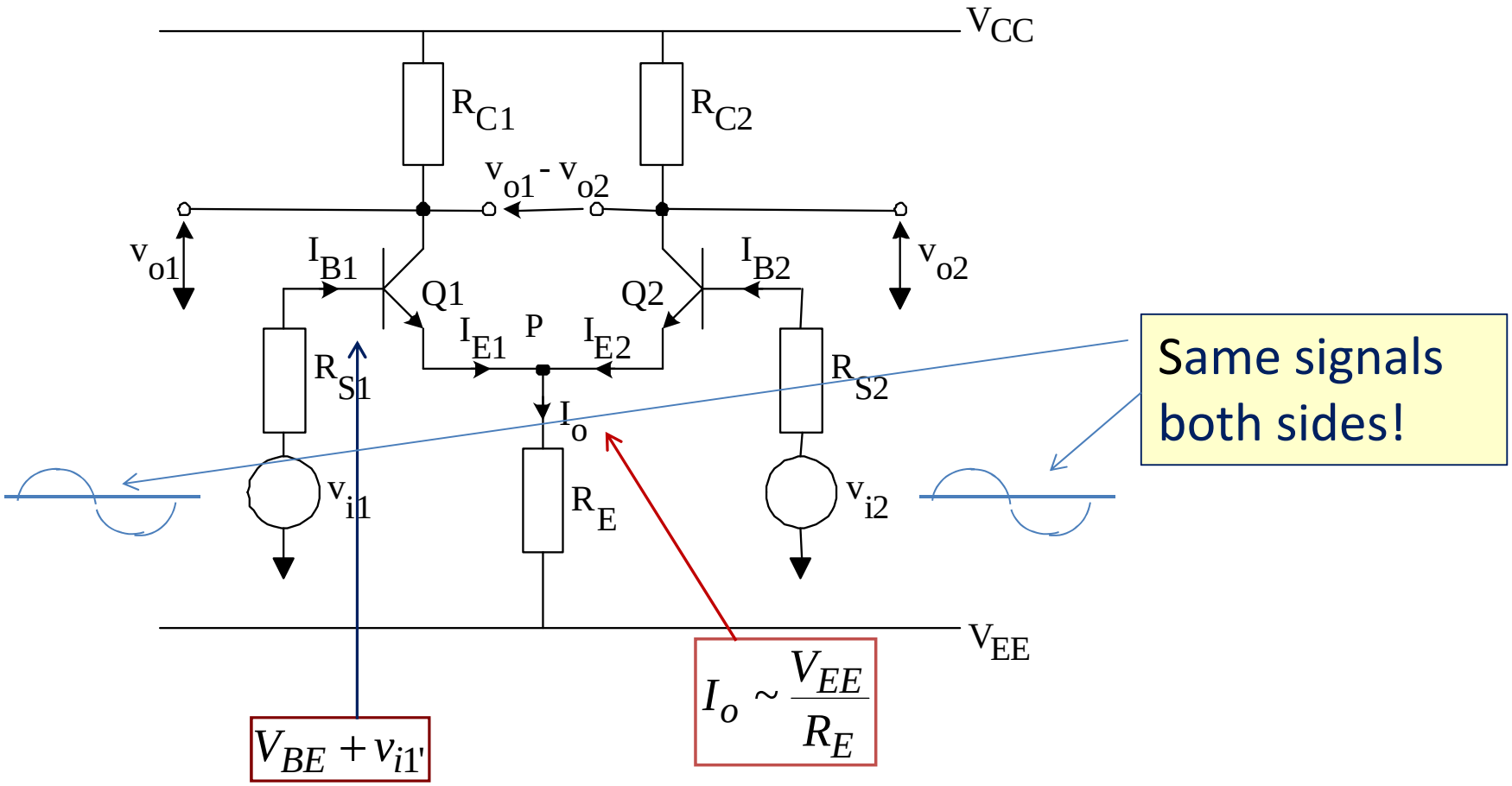
3. Use FET input transistors

JFET	**MOSFET**
$R_{id} \sim 10^8\ \Omega$	$R_{id} \sim 10^{10} - 10^{15}\ \Omega$

Response to **ac signals: Common mode**

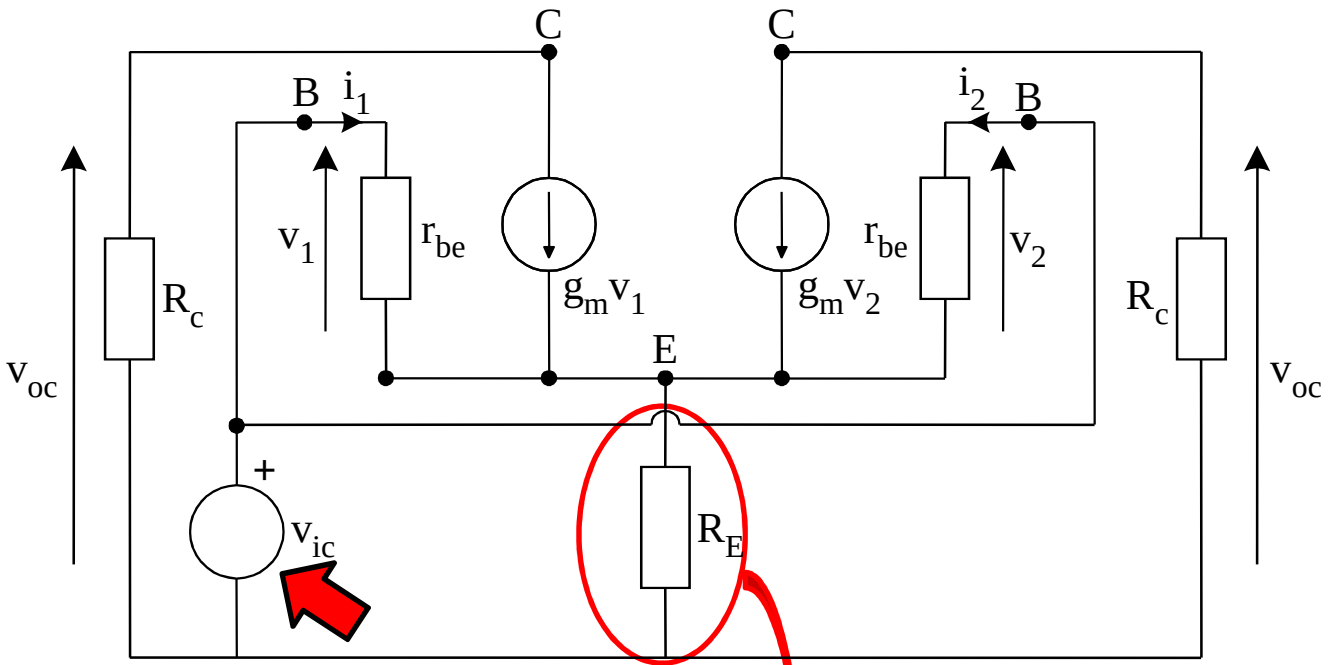
Consider the application of test sine waves to the inputs,

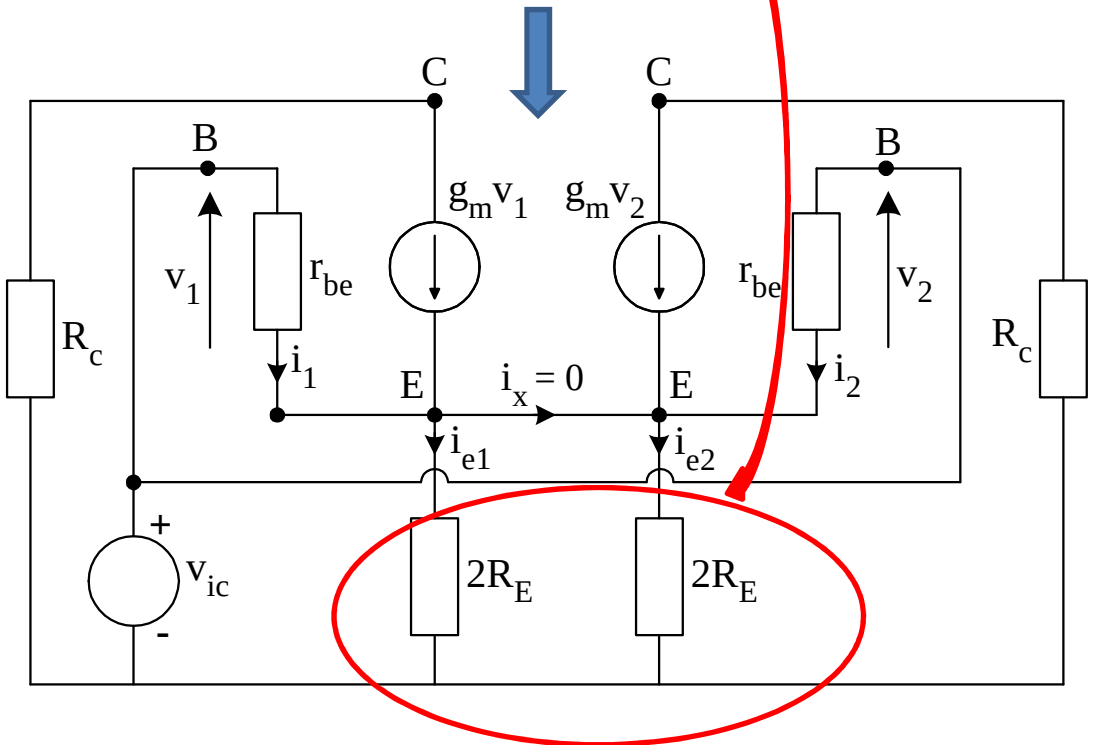
RECALL: $I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$

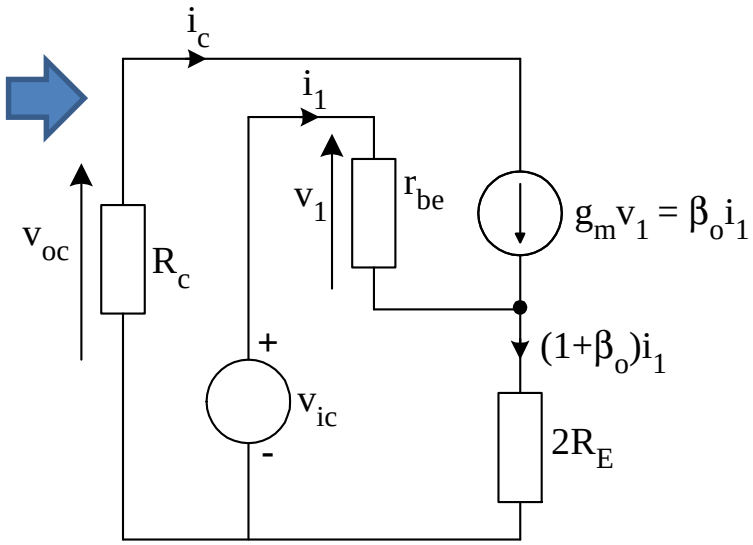


Small-signal analysis

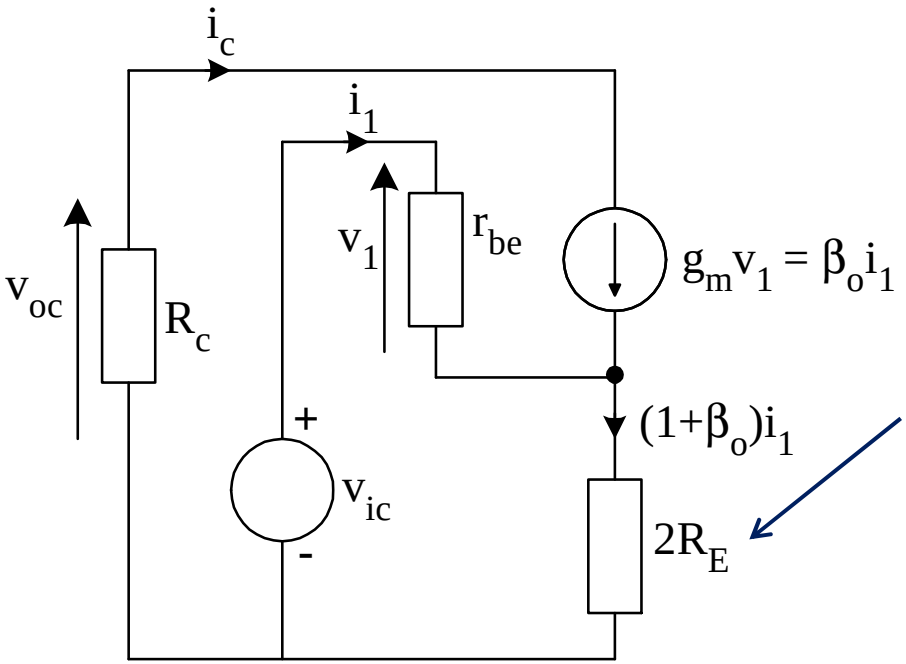
Common-mode inputs







CM - analysis



recognise this as the **CE-ED** configuration (see Part 2 notes).

Common mode signals therefore "see" the emitter resistor which thus severely degrades the common-mode gain.

common mode input resistance can be shown to be

$$R_{ic} = \frac{v_{ic}}{i_i}$$
$$= r_{be} + 2(1+\beta_o)R_E$$

Following the earlier analysis for CE-ED:

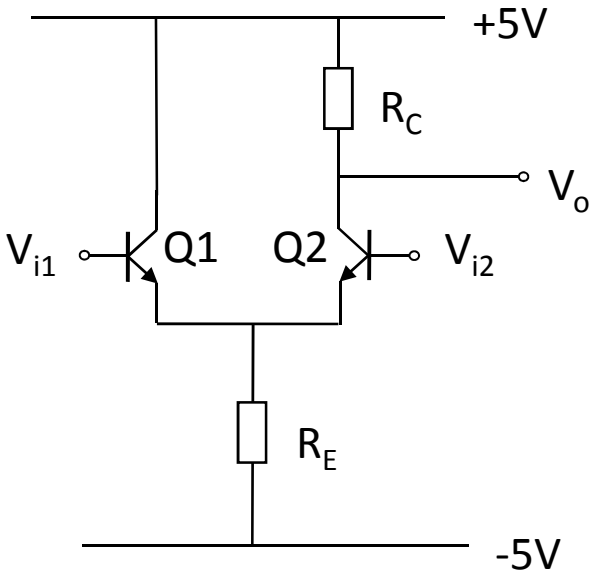
$$A_{Vc} = -\frac{R_C g_m}{1+2\left(g_m + r_{be}^{-1}\right)R_E}$$
$$= -\frac{R_C \beta_o}{r_{be} + 2(1+\beta_o)R_E}$$

$$g_m = \frac{\beta_o}{r_{be}}$$

$\Rightarrow$ **Thus R_E must be large to make A_{Vc} small. However, R_E is also responsible for setting the d-c-. bias condition ?!?**

Design Example 3

Work out values for R_E and R_C to give a bias current of 0.1 mA with V_o = 0 V (DC), β_o = 100



Voltage drop across R_E ?

$$R_E = \frac{V_{EE} - |-0.6|}{0.1m} = \frac{4.4}{0.1} k\Omega$$ **44 kΩ**

Voltage drop across R_C ?

$$R_C = \frac{V_{CC} - 0}{50\ \mu A} = \frac{5}{50} M\Omega$$ **100 kΩ**

Now work out the differential input resistance and voltage gain (β_o = 100)

$R_{id} = 2 \times r_{be} = 2\beta_o / g_m$ g_m= 40 × 50 µA = 2 mA/V R_{id} = 200/2 k = **100 kΩ**

A_{Vd} = g_m × ac load/2 $A_{Vd} = g_m \times R_C / 2$ A_{Vd} = 2m × 100k/2 = **100**

Now work out the common-mode voltage gain

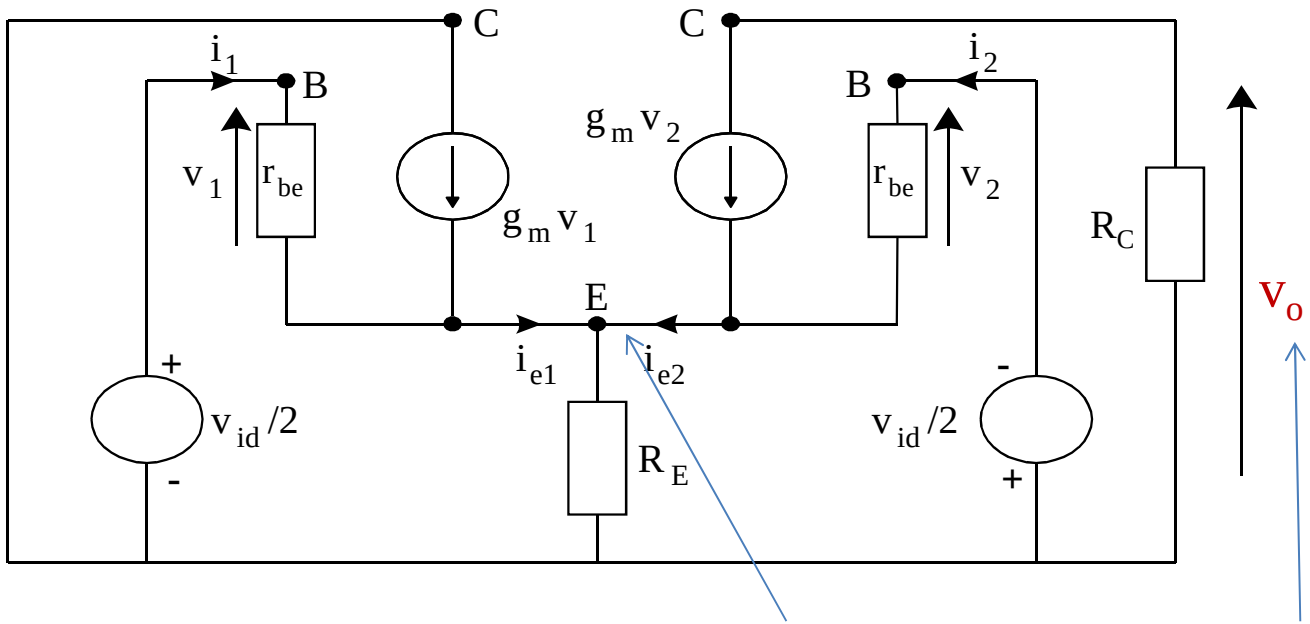
$$A_{VC} = \frac{100k \times 100}{50k + 2(1 + 100)44k}$$ **~ 1**

$$A_{VC} = \frac{R_C \times \beta_O}{r_{be} + 2(1 + \beta_O)R_E}$$

CMRR?

Single-ended output

Show that the voltage gain is $\frac{v_o}{v_{id}} = \frac{g_m R_C}{2}$



ac ground

So

$v_2 = \frac{v_{id}}{2}$

$v_o = -g_m v_2 \times R_C$

$v_o = -g_m R_C \times \frac{-v_{id}}{2}$

$\frac{v_o}{v_{id}} = \frac{g_m R_C}{2}$

Schematic entry in PSPICE

DC Analysis:

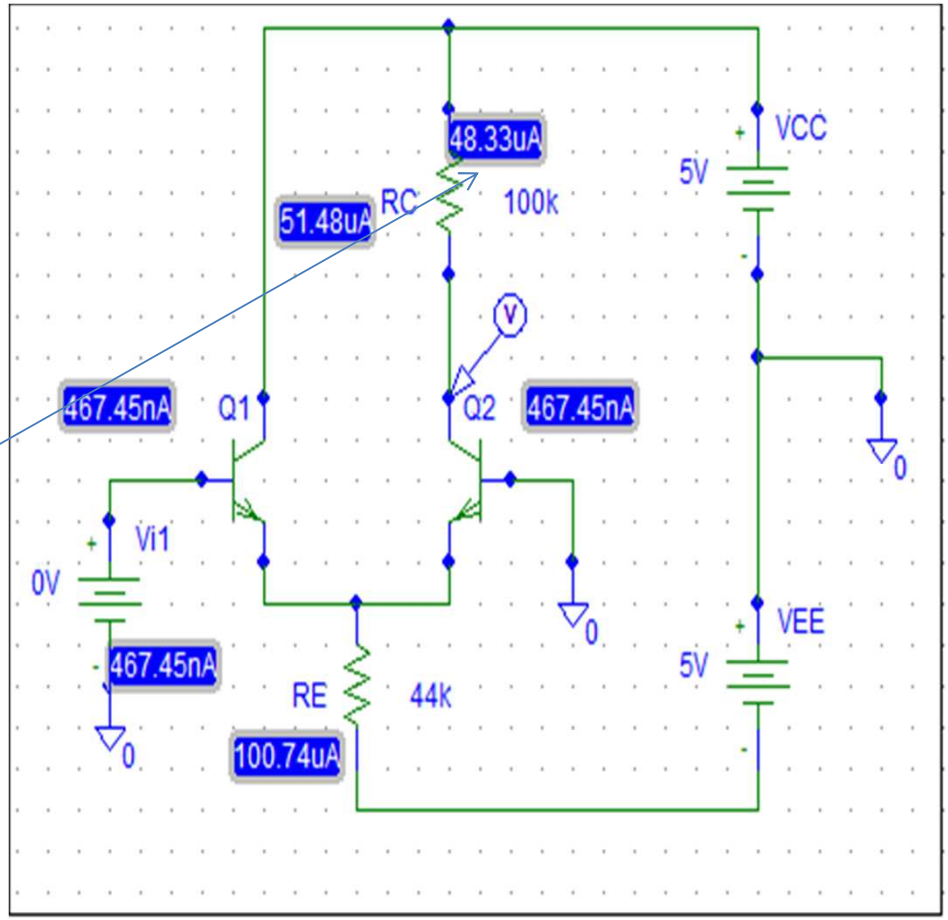
Bias current is 0.1 mA

Collector currents of Q1,2 a bit different

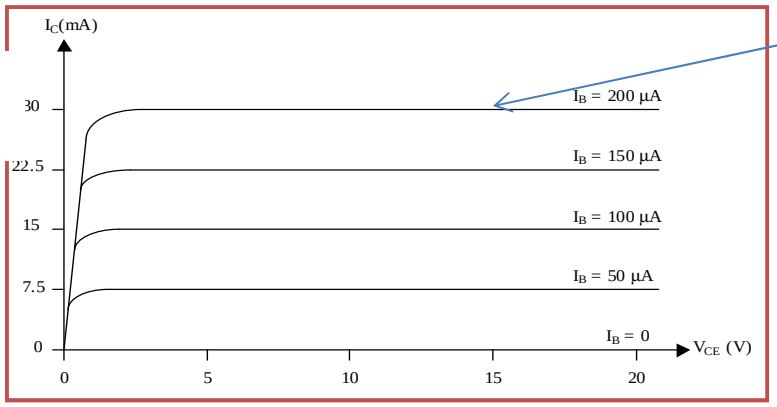
$I_{C1} > I_{C2}$

- Early Effect! (see Part 1)

I_{C2} = 48 µA (not 50 µA)

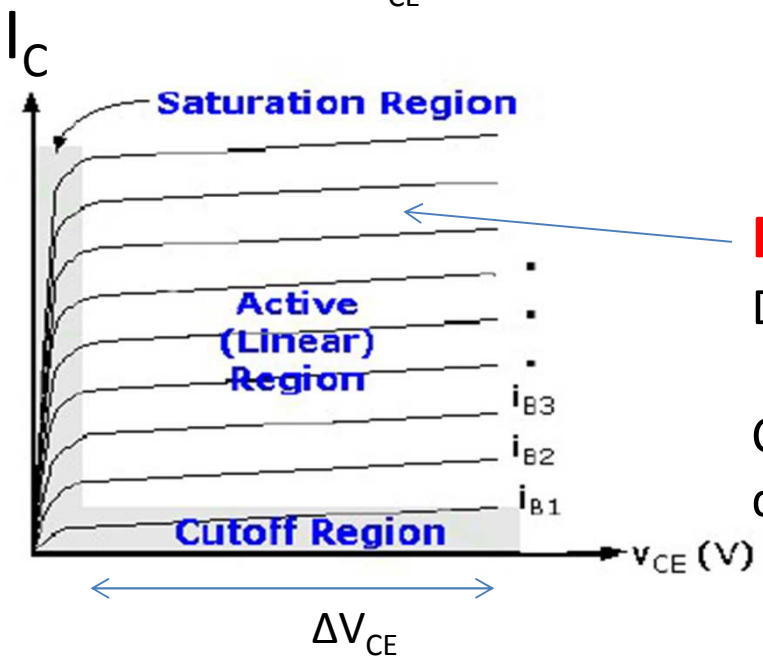


Output characteristics



IDEAL - FLAT

Collector current is independent of V_{CE}



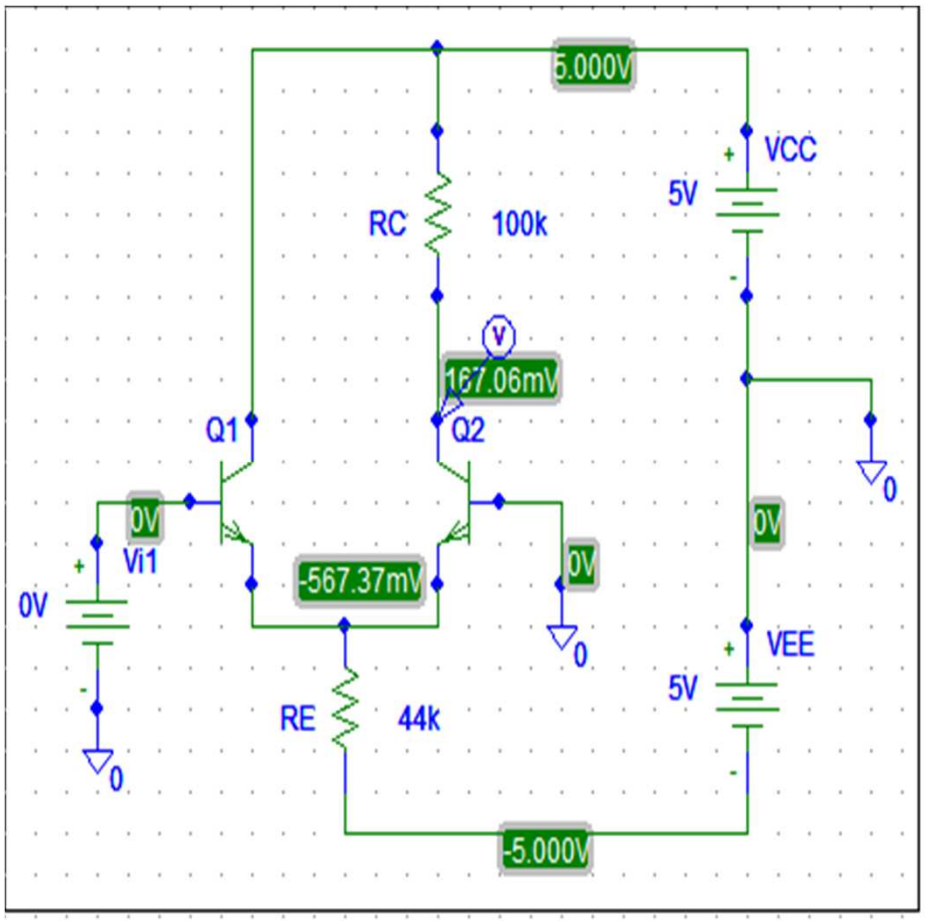
REAL – NOT FLAT

Due to the Early Effect

Collector current is weakly dependent on V_{CE}

I_C *increases* with increasing V_{CE}

DC Voltage levels



Output voltage ~ 170 mV (not 0 V)

V_{BE} (Q1, 2) = 0.567 V ~ 0.6 V

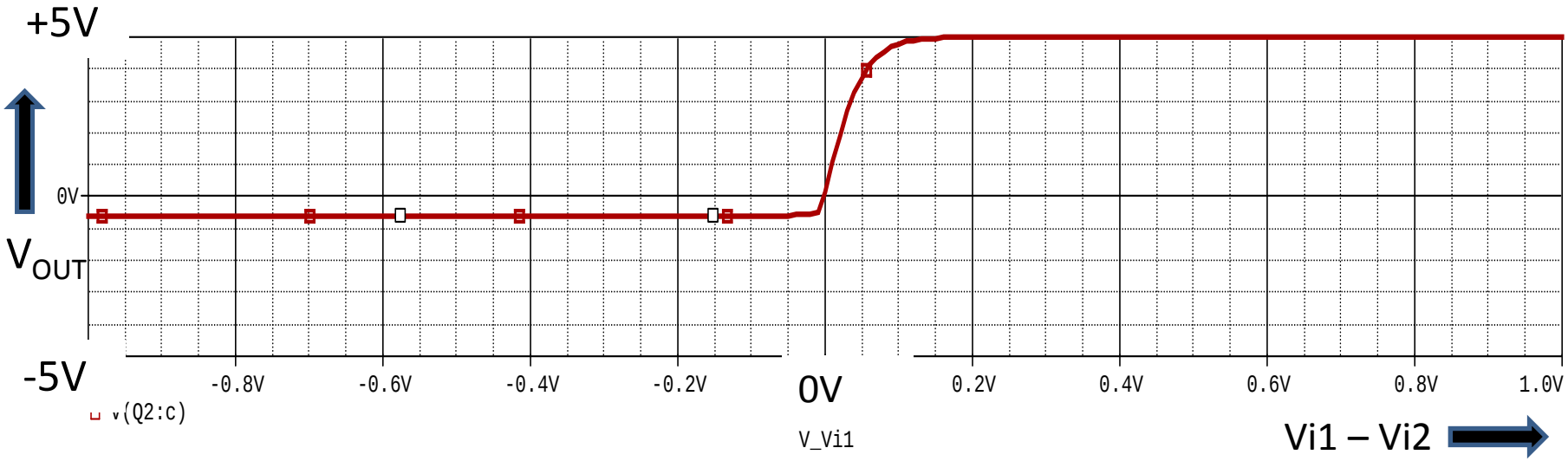
V_{CE} (Q1) = 5 – (– 0.6) = 5.6 V

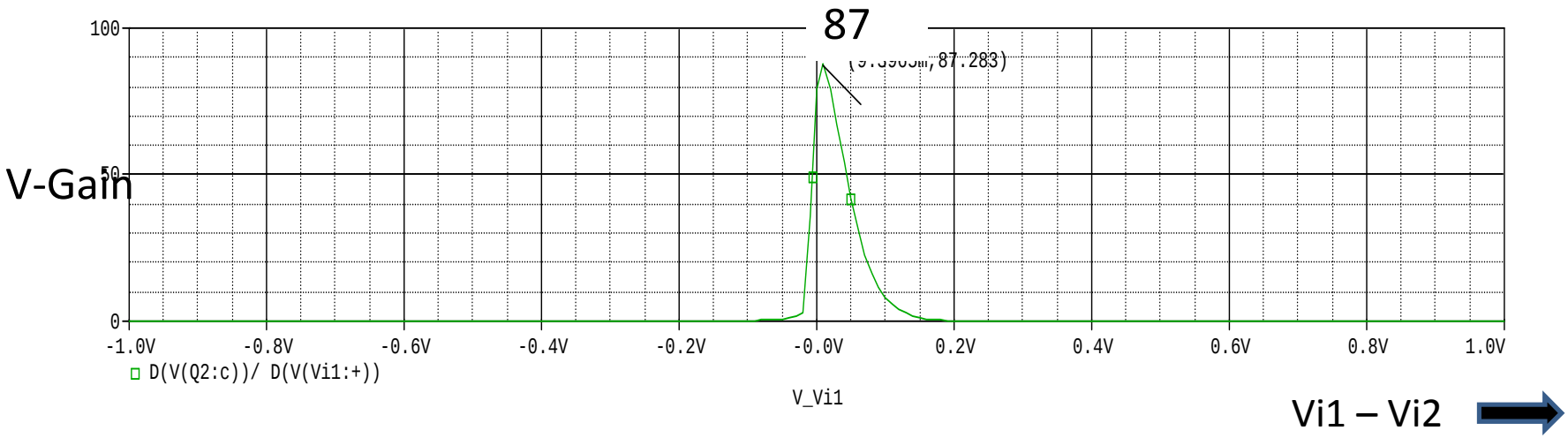
V_{CE} (Q2) = 0.17 – (– 0.6) = 0.77 V

V_{CE} (Q1) >> V_{CE} (Q2)

ideal transistors were assumed.
Flat output characteristic
Assume equal collector currents
Early Effect is modelled in SPICE

Transfer characteristic: Apply a voltage sweep to V_{i1}





Check

- Gain is 87 but we predicted 100
- Reason for poor agreement?

- We estimated I_C = 50 µA but Early Effect results in 48 µA
- Re-calculate g_m = 40 × 48 µA = 1.92 mA/V (not 2 mA/V!
- Re-calculate Diff. Gain = $g_m \times R_C /2$ = 1.92 × 50 = **96**

Simple theory predicts gain to circa 4%

Conclusions

We require

- **a better bias circuit to replace R_E, which will allow us to set the current I_o, independently of the resistance in the 'tail'.**
- **We would also like such a bias circuit to exhibit a very large dynamic resistance to give high common mode rejection ratio (CMRR).**
- **a circuit to replace the collector resistors, which will present a high resistance (for high gain) without creating a large voltage drop which causes the transistors to saturate and upsets the symmetry of the voltage swing.**

MCQ

The main function of the differential amplifier can be best described as:

a) Provide more gain
b) Increase input resistance
c) Reject unwanted interference signals
d) Make life more complicated for us

MCQ

The main function of the differential amplifier can be best described as:

a) Provide more gain
b) Increase input resistance
c) Reject unwanted interference signals
d) Make life more complicated for us

End of Part 3

- Next time
  - Look at better ways of biasing the diff.amp to give high CMRR
  - Decouple ac and dc design aspects