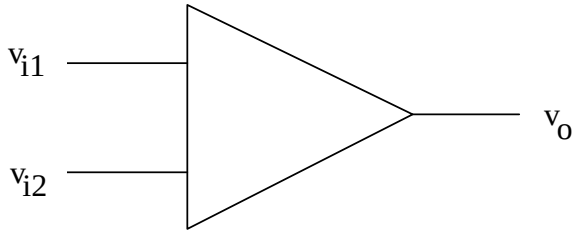
The Differential Amplifier

- amplifies the difference between two signals.

Ideally:-

$$v_o = A_d\left(v_{i1} - v_{i2}\right)$$

Note that signals that are common mode (CM), that is same phase, will not affect v_o.



Reality:-

Amplifer **will** amplify CM signals. We define:

Differential mode $v_{id} \equiv \left(v_{i1} - v_{i2}\right)$ (1)

Common mode $v_{ic} \equiv \frac{1}{2}\left(v_{i1} + v_{i2}\right)$ (2)

Why the factor ½?

Consider:- v_{i1} = + 50 μV compared to v_{i1} = 1050 μV
v_{i2} = - 50 μV v_{i2} = 950 μV

Corresponding DM and CM inputs are

v_{id} = + 100 μV and v_{id} = + 100 μV
v_{ic} = 0 V v_{ic} = 1000 μV

without the factor ½, the common mode for the second case would be considered incorrectly as 2000 μV: the average value of CM input must be used.

What is this 'common mode' signal? It is unwanted noise and interference that will be picked up on the two input pins of the amplifer - usually same in phase and magnitude.

Common mode rejection ratio, CMRR
This is a figure of merit for the amplifier which tells us how good it is at rejecting the unwanted signal (CM) relative to the one we want to amplify (DM).

First express output as a linear combination of the two inputs:

$$v_o = A_1 v_{i1} + A_2 v_{i2} \qquad (3)$$

Voltage amplification factor of input 1 with input 2 grounded

Voltage amplification factor of input 2 with input 1 grounded

Then, from Eqn.s 1,2: $v_{i1} = \frac{1}{2} v_{id} + v_{ic}$ $v_{i2} = -\frac{1}{2} v_{id} + v_{ic}$

Substitute in Eqn.3 to get

$$v_o = A_d v_{id} + A_c v_{ic} \qquad (4)$$

where $A_d \equiv \frac{1}{2}(A_1 - A_2)$ $A_c \equiv (A_1 + A_2)$

Want $A_d >> 1$, $A_c \to 0$ for a good diff. amp. Define:

$CMRR = \rho = \left|\frac{A_d}{A_c}\right|$ so Eqn.4 becomes $v_o = A_d v_{id}\left(1 + \frac{1}{\rho}\frac{v_{ic}}{v_{id}}\right)$

want ρ large. Examples of commercial op-amps:

741 ρ = 70 – 90 dB (3,000 to 30,000)
OP07 ρ = 94 – 106 dB (50,000 to 200,000)

The differential amplifier actually has two outputs as well as two inputs

Convention is therefore

Inputs $v_{i1} = \frac{v_{id}}{2} + v_{ic}$

$v_{i2} = -\frac{v_{id}}{2} + v_{ic}$

Outputs $v_{o1} = \frac{v_{od}}{2} + v_{oc}$ $(= A_d \frac{v_{id}}{2} + A_c v_{ic})$

$v_{o2} = -\frac{v_{od}}{2} + v_{oc}$ $(= -A_d \frac{v_{id}}{2} + A_c v_{ic})$

Diff. mode gain: $A_d = \frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} = \frac{v_{od}}{v_{id}}$	Common mode gain: $A_c = \frac{v_{o1} + v_{o2}}{v_{i1} + v_{i2}} = \frac{v_{oc}}{v_{ic}}$

$CMRR = \rho = \left|\frac{A_d}{A_c}\right|$

We now consider a real circuit.

Differential amplifier (a.k.a. long tail pair, or emitter coupled pair)

A schematic diagram is shown below.

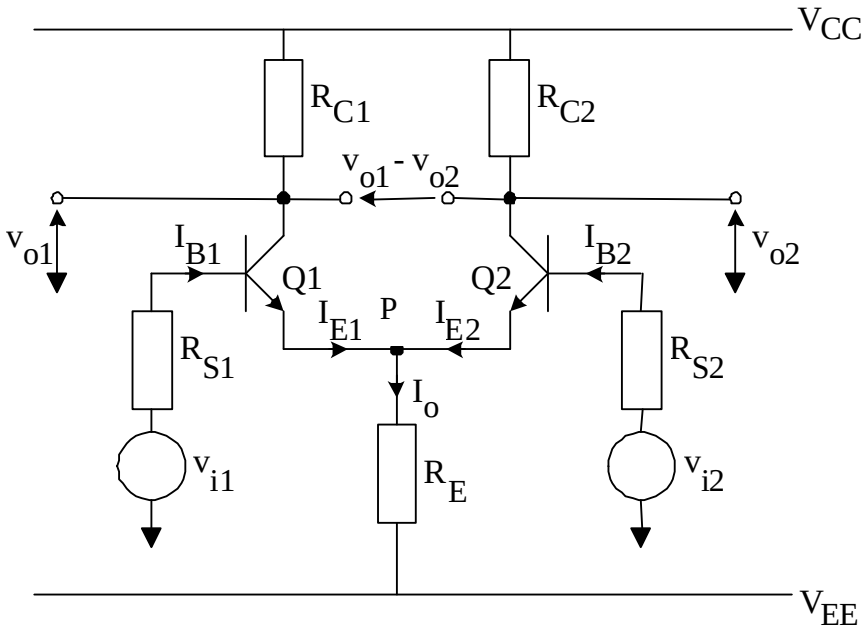


Figure 1

Question: Why are split supply rails used?

D.C. conditions: explanation of required conditions

Consider the operation of the circuit under d.c. conditions (with the a.c. voltage input signals $v_{i1} = v_{i2} = 0$). The negative supply rail effectively biases the transistors on - emitter resistor sets the current. Assume that the transistors do not saturate (in fact, R_{C1} and R_{C2} are chosen to ensure that this is true) the small base current flowing will cause little voltage drop so that the base of each transistor is close to 0 V. The point P will be at ~ -0.7 V due to the forward biased base-emitter diode drop and this voltage will not change significantly under normal conditions, thus the combination of R_E and V_{EE} constitute a simple current source

$$I_o = \frac{|V_{EE}| - 0.7}{R_E}$$ (note that V_{EE} is negative)

Under the assumption that the transistors are not saturated, the current will divide equally through R_{C1} and R_{C2}. Thus having selected a suitable current operating level, R_{C1} and R_{C2} must be chosen sufficiently small to ensure that the voltages at the nodes designated v_{o1}, v_{o2} do not fall below zero, that is to say, the transistors do not saturate.

D.C. Biasing: more rigorous analysis

Applying Kirchoff's law to the base circuit for $v_{in} = 0$:

$$I_{B1} R_{S1} + V_{BE1} + (I_{E1} + I_{E2}) R_E - V_{EE} = 0$$
and $$I_{B2} R_{S2} + V_{BE2} + (I_{E1} + I_{E2}) R_E - V_{EE} = 0$$

If the circuit is balanced i.e. $R_{S1} = R_{S2} = R_S$, $V_{BE1} = V_{BE2} = V_{BE}$ etc.

Adding and dividing by two gives

$$I_B R_S + V_{BE} + 2I_E R_E - V_{EE} = 0 \qquad (5)$$

Now $I_E = I_C + I_B = h_{FE} I_B + I_B = (h_{FE} + 1) I_B$

Sub. for I_B in Eqn. 5 and re-arrange: $$I_E = \frac{(V_{EE} - V_{BE})(h_{FE} + 1)}{2(h_{FE} + 1)R_E + R_S}$$

If $h_{FE} >> 1$ and $2(h_{FE} + 1) R_E >> R_S$ then

$$I_E \approx \frac{(V_{EE} - V_{BE})}{2R_E}$$

and I_o (current in R_E) $= 2 I_E \approx \frac{V_{EE} - V_{BE}}{R_E}$

Note that these equations show:

- I_E, and hence I_C, are independent of R_C
- I_o is not affected by unbalancing the base resistors.

If the circuit is unbalanced ($R_{S1} \neq R_{S2}$) but $V_{BE1} \approx V_{BE2}$ then

$$\frac{I_{B1}}{I_{B2}} \approx \frac{R_{S2}}{R_{S1}} \approx \frac{I_{C1}}{I_{C2}} \text{ as } I_C \propto I_B$$

A.C. Operation

Physical explanation: the important attribute of the differential input stage is the rejection of unwanted common-mode (in-phase) signals and the amplification of signals out of phase (differential signals). This can be understood with the aid of the equation:

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \qquad (1)$$

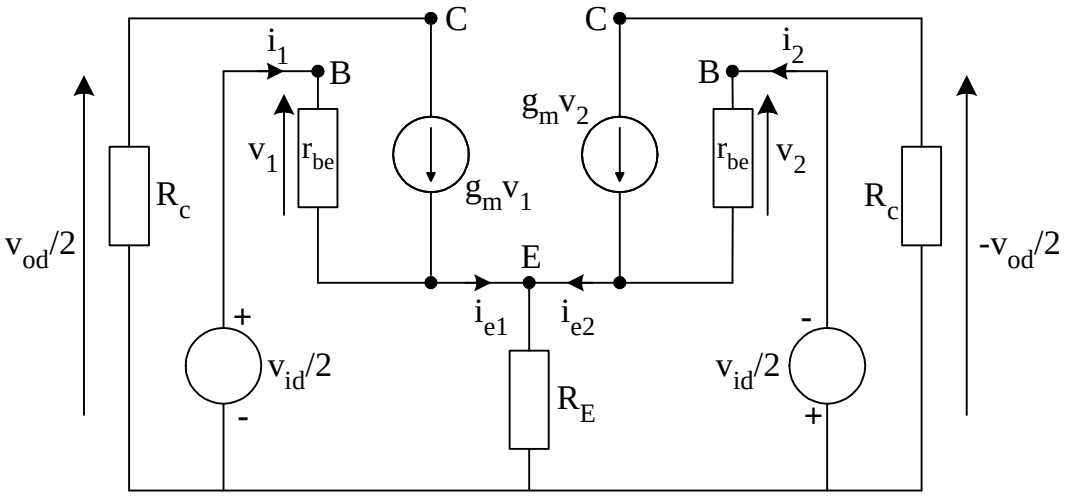
We consider first common mode sine-wave signals applied to each input. Over the first (positive going) half cycle of the input sine wave, the net voltage across the E-B junction of Q1 will be ($V_{BE1} + v_{i1}$), where the first term is the d.c. component and the second the a.c. component. According to Eqn.1, there will thus be an increase in collector current and a corresponding drop in collector voltage. By symmetry, the same events will occur for Q2 and so if the output is taken as ($v_{o1} - v_{o2}$), there will be no change, that is to say the common mode gain:

$$A_c = \frac{v_{o1} - v_{o2}}{v_{i1} + v_{i2}} \to 0$$

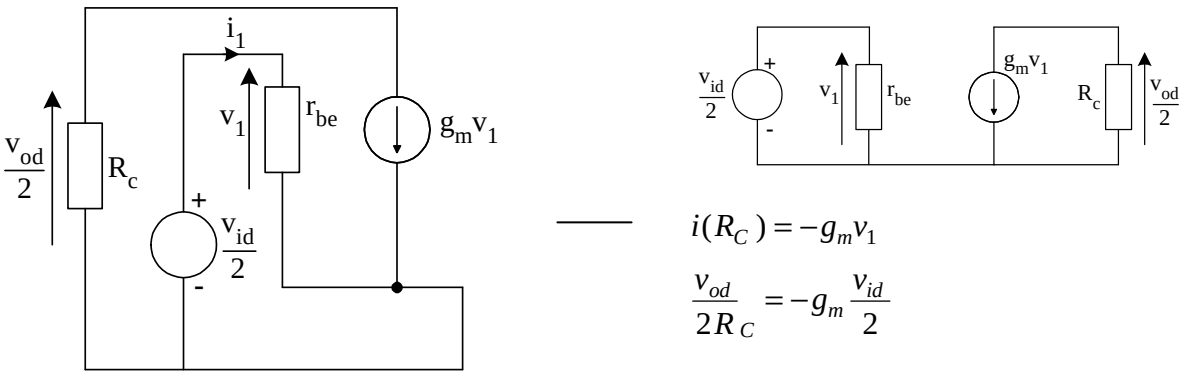
By similar arguments, for the differential signals, the collector voltage of one side will fall whilst the other rises and so voltage gain is realised for this case. The "common-mode" signal in reality represents noise/interference which will be picked up equally by both inputs. ***This configuration has the ability therefore to reject these unwanted signals.***

a.c. analysis: differential mode

Referring to the circuit diagram, with small a.c. signals, v_{i1} , v_{i2}, applied, we construct the a.c. equivalent circuit of the amplifier:-



The diagram is not quite as complicated as it looks! Notice we have used our convention for input and output signals. The circuit is seen to be symmetrical (assuming ideally matched transistors) so we can simplify things considerably for *differential* signals because $i_{e1} = - i_{e2}$. This means that no a.c. current flows in R_E for *differential* signals and we simply get.



$$i(R_C) = -g_m v_1$$

$$\frac{v_{od}}{2R_C} = -g_m \frac{v_{id}}{2}$$

the voltage gain for *differential (difference) mode* (inputs 180^o) out of phase, is thus given simply as:

$$A_d = \frac{v_{od}}{v_{id}} = -g_m R_C = 40\left(\frac{I_o}{2}\right)R_C \qquad (2)$$

where we have assumed $R_{C1} = R_{C2} = R_C$ (see exercise 1.b at the end of the handout for another case).

Thus a higher bias current leads to a higher voltage gain.

Taking the output **single ended** gives:

$$A_{d1} = \frac{v_{o1}}{v_{i1} - v_{i2}} = -g_m \frac{R_{C1}}{2}$$

$$A_{d2} = \frac{v_{o2}}{v_{i1} - v_{i2}} = +g_m \frac{R_{C2}}{2}$$

Note for single ended output, the gains are exactly half the voltage gain of double ended output or simple common emitter amplifier (why?).

Thus the voltage gain can be increased by increasing the value of collector resistor.

However, there is considerable constraint because of the need to avoid saturation in the transistors. This will lead us to use an active load (see later lecture).

The 'differential' input resistance of the D-M configuration is given approximately by:

$$R_{id} = \frac{v_{id}}{i_i} = \frac{2v_1}{i_i} = 2r_{be}$$

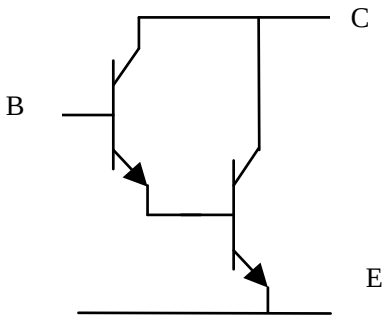
$$R_{id} = 2r_{be} = 2\frac{\beta_o}{g_m} = 2\frac{\beta_o}{40I_C} = \frac{\beta_o}{10I_o}$$

thus the operating current must be chosen small to increase the input resistance.

⇒ **We have an engineering trade-off as I_o must be large for high voltage gain (Eqn.2) and small for large input resistance.**

Alternatively, R_{id} can be increased by the following methods

1. Use Darlington transistors on the input



Effectively: $\beta_o \rightarrow \beta_o^2$

$r_{be} \rightarrow \beta_o^2/g_m$

Large increase in input resistance

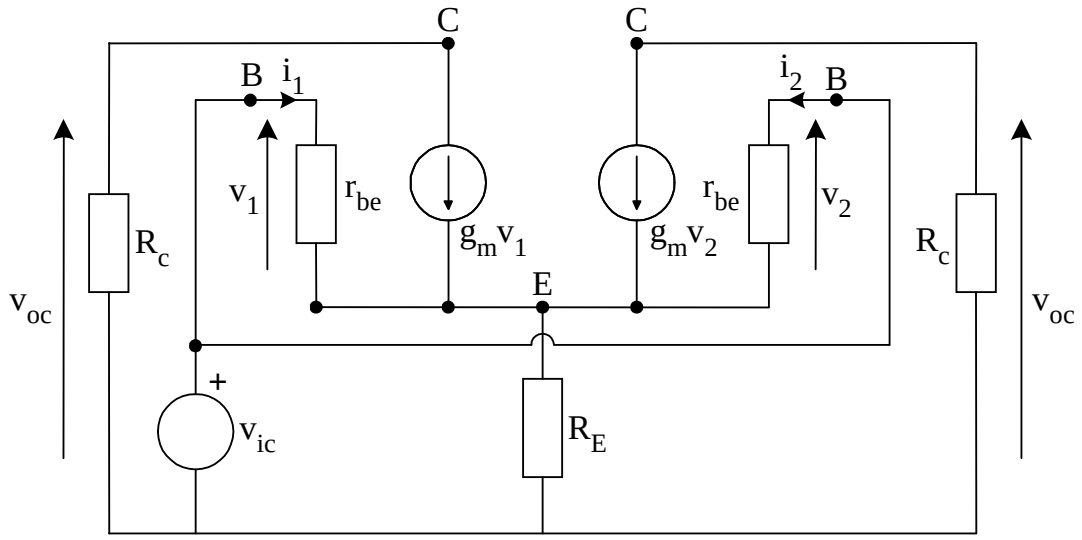
2. Use super gain transistors
   Very narrow base transistors – enhances collector current
   typically $\beta_o \sim 5{,}000$
   For $I_C = 1\mu A$, $r_{be} = \beta_o/g_m = 5{,}000/40 \times 1\mu A = 125\ M\Omega$

3. Use FET input transistors

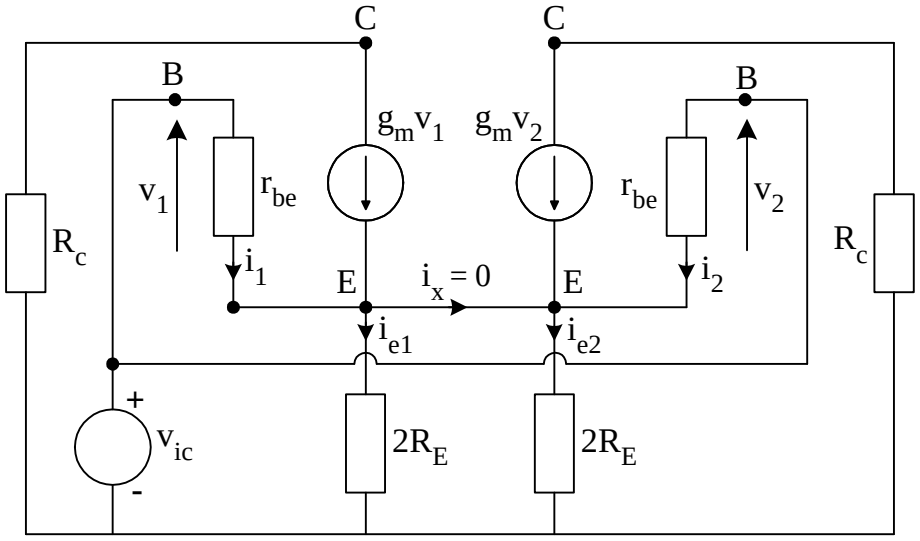
   JFET MOSFET
   $R_{id} \sim 10^8\ \Omega$ $R_{id} \sim 10^{10} - 10^{15}\ \Omega$

Common mode a.c. analysis

The equivalent circuit for *common* mode signals is:-

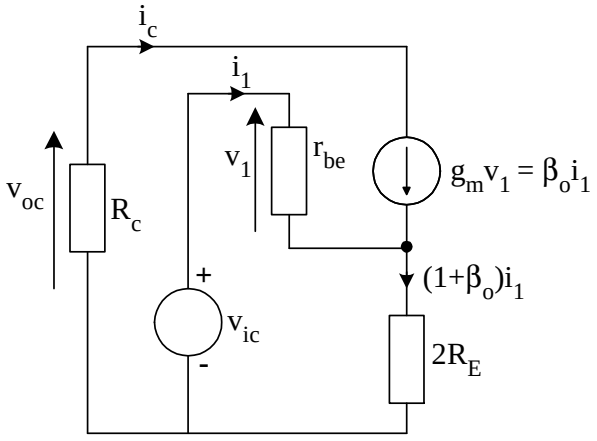


This can be transformed into



By symmetry $i_x = 0$

∴ Consider half-circuit



We recognise this as the CE-ED configuration (see Part 1). Common mode signals therefore "see" the emitter resistor which thus severely degrades the common-mode gain. Following the earlier analysis for CE-ED:

$$A_{Vc} = -\frac{R_C g_m}{1 + 2\left(g_m + r_{be}^{-1}\right)R_E} = -\frac{R_C \beta_o}{r_{be} + 2(\beta_o + 1)R_E}$$

⇒ Thus R_E must be large to make A_{Vc} small. However, R_E is also responsible for setting the d-c-. bias condition ?!?

[Note that the common mode input resistance can be shown to be $R_{ic} = \frac{v_{ic}}{i_i} = r_{be} + 2(1+\beta_o)R_E$] - a large value because β_o is large.

Conclude:

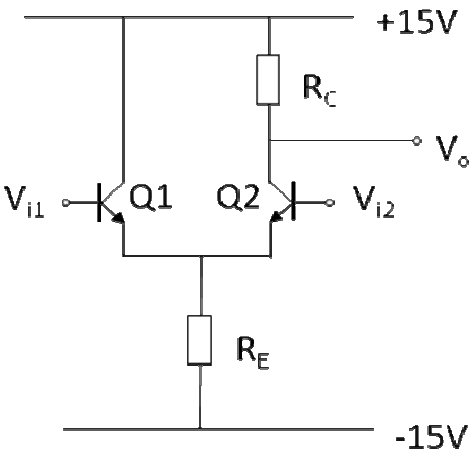
We require

1. **a bias circuit to replace R_E, which will allow us to set the current I_o, independently of the resistance in the 'tail'. We would also like such a bias circuit to exhibit a very large dynamic resistance to give high common mode rejection ratio (CMRR)**

2. **a circuit to replace the collector resistors, which will present a high resistance (for high gain) without creating a large voltage drop which causes the transistors to saturate and upsets the symmetry of the voltage swing.**

Worked Example

Work out values for R_E and R_C to give a bias current of 0.1mA with V_o = 0V (DC), β_o = 100.



Voltage drop across R_E ?

$$R_E \sim \frac{|V_{EE}| - |-0.7|}{0.1m} = \frac{14.3}{0.1} k\Omega$$ **143kΩ**

Voltage drop across R_C ?

$$R_C = \frac{|V_{CC}| - 0}{50\mu} = \frac{15}{50} M\Omega$$ **300kΩ**

Now work out the differential input resistance and voltage gain (β_o = 100)

$R_{id} = 2 \times r_{be} = 2\beta_o / g_m$ $g_m = 40 \times 50\mu A = 2mA/V^2$ $R_{id} = 200/2$ k = **100kΩ**

$A_{vd} = g_m \times$ ac load/2 $A_{vd} = g_m \times R_C / 2$ $A_{vd} = 2m \times 300k/2 = 300$

Now work out the common-mode voltage gain: $A_{Vc} = \frac{R_C \beta_o}{r_{be} + 2 \times \beta_o \times R_E}$

$$A_{Vc} = \frac{300k \times 100}{\frac{100}{2m} + 2 \times 100 \times 143k} \sim \mathbf{1}$$

CMRR??

Exercises

1. a) Show that the input resistance of the amplifier in figure 3a is given by:-

$R_i = r_{be} + (1 + \beta_o) R_E//r_i$

and that the voltage gain is:-

$$\frac{v_o}{v_i} = \frac{(1+\beta_o)R_E//r_i}{r_{be}+(1+\beta_o)R_E//r_i} \approx \frac{g_m R_E//r_i}{1+g_m R_E//r_i}$$

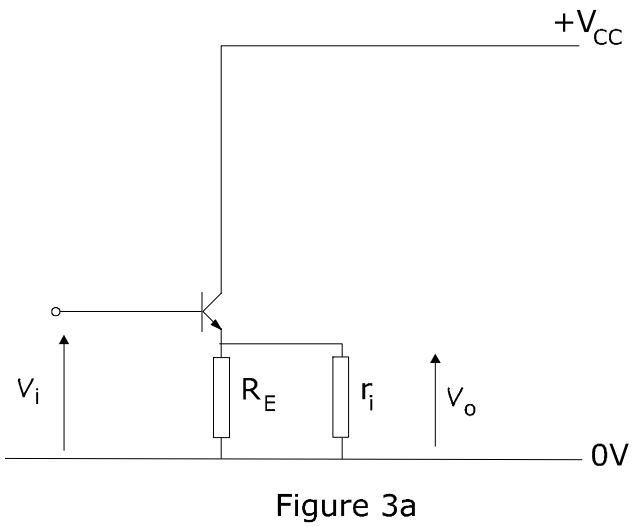


Figure 3a

b) Considering the amplifier in figure 3b as a two stage dc coupled amplifier show that the input resistance is

$R_i = r_{be} + (1 + \beta_o) R_E//r_e$

and that the voltage gain

$$\frac{v_o}{v_s} = \frac{g_m(R_E//r_e)}{1+g_m(R_E//r_e)} g_m R_c$$

Show that these reduce to:-

$R_i \approx 2r_{be}$ and $v_o/v_s \approx g_m R_c/2$

and state the necessary approximations.

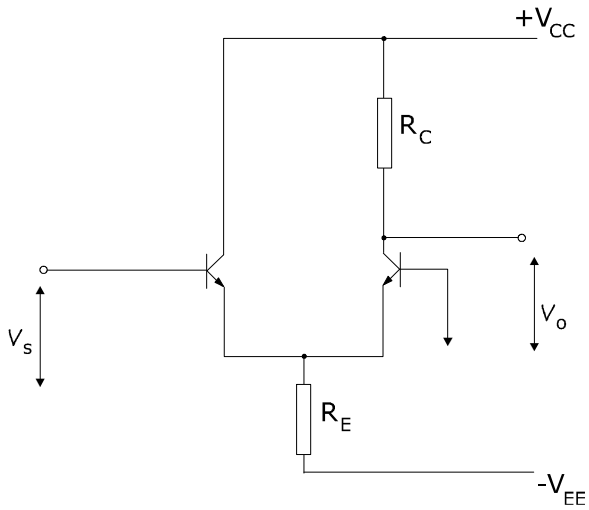


Figure 3b