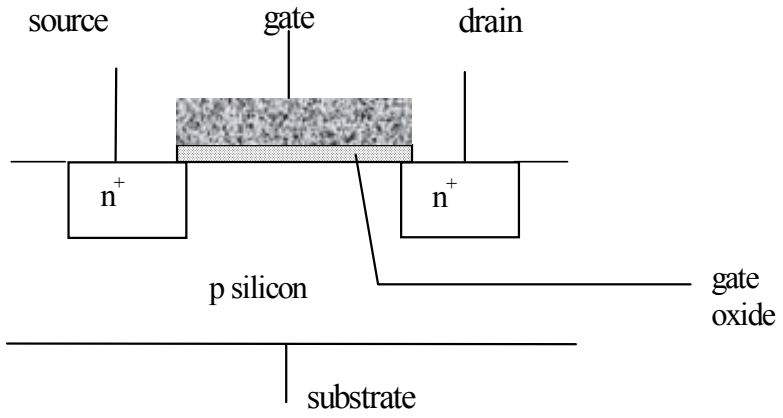
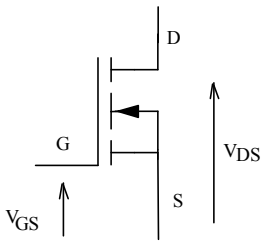
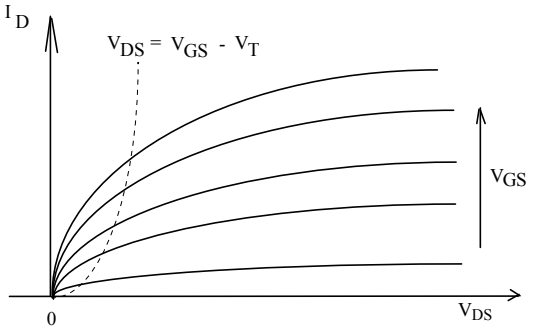
Field Effect transistors: MOSTs (or MOSFETs) and JFETs

The discussion will be presented for the very important MOST device although the a.c. model is equally valid for the JFET device.

D.C. model (see lectures on ELEC212: CMOS Integrated Circuits also)
The figures show the enhancement MOST device structure, circuit schematic and the output characteristic: I_D versus V_{DS} for gate voltage steps, V_{GS}. In amplifiers, the device is usually biased to the right of the locus '$V_{DS} = V_{GS} - V_T$'.







In this operating regime, the current obeys the 'MOST equation':

$$I_D = \frac{\beta}{2}\left[V_{GS} - V_T\right]^2\left(1 + \lambda V_{DS}\right)$$ (see ELEC212 for a derivation)

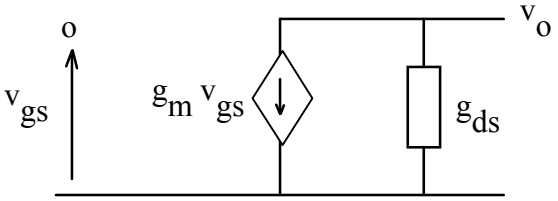
which includes a term $(1 + \lambda V_{DS})$ to account for the slope on the output characteristic (that is, the output resistance, r_{ds}):
λ is typically of the order 0.05 V^{-1} although the channel length of the MOST can be made very long to give a smaller value.
The 'drive constant' β is of the order 1 mA/V^2.

Note that: $$\beta = \left(\mu C_o\right)\frac{W}{L} \quad \text{or} \quad \beta = KN\frac{W}{L}$$

KN (some books use Kp) is the product of mobility (μ) and gate oxide capacitance C_o) per unit area; W and L are the physical width and length of the gate.

A.C considerations

The simple, low frequency equivalent circuit for the MOS transistor is:



(Note $g_{ds} = 1/r_{ds}$) Assuming that the MOST is saturated (on the 'flattish' part of its characteristic: not as flat as the bipolar transistor!) , we use the MOST equation

$$I_D = \frac{\beta}{2}\left[V_{GS} - V_T\right]^2\left(1 + \lambda V_{DS}\right)$$

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{VDS=const.} = \beta\left(V_{GS} - V_T\right)(1 + \lambda V_{DS}) = \sqrt{2I_D\beta(1 + \lambda V_{DS})} \approx \sqrt{2I_D\beta}$$

The output conductance ($g_d = 1/r_d$) is a particularly important parameter for MOSTs as the output characteristic is not flat (as it is in BJT's). It can be found as:

$$g_{ds} = \left.\frac{\Delta I_D}{\Delta V_{DS}}\right|_{VGS=const.} = \frac{\beta}{2}\left[V_{GS} - V_T\right]^2\lambda = I_D\frac{\lambda}{1 + \lambda V_{DS}} \approx I_D\lambda \qquad (\text{for } \lambda V_{DS} << 1)$$

$$r_{ds} = \frac{1}{g_{ds}} = \frac{1}{I_D\lambda} \qquad \text{(sometimes written as } r_d, g_d)$$

SPICE and y-parameter models

For the SPICE model, we consider $\beta = KN\frac{W}{L}$ where W, L are gate width and length.

KN, W, L are SPICE parameters and should be quoted by the manufacturer.

λ = LAMBDA is also a SPICE parameter.

Older data sheets often quote so-called y-parameters, y_{fs}, y_{os}, where: $y_{fs} \equiv g_m$ and $y_{os} \equiv g_d$.

Comparison of BJT and MOST

Comparing the BJT and the MOST at a bias current level of, **I = 1 mA:**

Taking for the MOST: $\lambda = 0.05\ V^{-1}$, $\beta = 1\ mA/V^2$.
And for the BJT : $V_A = 150$ V,

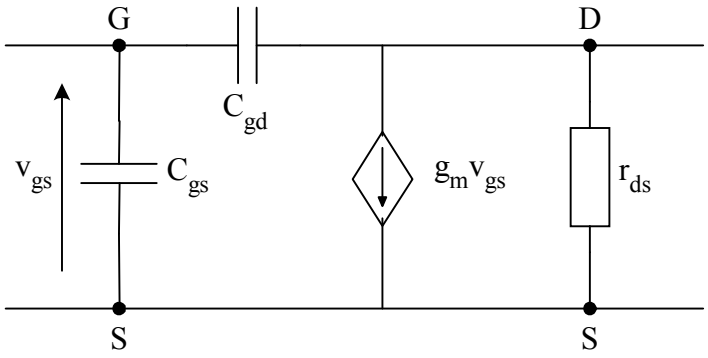
And recalling: $r_{ds} = 1/I\lambda$, $r_{ce} = V_A/I$
$g_{m(MOST)} = \sqrt{2I\beta}$, $g_{m\,(BJT)} = 40\ I_C$

$r_{ce}/r_{ds} = V_A\lambda = 8$; $\qquad \frac{g_{m(BJT)}}{g_{m(MOST)}} = 40\sqrt{\frac{I}{2\beta}} \approx 30$

Hence the BJT can be thought of as is a superior device for use in linear circuits, at least in electrical terms. The great advantage of the MOSFET is the ability to make very simple switching circuits from it: a CMOS inverter comprises only two transistors: a p-channel and an n-channel. Bipolar transistor switching circuits are based on a circuit similar to the differential amplifier configuration (ECL – emitter coupled logic) and are more complex hence take up more area on the Si chip.

FET at high frequency

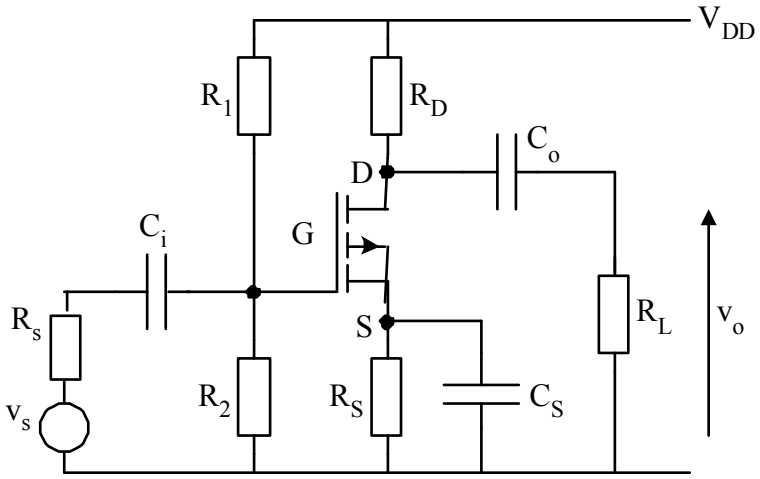
The high frequency equivalent circuit is shown below.



C_{gs} is the capacitance between the gate and source region
C_{gd} is the capacitance between the gate and drain region

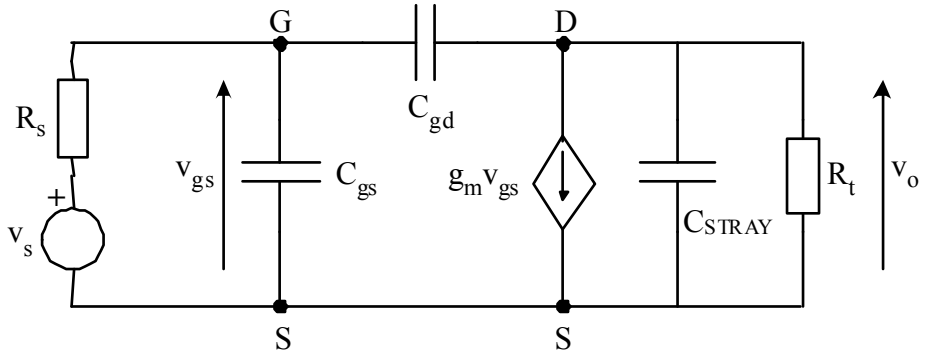
Typically the order pF's in discrete MOSTs (small); 10-100's fF in I.C.'s. Discrete MOSFETs are therefore useful as very fast switches and high frequency amplifiers.

The schematic diagram of a common source amplifier is shown below.



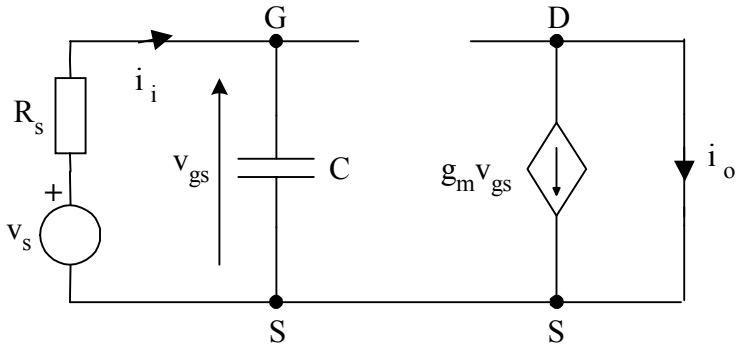
The corresponding a.c. equivalent circuit is shown overleaf :
(Note that C_{STRAY} takes into account stray capacitance between the output of the amplifier and the circuit board on which it is situated.)

(*For details on biasing the amplifier, see text books*)



Gain-bandwidth product

Following the approach adopted for the bipolar transistor, re-draw the circuit as :



Note we have ignored the current delivered to the output via the feed-through capacitor C_{gd}

(we have assumed current $i_{Cgd} << g_m v_{gs}$)

Then: $C = C_{gs} + C_{gd}$

$i_o = -g_m v_{gs}$ $\quad v_{gs} = \dfrac{i_i}{j\omega C}$ (Ohm's Law)

$\dfrac{i_o}{i_i} = -\dfrac{g_m}{j\omega C}$ and taking the modulus, $\left|\dfrac{i_o}{i_i}\right| = \dfrac{g_m}{2\pi f\left(C_{gs} + C_{gd}\right)}$

So $f_T = \dfrac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)}$ ($f = f_T$ when current gain = 1)

Justify approximation

Ratio of current through C_{gd} to $g_m v_{gs}$ = $\dfrac{v_{gs} 2\pi f_T C_{gd}}{g_m v_{gs}} = \dfrac{2\pi f_T C_{gd}}{2\pi\left(C_{gs} + C_{gd}\right) f_T} = \dfrac{C_{gd}}{\left(C_{gs} + C_{gd}\right)}$

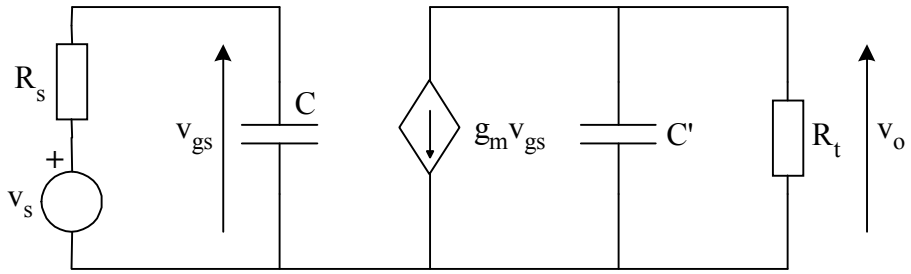
In saturation, $C_{gs} = CGSO + \dfrac{2}{3} C_{ox} WL$, $C_{gd} = CGDO$ Now CGSO ~ CGDO

(See notes for CMOS)

So ratio is $\dfrac{CGDO}{CGSO + \dfrac{2}{3} C_{OX} WL} = \dfrac{1}{1 + \dfrac{2}{3}\dfrac{C_{OX}}{CGDO} WL} << 1$

Voltage gain bandwidth

Apply the Miller theorem and again, see that the equivalent circuit comprises of two first order networks.



$C = \left[C_{gs} + (1-K)C_{gd}\right]$ C' = $C_{gd}(K-1)/K + C_{stray} \approx C_{gd} + C_{STRAY}$

The input and output circuits have characteristic time constants:

$$\tau_i = R_S\left[C_{gs} + (1-K)C_{gd}\right] \qquad \tau_o = R_t\left(C_{gd} + C_{STRAY}\right)$$

Note also that $R_t = R_D // R_L // r_{ds}$

It is generally the case that the input time constant is much greater than the output time constant i.e., $\tau_i >> \tau_o$ and we can therefore disregard the capacitor C' in the circuit.
Note than in any problem, it is important to justify the use of this approximation.

Using this approximation, it is the *input time constant* that sets the response of the amplifier:
thus

$$v_o = -g_m v_{gs} R_t \quad \text{and} \quad K = \frac{v_o}{v_{gs}} = -g_m R_t$$
$$C = C_{gs} + (1 + g_m R_t)C_{gd}$$

Voltage gain: $A_{Vs} = \frac{v_o}{v_s} = \frac{v_o}{v_{gs}}\frac{v_{gs}}{v_s}$

so

$$A_{Vs} = -g_m R_t \frac{1/j\omega C}{R_S + 1/j\omega C} = -g_m R_t \frac{1}{1 + j\omega R_S C}$$

$$A_{Vs} = -g_m R_t \frac{1}{1 + j\left(\frac{f}{f_H}\right)} \qquad \text{where } f_H = \frac{1}{2\pi R_S C} \text{ is the voltage gain bandwidth.}$$

Notes

1. The low frequency gain is $-g_m R_t$: a similar expression to the BJT but remember that g_m is given by a different expression for the MOST:

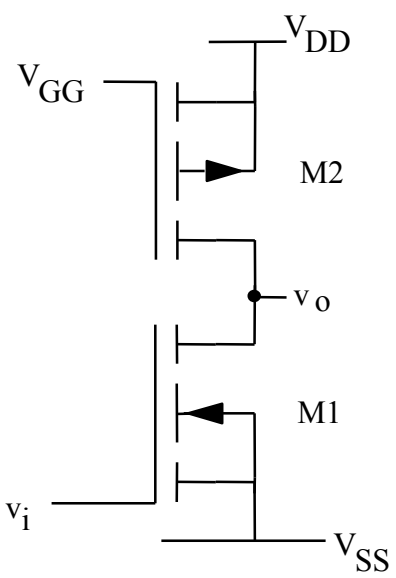
BJT: $g_m = 40 I_C$ MOST: $g_m = \sqrt{2 I_D \beta}$

$$A_{Vs} = -g_m R_t \frac{1}{1 + j\left(\frac{f}{f_H}\right)}$$

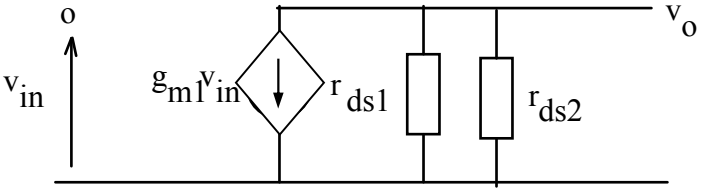
Notice that, unlike the case of the bipolar transistor, there is no 'coupling term'. Thus the high source resistance does not 'load' the front end of the amplifier (although take care with the bias resistors – a depletion mode device is best).

2. The source resistance does affect the bandwidth however.

3. The low frequency gain is likely to be low because of the small g_m. The gain can be increased by the use of **active loads** which will present an increased R_t. An active load can be constructed from another MOST as shown below. The active load presents a dynamic resistance of r_{ds} which can be large.



The equivalent circuit is shown below. Note that V_{DD}, V_{SS} and V_{GG} are all a.c. grounds.



Hence

$$v_o = -\frac{g_{m1} v_i}{g_{ds1} + g_{ds2}} \qquad \text{where } g_{ds} = 1/r_{ds}$$

$$A_V = \frac{v_o}{v_i} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}} \sim -\sqrt{\frac{2\beta_1}{I_D}}\left(\frac{1}{2\lambda}\right)$$

Using $\lambda = 0.01\ V^{-1}$, $\beta = 1\ mA/V^2$, $I_D = 0.1mA$ gives a gain of over 200.

This amplifier configuration is suitable for use as an **integrated circuit element** as the MOSTs occupy far less area than the resistors used in the earlier amplifier.

Phase
Similar analysis to that done earlier:

$$A_{Vs} = \frac{A_{Vso}}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}} e^{j(\pi - \phi)}$$

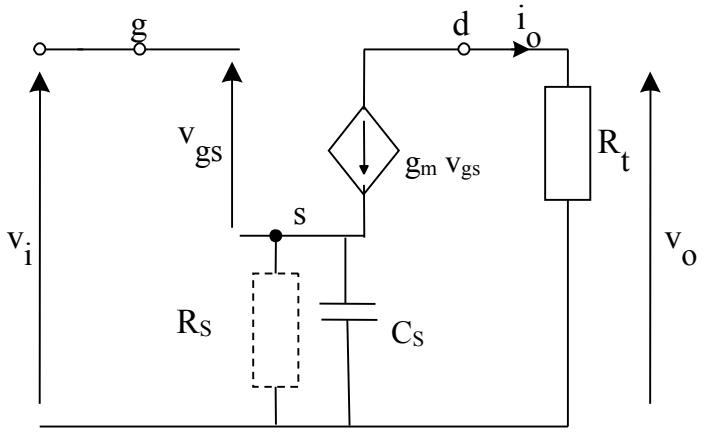
[Note: $e^{j(\pi-\phi)} = e^{j\pi} e^{-j\phi} = (-1)[\cos\phi - j\sin\phi]$]

where $\tan(\phi) = \frac{f}{f_H}$ and ϕ gives the phase angle between v_s and v_o; $A_{Vso} = g_m R_t$

Design Example

The low-frequncy roll-off, f_L is to be set by capacitor C_S. Estimate a value for C_S to give a low-frequency cut-off (-3 dB point) of 100 Hz if I_D = 0.1 mA, β = 1 mA/V^2 and R_t = 10 kΩ.

Cs: To keep it simple, assume that the impedance of C_S , Z_{CS} << R_S at the roll-off frequency. The equivalent circuit is shown opposite.



$$v_i = v_{gs} + g_m v_{gs} \times \frac{1}{j\omega C_S}$$

So

$$v_{gs} = \frac{v_i}{1 + \frac{g_m}{j\omega \times C_S}}$$

Now, $v_o = -g_m v_{gs} R_t$

Therefore the voltage gain is,

$$\frac{v_o}{v_i} = -\frac{g_m R_t}{1 + \frac{g_m}{j\omega \times C_S}} \longrightarrow \left|\frac{v_o}{v_i}\right| = \frac{g_m R_t}{\sqrt{1 + \left(\frac{g_m}{j\omega \times C_S}\right)^2}}$$

Now the gain falls by $1/\sqrt{2}$ when $g_m = \omega \times C_S$, so

$$C_S = \frac{g_m}{2 \times \pi \times f_L}$$

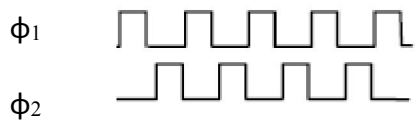
Now $g_m = \sqrt{2 \times I_D \times \beta}$, that is $g_m = \sqrt{2 \times 10^{-4} \times 10^{-3}}$ **= 0.45 mA/V**

Substitute the values: $C_S = \frac{0.45 \times 10^{-3}}{2 \times \pi \times 100}$ **= 0.7 µF.**

The switched-capacitor resistor (SCR)

The SCR comprises two MOSFETs used as switches, S1 and S2 and a capacitor, C.

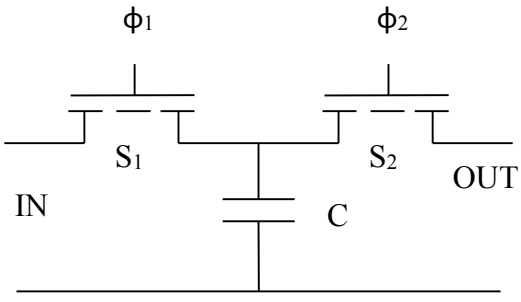
The non-overlapping clock waveforms, ϕ_1 ϕ_2, make the switches, S_1, S_2 turn on and off alternately with a given frequency, *f*.



Assume C is initially discharged:

when ϕ_1 goes high, S_1 turns on and C charges to V_1,

when ϕ_2 goes high (ϕ_1 goes low), S_2 turns on, and C discharge to V_2.



The amount of charge transferred during this process is

$Q = C (V_1 – V_2)$

and this occurs during one clock cycle, T_C.

The equivalent, average current is then:

$$I = \frac{Q}{T_C} = \frac{C(V_1 - V_2)}{T_C} \quad \text{that is,} \quad I = f_C C(V_1 - V_2) = \frac{V_1 - V_2}{R_{eq}}$$

Where $\mathbf{R_{eq} = 1/(f_C C)}$

As can be seen from the equation, a small capacitor with a low switch frequency provides large resistance. This means it can be easily fabricated on a chip, with a compact layout.

The equivalent resistance of a SC resistor is reliable because it has less process variation and loss-free propagation of switch frequency. Also it is tuneable by changing the switch frequency. This frequency related resistance is used in 'switched capacitor' circuits. SCRs can be used in operational amplifier circuits (replacing large value resistors), active and passive filters and for sample and hold in analogue to digital converters.

Worked Example

A transducer exhibits a very high internal resistance of R_S = 100 kΩ. A MOSFET is therefore to be used to amplifier its output. Work out values for the mid-frequency gain and the bandwidth of a common source amplifier given the following information:

For the MOSFET: C_{gs} = 4 pF, C_{gd} = 1 pF, β = 0.1 mA/V^2

Circuit (see page 3): R_S = 100kΩ, I_D = 1 mA (bias level), R_t = 22kΩ, C_S = 1pF (stray)

Solution

Mid frequency gain: $A_{Vs} = -g_m R_t$

Where $g_m = \sqrt{2I_D\beta} = \sqrt{2x\left(1.10^{-3}\right)x\left(0.1x10^{-3}\right)} = 0.45mA/V$

$\therefore A_{Vs} = -\left(0.45x10^{-3}\right)x\left(22x10^{3}\right) = -9.9$ (*note small gain*)

Input time constant $\tau_i = R_S\left[C_{gs} + (1-K)C_{gd}\right] = 1.5\mu s$

Output time constant $\tau_o = R_t\left(C_{gd} + C_{STRAY}\right) = 0.04\mu s$

Clearly input time const. >> output time const.

justifies use of $f_H = \dfrac{1}{2\pi R_S C}$ for voltage gain bandwidth.

Effective input capacitance:

$$C = C_{gs} + (1 + A_{Vs})C_{gd} = 15pF$$

Bandwidth = 106 kHz

Low because of high source resistance. If R_S was 50 Ω, get f_H = 200 MHz.

MOST analogue integrated circuits (I.C.s)

Building blocks similar to those we have studied for the BJT, can be constructed using MOSTs: that is, current sources, active loads, differential amplifiers etc. In general, resistors are not used widely in MOST I.C.s but rather a variety of forms of active load MOSTs are used as these are more compact and in general, offer higher dynamic resistance etc. Given the widespread use of CMOS digital circuit technology it is not surprising that analogue CMOS (MOST) should be of great interest despite the generally poorer performance of MOSTs compared to BJT's. In particular, 'mixed signal' (analogue and digital on the same 'chip' or in the same 'chip-set' is used widely in such areas as mobile communications ('phones). The design of such systems is difficult and software tools are far more primitive than those available for purely digital design. There are therefore good career prospects in the areas of analogue, digital and mixed signal design together with the software development of design 'tools'.

Exercises

1. Derive equations for the transconductance and output resistance of a MOSFET in the linear region of operation.

2. The figure shows a differential amplifier. Assuming that the amplifier feeds into a very large load resistance, show that the differential gain is given by $g_m \times r_{ds2} // r_{ds4}$ and the common mode is (ideally) zero. The technique is shown in part 5 – this derivation is much easier!