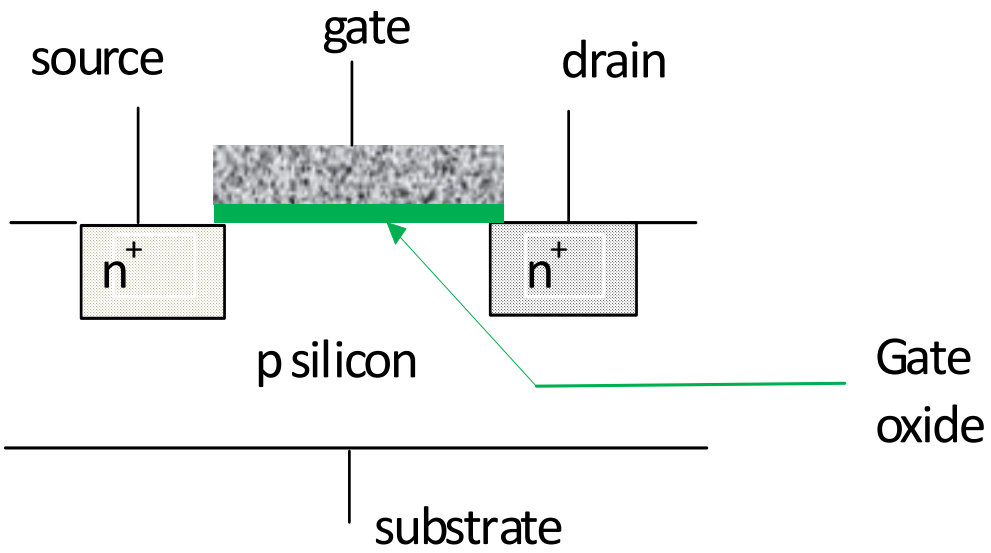
Electronic circuits and systems
ELEC271

Part 8
Field effect devices

Field Effect transistors: MOSTs (or MOSFETs) and JFETs

The MOSFET



Enhancement mode device

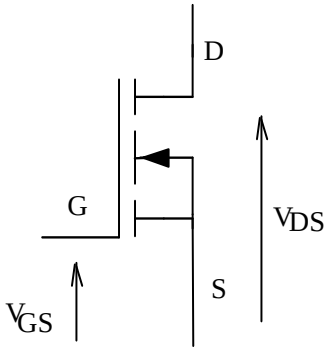
- The most widely used device in electronics.
- The major device in all common products: a p-channel and n-channel device together form the **CMOS inverter**
- **(see lectures of Dr. Mitrovic)**

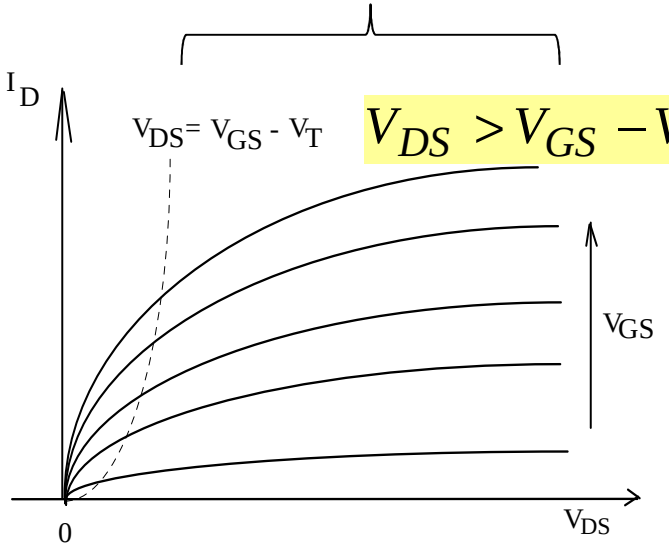
$$I_D = \frac{\beta}{2}[V_{GS} - V_T]^2(1 + \lambda V_{DS})$$

$$\beta = (\mu C_o)\frac{W}{L}$$

$$\beta = KN\frac{W}{L}$$

$$C_o = \frac{\varepsilon_o \varepsilon_s}{t_{ox}}$$



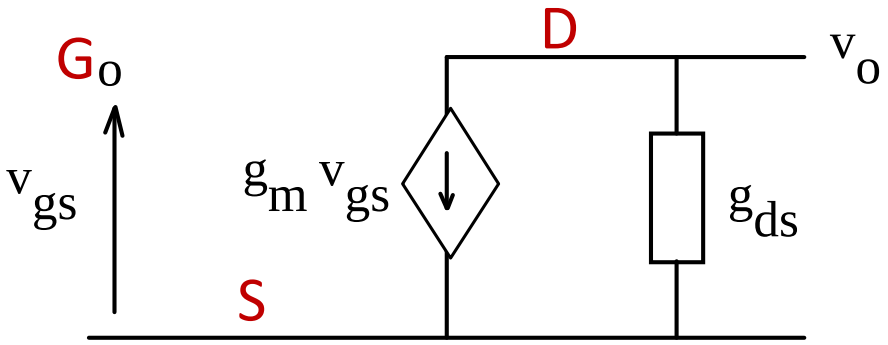


μ = mobility, C_o = gate oxide capacitance /unit area;
W and L are the physical width and length of the gate. **λ is the slope on the output characteristic**

Julius Edgar Lilienfeld (1882 – 1963)

- Lilienfeld moved to the United States in the early 1920s, originally in order to defend patents he possessed, and then made a scientific/industrial career there.
- Among other things, he invented an "FET-like" transistor and the electrolytic capacitor in the 1920s. He filed several patents describing the construction and operation of transistors as well as many features of modern transistors.
- (US patent #1,745,175 [1] for an **FET-like transistor was granted January 28, 1930**.) When Brattain, Bardeen, and Robert Gibney tried to get patents on their earliest devices, most of their claims were rejected due to the Lilienfeld patents.

A.C small-signal model



Assume the MOST is saturated (on the 'flattish' part of its characteristic: not as flat as the bipolar transistor!) ,
use the MOST equation

$$I_D = \frac{\beta}{2}[V_{GS} - V_T]^2(1+\lambda V_{DS})$$

transconductance

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{VDS=const} = \beta(V_{GS} - V_T)(1+\lambda V_{DS})$$

$$= \sqrt{2I_D\beta(1+\lambda V_{DS})}$$

$$\approx \sqrt{2I_D\beta}$$

$$g_m \sim= \sqrt{2I_D\beta}$$

Output conductance/resistance

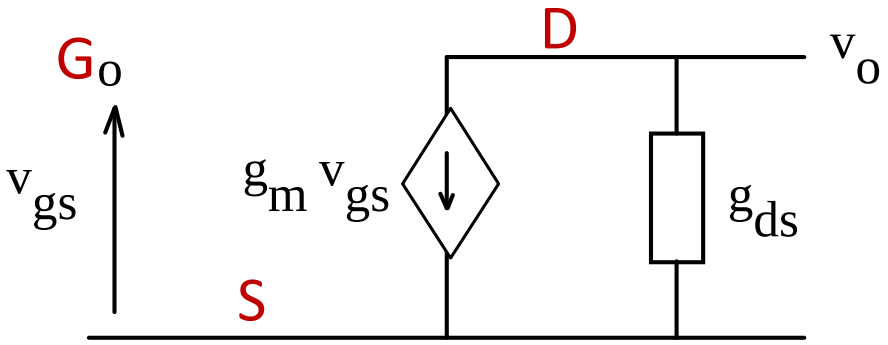
$$g_{ds} = \left.\frac{\Delta I_D}{\Delta V_{DS}}\right|_{VGS=const} = \frac{\beta}{2}[V_{GS} - V_T]^2\lambda$$

$$= I_D\frac{\lambda}{1+\lambda V_{DS}} \approx I_D\lambda \quad (\text{for } \lambda V_{DS} << 1)$$

$$r_{ds} = \frac{1}{g_{ds}} = \frac{1}{I_D\lambda}$$

$$g_{ds} \sim I_D\lambda$$

A.C small-signal model -2



Assume the MOST is saturated (on the 'flattish' part of its characteristic: not as flat as the bipolar transistor!) , **use the MOST equation**

$$I_D = \frac{\beta}{2}[V_{GS} - V_T]^2(1 + \lambda V_{DS})$$

transconductance

$$g_m \sim= \sqrt{2 I_D \beta}$$

Output conductance/resistance

$$g_{ds} \sim I_D \lambda \qquad r_{ds} = \frac{1}{g_{ds}} = \frac{1}{I_D \lambda}$$

SPICE and y-parameter models

For the SPICE model, consider $\beta = KN \frac{W}{L}$

where W, L are gate width and length. Sometimes you will see 'Kp' (same as KN)

KN, W, L and λ = LAMBDA are SPICE parameters and **can be obtained from the manufacturer.**

Older data sheets often quote so-called y-parameters, y_{fs}, y_{os}, where: $y_{fs} \equiv g_m$ and $y_{os} \equiv g_{ds}$.

Comparison of BJT and MOST

Comparing the BJT and the MOST at a bias current level of, **I = 1 mA:**

Taking for the MOST: $\lambda = 0.05\ V^{-1}$, $\beta = 1\ mA/V^2$.

And for the BJT : $V_A = 150$ V,

And recalling: $r_{ds} = 1/I_D\,\lambda$, $r_{ce} = V_A/I_C$ $\quad g_m^{MOST} \sim \sqrt{2I_D\beta}$ $\quad g_{m\,(BJT)} = 40\ I_C$

$$r_{ce}/r_{ds} = V_A\lambda = 8;$$

$$\frac{g_{m(BJT)}}{g_{m(MOST)}} = 40\sqrt{\frac{I}{2\beta}} \approx 30$$

Hence the BJT can be thought of as is a superior device for use in linear circuits, at least in electrical terms.

great advantage of the MOSFET is the ability to make very simple switching circuits from it: a CMOS inverter comprises only two transistors: a p-channel and an n-channel.
Bipolar transistor switching circuits are based on a circuit similar to the differential amplifier configuration (ECL – emitter coupled logic); more complex hence take up more area on the Si chip and consume a lot more power. **See Dr Mitrovic's module**

Don’t confuse symbols!

β (BJT) is dc current gain $\beta \equiv h_{FE} = \frac{I_C}{I_B}$

Also used for ac current gain sometimes) – as well as β_o ....

β (MOST) is drive constant $\beta = KN\frac{W}{L}$

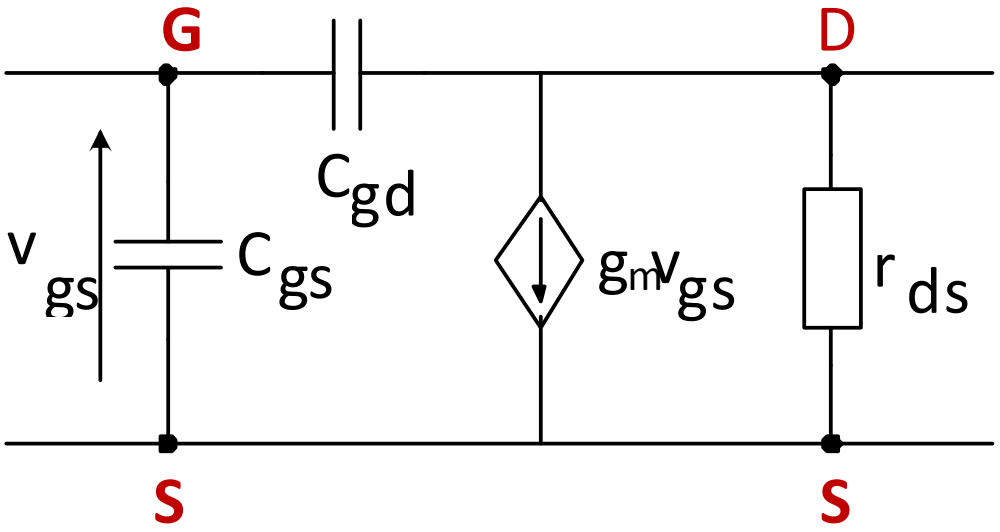
dimensions are A/V^2

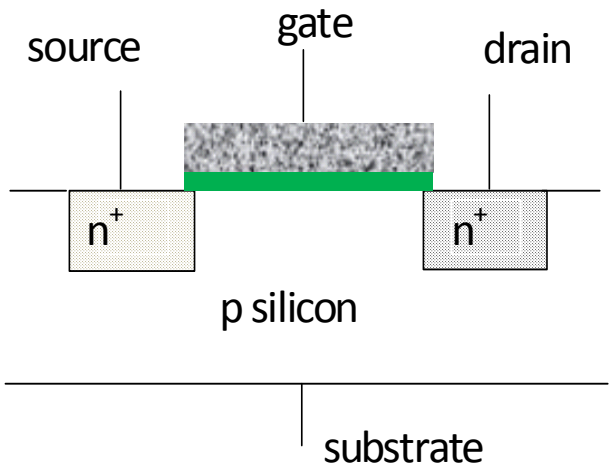
β_o (BJT) is ac current gain $\beta_o \equiv h_{fe} = \frac{\Delta I_C}{\Delta I_B} = \frac{i_c}{i_b}$

V_T is thermal voltage $V_T = \frac{kT}{q} \sim 25mV\,@\,300K$

V_T also used for threshold voltage of MOSFETs! (also V_{th} , V_{TH})

The FET at high frequency





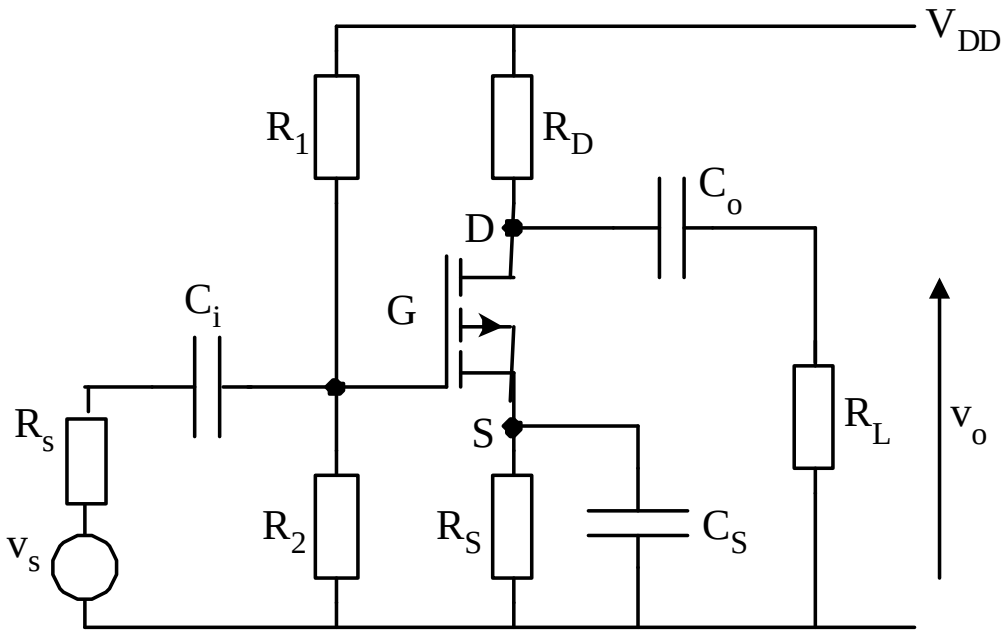
C_{gs} is the capacitance between the gate and source region
C_{gd} is the capacitance between the gate and drain region

Typically the order pF's in discrete MOSTs (small);

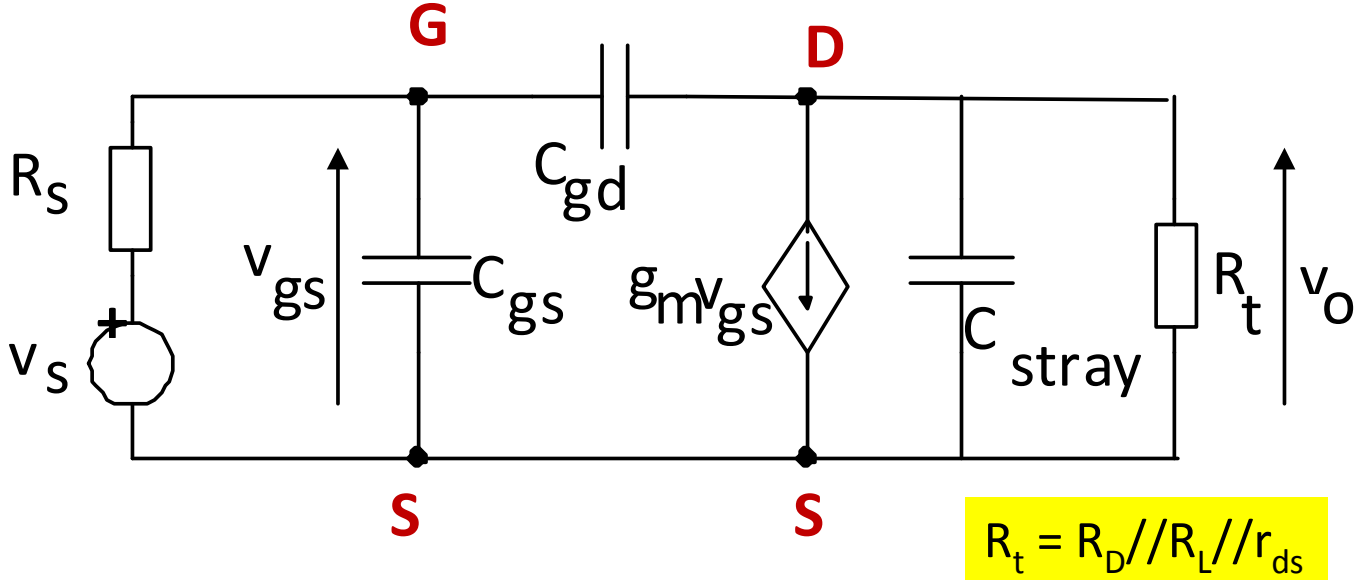
10-100's fF in I.C.'s. Discrete MOSFETs are therefore useful as very fast switches and high frequency amplifiers.

Discrete MOSFET common source amplifier

Schematic circuit



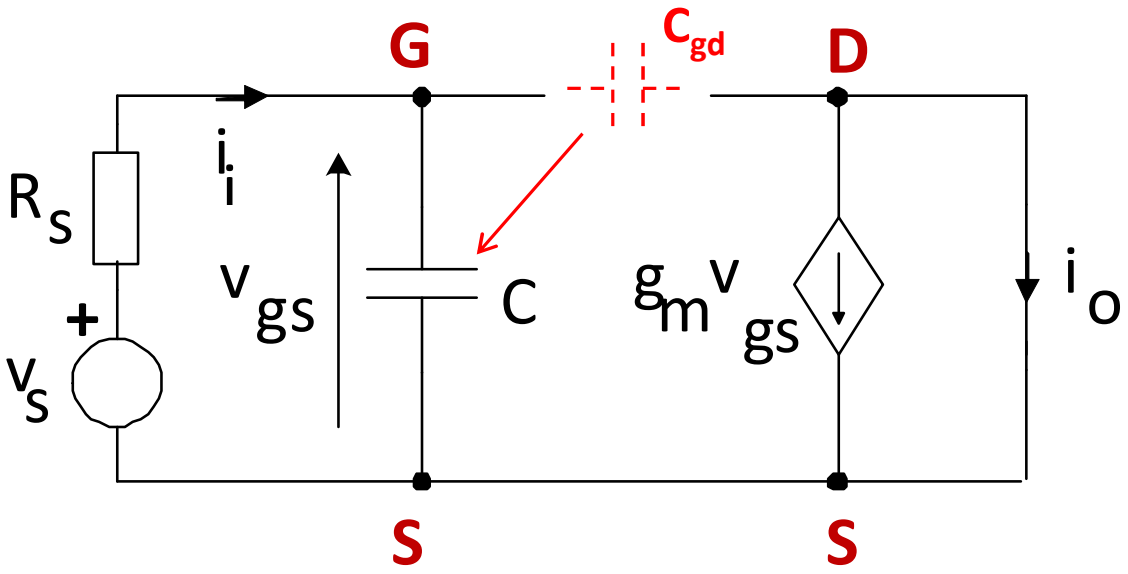
AC equivalent circuit



$R_t = R_D // R_L // r_{ds}$

Gain-bandwidth product – f_T

Follow the approach adopted for the bipolar transistor (part 6) :



$$i_o = -g_m v_{gs}$$

$$v_{gs} = \frac{i_i}{j\omega C}$$

$$\frac{i_o}{i_i} = -\frac{g_m}{j\omega \times C}$$

$$\left|\frac{i_o}{i_i}\right| = \frac{g_m}{2\pi \times f\left(C_{gs} + C_{gd}\right)}$$

Note we ignore the current delivered to the output via the feed-through capacitor C_{gd} ($i_{Cgd} << g_m v_{gs}$)

($f = f_T$ when current gain = 1)

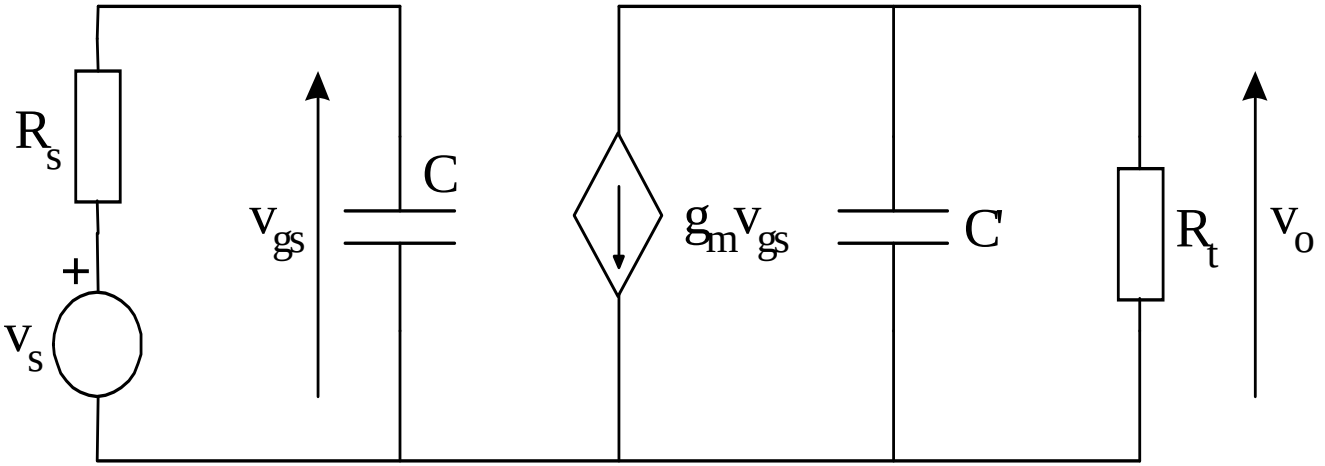
Then: $C = C_{gs} + C_{gd}$

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)}$$

Same form as the BJT!

Voltage-gain bandwidth

Apply **Miller's theorem** and again, see that the equivalent circuit comprises of two first order networks



$R_t = R_D // R_L // r_{ds}$

$$C = \left[C_{gs} + (1-K)C_{gd}\right]$$

$$C' = \left[C_{gd}\frac{K-1}{K} + C_{stray}\right] \approx C_{gd} + C_{stray}$$

The input and output circuits have characteristic time constants:

$$\tau_i = R_S\left[C_{gs} + (1-K)C_{gd}\right] \qquad \tau_o = R_t\left(C_{gd} + C_{stray}\right)$$

Generally $\tau_i >> \tau_o$ and we can therefore disregard the capacitor C' in the circuit.

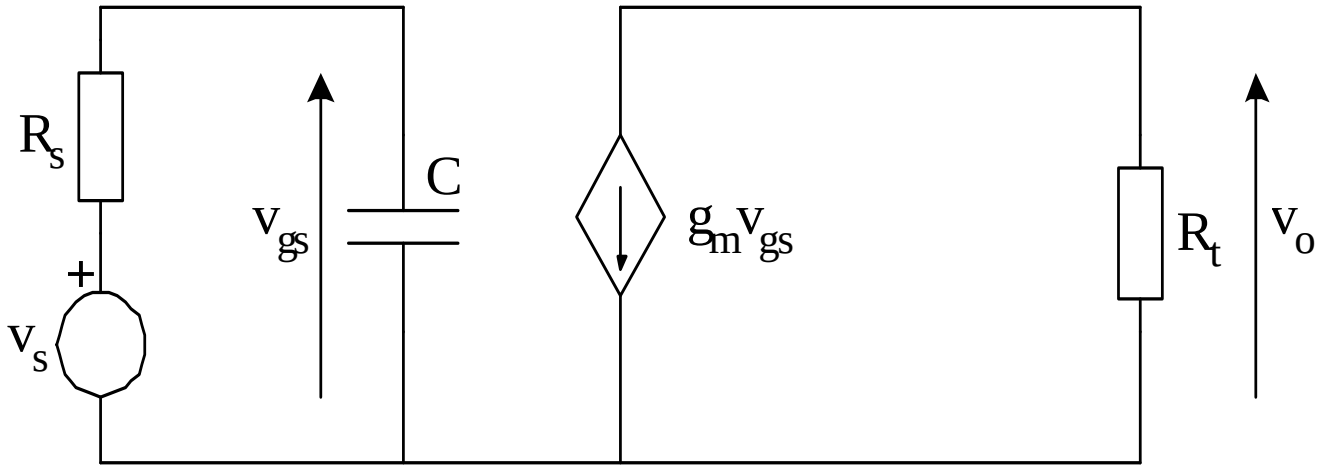
Note than in any problem, it is important to justify the use of this approximation.

Voltage-gain bandwidth: analysis

$$v_o = -g_m v_{gs} R_t$$

$$K = \frac{v_o}{v_{gs}} = -g_m R_t$$

$$C = C_{gs} + (1 + g_m R_t) C_{gd}$$



Voltage gain: $$A_{Vs} = \frac{v_o}{v_s} = \frac{v_o}{v_{gs}} \frac{v_{gs}}{v_s}$$

$$A_{Vs} = -g_m R_t \frac{1/j\omega C}{R_S + 1/j\omega C} = -g_m R_t \frac{1}{1 + j\omega R_S C}$$

$$A_{Vs} = -g_m R_t \frac{1}{1 + j\left(\frac{f}{f_H}\right)}$$

$$\boxed{f_H = \frac{1}{2\pi R_S C}}$$ **is the voltage gain bandwidth.**

Note

$$A_{Vs} = -g_m R_t \frac{1}{1 + j\left(\frac{f}{f_H}\right)}$$

$$f_H = \frac{1}{2\pi R_S C}$$

The low frequency gain is $-g_m R_t$: a similar expression to the BJT but

remember that g_m is given by a different expression for the MOST:

BJT: $g_m = 40 I_C$ MOST: $g_m = \sqrt{2 I_D \beta}$

Notice that, unlike the case of the bipolar transistor, there is no 'coupling term'.

Thus the high source resistance does not 'load' the front end of the amplifier (although take care with the bias resistors – a depletion mode device is best).

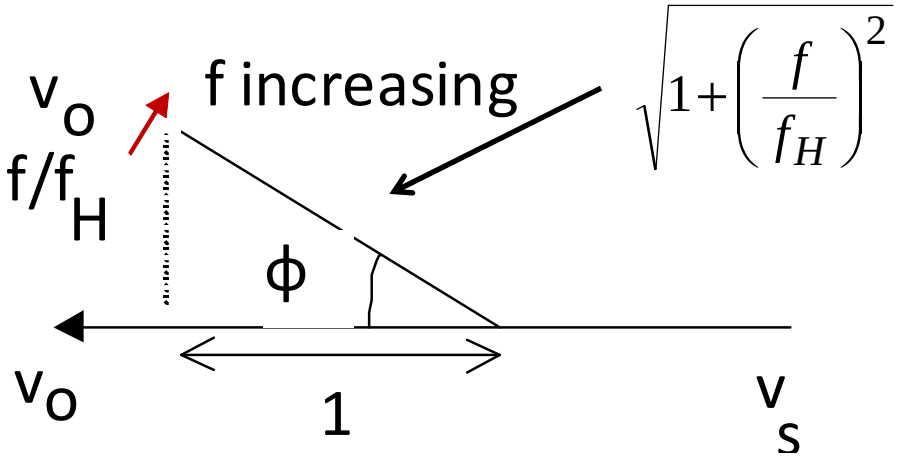
The low frequency gain is likely to be small because of the low g_m!

Phase

Similar analysis to that done earlier:

$$A_{Vs} = \frac{A_{Vso}}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}} e^{j(\pi-\phi)}$$

$$\tan(\phi) = \frac{f}{f_H}$$

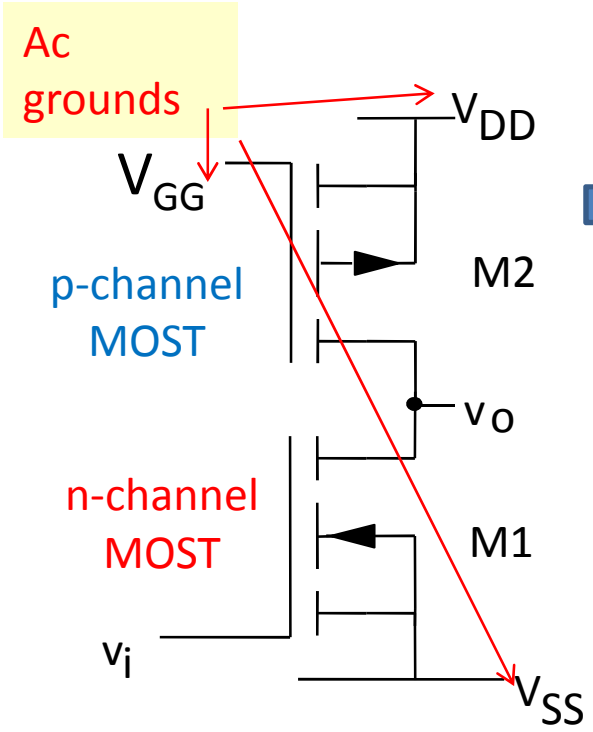


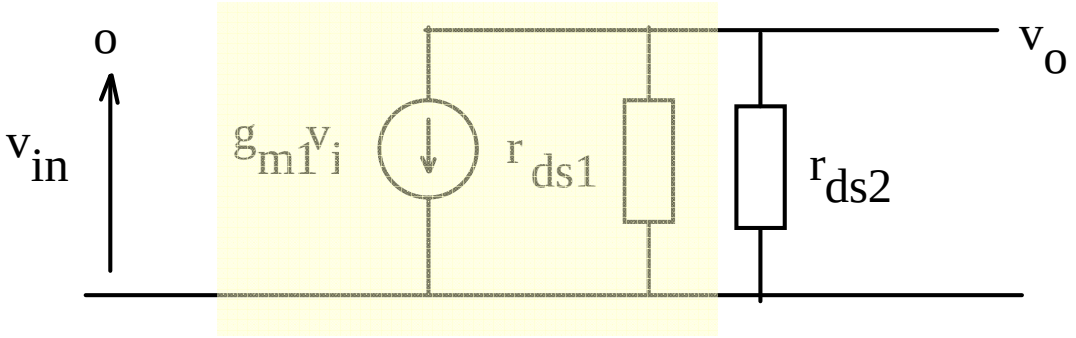
and ϕ gives the phase angle between v_s and v_o; $A_{Vso} = g_m R_t$

$$e^{j\pi} = -1$$

$$e^{j(\pi-\phi)} = e^{j\pi}e^{-j\phi} = (-1)[\cos\phi - j\sin\phi]$$

Increase the gain with an **active load**





Apply Ohm's Law on the output:

$$v_o = \frac{i}{g} = -\frac{g_{m1}v_i}{g_{ds1} + g_{ds2}}$$

where $g_{ds} = 1/r_{ds}$

This amplifier configuration
Is suitable for use as an
integrated circuit element
As MOSFETs occupy far less area
than the resistors used in
the earlier amplifier.

Using $\lambda = 0.01\ V^{-1}$, $\beta = 1\ mA/V^2$, $I_D = 0.1mA$ gives a gain of over 200!

Design Example: Set the low frequency roll-off at 100 Hz (say)

Assume: $Z_{CS} \ll R_S$

$$v_i = v_{gs} + g_m v_{gs} \times \frac{1}{j\omega C_S}$$

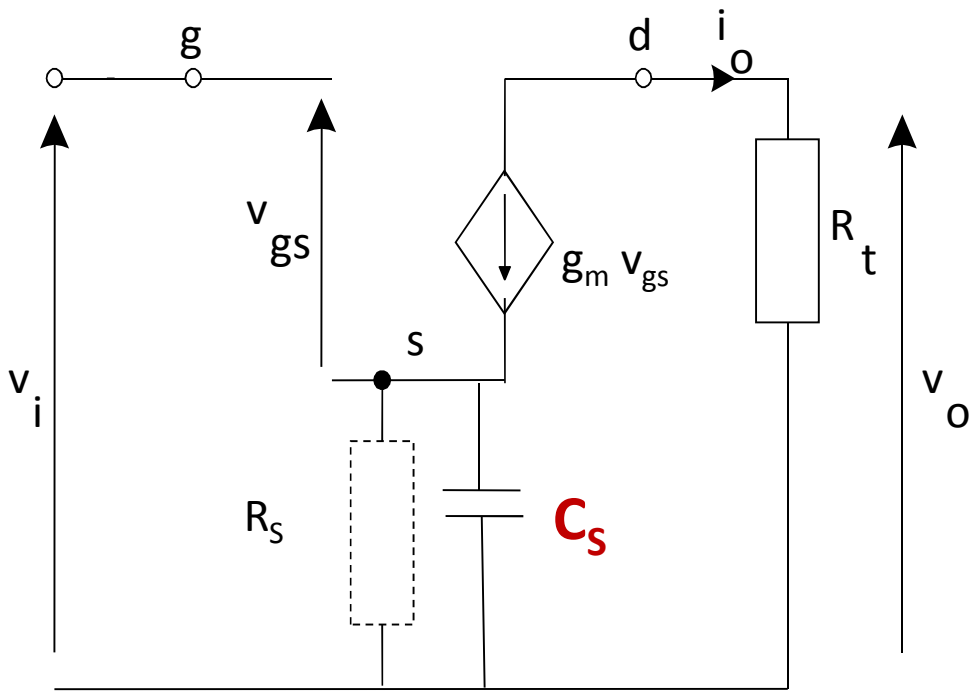
So $$v_{gs} = \frac{v_i}{1 + \frac{g_m}{j\omega \times C_S}}$$

Now, $$v_o = -g_m v_{gs} R_t$$

Therefore the voltage gain is,

$$\frac{v_o}{v_i} = -\frac{g_m R_t}{1 + \frac{g_m}{j\omega \times C_S}}$$

$$\left|\frac{v_o}{v_i}\right| = \frac{g_m R_t}{\sqrt{1 + \left(\frac{g_m}{j\omega \times C_S}\right)^2}}$$



Now the gain falls by $1/\sqrt{2}$ when: $g_m = \omega \times C_S$

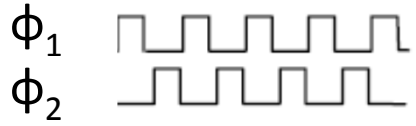
$$C_S = \frac{g_m}{2 \times \pi \times f_L}$$

$$g_m = \sqrt{2 \times I_D \times \beta}$$

100 Hz

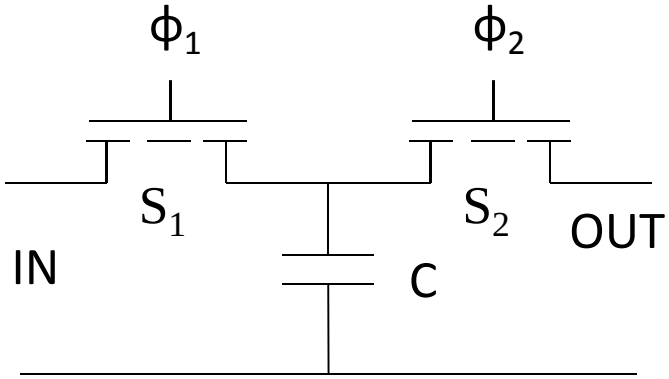
The switched-capacitor resistor (SCR)

2 MOSFETs used as switches, S1 and S2 and a capacitor, C.
clock the switches with ϕ_1 ϕ_2 at frequency, *f*.



Operation

- Assume C is initially discharged:
- ϕ_1 goes high, S_1 turns on and C charges to V_1,
- ϕ_2 goes high (ϕ_1 is low), S_2 turns on, and C discharged to V_2.



- charge transferred during this process is

$Q = C(V_1 - V_2)$ and this occurs during one clock cycle, T_C.

equivalent, average current is then: $I = \frac{Q}{T_C} = \frac{C(V_1 - V_2)}{T_C}$ $I = f_C C(V_1 - V_2) = \frac{V_1 - V_2}{R_{eq}}$

$R_{eq} = 1/(f_C C)$

A small C with a low switch frequency provides large resistance. This means it can be easily fabricated on a chip, with a compact layout. Use in op-amp circuits, ADCs, other

Worked Example

A transducer exhibits a very high internal resistance of R_S = 100 kΩ. A MOSFET is therefore to be used to amplifier its output. Work out values for the mid-frequency gain and the bandwidth of a common source amplifier given the following information:

For the MOSFET: C_{gs} = 4 pF, C_{gd} = 1 pF, β = 0.1 mA/V²

Circuit (CS amp): R_S = 100kΩ, I_D = 1 mA (bias level), R_t = 22kΩ, C_S = 1pF (stray)

Solution

Mid frequency gain: $A_{Vs} = -g_m R_t$ $\quad g_m = \sqrt{2 I_D \beta} = \sqrt{2 \times \left(1.10^{-3}\right) \times \left(0.1 \times 10^{-3}\right)} = 0.45 mA/V$

$$\therefore A_{Vs} = -\left(0.45 \times 10^{-3}\right) \times \left(22 \times 10^{3}\right) = -9.9$$ ***(note small V-gain)***

Input time constant $\tau_i = R_S \left[C_{gs} + (1-K) C_{gd}\right] = 1.5 \mu s$

Output time constant $\tau_o = R_t \left(C_{gd} + C_s\right) = 0.04 \mu s$

Clearly input time const. >> output time const.

justifies use of $f_H = \dfrac{1}{2\pi \times R_S C}$ for voltage gain bandwidth.

Effective input capacitance: $C = C_{gs} + (1 + A_{Vs}) C_{gd} = 15 pF$ **Bandwidth = 106 kHz**

Low because of high source resistance. If R_S was 50 Ω, get f_H = 200 MHz.

1. Derive equations for the transconductance and output resistance of a MOSFET in the linear region of operation.

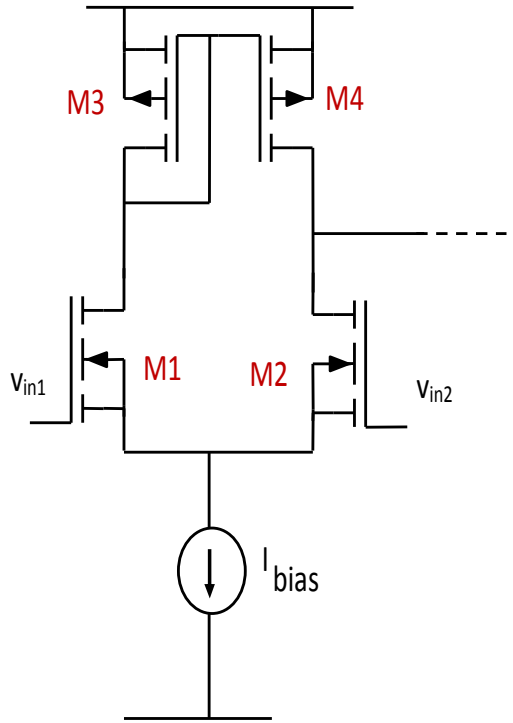
$$I_D = \beta\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}=const} = \beta \times V_{DS}$$

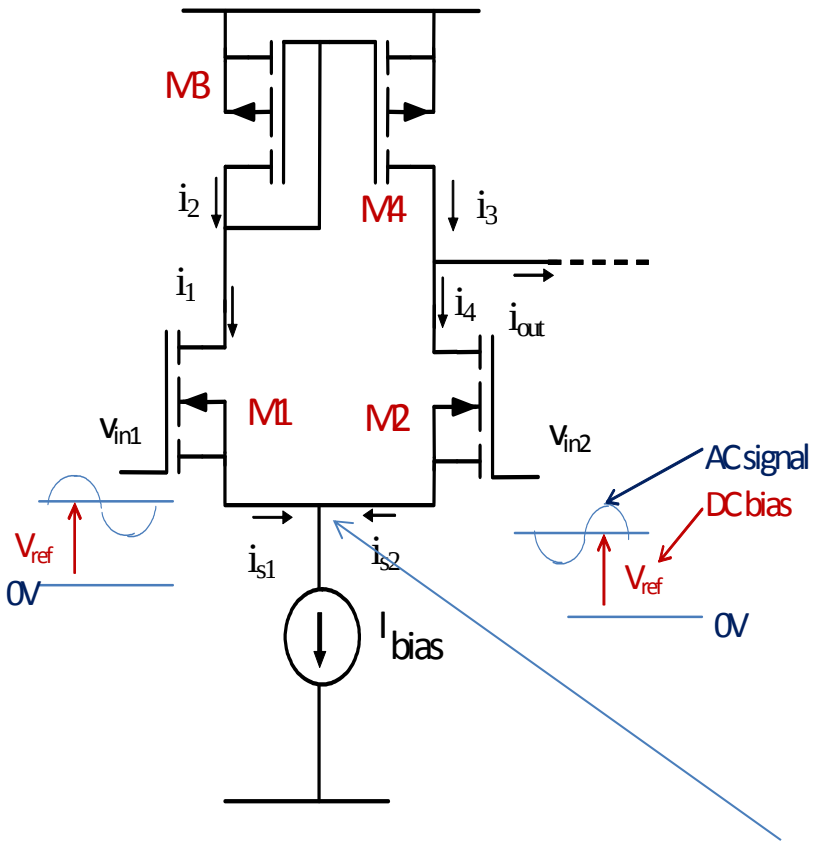
$$g_{ds} = \left.\frac{\Delta I_D}{\Delta V_{DS}}\right|_{V_{GS}=const} = \beta \times (V_{GS} - V_T - V_{DS})$$

$$r_{ds} = \frac{1}{g_{ds}}$$

2. The figure shows a differential amplifier. Assuming that the amplifier feeds into a very large load resistance, show that the differential gain is given by $g_m \times r_{ds2} // r_{ds4}$ and the common mode is (ideally) zero. The technique is shown in part 5 – this derivation is much easier!



MOSFET Differential Amplifier



$$I_D \sim V_{GS}^2$$

$$i_1 = i_2$$

$$i_2 = i_3$$

Over 1st half of sine wave, i_1 increases, hence so does i_3

i_4 reduces, hence

$$i_{out} = i_4 - i_3$$

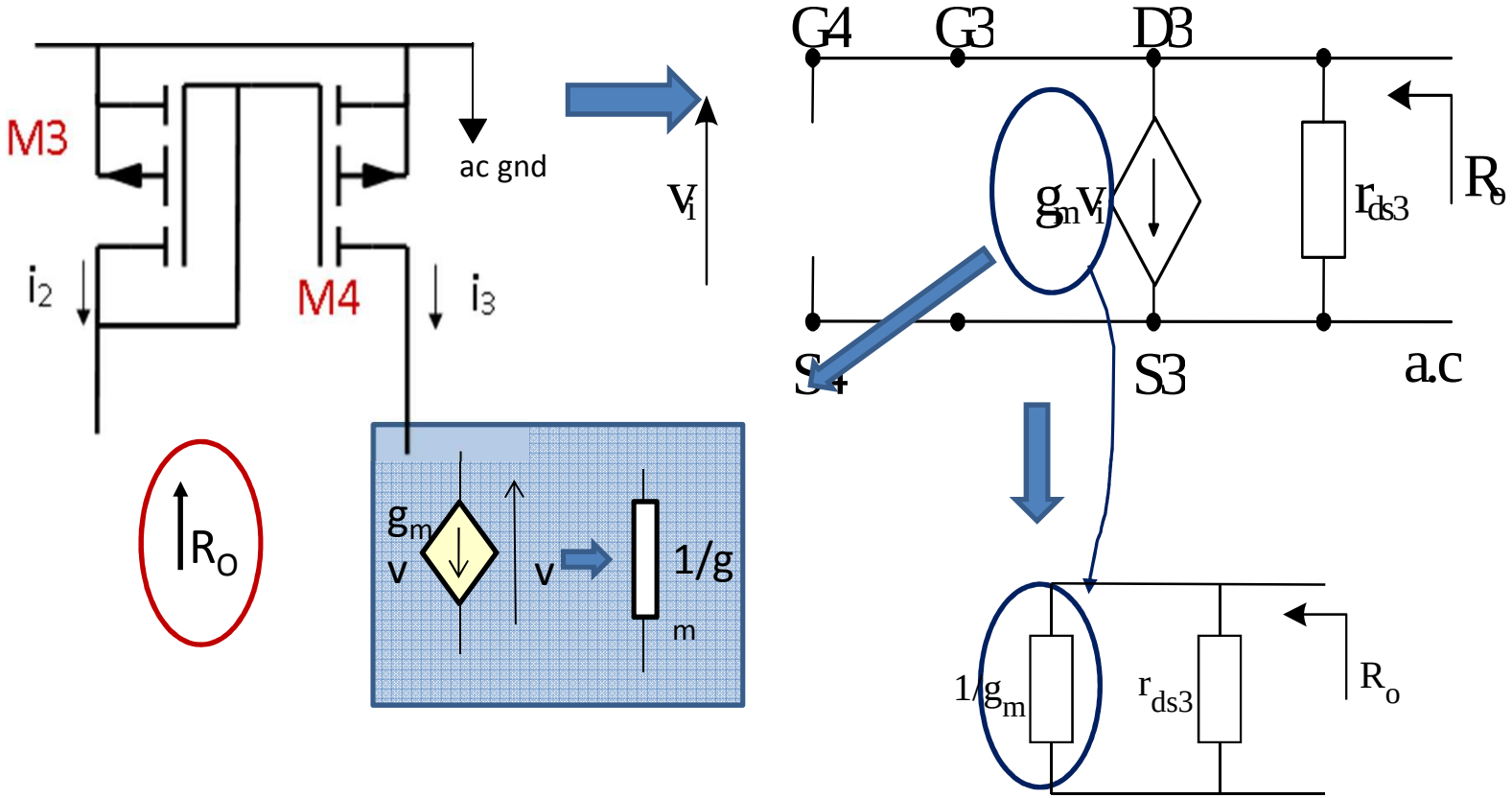
$$i_{s1} = -i_{s2}$$

voltage gain?

So forms an ac ground

a.c. analysis: simpler than for BJTs!

Need an equivalent circuit for the current mirror load: what 'resistance' is seen looking up into the current mirror?



The approximation opposite can again be made

(see Widlar CM notes)

$$R_o = \frac{1}{g_m} // r_{ds3} \approx \frac{1}{g_m}$$

Ac equivalent circuit for A_{Vd} (ignore r_{ds})

Note that the voltage drop across the $1/g_m$ load is

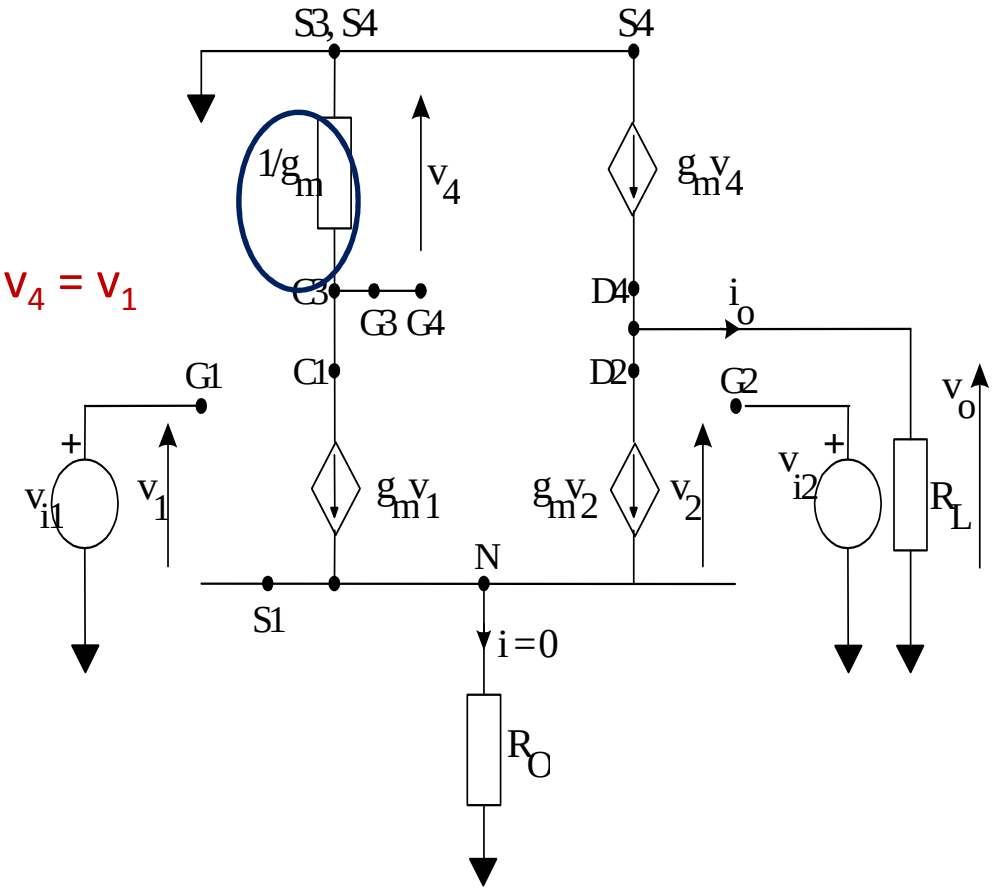
$v_4 = (g_m v_1) \times 1/g_m = v_1$ So $v_4 = v_1$

Then write:

$i_o = g_m (v_4 - v_2)$ (KCL)
$= g_m (v_1 - v_2)$
$= g_m v_{id}$;

That is, $i_o = g_m v_{id}$

So $v_o = g_m v_{id} R_L$



$\therefore A_{vd} = g_m R_L$ (single ended voltage gain)

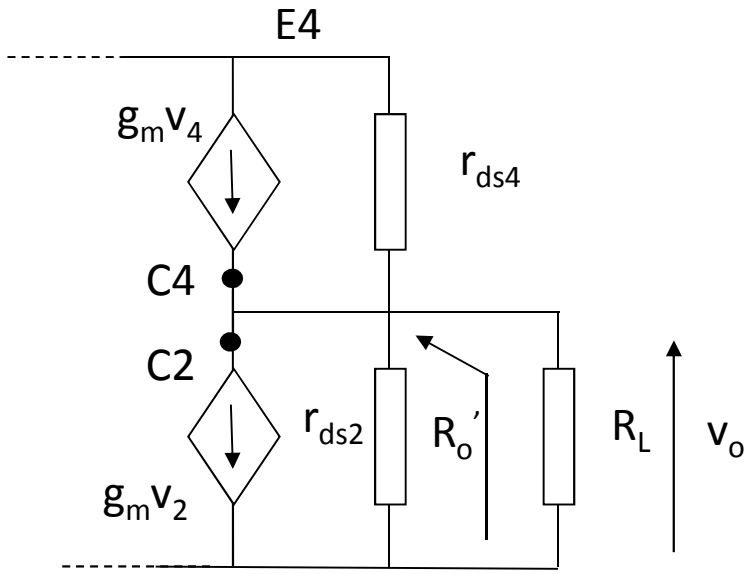
Include the effect of r_{ds}'s

v_2 and v_4 are set to zero

(by convention) for finding

output resistance,

the a.c. load is by inspection,



$R_o' = r_{ds4} // r_{ds2}$ and $R_o = r_{ds4} // r_{ds2} // R_L$

So **without** R_L $A_{Vd} = g_m (r_{ds4} // r_{ds2})$ - VERY HIGH

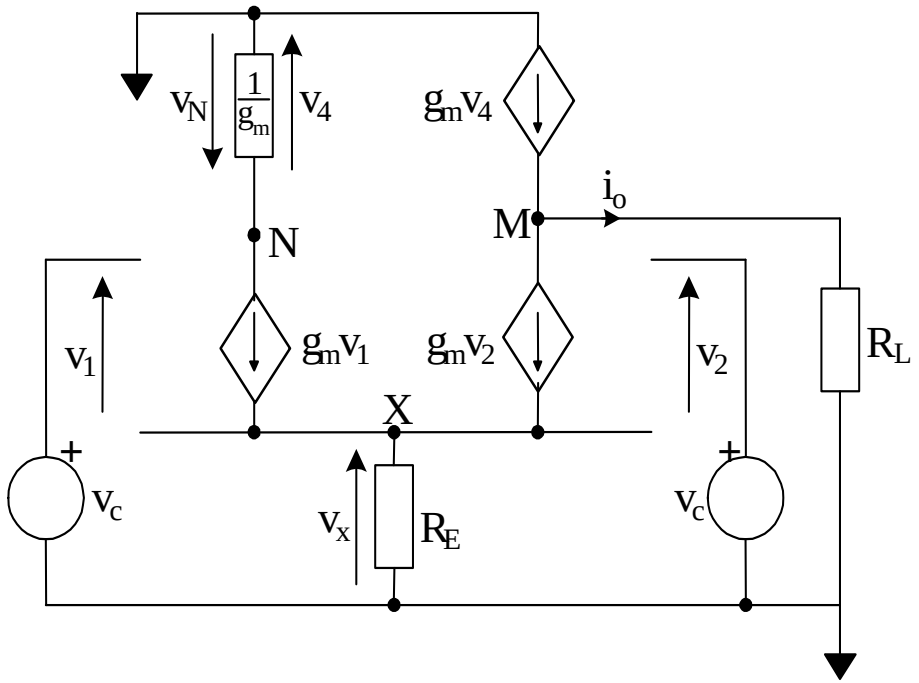
Common Mode Gain

Currents in left and right- hand sides of the circuit are the same (by CM action), so

$i_o = 0$

$v_o = 0$

$A_{vc} = 0$



Ideally, the common-mode gain is zero! (In reality, very small)

End of MOSFET lecture

- Now look at step response of amplifiers

Design Exercise 2

Design a 2-stage voltage amplifier to meet the following criteria:

i) an input resistance of 100 kΩ

ii) an overall voltage gain > 500, with a resistor load of 10kΩ.

Given: V_{CC} = 20V, β_o = 200

DC level of the first stage output needs to be set at half the supply voltage.

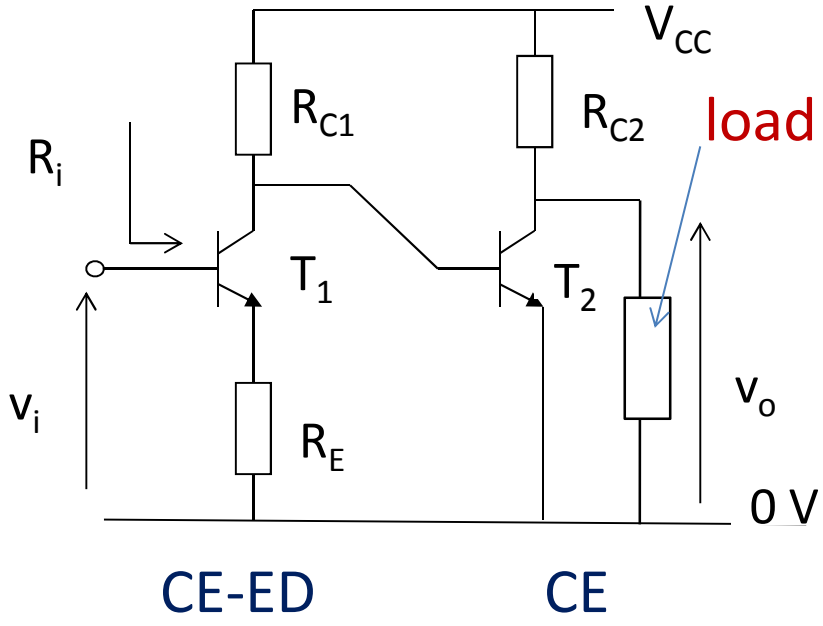
Allow 10% of V_{CC} across R_E)

Use CE-ED (R_E) stage for the input and a CE stage biased at 1mA

Solution.

The schematic circuit

omitting bias resistors and coupling capacitors



Design

First consider input resistance spec.

$$g_m \times r_{be} = \beta_o$$

$$R_i = r_{be1} + (1+\beta_o)R_E$$

10% V_{CC} across R_E

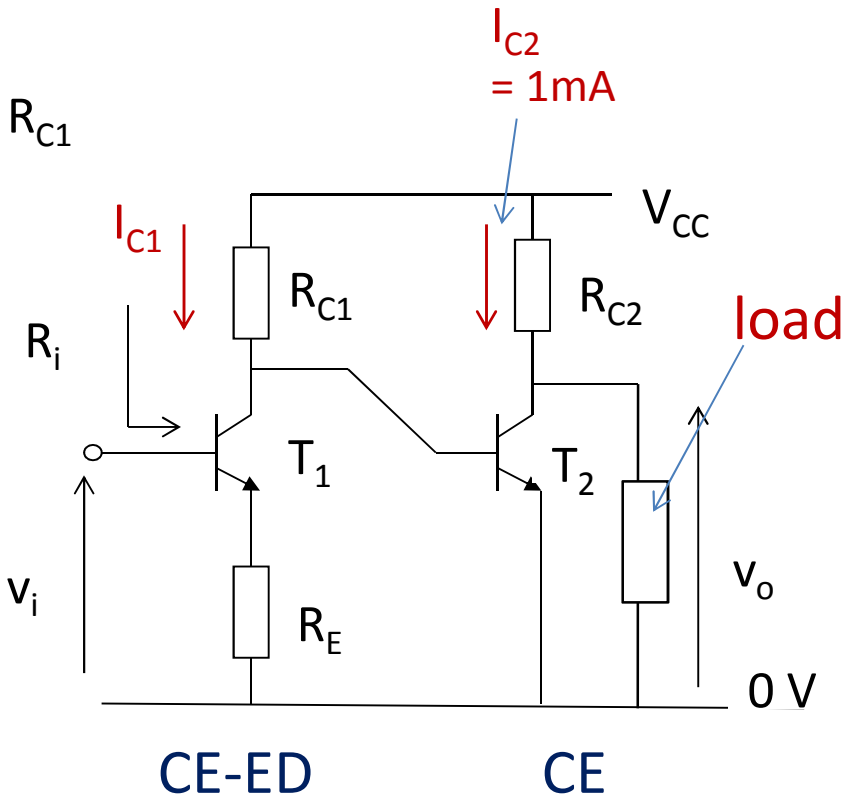
$$\Rightarrow 100k = \frac{200}{40I_{C1}} + (1+200)\frac{2}{I_{C1}}$$

I_{C1} = 4.1mA

V_{CC} /2 across R_{C1}

$$R_E = \frac{2}{4.1m} = 494\Omega$$

$$R_{C1} \sim \frac{20}{2}\frac{1}{4.1m} = 2.5k\Omega$$



Gain of 1st stage is $$A_{V1} = -\frac{g_{m1} \times R_{C1} // R_{i2}}{1 + g_{m1} \times R_E}$$

$$R_{i2} = r_{be2} = \frac{\beta_o}{g_{m2}} = \frac{200}{40 \times 1mA} = 5k\Omega$$

$$A_{V1} = -\frac{40 \times 0.41m}{1 + 40 \times 0.41m}\frac{2.5 \times 5}{2.5 + 5}k$$

$$= 3.31$$

Want total gain to be >500, so A_{V2} = 500 /3.31 = 151; **A_{V2} = 155 say**

Design - 2

Gain of second stage is $A_{V2} = -g_{m2} R_{C2} \,//\, R_L$

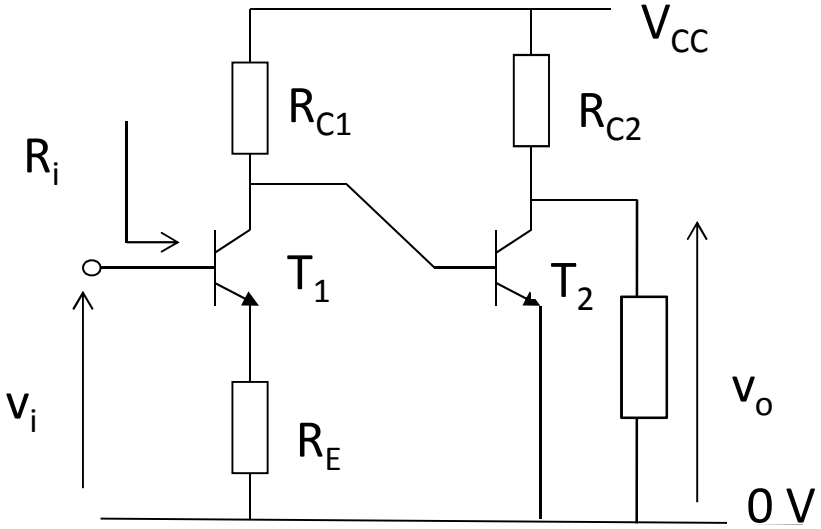
$$A_{V2} = -40 \times 1m \times \frac{R_{C2} 10k}{R_{C2} + 10k}$$

$$155(R_{C2} + 10k) = -40m \times R_{C2} \times 10k$$

$$155R_{C2} + 1550k = 400R_{C2}$$

$$R_{C2} = \frac{1550}{400 - 155} k$$

R_{C2} = 6.4k



Note, use the nearest preferred values in a real design so use R_{in} > 100k, A_V > 500

Gain could be made higher by adding a further CE stage,
Input resistance could be improved by using **feedback**: sacrifice some gain.

Next Topic

- Feedback

Next lecture

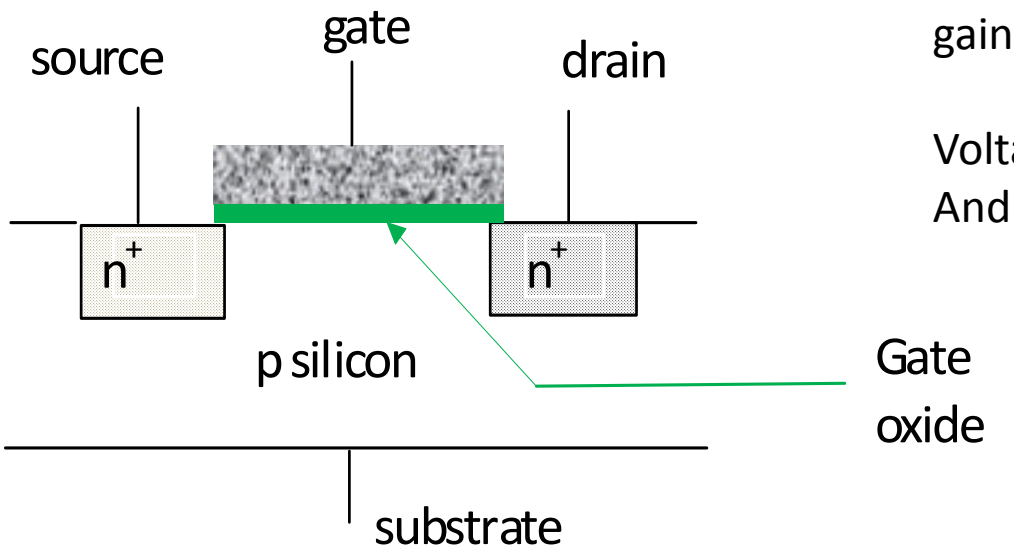
- Consider the TRANSIENT response of an amplifier – response to a voltage STEP applied to the input
- Forms a simple method measurement of the amplifier voltage bandwidth

Lecture today

- Finish MOSFET lecture
  - SCR – a device for achieving large R-values in a small space
  - worked example
- Design example 2 – a 2-stage amplifier (BJT)
- Introduction to Feedback

Note that Pre-Lab test for Expt 5 (Op-amp design) is now live on VITAL

Last time: The MOSFET



gain-bandwidth product $f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})}$

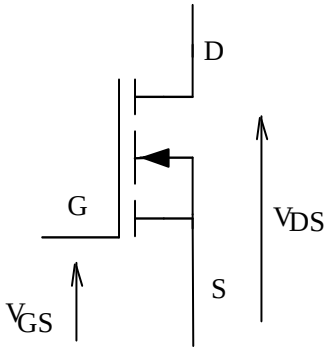
Voltage gain And b'width $A_{Vs} = -g_m R_t \frac{1}{1+j\left(\frac{f}{f_H}\right)}$ $f_H = \frac{1}{2\pi R_S C}$

Enhancement mode device

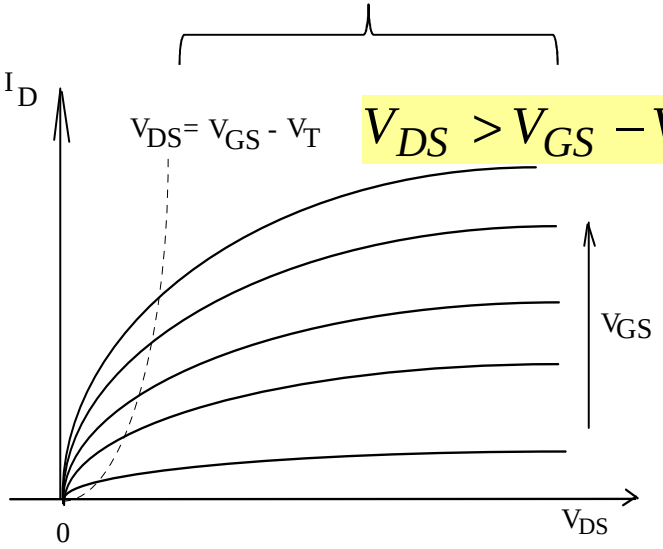
$$\beta = (\mu C_o)\frac{W}{L}$$

$$\beta = KN\frac{W}{L}$$

$$C_o = \frac{\varepsilon_o \varepsilon_s}{t_{ox}}$$



$$I_D = \frac{\beta}{2}[V_{GS} - V_T]^2(1+\lambda V_{DS})$$



μ = mobility, C_o = gate oxide capacitance /unit area;
W and L are the physical width and length of the gate. **λ is the slope on the output characteristic**