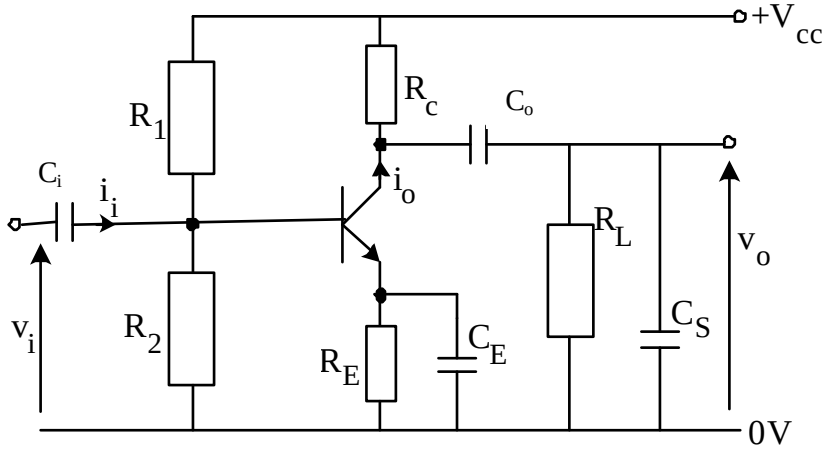
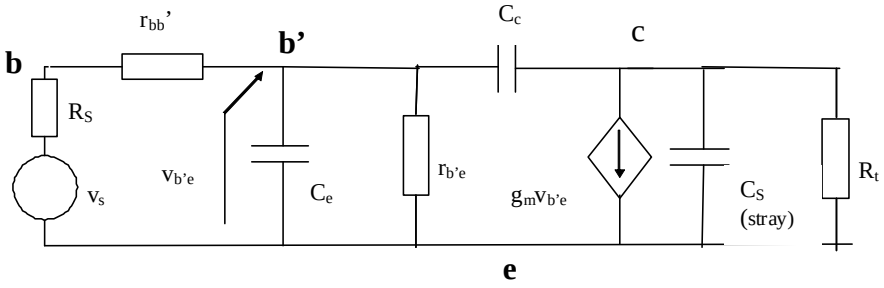
High frequency voltage gain of CE amplifier

We now analyse for voltage gain. The presence of a collector load means that the effective collector capacitance C_c is greatly increased by the Miller effect, explained below.

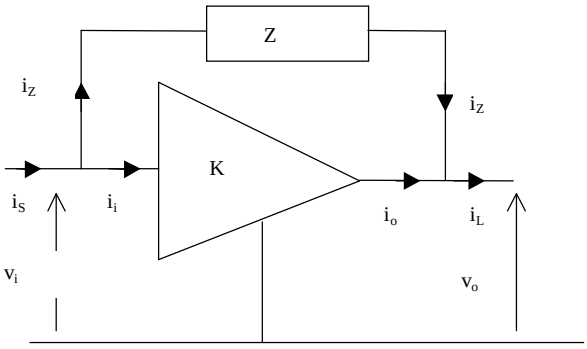


Notice that we have included stray capacitance (C_S) on the output terminal. The equivalent circuit is



The large (amplified) voltage signal on the right hand plate of the collector capacitor, C_C compared to the small input voltage on the opposite plate effectively 'amplifies' C_C to ~ KC_C where K is the voltage gain. This is the Miller effect. The following theorem allows us to simplify the analysis considerably.

Miller's theorem
Consider the amplifier shown opposite.



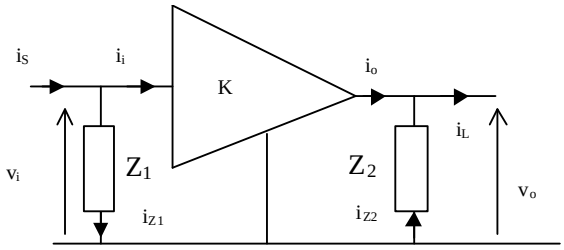
The voltage gain is K where

$$K = \frac{v_o}{v_i}$$

We will now show that this configuration can be re-drawn as that shown underneath if the impedances are of value:

$$Z_1 = \frac{Z}{1-K}$$

$$Z_2 = Z\left[-\frac{K}{1-K}\right]$$



Proof:

Consider the input side of the two amplifier
We seek to find the condition such that $i_Z = i_{Z1}$.
Now KCL gives:

$$i_S = i_Z + i_i$$

and $$i_Z = \frac{v_i - v_o}{Z} = \frac{v_i}{Z}\left(1 - \frac{v_o}{v_i}\right) = \frac{v_i}{Z}(1-K)$$

looking at the lower diagram, $$i_{Z1} = \frac{v_i}{Z_1}$$

so for $i_{Z1} = i_Z$, we have

$$\frac{v_i}{Z_1} = \frac{v_i}{Z}(1-K)$$

Giving $$Z_1 = \frac{Z}{1-K}$$

for the currents on the input side of the 2 configurations to be the same.

Consider the output side of the two amplifiers

$$i_L = i_Z + i_O$$

and $$i_Z = \frac{v_i - v_o}{Z} = \frac{v_o}{Z}\left(\frac{v_i}{v_o} - 1\right) = \frac{v_o}{Z}\left(\frac{1}{K} - 1\right)$$

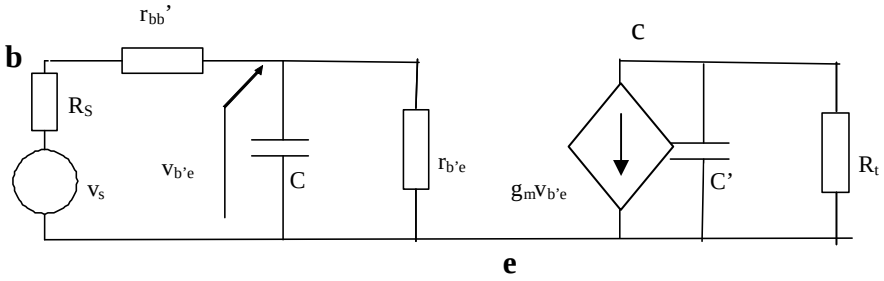
we require $i_{Z2} = i_Z$, to make the two circuits equivalent, i.e.

$$-\frac{v_o}{Z_2} = \frac{v_o}{Z}\left(\frac{1}{K} - 1\right)$$

Re-arranging: $$Z_2 = Z\left(-\frac{K}{1-K}\right)$$

and the currents on the output side of the 2 configurations are the same.

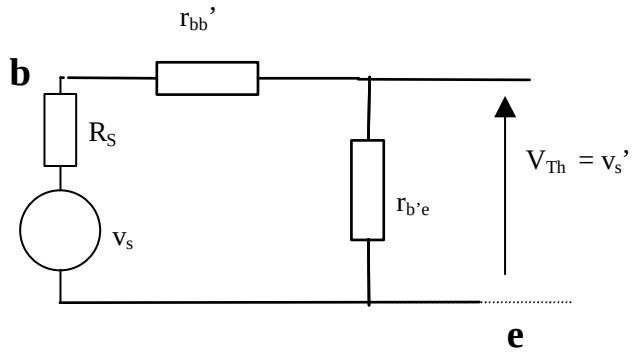
use the Miller theorem to transform the equivalent circuit:



where $C = C_e + C_c(1 - K) \approx C_e + C_c\,|K|$ $\qquad$ $C' = C_S + C_c(K - 1)/K \approx C_S + C_c$

because $K = -\,g_m R_L >> 1$

Note that the equivalent circuit comprises of two first order networks: input and output circuits. Now convert the input circuit to a Thevenin equivalent. Remove the capacitor to get:

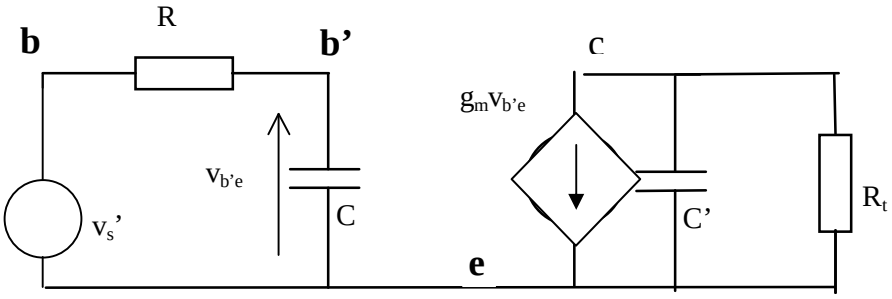


The Thevenin voltage and resistance are

$$v_s' = \frac{r_{b'e}}{r_{b'e} + r_{bb'} + R_S}\, v_S$$

$$R = r_{b'e} \,//\, \left(R_S + r_{bb'}\right).$$

Hence the equivalent circuit reduces to



Both input and output sections of the amplifier are simple, first order circuits. Consider the time constants ('RC') of the two first order circuits:

$$\tau_i = RC = \left[r_{b'e} \,//\, \left(R_S + r_{bb'}\right)\right]C \qquad \tau_o = R_t C'$$

Now it is generally the case that the input time constant is much greater than the output time constant i.e., $\tau_i >> \tau_o$ and the capacitor C', in the circuit can therefore be disregarded.

Note than in any problem, it is important to justify the use of this approximation and this is easily done for given values of R_C, R_L, C_c etc.

Using this approximation, it is the *input time constant* that sets the response of the amplifier and we proceed to analyse the last circuit above:

$i_o = - g_m v_{b'e} = v_o/R_t$

$v_o = - v_{b'e} g_m R_t$ (*)

Now potential division across R and C gives

$$v_{b'e} = v_s' \frac{1/j\omega C}{R + 1/j\omega C} = v_s' \frac{1}{1 + j\omega RC} \quad \rightarrow \quad v_o = -v_s' \frac{1}{1 + j\omega RC} g_m R_t$$

where we have multiplied top and bottom by jωC and substituted into (*). Substituting for v_s' and R and re-arranging, we get the desired expression for voltage gain in the standard form:

$$A_{Vs} = \frac{v_o}{v_s} = -g_m R_t \frac{r_{b'e}}{r_{b'e} + r_{bb'} + R_s} \frac{1}{1 + j\left(\frac{f}{f_H}\right)}$$

$$v_s' = \frac{r_{b'e}}{r_{b'e} + r_{bb'} + R_S} v_S$$

$$R = r_{b'e} // \left(R_S + r_{bb'}\right).$$

where $f_H = \dfrac{1}{2\pi\left[r_{b'e} // \left(r_{bb}' + R_S\right)\right]C}$ is the voltage gain bandwidth.

Notes:

1. The low frequency gain ($f << f_H$) is

$$A_{Vs} = \frac{v_o}{v_s} = -g_m R_t \frac{r_{b'e}}{r_{b'e} + r_{bb'} + R_s}$$

Notice that, if $r_{bb}' = 0$ and $R_S = 0$, then $A_{Vs} = -g_m R_L$: an approximation we have usually used. The more exact expression shows the need for a low source resistance to achieve high voltage gain, that is a coupling factor close to unity. A low source resistance however can have implications for other properties of the amplifier such as distortion but that is beyond the scope of this course.

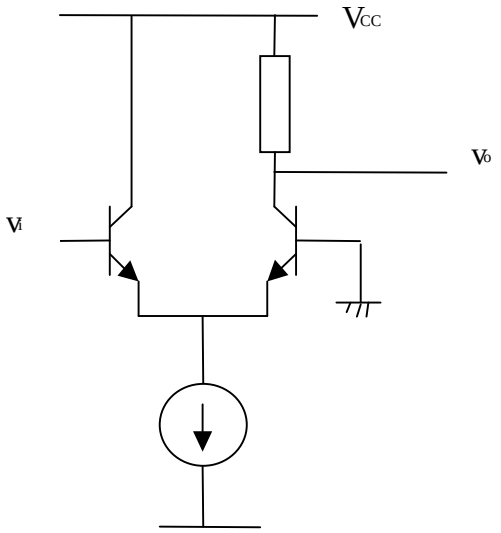
2. An approximation inherent in our use of the Miller theorem is that the input capacitance is overestimated because we have used the *low frequency* expression for 'K' although we are analysing up to high frequencies. This approximation leads to an *under-estimate* of $f_{H.}$ However, we also neglected the output time constant and this results in an *over-estimate* of $f_{H.}$ The net effect of these approximations is that we *over-estimate* the bandwidth f_H by 5-10% (i.e. get a bigger value). This is often accurate enough for our purposes. Circuit simulators such as SPICE can provide a more accurate analysis.

3. Consider again the bandwidth of the amplifier, which we write out in full:

$$f_H = \frac{1}{2\pi\left[r_{b'e} \,//\, \left(r_{bb}' + R_S\right)\right]\left(C_e + C_c|K|\right)} \qquad \text{for K >>1}$$

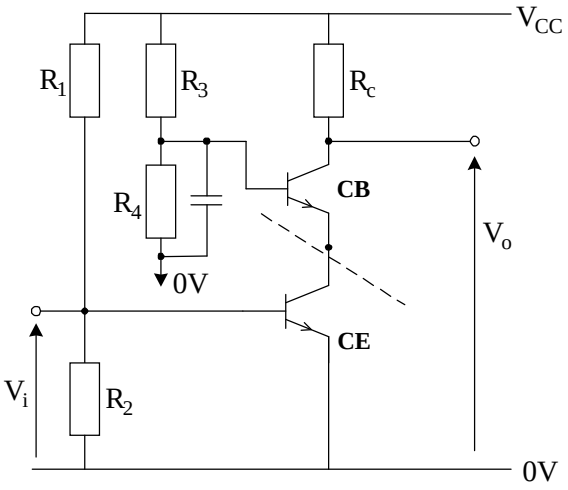
We see that the Miller effect causes a considerable reduction in bandwidth as it 'amplifies' the capacitor C_c by the voltage gain of the amplifier. R_S also reduces bandwidth. Below are two circuits which reduce Miller effect and so have greatly increased bandwidth:

We have seen (problem 5) that this differential amplifier configuration can be considered a two-stage, d.c. coupled amplifier: CC followed by CB. CC is inherently immune to Miller Effect because it has less than unity voltage gain (K < 1). The CC also presents a low impedance into the CB stage. CB does not experience Miller Effect (why?).



Another example is the 'cascode'configuration which involves a CE stage with a CB stage in the collector load. The CE stage 'sees' the small input resistance of the CB stage as its load. There is therefore very little change in collector voltage for the CE and hence no Miller Effect.
($A_{VCE} \sim -g_m R_t = g_m.r_e = -1$)

The collector current however, passes through to the top transistor and hence the output voltage is developed across R_C. As before, the CB does not suffer from Miller Effect.



Again, this can be analysed as a multi-stage amplifier; CE followed by CB. Note that the resistors $R_1 – R_4$ provide the biasing and the capacitor provides an a.c. ground on the base of CB.

Voltage gain of the CB stage is $A_{VCB} \sim g_m R_t = g_m.R_C$
So overall gain is $A_V = A_{VCE} \times A_{VCB} = -1 \times g_m R_C = -g_m R_C$

Phase relationships

Voltage gain

Write as $A_{Vs} = \frac{v_o}{v_s} = -\frac{A_{Vso}}{1 + j\frac{f}{f_H}}$ $\quad\left[A_{Vso} = g_m R_t \frac{r_{b'e}}{r_{b'e} + r_{bb'} + R_s} \right]$

to find phase information between v_o and v_s, we need to convert to polar co-ordinates:

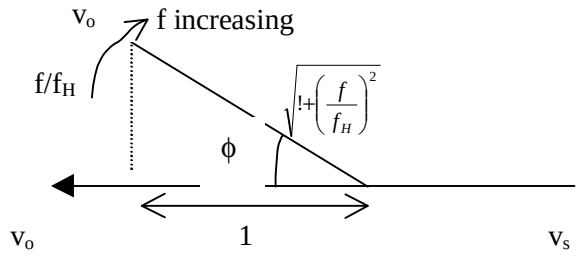
$$A_{Vs} = -\frac{A_{Vso}}{1 + j\frac{f}{f_H}} \frac{1 - j\frac{f}{f_H}}{1 - j\frac{f}{f_H}}$$

$$A_{Vs} = -\frac{A_{Vso}}{1 + \left(\frac{f}{f_H}\right)^2}\left(1 - j\frac{f}{f_H}\right) = -\frac{A_{Vso}}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}}\left(\frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}} - \frac{j\frac{f}{f_H}}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}}\right) \quad (*)$$

This can be represented in the standard form:

$$A_{Vs} = \frac{A_{Vso}}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}} e^{j(\pi - \phi)}$$

where $\tan(\phi) = \frac{f}{f_H}$ and ϕ gives the phase angle between v_s and v_o.



[Maths note : Recall for complex numbers that:

1. $\cos\phi - j\sin\phi = e^{-j\varphi}$

$$cos(\varphi) = \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}} \qquad sin(\varphi) = \frac{f/f_H}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}}$$

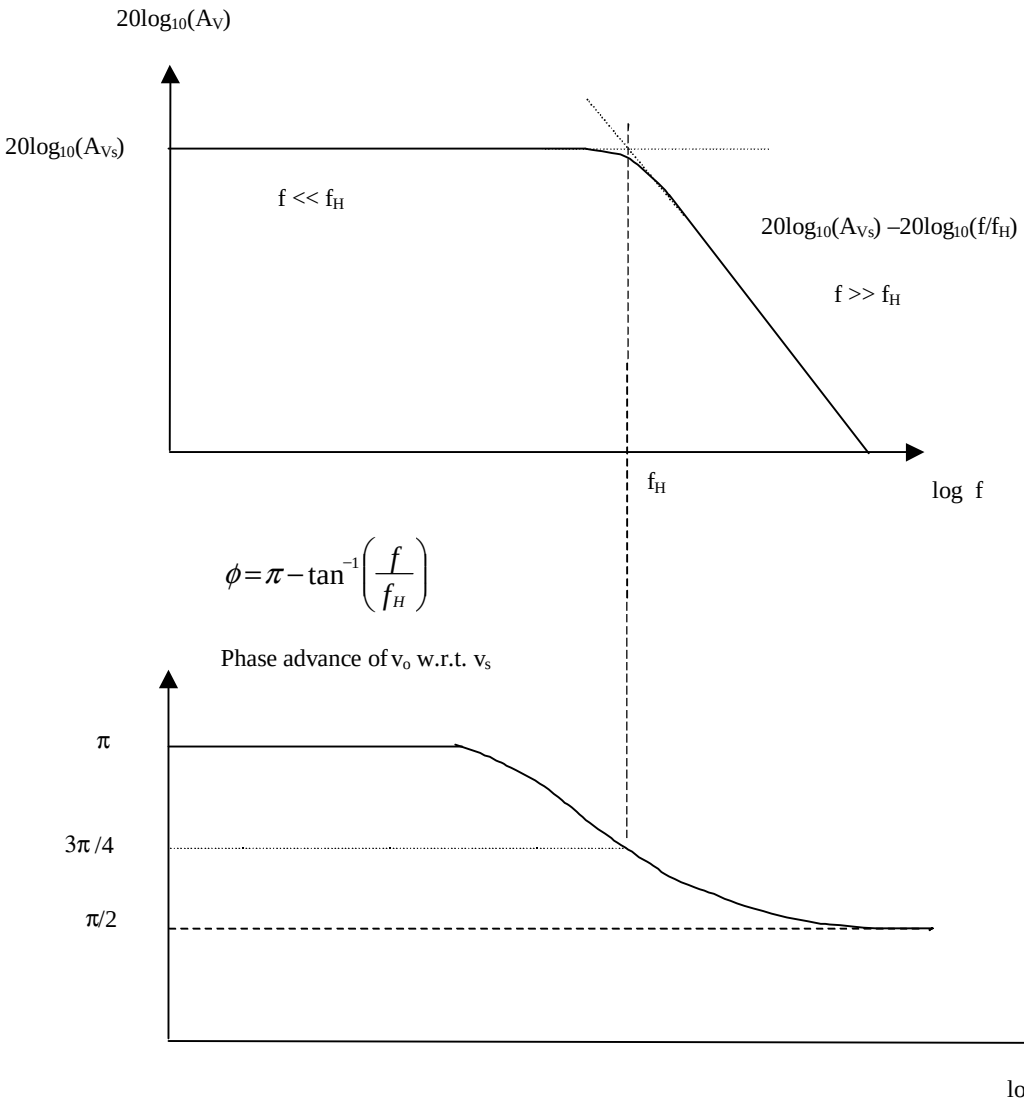
2. $e^{j\pi}$ *= -1 and this accounts for the -ve sign in front of the gain (Eqn *)*

3. $e^{j\pi}.e^{-j\phi} = e^{j(\pi-\phi)}$*; the magnitude of the phase term,* $e^{j(\pi - \phi)}$ *is always equal to one, so the exponential term does not affect the overall magnitude of the gain.]*

Note: $f = 0$ (or $f << f_H$), $\tan(\phi) = 0$ hence $\phi = 0^o$
$e^{j(\pi-\phi)} = e^{j(\pi)} = -1$, hence $A_V = -A_{Vso}$

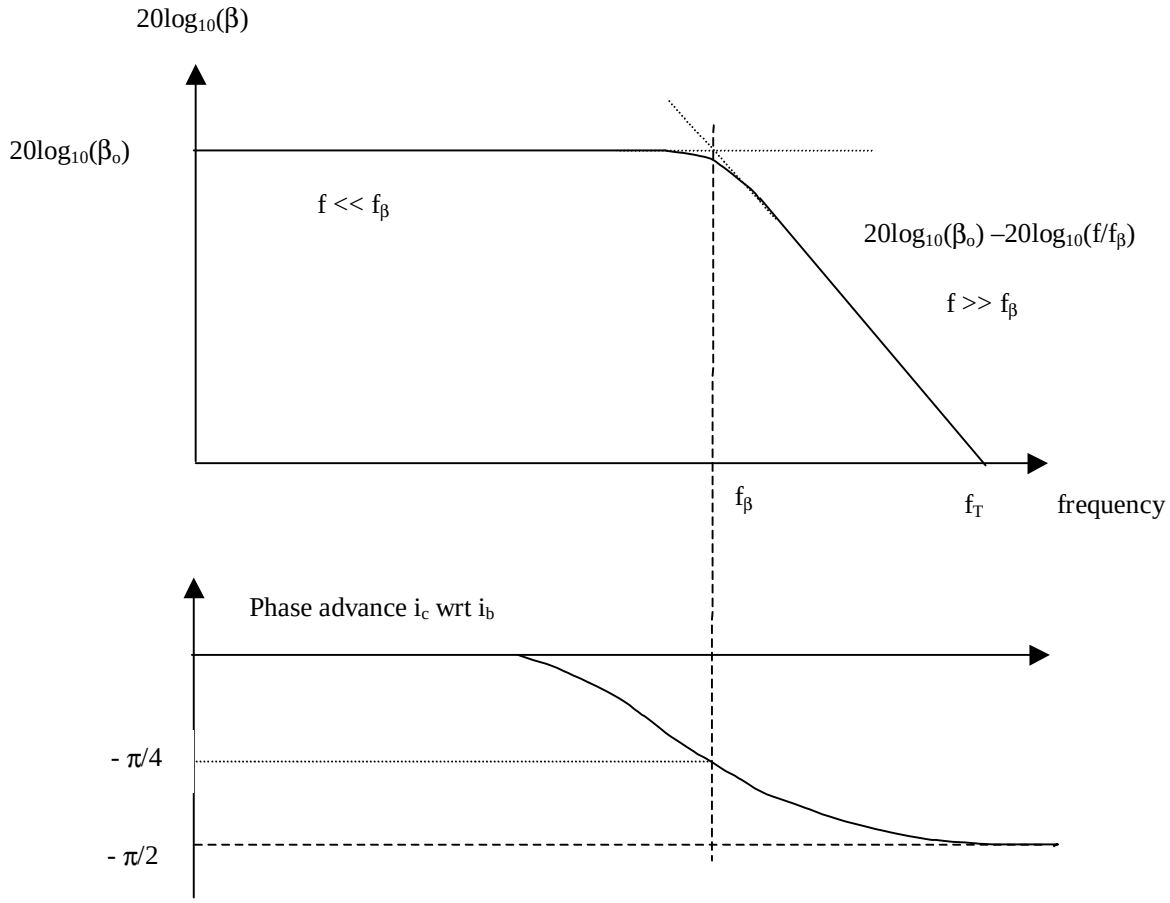
$f = f_H$, $\tan(\phi) = 1$ hence $\phi = 45^o$ $(\pi/4)$
$A_{Vs} = A_{Vso}/\sqrt{2}$
$f = \infty$, $\phi = 90^o$ $(= \pi/2)$ and $A_{Vs} \rightarrow 0$ as required.

With reference to the Bode plot:



Current gain

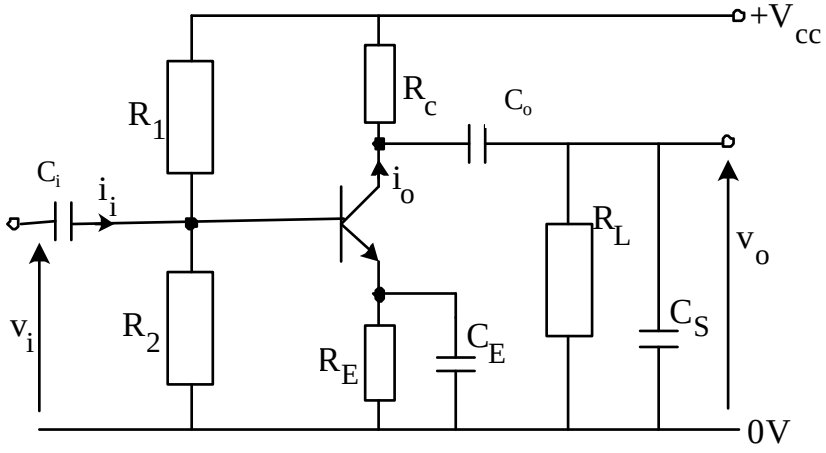
Similar analysis but note that $i_c = - i_o$, so that for low frequencies, i_c is in phase ($\phi = 0$) with i_b and advances 90^o at high frequencies, as shown below. Applying the analysis outlined above to current *gain* (i_o/i_i), would give the same phase response as for voltage gain.



Design Example

Refer to the CE amplifier design covered in part 2 (see slides on vital). Design the amplifier to have a lower cut-off frequency of 100 Hz (recall $I_C = 0.4$ mA).

There are three capacitors in the circuit. Which one should we chose to set the lower frequency cut-off? The answer is we should chose C_E as C_i and C_o are present to block the DC current only. Also, it turns out that C_E is the most important and largest!



Method: consider the effect of each capacitor in turn, shorting out the others.

C_i: The input circuit comprises an RC circuit set by C_i and r_{be} (if we assume that $R_1//R_2 >> r_{be}$.

So $\frac{v_{be}}{v_i} = \frac{r_{be}}{r_{be} + \frac{1}{j\omega \times C_i}} = \frac{1}{1 + \frac{1}{j\omega \times r_{be} \times C_i}}$

Take the magnitude:

$$\left|\frac{v_{be}}{v_i}\right| = \frac{1}{\left[1 + \left(\frac{1}{\omega \times r_{be} \times C_i}\right)^2\right]^{1/2}}$$

This term falls to $1/\sqrt{2}$, when $\omega \times C_i \times r_{be} = 1$

That is, $C_i = \frac{1}{2 \times \pi \times 100 \times r_{be}}$

(for 100 Hz cut-off)

C_o: The output circuit comprises an RC circuit set by C_o and (R_C + R_L) (*Draw the equivalent circuit to show this – you'll need to convert the current source into a voltage source – call it v_o'.*

$$\frac{v_o}{v_o'} = \frac{R_L}{R_L + R_C + \frac{1}{j\omega \times C_o}}$$

So

$$= \frac{R_L}{R_L + R_C} \frac{1}{1 + \frac{1}{j\omega \times (R_L + R_C) \times C_i}}$$

Take the magnitude:

$$\left|\frac{v_o}{v_o'}\right| = \frac{R_L}{R_L + R_C} \frac{1}{\left[1 + \left(\frac{1}{\omega \times (R_L + R_C) \times C_i}\right)^2\right]^{1/2}}$$

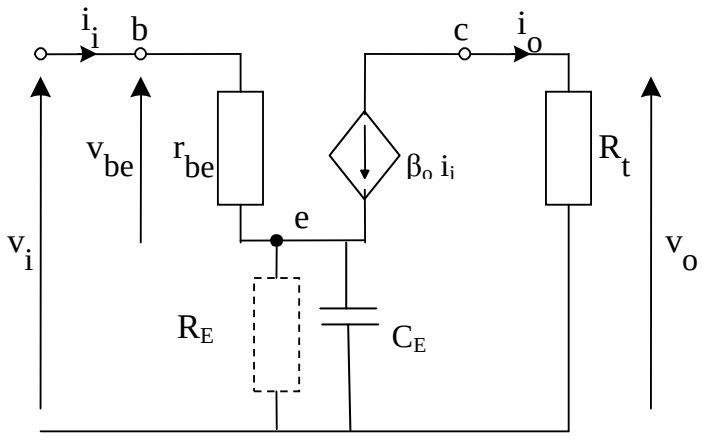
Term falls to $1/\sqrt{2}$, when $\omega \times (R_L + R_C) \times C_o = 1$

That is, $C_o = \frac{1}{2 \times \pi \times 100 \times (R_L + R_C)}$

(for 100 Hz cut-off)

Don't want these capacitors to influence the cut-off, so multiply the values by x 10 (say)

C_E: To keep it simple, assume that the impedance of C_E , Z_{CE} << R_E at the cut-off frequency. The equivalent circuit is shown opposite.



$$v_i = i_i r_{be} + (1 + \beta_o) \times i_i \times \frac{1}{j\omega C_E}$$

So

$$i_i = \frac{v_i}{r_{be} + \frac{1 + \beta_o}{j\omega \times C_E}}$$

Now, $v_o = -\beta_o i_i R_t$

Therefore the voltage gain is,

$$\frac{v_o}{v_i} = -\frac{\beta_o R_t}{r_{be} + \frac{1 + \beta_o}{j\omega \times C_E}} \longrightarrow \frac{v_o}{v_i} = -\frac{\beta_o R_t / r_{be}}{1 + \frac{1 + \beta_o}{j\omega \times r_{be} \times C_E}}$$

The magnitude of the gain will drop by 1/√2, when $\frac{1+\beta_o}{\omega \times r_{be} \times C_E} = 1$

That is, when $C_E = \frac{1+\beta_o}{2 \times \pi \times f_o \times r_{be}}$ where f_o is the lower cut-off point.

Worked Example

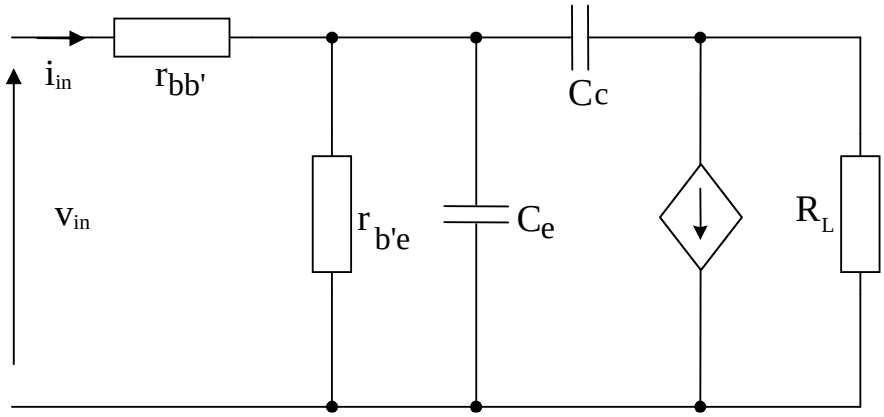
A. For the common emitter amplifier equivalent circuit shown, apply Miller's Theorem and hence show that the input impedance is given by:

$$Z_{in} = \frac{v_{in}}{i_{in}} = (r_{b'e} + r_{bb'}) \frac{1 + j\frac{f}{f_1}}{1 + j\frac{f}{f_2}}$$

where $f_1 = \frac{1}{2\pi RC}$

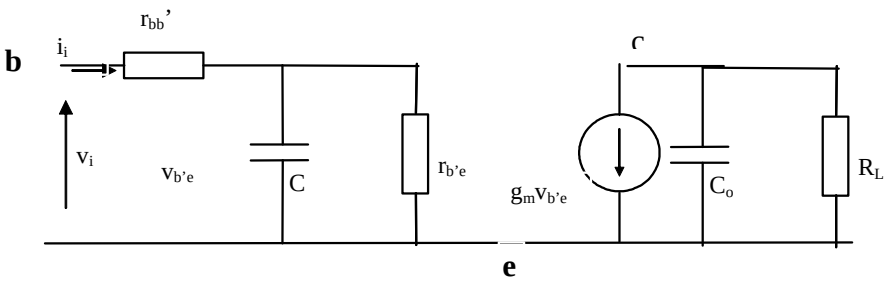
$$f_2 = \frac{1}{2\pi r_{b'e} C}$$

with $R = r_{b'e} // r_{bb'}$, $C = C_e + A_{Vo} C_c$, and A_{Vo} is the mid-frequency voltage gain.



Solution

Apply M. Thm. to give



where $C \approx C_e + |g_m R_L| \; C_c$

$$v_i = i_i\left(r_{bb'} + \frac{r_{b'e}/j\omega C}{r_{b'e}+1/j\omega C}\right) \quad \text{so} \quad \frac{v_i}{i_i} = r_{bb'} + \frac{r_{b'e}}{1+j\omega r_{b'e}C}$$

$$\frac{v_i}{i_i} = \frac{r_{bb'} + r_{b'e} + j\omega r_{b'e}r_{bb'}C}{1+j\omega r_{b'e}C}$$

hence $\frac{v_i}{i_i} = (r_{bb'} + r_{b'e})\frac{1+j\omega RC}{1+j\omega r_{b'e}C}$

write in standard form: $Z_{in} = \frac{v_{in}}{i_{in}} = (r_{b'e} + r_{bb'})\frac{1+j\frac{f}{f_1}}{1+j\frac{f}{f_2}}$

as required.

Sketch should show 1st order roll-off from ($r_{bb'} + r_{b'e}$) to $r_{bb'}$ with poles at f_1, f_2.

B. Show that Z_{in} reduces to:

$Z_{in} \sim (r_{b'e} + r_{bb'})$ at low frequencies such that $f << f_1, f_2$

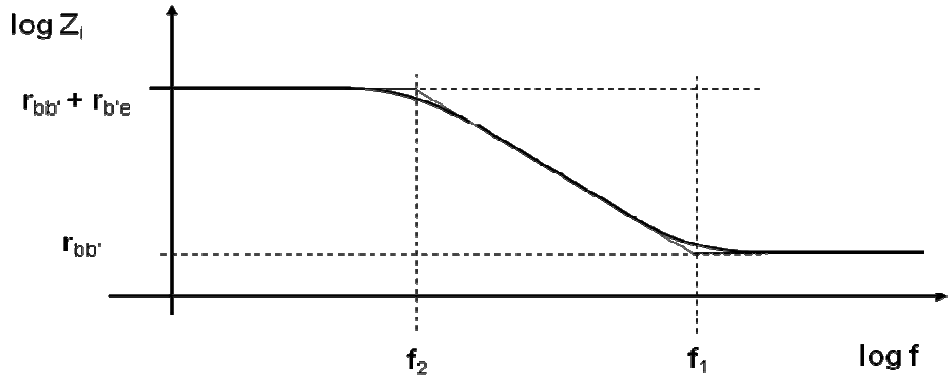
$Z_{in} \sim r_{bb'}$ at high frequencies such that $f >> f_1, f_2$

If $f << f_1, f_2$, then $Z_{in} \sim (r_{bb'} + r_{b'e})$

If $f >> f_1, f_2$ $Z_{in} \sim (r_{bb'} + r_{b'e})\frac{R}{r_{b'e}}$ = $Z_{in} \sim (r_{bb'} + r_{b'e})\frac{r_{b'e}r_{bb'}}{r_{b'e}(r_{bb'} + r_{b'e})}$

$Z_{in} = r_{bb'}$

Sketch Z_{in} (f). labelling your diagram appropriately, for the case of $\beta_o = 200$, $r_{bb'} = 100\Omega$, a bias current of 1mA, load resistor of 2kΩ, $C_e = 10$pF and $C_c = 2$pF.



Magnitude of $A_{vo} = g_m R_L$ = 400m x 2k = 80

So $C = C_e + A_{Vo}C_c = 10p + 80x2p$ = 170pF,

$r_{b'e} = \frac{200}{40\times 1m}$ = 5000R

$$R = \frac{5000 \times 100}{5000 + 100} = 98\text{R} \quad (R = r_{b'e} // r_{bb'})$$

$$f_1 = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 98 \times 170p} = 9.6\text{MHz} \qquad f_2 = \frac{1}{2\pi r_{b'e} C} = \frac{1}{2 \times \pi \times 5k \times 170p} = 1.8\text{MHz}$$

How do you expect Z_{in}, f_1 and f_2 to vary with bias current? Explain your reasoning.

Considering f_2.
If I_C increases, g_m increases and A_{V0} (= $g_m R_L$) increases in proportion. In this example, C is dominated by $A_{V0}C_C$ (Miller effect) so C also increases in proportion to I_C. However, $r_{b'e}$ varies inversely with I_C because $r_{b'e} = \beta_o / g_m$. **Hence f_2 remains constant**, independent of I_C, provided β_o stays constant (actually β_o will eventually decrease due to series resistance and the Kirk Effect –not studied here).

Considering f_1
At I_C = 10mA (say), R (=$r_{b'e}$ // $r_{bb'}$) is still determined mainly by $r_{bb'}$ but decreases as I_C increases above 10mA. Eventually R becomes dominated by $r_{b'e}$. At this point, $f_1 \approx f_2$ and f_1 will also be constant until β_o starts to fall. When this happens, both f_1 and f_2 rise.
If I_C were to decrease below 10mA, R becomes increasingly dominated by $r_{bb'}$ and so remains constant. The product RC then decreases as I_C decreases and f_1 rises, The current would need to fall to very low values so that $A_V \rightarrow 1$ for the value of C to become constant at $C_{b'e}$+ C_C at which point f_1 becomes constant.

Exercise

1. The bandwidth for voltage gain of a single common-emitter amplifier stage is required to be 1.5 MHz with a quiescent current of 5 mA and a total load, R_L = 1 kΩ. The transistor parameters are β_o = 100, $r_{bb'}$ = 20 Ω, $C_{b'c}$ = 2 pF and f_T = 200 MHz. From this information deduce the values of g_m, $r_{b'e}$, $C_{b'e}$ and f_β. Find the value of the source resistance to give the required bandwidth and the mid-frequency voltage gain v_o/v_s. Derive any formulae you may use.
   (Ans: 200 mA/V, 500 Ω, 157 pF, 2MHz, 280 Ω, 125)

   If there is a stray capacitance of 0.01 μF in parallel with R_L calculate the new bandwidth, neglecting the input time constant.

2. Recalulate the value of C_i from the design section above, by taking into account the bias resistors. Use the values from the design exercise in Part 2 (see slides on vital).