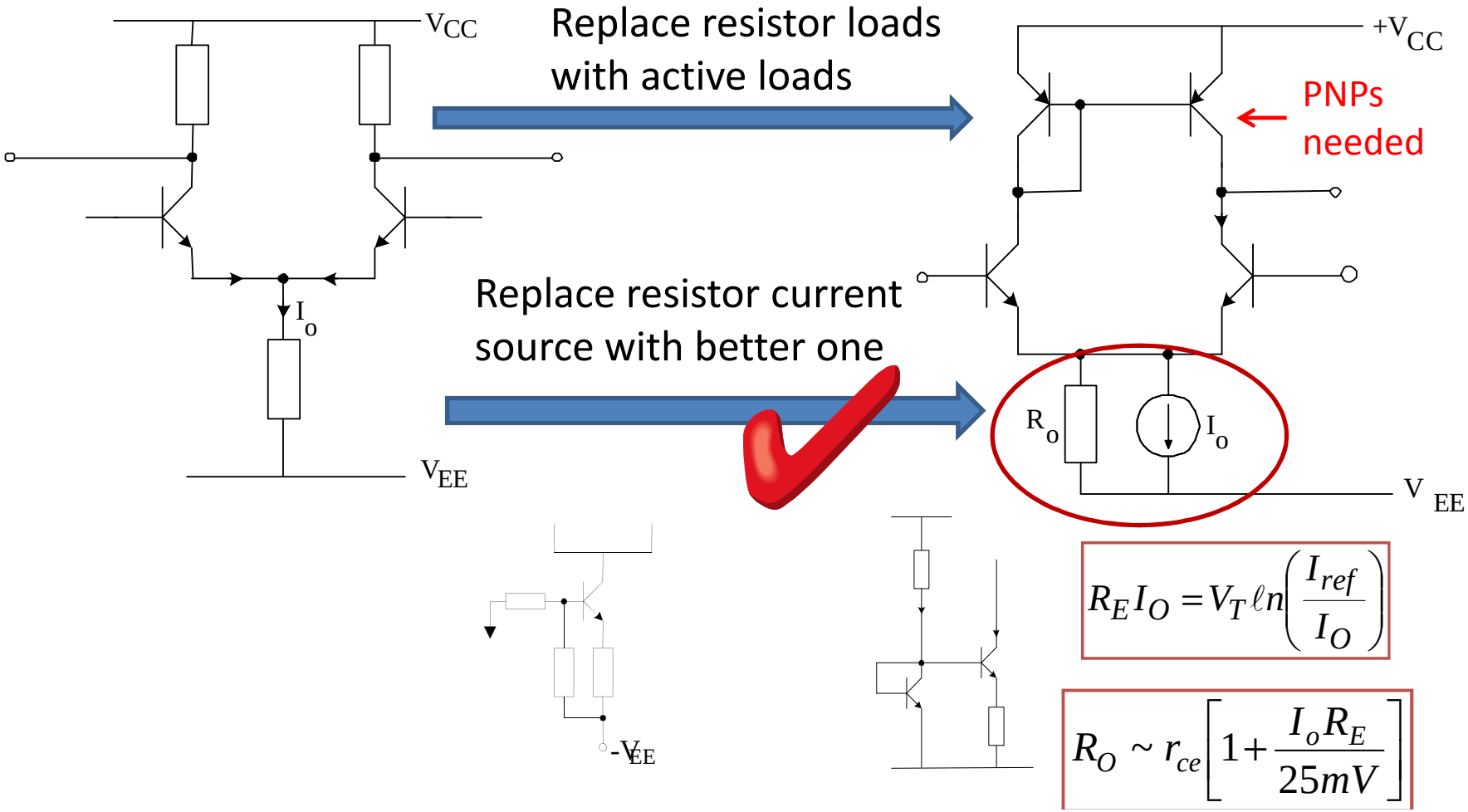
Electronic circuits and systems
ELEC271

Part 5
Active loads

How to greatly increase the differential gain

Optimising the Diff. Amp

- Use of a current source bias **greatly reduces the common-mode gain**
- now address the problem of achieving a large effective load resistor, R_C for high gain without upsetting d.c. conditions



$$R_E I_O = V_T \ell n\left(\frac{I_{ref}}{I_O}\right)$$

$$R_O \sim r_{ce}\left[1+\frac{I_o R_E}{25mV}\right]$$

How it works

d.c. operation: inputs grounded

assume $I_B \sim 0$

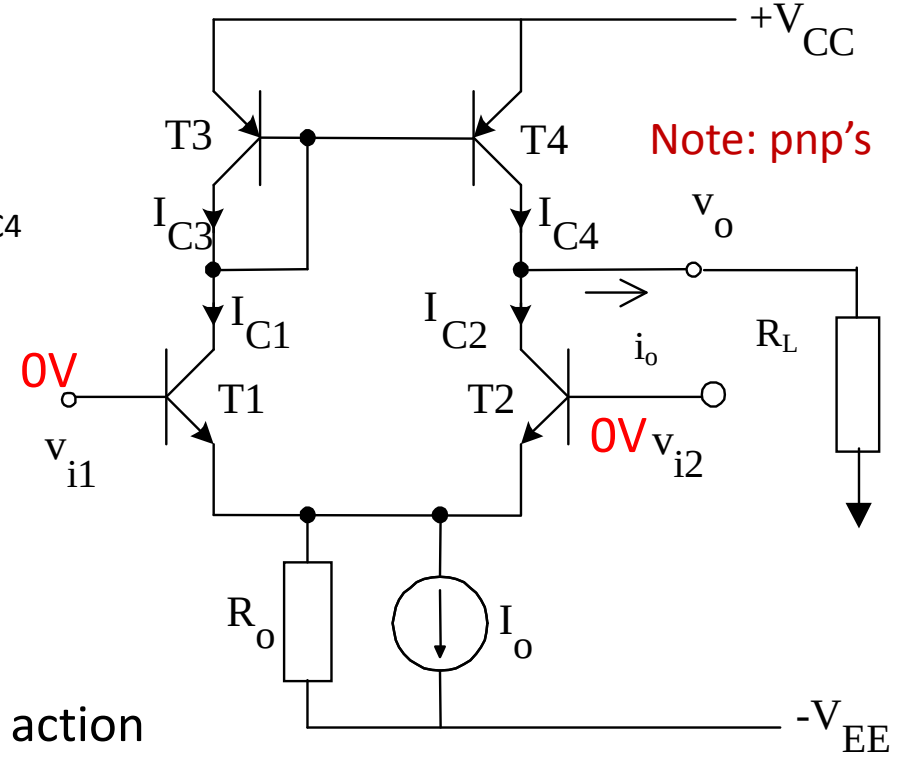
CM action in T_3 and T_4 means that $I_{C3} = I_{C4}$

$I_{C3} \approx I_{C1}$

$I_{C1} = I_{C2} \approx Io/2.$

Hence $i_o = 0$ (as $I_{C4} = I_{C2}$)

No output!



AC Operation

Consider vi1 ↑, vi2↓

I_{C1} ($\approx I_{C3}$) will rise and hence I_{C4} , by CM action

I_{C2} will fall

Hence, KCL gives

$$i_o = I_{C4} - I_{C2}$$
$$= I_{C1} - I_{C2}$$

$$g_m v_{i1} - g_m v_{i2} = g_m (v_{i1} - v_{i2}) = g_m v_{id}$$

(as '$I_C = g_m v_{be}$')

the configuration is thus best thought of as a ***transconductance*** amplifier:

$$G_m = \frac{i_o}{v_{id}}$$

Voltage gain

recall that voltage gain of a diff. amp. with resistors R_C was

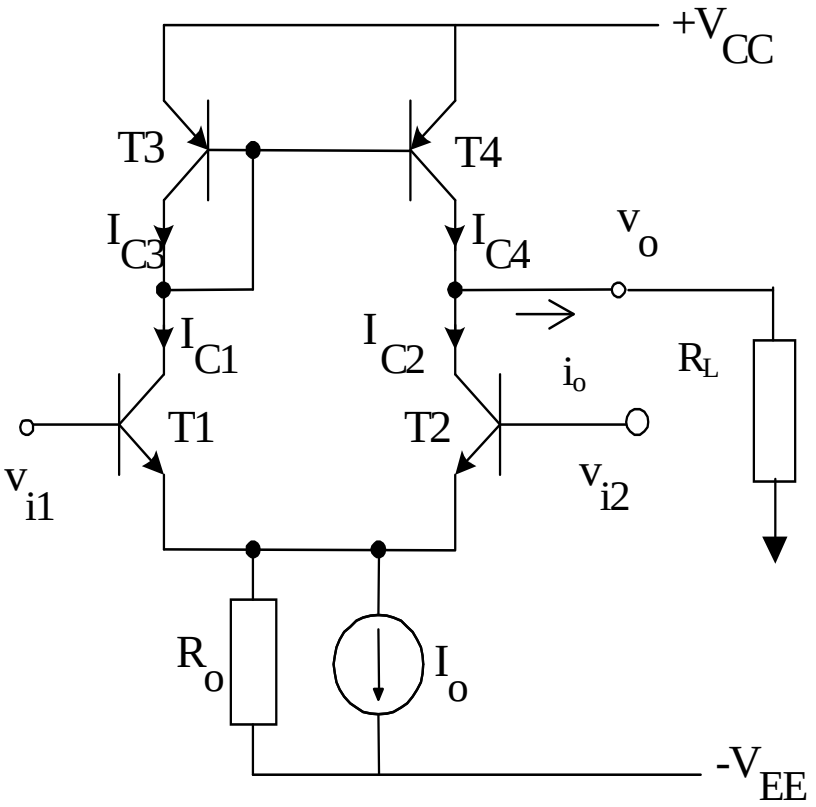
$$A_{Vd} \sim g_m R_C$$

The 'R_C' is now the *dynamic* resistance 'looking up' into the collectors of the current mirror and T2.
We might 'guess' that the voltage gain Now becomes

$$A_{Vd} = g_m (r_{ce4} // r_{ce2} // R_L)$$

$$\sim g_m (r_{ce4} // r_{ce2})$$

if R_L is very big (infinity say)



Voltage gain is thus large without the need for a very large (area consuming) discrete resistor !

Exercise

Show that A_{Vd} can be expressed in terms of the Early voltages (V_{An}, V_{Ap}):
[recall that $g_m = I_C/V_T$ and $r_{ce} = V_A/I_C$]

$$A_{Vd} = \frac{1}{V_T}\frac{V_{An}V_{Ap}}{V_{An}+V_{Ap}}$$

Solution

The output resistance of $T_2 = V_{An}/I_C$

The output resistance of $T_4 = V_{Ap}/I_C$

Without R_L we have

$$A_{Vd} = g_m\left(r_{ce2} \,//\, r_{ce4}\right) = \left(\frac{I_C}{V_T}\right)\frac{\frac{V_{An}}{I_C}\times\frac{V_{Ap}}{I_C}}{\frac{V_{An}}{I_C}+\frac{V_{Ap}}{I_C}}$$

$$\frac{r_{ce2}r_{ce4}}{r_{ce2}+r_{ce4}}$$

$$\Rightarrow \quad A_{Vd} = \frac{1}{V_T}\frac{V_{An}\times V_{Ap}}{V_{An}+V_{Ap}}$$

as required

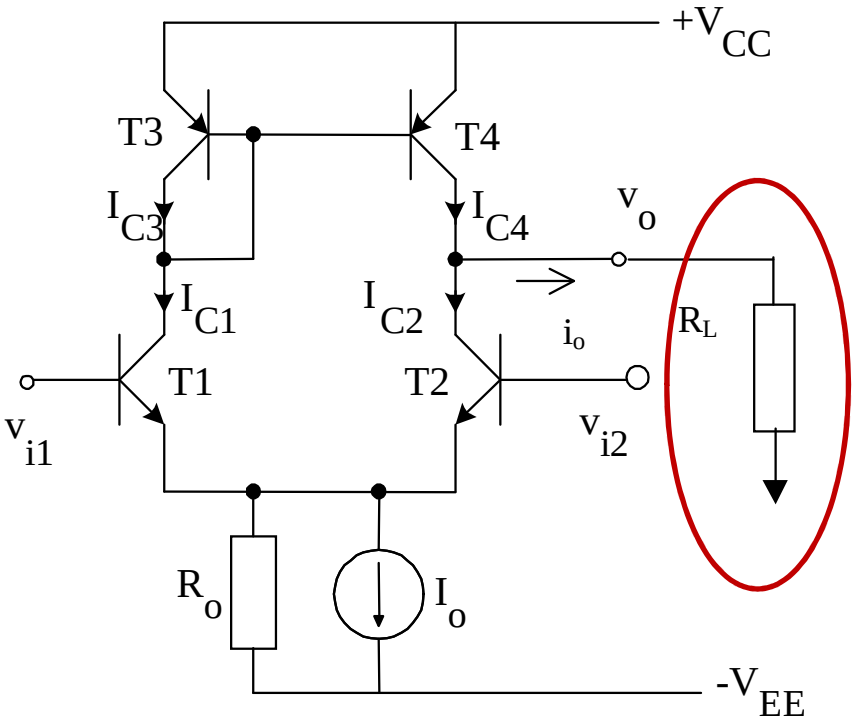
Substitute values: V_{An} ~ 74 V, V_{Ap} ~ 120 V, gives A_{Vd} = 1,830

Points to note 1 – loading effects

We have assumed above that the amplifier is driving an infinitely large resistance load R_L. In reality, the **total load resistance** would be

$R_L // r_{ce2} // r_{ce4} \rightarrow R_L$ (if $R_L << r_{ce}$)

high gain can therefore be severely reduced by the loading of the following stage!



Solution?

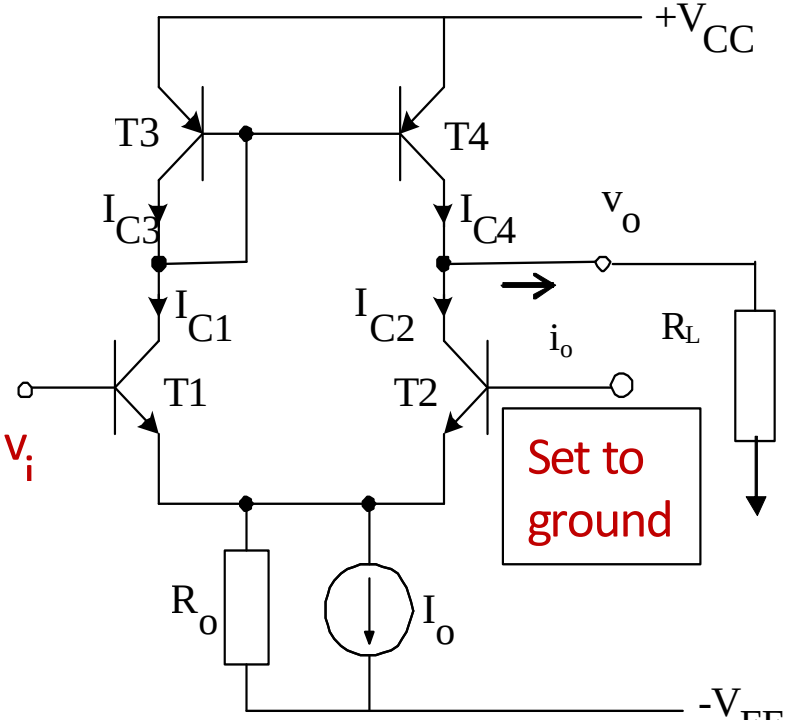
ensure a high resistance for the following stage by making it an emitter follower (high input resistance) and thus high voltage gain can be obtained.

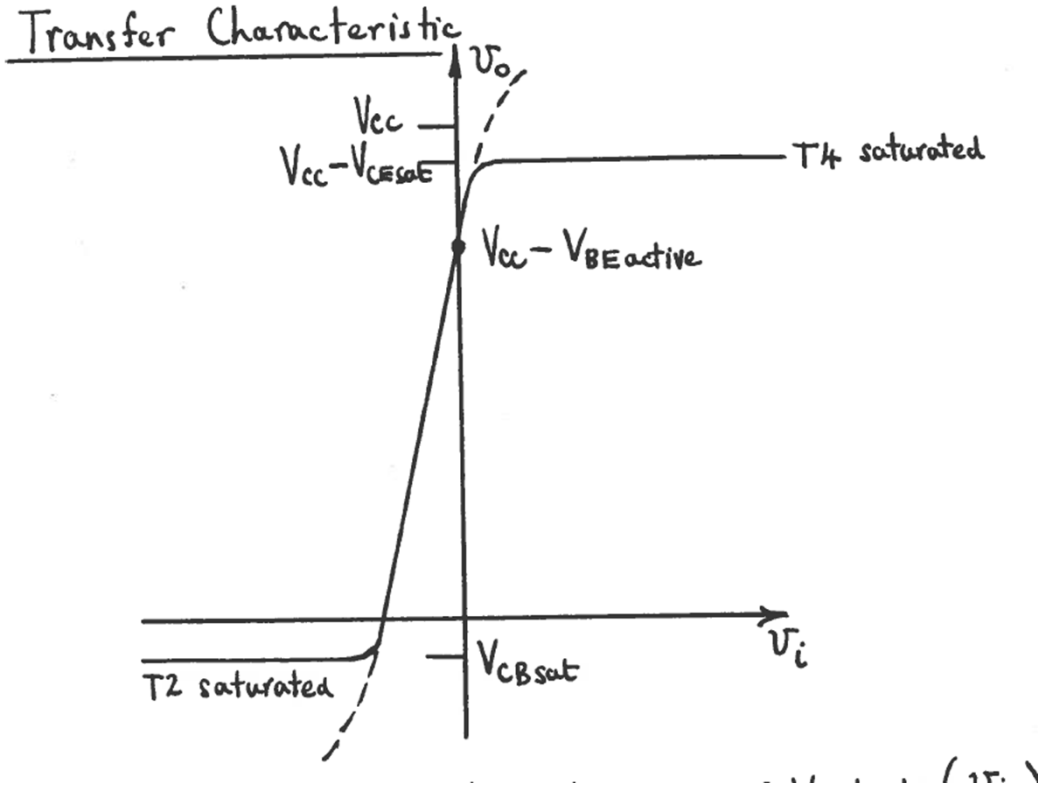
Remember this when doing Expt.5…

Points to note 2 – voltage swing

The d.c. output voltage is a 'V_{BE}' drop less than the supply rail V_{CC}. Thus d.c. output at v_i = 0 V is (~ V_{CC} – 0.7 V) → Implies only a very small (a.c.) voltage swing at v_o.!

- However, recall that in the main purpose of achieving very high gain amplifiers is to 'trade' the gain for feedback to stabilise and enhance the overall performance .
- Thus a large amount of negative feedback is generally used and this tends to make vin1 ~ vin2. **[See later notes on feedback & Recall the 'Golden rules' of op-amps…]**





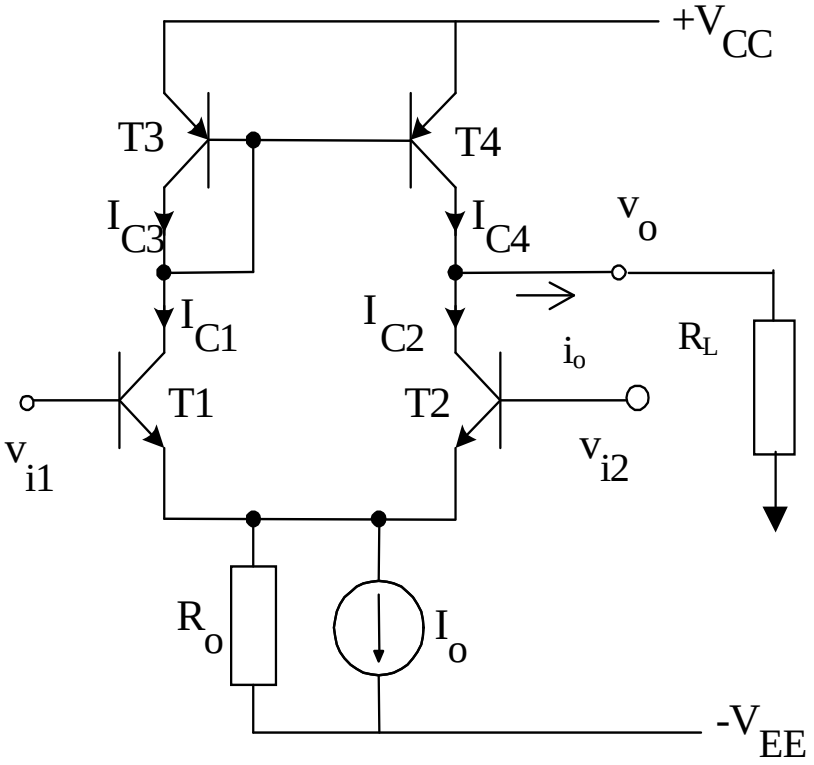
Points to note – 3: advantages

• Both high transconductance (gain) and large input resistance are required and this constitutes a design trade-off.

(*See earlier notes for ways of increasing input resistance*.)

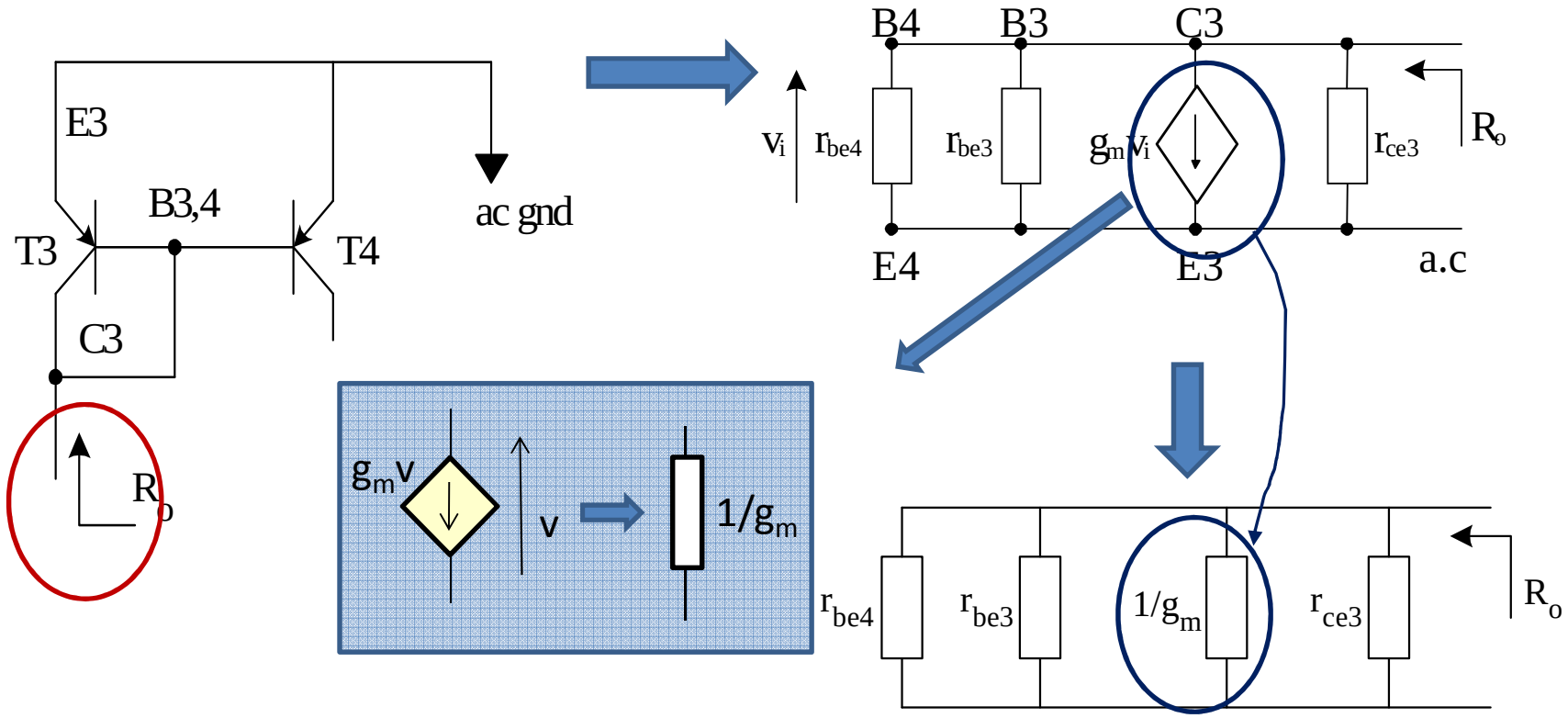
• **greatly improved CMRR** because of the large dynamic resistance of the current source I_o, R_O

• the current mirror effectively provides the 'subtraction' of the outputs so the output can be taken **single ended.**



a.c. analysis – more rigorous analysis

- Now derive the expression for gain again, by considering the a.c. equivalent circuit.
- **Need an equivalent circuit for the current mirror load: what 'resistance' is seen looking up into the current mirror?**



The approximation opposite can again be made

$$R_o = r_{be4} // r_{be3} // \frac{1}{g_m} // r_{ce3} \approx \frac{1}{g_m}$$

(see Widlar CM notes)

Ac equivalent circuit for A_{Vd} (ignore r_{ce})

Note that the voltage drop across the $1/g_m$ load is

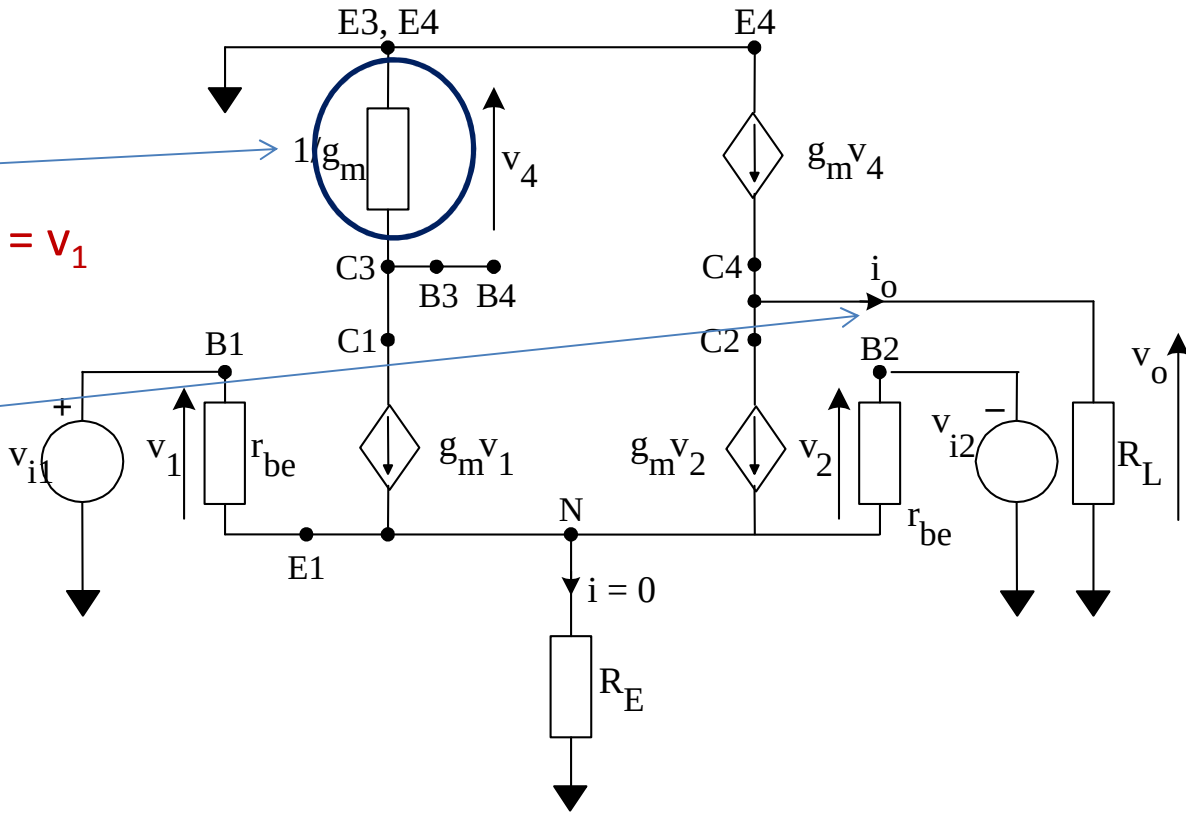
$v_4 = (g_m v_1) \times 1/g_m = v_1$

So $v_4 = v_1$

Then write:

$i_o = g_m (v_4 - v_2)$ (KCL)
$= g_m (v_1 - v_2)$
$= g_m v_{id}$;

That is, $i_o = g_m \times v_{id}$
So $v_o = i_o R_L = (g_m v_{id}) R_L$



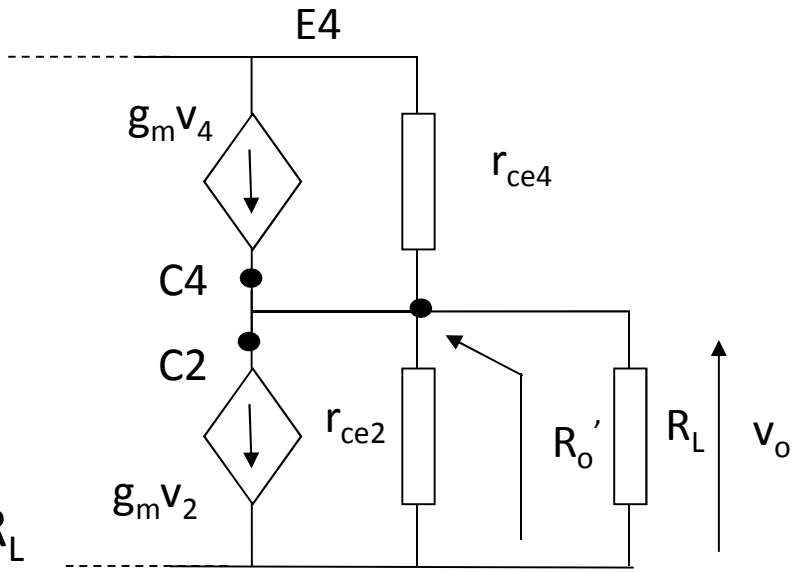
$\therefore A_{vd} = g_m \times R_L$ (single ended voltage gain)

$$\left.\begin{aligned} v_{i1} &= i_i r_{be} \\ v_{i2} &= -i_i r_{be} \end{aligned}\right\} \quad v_{id} = i_i r_{be} - (-i_i r_{be})$$

and **Diff. input resistance**, $R_{id} = \dfrac{v_{id}}{i_i} = 2 \times r_{be}$

Include the effect of r_{ce}'s

v_2 and v_4 are set to zero (by convention) for finding output resistance, the a.c. load is by inspection,



$R_o' = r_{ce4} // r_{ce2}$ and $R_o = r_{ce4} // r_{ce2} // R_L$

So **without** R_L $A_{Vd} = g_m (r_{ce4} // r_{ce2})$ - VERY HIGH
But **with** R_L, $A_{Vd} = g_m (r_{ce4} // r_{ce2} // R_L)$

if $R_L << r_{ce4} // r_{ce2}$, then $A_{Vd} \sim g_m R_L$ - VOLTAGE GAIN MUCH REDUCED if R_L small!

→ ensure that the diff. amp. is not fed into a low impedance stage!

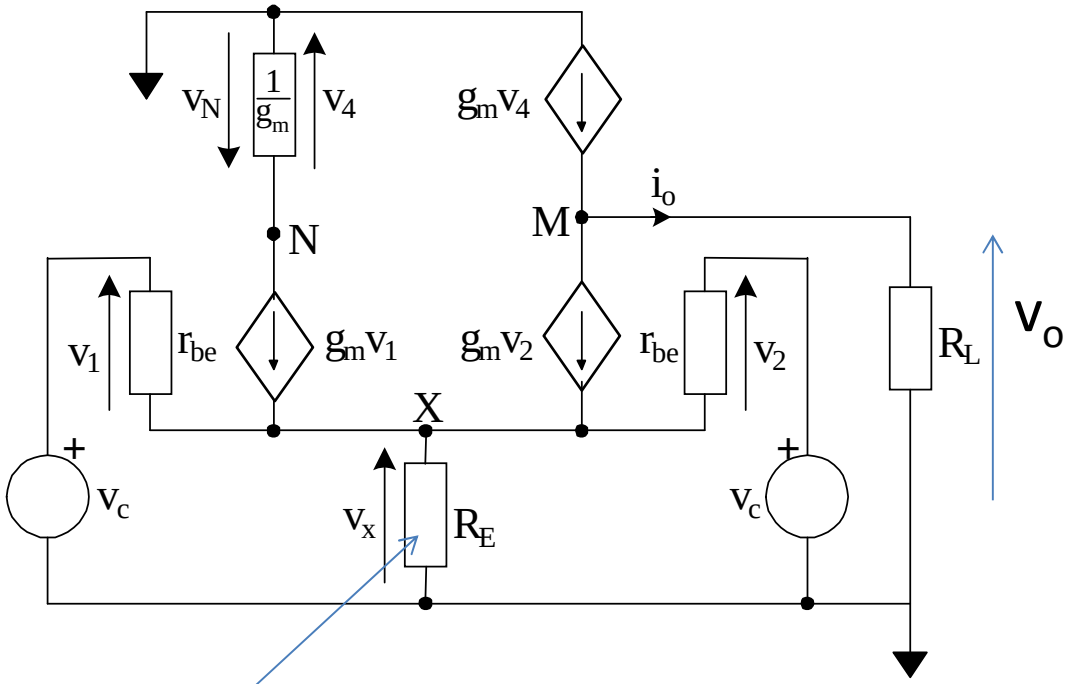
Common Mode Gain

Currents in left and right-hand sides of the circuit are the same (by CM action), so

$i_o = 0$

$v_o = 0$

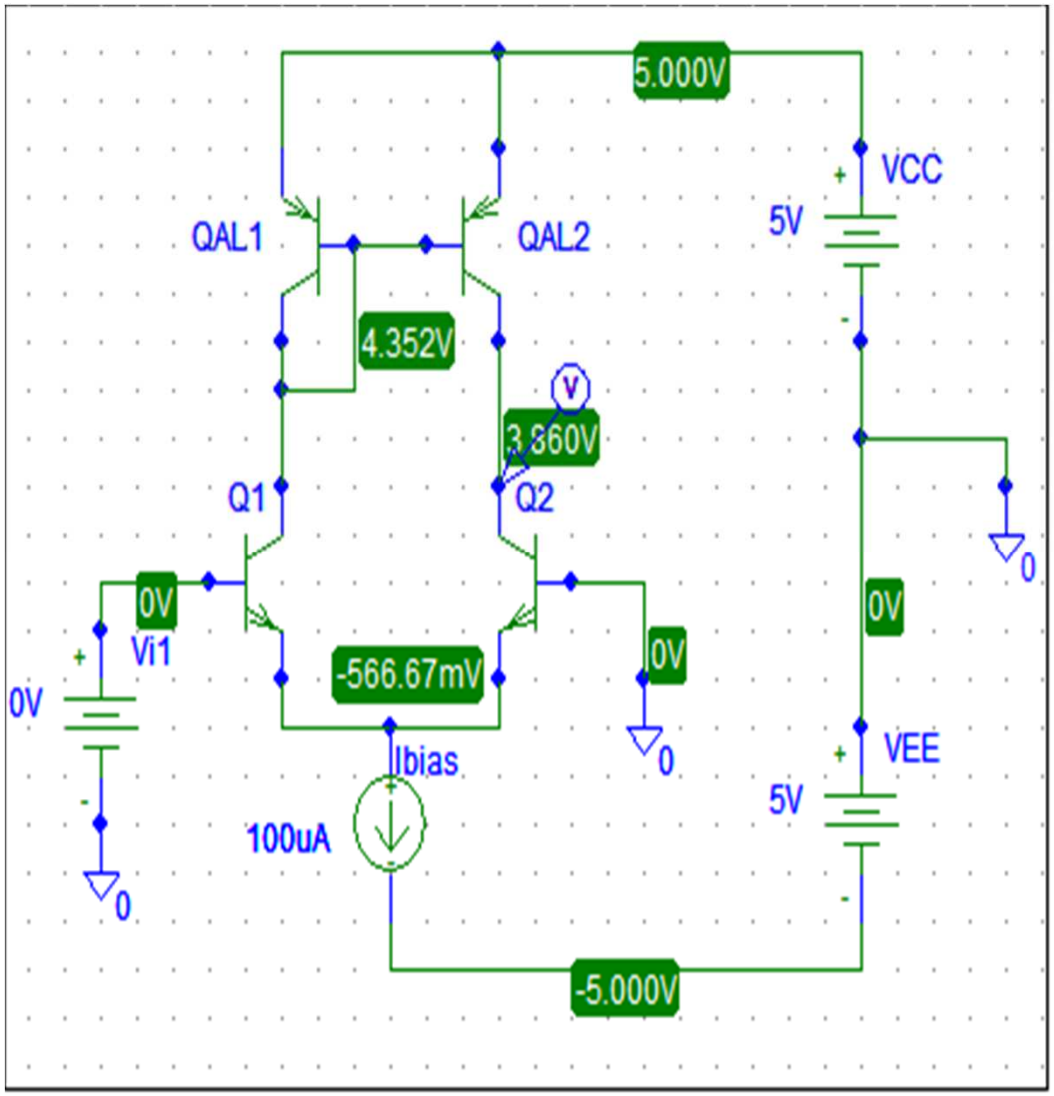
$\mathbf{A_{vc} = 0}$



- **Ideally, the common-mode gain is zero! - if the current source bias is IDEAL**
- **In reality, CM is small: $A_{Vc} \sim 1/R_E$ (circuit above)**
- **or <u>very small</u> $A_{vc} \sim 1/R_O$ for the case of an active current source**

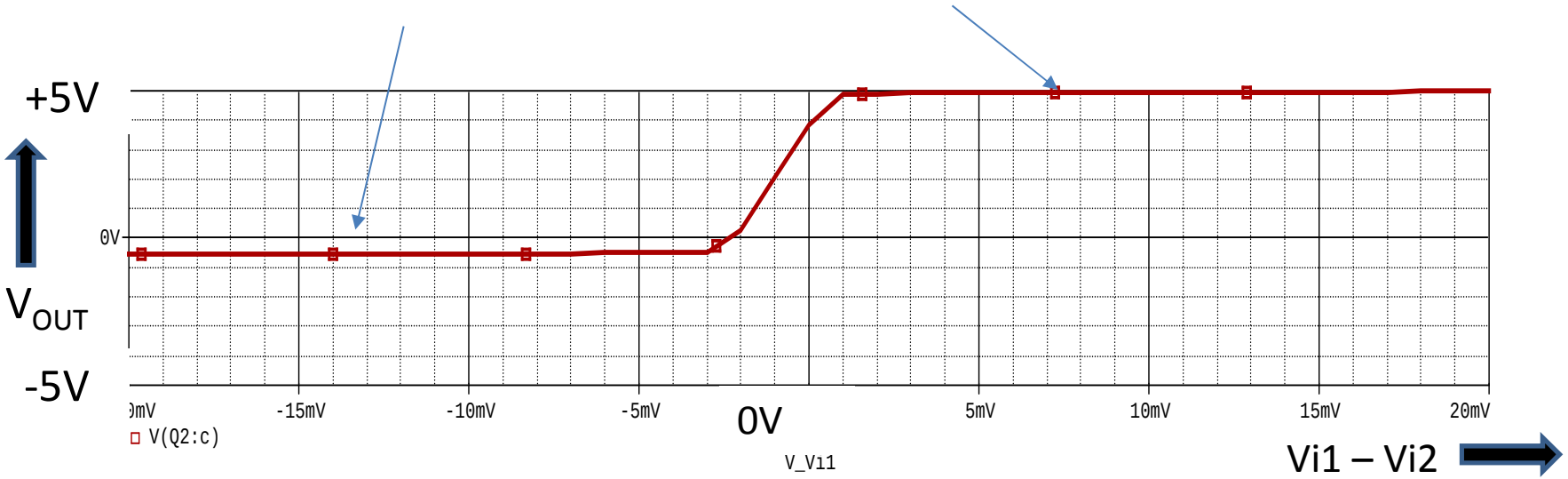
PSPICE simulation

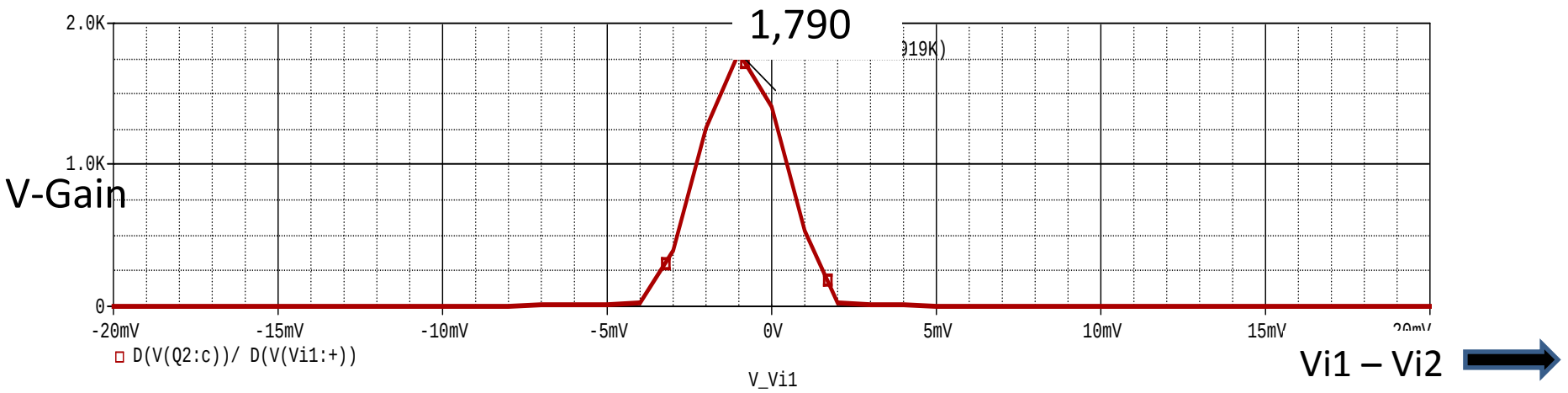
V_{BE} (Q1, 2) ~ 0.6 V



Transfer characteristic and gain

In these regions, current ‘hogged’ by just one transistor so output is pinned





Check

- Theory for gain, Early voltages of pnp and npn

V_A (npn) 2N222 = 74 V

V_A(pnp) 2N907A =116 V

$$A_V = \frac{1}{V_T}\frac{V_{An}V_{Ap}}{V_{An}+V_{Ap}}$$

$$A_V = \frac{1}{25mV}\frac{74\times116}{74+116} \quad =1{,}800$$

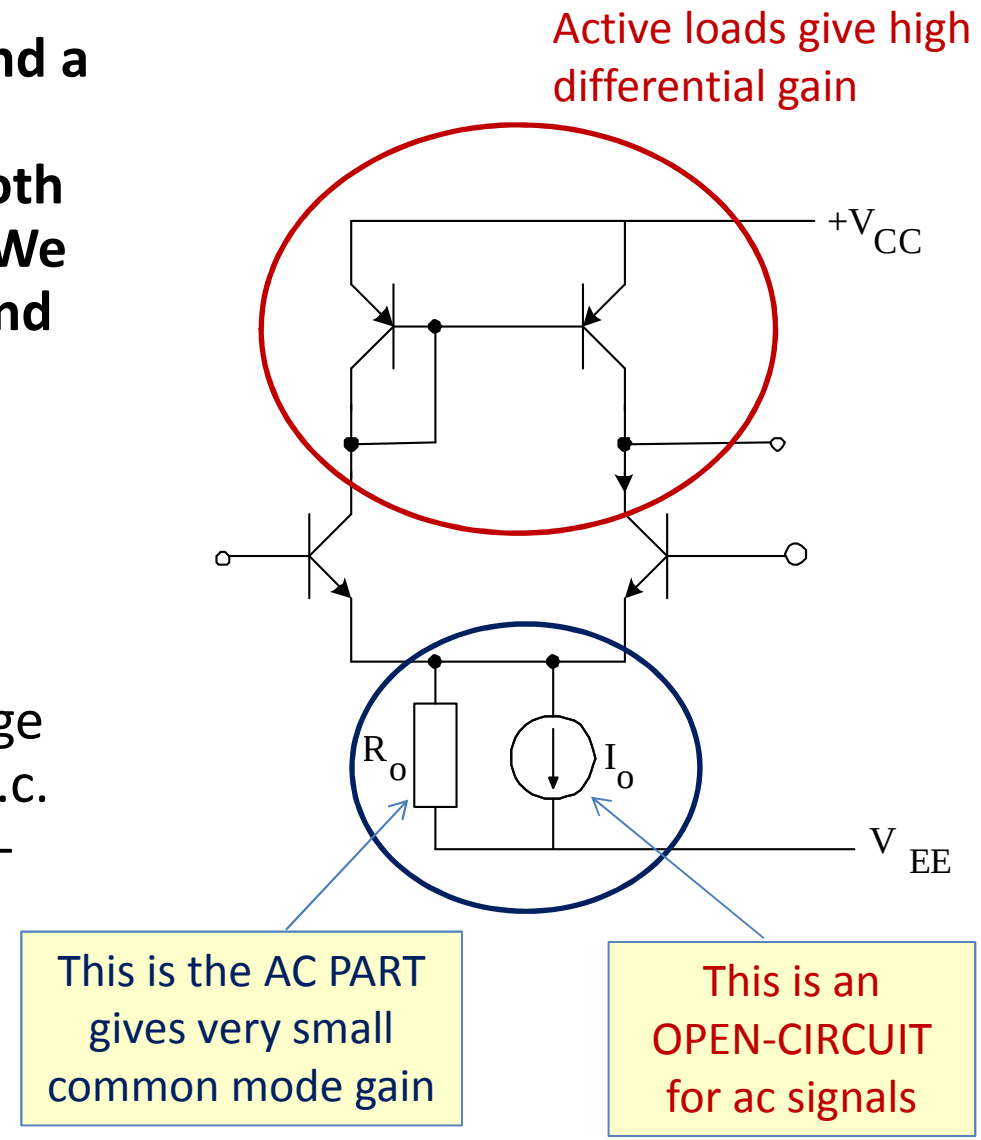
Perfect agreement with simulation

(recall we got a gain of 96 with a resistor load)

Conclusions

- **By the use of active loads and a current source, we have achieved the objective of both high gain and large CMRR. We have 'de-coupled' the a.c. and d.c. roles of the biasing components.**

- We are now in a position to analyse a 'real' operational amplifier using our knowledge of d.c. biasing techniques, a.c. equivalent circuits and multi-stage amplifiers.



MCQ

Use of an active load has the following benefit for the differential amplifier:

a) Increasing the differential gain
b) Increasing the common-mode gain
c) Decreasing the common-mode rejection ratio
d) Decreasing the output resistance

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Use of an active load has the following benefit for the differential amplifier:

a) Increasing the stability
b) Increasing the common-mode gain
c) Decreasing the common-mode rejection ratio
d) Increasing the common-mode rejection ratio

MCQ

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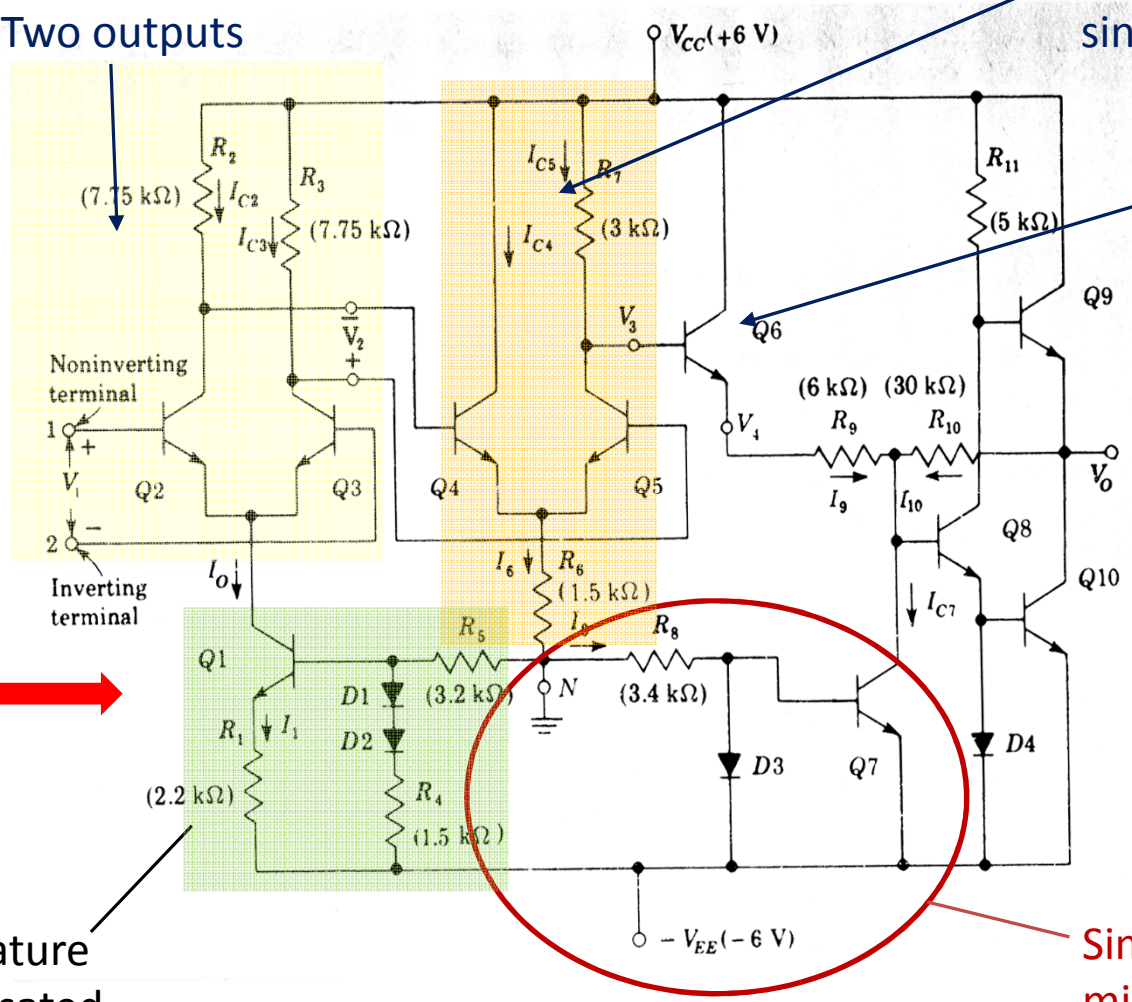
Milestone…

Differential amplifier
Two outputs

Differential amplifier
single output

Emitter-follower to ‘match’ the stages

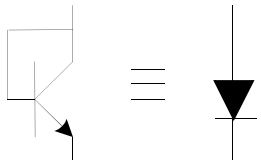


Ensures a good CMRR - Rejects the CM signals

Temperature compensated current source

Simple current mirror

- Identify building blocks
- Perform a d.c. analysis
- Perform an a.c. analysis



End of lecture

- Next lecture, analyse the MC1350 op-amp
  - The circuit is at the back of part 5 notes
  - Some hints are given as to how to tackle the analysis

- Try if before the lecture on Tuesday!

Milestone…

Differential amplifier
Two outputs

Differential amplifier
single output

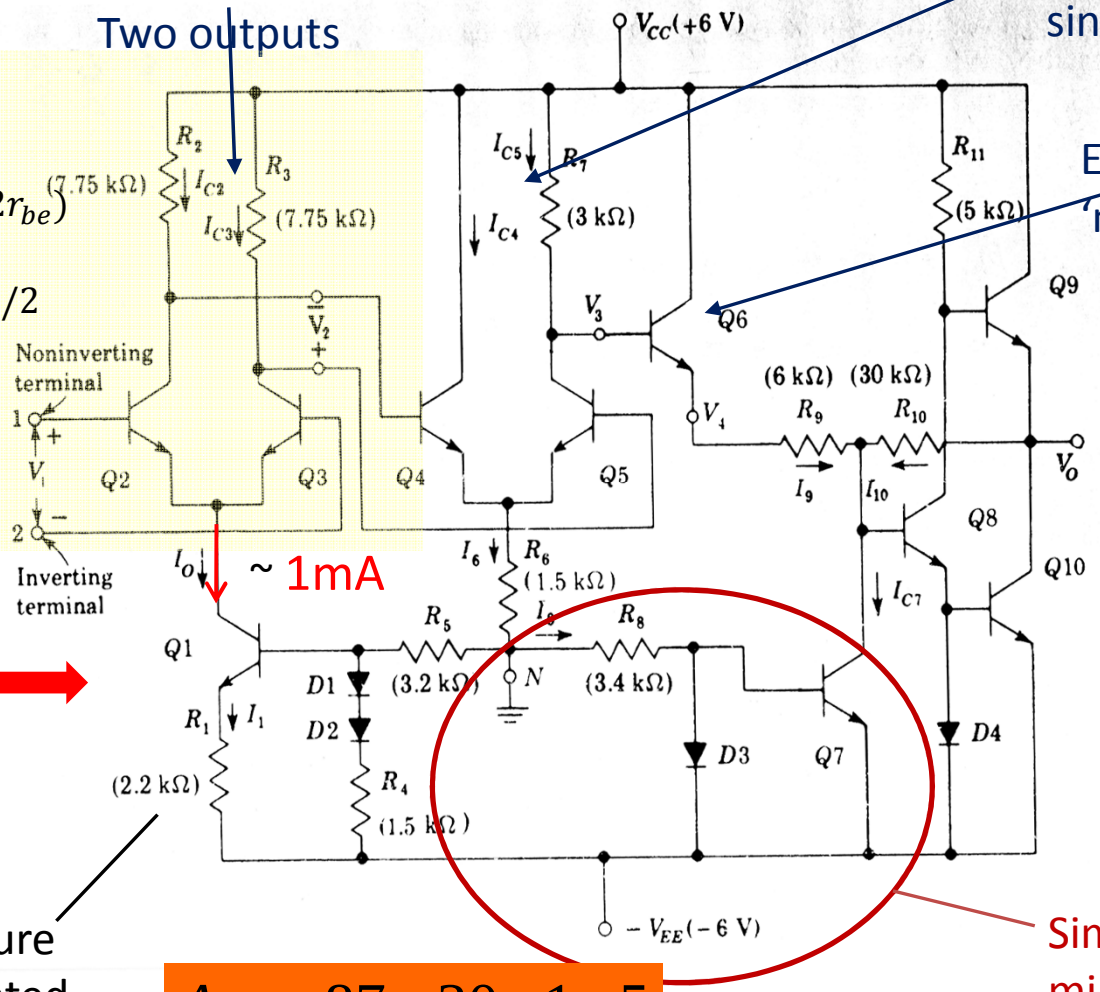
Emitter-follower to ‘match’ the stages

$$A_{Vd} = g_m(R_C \,//\, R_{i2})$$

$$A_{Vd} = 40 \times \frac{1}{2} mA(R_C//2r_{be})$$

$$A_{Vd} = 20mA(7.75k//2 \times 10k)$$

$$A_{Vd} = 87$$



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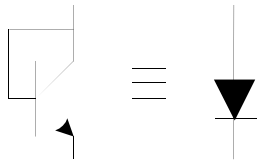

$$A_{Vd} = 87 \times 30 \times 1 \times 5 = 1{,}310$$