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ELEC 271

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UNIVERSITY OF LIVERPOOL

SECOND SEMESTER EXAMINATION REPLACEMENTS 2019/20

ELECTRONIC CIRCUITS AND SYSTEMS

INSTRUCTIONS TO CANDIDATES

The numbers in the right hand margin represent an **approximate guide** to the marks available for that question (or part of a question). Total marks available are 100.

Copying any material from another source, or colluding with any other person in the preparation and production of this work will be considered suspected academic misconduct and will be dealt with according to the University's Academic Integrity Policy.

This is an open-book test.

Answer ALL Questions.
The use of a calculator IS allowed.

Additional Information

Amplifier properties can be found in your notes.

1. a) Draw the mid-frequency, small-signal equivalent circuit for a bipolar transistor, labelling clearly the parameters. Work out values for the parameters, g_m, r_{ce} and r_{be} (the parameters have their usual meaning). The DC collector current is 1 mA; ac current gain, β_o is 100 and the Early voltage, V_A is 100 V. **5**

b) Figure Q1b shows an amplifier circuit where bias resistors are omitted. Identify the amplifier type and hence design it to have a voltage gain of 10. **5**

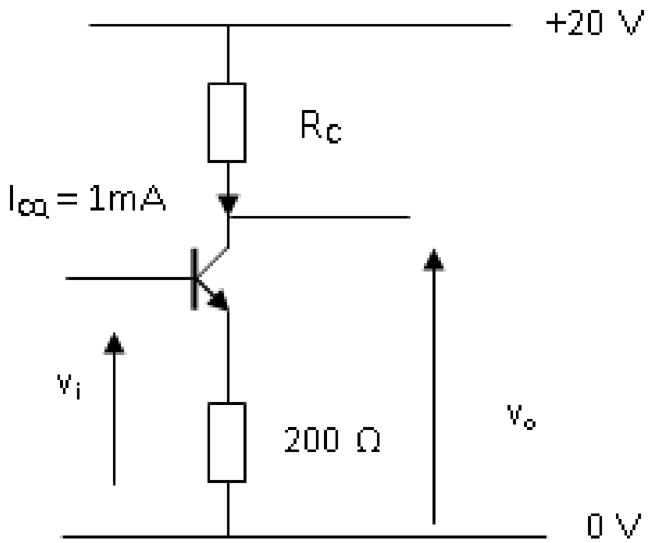

Figure Q1b

Question continues overleaf.

Question continued.

c) Figure Q1c shows an amplifier system. The source has a small internal impedance and the load is a small resistance. Choose a suitable amplifier type to ensure good matching between the source and the load. Hence, sketch a system's diagram with appropriate equivalent circuits for the source (Thevenin or Norton) and generic amplifier type. **5**

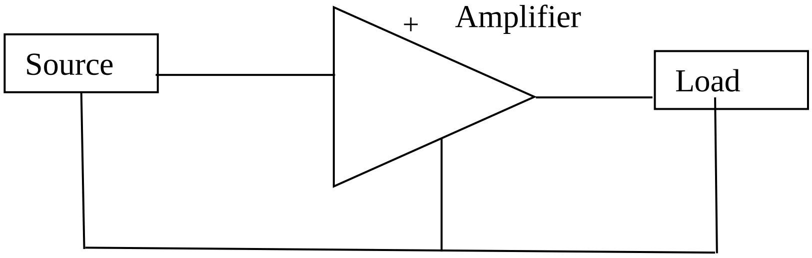

Figure Q1c

d) Work out the dc voltage levels of the circuit of Fig. Q1d and hence find values for $I_C(Q_1)$, $I_C(Q_2)$, I_{R1}, I_{R2}. **5**

Assume that $V_{BE}\,(on)$ = 0.6 V and dc base currents can be assumed negligible.

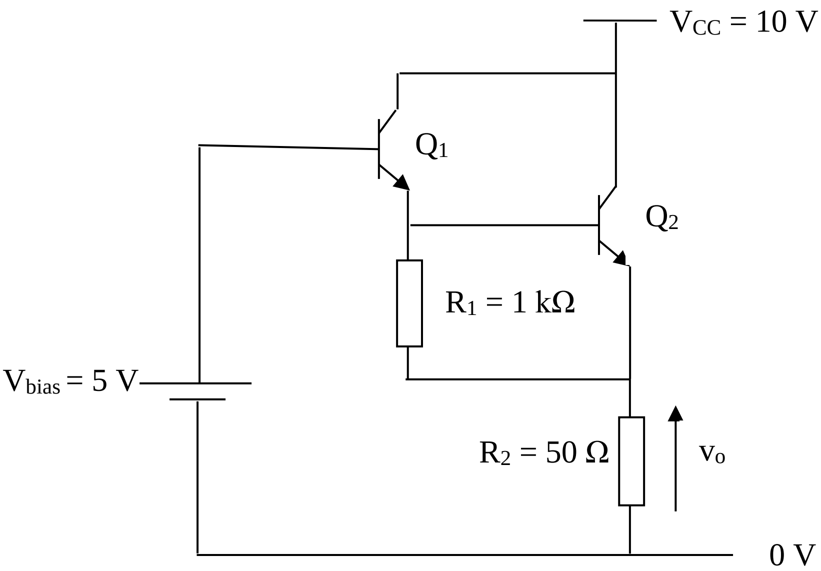

Figure Q1d

Question continues overleaf.

Question continued.

e) Compare and contrast the use of bipolar and MOSFET transistors in analogue circuits. **5**

f) How would you design a near ideal voltage amplifier incorporating negative feedback? What would be the advantages and disadvantages of your design compared to a voltage amplifier without negative feedback? **6**

g) Design the operational amplifier circuit of Figure Q1g to have an input resistance of 10 kΩ and a time constant ($R \times C$) of 10 μs. What function does the circuit perform? **4**

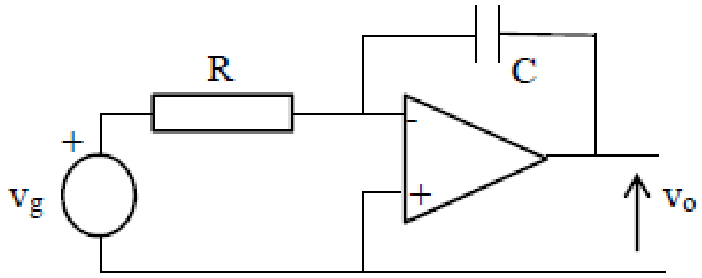

Figure Q1g

Question continues overleaf.

Question continued.

h) Figure Q1h shows a schematic diagram of a feedback amplifier with bias components removed. Identify the feedback topology and the amplifier type. Hence write down an expression for the feedback fraction, β. **5**

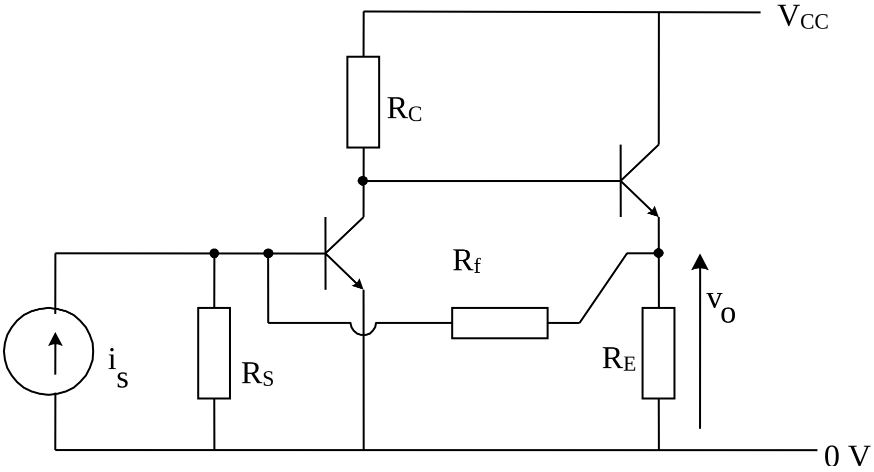

Figure Q1h

Total 40

2. a) Perform a simple initial design of an ac coupled common-emitter amplifier with four resistor biasing and emitter by-pass capacitor, to have a voltage gain of about 100, for the following conditions. Justify any approximations used. **10**

   i) Transistor ac common-emitter gain, β_o = 100 and dc gain is also 100.

   ii) Supply voltage of V_{CC} = 20 V.

   iii) Allow 10% V_{CC} across R_E.

   iv) DC collector voltage of about V_{DD} /2.

   v) DC current in the base bias resistors should be ten times greater than the DC base current.

   Assume $V_{BE}(on)$ = 0.6 V. The load resistor, R_L = 1 k Ω.

   (Hint: first find a value for the collector resistor.)

b) Estimate a value for the input capacitor, C_{IN} to set the low-frequency roll-off to be 1 kHz. **4**

c) Which is the preferred way to set the low-frequency roll-off and how is this generally accomplished? What would be a practical value for C_{IN} ? **2**

d) What would be the next step in the design process? **4**

Total
20

3. Figure Q3 shows a differential amplifier where the transistors can be considered to be identical. The voltage gain is given by $A_V = \frac{g_m}{2} \times R_C$, V_{BE} (on) ~ 0.6 V and V_T = 25 mV.

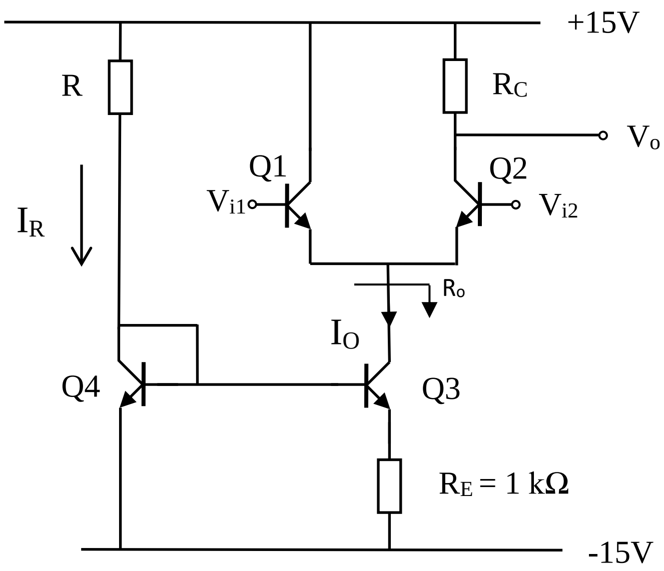

Figure Q3

a) Prove the relationship: **12**

$$R_E = \frac{V_T}{I_O} \times log_e \left(\frac{I_R}{I_O}\right)$$

stating assumptions made in the derivation. Hence design the amplifier (estimate values for resistors R and R_C) to give a voltage gain > 100 and a DC voltage level at the output of 0 V (Hint: allow 4 × V_T across R_E). Calculate a value for the differential input resistance of the amplifier.

b) Explain the meaning of the term ‘common-mode rejection ratio (CMRR)’. Comment on the dynamic resistance (R_O) looking into the current mirror and explain its significance for the CMRR. **4**

c) Suggest how the design might be improved to make a better voltage amplifier. **4**

Total 20

4. a) Explain what is meant by the virtual short principle as applied to operational amplifiers with negative feedback. **5**

b) Draw an appropriate equivalent circuit for the amplifier shown in Figure Q4b, and hence derive the following expression for the input impedance. **8**

$$R_{in} = r_d\left(1 + A_{ol}\right) + r_o$$

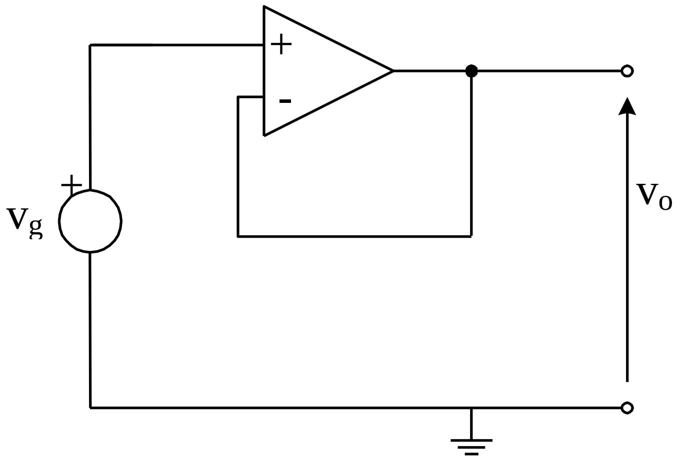

Figure Q4b

c) Derive the following expression for the loop gain of the amplifier in question 4b). **7**

$$T = A_{ol}\,\frac{r_d}{r_o + r_d}$$

Estimate values for T, β, R_{in} and comment on the values obtained.

Parameter values are r_d = 10 kΩ, r_o = 50 Ω and $A_{ol} = 10^5$.

Total 20