Digital Electronics and Microprocessor Systems (ELEC211)

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Digital 9: Introduction to State Machines

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Outline

- State machines
- Moore and Mealy circuits
- State graphs / diagrams
- Analysis by signal tracing
- Algorithmic State Machine (ASM) Charts

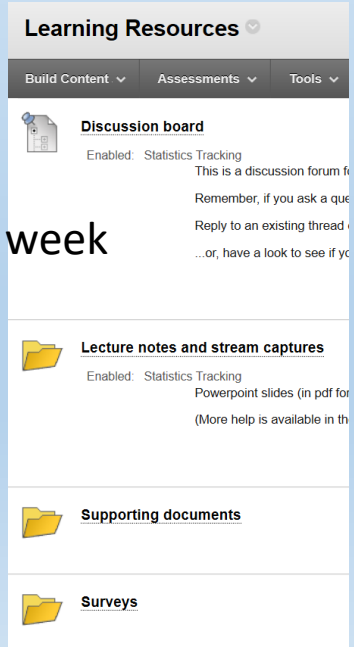
Previous material

Simple counters ✓
Combinational and sequential logic ✓
Design with flip-flops ✓
Next-state maps ✓
State tables ✓

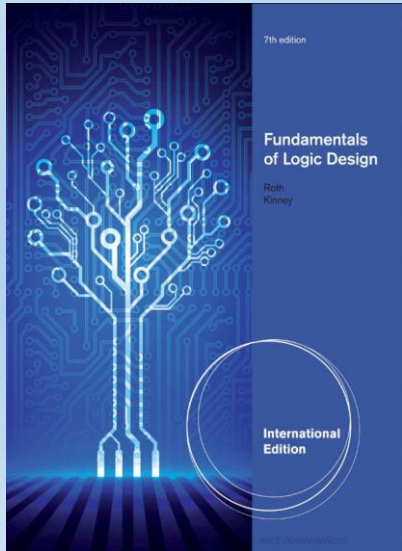
Use VITAL!:

- Stream lectures
- Handouts
- Notes and Q&A each week
- Discussion Board
- Exam resources

www.liv.ac.uk/vital



Course textbook – 7th ed. available as e-book!



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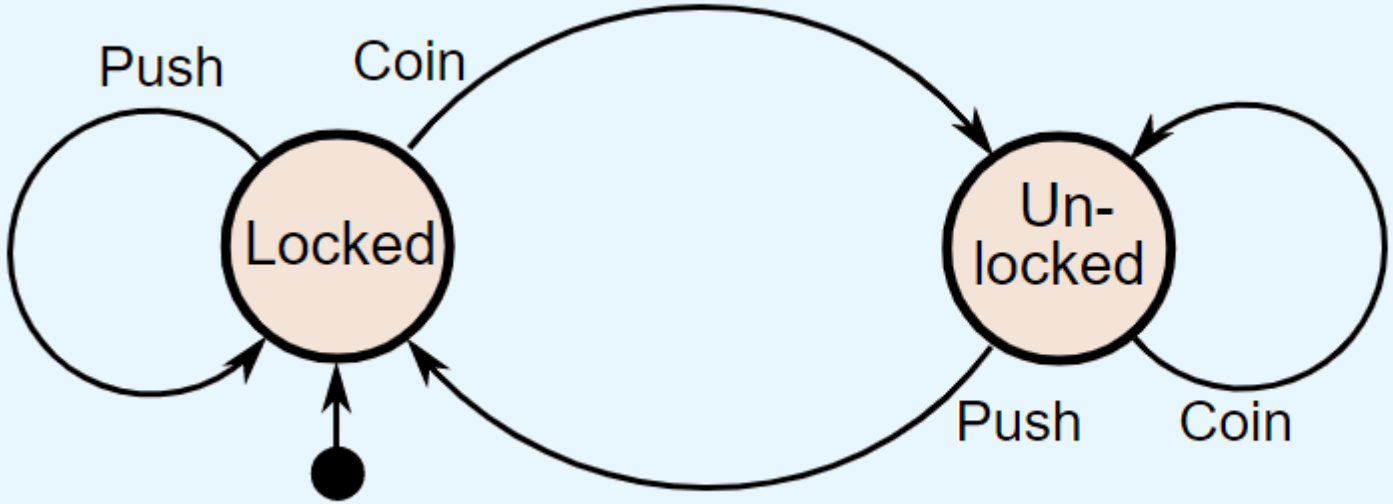
Remember the turnstile?



State Diagram for a simple coin-operated turnstile

https://commons.wikimedia.org/wiki/File:Turnstiles_in_Alewife_station,_August_2005.jpg

https://en.wikipedia.org/wiki/Finite-state_machine#/media/File:Turnstile_state_machine_colored.svg

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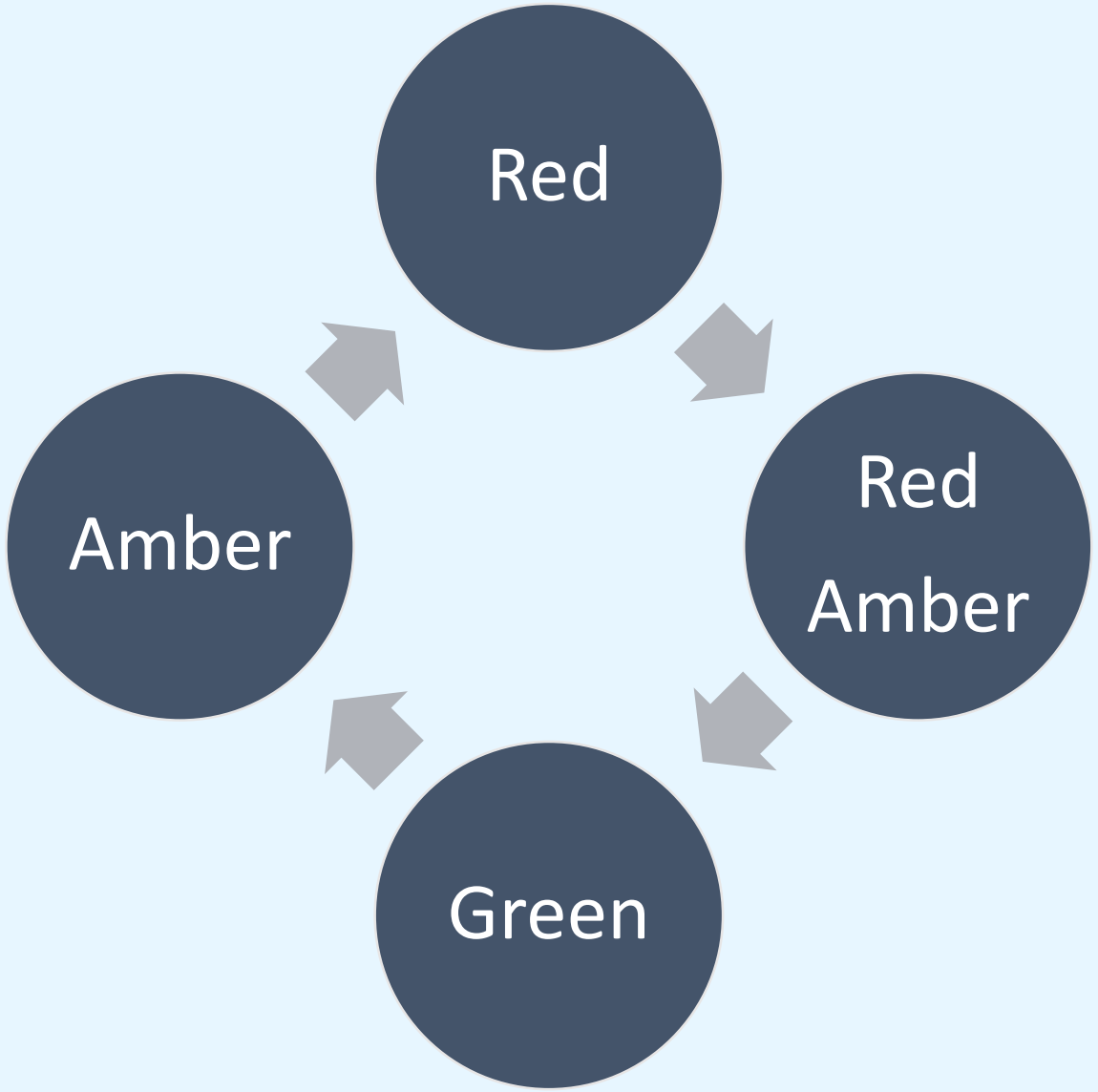
https://en.m.wikipedia.org/wiki/File:Traffic_lights.jpg



A (VERY) simplistic ‘state diagram’…!

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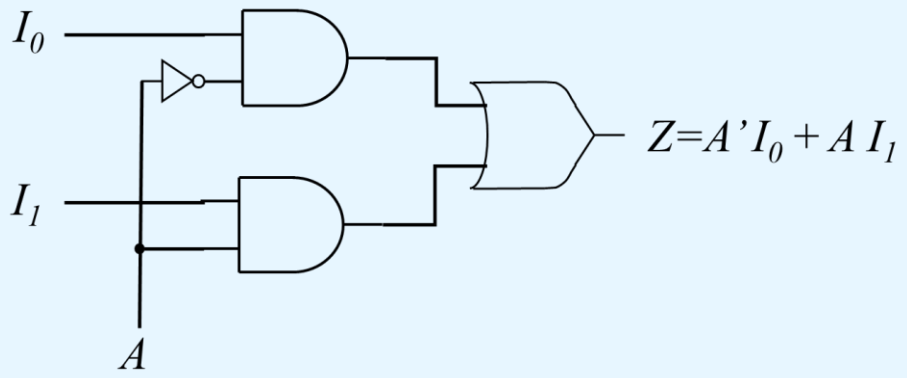
Combinational

V

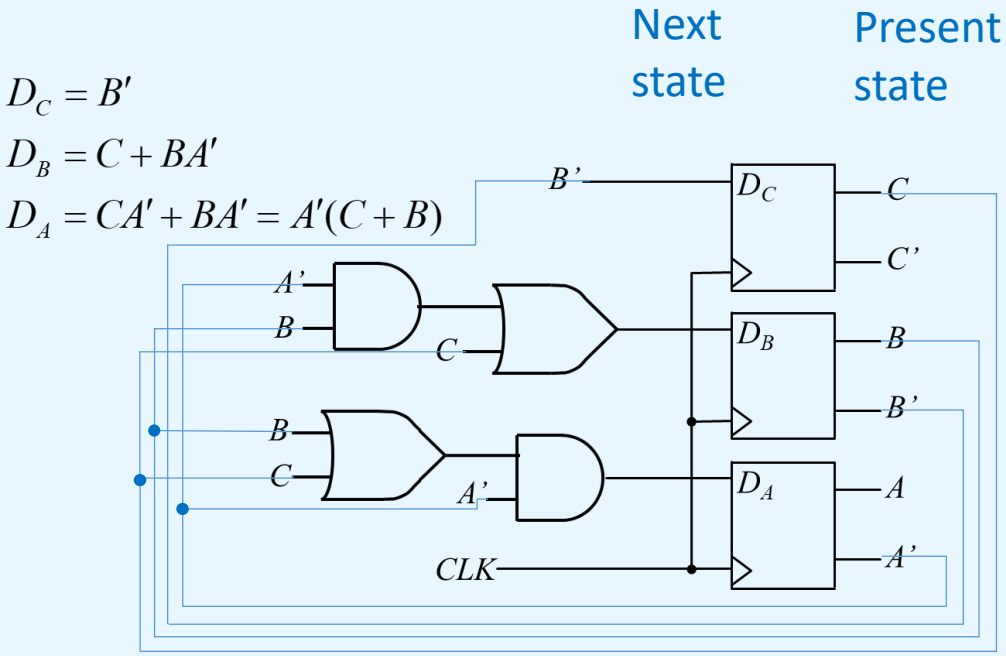
Sequential

- Logic circuit for a 2-1 MUX



Present state does **not** influence the next output

All input changes have an **'immediate'** effect on output (apart from propagation delay)

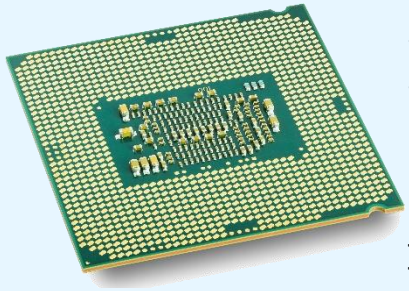


Present state (**memory**) may affect the next output

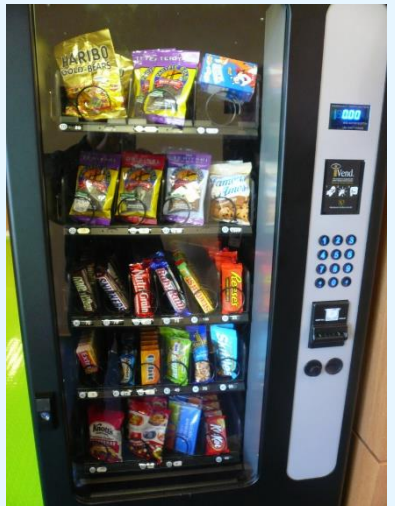
At least some input changes must wait for the next active edge of the **clock** to take effect

Feedback loop

State Machine…



- … abstract concept
- … of a device which stores info about its state
  - i.e. it has memory
- We use state machines to model the design of digital hardware
- Finite State Machine (FSM)
  - Has a **finite** number of states
  - **Transitions** between them
- The present output may depend on:
  - The present state (Moore machine)
  - The present state AND the present input (Mealy machine)



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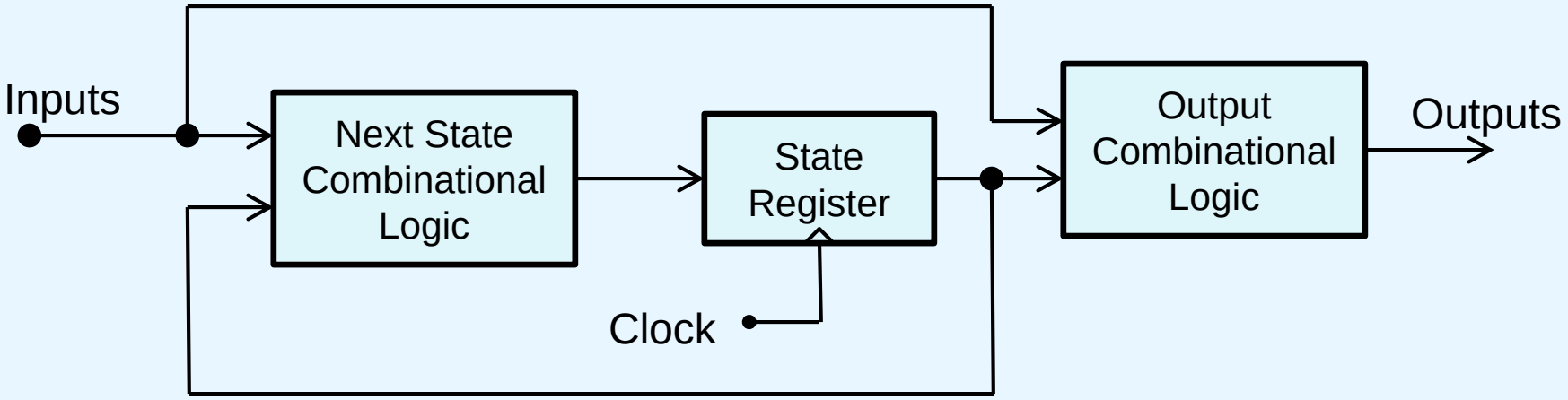
Mealy Model of Finite State Machines

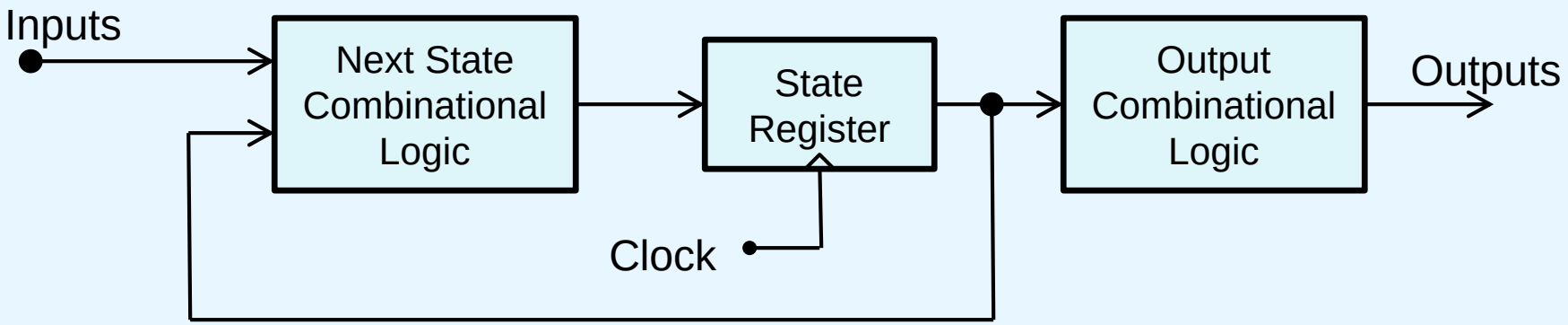


Finite State Machine – a set of states and transitions

In this model, the present output is a function of **both the present state and the present input.**

The Next State Combinational Logic block calculates the next state of the machine and applies the appropriate inputs to the state register flip-flops.

Moore Model of Finite State Machines

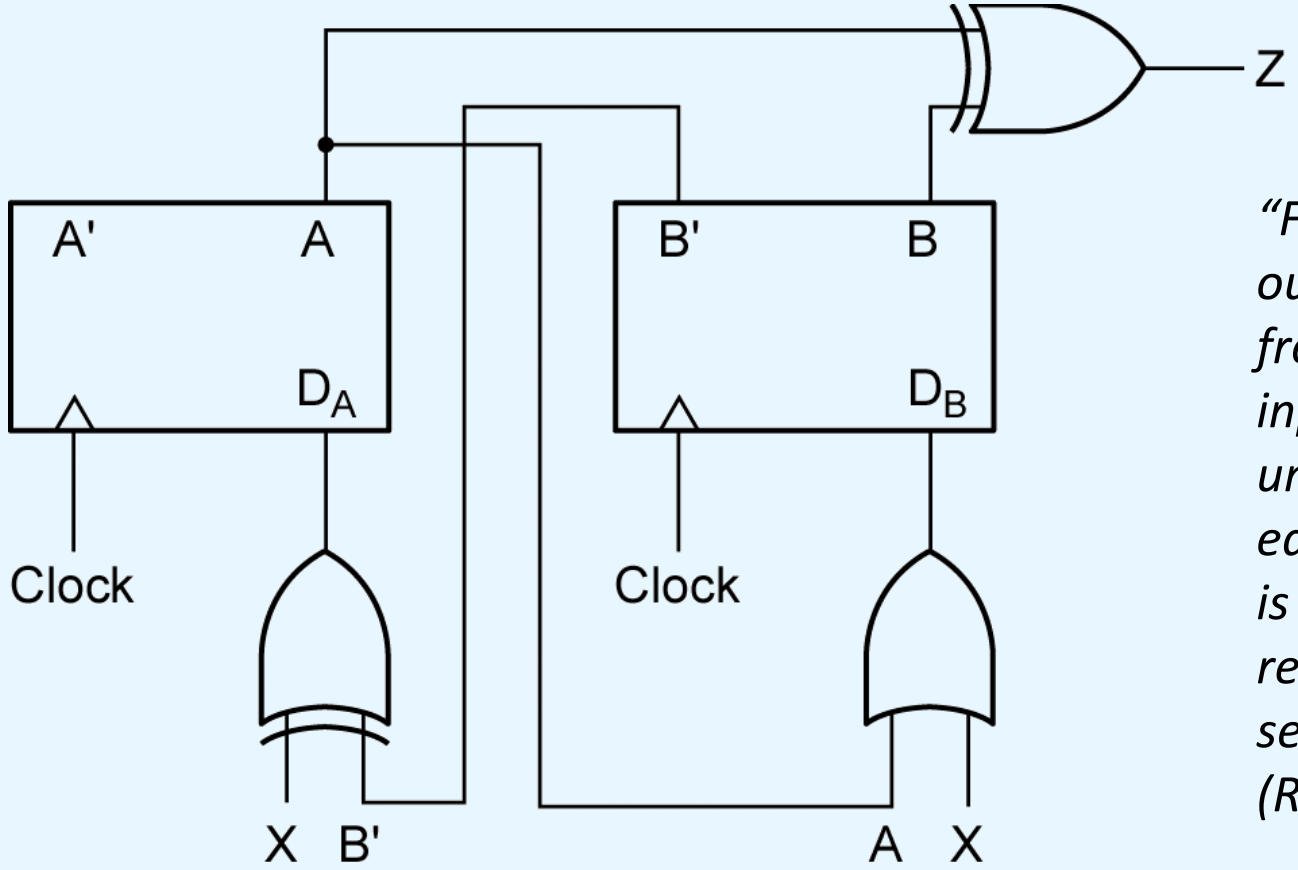


Operation of the Moore circuit is similar to that of the Mealy except when a set of inputs is applied to the Moore circuit, the resulting outputs do not appear until after the clock's active edge.

Moore Sequential Circuit

$$Z = A \oplus B$$

Output only changes when the state changes (when the flip-flops change state)



*"For the **Moore** circuit, the output (Z) which results from application of a given input (X) does not appear until after the active clock edge; the output sequence is displaced in time with respect to the input sequence"*
(Roth/Kinney p.399)

Moore machine: **present output (Z) is only a function of the present state (A,B)** and not the present input (X)

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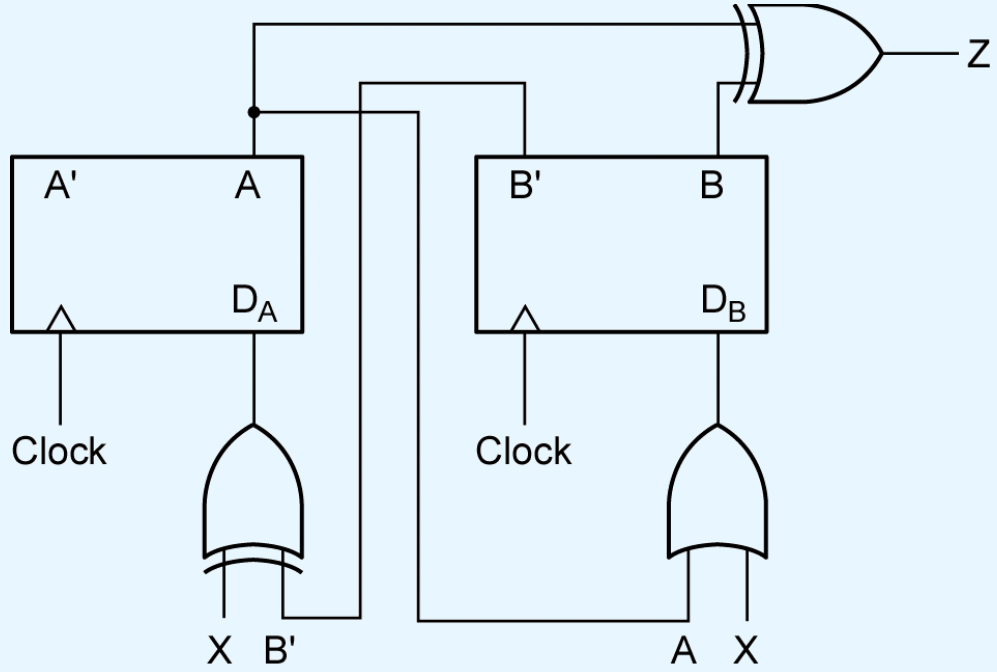
Analysis by Signal Tracing and Timing Charts

All flip-flops reset to 0 (start with **A=B=0**)

X sequence (predetermined): **01101**

X synchronised: assumes new value after each rising edge



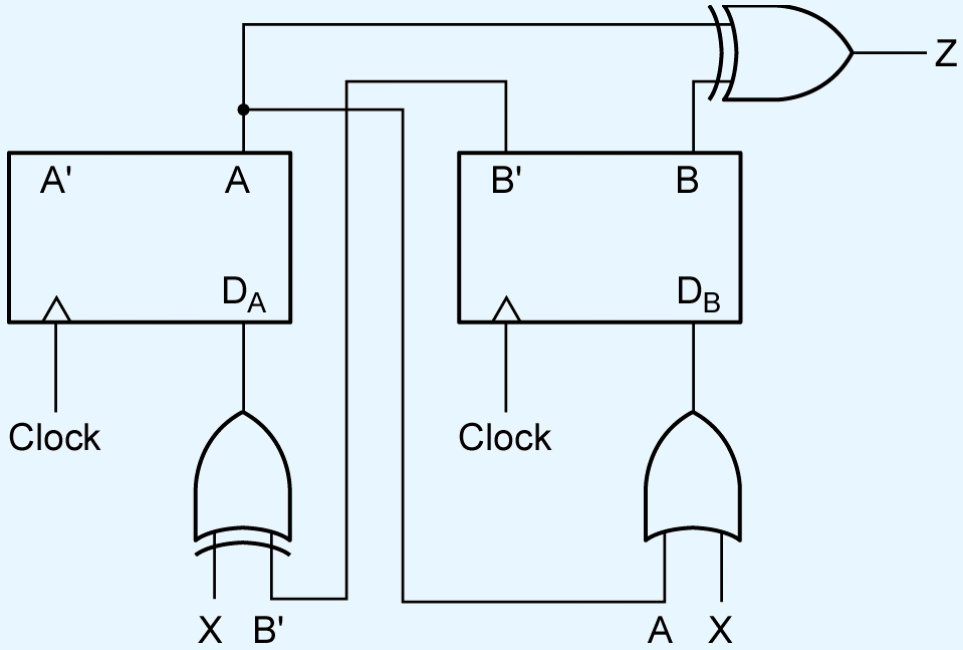
For the first input in the given sequence, determine the circuit outputs and flip-flop inputs

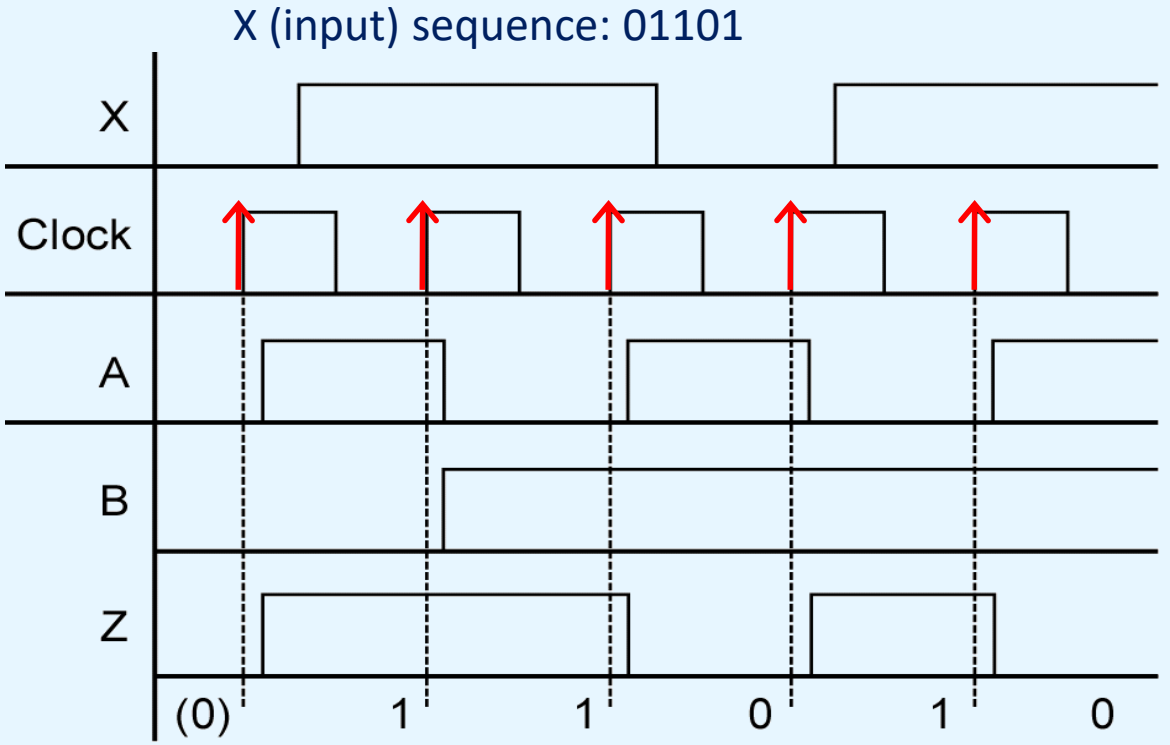
Determine the new set of flip-flop states after the next clock edge

Determine the outputs that correspond to the new states.

Repeat the sequence until the timing chart can be constructed.

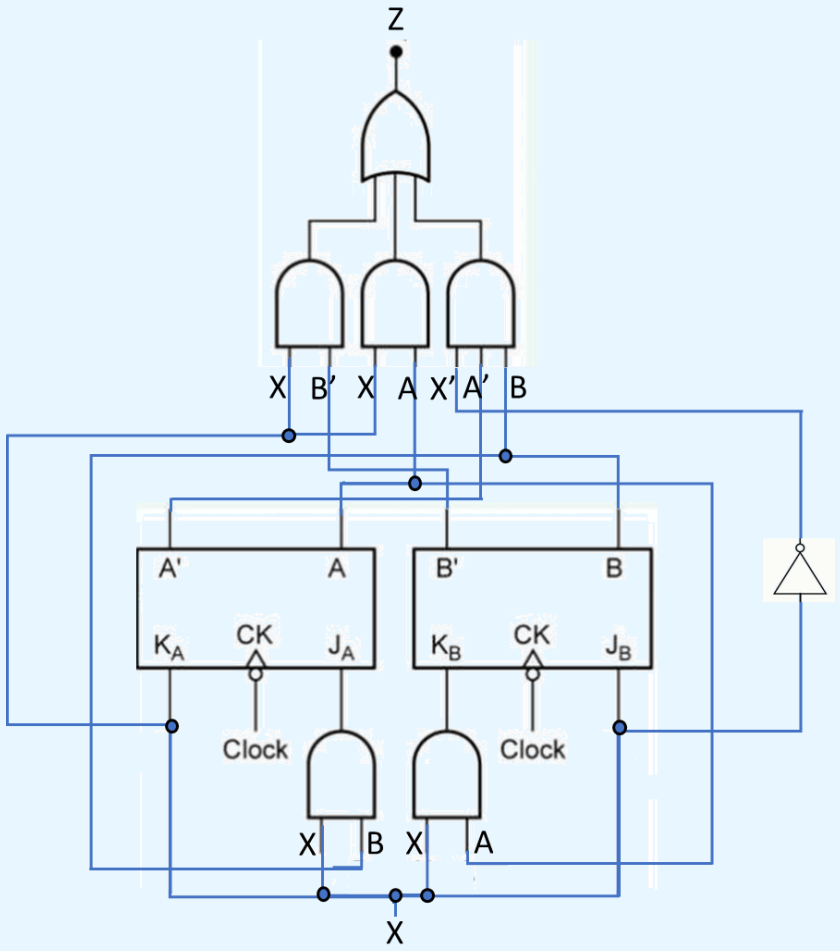
Analysis by Signal Tracing and Timing Charts





Initially: X=0, A=0, B=0 so D_A=1, D_B=0 → after first rising clock edge: A = 1, B = 0
Now X changes to 1 (and A=1, B=0) so D_A= 0, D_B= 1 → after second rising clock edge: AB = 01
Now X stays at 1 (and A=0, B=1) so D_A= 1, D_B= 1 → after third rising clock edge: AB = 11 ……..

Mealy Sequential Circuit



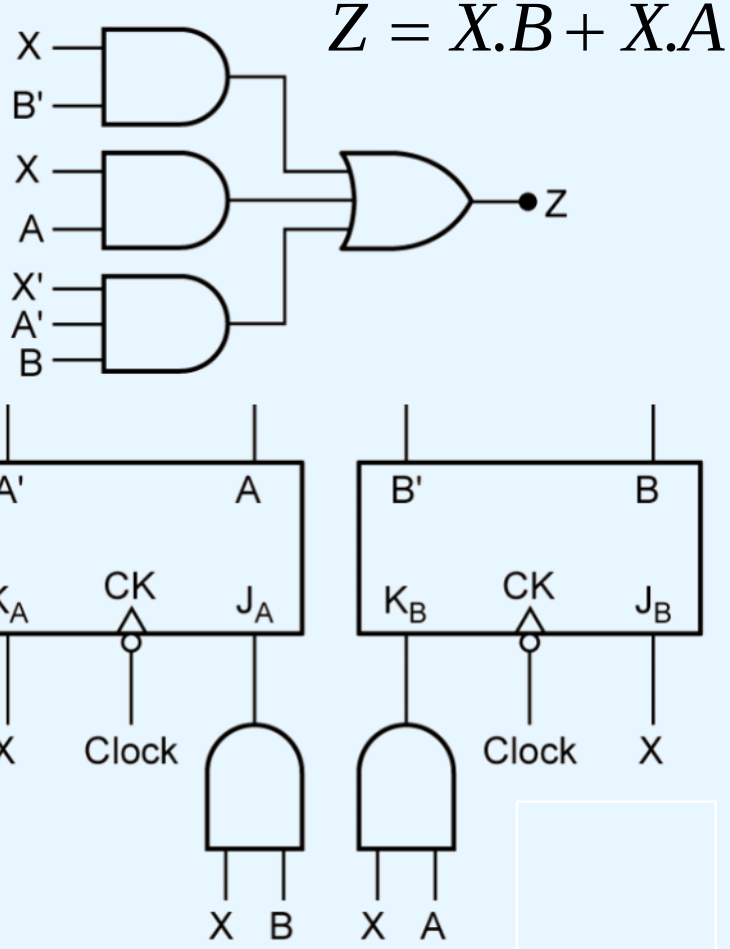
In a Mealy machine the output is a function of **both the present state and the present input.**

In this case, Z is a function of A and B, representing the present state (present states of the flip-flops), and also is 'directly' a function of X which is an input.

Z may change EITHER when the flip-flops change state OR when the input changes

Mealy Sequential Circuit

$$Z = X.\overline{B} + X.A + \overline{X}.\overline{A}.B$$



Simplified diagram

In a Mealy machine the output is a function of **both**

- **the present state <u>and</u>**
- **the present input**

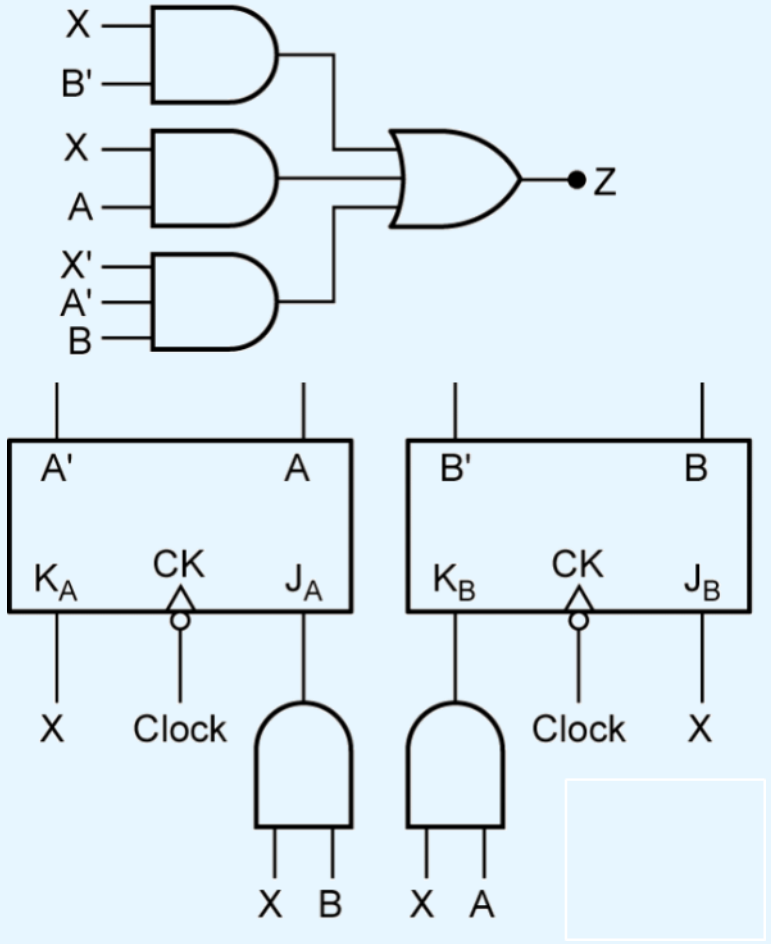
In this case:

- Z is a function of A and B, representing the present state (present states of the flip-flops)
- Z is also a function ‘directly’ of X which is an input

Z may change

- EITHER when the flip-flops change state (after clock active edge)
- OR when the input changes

Mealy Sequential Circuit



For a clocked sequential circuit, the value of the input immediately before the active clock edge determines the next state of the flip-flops.

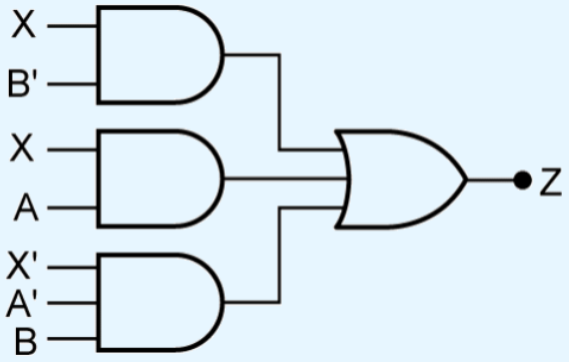
The output from a Mealy circuit is only of interest immediately preceding the active clock edge.

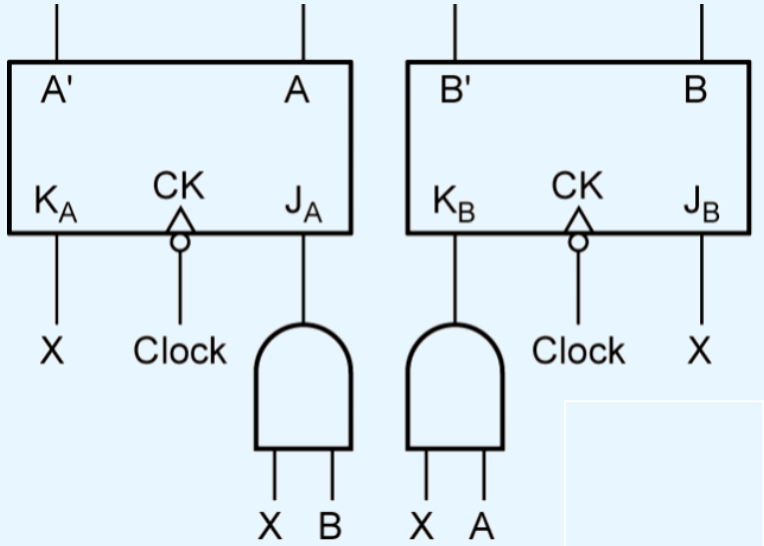
Ignore extra changes in-between. These occur because our Mealy output is also affected directly by input changes, independent of the clock.

These false outputs are referred to as ‘glitches’ or ‘spikes’ (mentioned in a previous lecture)

Mealy Sequential Circuit

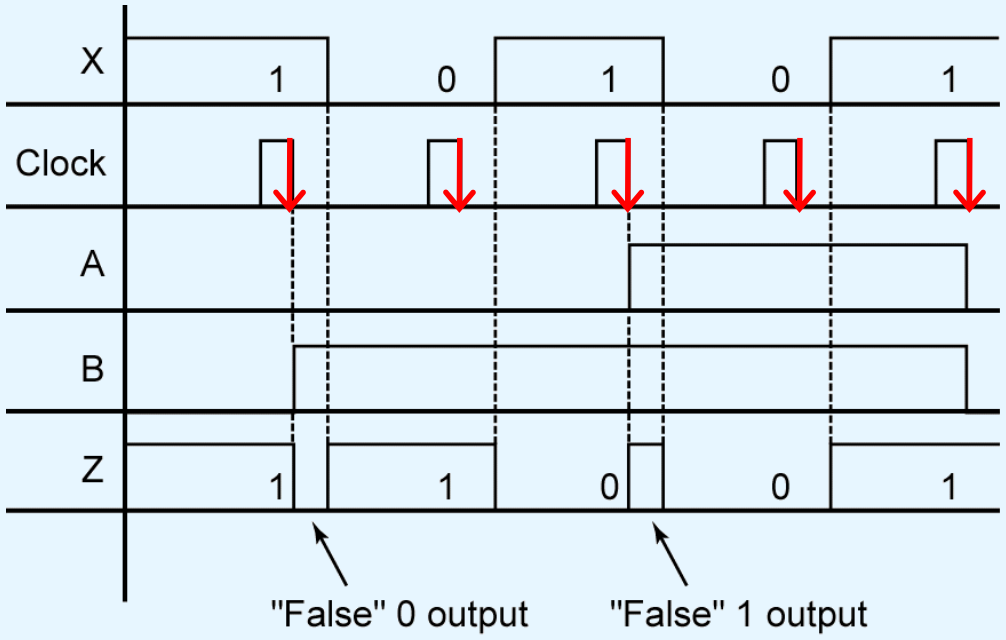
$$Z = X.\overline{B} + X.A + \overline{X}.\overline{A}.B$$





X (input) sequence: 10101

X	1	0	1	0	1
A	0	0	0	1	1
B	0	1	1	1	1
Z	1	1	0	0	1



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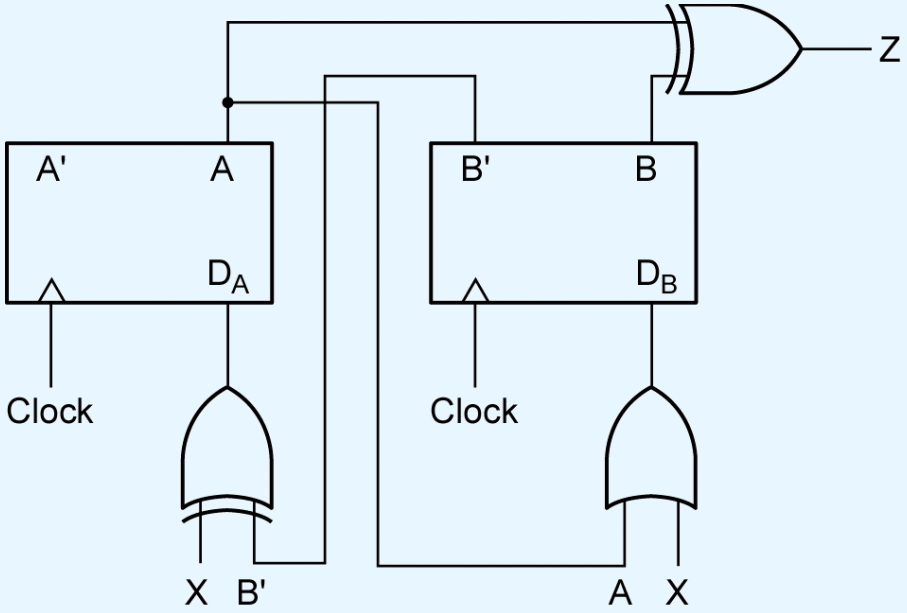
See Roth/Kinney p399-400

State Tables & Graphs for Moore Machine

Although signal tracing and timing chart construction is OK for small circuits, state graphs & state tables provide a more systematic approach. This leads us to a general synthesis procedure for sequential circuits.

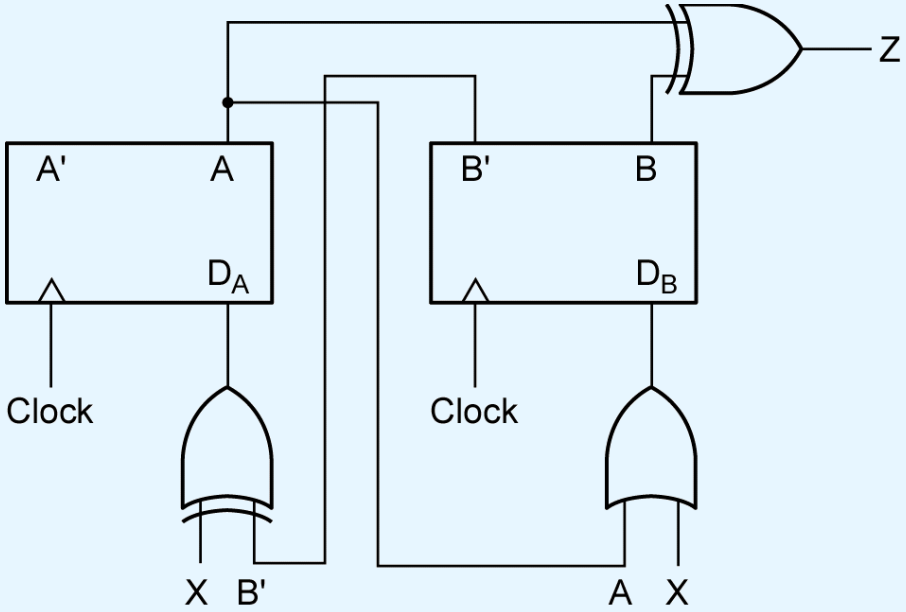


$$D_A = A^+ = X \oplus B'$$

$$D_B = B^+ = X + A$$

$$Z = A \oplus B$$

State Table – Moore Machine



$$D_A = A^+ = X \oplus B'$$
$$D_B = B^+ = X + A$$
$$Z = A \oplus B$$

AB	A^+B^+		
	X=0	X=1	Z
00	10	01	0
01	00	11	1
10	11	01	1
11	01	11	0

Initially AB=00 and X=0, so Z=0 and A^+B^+=10.
This means that *after* the rising clock edge , the flip-flop state will be AB=10 and then the output will be Z=1.

State Table – Moore Machine

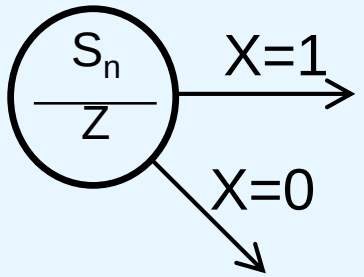
We can replace each combination of flip-flop states with a single symbol which represents the state of the circuit.

AB	A^+B^+		
	X=0	X=1	Z
00	10	01	0
01	00	11	1
11	01	11	0
10	11	01	1

Present State	Next State		Present Output
	X=0	X=1	Z
S_0	S_3	S_1	0
S_1	S_0	S_2	1
S_2	S_1	S_2	0
S_3	S_2	S_1	1

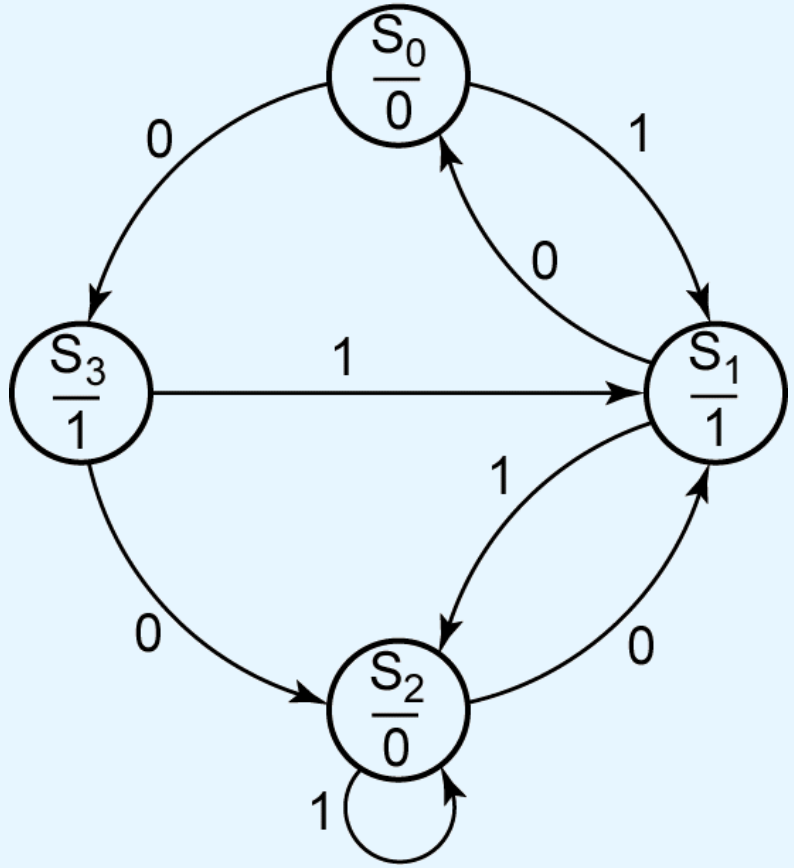
Note that state S_2 has been designated AB = 11 and state S_3 has been designated AB = 10. i.e. we have changed the order in which we present the states.

State Graph – Moore Machine



Present State	Next State		Present Output
	X=0	X=1	Z
S_0	S_3	S_1	0
S_1	S_0	S_2	1
S_2	S_1	S_2	0
S_3	S_2	S_1	1

The state graph (right) represents the state transition table (above).



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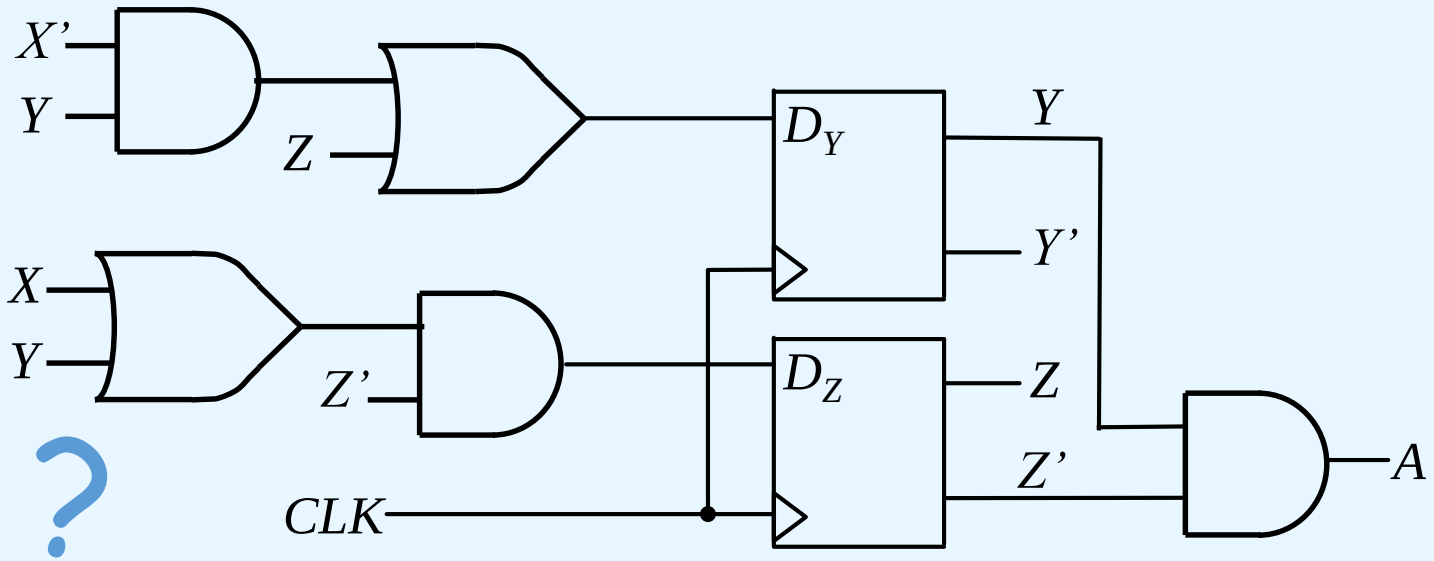
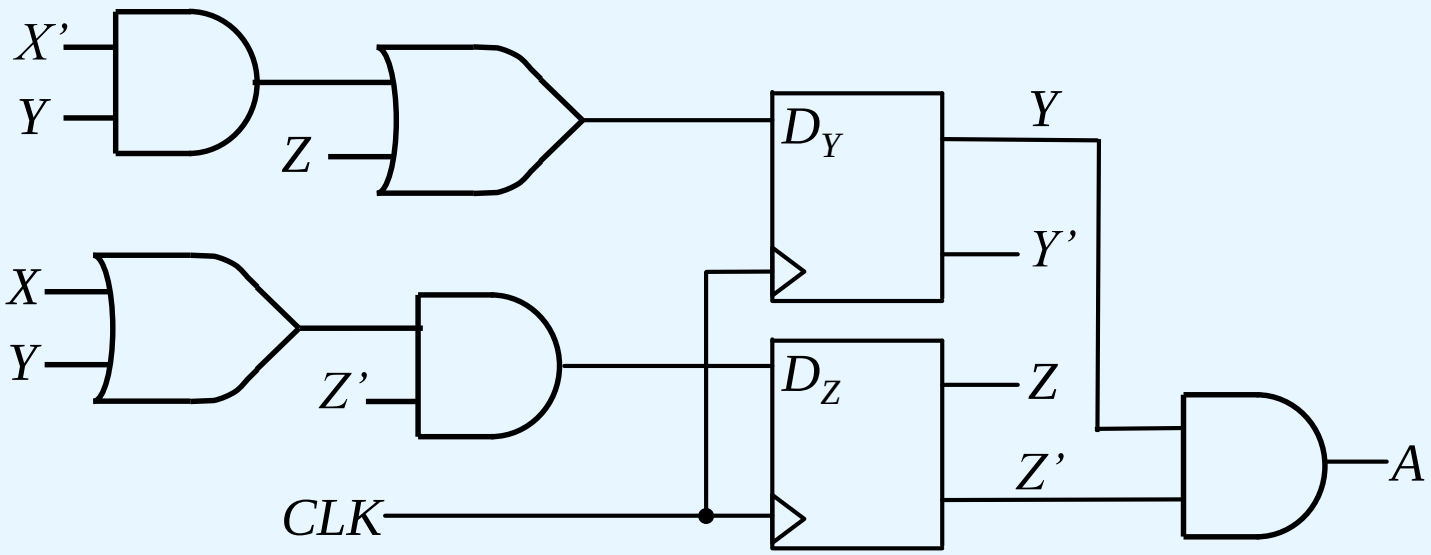
Question

Find the State Diagram for the following Moore Machine (X is an input, A is the output).



Y	Z	State
0	0	S_0
0	1	S_1
1	0	S_2
1	1	S_3

Method



$Y^+ = D_Y = X'.Y + Z$

$Z^+ = D_Z = (X + Y).Z'$

$A = Y.Z'$

YZ	Y^+Z^+		
	X=0	X=1	A
00	00	01	0
01	10	10	0
10	11	01	1
11	10	10	0

Present State	Next State		Present Output
	X=0	X=1	A
S_0	S_0	S_1	0
S_1	S_2	S_2	0
S_2	S_3	S_1	1
S_3	S_2	S_2	0

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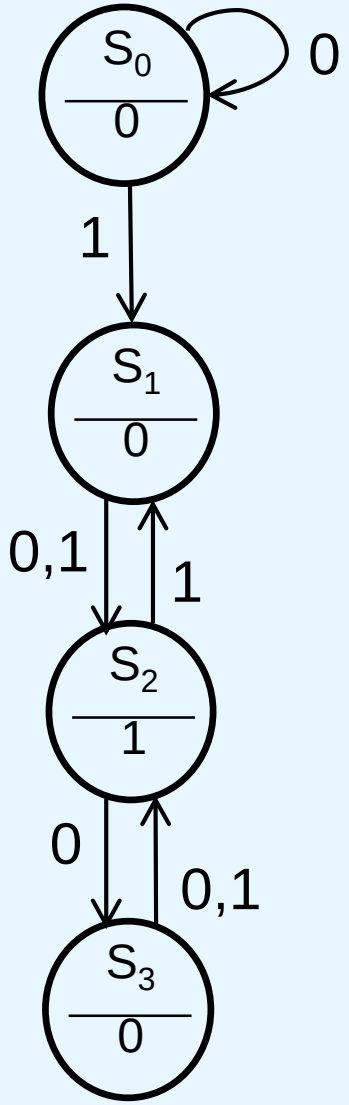
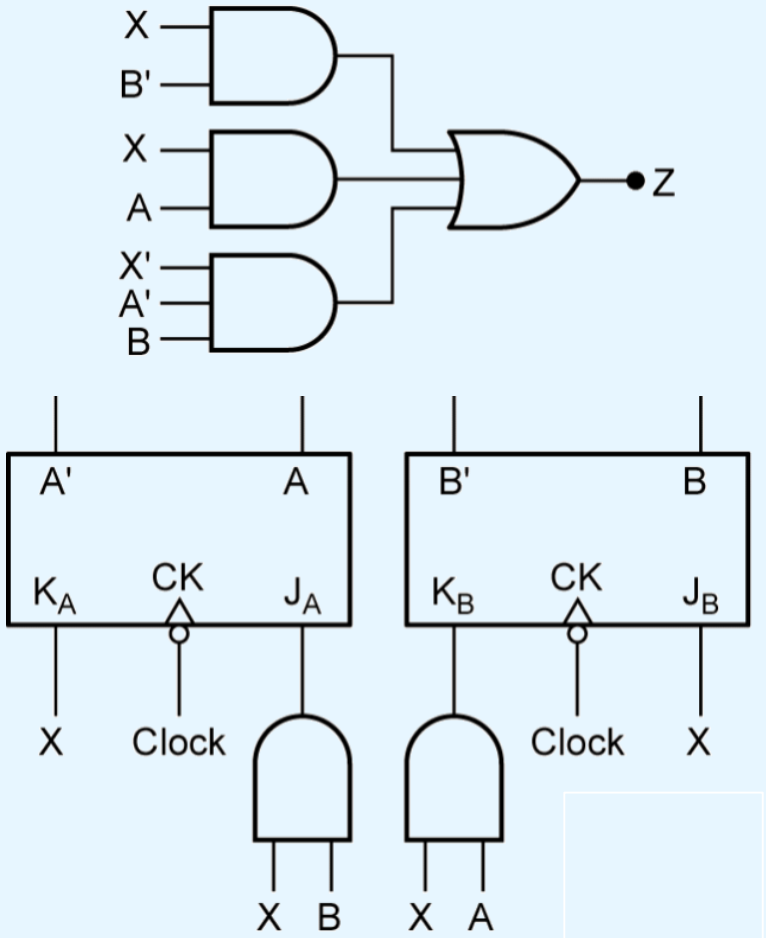
Answer

Present State	Next State		Present Output
	X=0	X=1	A
S_0	S_0	S_1	0
S_1	S_2	S_2	0
S_2	S_3	S_1	1
S_3	S_2	S_2	0



State Tables & Graphs for Mealy Machine



$$A^+ = J_A\overline{A} + \overline{K_A}A = X.B.\overline{A} + \overline{X}.A$$

$$B^+ = J_B\overline{B} + \overline{K_B}B = X.\overline{B} + (\overline{X.A}).B$$

$$= X.\overline{B} + \overline{X}.B + \overline{A}.B$$

$$Z = X.\overline{B} + X.A + \overline{X}.\overline{A}.B$$

State Table – Mealy Machine

AB	A^+B^+		Z	
	X=0	X=1	X=0	X=1
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

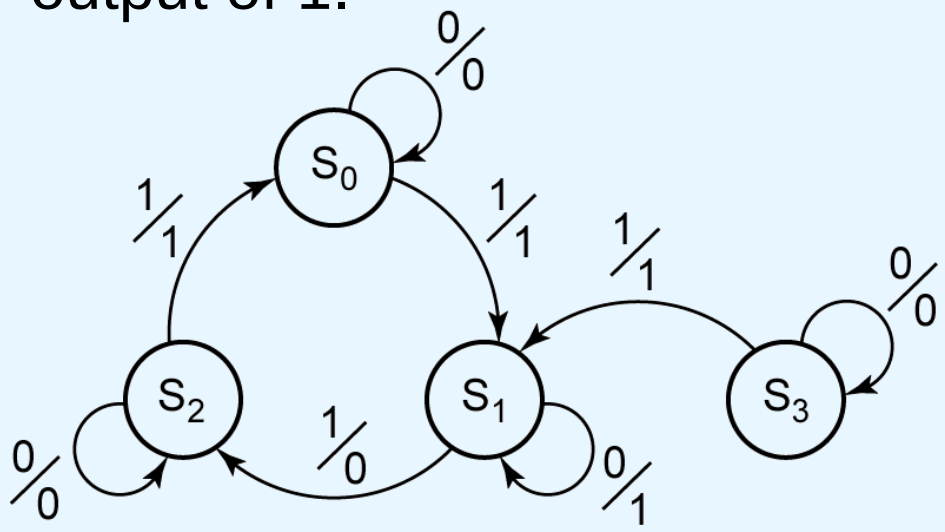
Present State	Next State		Present Output Z	
	X=0	X=1	X=0	X=1
S_0	S_0	S_1	0	1
S_1	S_1	S_2	1	0
S_2	S_2	S_0	0	1
S_3	S_3	S_1	0	1

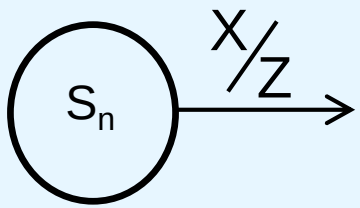
Again, state S_2 has been designated AB = 11
and state S_3 has been designated AB = 10.

State Graph – Mealy Machine

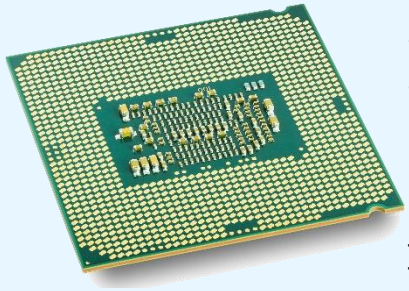
The labels on the arrows between states are of the form X/Z. In state S_0 an input of 0 gives an output of 0, and an input of 1 gives an output of 1.

Present State	Next State		Present Output Z	
	X=0	X=1	X=0	X=1
S_0	S_0	S_1	0	1
S_1	S_1	S_2	1	0
S_2	S_2	S_0	0	1
S_3	S_3	S_1	0	1

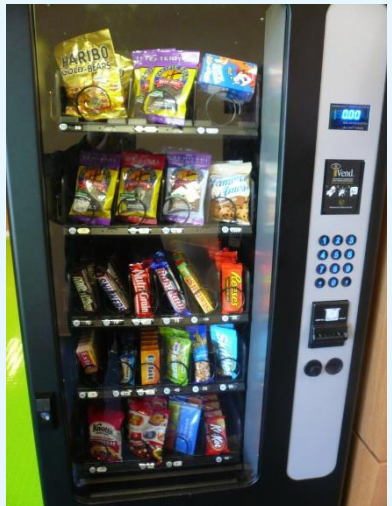




Algorithmic State Machine (ASM)



- "Algorithm": set of rules or process to follow
- → **Algorithmic State Machine (ASM)**
  - Method for designing finite state machines
- State graph → ASM chart → state [transition] table …
- … → equations for outputs and next-state logic
- … → realise (make it real, implement) with flip-flops & gates



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https://commons.wikimedia.org/wiki/File:Intel_CPU_Core_i7_6700K_Skylake_perspective.jpg

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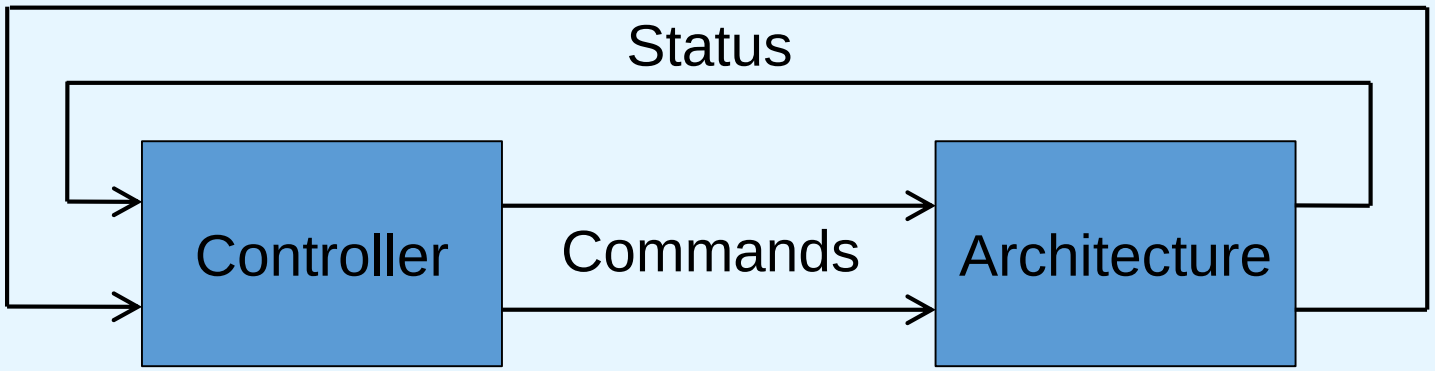
Algorithmic State Machine (ASM)



The controller issues properly sequenced commands to the controlled device

These commands make the architecture perform the actions dictated by the control algorithm

Usually the controller will need status information from the architecture that serves as **decision variables** for the control algorithm

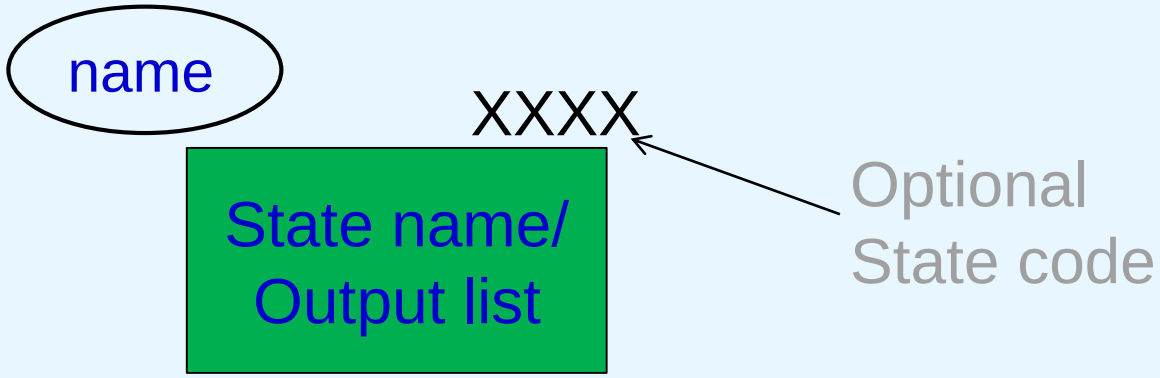
States and Clock

- The algorithmic state machine (ASM) moves through a sequence of states based on the position (state) in the control algorithm and the value of the relevant status variables.
- It is the task of the present state of the system to:
  1. Produce any required output signals
  2. To use appropriate input information to move, at the proper time, to the *next state*
- In synchronous systems, the state times are determined solely by the *master clock*

States

Each active transition of a clock causes a change of state from the *present* state to the *next* state

The ASM chart describes the control algorithm such that, given the present state, and the values of the input variables, the next state is determined unambiguously.

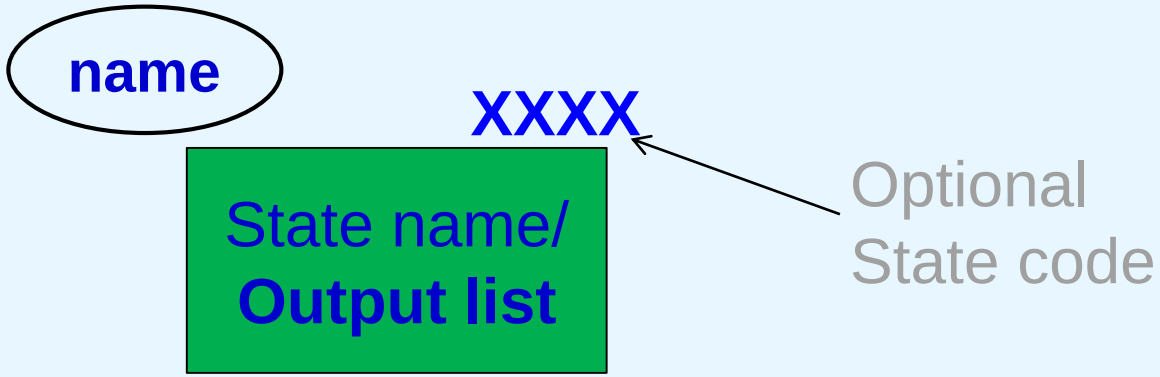


States

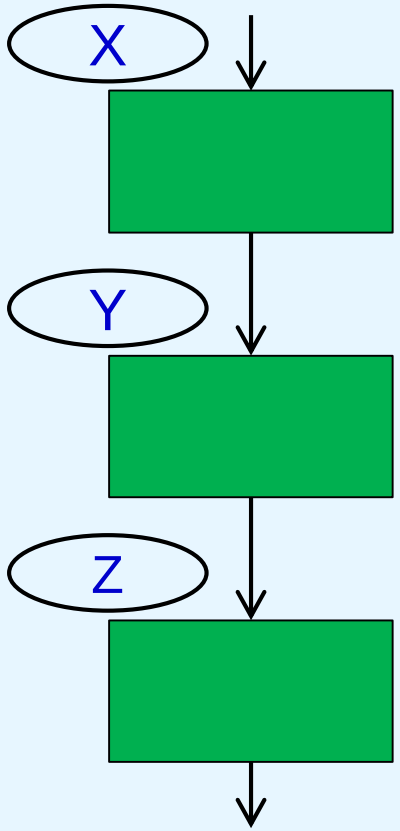
The symbol for a state is a rectangle with its symbolic name enclosed in a small circle (or oval) at the upper left corner (our usual practice.)

Sometimes the state name is written inside the state box.

The outputs are written inside the state box.

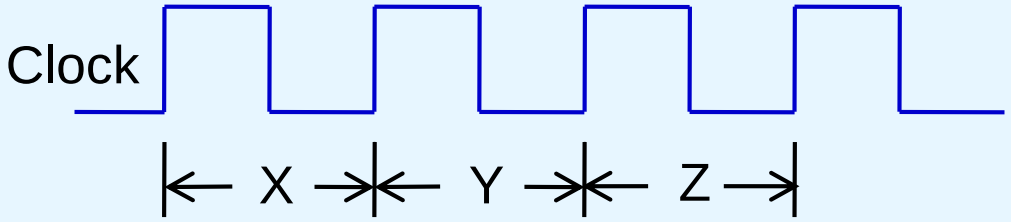


Sequential ASMs



We can represent a purely sequential algorithm as an ASM chart of a sequence of states.

The timing diagram for this sequence of states is:

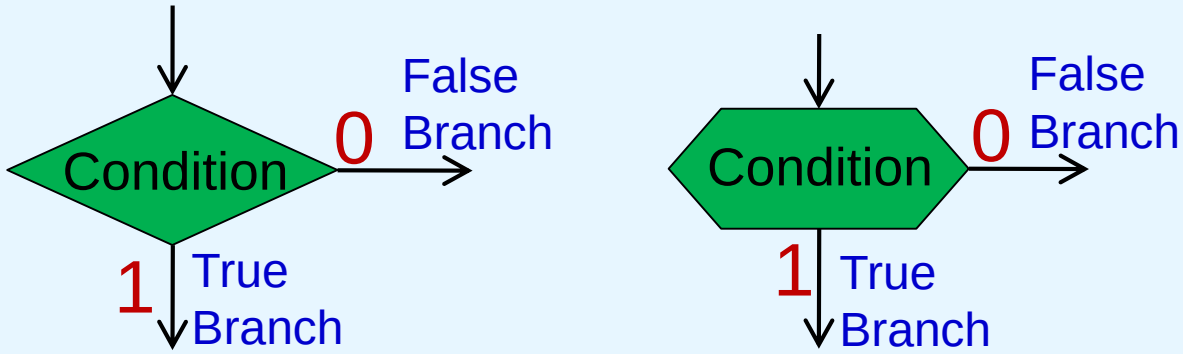


You should think of time as rigorously implied in the ASM chart notation.

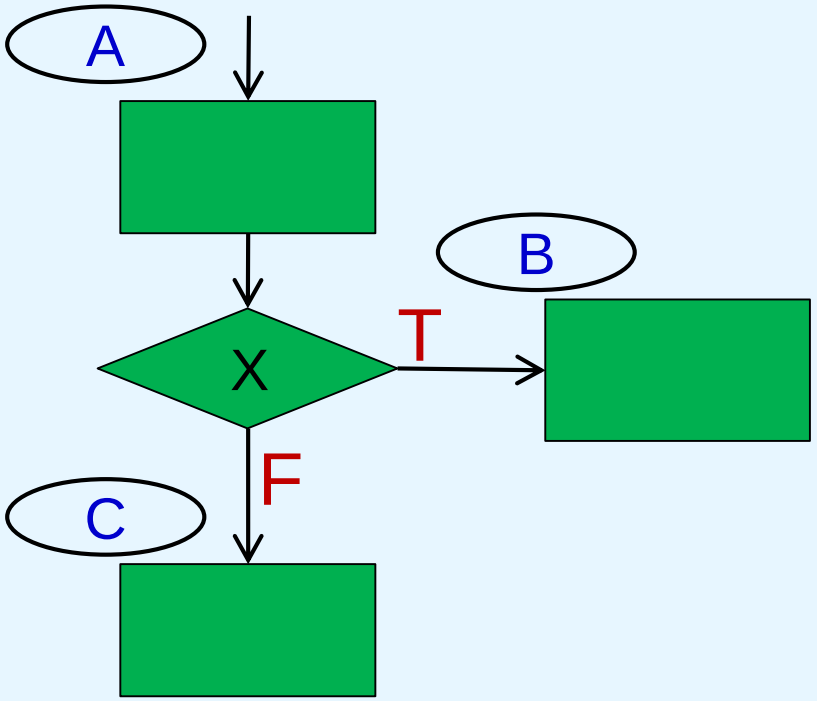
Branches

We need some way to express conditional branches so that the next state is determined not only by the present state but also by the present vale of one or more test (status) inputs.

The symbol is the same as in conventional flowcharts for software: the diamond (or diamond-sided rectangle).



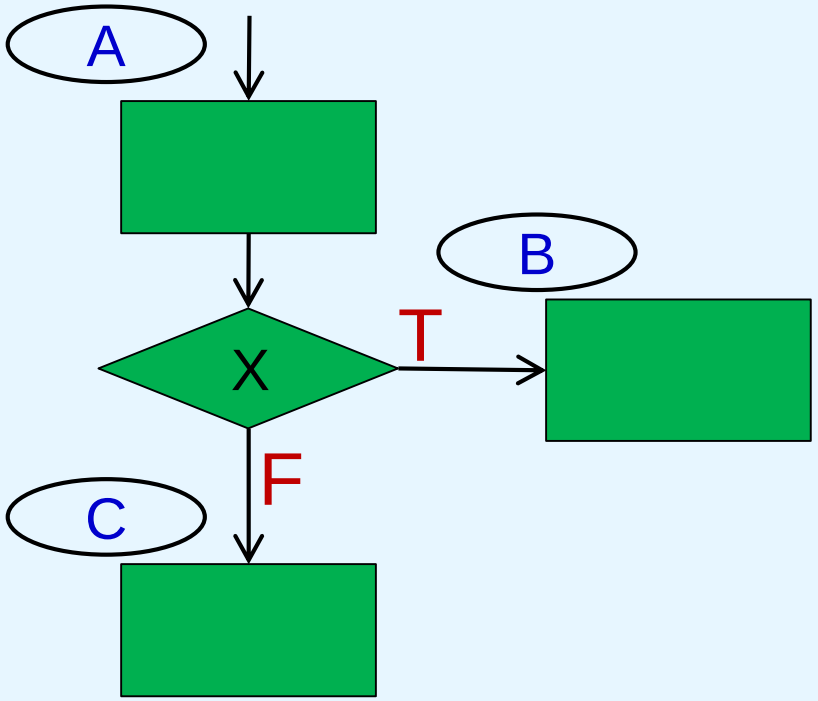
Branches – continued

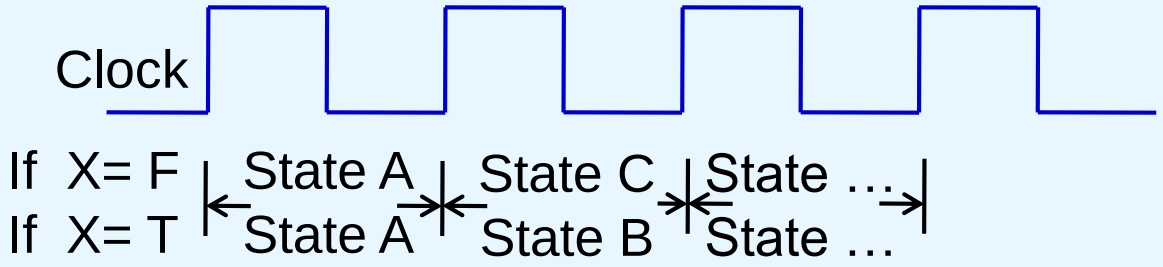


The **decision to jump** to either state B or state C is made **during** state A, and the jump occurs at the end of state A.

In hardware implementations, the voltage representing X must be stable for some period before the decision is made.

Branches – continued

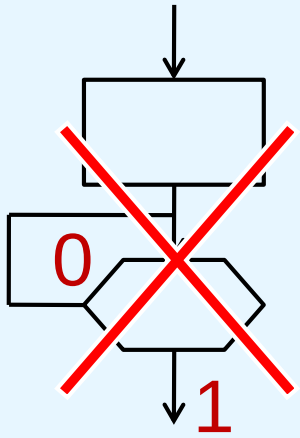




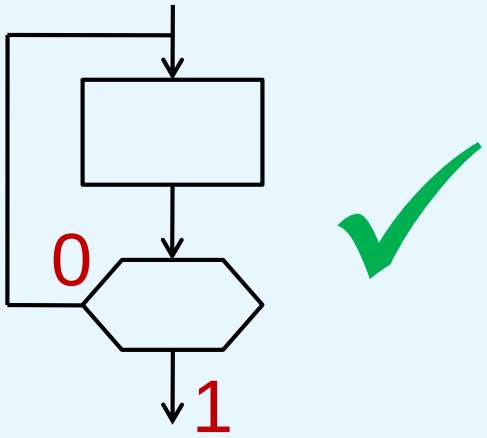
The test does not require a separate clock period; it is done **in parallel with the actions of the parent state rectangle** and thus is part of the parent state.

Feedback branches

For feedback, the path must return to a **state**:



Incorrect feedback

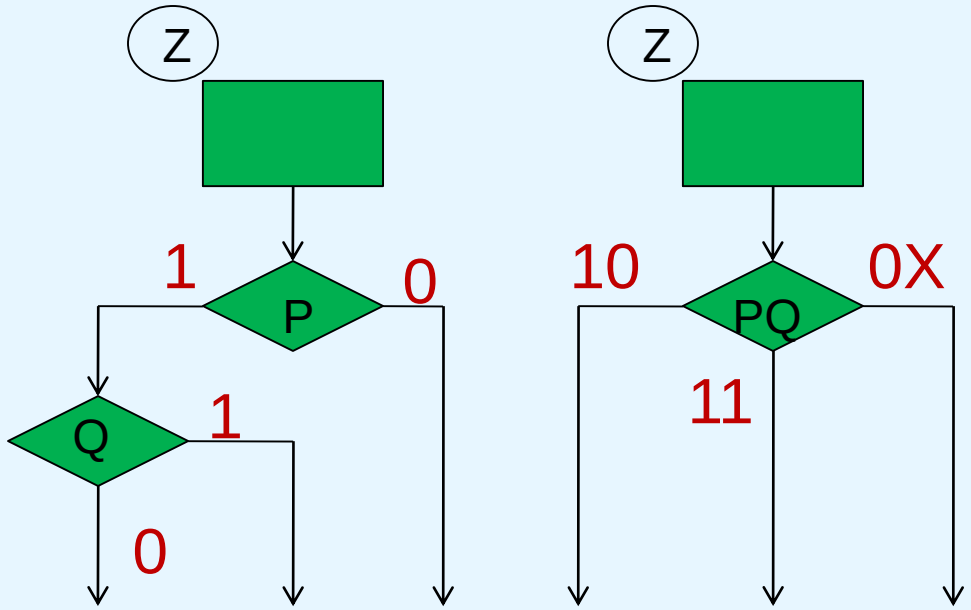


Correct feedback

Multi-way branches

We may draw a sequence of diamonds or have more than two paths coming from the same diamond.

Figure (a) conveys the incorrect impression that the test of variable P is of a higher priority than the test of Q.



(a) (b)

For every valid combination of the input variables, there must be exactly one exit path defined.

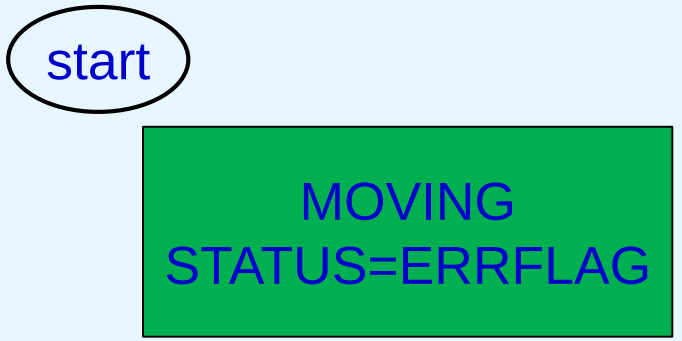
Outputs

The function of a controller is to send properly sequenced outputs to the controlled device according to some algorithm.

To indicate an output, a command description is placed within the appropriate state rectangle.

The first line, MOVING, calls for the ‘assertion’ of the signal MOVING, during the state i.e. MOVING = TRUE.

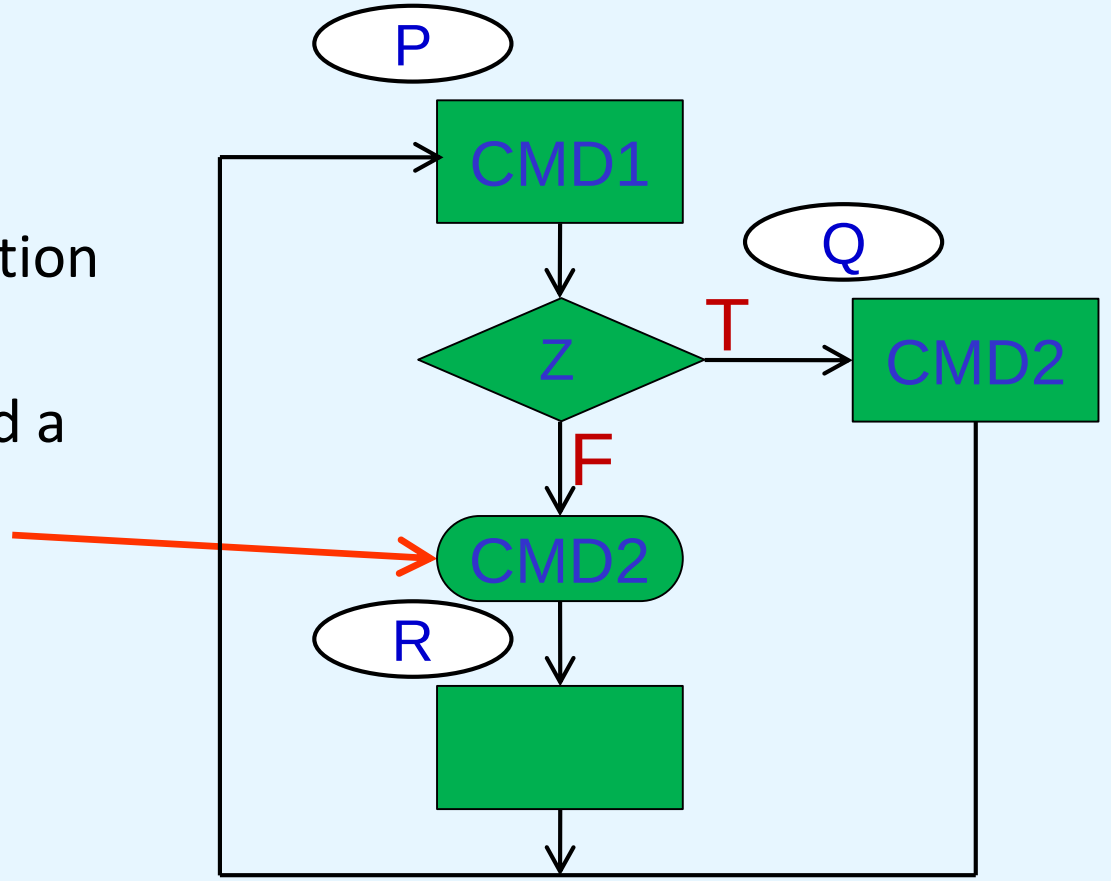
The last line means that the output STATUS is to have the value of the variable ERRFLAG (T or F) during this state.



Conditional Outputs

Sometimes we want a command to occur only when some other condition exists.

We call such a command a conditional output and specify it with an oval.



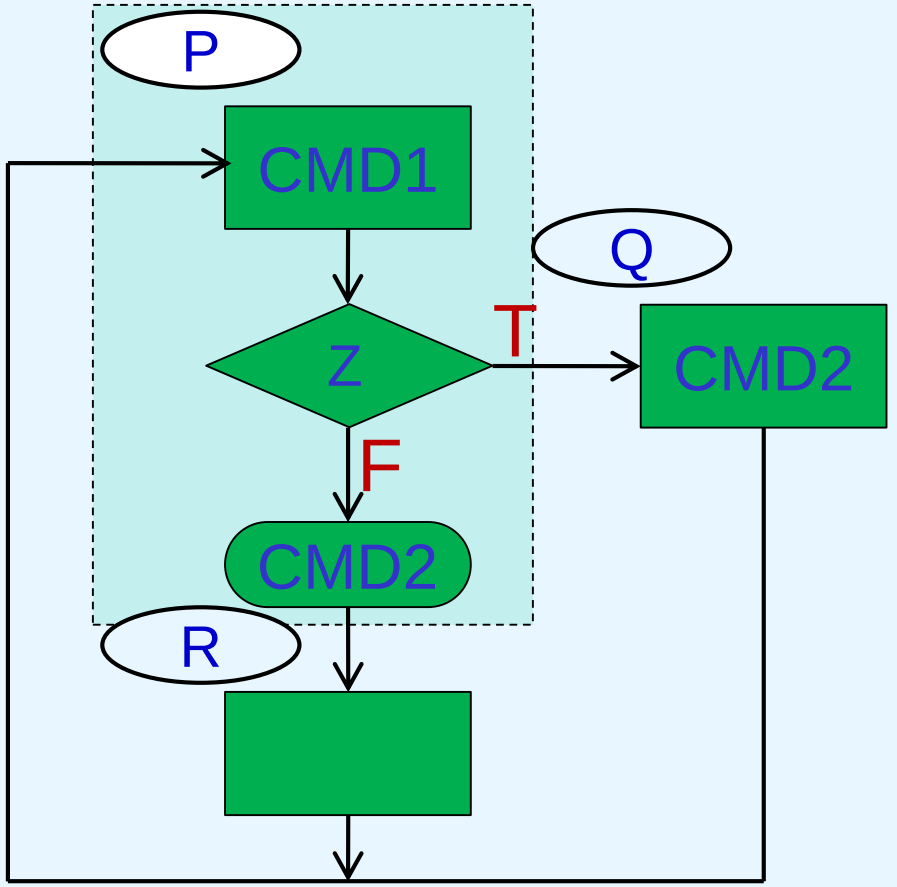
Conditional Outputs

Output CMD1 will be true for one state time whenever the ASM is in state P.

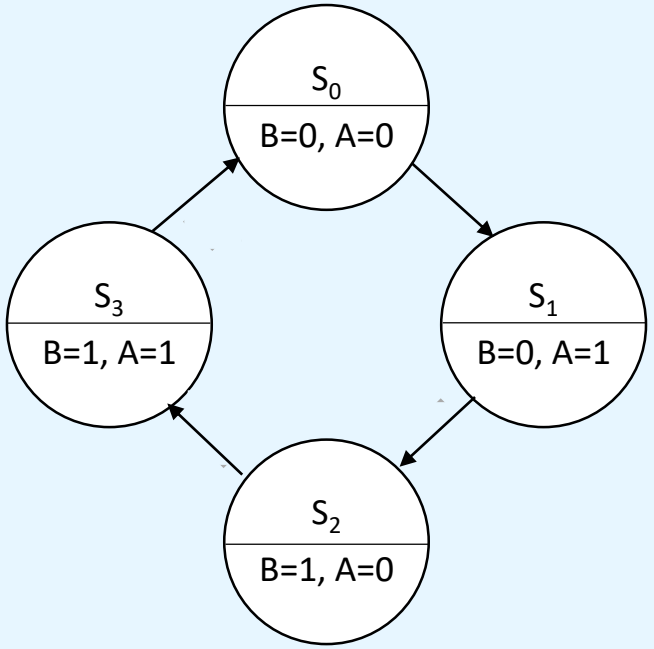
CMD2 will be true for one state time whenever the ASM is in state Q.

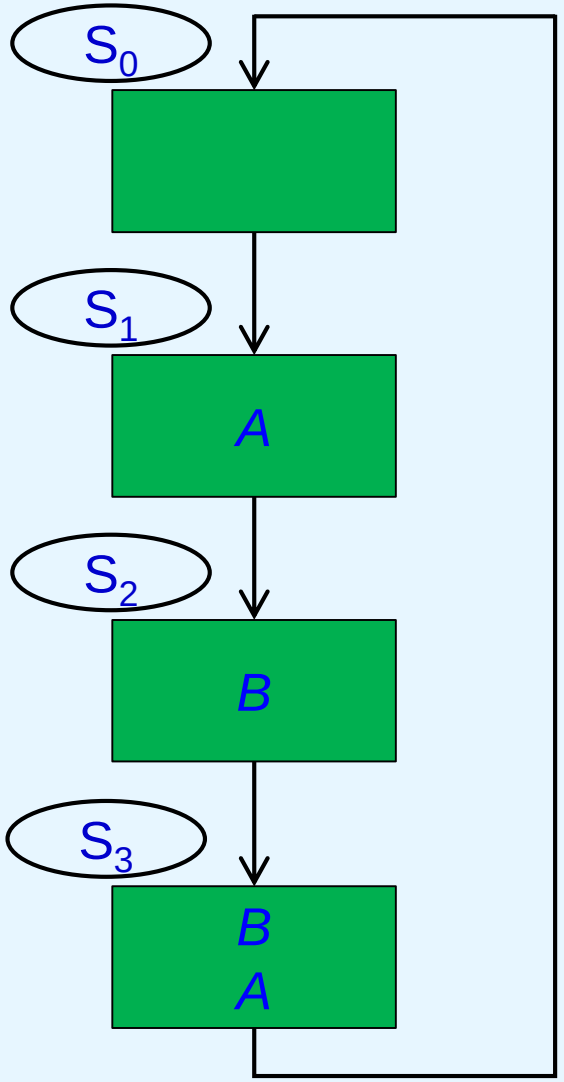
Also, when in state P CMD2 will be true if test input Z is false.

In this example CMD2 is an **unconditional** output in state Q and a **conditional** output in state P.



Very simple example – synchronous binary counter

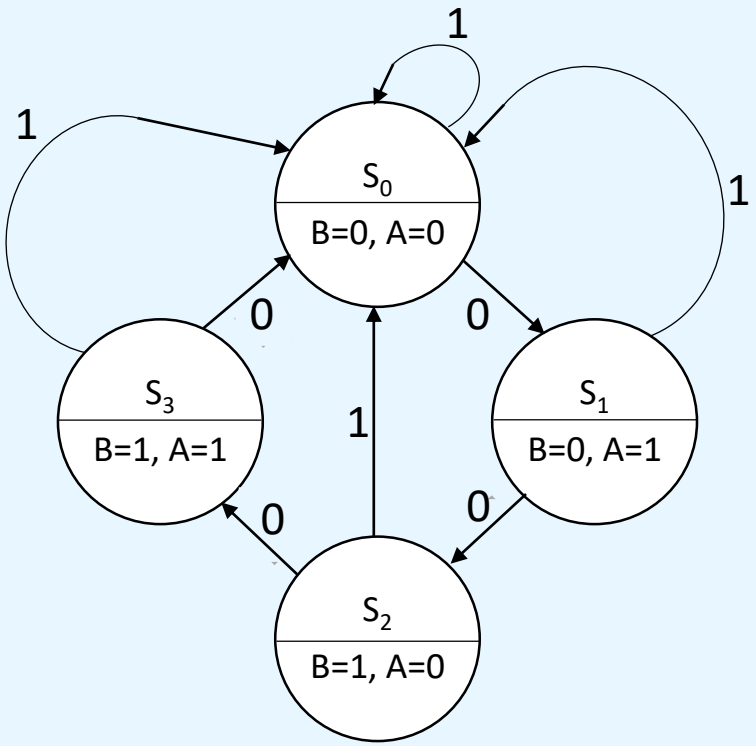


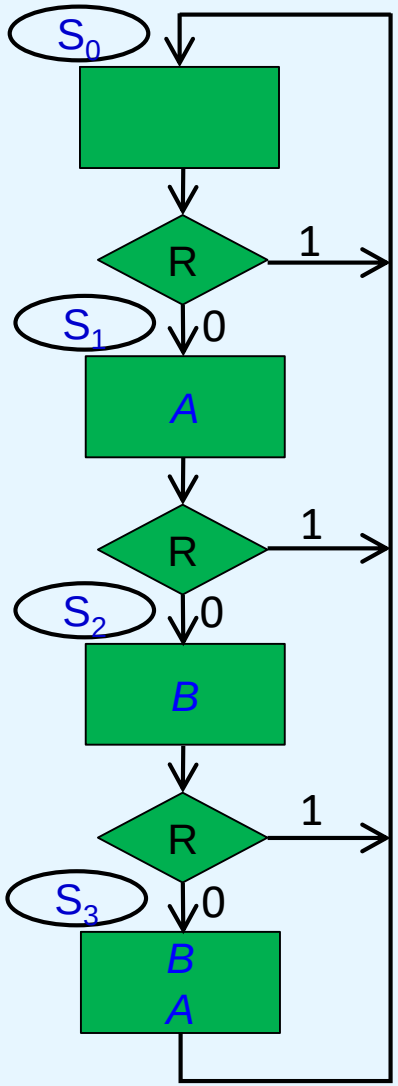


Present State	Next State	Present Outputs	
		B	A
S_0	S_1	0	0
S_1	S_2	0	1
S_2	S_3	1	0
S_3	S_0	1	1

Output bit order: BA

… with a Reset input – Moore machine



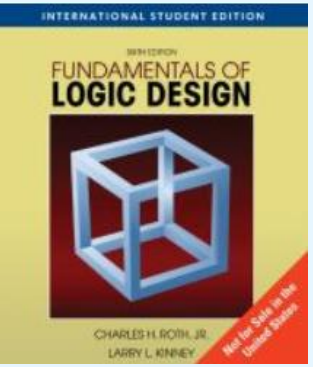


Present State	Next State		Present Outputs	
	R=0	R=1	B	A
S_0	S_1	S_0	0	0
S_1	S_2	S_0	0	1
S_2	S_3	S_0	1	0
S_3	S_0	S_0	1	1

Summary of ASM Symbols

- Test inputs may serve two functions in ASM charts:
  1. They may help specify the next state
  2. They may control the issuing of conditional outputs.
- Ovals for conditional outputs and diamonds for test inputs belong to the parent state; since the activities occur concurrently during the state time.
- A state consists of its rectangle, which is always present, and any test diamonds and conditional output ovals associated with that state.
- Unconditional outputs are a function only of the parent state. Conditional outputs depend on both the state and the path within the state.

Summary and suggested reading



- Section 13.2 Signal tracing & timing charts
- Section 13.2 Moore and Mealy machines
- Section 13.3 State Tables and Graphs

Next lecture:
ASM Charts / One hot state and Encoded state

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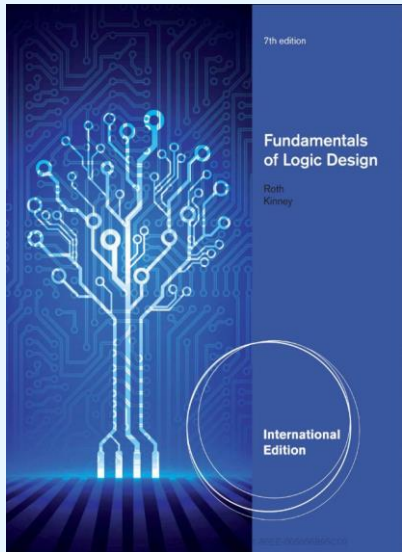

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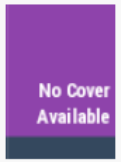

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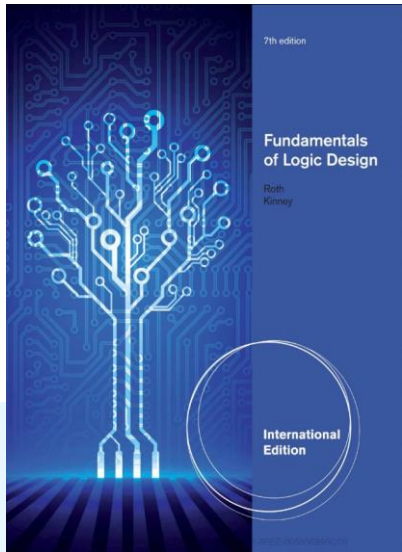

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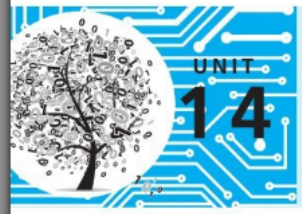

Derivation of State Graphs and Tables

Objectives

1. Given a problem statement for the design of a Mealy or Moore sequential circuit, find the corresponding state graph and table.
2. Explain the significance of each state in your graph or table in terms of the input sequences required to reach that state.
3. Check your state graph using appropriate input sequences.

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