PART 21: Some Op-amp limitations

Although op-amps with negative feedback operate in a practically ideal way, op-amps do suffer from some "non-idealities" or imperfections.

Slew-rate limit

This relates to the ability of the op-amp to respond to a signal; that is, it relates to the **transient response** of the opamp.

Consider a test set-up with a unity gain op-amp circuit subject to application of a large signal – a 5V voltage step.

The output cannot instantly respond to such a signal. Indeed the input of the op-amp is over-driven into a 'saturated' mode (recall the transfer characteristic of the op-amp.) We recall the response of a first order circuit to such a response (**see Part 9**) to be exponential in nature. It turns out however, that op-amps respond in a different manner.

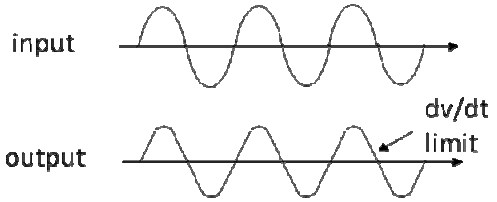
The transient response of an op-amp is in fact **linear** and the gradient is referred to as the **slew rate**. Note that such a response is obtained when a capacitor is charged by a constant current. The capacitor in this case is the large Miller compensation one (C) – see the 741 schematic circuit - the constant current (I) is provided by the current mirror bias circuit at the saturated input stage. Thus we can write:

$$SR \equiv \frac{dV_o}{dt} = \frac{I}{C}$$

For the 741 op-amp C = 30pF and I ~ 19μA giving a SR value of about 0.6V/μs.
Other op-amps have better SRs – up to 10V/ μs)

SR depends on both amplitude and frequency

SR distortion will be apparent from the output waveform



Consider a sine-wave input: $V_i = V_{mi}\sin(\omega t)$

Then $SR = \frac{dV_o}{dt} = \omega V_{mo}\cos(\omega t)$ and $SR = \omega V_{mo} = 2\pi f V_{mo}$ (V_{mo} = Gain * V_{mi})

As long as this value (ωV_{mo}) is less than the SR limit, the output can follow the input.

Example: Assume a 741 with the input amplitude such that the output is the same as the power supply value (10V say), then V_m = 10V. SR = 0.

Equate to slew rate: $\omega V_m = 0.6V/\mu s$ that is, $f = \frac{0.6}{2\pi 10^{-6}}\frac{1}{10}$ = 9.6kHz for the slew rate limited frequency.

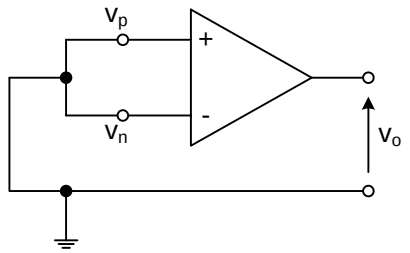
Higher frequency signals would be limited and distorted as in the diagram above.

Exercise: An operation amplifier with a slew-rate limit of 1V/us, is required to amplify a sinusoidal 100kHz signal. Calculate the maximum amplitude of the output voltage that can be achieved without distortion.

Solution: Slew rate = dv_o/dt = 1V/us. For a sinusoidal signal, $v(t) = V_o\sin(\omega t)$; $dv_o/dt = V_o\omega\cos(\omega t) = V_o\omega$ (maximum)
for a signal frequency of 100kHz, then $10^6 = V_o \times 2 \times \pi \times 10^5$ So **V_o = 1.6**

The Voltage Offset

Consider:

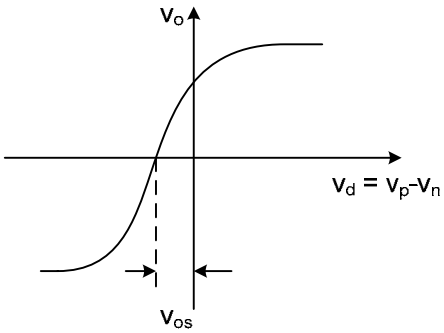


Here $V_p = V_n = 0$ (tied to ground)

So **ideally** we expect: $V_o = A_{ol}\left[V_p - V_n\right] \equiv 0$

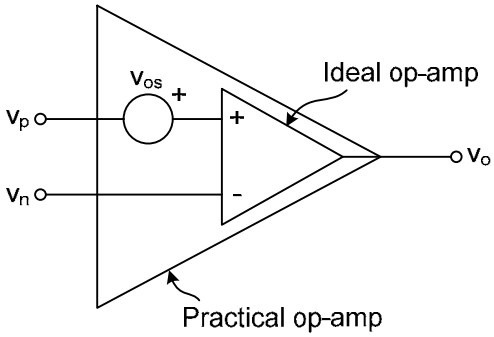
In **practice,** find $V_o \neq 0$

Due to **imbalance** between input stages of op-amp which process V_p and V_n , the VOLTAGE TRANSFER CURVE (VTC) for a real op amp might look like:



There is a **shift** (can be to the left OR right) of the VTC away from the origin – called the "input offset voltage", V_{os}

We can therefore **model** a real op-amp as



NB V_{os} is a DC source – always connected to positive (+ve) input by convention, with polarity shown.
But note V_{os} is equally likely to be positive or negative!

The manufacturer usually gives **magnitude** of V_{os} eg for 741C, $V_{os} = 2mV$ typical, $6mV$ max. This means ~50% of 741C's tested have V_{os} between -2mV to +2mV, but all have V_{os} between -6mV and +6mV.

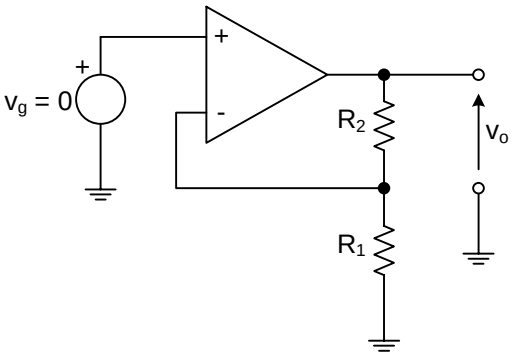
Errors causes by V_{os}

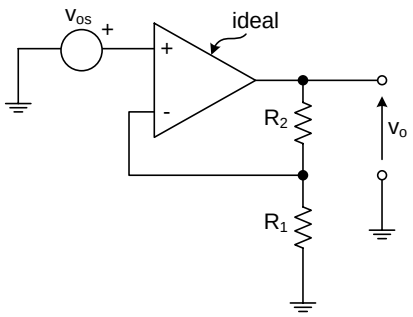
For the non –inverting amp:

We first suppress V_g

To allow us to concentrate on the effect of V_{os}

Replacing real op-amp by its model gives





Which shows that the output is

$$V_o = \left[\frac{R_1 + R_2}{R_1}\right] \times V_{os}$$

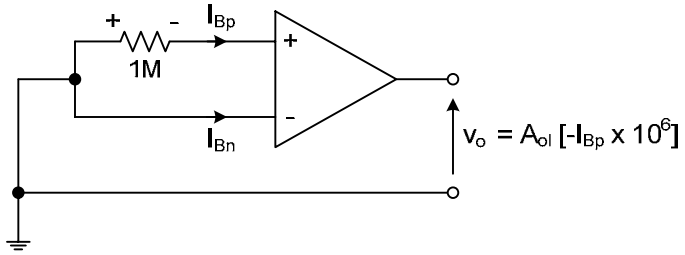
↑
Non-inverting gain

If gain is small, so is output offset V_o; but if $R_2 = 10^3 R_1$, for example, so that gain is ~ 1000, then V_o becomes $\pm 2V$ typical, $\pm 6V$ maximum for a 741C, **not a small error!**

The Current Offset

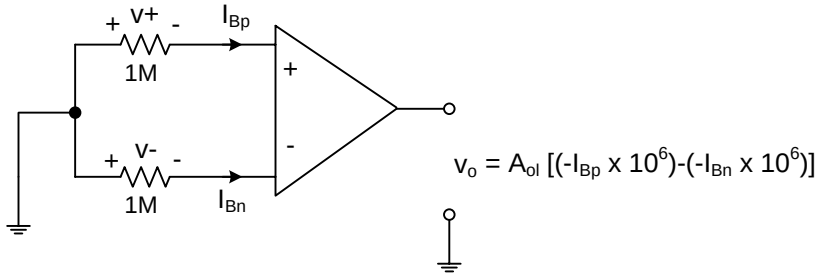
It is always possible by careful selection to find an op-amp with $V_{os} \approx 0$. However even this op-amp would suffer from offset problems – but due to **current offsets**.

Suppose, we take an op-amp with $V_{os} = 0$ and build the following circuit:



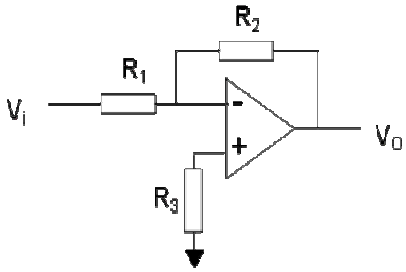
Then, **because input transistors in op-amp MUST be provided with base current in order to operate** - I_{Bp} & I_{Bn} - then a voltage is generated across the $1M\Omega$ resistor which acts as an input to the op-amp, and so it is amplified to give an output, V_o.

We might hope to cure this by putting **two** equal resistors in circuit to restore the balance.



These currents are particularly troublesome because they are temperature dependent – the output voltage drifts.

The effect can be significantly reduced if the circuit is arranged to present the same resistance to both input terminals, for example, in the inverting op-amp circuit, always make $R_3 = R_1 // R_2$. (This will be explored further in the next section.)



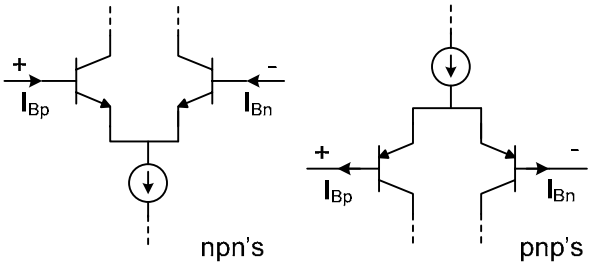
BUT this only works if $I_{BP} = I_{BN}$ which is rarely the case!

The manufacturer, after measuring a large no. of samples, gives us the average base current $I_B = \frac{I_{BP} + I_{BN}}{2}$ which is called the 'input bias current' on data sheets.

AND they give us the magnitude of the difference between I_{Bp} & I_{Bn}

ie. $I_{os} = \left| I_{Bp} - I_{Bn} \right|$ = 'input offset current'

N.B. I_B can be either into op-amp or out of op-amp depending on whether input stage is constructed with npn or pnp transistors:



For a 741C: $I_B = 80\,nA$ *typical* $,500\,nA$ max
$I_{os} = 20\,nA$ *typical* $,200\,n\,A$ max

In the WORST possible case, this means

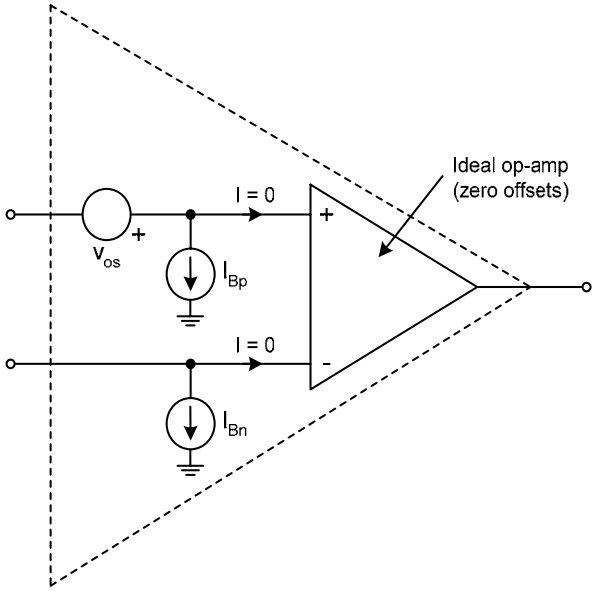
Either $I_{BP} = 600nA,\ I_{BN} = 400nA$ Or $I_{BP} = 400nA,\ I_{Bn} = 600nA$

Summarise this by saying that in all cases $I_B - \frac{I_{os}}{2} < I_{BP} < I_B = \frac{I_{os}}{2}$ AND $I_B - \frac{I_{os}}{2} < I_{Bn} < I_B + \frac{I_{os}}{2}$

Model of a Real Op-Amp including both Voltage and Current offsets

We model current offsets by CURRENT sources:

With current sources of polarity shown, model is of an op-amp with npn input transistors.

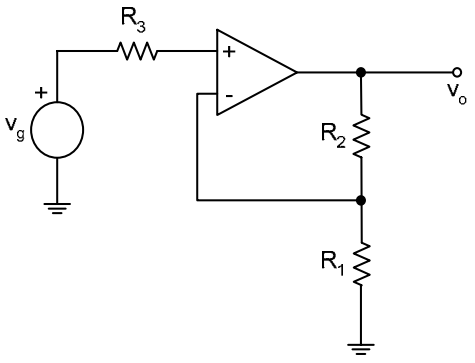


Example: calculation of output offset in general case

Find $V_o =$ for :-

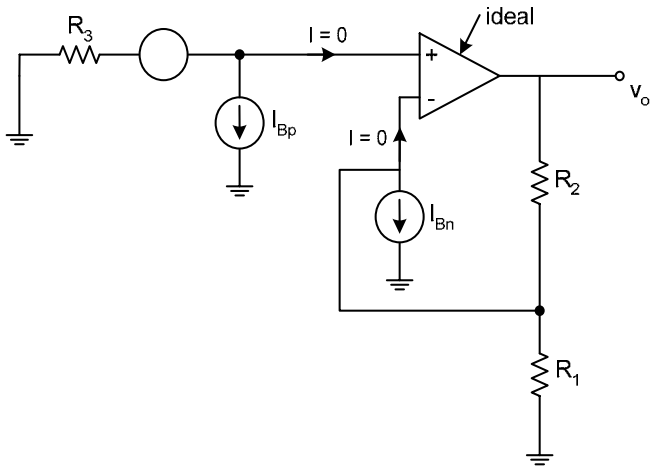
When $V_g = 0$ in WORST CASE

$R_1 = 45k; R_2 = 90k; R_3 = 10k$, and
$V_{os} = 6mV; I_B = 500nA, I_{os} = 200nA$ - all maximum values



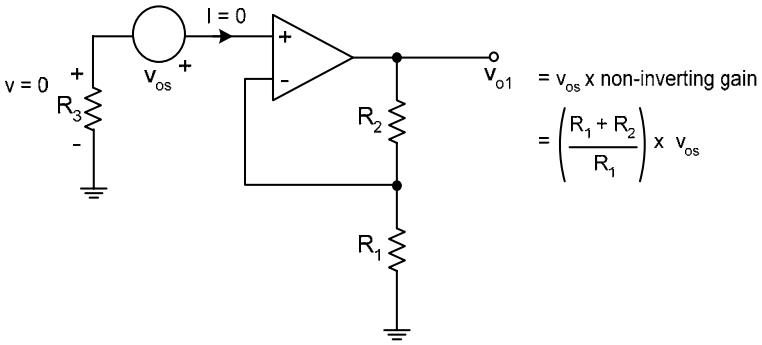
PREPARATION FOR CALCULATION

- suppress V_g ; insert model

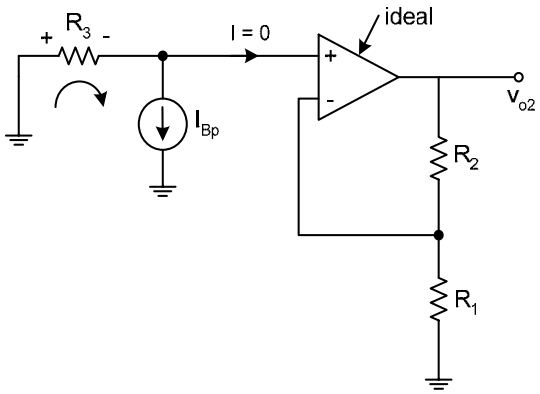


Solution – using principle of superposition

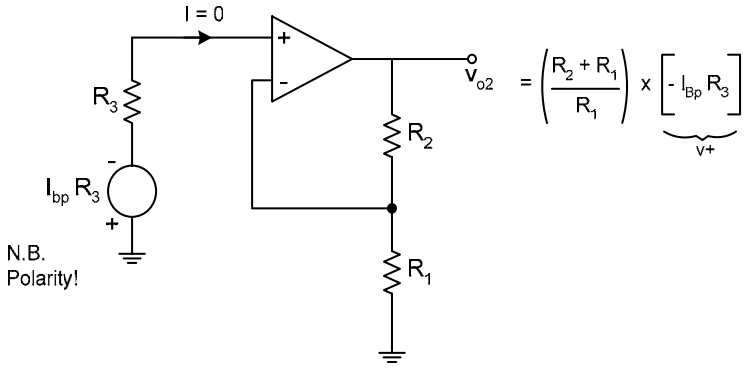
Effect of V_{os} alone



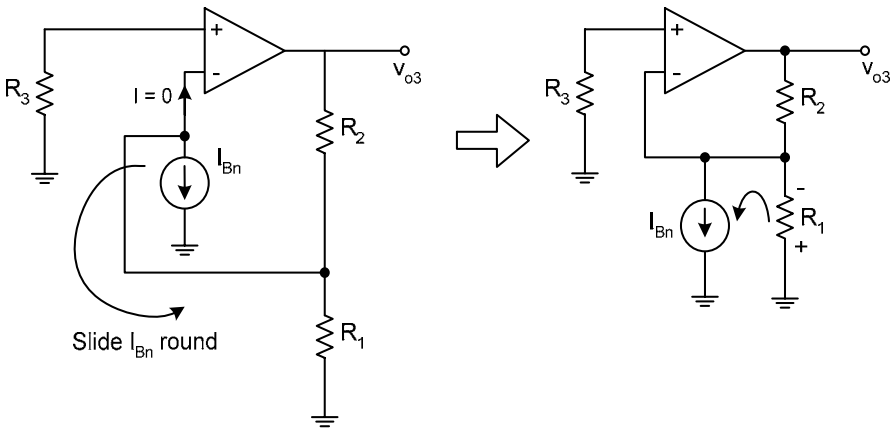
Effect of I_{Bp} alone



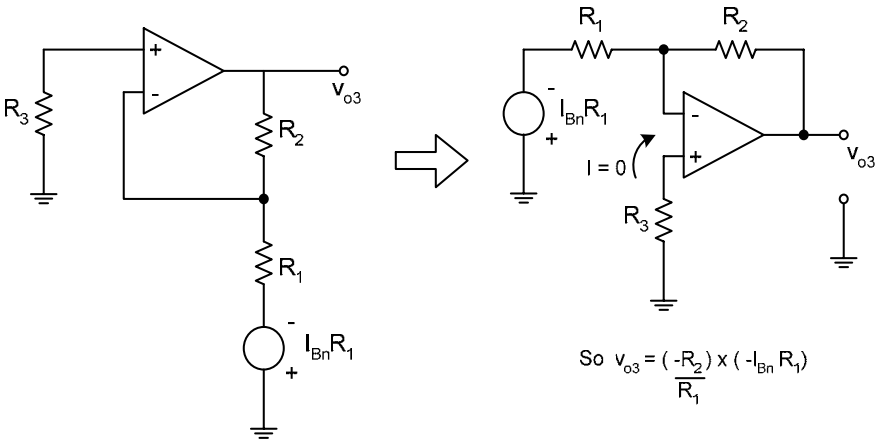
Replacing current source by a voltage source gives:-



Effect of I_{Bn} alone



Now a source transformation:



COMBINING contributions gives $(V_o = V_{o1} + V_{o2} + V_{o3})$

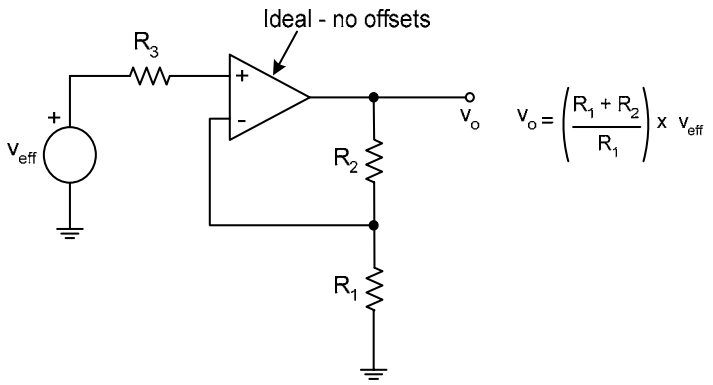
$$V_o = \left(\frac{R_1+R_2}{R_1}\right)\left[V_{os} - I_{Bp}\,R_3\right] + \frac{R_2}{R_1} I_{Bn}\,R_1$$

$$= \left(\frac{R_1+R_2}{R_1}\right)\left[V_{os} - I_{BP}\,R_3\right] + \left(\frac{R_1+R_2}{R_1}\right)\left(\frac{R_1}{R_1+R_2}\right) R_2 I_{Bn}$$

$$= \left(\frac{R_1+R_2}{R_1}\right)\left[V_{os} - I_{Bp}\,R_3\right] + \left(\frac{R_1+R_2}{R_1}\right) R_1 \,||\, R_2\, I_{Bn}$$

$$= \left(\frac{R_1+R_2}{R_1}\right)\left[V_{os} - I_{BP}\,R_3 + R_1 || R_2\, I_{Bn}\right]$$

NOTE we would get SAME OUTPUT from diagram shown opposite



Provided we take

$V_{eff} = V_{os} - I_{BP} R_3 + R_1 || R_2 \, I_{Bn}$

= effective input offset voltage – for this amplifier circuit

CALCULATION OF VALUE OF V_O IN WORST CASE

Gain = $\frac{R_1 + R_2}{R_1} = \frac{45k + 90k}{45k} = 3$

$R_1 || R_2 = 45k || 90k = 30k$ From data sheet: $-6mV < V_{os} < 6mV$ maximum range

And since $I_B - \frac{I_{os}}{2} < \left\{ \frac{I_{BP}}{I_{BN}} \right\} < I_B + \frac{I_{os}}{2}$, Then 400nA $< \left\{ \frac{I_{BP}}{I_{BN}} \right\} < 600nA$

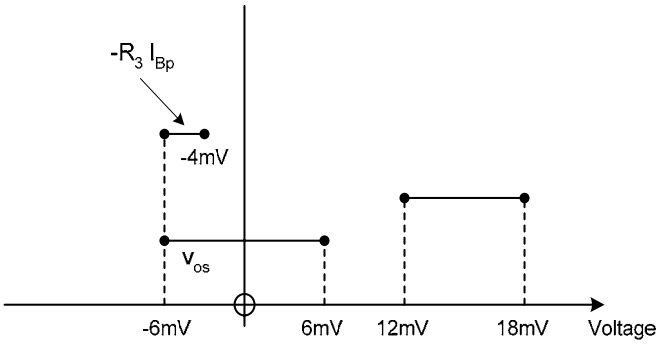
Find V_{eff} first (ie eqn *): $30k \times 400nA < R_1 || R_2 \, I_{Bn} < 30k \times 600nA = 18mV$

(= 12mV)

$10k \times 400nA < R_3 \, I_{Bp} < 10k \times 600nA = 6mV$

(= 4mV)

Combine graphically Draw ranges of each component



MAX NEG value of V_{eff} when each component has max neg. value

$\therefore Max.neg.V_{eff} = -6mV + 12mV - 6mV$ = 0

MAX POS value of V_{eff} when each component has max positive value

So max. possible V_{eff} = $+6mV + 18mV - 4mV$

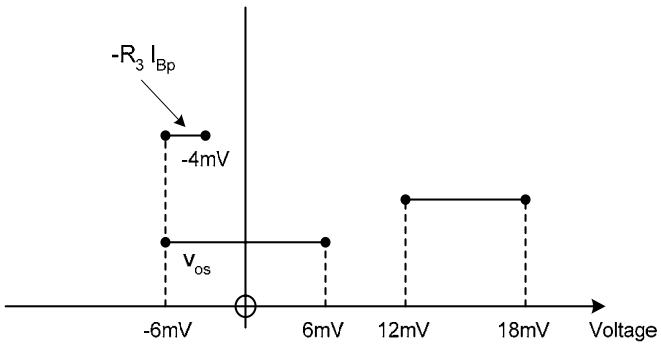
= +20mV

$\therefore$ In **worst case**, V_o lies in range

$0 \le V_o \le 3 \times 20mV$

ie $0 \le V_o \le 60mV$

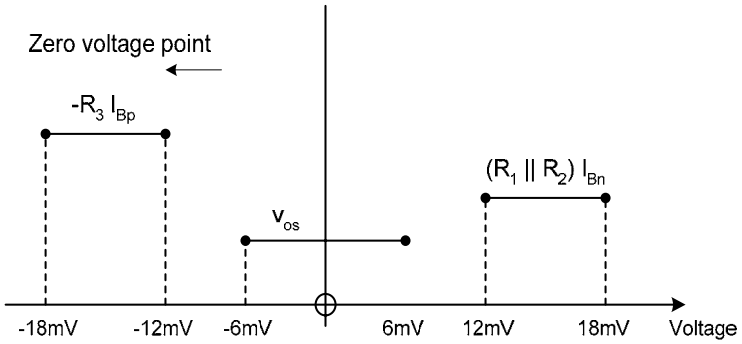
MOST LIKELY value of V_o is mid-way through this range ie V_o (max probable) = 30mV



NB If we can adjust R_3, then chose

$\boxed{R_3 = R_1 \| R_2}$

Since in this case range pattern is symmetrical about zero voltage point



Min V_{eff}	=	-18mV – 6mV +12mV	=	-12mV
Max V_{eff}	=	-12mV + 6mV + 18mV	=	+12mV

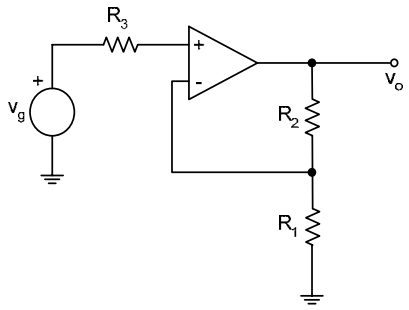
So that output offset voltage is: -36mV $\le V_o \le 36mV$ (for a gain of 3x)

And most likely output offset voltage is zero NB Much better than previous case where there was no possibility at all that V_o could be zero.

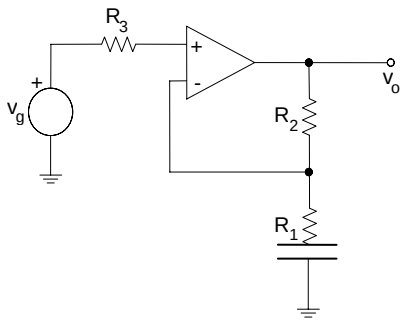
Practical points

It is important to remember that we are dealing here with DC quantities for V_{OS} and I_{Bp} and I_{Bp}. *The analysis must consider only DC paths.* If capacitors are present then the analysis must treat them as OPEN CIRCUIT because they block DC.

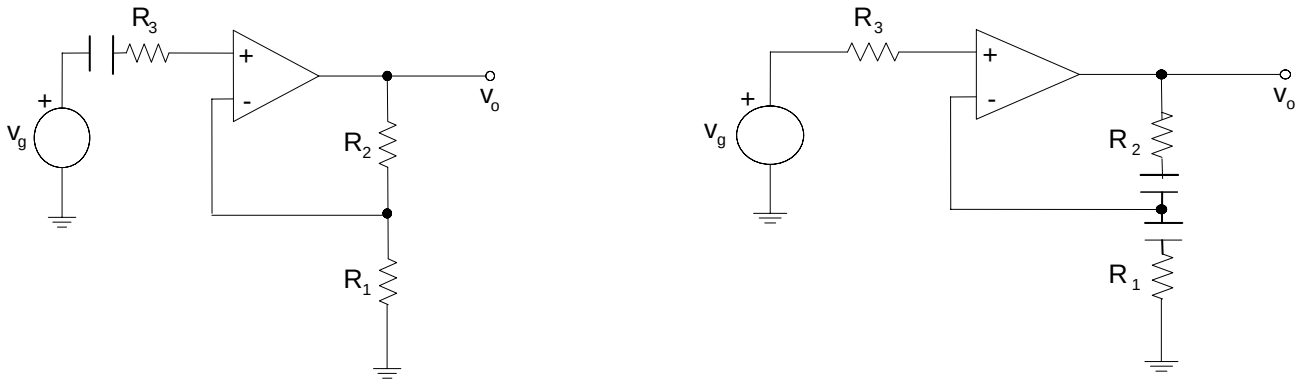
1) In this circuit we make $R_3 = R_1//R_2$ so that the DC paths resistances seen by the bias currents I_{Bp} and I_{Bn} are equal



2) But in this circuit we make $R_3 = R_2$ because the capacitor blocks the DC path through R_1



Note that there will be a problem if no DC paths are provided to one or other of the inputs to allow the bias currents to flow. e.g



The solution would be to place a resistor across at least one of the capacitors, that is large enough not to affect the expected response but small enough to allow the small bias currents to flow without creating a significant DC voltage offset.

End of Module.....