Design example 1

•The following is a 'rough' design with a number of approximations.

• It can be **validated** by PSPICE simulation and fine-tuning of the parameter values undertaken

Specification

- Design a common-emitter amplifier to the following specification
  - V_{CC} = 20V, A_V > 100, V_C ~V_{CC}/2, a load of 10k
- Given
  - β_o =250, make R_1 //R_2 ~ 10xR_{in}, V_{RE} =10%V_{CC}
- Hints
  - First draw the schematic circuit
  - Estimate values for R_C, I_C, R_E, V_B, R_2, R_1

Draw schematic, find R_C, I_C

*** Assume all capacitors are short circuit at frequencies of interest – see later notes for C calculations**

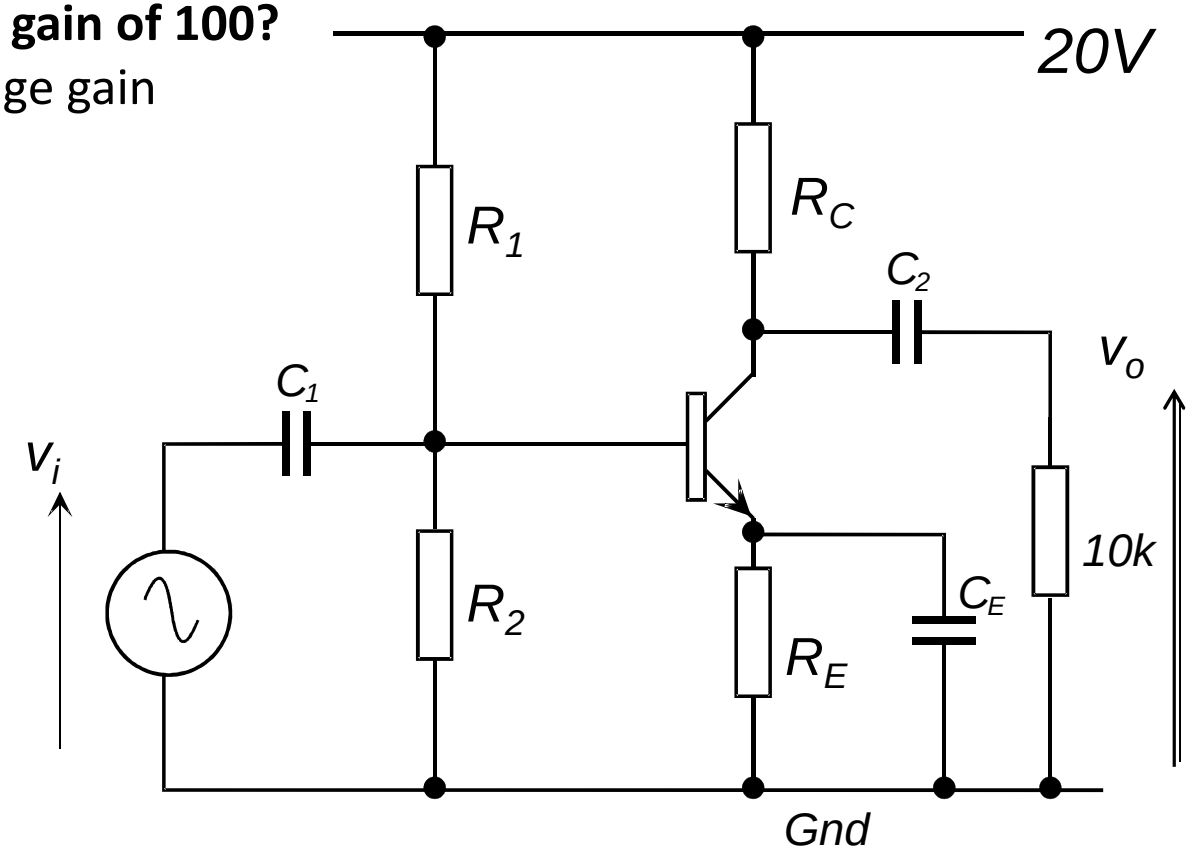
How do we achieve a voltage gain of 100?
What is the equation for voltage gain of a CE amp?

$$\left|A_V\right| \equiv \frac{v_o}{v_i} = g_m \times ac\ \ load$$

$$g_m = 40 I_C$$

$$ac\ \ load = \frac{R_C \times 10k}{R_C + 10k}$$

$$\Rightarrow \quad \frac{A_v}{40.I_C} = \frac{R_C \times 10k}{R_C + 10k}$$



$$\frac{120}{40.I_C} = \frac{R_C \times 10k}{R_C + 10k} \quad \Rightarrow \quad \frac{3R_C}{10} = \frac{R_C \times 10k}{R_C + 10k}$$

$$I_C = \frac{20 - 10}{R_C}$$

R_C = 23k

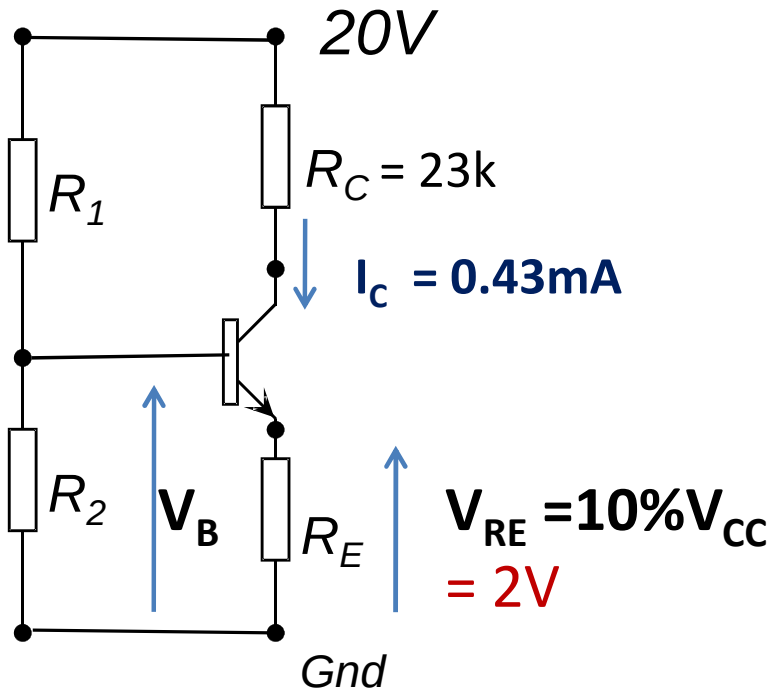
Hence I_C = 0.43mA

Now consider the DC biasing

V_{RE} =10%V_{CC} (stability)

Assume **$I_C \sim I_E$**

$$R_E = \frac{2V}{0.43mA} = 4.7k\Omega$$



Voltage at V_B ?? V_B = 2.6V

How to find R_1, R_2.....

make R_1 //R_2 ~ 10×R_{in}

R_{in} ?

$$R_{in} = r_{be} = \frac{\beta_o}{g_m} = \frac{250}{40 \times 0.43mA} = 14.5k\Omega$$

Now consider the DC biasing

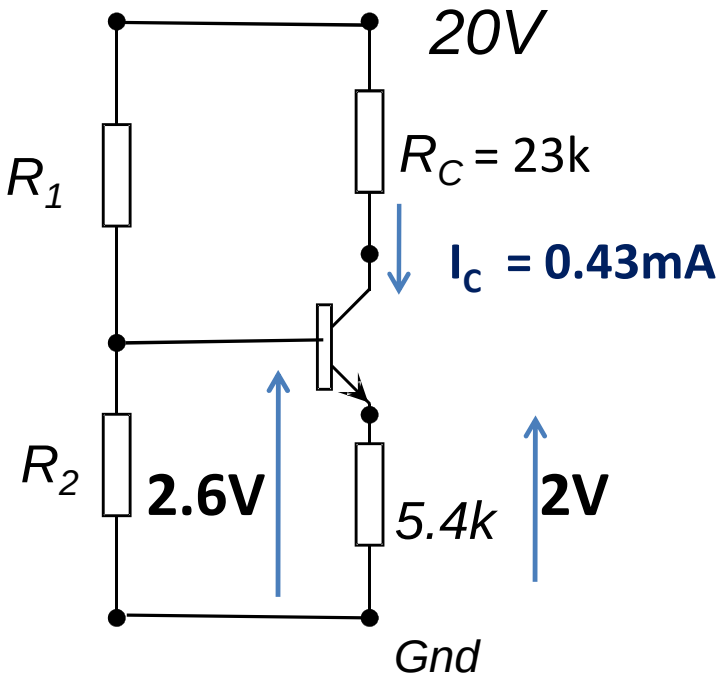
How to find R_1, R_2.....

make R_1 //R_2 ~ 145k

$$\frac{R_1 \times R_2}{R_1 + R_2} = 145k\Omega$$

Need another equation....

Assume DC base current is small (~0) compared to current in bias resistors



$$\Rightarrow \quad \frac{20 - 2.6}{R_1} = \frac{2.6}{R_2} \quad \Rightarrow \quad 17.4R_2 = 2.6R_1$$

Solve 2 equations to give R_1, R_2

R_1 = 1.1MΩ
R_2 = 167kΩ

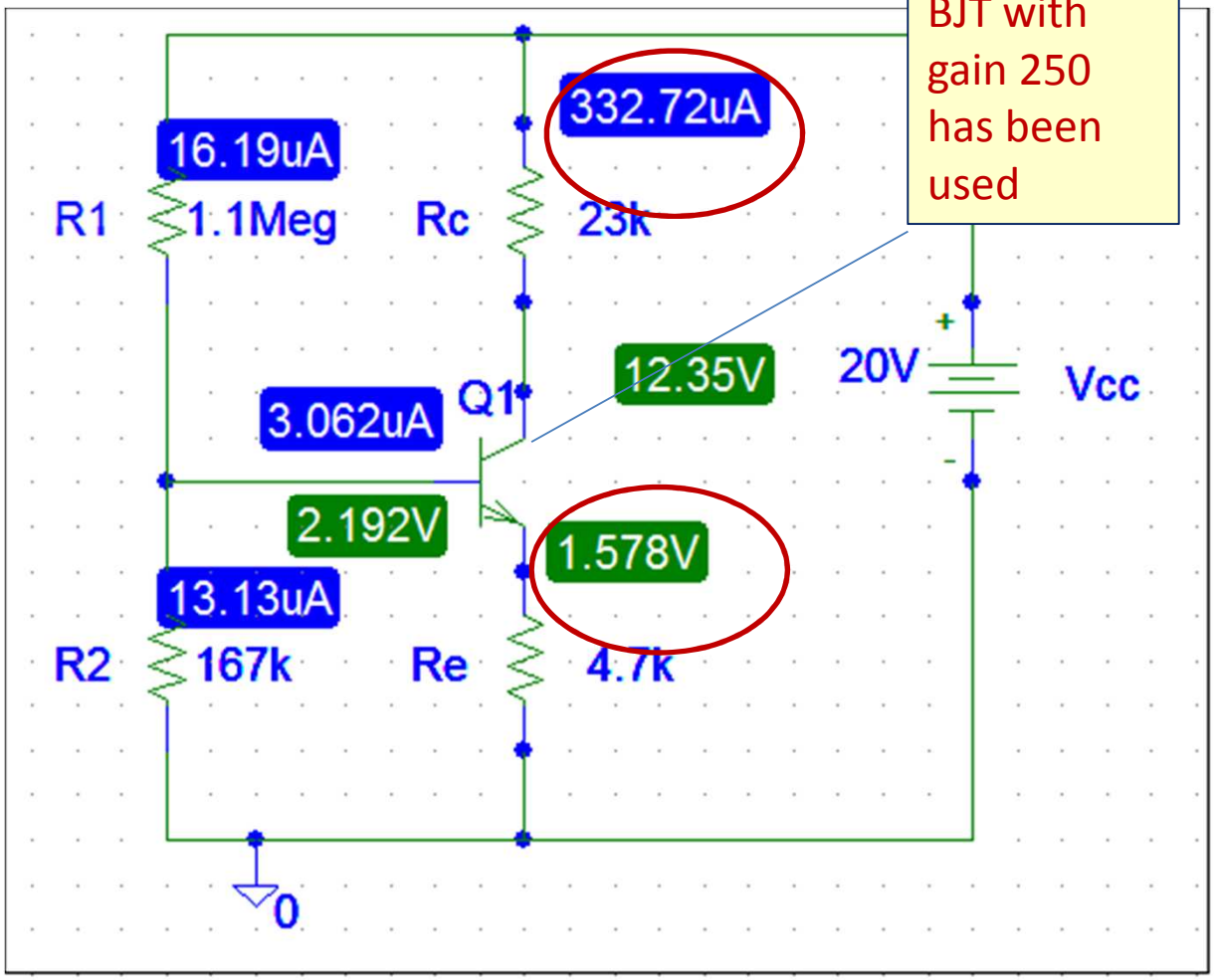
SPICE simulation – DC-1

Check :

- DC levels
- approximations

I_C (spec.) = 0.43mA
I_C (simul.) = 0.33mA

Poor agreement with target I_C = 0.43mA.....

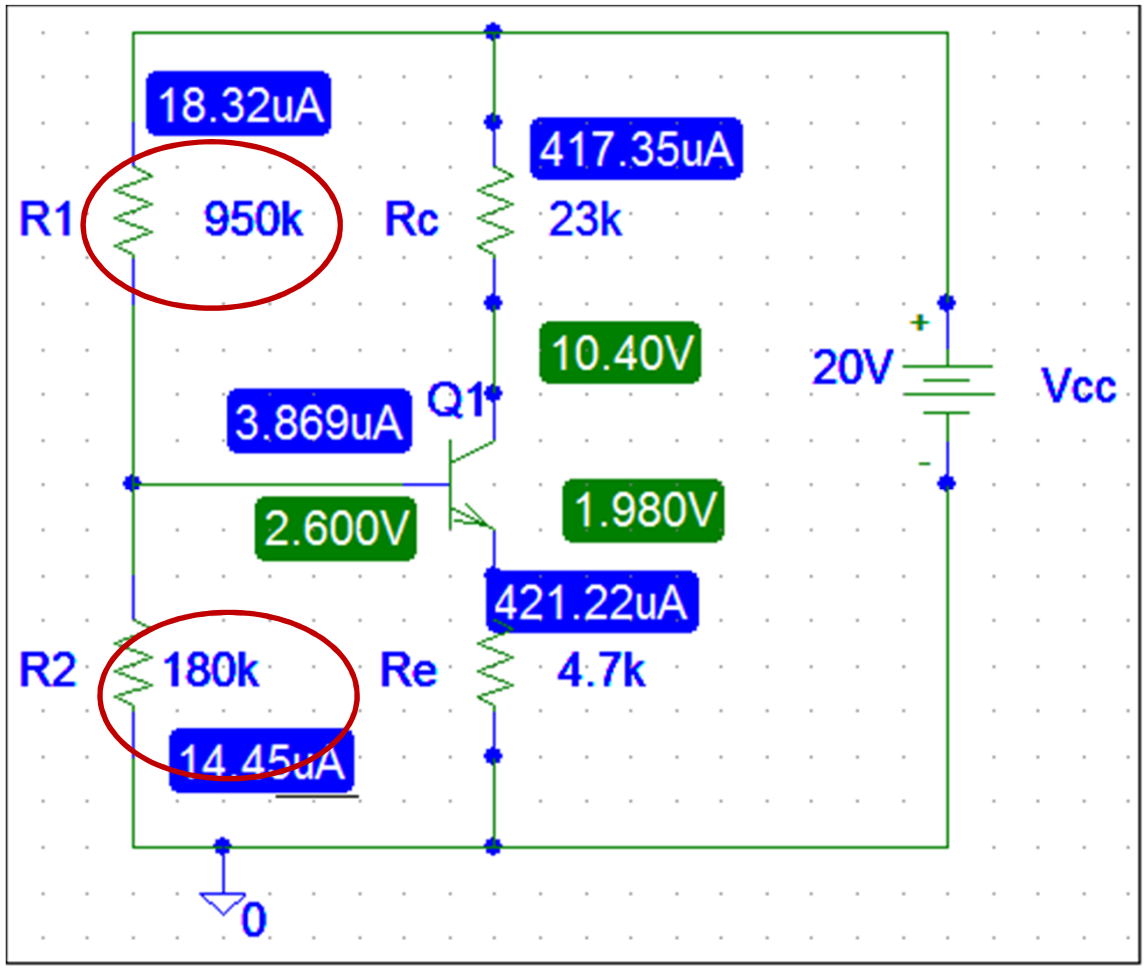


Any ideas Why?? Are the approximations good?

SPICE simulation – DC-2

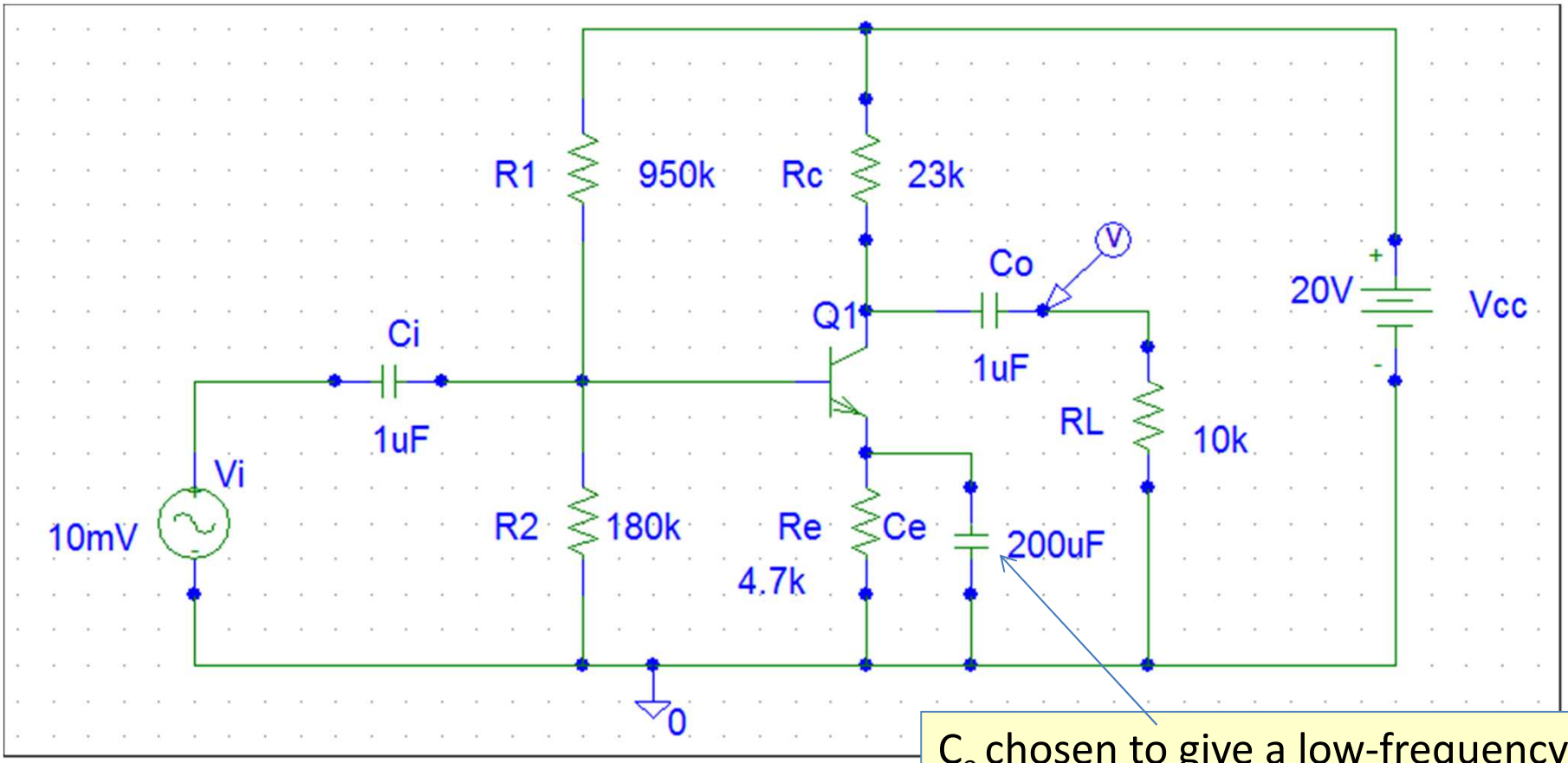
A more rigorous treatment of the estimate for R_1 , R_2 (or a bit of 'tweaking' to get the voltage levels required.. gives

I_C (spec.) = 0.43mA
I_C (simul.) = 0.42mA



Good agreement with target I_C = 0.43mA

Ac simulation

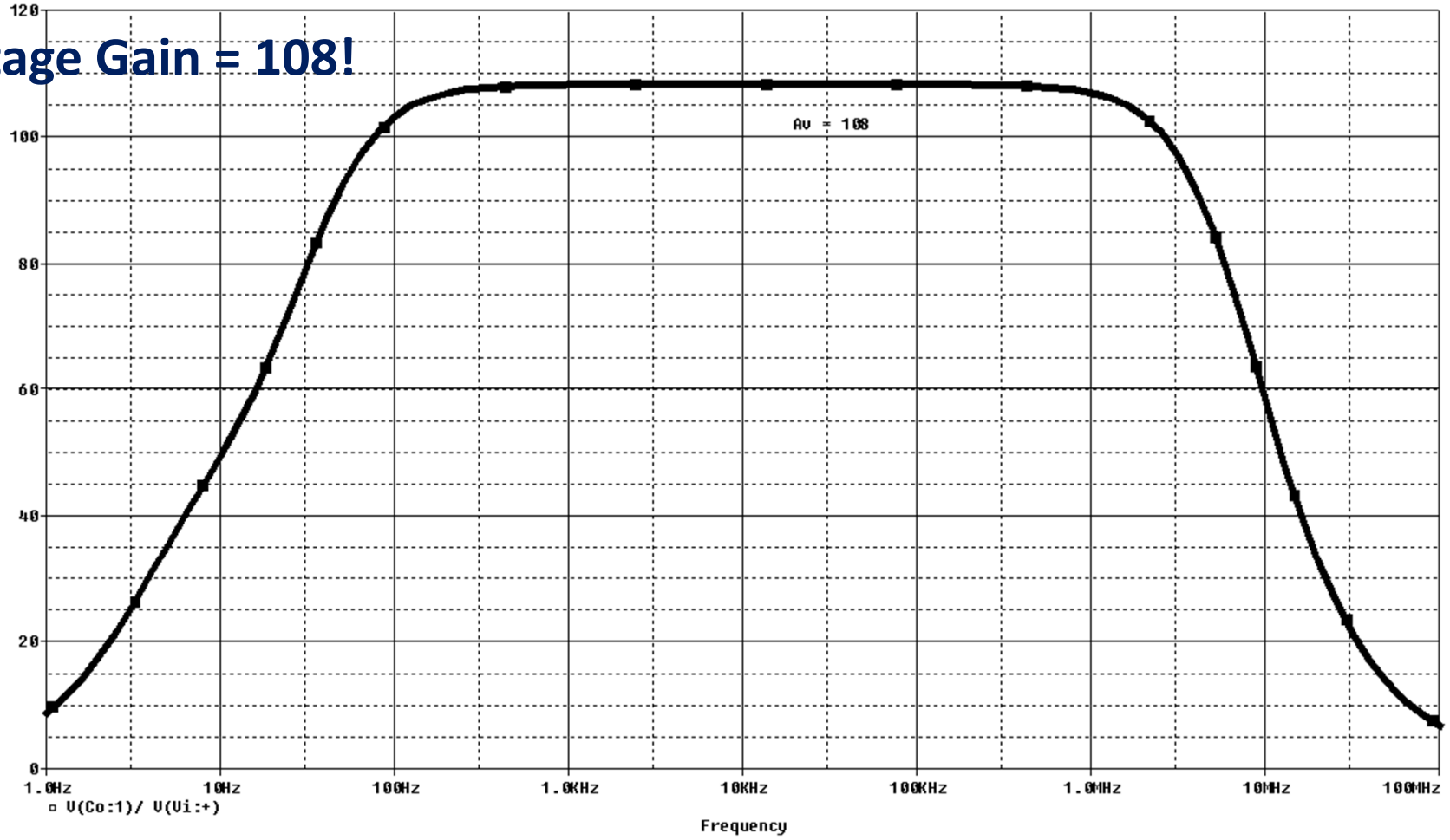


C_e chosen to give a low-frequency roll-off point of 100 Hz

See part 7 for design details for the capacitors, C_i, C_o, C_e

Ac simulation results

Voltage Gain = 108!



$$A_V = g_m \times acload \quad \Rightarrow \quad A_V \approx 40 \times 0.42m \times (23 // 10)k\Omega$$

A_V (theory) = 117
A_V (simul.) = 108

Further work

- Find the nearest preferred values to the resistor values
- Work back through the calculations to find the new values for I_C and A_v

Design Exercise 2

Design a 2-stage voltage amplifier to meet the following criteria:

i) an input resistance of 100 kΩ

ii) an overall voltage gain > 500, into a resistor load, R_L

Given: V_{CC} = 20V, β_o = 200

DC level of the first stage output needs to be set at half the supply voltage.

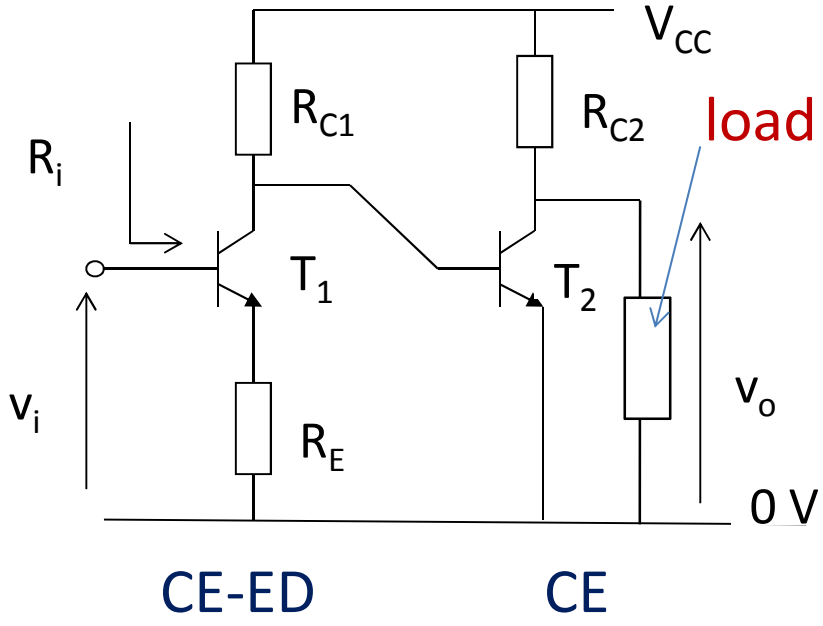
Allow 10% of V_{CC} across R_E)

Use CE-ED (R_E) stage for the input and a CE stage biased at 1mA

Solution.

The schematic circuit

omitting bias resistors and coupling capacitors



Design

First consider input resistance spec.

$$g_m \times r_{be} = \beta_o$$

$$R_i = r_{be1} + (1+\beta_o)R_E$$

10% V_{CC} across R_E

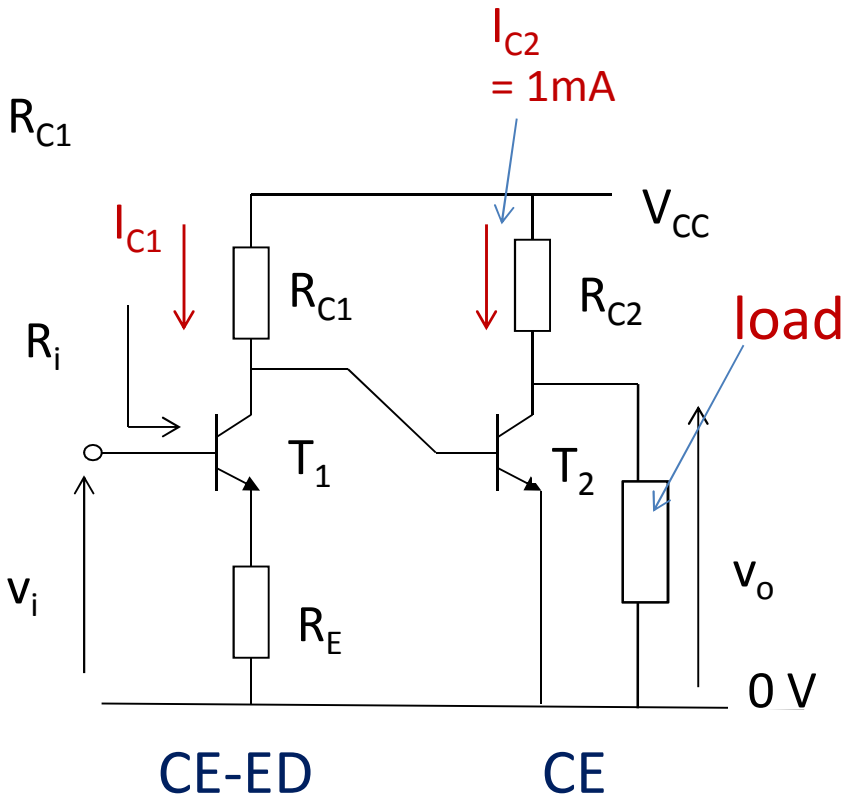
$$\Rightarrow 100k = \frac{200}{40I_{C1}} + (1+200)\frac{2}{I_{C1}}$$

I_{C1} = 4.1mA

V_{CC} /2 across R_{C1}

$$R_E = \frac{2}{4.1m} = 494\Omega$$

$$R_{C1} \sim \frac{20}{2}\frac{1}{4.1m} = 2.5k\Omega$$



Gain of 1st stage is $$A_{V1} = -\frac{g_{m1} \times R_{C1} // R_{i2}}{1 + g_{m1} \times R_E}$$

$$R_{i2} = r_{be2} = \frac{\beta_o}{g_{m2}} = \frac{200}{40 \times 1mA} = 5k\Omega$$

$$A_{V1} = -\frac{40 \times 0.41m}{1 + 40 \times 0.41m}\frac{2.5 \times 5}{2.5 + 5}k$$

$$= 3.31$$

Want total gain to be >500, so A_{V2} = 500 /3.31 = 151; **A_{V2} = 155 say**

Design - 2

Gain of second stage is $A_{V2} = -g_{m2} R_{C2} \,//\, R_L$

$$R_{C2} = \frac{10}{1mA} = 10k\Omega$$

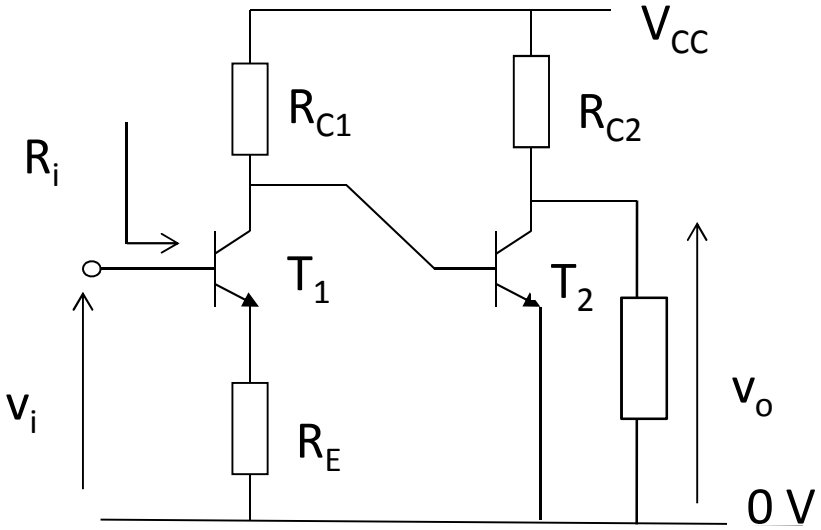
What about R_L ?

$$A_{V2} = -40 \times 1m \times \frac{R_L 10k}{R_L + 10k}$$

$$155(R_L + 10k) = -40m \times R_L \times 10k$$

$$155R_L + 1550k = 400R_L$$

R_L = 6.3 kΩ



This is a MINIMUM value to achieve the desired gain!

Note, use the nearest preferred values in a real design so use R_{in} > 100k, A_V > 500

Gain could be made higher by adding a further CE stage,
Input resistance could be improved by using **feedback**: sacrifice some gain.