Electronic circuits and systems
ELEC271

Part 21
Op-amp limitations

So far have assumed an ideal op-amp:

Input draws no current

Zero output voltage for zero input voltages

Not in fact true! Although OK for doing simple design

Now the truth! ..... And what can be done

Slew-rate limit to bandwidth

SR relates to the ability of the op-amp to respond to a signal;
that is, it relates to the **transient response** of the op-amp.

Part 9: the response, t_{rise} of an ac coupled amplifier should be an **exponential rise** with a time constant related to the upper cut-off frequency, f_H of the amplifier:

$$f_H = \frac{1}{2\pi\tau_r}$$

Op-amps also have a limit on how rapidly the output voltage can change

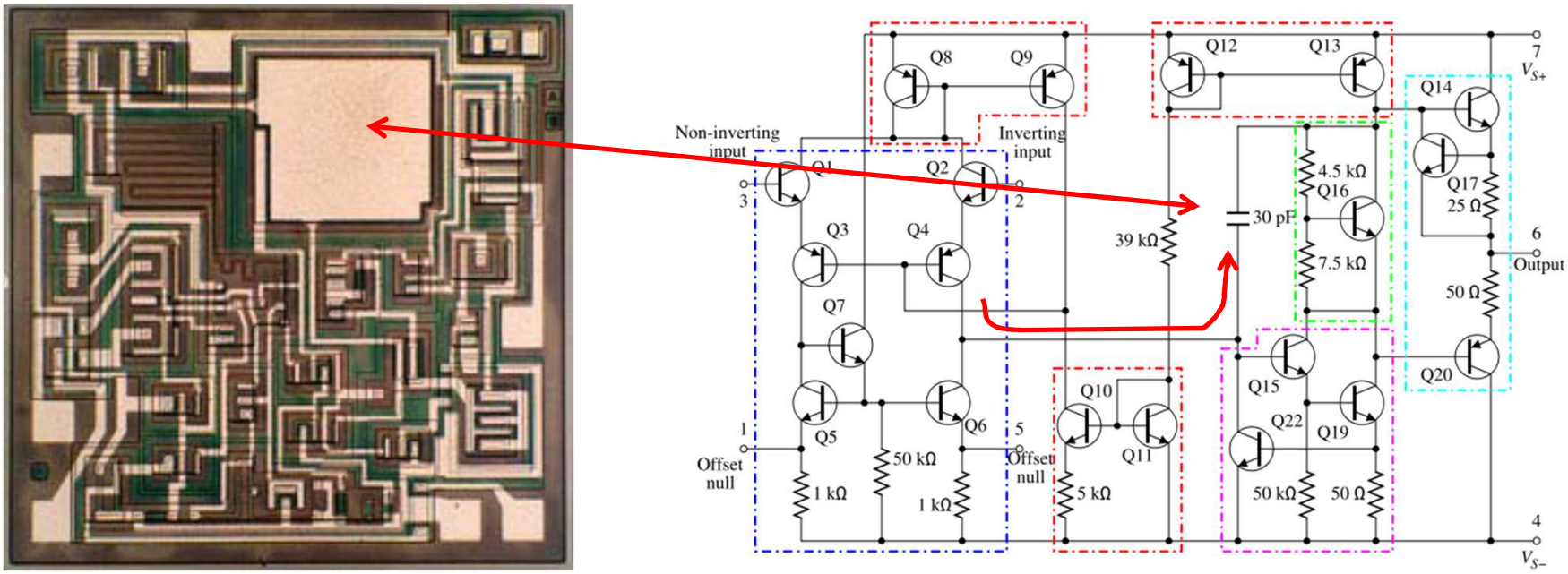
- Transient response of an **op-amp** is **linear -** gradient is referred to as the **slew rate**.
- such a response is obtained when a capacitor is charged by a constant current.
- The capacitor in this case is the large compensation one (C) – see the 741 schematic circuit - the constant current (I) is provided by the current mirror bias circuit at the saturated input stage. So....

$$SR \equiv \frac{dV_o}{dt} = \frac{I}{C}$$

For the op-amp

If the applied signal amplitude exceeds the slew rate limit at some frequency below f_H, then an incorrect estimate of the true bandwidth will be obtained.

Charging of Compensation capacitor



30pF Compensation capacitor charges via a constant current source (current mirror)

Slew rate (contd.)

$$SR \equiv \frac{dV_o}{dt} = \frac{I}{C}$$

For the 741 op-amp C = 30pF and I ~ 19µA giving a SR value of about 0.6V/µs.

Consider a sine-wave input to an op-amp circuit: $V_i = V_m \sin(\omega t)$

Then $\frac{dV_i}{dt} = \omega V_m \cos(\omega t)$ and $\left.\frac{dV_i}{dt}\right|_{\max} = \omega V_m = 2\pi f V_m$

If the value of ($2\pi f V_m$) is **less than** the **SR limit**, the output can follow the input!

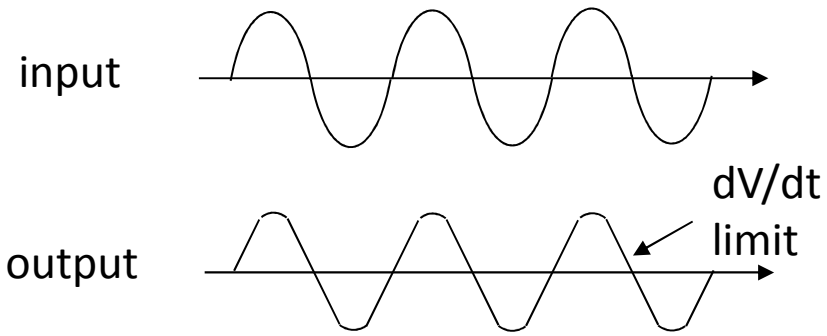
Example: Assume input signal amplitude same as power supply value (10V say),

then V_m = 10V. Now $SR = \omega V_m = 0.6V/\mu s$

that is, $f = \frac{0.6}{2\pi \times 10^{-6}} \frac{1}{10}$ = 9.6kHz for the slew rate limited frequency of a 10 V amplitude signal

Higher frequency signals would be limited and distorted.

A slew rate limited output will be apparent from the shape of the output waveform



Unlike the upper bandwidth limit, the frequency at which the slew rate limit is reached depends on the **amplitude of the output signal as well as its frequency.**

Exercise: An operation amplifier with a slew-rate limit of 1V/us is required to amplify a sinusoidal 100kHz signal. Calculate the maximum amplitude of the output voltage that can be achieved without distortion.

Solution

Slew rate = dv_o/dt = 1V/us

For a sinusoidal signal, $v(t) = V_o\sin(\omega t)$; $dv_o/dt = V_o\omega\cos(\omega t) = V_o\omega$ (maximum)

for a signal frequency of 100kHz, then: $10^6 = V_o\ 2 \times \pi \times 10^5$

$$SR = V_o 2\pi \times f$$

So **V_o (max) = 1.6 V (so to avoid SR limiting, ensure V_o < 1. 6V)**

Part 21
Op-amp limitations (contd.)

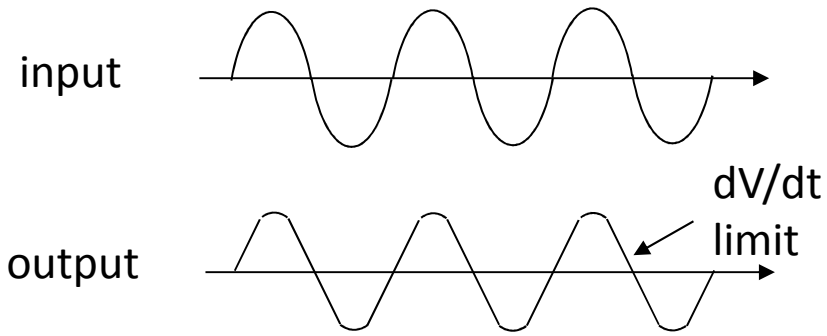
So far have assumed an ideal op-amp:

Input draws no current

Zero output voltage for zero input voltages

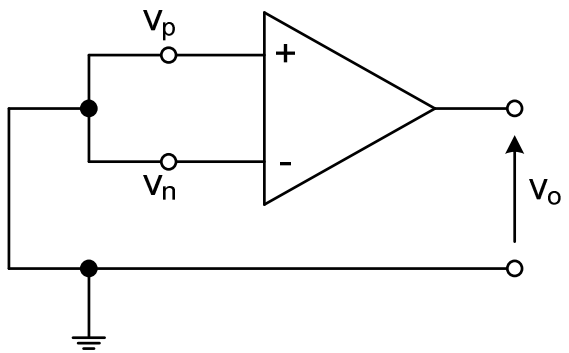
Not in fact true! Although OK for doing simple design

Last time: slew rate – need to consider dynamic response (time domain) – 741 – 0.6V/µs



The Voltage Offset

Consider an experiment:

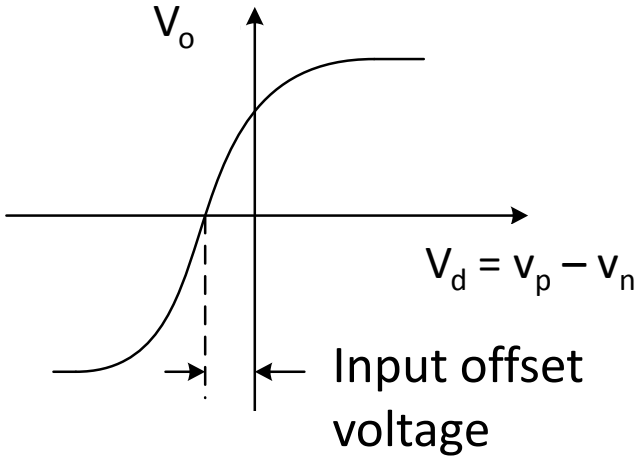


Here $V_p = V_n = 0$ (tied to ground)
So **ideally** we expect:

$$V_o = A_{ol}\left[V_p - V_n\right] \equiv 0$$

However, in **practice,** we usually find $V_o \neq 0$

This is due to **an imbalance** between input stages of the op-amp which process V_p and V_n resulting in the **VOLTAGE TRANSFER CURVE (VTC)** for a real op amp being displaced from the origin:



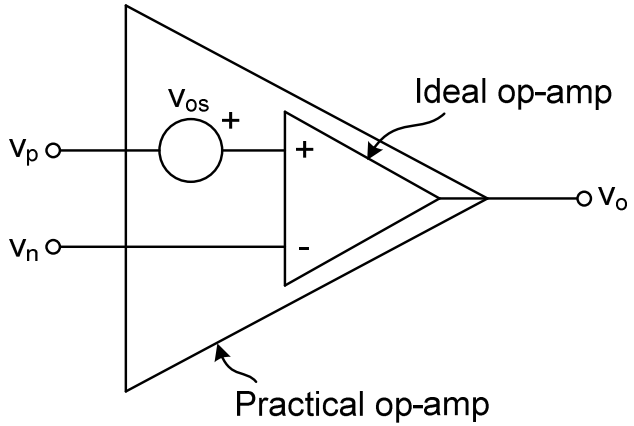
There is a **shift**

can be to the left OR right of the VTC away from the origin

– called the "**input offset voltage**",

How to model the offset

We can therefore **model** a real op-amp as



N.B. $\mathbf{V_{OS}}$ is a DC source **referenced to the input** – it is always connected to the positive (+ve) input **by convention**, with polarity shown.
But note that it is equally likely to be a positive or negative value!
It is the equivalent input voltage that would need to be applied (as shown) to make $V_O = 0$

The manufacturer usually gives the **magnitude** of V_{OS} - eg for 741C,

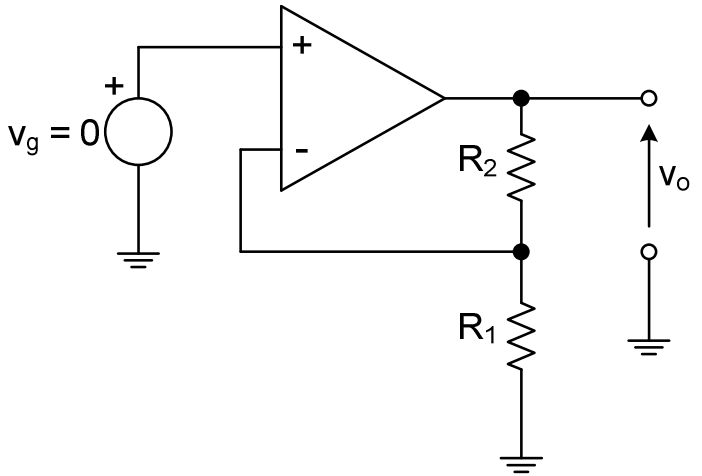
V_{OS} = 2mV typical, 6mV max.

This means ~50% of 741C's tested have V_{OS} between -2mV to +2mV,
but all have V_{OS} between -6mV and +6mV.

What error is caused by V_{OS} ?

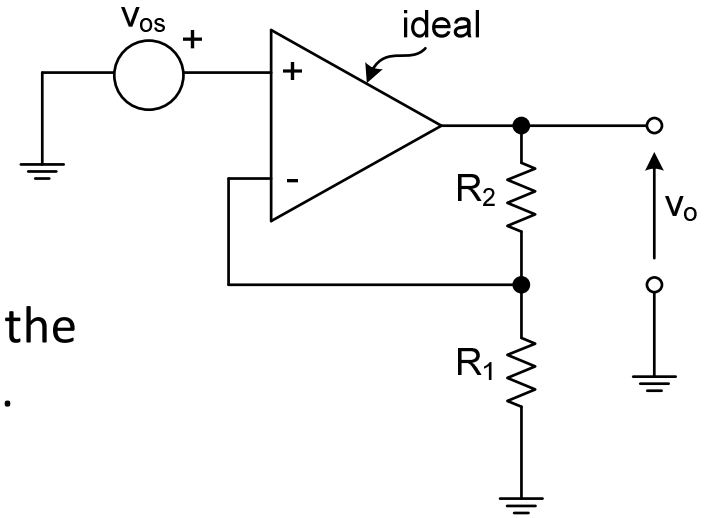
e.g. For the non –inverting amp:

We first suppress Vg to allow us to concentrate on the effect of V_{OS} alone



Replacing real op-amp by its model gives

$$V_o = \left[\frac{R_1 + R_2}{R_1}\right] \times V_{os}$$



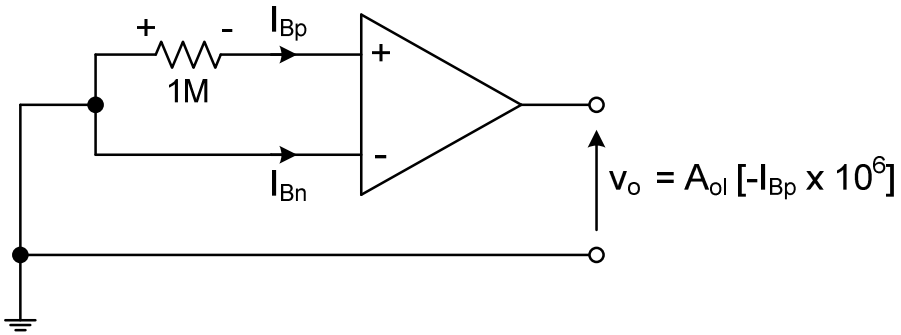
So the offset voltage is amplified by the gain of the amplifier to produce a DC output offset voltage.

If the gain is small, so is the output offset ;

but if, for example, the gain is ~ 1000, then V_{OS} becomes ±2V typical, ±6 V max for a 741C, **not a small error!**

The Current Offset (1)

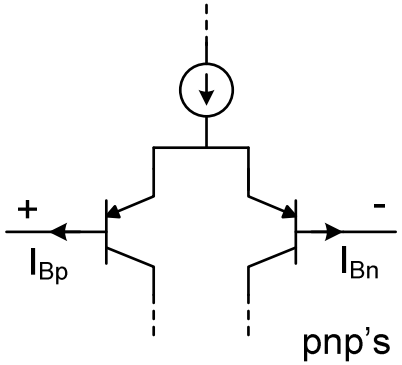
Suppose, we take an op-amp and build the following circuit:

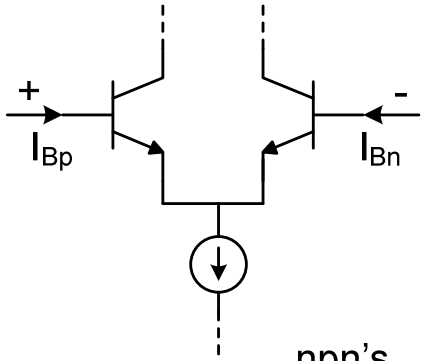


Input transistors in the **op-amp MUST be provided with base current** in order to operate (I_{Bp} and I_{Bn})

→ a voltage is generated across the 1MΩ resistor which acts as an input voltage to the op-amp, and so it is amplified to give a DC output V_O.

N.B. the input bias currents can be either into op-amp or out of op-amp depending on whether input stage is constructed with npn or pnp transistors:

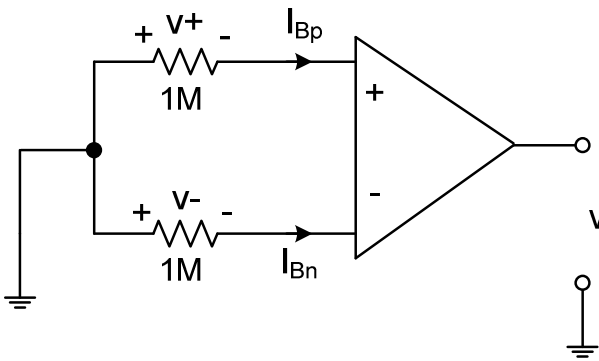




The Current Offset (2)

These currents are particularly troublesome because they are **strongly temperature dependent** – so ***the output voltage drifts***

The effect can be significantly reduced if the circuit is arranged to present the same resistance to both input terminals

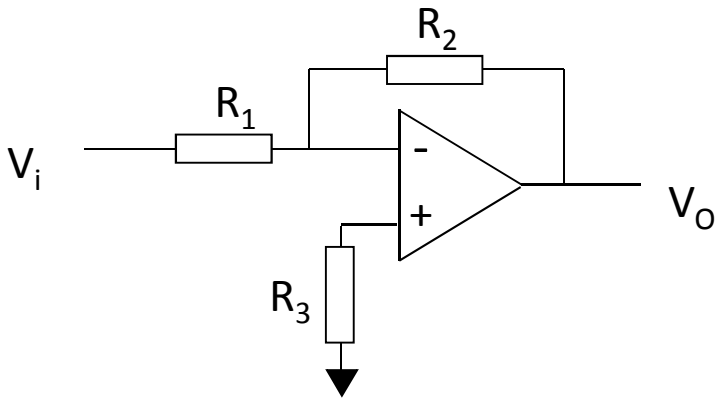


So now we are only concerned with the **difference** between the two currents I_{Bp} and I_{Bn}

$$v_o = A_{ol}\,[(-I_{Bp} \times 10^6)-(-I_{Bn} \times 10^6)]$$

$$V_O = A_v\,(I_{Bp} - I_{Bn}) \times 1M$$

For example, in the inverting op-amp circuit, always make $R_3 = R_1//R_2$



* Practical tip

Data Sheets

The manufacturer, after measuring a **large number of samples**, gives us the average base current

$$I_B = \frac{I_{Bp} + I_{Bn}}{2}$$

which is called the **'input bias current'** on **data sheets.**

AND they give us the magnitude of the offset current difference

$$I_{os} = \left| I_{Bp} - I_{Bn} \right| =$$ **'input offset current'**

$$I_{Bn} = I_B - \frac{I_{os}}{2}$$

$$I_{Bp} = I_B + \frac{I_{os}}{2}$$

For a 741C:

I_B = 80nA typical, 500nA max
I_{os} = 80nA typical, 200nA max

In the WORST possible case, this means either $I_{Bp} = 600nA,\ I_{Bn} = 400nA$

or $I_{Bp} = 400nA,\ I_{Bn} = 600nA$

Summarise this by saying that in all cases

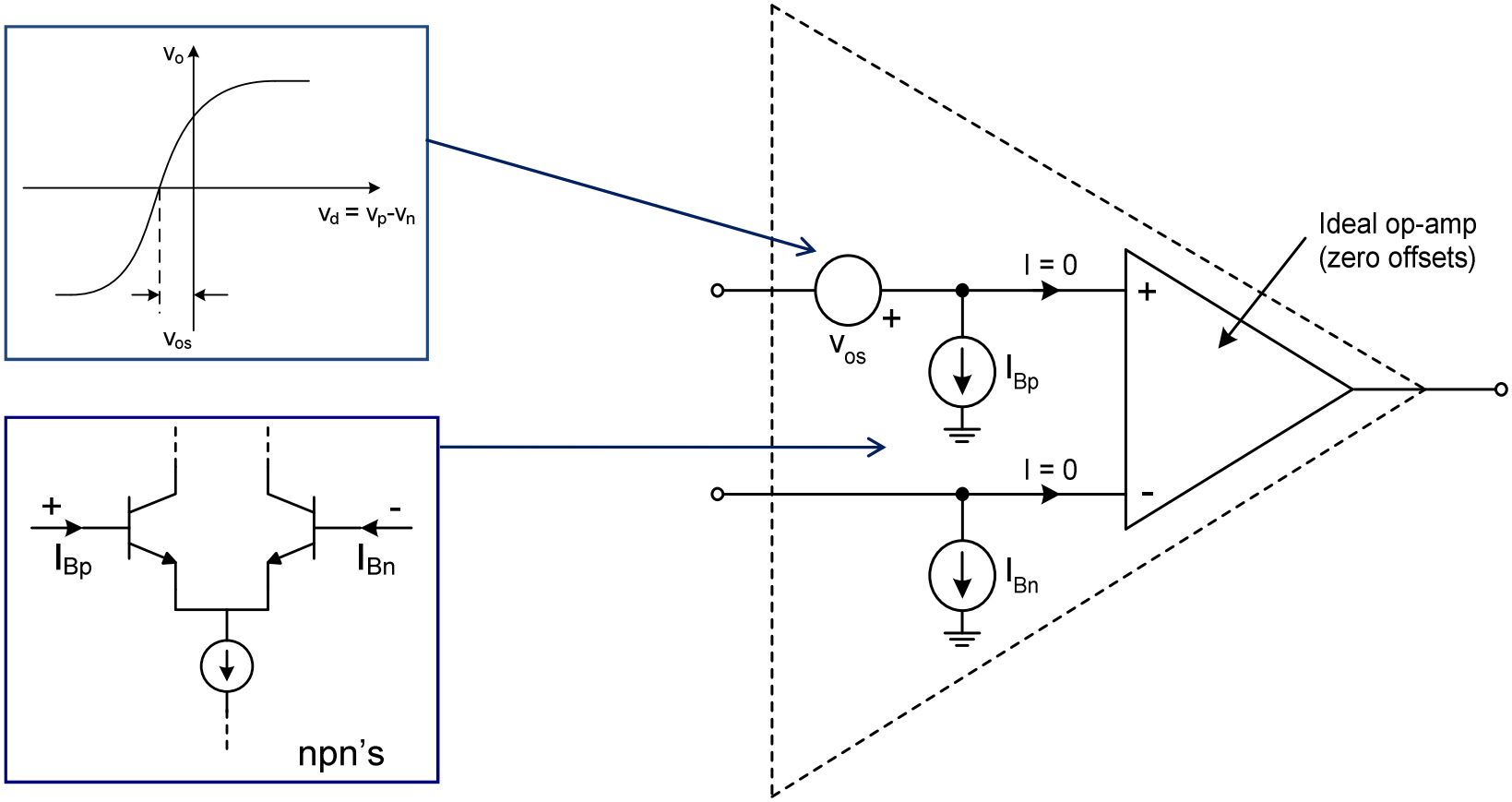
$$I_B - \frac{I_{os}}{2} < \left[I_{Bn}\ , I_{Bp} \right] < I_B + \frac{I_{os}}{2}$$

Model of a Real Op-Amp including both Voltage and Current offsets

We model current offsets by CURRENT sources:

With current sources of polarity shown, model is of an op-amp with npn input transistors.

Also, the voltage off-set voltage source is added to give the complete model



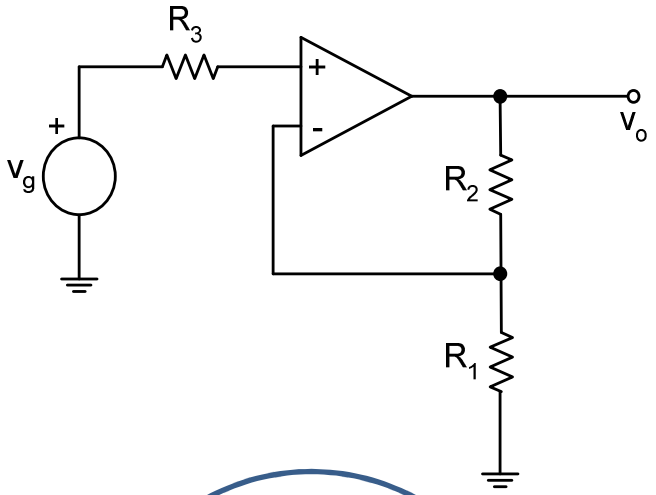
Example: calculation of output offset in general case

Find V_O when

$$R_1 = 45k \quad R_2 = 90k \quad R_3 = 10k$$

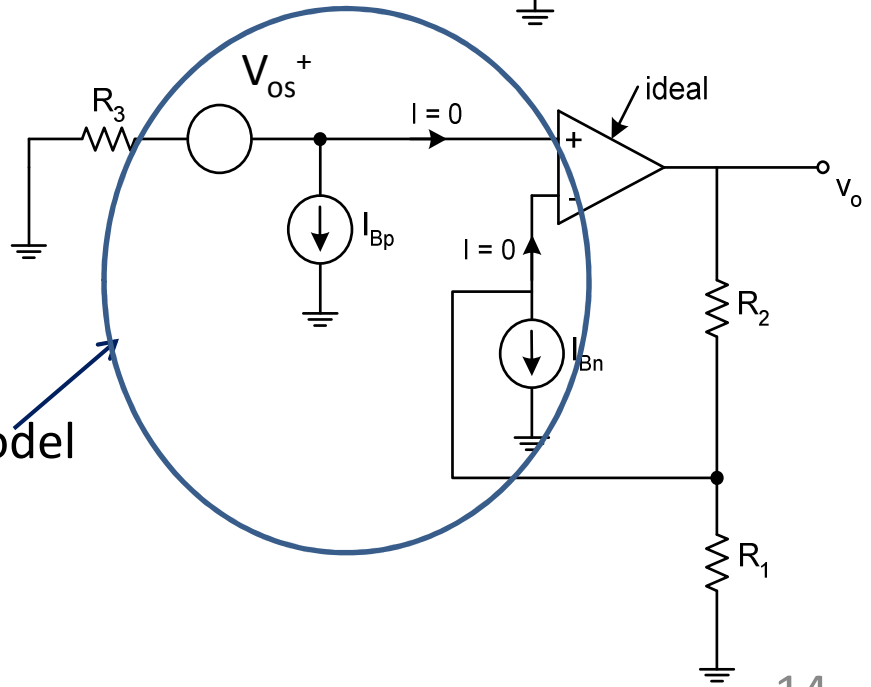
Given that

$$V_{os} = 6mV; I_B = 500nA, I_{os} = 200nA$$



PREPARATION FOR CALCULATION

suppress V_g and insert model

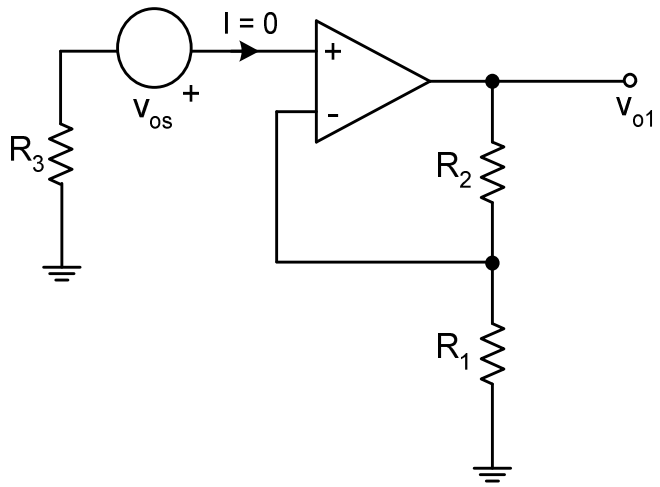


Solution: find effect on output of all 'parasitic' sources

– use principle of superposition

Effect of V_{OS} alone is

$$V_{o1} = \left[\frac{R_1 + R_2}{R_1} \right] \times V_{os}$$

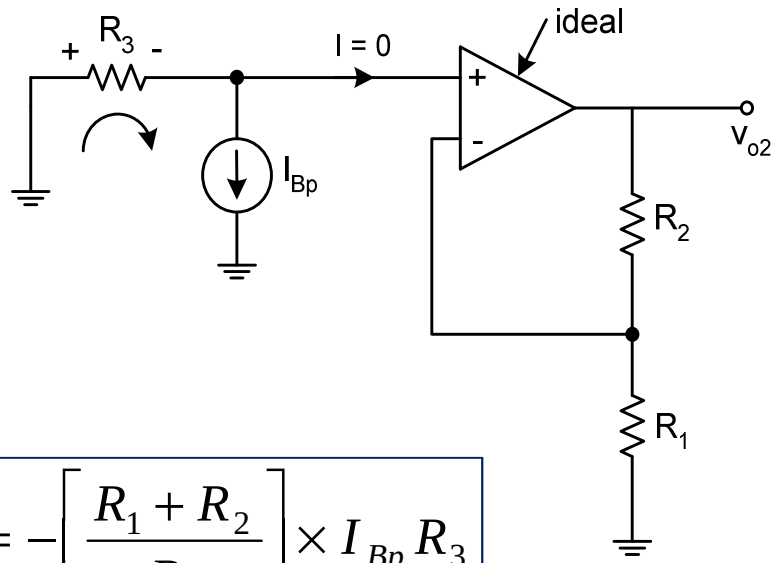


Effect of I_{Bp} alone is obtained by first replacing the current source with the equivalent voltage source = - $I_{Bp}R_3$

(N.B. Note polarity !)

Then

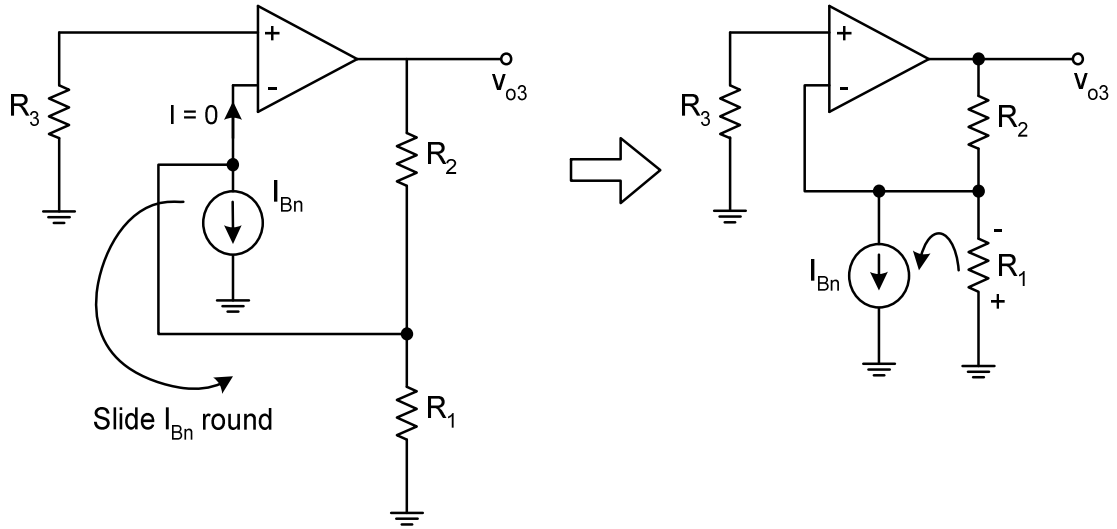
$$V_{o2} = \left[\frac{R_1 + R_2}{R_1} \right] \times \left(- I_{Bp} R_3 \right)$$



$$V_{o2} = -\left[\frac{R_1 + R_2}{R_1} \right] \times I_{Bp} R_3$$

Calculation of output offset in general case (contd.)

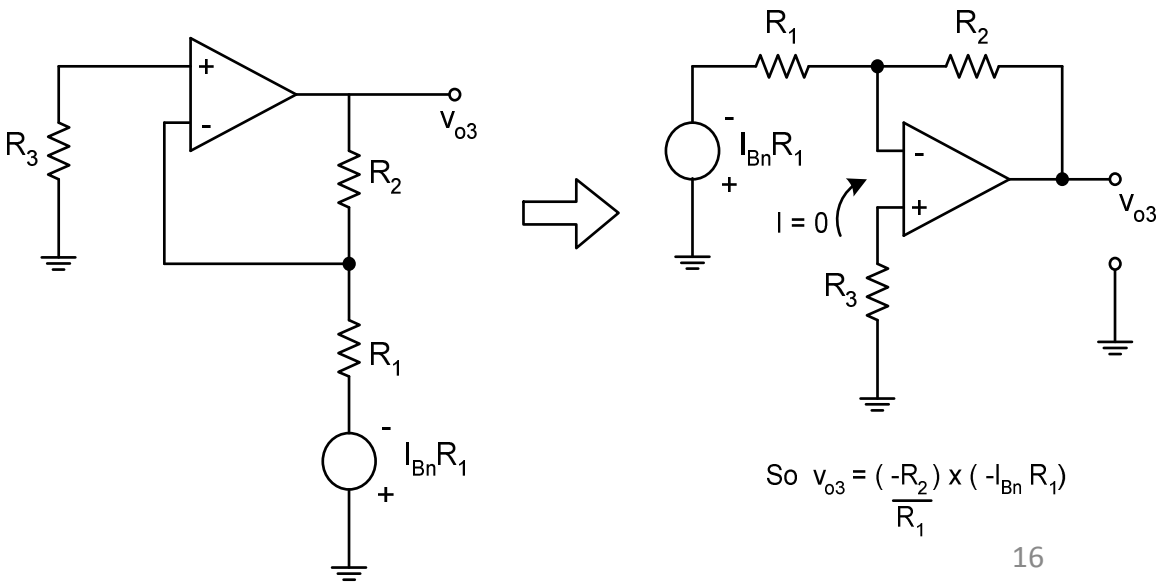
Effect of I_{Bn} alone



Now a source transformation:

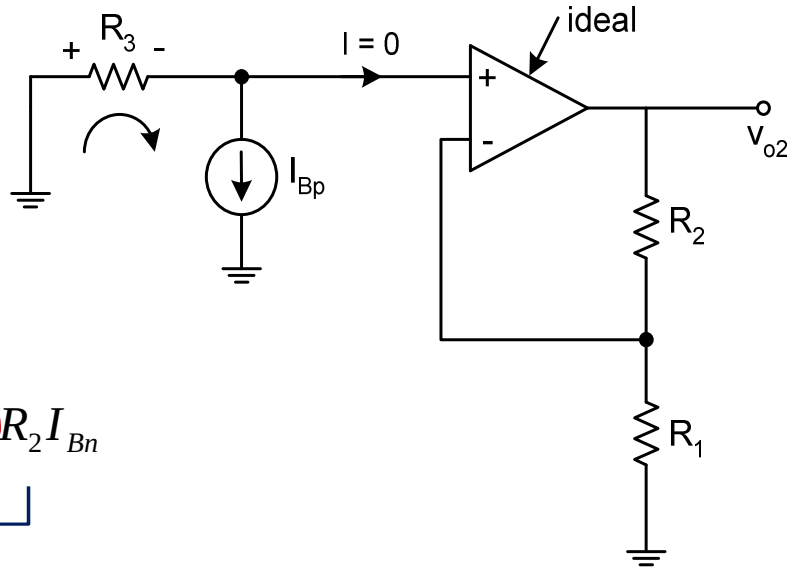
$$V_{o3} = \left(-\frac{R_2}{R_1} \right) \times \left(-I_{Bn} R_1 \right)$$

$$\boxed{V_{o3} = I_{Bn} R_2}$$



COMBINING contributions gives

$$V_o = V_{o1} + V_{o2} + V_{o3}$$



$$V_O = \left(\frac{R_1 + R_2}{R_1}\right)\left[V_{os} - I_{Bp}\,R_3\right] + \frac{R_2}{R_1} I_{Bn}\,R_1$$

$$= \left(\frac{R_1+R_2}{R_1}\right)\left[V_{os} - I_{Bp}\,R_3\right] + \left(\frac{R_1+R_2}{R_1}\right)\left(\frac{R_1}{R_1+R_2}\right) R_2 I_{Bn} \quad \text{=1!}$$

$$= \left(\frac{R_1 + R_2}{R_1}\right)\left[V_{os} - I_{Bp}\,R_3\right] + \left(\frac{R_1 + R_2}{R_1}\right) R_1 \,\|\, R_2\, I_{Bn}$$

$$= \left(\frac{R_1 + R_2}{R_1}\right)\left[V_{os} - I_{Bp}\,R_3 + R_1 \,\|\, R_2\, I_{Bn}\right]$$

(Take $\left(\frac{R_1 + R_2}{R_1}\right)$ outside the bracket)

$$V_o = \left(\frac{R_1 + R_2}{R_1}\right) V_{eff} \qquad \text{with} \qquad V_{eff} = \left[V_{os} - I_{Bp}\,R_3 + R_1 \,\|\, R_2\, I_{Bn}\right]$$

where V_{eff} = effective input offset voltage – for this amplifier circuit

Calculation of V_O in worst case

$$Gain = \frac{R_1 + R_2}{R_1} = \frac{45k + 90k}{45k} = 3 \qquad R_1 \| R_2 = 45k \| 90k = 30k$$

Consider components of $V_{eff} = \left[V_{os} - I_{Bp} R_3 + R_1 \| R_2 \, I_{Bn} \right]$

From data sheet: $-6mV < V_{os} < 6mV$ and $400\,nA < \left| I_{Bp}, I_{Bn} \right| < 600\,nA$

$$10k \times 400nA < R_3 I_{Bp} < 10k \times 600nA \Rightarrow 4mV < R_3 I_{Bp} < 6mV$$

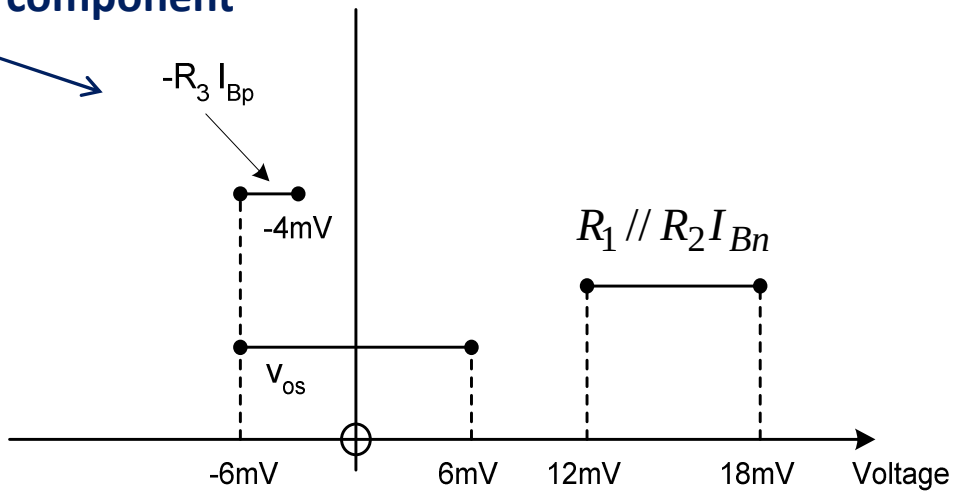
$$30k \times 400nA < R_1 // R_2 I_{Bn} < 30k \times 600nA \Rightarrow 12mV < R_1 // R_2 I_{Bn} < 18mV$$

Combine graphically: Draw ranges of each component

MAX NEG value of V_{eff} when each component has max. neg. value

$$\therefore Max.neg.V_{eff} = -6mV + 12mV - 6mV = 0$$

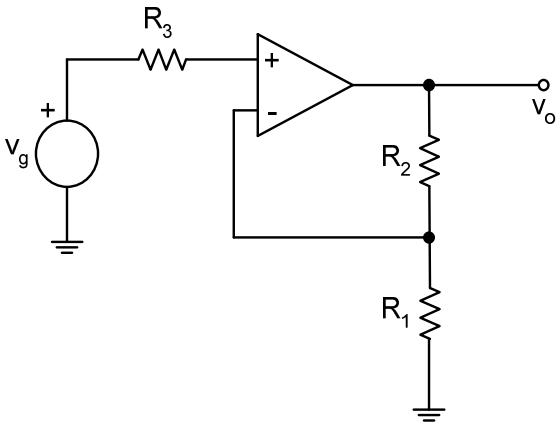
MAX Pos value of V_{eff} when each component has max. pos. value



$$\therefore Max.pos.V_{eff} = -4mV + 6mV + 18mV = +20mV$$

Most probable value for V_O is half way through this range i.e. 10mV × Gain = 30 mV

Calculation of V_O in worst case (contd.)

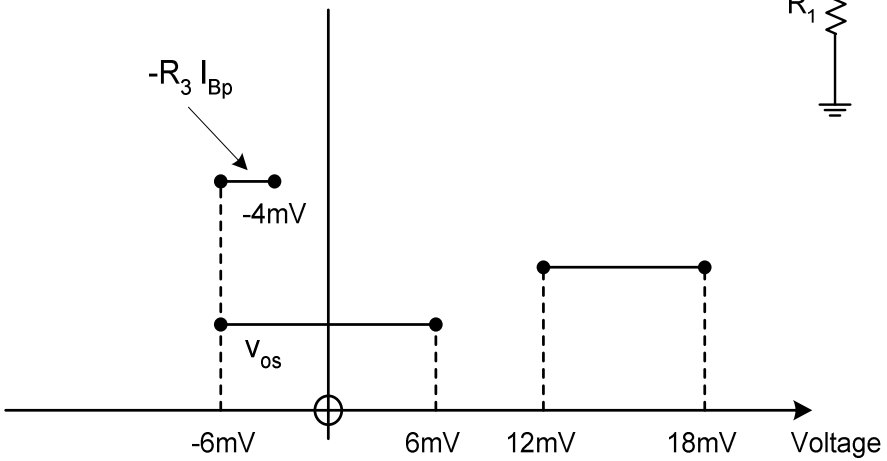


So in worst case, V_o lies in the range

$$0 \le V_o \le 3 \times 20mV$$

$$0 \le V_o \le 60mV$$

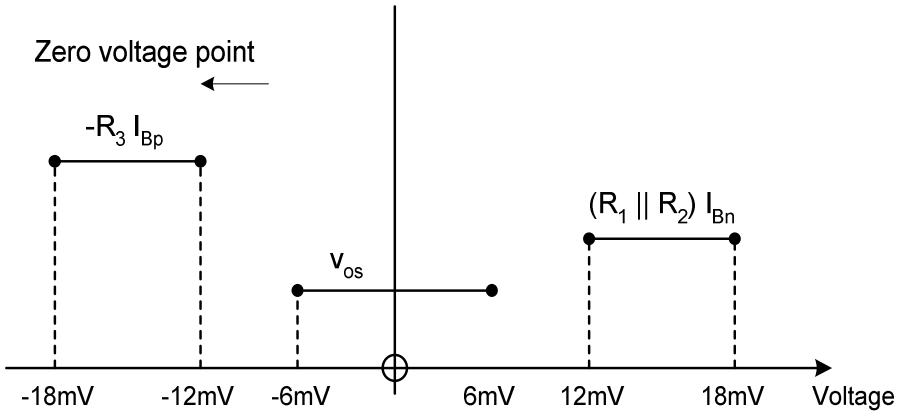
MOST LIKELY value of V_o is mid-way through this range; ie V_o (max probability) **= 30mV**



NB We can adjust **R_3** then chose

$$R_3 = R_1 \| R_2$$

Since in this case, range pattern is symmetrical about zero voltage point!



$$Min\ V_{eff} = -18mV - 6mV + 12mV = -12mV$$

$$MaxV_{eff} = -18mV + 6mV + 18mV = +12mV$$

So that o/p offset voltage is $-36mV < V_o < 36mV$

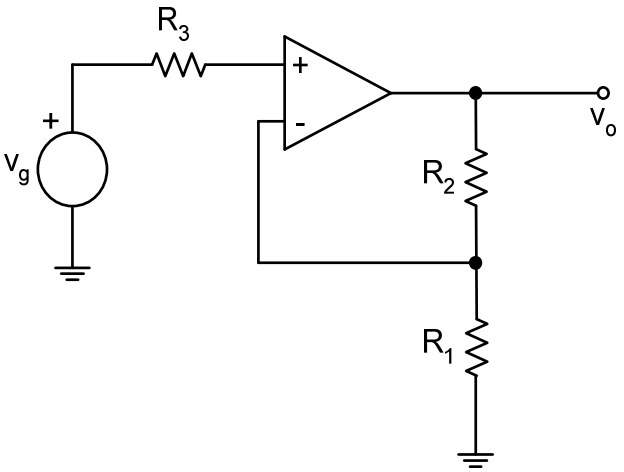
Most probable value for V_O is zero!

Some PRACTICAL points

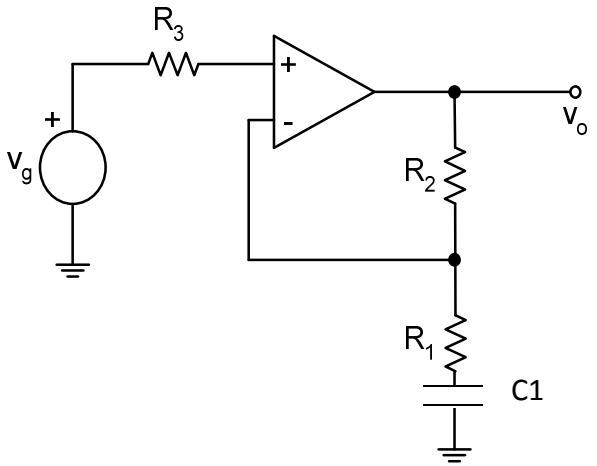
Important to remember that we are dealing here with **DC** V_{OS} and I_{Bp} and I_{Bp}.

The analysis must consider only DC paths. If capacitors are present then the analysis must treat them as OPEN CIRCUIT because they block DC.

1) In this circuit we make $R_3 = R_1//R_2$ so that the DC paths resistances seen by the **bias currents I_{Bp} and I_{Bn}** are equal

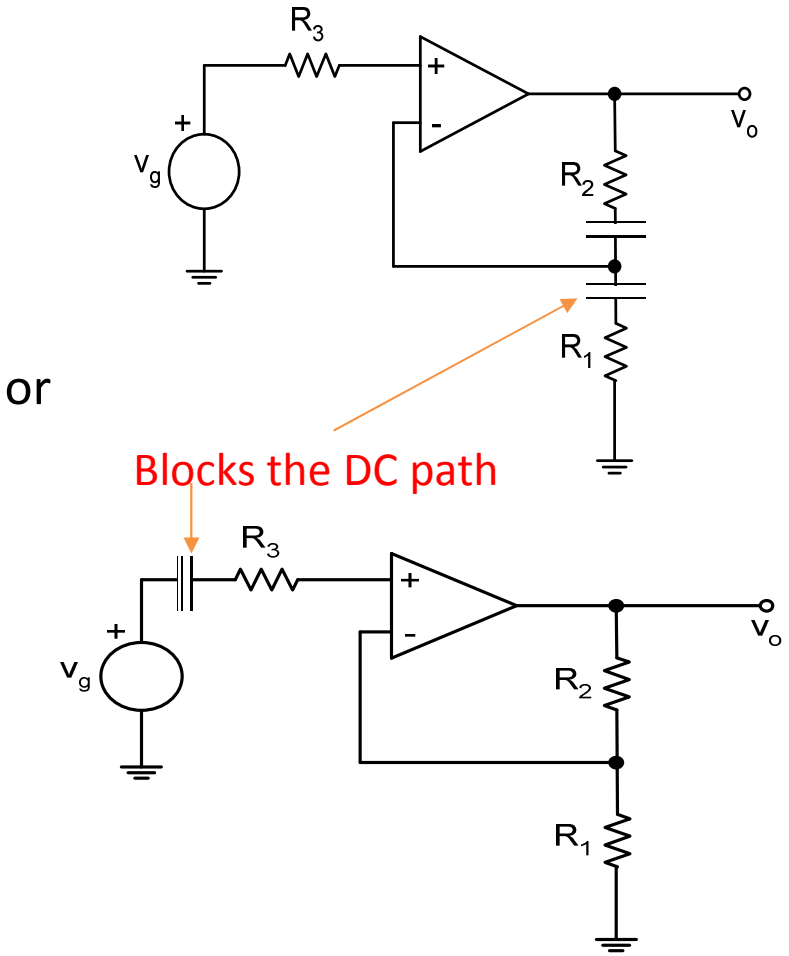


2) But in this circuit we make $R_3 = R_2$ because the capacitor blocks the DC path through R_1



Some further PRACTICAL points

Note that there will be a problem if no DC paths are provided to one or other of the inputs to allow the bias currents to flow. e.g

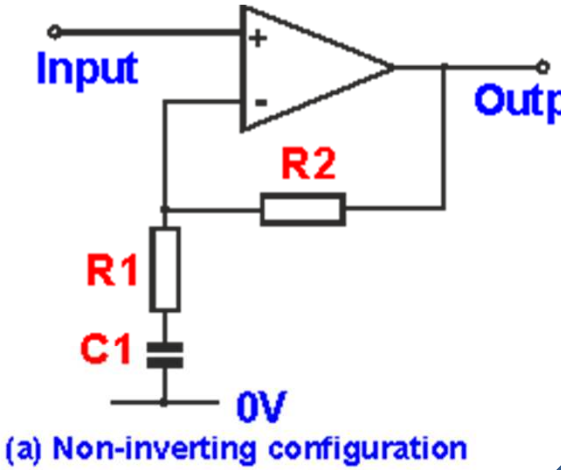


The solution in both cases would be to place a resistor across at least one of the capacitors that is:

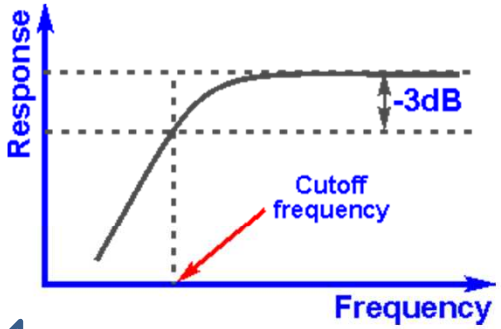
- large enough not to affect the expected response
- but small enough to allow the small bias currents to flow without creating a significant DC voltage offset

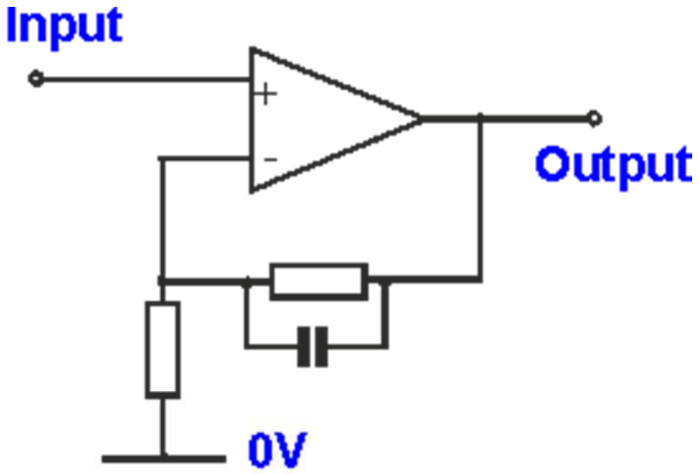
These circuits are OK

What do they do?

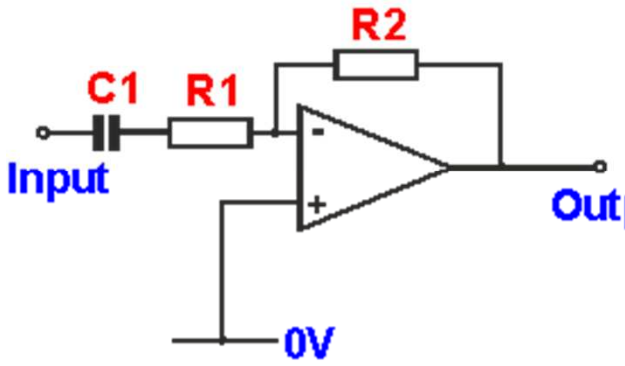


(a) Non-inverting configuration

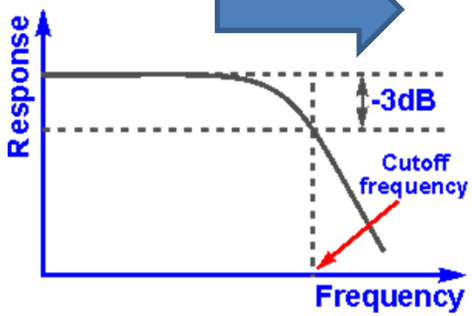


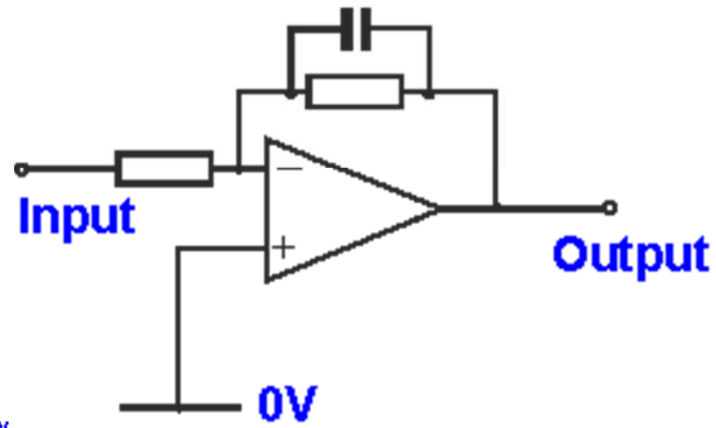


(a) Non-inverting configuration



(b) Inverting configuration





(b) Inverting configuration

End of ….the lecture topics !!

Some revision classes will follow (3-4)

1st one on Monday after Easter

The slides can be found on VITAL
First item in ‘Sessions/resources

Self-assessment Test 2

- A self-assessment test will be available on VITAL on 1st Monday of next term at 9am (look in ‘Assessment’ section).
- 12 short questions
- It should take no more than 1 hour
- use your notes! – it’s all there.