PAPER CODE NO.	EXAMINER: Dr S Khursheed
ELEC 370	DEPARTMENT: **EE&E** TEL. NO: 44510

UNIVERSITY OF LIVERPOOL

SECOND SEMESTER EXAMINATIONS 2017/18

EMBEDDED COMPUTER SYSTEMS

TIME ALLOWED: Three Hours

INSTRUCTIONS TO CANDIDATES

The numbers in the right hand margin represent an **approximate guide** to the marks available for that question (or part of a question). Total marks available are 100.

Answer ALL Questions.

The use of a calculator IS allowed.

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1. a) The ARM9 microprocessor has a 5 stage pipeline and reads registers at the end of stage 2 (decode) but writes values to registers in stage 5 (write-back). **6**

   i) How does this lead to a ‘read-after-write’ hazard?

   ii) How is this problem eliminated using ‘data forwarding’?

   iii) If the problem cannot be eliminated then an ‘interlock’ results; what is an ‘interlock’?

   b) In the following ARM9 program, there are two examples of ‘data forwarding’ and one further example of a ‘read-after-write’ hazard that results in an interlock. Identify all three. **6**

```
Mnemonic                    Comment
MOV r1, #0x0004A000         ;move 0x0004A000 into r1
MOV r2, #0x00003BC0         ;move 0x00003BC0 into r2
MOV r0, r1, LSL #8          ;left shift r1 by 8 bits
SUB r3, r2, r1              ;subtract r1 from r2
ADD r4, r1, r2              ;add r1 and r2, sum in r4
RSB r5, r4, r0              ;subtract r4 from r0
MOV r6, #0x000002E4         ;move 0x000002E4 into r6
MOV r7, #0x0002E400         ;move 0x0002E400 into r7
ADD r2, r1, r0              ;add r1 and r2, sum in r2
```

   c) Draw a pipeline diagram for the program given above assuming that it is executed using the ARM9 microprocessor. What is the performance as measured in ‘clocks per instruction’ (CPI)? (counting clock cycles from the execute stage of the first instruction to the execute stage of the last instruction) **8**

   How can the instructions be reordered so that ‘read-after-write’ hazards do not occur without changing the function of the programme?

Total 20

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2. a) Booth's algorithm to find the product of a multiplier, M, and a multiplicand, B, can be summarized by the following table: **12**

C_{in}	Multiplier	LSL #	ALU	C_{out}
0	$\times 00_2$	-	A+0	0
0	$\times 01_2$	2N	A+B	0
0	$\times 10_2$	(2N+1)	A+B	0
0	$\times 11_2$	2N	A–B	1
1	$\times 00_2$	2N	A+B	0
1	$\times 01_2$	(2N+1)	A+B	0
1	$\times 10_2$	2N	A–B	1
1	$\times 11_2$	-	A+0	1

Demonstrate how Booth's algorithm performs multiplication by finding the product of 00011110_2 (M) and 11011100_2 (B). Each step in the calculation should be given. Give the result in a 16 bit binary format.

b) The ARM7 multiplier can give a double length 64 bit product. **5**
Why is it important to know the number format, either two's complement or unsigned integer, when calculating a double length product?

c) How many clock cycles does the ARM7 microprocessor require to produce **3**
(i) a 32 bit product and (ii) a 64 bit product?

Total
20

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3. a) Figure Q3 shows the relative performance of three different cache designs at four different sizes of cache memory assuming that the clock frequency of the cache memory is 2.5 times greater than the main memory clock frequency. **6**

Briefly explain the difference between a direct mapped cache, a 2-way set associative cache and a fully associative cache.

b) Why does a fully associative cache have a better performance than a 2-way set associative cache which in turn has a better performance than a direct-mapped cache for the same size of cache e.g. 4 Kbytes? **3**

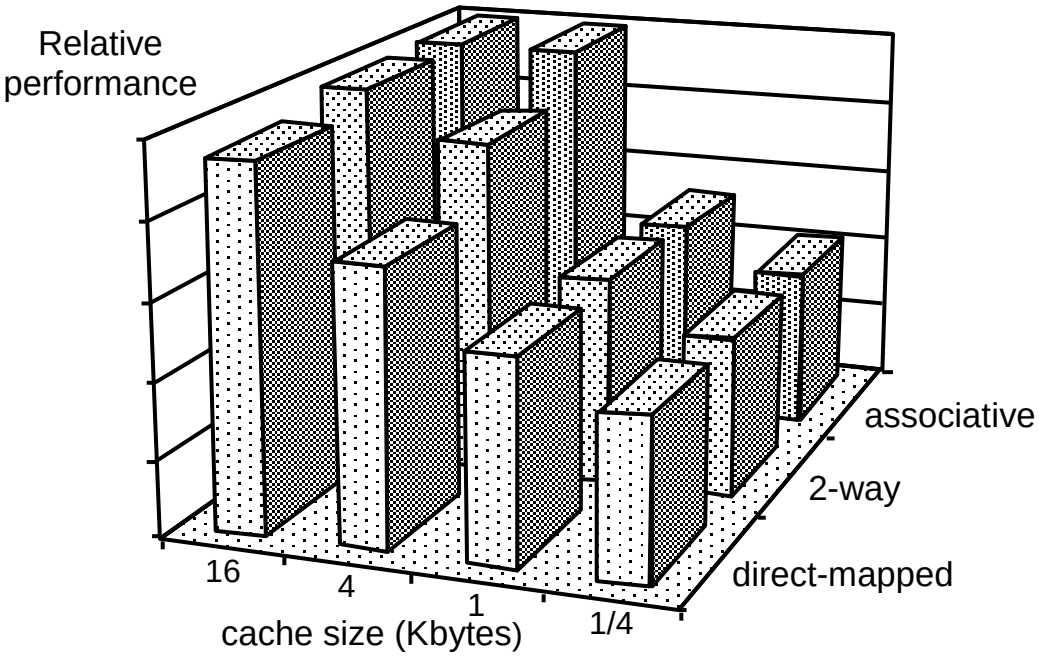

Figure Q3

Question 3 continues overleaf.

Question 3 continued.

c) Why does a larger cache have a better performance than a smaller cache? **3**

d) What are the disadvantages of a larger cache? **2**

e) What is the difference between the write strategies known as ‘copy back’ and ‘write through’? **4**

f) Why is the external memory bandwidth requirement reduced for a ‘copy back’ strategy? **2**

Total

20

4. a) Low power design is important for many embedded processor systems. Describe what is meant by the terms dynamic power dissipation and leakage power dissipation.
Write down a mathematical relationship for dynamic power dissipation in terms of operating frequency, switching capacitance and supply voltage. **7**

b) With reference to the equation you gave for part (a) above, describe how good circuit design and good software design can lead to a reduction in dynamic power dissipation. **5**

c) Figure Q4 shows a circuit diagram of a NAND gate which uses multithreshold CMOS technology (MTCMOS) to implement power gating. With reference to the figure, describe how power gating leads to a reduction in leakage power dissipation. **8**

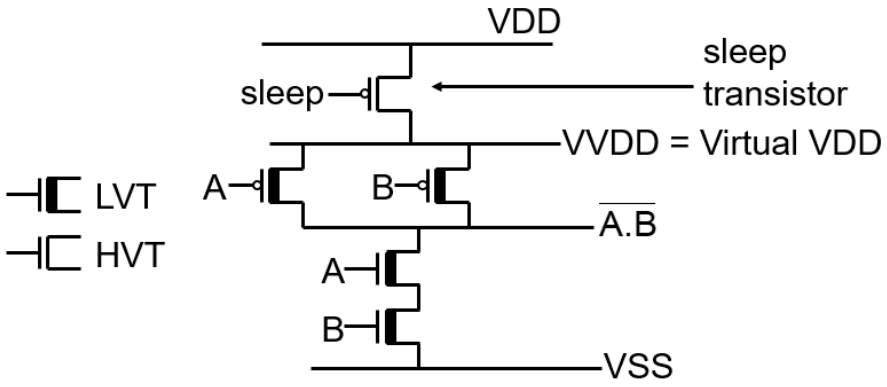

Figure Q4

Total 20

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5. a) The ARM family of microprocessors can execute either 32 bit ARM instructions or 16 bit Thumb instruction. **6**
What are the major features of the ARM instruction set that are omitted from the Thumb instruction set?

b) Explain the mechanism, known as decompression, whereby the ARM7 microprocessor can execute Thumb code. **7**

c) What is the purpose of the Thumb instruction set? **7**
In what situations is it advantageous to use Thumb code?

Total 20

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First Semester Examinations 2019-20

EMBEDDED COMPUTER SYSTEMS

TIME ALLOWED: Three Hours

INSTRUCTIONS TO CANDIDATES

The numbers in the right hand margin represent an **approximate guide** to the marks available for that question (or part of a question). Total marks available are 100.

Answer ALL Questions.

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1. a) Figure Q1.1 shows the relative performance of three different cache designs at four different sizes of cache memory assuming that the clock frequency of the cache memory is 2.5 times greater than the main memory clock frequency. **6**

   Briefly explain the difference between a direct mapped cache, a 2-way set associative cache and a fully associative cache.

   b) Why does a fully associative cache have a better performance than a 2-way set associative cache which in turn has a better performance than a direct-mapped cache for the same size of cache e.g. 4 Kbytes? **3**

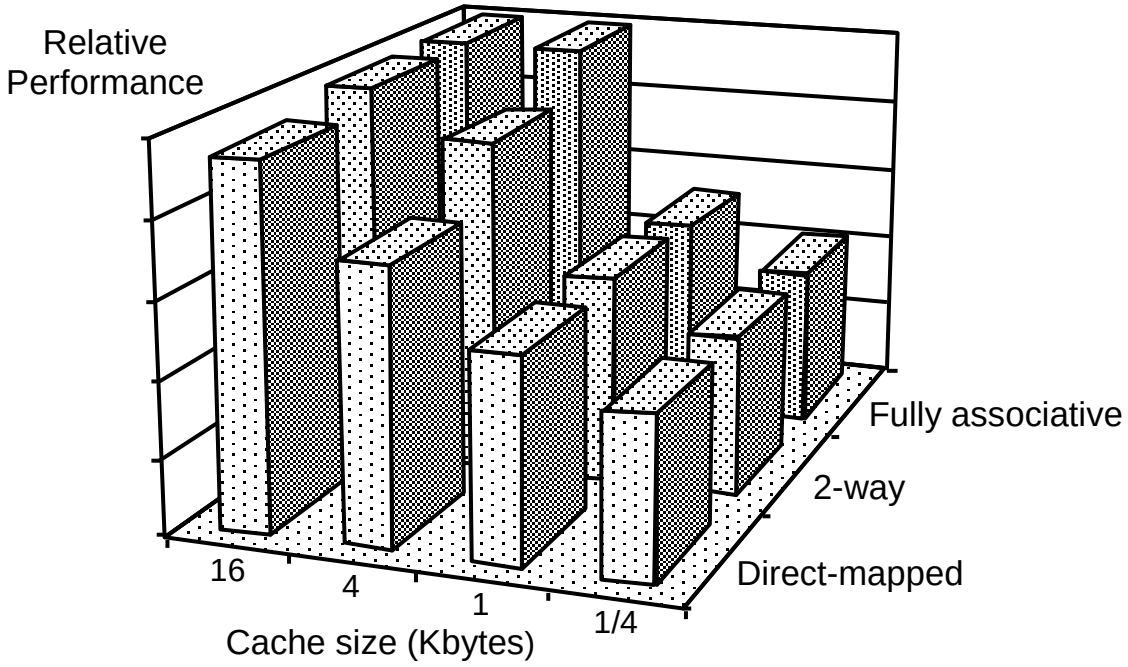

Figure Q1.1

   c) Why does a larger cache have a better performance than a smaller cache? **3**

Question 1 continues overleaf.

Question 1 continued.

d) What are the disadvantages of a larger cache? **3**

e) In Figure Q1.2 the performance of a 4 Kbyte cache is plotted against the number of ways of associativity from 1 (direct mapped) to 256 (fully associative). The cache line length is 16 bytes. Also shown is the external memory bandwidth. Why does the external memory bandwidth decrease as the ways of associativity increases? **4**

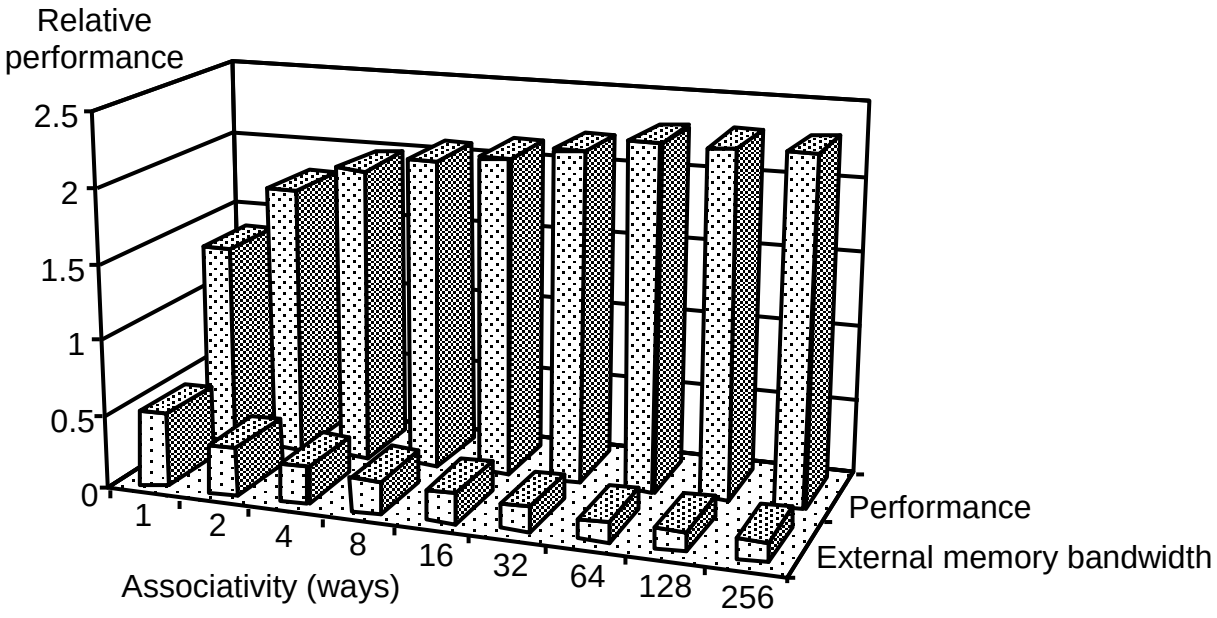

Figure Q1.2

f) What is the difference between the write strategies known as 'copy back' and 'write through'? **3**

g) Why is the external memory bandwidth requirement reduced for a 'copy back' strategy? **3**

Total 25

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2. a) Booth's algorithm to find the product of a multiplier, M, and a multiplicand, B, can be summarized by the following table: **12**

C_{in}	Multiplier	LSL #	ALU	C_{out}
0	$\times 00_2$	-	A+0	0
0	$\times 01_2$	2N	A+B	0
0	$\times 10_2$	(2N+1)	A+B	0
0	$\times 11_2$	2N	A–B	1
1	$\times 00_2$	2N	A+B	0
1	$\times 01_2$	(2N+1)	A+B	0
1	$\times 10_2$	2N	A–B	1
1	$\times 11_2$	-	A+0	1

Demonstrate how Booth's algorithm performs multiplication by finding the product of $0001\ 1001_2$ (M) and $0100\ 1011_2$ (B). Each step in the calculation should be given. Give the final result in a 16 bit binary format.

b) Describe the difference between a 'carry propagate' adder and a 'carry save' adder. How is a carry save adder used to improve the performance of the multiplier circuit used in the ARM7 microprocessor? **4**

c) The ARM7 multiplier can give a double length 64 bit product. **4**
Why is it important to know the number format, either two's complement or unsigned integer, when calculating a double length product?

d) A barrel shifter is used in ARM7 to execute a number of instruction for example, LSL (logical shift left), ROR (Rotate right) etc. Using appropriate instructions, explain how a barrel shifter may be used to multiply and divide a number by 2^n. **5**

Total

25

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3. a) Computer programmes are said to exhibit the properties of temporal and spatial locality. What is meant by these terms and why do computer programmes have these properties? **5**

b) A memory protection unit (MPU) can be used to assign different attributes to blocks of memory. Name some of the typical attributes. Why might a particular memory address be assigned as 'uncachable'? **6**

c) A memory management unit (MMU) system divides the memory into many equally sized pages. In the context of an MMU, what is meant by the following terms: virtual address, physical address, and page table? **6**

d) What is the memory access time penalty associated with page table walking and how does a transition look-aside buffer (TLB) decrease the memory access time? How does the property of locality effect the operation of a TLB and what hit rate would you expect for a typical TLB with 64 entries? **4**

e) What is meant by the following terms: virtualization and hypervisor? **4**

Total 25

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4. a) The ARM9 instruction set includes a few instructions (such as CLZ and QADD) that are not included in the ARM7 instruction set. **6**
What factors should be considered when making the decision to add extra instructions to an instruction set?
What are the advantages and disadvantages of adding instructions to an instruction set?

b) Describe the operation of the 'count leading zeros' instruction, CLZ, using an appropriate example of your choice. **4**
How can the CLZ instruction be used to ensure that the product of two numbers does not exceed 32 bits?

c) Describe the operation of the 'saturated addition' instruction, QADD. **4**
Perform the addition of 0x70000000 and 0x20000FFF using both ADD and the saturated addition instruction, QADD.

d) When is the Q flag set? **6**
Why is the Q flag also known as the 'sticky bit'?
In what circumstances is the 'sticky' property useful?

e) ARM7 achieves a performance of about 1.9 CPI (Clock cycles per Instruction) for a given set of benchmarks. Name and briefly explain key features used by ARM9 and later versions of ARM microprocessors that led to performance improvement. **5**

Total 25

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Second Semester Examinations 2016-17

EMBEDDED COMPUTER SYSTEMS

TIME ALLOWED: Three Hours

INSTRUCTIONS TO CANDIDATES

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Answer ALL Questions.

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1. a) Briefly describe the different computer architectures that are known as (i) von Neumann and (ii) Harvard and the advantages / disadvantages of each. **4**

b) An instruction pipeline is an important element in the RISC (reduced instruction set computer) architecture. Briefly describe how an instruction pipeline works and explain why a pipeline with more stages can give an improved performance. **8**

c) The performance of a microprocessor, as measured by the time taken to execute a particular computer programme, T_{prog}, is given by the following expression: **8**

$$T_{prog} = \frac{N_{inst} \times CPI}{f_{clk}}$$

How does the ARM9 microprocessor achieve an improvement in performance compared with the ARM7 microprocessor for each of the three parameters;

(i) N_{inst}, the number of machine code instructions executed in the program,

(ii) CPI, number of clock cycles per machine code instruction

(iii) f_{clk}, the clock frequency?

Total 20

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2. a) Modern microprocessors are typically designed so that the clock period is less than 10 gate delays. With reference to this, explain why a 32 bit addition cannot be implemented using a traditional ripple carry adder. Your answer should include a diagram of part of a ripple carry adder (not all 32 bits). **6**

b) Describe how a carry look ahead adder works, including a diagram in your answer. Clearly state the conditions for setting the generate and propagate logic signals.
What are the advantages and disadvantages of the carry look ahead adder compared to the ripple carry adder for 32-bit additions? **8**

c) Describe how a carry select adder works, including a diagram in your answer.
What are the advantages and disadvantages of the carry select adder compared to other designs for 32-bit additions? **6**

Total 20

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3. a) Low power design is important for many embedded processor systems. Describe the following terms: **9**

   (i) Dynamic power dissipation
   (ii) Leakage power dissipation.
   (iii) Dynamic voltage and frequency scaling.

   b) Briefly describe what is meant by ‘clock gating’. **5**
   How does clock gating reduces power dissipation?

   c) Sketch a simple circuit that uses latched clock gating. **6**
   Why is latched clock gating preferred to a circuit that does not latch the gated clock signal?

Total 20

UNIVERSITY OF LIVERPOOL

4. a) Computer programmes are said to exhibit the properties of temporal and spatial locality. What is meant by these terms and why do computer programmes have these properties? **4**

b) A memory protection unit (MPU) can be used to assign different attributes to blocks of memory. Name some of the typical attributes. Why might a particular memory address be assigned as 'uncachable'? **6**

c) A memory management unit (MMU) system divides the memory into many equally sized pages. In the context of an MMU, what is meant by the following terms: virtual address, physical address, and page table? **6**

d) What is the memory access time penalty associated with page table walking and how does a transition look-aside buffer (TLB) decrease the memory access time? How does the property of locality affect the operation of a TLB and what hit rate would you expect for a typical TLB with 64 entries? **4**

Total 20

UNIVERSITY OF LIVERPOOL

5. a) The ARM9 instruction set includes a few instructions (such as CLZ and QADD) that are not including in the ARM7 instruction set. **6**
What factors should be considered when making the decision to add extra instructions to an instruction set?
What are the advantages and disadvantages of adding instructions to an instruction set?

b) Describe the operation of the 'count leading zeros' instruction, CLZ, using an appropriate example of your choice. **4**
How can the CLZ instruction be used to ensure that the product of two numbers does not exceed 32 bits?

c) Describe the operation of the 'saturated addition' instruction, QADD. **4**
Perform the addition of 0x60000000 and 0x20000FFF using both ADD and the standard addition instruction, QADD.

d) When is the Q flag set? **6**
Why is the Q flag also known as the 'sticky bit'?
In what circumstances is the 'sticky' property useful?

Total 20

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Second Semester Examinations 2018-19

EMBEDDED COMPUTER SYSTEMS

TIME ALLOWED: Three Hours

INSTRUCTIONS TO CANDIDATES

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Answer All Questions.

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1. a) Explain the terms ‘semantic gap’ and ‘code density’. Explain the advantages and disadvantages of Complex Instruction Set Computer (CISC) and Reduced Instruction Set Computer (RISC) designs with reference to the semantic gap and code density. **7**

   b) What are the key features of the Berkeley RISC 1 processor invented in 1980?
   How did the performance of this RISC processor compare with the performance of CISC processors available around 1980? **7**

   c) What features of the Berkeley RISC 1 processor are used in the design of the ARM7 microprocessor?
   What features of the Berkeley RISC 1 processor were rejected in the design of the ARM7 microprocessor? **6**

Total 20

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2. a) Modern microprocessors are typically designed so that the clock period is less than 10 gate delays. With reference to this, explain why a 32 bit addition cannot be implemented using a traditional ripple carry adder. Your answer should include a diagram of part of a ripple carry adder (not all 32 bits). **6**

b) Describe how a carry look ahead adder works, including a diagram in your answer. Clearly state the conditions for setting the generate and propagate logic signals.
What are the advantages and disadvantages of the carry look ahead adder compared to the ripple carry adder for 32-bit additions? **8**

c) Describe how a carry select adder works; include a diagram in your answer.
What are the advantages and disadvantages of the carry select adder compared to other adder designs for 32-bit addition? **6**

Total 20

3. a) Low power design is important for many embedded processor systems.
Describe the following terms: **9**

(i) Dynamic power dissipation
(ii) Leakage power dissipation.
(iii) Dynamic voltage and frequency scaling.

b) Briefly describe what is meant by ‘clock gating’. **5**
How does clock gating reduces power dissipation?

c) Sketch a simple circuit that uses latched clock gating. **6**
Why is latched clock gating preferred to a circuit that does not latch the gated clock signal?

Total
20

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4. a) What is meant by the term ‘memory remapping’? **3**

b) Why is memory remapping used in an embedded processor? **3**

c) Different types of memory have different maximum operating frequencies. How can a memory system be designed so that the clock frequency matches the performance of the fastest component but allows time for a memory transfer with the slowest memory component? **9**

d) Some memory components, such as dynamic RAM, can operate at a higher frequency when memory transfers are from sequential addresses. Approximately 75% of memory accesses are sequential for a typical computer program. The ARM7 microprocessor produces a signal that indicates when sequential accesses are required.
How would memory control logic make use of that signal to improve the overall performance of the memory system? **5**

Total 20

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5. a) A memory management unit (MMU) uses address translation. **5**
Describe the process of address translation and explain why it is useful.

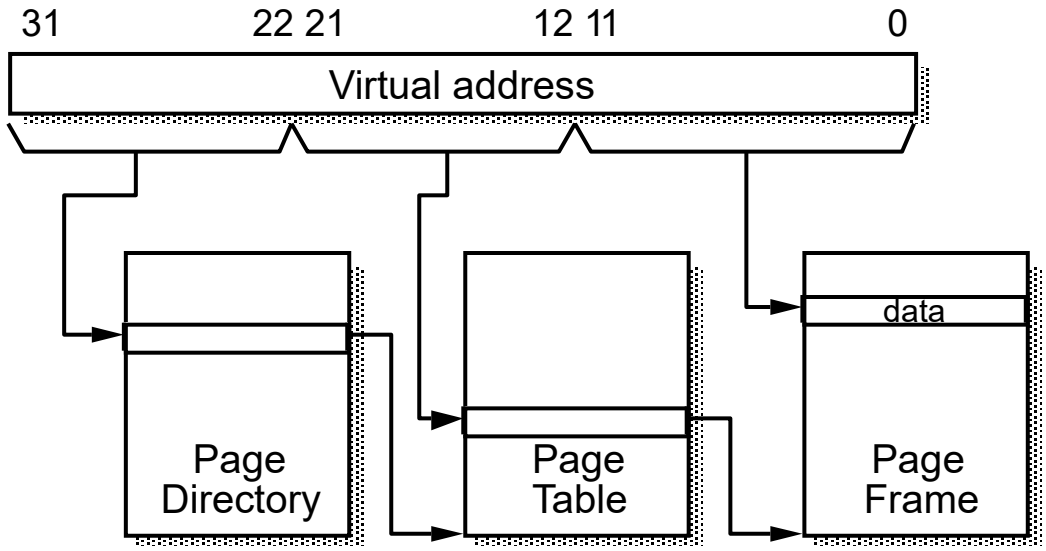

Figure Q5

b) Demonstrate, using the Figure Q5, how a page table walk identifies a unique physical address, e.g. 0x086A8198, with a unique virtual address, e.g. 0xF58B4198. **8**

c) What is the memory access time penalty associated with page table walking and how does a transition look-aside buffer (TLB) decrease the memory access time? How does the property of locality effect the operation of a TLB and what hit rate would you expect for a typical TLB with 64 entries? **7**

Total 20


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