MMU初始化和使能主要代码如下：

```
void kernel_vmm_enable() {
    write_prrr(0xf0040000);
    LogInfo("[vmm]: Primary Remap Registe writed\n");

    write_ttbcr(0xb0003500);
    LogInfo("[vmm]: ttbcr writed\n");

    write_ttbr0((uint32_t) kernelVMML1PT);
    LogInfo("[vmm]: ttbr0 writed\n");

    mmu_enable();
    LogInfo("[vmm]: vmm enabled\n");
}
```

1.write_prrr函数向内存重映射寄存器写入0xf0040000,对照下图，说明配置的attr3为11RW模式，attr0为0100模式。

	31 24	23 16	15 8	7 0
MAIR0	Attr3	Attr2	Attr1	Attr0
MAIR1	Attr7	Attr6	Attr5	Attr4

Table B4-7 MAIR*n*.Attr*m*[7:4] encoding

Attr*m*[7:4]	Meaning
0000	Strongly-ordered or Device memory, see encoding of Attr*m*[3:0].
00RW, RW not 00	It is IMPLEMENTATION DEFINED whether the encoding is: • UNPREDICTABLE • Normal memory, Outer Write-Through[b] Transient.
0100	Normal memory, Outer[a] Non-cacheable.
01RW, RW not 00	It is IMPLEMENTATION DEFINED whether the encoding is: • UNPREDICTABLE • Normal memory, Outer Write-Back[b] Transient.
10RW	Normal memory, Outer[a] Write-Through Cacheable[b], Non-transient[c].
11RW	Normal memory, Outer[a] Write-Back Cacheable[b], Non-transient[c].

2.write_ttbcr向转换表基本控制寄存器（ttbcr）写入0xb0003500，对照下图表配置为LPAE模式，ORGN1和IRGN1分别为01模式。

31	30	29–28	27–26	25–24	23	22	21–19	18–16	15–14	13–12	11–10	9–8	7	6	5	4	3	2–0
EAE	IDF	SH1	ORGN1	IRGN1	EPD1	A1	SBZP	T1SZ	SBZP	SH0	ORGN0	IRGN0	EPD0	SBZP	PD1	PD0	SBZP	T0SZ

- EAE – Extended Address Enable. SBZP if LPAE is not supported

Following fields are SBZP if EAE=0

- IDF – Implementation Defined
- SH1 – Shareability attribute for memory associated with translation table walks using TTBR1.

00	01	10	11
non–shareable	unpredictable	outer shareable	inner shareable

- ORGN1 – Outer cacheability using TTBR1

00	01	10	11
outer non–cacheable	outer write–back write–allocate cacheable	outer write–through cacheable	outer write–back no write–allocate cacheable

- IRGN1 – Inner cacheablility using TTBR1

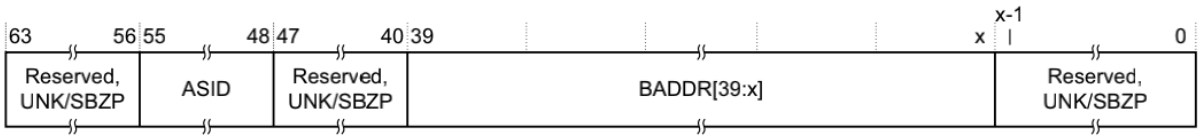
00	01	10	11
inner non–cacheable	inner write–back write–allocate cacheable	inner write–through cacheable	inner write–back no write–allocate cacheable

- EPD1 – Disable Page walks with TTBR1. If 0, table walks are performed. Otherwise, a translation fault is generated.
- A1 – defines whether TTBR0 or TTBR1 defines the ASID, for 0 and 1 respectively. The ASID is the Address Space Identifier.
- SBZP – Should Be Zero or Preserved. This is more commonly called RES0.
- T1SZ – The size of the memory region addressed by TTBR1. 2^(32–T1SZ) is the size.
- SH0 – like SH1, but for TTBR0.
- ORGN0 – ""
- IRGN0 – ""
- EPD0 – ""

3.write_ttbr0向转换表基址寄存器0写入TLB表基地址kernelVMML1PT。

64-bit TTBR0 and TTBR1 format

The bit assignments for the 64-bit implementations of TTBR0 and TTBR1 are identical, and are:



4.mmu_enable代表使能mmu。