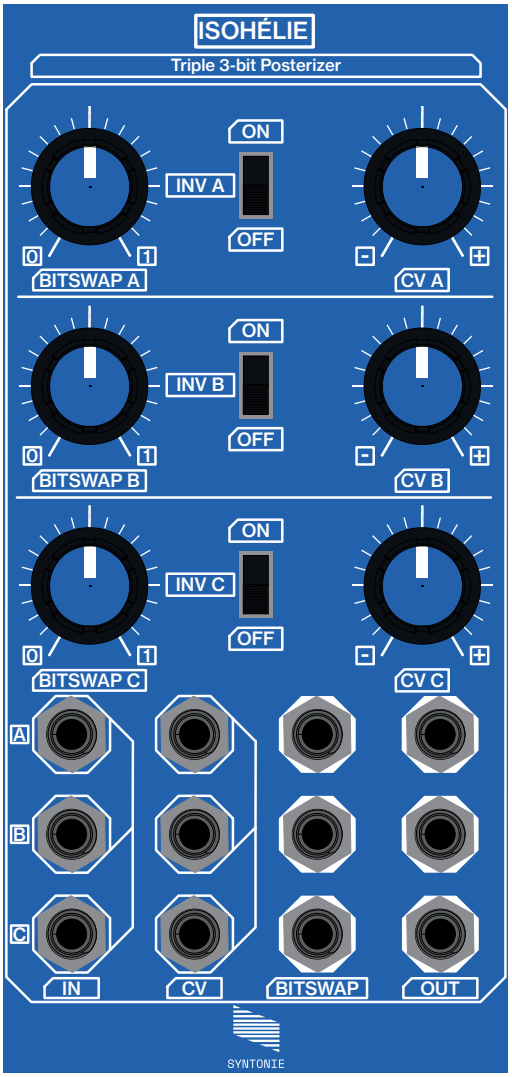
Isohélie

Triple 3-bit Posterizer¬

User documentation

SYNTONIE

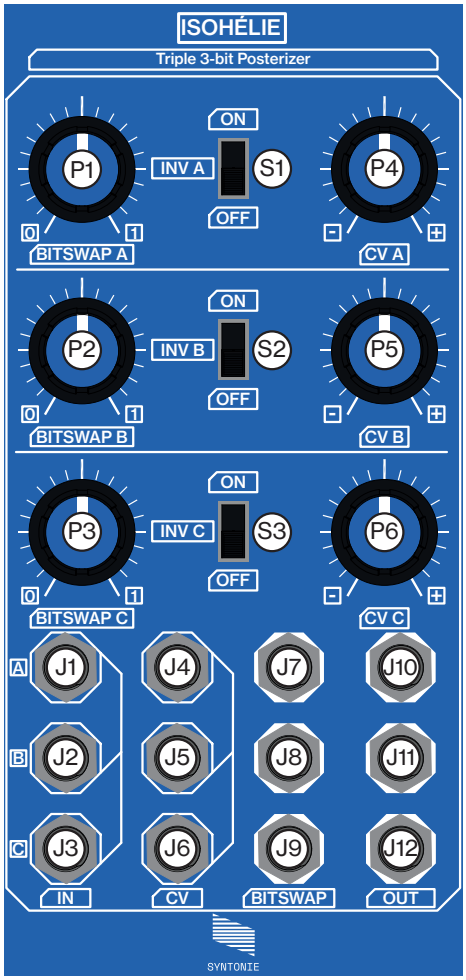


Isohélie is a term used in french versions of graphic editing softwares to describe posterization, it is formed from the ancient Greek “iso” meaning equal and “hêlios” meaning sun/light. Each channel is centered around a 3-bit ADC/DAC which will quantizes the input signal into 8 equal steps.

Specifications

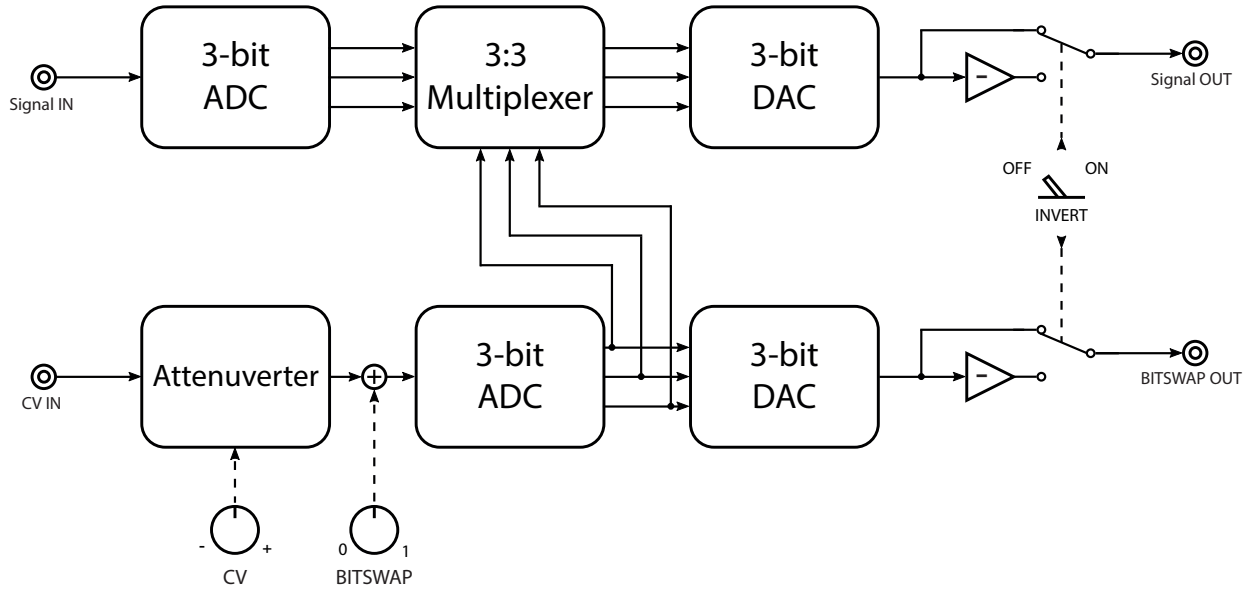
- 12HP
- 230 mA +12V (16pin or DC)
- 0 mA -12V
- 0 mA +5V
- 42mm depth

Special thanks to: **Phil Baljeu and the LZX team** for the Castle series of modules which have been the starting point to develop this module. **Lorenzo Ferronato** for the documentation design // And of course, **everyone who has supported Syntonie until now & those who will support it in the future.**



(P1) Bitswap manual control Ch. A
(P2) Bitswap manual control Ch. B
(P3) Bitswap manual control Ch. C
(P4) Bitswap CV Attenuverter Ch. A
(P5) Bitswap CV Attenuverter Ch. B
(P6) Bitswap CV Attenuverter Ch. C
(S1) Invert switch Ch. A
(S2) Invert switch Ch. B
(S3) Invert switch Ch. C

(J1) Signal input Ch. A
(J2) Signal input Ch. B (normalled to Ch. A)
(J3) Signal input Ch. C (normalled to Ch. B)
(J4) Bitswap CV input Ch. A
(J5) Bitswap CV input Ch. B (normalled to Ch. A)
(J6) Bitswap CV input Ch. C (normalled to Ch. B)
(J7) Bitswap CV output Ch. A
(J8) Bitswap CV out put Ch. B
(J9) Bitswap CV output Ch. C
(J10) Signal output Ch. A
(J11) Signal output Ch. B
(J12) Signal output Ch. C



Here is the block diagram of one channel of Isohélie, the two other channels are identical. It can be separated in two sections: the signal path and the control voltage path.

Signal path: the input signal is buffered and sent to the 3-bit ADC, which is composed of 8 comparators and an 8-to-3-bit priority encoder, the input signal is now quantized. Those 3 bits are then sent to the 3:3 multiplexer, which will swap them together, the multiplexer is controlled using the quantized signal coming from the CV path. Those swapped 3 bits are then summed together at the DAC stage, producing a stepped signal composed of 8 steps. Finally, this stepped signal either goes directly to the output or through an inverter, controlled using the front panel invert switch.

CV path: the CV signal is going through an attenuverter, which attenuates and/or inverts the signal based on the CV potentiometer position (fully clockwise: original signal at full amplitude, fully counter clockwise: inverted signal at full amplitude). The resulting signal is then summed to the bias/offset potentiometer, labelled BITSWAP, which offer manual control over the multiplexer that swaps the bits of the signal path. The resulting sum is going through a 3-bit ADC, which is identical to the one in the signal path, it will produce 3 signals that are used to control the multiplexer. When the BITSWAP is fully counter clockwise, the bits are in the original order, and can achieve 7 different swaps when turned clockwise.
Those 3 bits are also summed using a DAC and can be inverted using the invert switch. The invert switch controls both the signal and CV path inversion at the same time.

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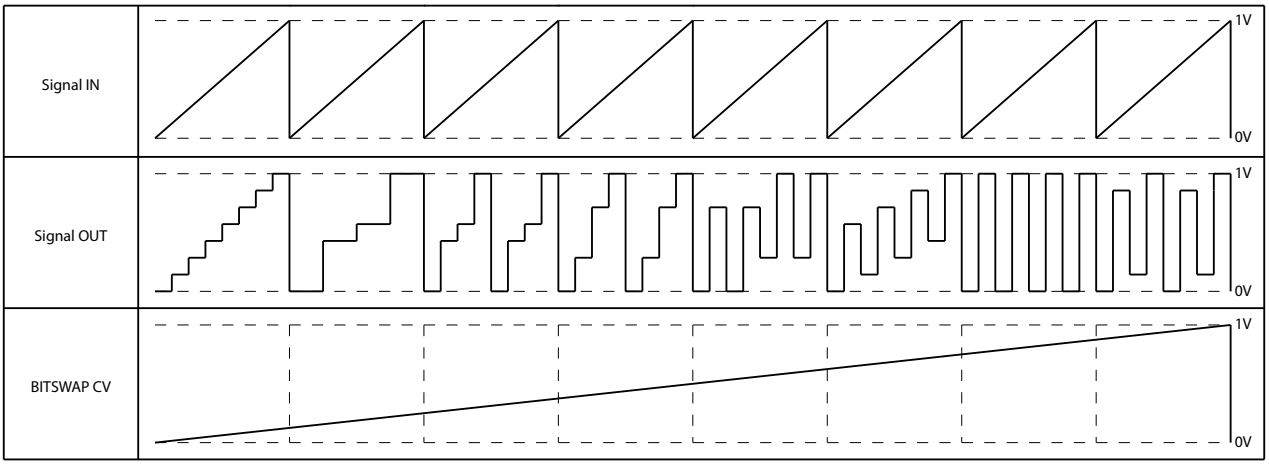

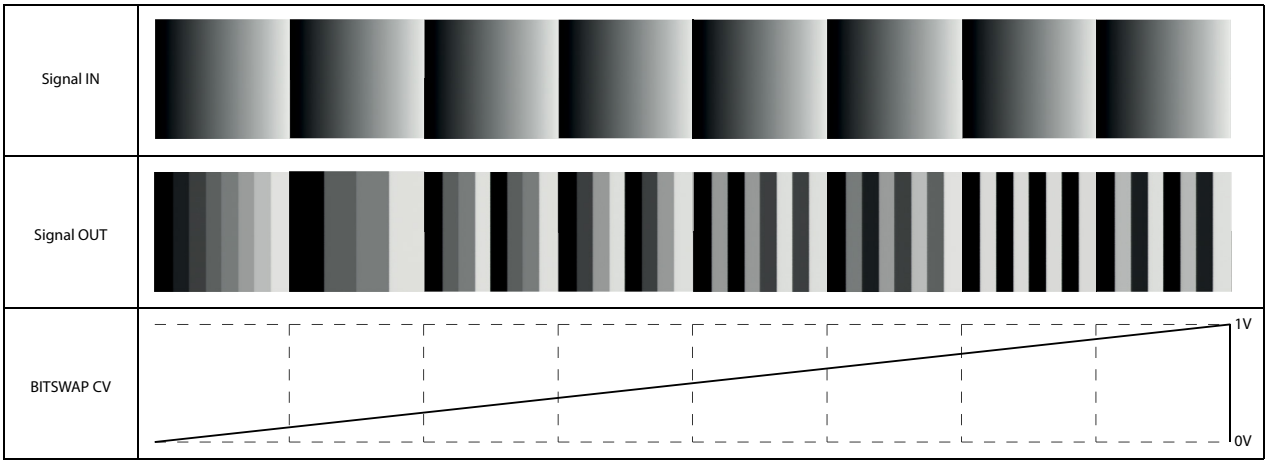

Graphic representation and video captures of the bitswap feature with a rising ramp as the input signal: as the bitswap CV signal rises from 0V to 1V, the signal out cycles through 8 different stepped wave shapes.

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