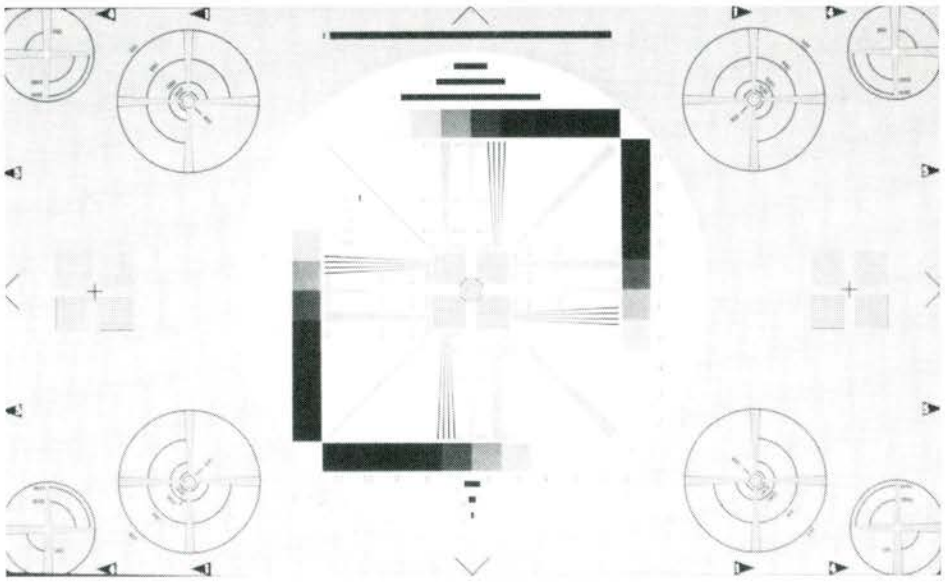
CHROMINANCE-LOCKED CLOCK GENERATOR



A remarkably simple solution is offered to a problem almost any constructor of a test card or callsign generator, logomat, graphics card, or any other video equipment must have been faced with at some time: phase synchronicity between clock pulses in the system and the chrominance subcarrier.
A PLL circuit is described that enables deriving the TV line and field frequency, and a number of other useful signals, from the chrominance frequency, 4.433 MHz. A mystery unravelled!

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In video equipment, the beneficial effects of phase-locking the central clock oscillator to the chrominance subcarrier are mainly the elimination of annoying digital interference and colour cross-patterning. The improvement can be noticed in the well-known colour bar test chart, in which colour transitions become sharply defined rather than blurred with bands of spurious lines and randomly moving coloured spots while longer lines are moving slowly and diagonally or horizontally across the screen.
In professional video systems and studios, complex equipment is available to ensure that all TV synchronization signals have a fixed phase relationship with the chrominance frequency, as set forth in the relevant CCIR specifications.

This article demonstrates how some thinking on the technical background of the PAL (*Phase Alternation Line*) and NTSC (*National Television System Committee*) TV systems, and a comparison between these in respect of possible interference, leads up to simple computer-assisted arithmetic and, finally, the design of a circuit that achieves the above objective of providing chrominance-locked, standard clock frequencies for digital video generators.

Choice of the chrominance subcarrier frequency

The PAL TV system is based on double-sideband modulation of the picture colour information onto a subcarrier of 4.433 MHz. This system is basically similar to that used for NTSC TV. The Y (luminance) signal is obtained by adding the three primary colours, red (R), green (G) and blue (B), in proportion, as

$$Y = 0.3R + 0.59G + 0.11B$$

The degree of luminance of each individual pixel determines its brilliance, black corresponding to minimum, and white to maximum luminance. For a monochrome TV set, the luminance signal is sufficient for producing a picture. A colour receiver, however, needs the three primary colours for mixing to give each pixel on the screen the correct colour. The colour receiver finds two modulated signals, R–Y and B–Y adjacent to the 4.433 MHz subcarrier. From these, the R, G and B signals are obtained by means of a number of

simple operations involving subtraction and addition. The R–Y and B–Y signals are quadrature-modulated on the 4.433 MHz carrier, so that the instantaneous phase provides a measure for the colour of a pixel, and the amplitude for the colour saturation. Since the colour subcarrier is found within the luminance band (0...5 MHz), its sidebands will become visible as a pattern of thin lines. In the NTSC TV system, this undesirable effect is minimized by using a colour subcarrier frequency that is an odd multiple of the line frequency. This gives rise to a dot pattern which is far less conspicuous and annoying than the line pattern that would be formed in the PAL picture (see Fig. 1).

In the PAL system, the phase of the modulated R–Y signal is inverted for every line in the picture. This causes two sidebands adjacent to the 4.433 MHz

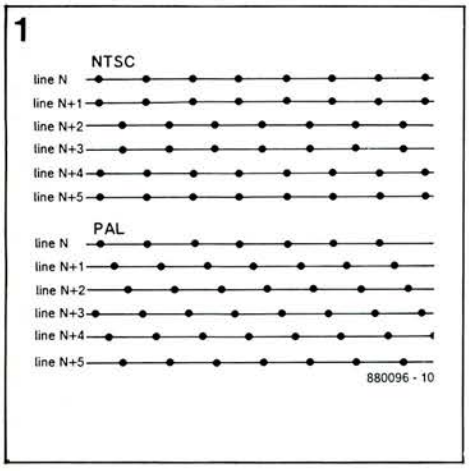

Fig. 1. Comparison between PAL and NTSC: luminance patterns caused by chrominance information.

subcarrier, at an offset corresponding to half the line frequency. When the subcarrier frequency is chosen such that it is an odd-numbered multiple of *half* the line frequency, B–Y information will result in a dot pattern, and R–Y information in a line pattern. To avoid this, the chrominance subcarrier frequency is an odd multiple of the line frequency divided by four (*quarter-offset*). Time-averaging of the remaining interference on a raster-by-raster basis is further achieved by adding 25 Hz (raster frequency) to the colour subcarrier, so that cross-interference between luminance and chrominance is least noticed. Summarizing the above, the optimum frequency of the chrominance subcarier, f_{chr}, becomes:

$$f_{chr} = (15{,}625/4) \cdot 1135 + 25$$
$$= 4{,}433{,}618.75 \text{ Hz}$$

corresponding to the line frequency multiplied by 283.7516. The deriving of the line frequency from the chrominance frequency would, therefore, require dividing this by 283.7516. This is impossible by electronic means, which only allows dividing by integers. Subtraction of 25 Hz, division by 1135 and subsequent multiplication by 4 is also very complex in terms of electronics. Reasonable accuracy is, however, obtained by approximation of the denominator, 283.7516.

Table 1.

```
1 REM chrominance-locked clock generator
5 REM successive approximation of clock divisors
10 K=4433618.75
20 INPUT''Enter output frequency '',F
30 H=K/F
40 P=H/(H-1)
50 B=1
60 FOR X=1 TO 1000
70 Y=P*X
80 A=ABS(Y-RND(Y,-1)/X
90 IF A>=B; NEXT X
100 IF A<B; B=A : D=RND(X*P,-1) : E=D-X : PRINT X,D,E
110 R=K/D*E : U=K/D
120 S=R/256-15625
130 PRINT R,S,U
140 NEXT X
```

Table 2.

Objective: f_o = 4 MHz

x	divisor *d*	divisor *e*	real output frequency [Hz]	deviation from 15,625 [Hz]	phase comparator frequency [Hz]
1	10	9	3,999,256.875	−38.05908	443,361.875
3	31	28	4,004,558.871	17.80809	143,019.9597
4	41	37	4,001,070.579	4.1819501	108,137.0427
5	51	46	3,998,950.245	−4.1006052	86,933.70098
9	92	83	3,999,895.177	−0.4094664	48,191.50815
31	317	286	4,000,047.2	0.1843761	13,986.17902
40	409	369	4,000,013.004	0.0507978	10,840.14364
49	501	452	3,999,991.367	−0.0337217	8,849.538423
89	910	821	4,000,001.092	0,0042657	4,872.108516
227	2321	2094	3,999,998.993	−0.0039341	1,910.219194
316	3231	2915	3,999,999.584	−0.0016247	1,372.21255
405	4141	3736	3,999,999.916	−0.0003293	1,070.663789
899	9192	8293	4,000,000.032	0.000125	482.3345028

Wanted: two denominators

Many digital video circuits have a central clock oscillator that runs at a multiple of 1 MHz. This is so arranged because the line frequency is then readily obtained with the aid of binary counters/dividers. For instance, when a clock of 4 MHz is available, 15,625 Hz is obtained by division by 256 ($=2^8$). The question is now: how can we relate 4,433,618.75 Hz to 4,000,000 Hz? The answer can be provided by a computer, programmed to find two integer denominators: one, *d*, for the chrominance frequency, and another, *e*, for the clock frequency. In other words, if the chrominance frequency is divided by *d*, and the result of this division is multiplied by *e*, 4,000,000 MHz should be obtained.

The BASIC computer program listed in Table 1 gave the results summarized in Table 2. Denominators 910 for *d* and 821 for *e* were found to yield a reasonable approximation of the target frequency whilst giving a practicable operating frequency for the phase comparator in the PLL to be designed. Also, these denominators allow relatively simple divider circuits to be used. The final deviation from 4,000,000 MHz is virtually negligible at +1.092 Hz.

Practical circuit

The above considerations lead up to the block diagram of Fig. 2. It is seen that 4 MHz is divided by multiples of 2 to obtain commonly used frequencies in digital video circuits. The chrominance frequency is multiplied by two to give 8.86 MHz, which is frequently required as a clock signal for IC-based colour generators.

Figure 3 shows the circuit diagram of the chrominance-locked clock generator, which is essentially a discrete phase-locked loop designed around commonly available parts.

The 4.433 MHz crystal oscillator is set up around gate N_5, whose output signal is fed to buffer N_1 and counter IC_3. This, together with bistable FF_1, divides the chrominance frequency by 910 to give 4.8721085 kHz. IC_3 counts 909 periods of the clock signal, while FF_1 delays 1 period (approx. 226 ns) during the resetting of the counter, giving the required divisor and allowing sufficient time for IC_3 to reset all internal bistables.

The 4 MHz L-C oscillator is a varicap-controlled Colpitts type set up around T_1, with T_2 and Schmitt-trigger gate N_4 acting as a buffer to obtain a digital compatible output signal.

Division by 810 in IC_4 is achieved in a manner similar to that in IC_3-FF_1 as discussed.

Gate network N_2-N_6-N_7-N_3 forms the phase comparator, while R_4-C_3 forms the loop filter with a roll-off of 7.2 Hz. The natural frequency of the PLL is 12.96 Hz, while the hold range is of the order of 150 kHz.

Construction and setting up

The circuit is fairly uncritical in respect of construction, and is simple to build on a small piece of Veroboard. Connections in the 4 MHz and 4.433 MHz oscillators should be as short as possible though, and due attention should be paid to decoupling of the positive supply line.

The only component that requires further discussion here is L_1. In the prototype, good results were obtained with a Neosid Type 7A0 inductor assembly. The required inductance of about 22 μH was achieved by winding 60 turns of 0.2 mm dia. enamelled copper wire onto the former. Do not use ready-made 4.433 MHz inductors with a built-in parallel capacitor, since this is often too large to ensure the relatively high L-C ratio required in this application. The 4.433 MHz crystal was a type salvaged from a colour TV chassis.

After building the circuit, it is recommended to commence testing the 4 MHz oscillator by temporarily breaking the PLL control loop. Disconnect R_4 from pin 4 of N_3. This enables checking the operation of the 4 MHz oscillator with the aid of an external tuning voltage obtained from the wiper of a po-

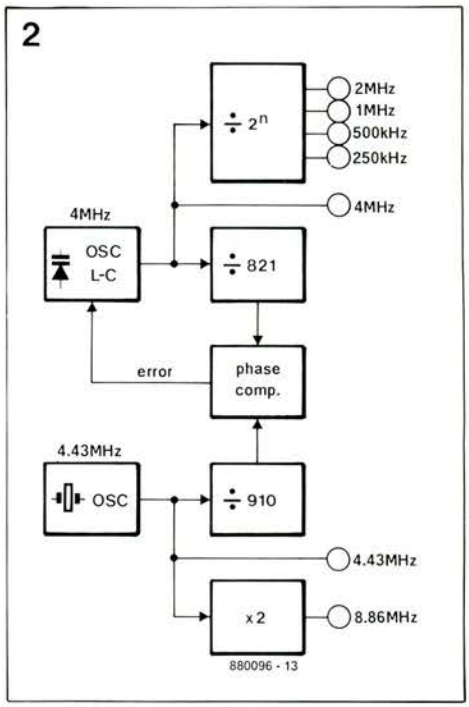

Fig. 2. Block diagram of the chrominance-locked clock generator for video systems.

Parts list

Resistors (±5%):
R_1 = 10M
R_2 = 120K
R_3;R_7;R_{11};R_{12} = 10K
R_4;R_6 = 100K
R_5 = 560K
R_8 = 12K
R_9 = 1K0

Capacitors:
C_1 = 100p
C_2 = 40p trimmer
C_3 = 220n
C_4;C_5;C_9;C_{10};C_{13} = 47p
C_6 = 68p
C_7;C_8;C_{11} = 100p
C_{12} = 1n0
C_{14};C_{15} = 100n

Inductors:
L_1 = winding details are given in the text. Neosid Type 7A0 (Neosid Limited • Icknield Way West • LETCHWORTH SG6 4AS. Telephone: (0462) 481000. Telex: 826405. Contact Mr. E. Adcott). Neosid inductors are also available from C-I Electronics.
L_2 = 13μH with centre tap (see text).
L_3 = 7μH with centre tap (see text).

Semiconductors:
D_1 . . . D_{11} incl. = 1N4148
D_{12} = BB105
D_{13};D_{14} = AA119
IC_1 = 4093
IC_2 = 4001
IC_3;IC_4 = 4040
IC_5 = 4013
IC_6 = 4516
T_1;T_2 = BF199

Miscellaneous:
X_1 = quartz crystal 4.433 MHz.

It is regretted that a printed-circuit board for this project is not available.

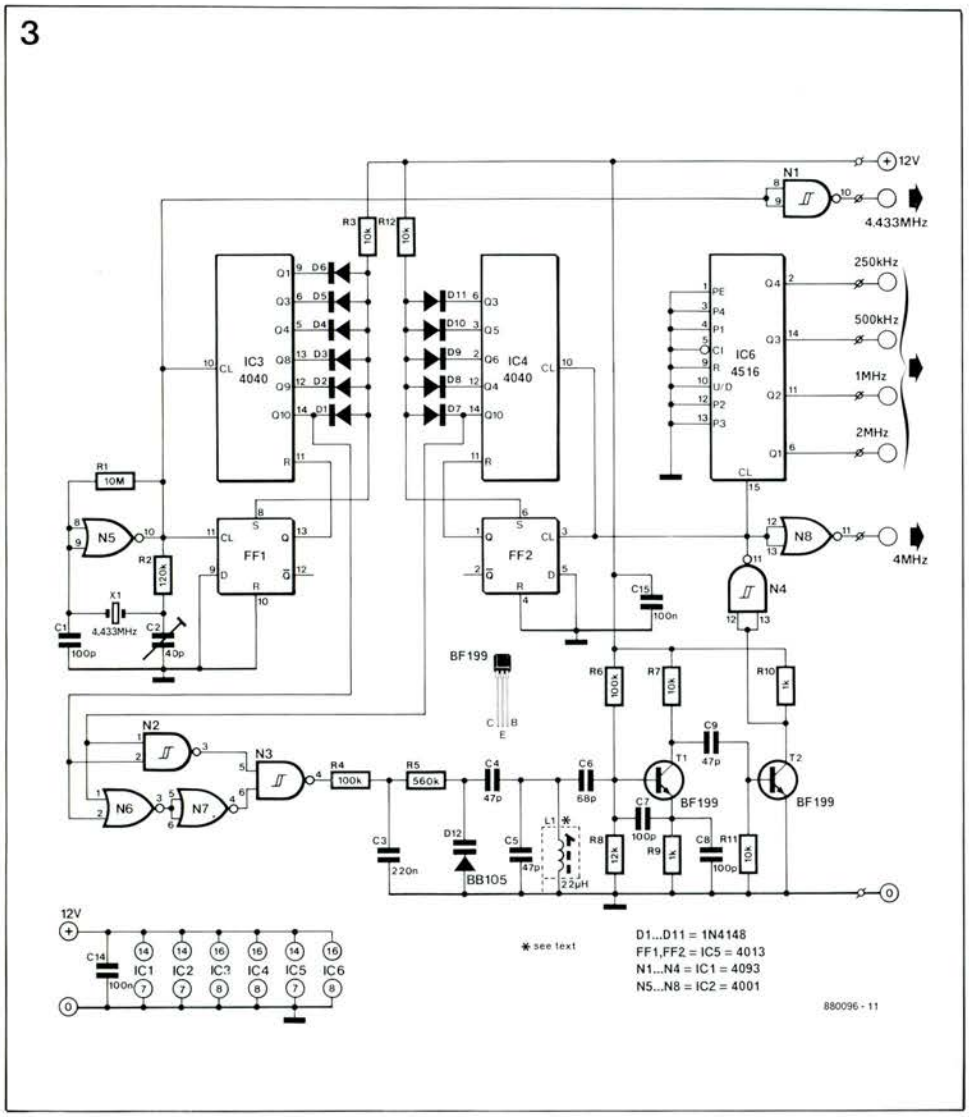

Fig. 3. The clock generator is essentially a discrete phase-locked loop.

tentiometer connected between +12 V and ground. To begin with, adjust L_1 so that oscillation is achieved around 4 MHz. Check that the oscillator can be tuned with the potentiometer. The output of N_4 should supply CMOS-compatible clock pulses. It is essential that these pulses have the full CMOS swing of about 12 V_{pp} when the oscillator is tuned around 4 MHz. Do not add too much capacitance to the parallel tuned circuit when its resonance frequency is found to be too high: instead, ensure more inductance by increasing the number of turns on L_1.

Next, adjust trimmer capacitor C_2 to give 4.43362 MHz at the buffered output. Measure the frequency at pin 2 of N_2 — this should be 4.8721085 kHz. Similarly, measure the frequency at pin 1 of N_2 to check the operation of IC_4-FF_2. Tune the oscillator to obtain about 4.8 kHz here.

When these tests check out, it is time to close the loop by removing the potentiometer, and connecting R_4 to the output of N_3. Connect the frequency meter to the 4 MHz output. Some readjustment of L_1 may be required to get the PLL to lock.

The oscilloscope photographs of Fig. 4 may be used as guidance if difficulties are encountered in the setting up. The upper two traces show the 4.8 kHz signals at the inputs of the phase comparator, i.e., pins 1 and 2 of N_2 (or N_6), the lower trace the phase comparator output (pin 4 of N_3). Although the latter signal is different in the photographs, the PLL was locked in both conditions, with only L_1 set differently within the hold range of the oscillator. It is clearly seen that the phase comparator is essentially an exclusive NOR function: the output goes low only when the two input signals are different.

The operation of the PLL can be checked by carefully adjusting L_1 while monitoring the phase comparator output with an oscilloscope. It will be found that the PLL loses lock when the pulses become significantly narrower than those in the lower trace of Fig. 4b. When the PLL is locked, L_1 can be adjusted over a small span while the output frequency remains stable at 4.000002 MHz (7-digit resolution).

Finally, switch the power to the circuit on and off a few times to verify that the PLL starts and locks properly. All drift on the 4 MHz output is, of course, caused by drift of the quartz crystal frequency. It is, therefore, recommended to make the final adjustment of C_2 and L_1 after a warming-up period of about 10 minutes.

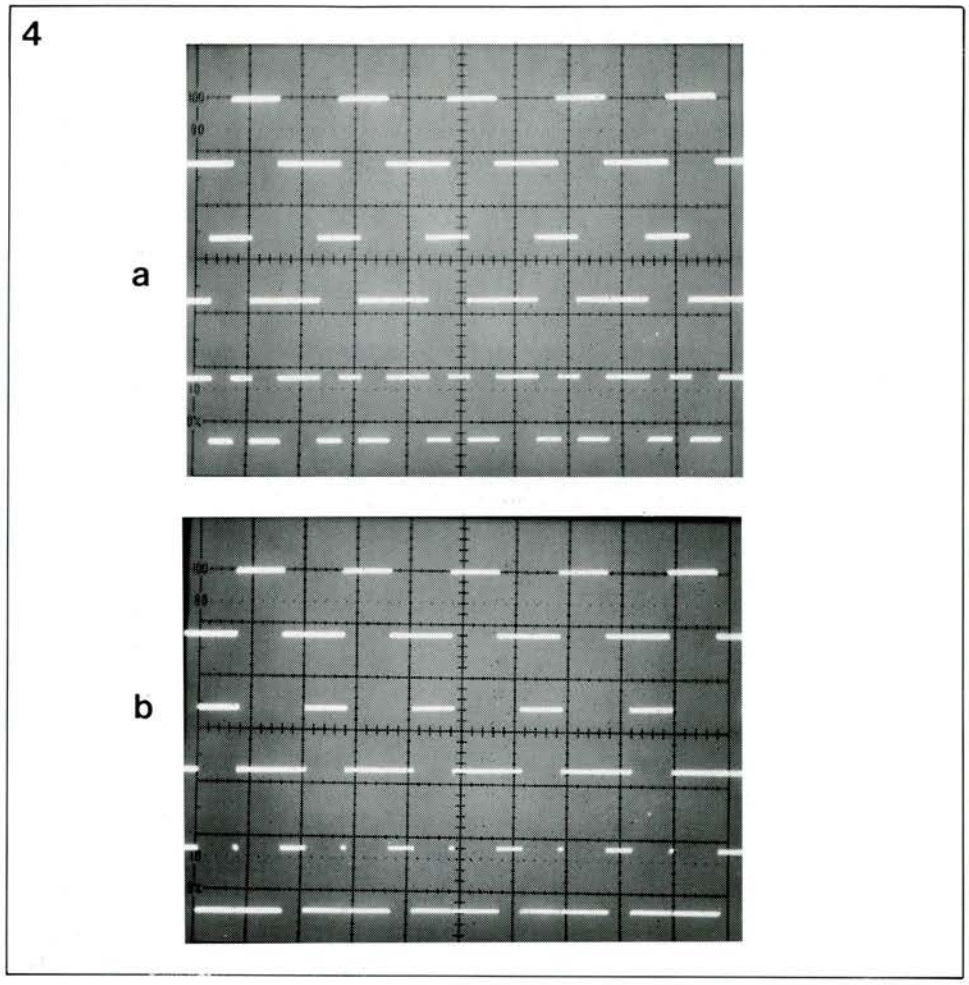

Fig. 4. Oscillograms showing the operation of the XNOR phase comparator.

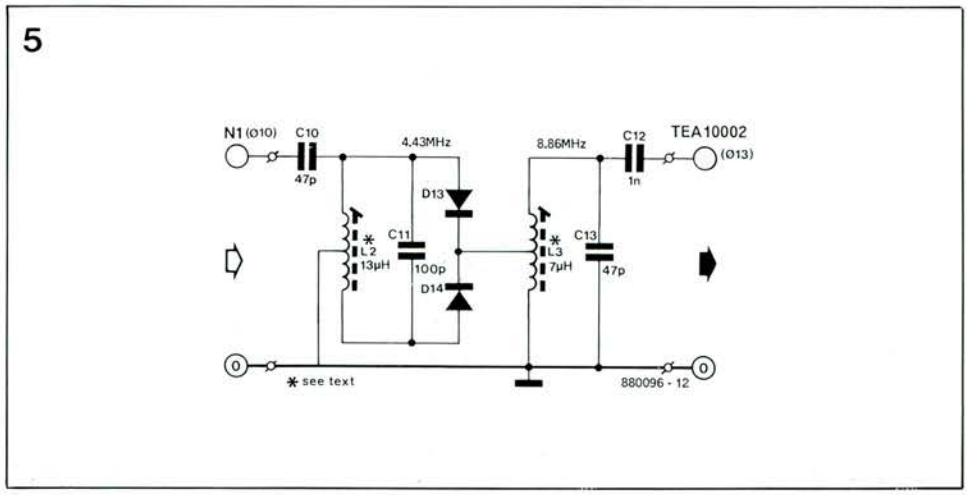

Fig. 5. Frequency multiplier circuit for driving the Type TEA1002 colour generator.

Multiplier for TEA1002

The circuit described is used by the author as part of a digital test chart and call-sign generator for amateur television. The system incorporates a TEA1002 colour generator chip (Ref. [1]) which requires an input signal of 8.86 MHz. The circuit of Fig. 5 multiplies the buffered crystal oscillator output of the chrominance oscillator by two to obtain this frequency. The multiplier is essentially a double-phase rectifier with a parallel-resonant L-C output filter. Suggested diode types are AA119 or OA95 (in any case, germanium types should be used). L_2 and L_3 are wound as 30 and 20 turns respectively of 0.2 mm dia. enamelled copper wire, with a centre tap. It is also possible to use ready-made inductors provided they are known to have a centre tap and the correct inductance (use a grid-dipper to check the in-circuit resonance frequency). Both L_2 and L_3 are simply peaked for maximum amplitude of the 8.86 MHz output signal. *Bu*

Reference:

[1] Video combiner. *Elektor Electronics* February 1984, p. 2-36 ff.

For further reading:

Principles of PAL Colour Television. H. V. Sims, London Iliffe Books Ltd. 1969.
Phase-lock techniques. F. M. Gardner, John Wiley & Sons Inc. 1966.