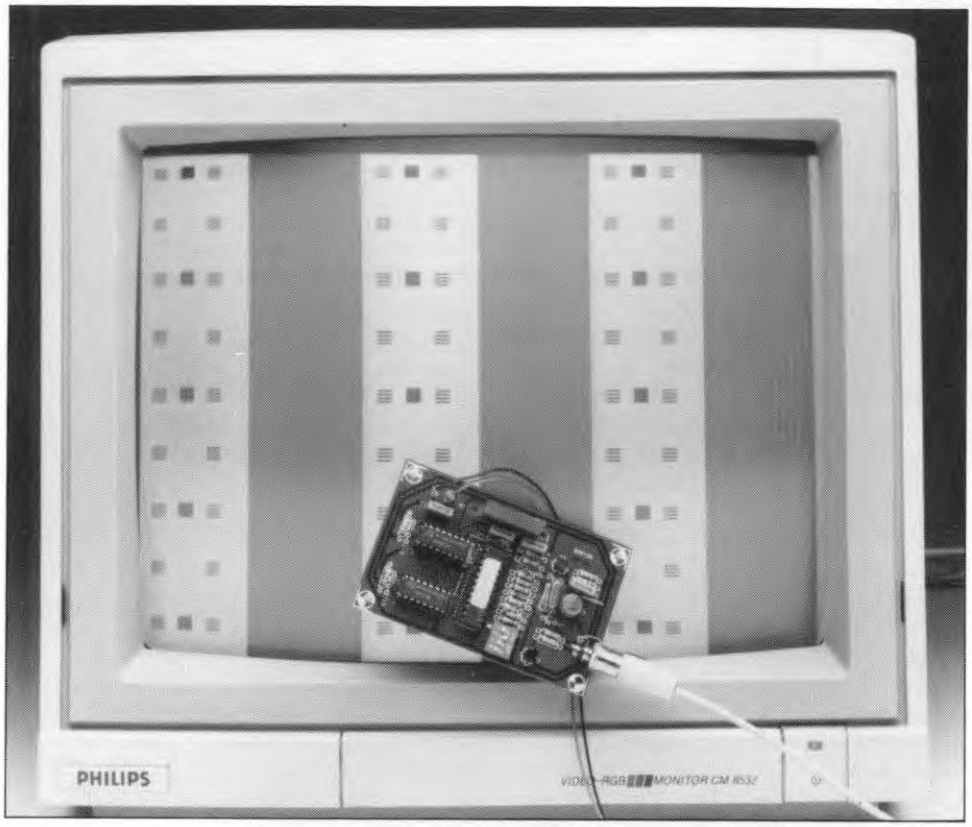
PAL TEST PATTERN GENERATOR



BRIEF SPECIFICATION

- Quartz controlled for optimum stability
- Four test patterns:
  - green (225°)
  - orange (134°)
  - green with 4 white bars
  - orange with 4 white bars
- Based on readily available components
- Simple to adjust
- Compact design using one GAL
- Digital RGB-csync outputs

A stable reference signal is essential whenever you want to adjust a television or a video monitor. Special integrated circuits have been developed that enable a PAL/NTSC colour test pattern generator to be built from a minimum of components. Unfortunately, these ICs are generally expensive as well as hard to obtain, and that is why we propose to do without one for a change.

Design by W. Foede

A number of PAL test chart generators were published in this magazine over the past few years. These circuits are generally based on integrated PAL encoder ICs to ensure that all synchronization signals are correctly timed. The entire sync processor is thus contained inside a single IC, which affords good repeatability of a circuit for home construction.

The test pattern generator described here is based on remarkably few components: two digital counters Type HC4040, a GAL (generic array logic) Type 20V8 and a handful of discrete components to furnish the central clock frequency. The GAL is the central part — here, it forms a kind of junction between a number of clock signals, which are combined into a usable video signal. The design concept of the test pattern generator is illustrated in the block diagram shown in Fig. 1. All synchronization signals are generated digitally, and derived from a single quartz crystal, which ensures accuracy, stability and fixed phase relationships (those of you who have ever tried to design a test pattern generator will confirm the importance of these features). The divide-by-two scaler in the lower left-hand corner of the diagram supplies the PAL chrominance ('colour') subcarrier frequency of 4.433 MHz. It is followed by an XOR gate which supplies a 90° phase-shifted copy of this signal. The section marked as 'PAL switch' determines whether the pulse shaper is fed with the 0° signal or the 90° phase shifted signal. The pulse shaper serves to combine the colour subcarrier with the horizontal and vertical synchronization signals.

The output of the PAL test pattern generator supplies a standard CVBS (chrominance-video-blanking-synchronization, or 'composite video') signal with a level of 1 V into 75 Ω, which corresponds to the load impedance presented by most video recorder and TV video inputs. The second output of the generator supplies TTL-level R, G and B (red, green and blue) signals, along with the combined synchronization pulses. These separate output signals are particularly useful for testing colour monitors.

Colour generation

Generating the colours is the most critical process in the test pattern generator. In a PAL (phase alternating line) encoded video signal, the chrominance ('colour') component, C, is conveyed to the receiver with the aid of a subcarrier at 4.43361875 MHz. This carrier is amplitude-modulated by the colour saturation information, and phase-modulated by the colour information. These two functions rather complicate the design of a good test pattern generator. In particular, due care must be taken to ensure that the subcarrier frequency and the colour burst are sufficiently stable.

In the PAL system, the colour burst is transmitted during the horizontal blanking period (A-H in Fig. 2). It is positioned in the so-called back porch period, and starts 5.6 µs after the falling edge of the line sync pulse. The burst itself consists of 12 periods of the chrominance subcarrier frequency. The phase shift of these periods alternates every other line between 135°

and 225°, which corresponds to a phase shift of 90° (Fig. 3). The phase switching operates at half the line frequency, or 7.8125 kHz. The burst contains two synchronization signals. The average phase shift of 180° serves to synchronize the 4.43 MHz oscillator in the TV set, while the phase changes synchronize the phase switch circuitry contained in the colour decoder.

The line (or 'horizontal') frequency, f_h, and the colour subcarrier frequency, f_c, have a fixed relation:

$$f_c = 283.75\, f_h + 25.$$

Further details on this relation may be found in Ref. 1. In the present generator, this relation is approximately correct by using an offset of 284. This means that the line frequency becomes the quartz frequency divided by two times 284, or

$$f_h = 8.86\ \text{MHz}/568 = 15{,}611\ \text{Hz}.$$

It is necessary to use the factor of two because the crystal used supplies a frequency of two times the desired colour subcarrier frequency (4.43 MHz). This clock frequency of 8.86 MHz makes it much easier to generate a phase shift of 90°. The divide-by-568 function is realized by a counter, IC3 (see the circuit diagram in Fig. 5.). The use of the factor 284 instead of 283.75 has an important advantage during measurements. The fact that the line frequency is coupled to an even number of colour subcarrier periods enables the 'TV line' trigger mode found on many oscilloscopes to be used when viewing the colour burst and related signals in a TV set.

According to the CCIR standard, a PAL television signal has 312.5 lines in every raster. Two rasters are interlaced to form one complete picture or frame. The half line (312.5) allows an easy transition to be made from one raster to another. Interlacing is, however, not generally desirable on test patterns, and is therefore not implemented in the present circuit, which supplies an even number of lines per raster. Based on a line frequency of 15,611 Hz and 312 lines per raster, we obtain a field frequency of 50.036 Hz. The deviation of 0.036 Hz from the standard 50 Hz has no practical significance. The colour signal changes phase (135°/225°) in unison with the burst signal, at a rate equal to half the line frequency. In general, the phase required for the colour is processed during the 135° burst. In terms of the colour signal, this phase shift corresponds to 'orange'. The PAL switch causes this signal to be changed from 135° to 225° by 'mirroring' it against the 0-180° reference (*x*-axis). Thus, the original 135° (180°–45°) becomes 225° (180°+45°). In the receiver, the new signal phase must be processed in the reverse way to ensure that the original colour is restored. Without this phase reversal, orange and green would appear alternately. The 90° phase reversal on every alternate line is the characteristic difference between the PAL and NTSC (National Television Standards Committee) TV systems. The advantage of PAL over NTSC is that the system is capable of counteracting static phase changes, which would cause colour instability. NTSC does not allow for phase correction, and the acronym is often jocularly said to stand for 'Never The Same Colour'.

If we limit the number of colours supplied by the test pattern generator to two, orange (135°) and green (225°), all that is required are the two 90° phase shifted signals supplied by the previously mentioned 8.86-MHz central clock oscillator. This oscillator is quartz controlled, and has only one transistor. It is a standard design used in many colour TV receivers. Obtaining two 90° phase-shifted clock signals, and halving the central clock frequency is achieved with an XOR gate and a bistable, which are contained in the GAL. The timing of the signals at the input and output of the digital divider and the phase shift circuit is shown in Fig. 4. The operation of the XOR gate is illustrated further in the top right hand corner of the diagram.

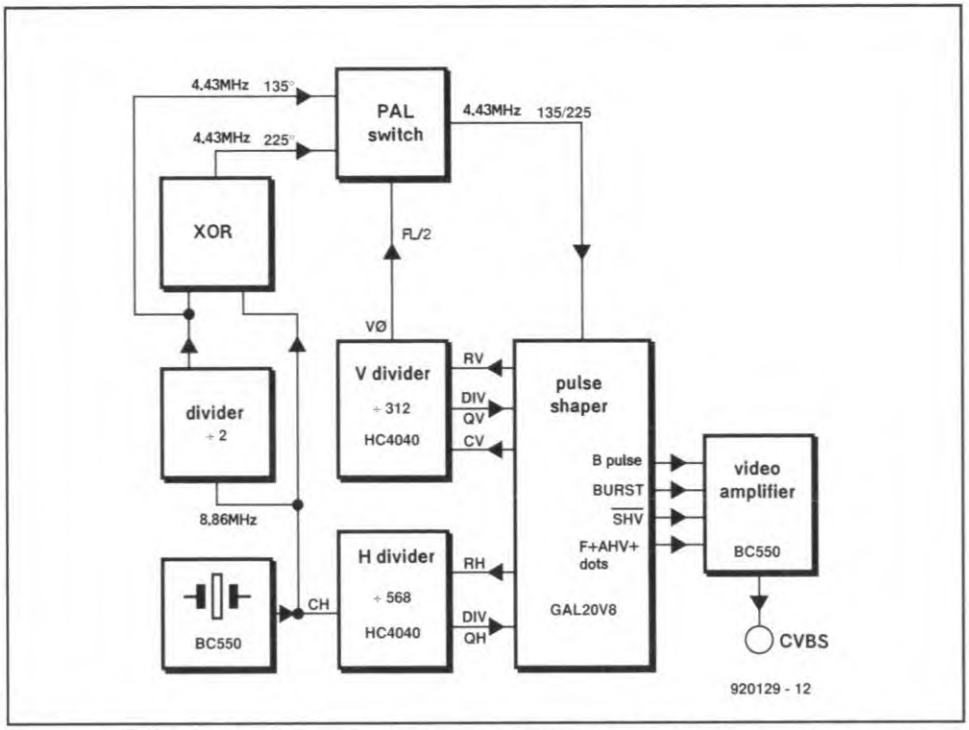


Fig. 1. This block diagram shows the sub-sections of the test pattern generator. Not all blocks are found back in the actual circuit as ICs or active components. This is because most functions indicated here are contained in a GAL (generic array logic) device.

TIMING SPECIFICATION

PAL encoded test signals:
(1). green (225°) or orange (135°).
(2). as (1), but with 4 white vertical bars.

Quartz frequency:	8.88672375 MHz
Colour subcarrier:	4.43361875 MHz
Line frequency:	15,611 Hz (Δ = –14 Hz)
Field frequency:	50.036 Hz (Δ = +0.036 Hz)
Line sync pulse:	4.5 µs (Δ = –0.2 µs)
Front porch:	2.7 µs (Δ = +1.2 µs)
Line blanking:	14.4 µs (Δ = +2.4 µs)
Start of burst:	5.4 µs (Δ = +0.2 µs)
Burst length:	2.7 µs (Δ = +0.45 µs)
Field sync pulse:	0.5 ms (Δ = +0.35 ms)
Field blanking:	1.5 ms (Δ = 0.1 ms)

Deviations (Δ) relative to CCIR recommendation 470 and Report 624.

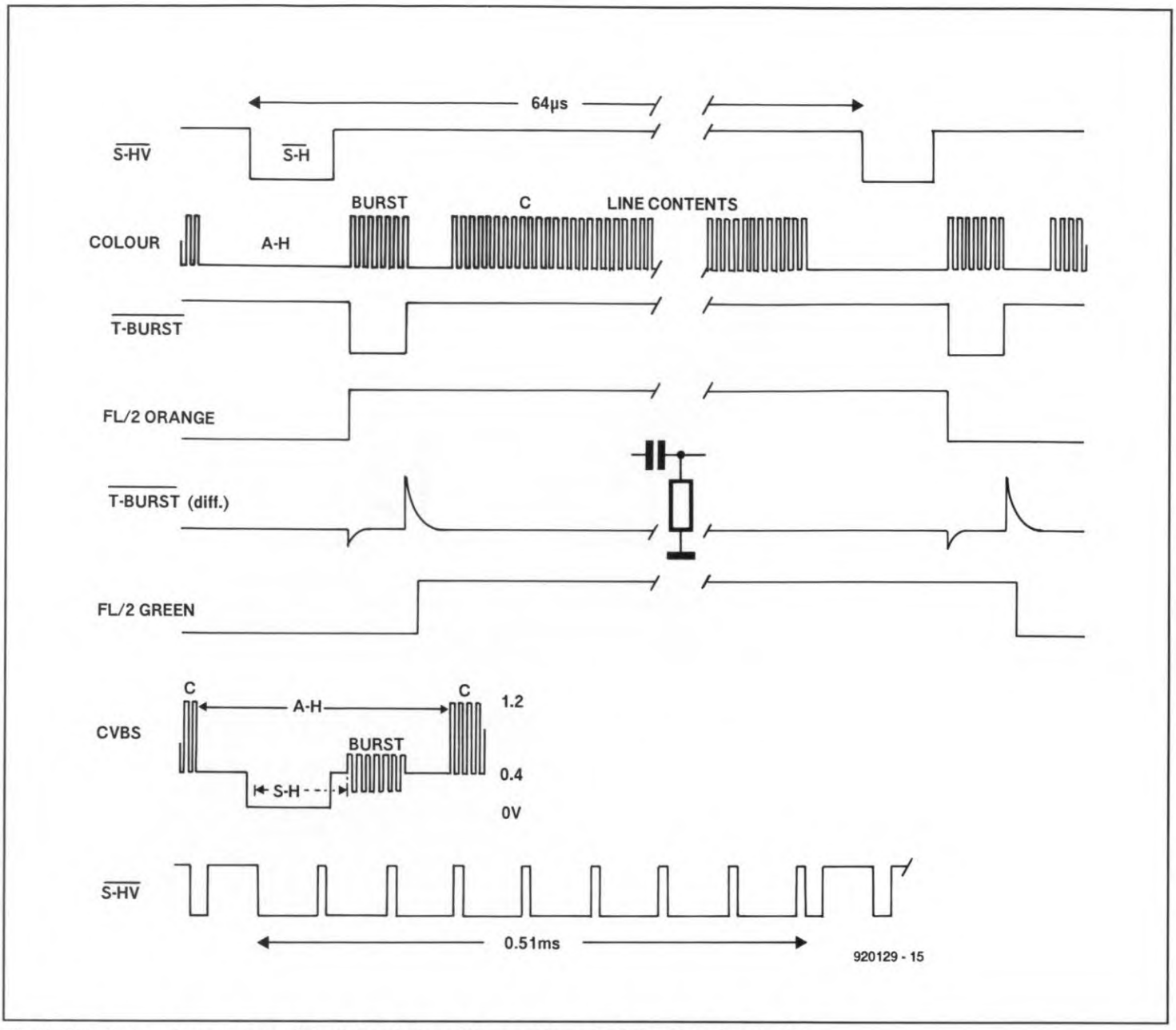


Fig. 2. This timing diagram shows the relation between the most important signals in the circuit.

The burst and the colour signal can have two combinations: either they have the same phase (orange), or they have a phase difference of 90° (green). The selection between these two colours is made with switch S1.

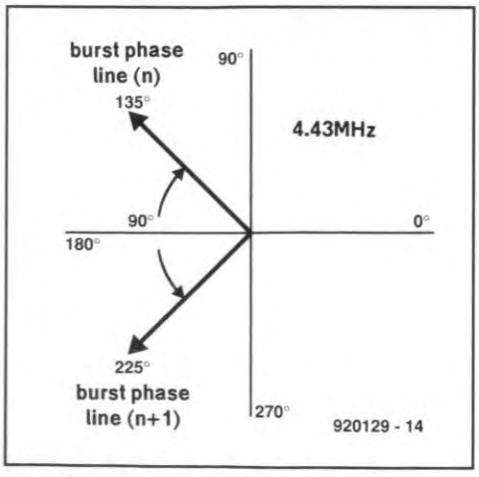


Fig. 3. The phase of the colour burst changes between 135° and 225° every alternate picture line.

The 'vertical' counter, IC2, is clocked with the line frequency, for which the burst pulse (T-burst\) is used. The Q0 output of IC3 supplies the FL/2 signal, i.e., half the line frequency. When T-burst\ is not inverted, the phase is switched before the burst, which results in an orange picture. By contrast, when T-burst\ is differentiated by C2-R2, (Fig. 3, centre), the phase changes a little later, between the burst and the colour signal (Fig. 2). The result is a green test picture.

Inside the GAL

The ready-programmed GAL in the circuit generates a number of digital signals: the inverted burst pulse (T-burst\), the inverted composite synchronization signal (S-HV\) and the composite burst/colour signal (C). These three signals are added in a passive matrix circuit R7-R8-R9-D1, and subsequently buffered by emitter follower T1. Resistors R3 and R4 enable the emitter follower to provide the required source impedance (75 Ω) and signal level (1 V_{pp}). The burst is given the appropriate level and offset by a clipper, R9-D1. These two parts function only when the T-burst signal is active.

The fact that the 4.43 MHz signal is rectangular need not worry us too much. In general, the bandwidth of video amplifiers in video recorders and TV sets is limited to about 8 MHz, so that harmonics of the 4.43-MHz signal do not cause problems.

The line and dot patterns in the test chart have the 4:3 format. There is, however, one flaw in the test pattern: the picture is shifted by 0.3 µs. In

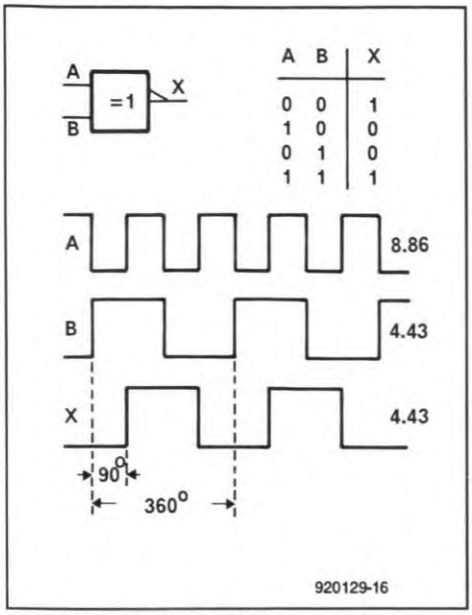
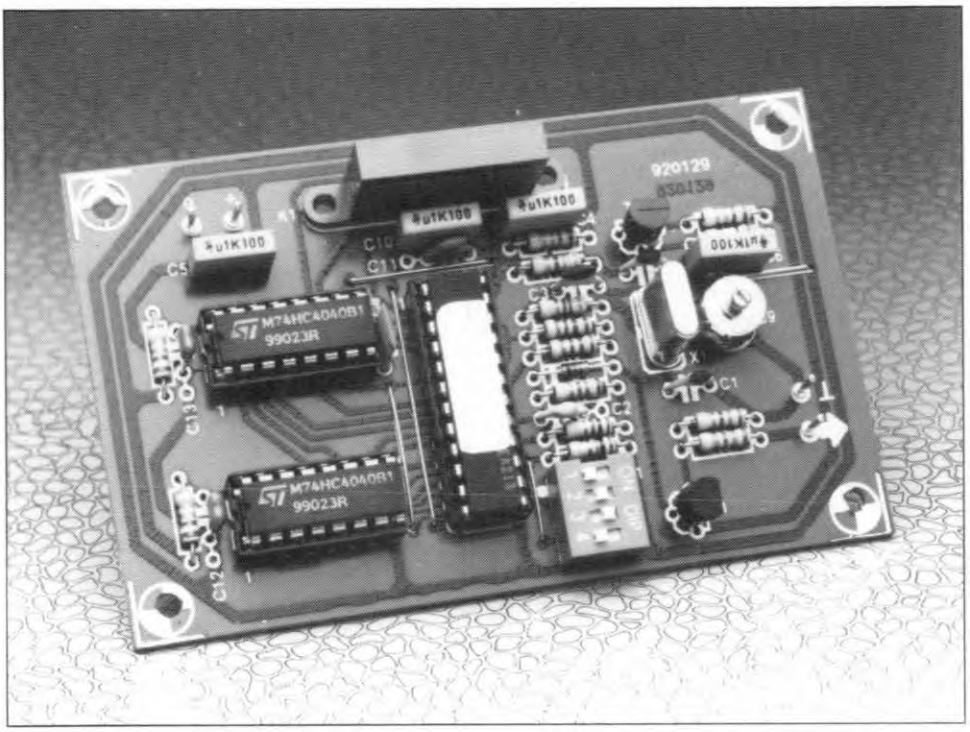


Fig. 4. A bistable (divide-by-two device) and an XOR gate supply two 90° phase shifted signals that are required for the picture generator.



practice, this means that the pattern is not exactly centred on the screen. However, this is not visible from a distance.

Finally, the signals S-HV, R, G and B (Fig. 6) are available with TTL levels on connector K1. These signals also take into account the blanking period, A-H. It should be noted that the signals on K1 are suitable for driving high-impedance inputs only. Buffers such as the HC4049 or the HC4050 are required when low-impedance loads are to be connected — the GAL itself it **not** capable of supplying enough current to drive inputs with an impedance of 75 Ω.

Construction and test

The track layout and component

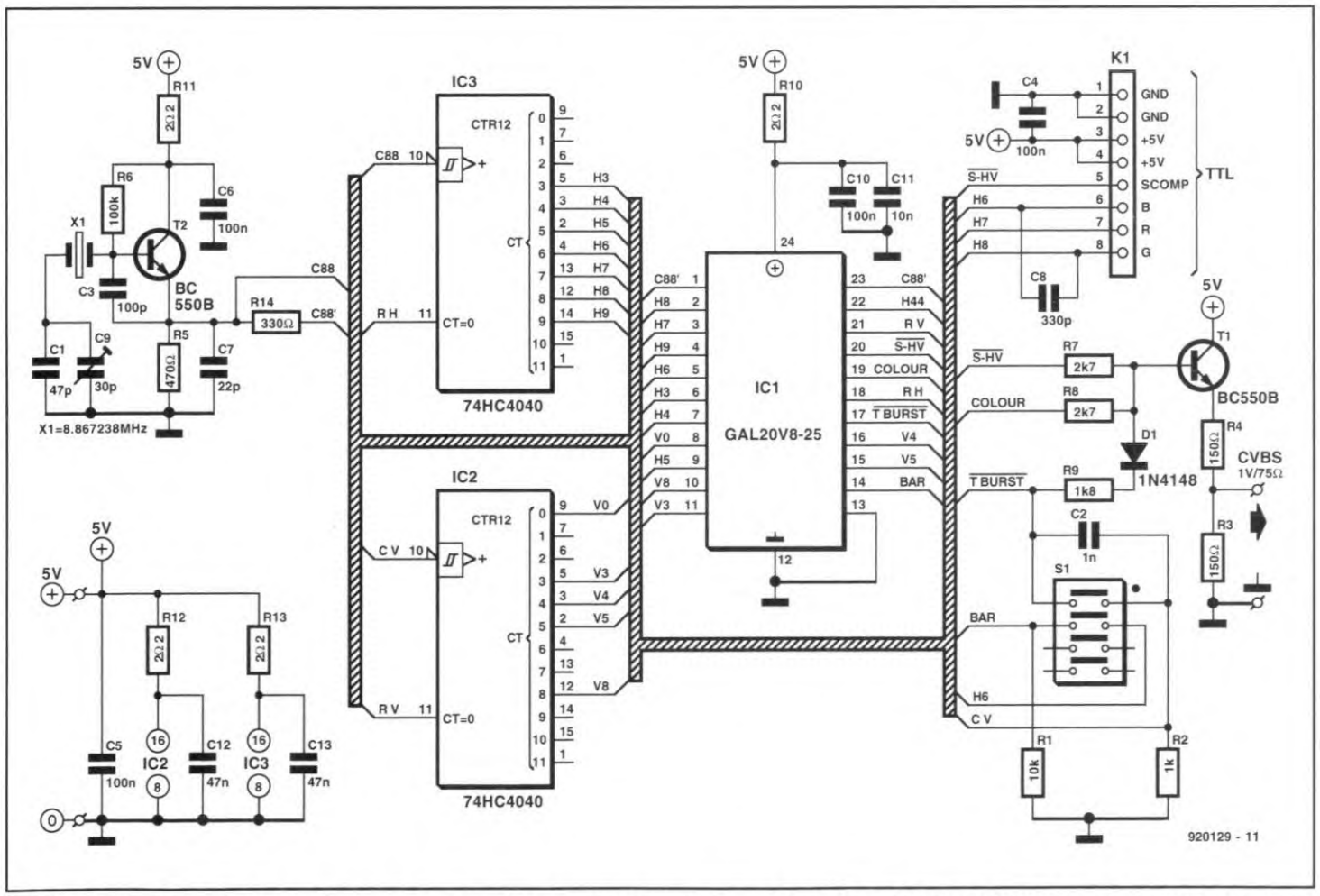


Fig. 5. Circuit diagram of the test pattern generator. Most functions are performed by a single GAL Type 20V8, which is available ready-programmed through our Readers Services.

mounting plan of the printed circuit board designed for the test pattern generator is shown in Fig. 7. Since the circuit operates at relatively high frequencies, construction on, for example, veroboard or stripboard is not recommended. To minimize cross-effects between various sections of the circuit, the dividers (IC2 and IC3) and the GAL (IC1) have individual supply decoupling networks. The *R-C* networks used prevent the ICs from affecting each other's operation via the power supply.

When purchasing components for this project, make sure to use HC types, **not** HCT types, for IC2 and IC3. The DIP switch, S1, may be replaced with two miniature switches which are fitted on the case front panel. The wires between these switches and the board must be kept as short as possible — not longer than a couple of centimetres! The same goes for the wires between the PCB and the output socket.

The adjustment of the circuit is limited to trimmer capacitor C9 in the quartz oscillator. This setting is not critical, and easily carried out with the aid of a properly working TV set. Connect the output of the generator to the CVBS (composite video) input pin on the SCART plug. Adjust C9 until the colours are stable. The 'lock-and-track' characteristic of the colour decoder inside the TV makes the adjustment of C9 relatively broad. If you are fortunate enough to have access to a frequency meter, connect it to the H44 signal (pin 22 of the GAL), and adjust C9 for a reading of 4.43361857 MHz.

The test pattern generator is not critical in regard of its power supply: all that is needed is a regulated 5-V source capable of supplying an output current of about 60 mA.

The coloured screens supplied by the generator are well suited to checking the operation of sub-circuits in the TV that have to do with the colour processing. In particular, we refer to the colour decoder. The white vertical bars supplied by the generator allow you to check the TV's linearity, focussing and picture position. The bars are selected by the second switch contained in S1. The test pattern then produced is shown in the introductory photograph. ■

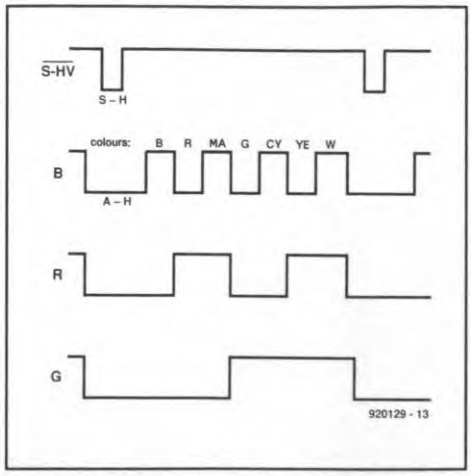


Fig. 6. Timing of the signals at the TTL output (R, G, B and the composite H/V syncs). These signals may be used to put a test pattern with white bars on a colour monitor.

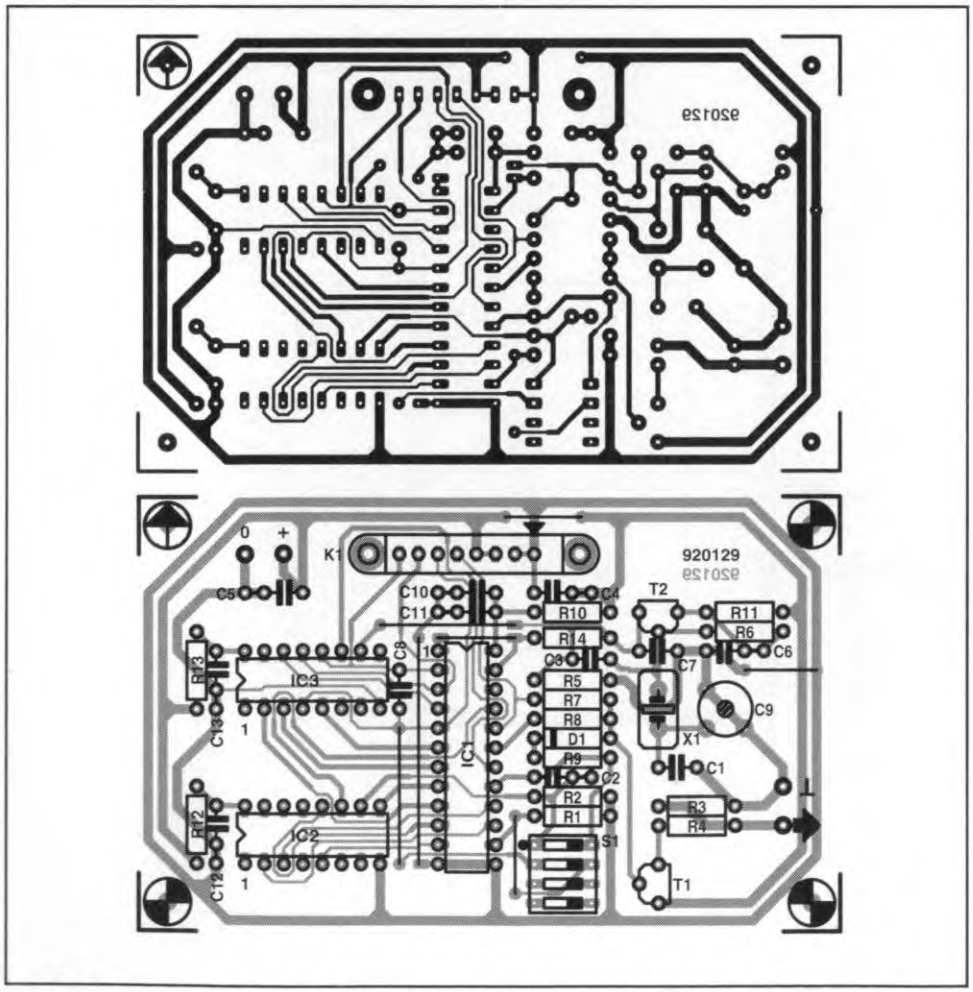


Fig. 7. Track layout (mirror image) and component mounting plan of the printed circuit board designed for the test pattern generator.

Reference:

1. 'Chrominance-locked clock oscillator'. *Elektor Electronics* July/August 1988.

For further reading:

Colour Television (System Principles, Engineering Practice, Applied Technology). By Geoffry Hutson, Peter Shepherd and James Brice. McGraw-Hill, 1990. ISBN 0-07-084199-3.

COMPONENTS LIST

Resistors:

1	10kΩ	R1
1	1kΩ	R2
2	150Ω	R3;R4
1	470Ω	R5
1	100kΩ	R6
2	2kΩ7	R7;R8
1	1kΩ8	R9
4	2Ω2	R10-R13
1	330Ω	R14

Capacitors:

1	47pF	C1
1	1nF ceramic	C2
1	100pF	C3
4	100nF	C4;C5;C6;C10
1	22pF	C7
1	330pF	C8
1	30pF trimmer	C9
1	10nF ceramic	C11
2	47nF ceramic	C12;C13

Semiconductors:

1	1N4148	D1
2	BC550B	T1;T2
1	GAL20V8-25 (order code ESS6211; see page 70) *	IC1
2	74HC4040	IC2;IC3

Miscellaneous:

1	8-way SIL pin header	K1
1	4-way DIP switch	S1
1	8.867238 MHz quartz crystal	X1
1	Set of printed circuit board and GAL (ready-programmed). Order code: 920129 (see page 70).	

* contained in set 920129

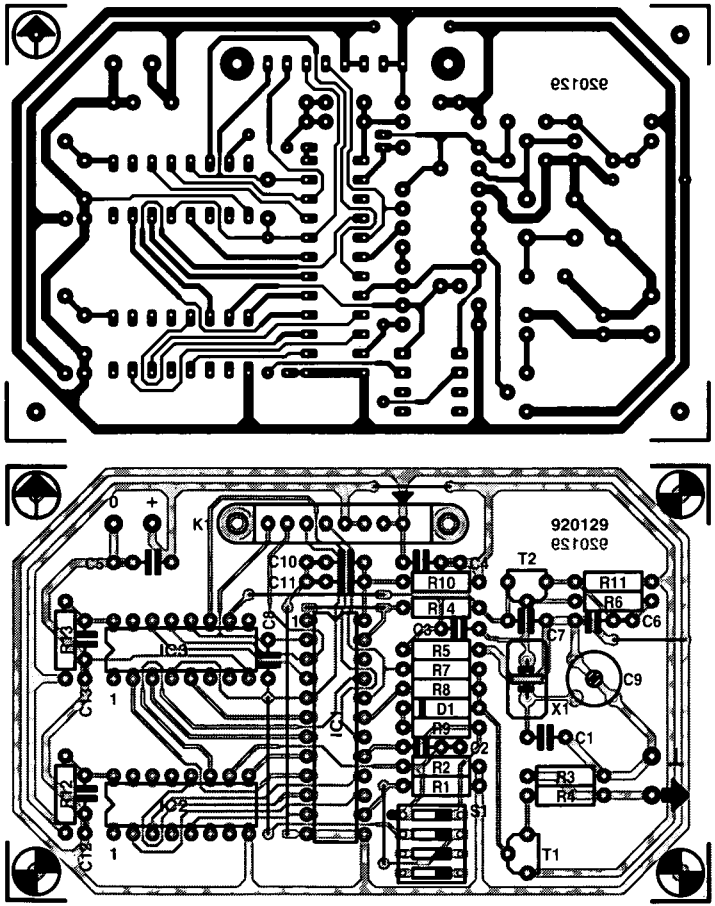


Fig. 7. Track layout (mirror image) and component mounting plan of the printed circuit board designed for the test pattern generator.

2	150Ω	R3;R4
1	470Ω	R5
1	100kΩ	R6
2	2kΩ7	R7;R8
1	1kΩ8	R9
4	2Ω2	R10-R13
1	330Ω	R14

Capacitors:

1	47pF	C1
1	1nF ceramic	C2
1	100pF	C3
4	100nF	C4;C5;C6;C10
1	22pF	C7
1	330pF	C8
1	30pF trimmer	C9
1	10nF ceramic	C11
2	47nF ceramic	C12;C13

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