# RGB-TO-CVBS CONVERTER RFK7000


**This RGB-to-CVBS converter, designed by ELV GmbH, accepts digital as well as analogue RGB signals from computer systems, and supplies a composite output signal suitable for driving a monitor, a PAL-compatible TV set with SCART input, or a video recorder.**

Nearly all of today's home computers and personal computers (PCs) are capable of supplying RGB (*red-green-blue*) output signals for driving a colour monitor. The RFK7000 RGB-to-CVBS (*chrominance-video-blanking-synchronisation*) converter allows computer-generated colour pictures to be recorded on a VCR, or displayed on a TV set, which normally has a greater screen size than a computer monitor. This brings interesting applications related to 'televised' demonstrations, multi-display networks, etc. within reach of the computer enthusiast with an interest for graphics applications.

## Connecting the converter

The RFK7000 has 4 connectors on its rear panel:

**BU1:**
This socket accepts a 3.5 mm jack socket via which the unregulated 12 V d.c. supply voltage is applied to the converter.

**BU2:**
This SCART socket takes the 3 analogue RGB signals at an amplitude of about 1.5 $V_{pp}$. Analogue RGB signals allow an almost infinite number of colour combinations to be displayed.

**BU3:**
Via this SCART socket, the RFK7000 supplies the CVBS signal to the TV set or video recorder. A potentiometer allows the CVBS output level to be adjusted over a wide range.

**BU4:**
A 9-way sub-D connector accepts the digital RGB signals at TTL level supplied by the computer. The 3 signal lines and the associated Intensity line give a maximum of 16 colours.

The supply input of the RFK7000 is connected to a mains adapter with 12 V d.c. output. The SCART output is connected to the CVBS (composite-video) input of the video recorder, monitor or TV set. Either BU2 or BU3 is used to drive the RFK7000: BU2 for analogue, BU3 for digital, RGB sources.

Optimum picture quality is achieved by adjusting the VIDEO LEVEL control on the front panel of the converter.

## Circuit description

The circuit diagram of the RFK7000 is fairly complex — see Fig. 1.

### Digital RGB input

The digital RGB signals are applied tot he converter via 9-pin socket $BU_4$. This input is intended mainly for IBM PCs and compatibles equipped with colour graphics adapter (CGA). A CGA card supplies the 3 RGB signals plus an intensity signal that allows any basic colour to be switched to half intensity. This results in a maximum of 16 different colours. The pinning of the 9-way connector is as follows:

Pin 1: ground
Pin 2: not connected
Pin 3: red
Pin 4: green
Pin 5: blue
Pin 6: intensity
Pin 7: not connected
Pin 8: horizontal sync
Pin 9: vertical sync

The RGB and intensity signals are applied to XOR gate inputs ($IC_4$). Jumpers $Br_1$ and $Br_2$ enable the RGB and/or intensity signal to be inverted, so that the entire video signal can be inverted if desired.

The intensity signal is coupled into a matrix network via a CMOS switch. The second brightness level can be adjusted with preset $R_{23}$.

The 3 RGB signals are taken to the analogue inputs (pin 3, 4 and 5) of PAL encoder $IC_7$ (a Type MC1377) via a resistor network composed of $R_{16}$–$R_{21}$ and $R_{36}$–$R_{38}$. At the chip inputs, the RGB signals have an amplitude of about 1 $V_{pp}$ at maximum intensity.

Each synchronisation signal is first fed to a transistor buffer stage, $T_1$-$T_2$, and from there to a XOR gate in $IC_6$. The polarity of the synchronisation signals can be set to requirement with the aid of jumpers $Br_3$ and $Br_4$. XOR gate $IC_{6b}$ supplies the composite sync signal at digital level. This negative-going signal is fed to pin 2 of $IC_7$ via voltage divider $R_{39}$-$R_{40}$.

### PAL encoder

The Type MC1377 PAL encoder from Motorola forms the nucleus of the circuit, because it performs the bulk of the signal conversion functions. The colour subcarrier frequency is adjustable with trimmer $C_{25}$, while the position of the colour burst on the rear porch of the CVBS signal is adjusted with $R_{34}$.

### Analogue RGB input

The circuit takes analogue RGB signals from SCART socket $Bu_2$. This is intended for computers such as the Atari ST or Commodore Amiga, having an analogue or quasi-analogue RGB output. Since the RGB output level supplied by these computers is usually 1.5 $V_{pp}$ to 3 $V_{pp}$, potential dividers $R_8$-$R_9$-$R_{10}$ and $R_{36}$-$R_{37}$-$R_{38}$ are required to ensure that the converter inputs are driven with a maximum level of 1 $V_{pp}$.

The RFK7000 allows separate as well as composite sync signals to be applied to the SCART input. Separate horizontal syncs at pins 10 and 14 are fed to $T_1$ and $T_2$ via 4.7 kΩ resistors. The function of the transistors is similar to those used for the digital sync signals, as discussed above. A composite sync signal as supplied by, for instance, the Atari ST, is applied via pin 20 of the SCART input. This signal is peculiar because it lacks horizontal synchronisation pulses during the vertical blanking interval. The MC1377, however,

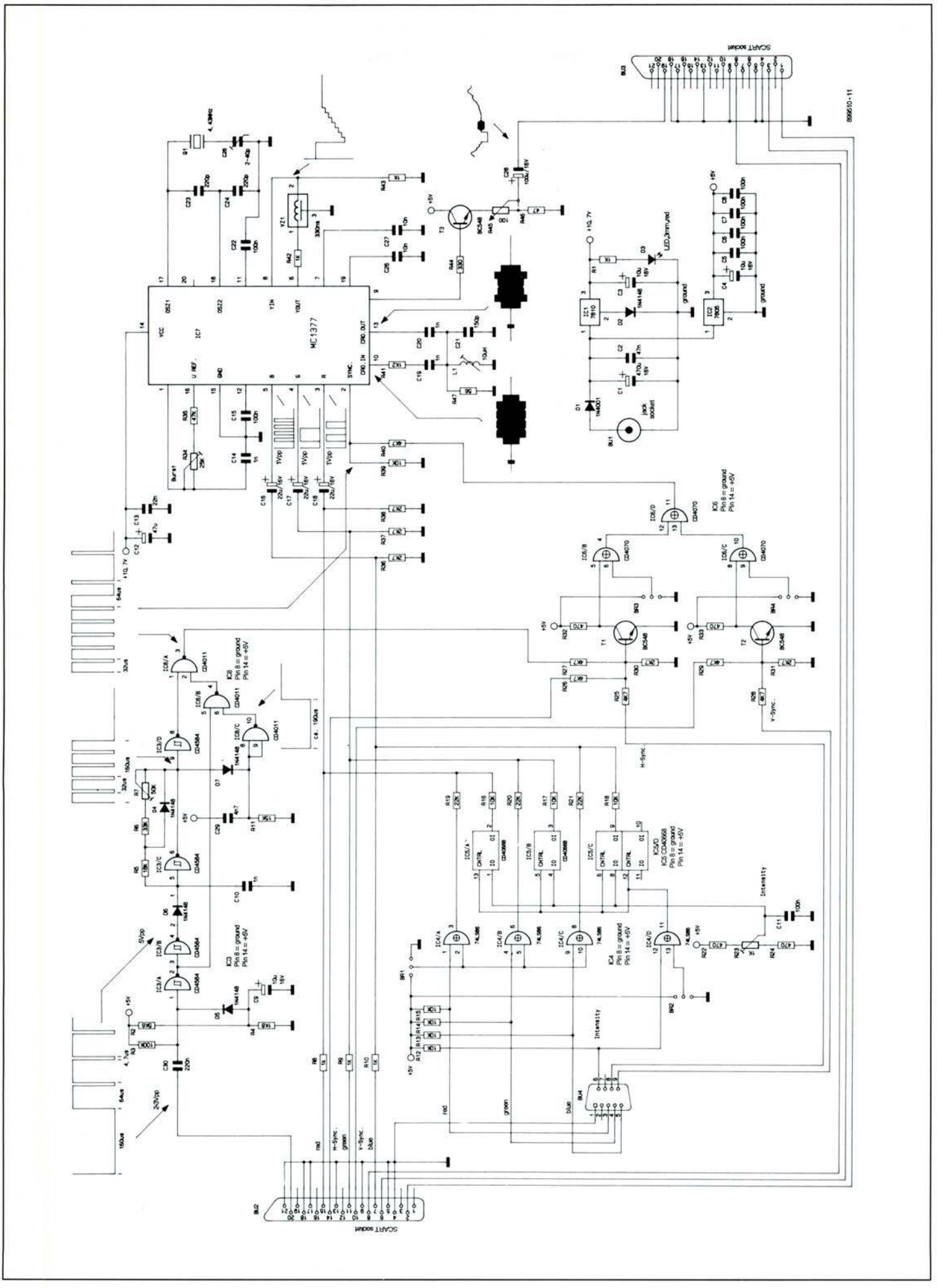



**Fig. 1. The heart of the RGB-to-CVBS converter is formed by a PAL encoder Type MC1377 from Motorola.**

**Content of the kit supplied by ELV France.**

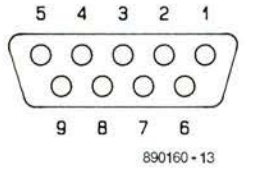
can not work properly without these pulses. The circuit around IC3 and IC8 converts the composite video signal into a standard composite sync signal that can be handled by the MC1377.

The composite synchronisation signal at pin 20 of the SCART input socket has an amplitude of 2 to 3 $V_{pp}$. A clamping circuit composed of C30-R2-R3-R4-D5-C9 is used to derive a direct voltage from the composite sync signal. This direct voltage is given a digital level to control gate IC3a. A subsequent gate, IC3b, inverts this control voltage.

Gate IC3c and surrounding components C10-R5-R6-R7-D4 form an oscillator that is disabled outside the vertical blanking interval by means of D6. This means that the oscillator supplies horizontal synchronisation pulses during the raster blanking interval only. The number of pulses and with it their spacing (32 µs) is adjusted with preset R7. Gate IC3d normally supplies a steady logic high level, but positive-going horizontal sync pulses during the vertical blanking interval.

The length of the raster blanking interval is determined by components D7-C29-R11 and inverter IC8c, whose output level changes from low to high at the end of the vertical synchronisation. This event enables the regenerated horizontal synchronisation pulses from pin 2 of IC3a to be added via IC8b, so that the output of the sync generator, pin 8 of IC8, supplies a normal composite synchronisation signal.

If the input signals for the converter are obtained via SCART socket BU2, the jumpers on Br1 and Br2 must be set in a

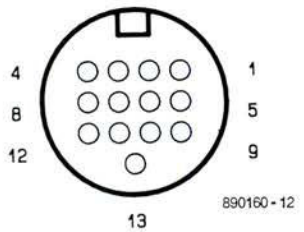



**9-way sub-D video connector**

front view

| Pin | Signal |
|---|---|
| 1 | ground |
| 2 | ground |
| 3 | red |
| 4 | green |
| 5 | blue |
| 6 | intensity |
| 7 | n.c. |
| 8 | h-sync |
| 9 | v-sync |

**Fig. 2. IBM PC CGA socket pinning.**




**Atari ST 13-way monitor connector**

front view

| Pin | Signal |
|---|---|
| 1 | audio output |
| 2 | composite sync |
| 3 | port IO87; YM-2149 sound generator |
| 4 | monochrome sense |
| 5 | audio input |
| 6 | green |
| 7 | red |
| 8 | +12 V via 1k2 |
| 9 | horizontal sync |
| 10 | blue |
| 11 | monochrome video |
| 12 | vertical sync |
| 13 | ground |

**Fig. 3. Atari ST monitor socket pinning.**

**Parts list**

**Resistors:**
R46 = 47Ω
R44 = 330Ω
R22;R24;R32;R33 = 470Ω
R1;R8;R9;R10;R42;R43 = 1k0
R41 = 1k2
R4 = 1k8
R30;R31;R36;R37;R38 = 2k7
R25 – R29 = 4k7
R2 = 5k6
R12 – R21 = 10k
R11 = 15k
R5 = 18k
R6 = 33k
R35 = 47k
R3 = 100k
R45 = 100Ω potentiometer with 6 mm spindle
R23 = 1k0 preset H
R34 = 25k preset H
R7 = 50k preset H

*Note:* R39, R40 and R47 are not fitted.
R19, R20 and R21 changed w.r.t. circuit diagram.

**Capacitors:**
C21 = 150p
C23;C24 = 220p
C10;C14;C19;C20 = 1n0
C29 = 4n7
C26;C27 = 10n
C13 = 22n
C2 = 47n
C5 – C8;C11;C15;C22 = 100n
C30 = 220n
C3;C4;C9 = 10µ; 16 V
C16;C17;C18 = 22µ; 16 V
C12 = 47µ; 16 V
C28 = 100µ; 16 V
C1 = 470µ; 16 V
C25 = 40p trimmer

**Semiconductors:**
IC7 = MC1377
IC8 = CD4011
IC5 = CD4066
IC6 = CD4070
IC3 = CD4584
IC4 = 74LS86
IC2 = 7805
IC1 = 7810
D1 = 1N4001
D2;D4 – D7 = 1N4148
D3 = LED; red; dia. 3 mm
T1;T2;T3 = BC548

**Miscellaneous:**
Q1 = quartz crystal 4.433 MHz.
Vz1 = 330ns delay line.
L1 = 10µH, adjustable.
Br1 – Br4 = 3-way pin header.
BU2;BU3 = SCART socket for PCB mounting.
BU4 = 9-way angled sub-D socket for PCB mounting.
BU1 = 3.5 mm jack socket for PCB mounting.
4 off jumpers.
6 off screw M3×8 mm.
6 off nut M3.
Enclosure.
PCB Type ELV892525.

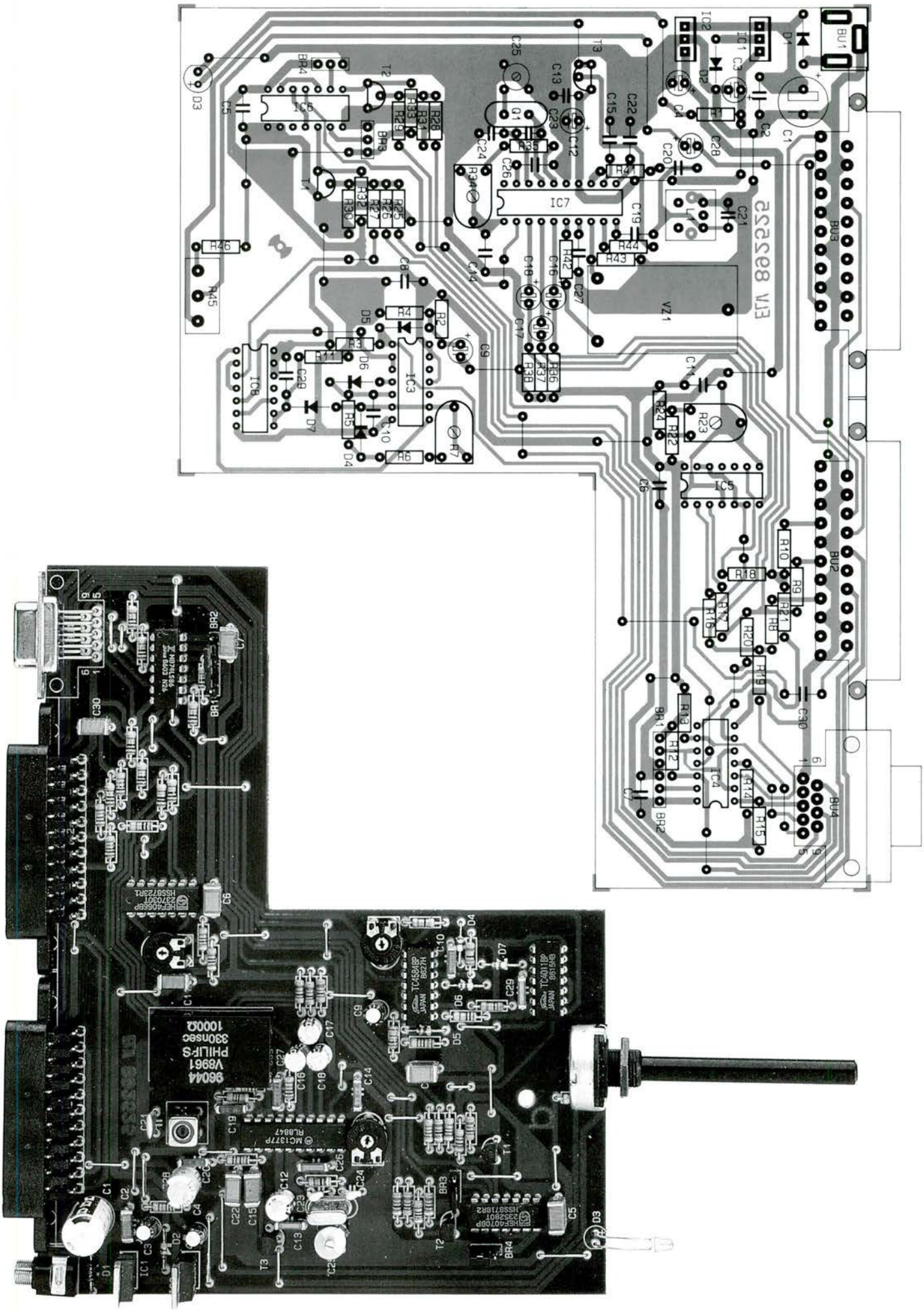


Fig. 4. Component mounting plan and top view of the printed-circuit board for the RGB-to-CVBS converter.

manner that ensures low levels at the outputs of XOR combination $IC_4$ ($Br_1$ and $Br_2$ at +12 V).

**CGA and 50/60 Hz**

The colour graphics adapter (CGA) in IBM PCs and compatibles supplies a vertical scanning frequency of 60 Hz. Most modern TV sets are capable of detecting this and switch automatically from 50 Hz to 60 Hz. Older types, however, may require the vertical synchronisation to be corrected if the picture rolls. In most cases, this adjustment is fairly simple to make by means of the vertical sync control at the rear of the set.

In case the picture is not correctly centred, use MS-DOS command

MODE CO80,R

to shift the entire picture one character to the right.

**Output circuit and power supply**

The composite output signal is supplied by buffer $T_3$, level control $R_{45}$ and electrolytic capacitor $C_{28}$.

The RFK7000 has two on-board voltage regulators, so that is conveniently powered from a standard mains adapter with 12 V d.c. output at about 300 mA. The unregulated input voltage is applied via 3.5 mm jack socket $BU_1$, and fed to buffer capacitor $C_1$ via $D_1$, which affords reverse polarity protection. Capacitor $C_2$ serves to suppress noise. Regulator $IC_1$ has a diode, $D_2$, connected to its ground terminal to raise the output voltage from 10.0 to about 10.7 V. This provides the supply voltage for the PAL encoder MC1377, which requires a minimum of 10.5 V for correct operation. Capacitor $C_3$ serves to eliminate any risk of oscillation. LED $D_3$ is powered via $R_1$ and indicates that the RFK7000 is switched on. Finally, the 5 V supply for the digital circuits is formed by regulator $IC_2$ in combination with decoupling capacitors $C_4$ to $C_8$.

## Construction

The RFK7000 is relatively simple to build because all parts are accommodated on the single printed-circuit board supplied with the kit. Construction is expected to take about 3 hours.

Start by inserting the lowest profile parts, the 29 wire links (do not solder them as yet). Next, bend all resistor terminals to obtain the right pitch. Insert the resistors in accordance with the Parts List and the component overlay on the PCB. Push the terminals apart after inserting the resistors to ensure that they do not drop from the board as it is turned and pushed firmly on a flat surface. Solder all wire terminals, and cut them off as close as possible to the solder joint.

Next, turn the board and fit the 7 diodes, 8 ICs, capacitors, etc. in the normal manner. Lastly, mount the 4 connectors and the video level potentiometer on to the board. Check your work by inspecting all solder joints.

Remove the nut from the 3.5 mm jack socket, and fit the rear panel of the enclosure on to the rear side of the PCB. The two SCART sockets and the 9-way sub-D socket are each secured with two M3×10 mm screws inserted through the socket flanges from the outside of the rear panel. Each screw is secured with two M3 nuts. Mount and tighten the nut on to the jack socket.

The front panel supplied with the kit is also quite simple to mount. Remove the nut from the level control potentiometer, mount the front panel, and secure the nut again at the outside. The potentiometer spindle is cut to about 10 mm. Next, fit the collet knob and secure it on to the spindle.

Insert the PCB with the front and rear panel attached into the guides in the bottom half of the enclosure.

## Jumper settings

Most CGAs in IBM PCs and compatibles supply a positive h-sync and v-sync signals. Some cards, however, supply a negative v-sync signal.

The horizontal sync signal is fed to the base of $T_1$ via pin 8 of socket $BU_4$ and $R_{25}$, and the vertical sync signal to the base of $T_2$ via pin 9 of $BU_4$ and $R_{28}$. Assuming that positive sync signals are applied, either the horizontal or the vertical sync signal must be inverted to ensure a negative-going composite sync signal at pin 11, the output of $IC_{6d}$. This may be achieved in two ways:

1. Pin 6 of $IC_{6b}$ is tied to +5 V via $Br_3$, and pin 9 of $IC_{6c}$ to ground via $Br_4$;
2. Pin 6 of $IC_{6b}$ is tied to ground via $Br_3$, and pin 9 of $IC_{6c}$ to +5 V via $Br_4$.

Since most CGA cards supply positive-going RGB signals, $Br_1$ is connected to ground to ensure that the signals are not inverted by gates $IC_{4a}$ through $IC_{4c}$. The same applies to the intensity signal: pin 13 of $IC_{4d}$ is normally connected to ground via $Br_2$. The value of $R_{23}$ determines the effect of the intensity bit on the colours, and may be adapted to individual requirements.

The jumpers on the board are fitted to allow the RFK7000 to accept sync polarities from CGA cards other than the standard types around. In case of doubt, consult the manual supplied with your CGA card.

## Alignment

The alignment of the RGB-to-CVBS converter concentrates mainly on PAL encoder $IC_7$. Alignment is straightforward, and can be carried out without an oscilloscope.

Apply a digital RGB signal to $BU_4$ (if necessary, refer to the pinning shown in Fig. 2), and connect a monitor with CVBS input to $BU_3$. Adjust $C_{25}$ and $R_{34}$ alternately until the colour appears on the monitor.

Alignment with the aid of an oscilloscope is even simpler because the instrument allows $R_{34}$ to be adjusted beforehand. Connect the scope to the output of the RFK7000, pin 19 of $BU_3$. Adjust $R_{34}$ until the colour burst starts at 0.5 µs after the horizontal sync pulse.

Next, adjust the cross-colour filter, $L_1$-$C_{21}$. Use an insulated trimming tool to adjust the core of $L_1$. Watch the picture on the monitor, and minimize the moving cross-colour patterns that occur typically at colour boundaries. This adjustment is also possible with the aid of an oscilloscope: peak the chrominance signal measured at pin 10 of the PAL encoder chip. This completes the adjustment of the RFK7000 for use with CGA-compatible PCs.

No further alignment is required if the separate sync signals are applied to the SCART input socket. If, however, composite sync is applied to pin 20, preset $R_7$ has to be adjusted.

Although the Atari ST supplies separate sync signals to the monitor socket (pinning: see Fig. 3), composite sync is used on the SCART cable provided with some STs.

Preset $R_7$ is used to set the pulse spacing of the horizontal sync signal generated during the vertical blanking interval. The pulse spacing may be measured at pin 8 of $IC_{3d}$, and should be about 32 µs. The actual value is fairly uncritical — the important thing is that the MC1377 receives an even number of horizontal sync pulses during the raster blanking interval. This is required for correct synchronisation of the internal PAL bistable. Constructors not in possession of an oscilloscope simply adjust $R_7$ until the colour shows up on the screen. Some re-adjustment of R34, $R_7$ and C25 may be required for optimum results, because these adjustments have a fairly large range and some interaction. In most cases, however, the alignment of the RFK7000 is straightforward by optimising the colour fidelity with the aid of the monitor.

Finally, it should be noted that the graphics card or computer used to drive the converter must be programmed to supply 50 Hz vertical synchronisation pulses if pictures are to be recorded on a VCR. This is not required for most monitors and TV sets, whose vertical scanning rate is adjusted either automatically or manually to synchronize at 60 Hz. The RFK7000 is not suitable for NTSC systems.

A complete kit of parts for the RGB-to-CVBS converter, which is designed in West-Germany, is available from the designers' exclusive worldwide distributors (regrettably not in the USA and Canada):

**ELV France**
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Telephone: +33 82827213
Fax: +33 82838180

Also see ELV France's advertisement elsewhere in this issue.