



## TPS22968-Q1 5.5-V, 4-A, 27-mΩ On-Resistance Load Switch

### 1 Features

- Integrated Dual Channel Load Switch
- Qualified for Automotive Applications:
  - Device Temperature Grade 1 (Operating Ambient Temperature:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ )
- Input Voltage Range: 0.8 to 5.5 V
- VBIAS Voltage Range: 2.5 to 5.5 V
- On-Resistance
  - $R_{\text{ON}} = 29\text{ m}\Omega$  at  $V_{\text{IN}} = 5\text{ V}$  ( $V_{\text{BIAS}} = 5\text{ V}$ )
  - $R_{\text{ON}} = 27\text{ m}\Omega$  at  $V_{\text{IN}} = 3.3\text{ V}$  ( $V_{\text{BIAS}} = 5\text{ V}$ )
  - $R_{\text{ON}} = 26\text{ m}\Omega$  at  $V_{\text{IN}} = 1.8\text{ V}$  ( $V_{\text{BIAS}} = 5\text{ V}$ )
- 4-A Maximum Continuous Switch Current per Channel
- Low Quiescent Current
  - $58\text{ }\mu\text{A}$  at  $V_{\text{BIAS}} = 5\text{ V}$  (Both Channels)
- Low Control Input Threshold Enables Use of 1.2-/1.8-/2.5-/3.3-V Logic
- Configurable Rise Time With CT Pin<sup>(1)</sup>
- Quick Output Discharge (QOD)<sup>(2)</sup>
- 10-Pin WSON Package With Wettable Flanks
- ESD Performance Tested per JEDEC STD
  - $\pm 2\text{-kV}$  HBM and  $\pm 1\text{-kV}$  CDM
- Latch-Up Performance meets 100 mA per JESD 78, Class II
- GPIO Enable – Active High

(1) See [Adjustable Rise Time](#) for CT value versus rise time

(2) This feature discharges output of the switch to GND through a 270-Ω resistor, preventing the output from floating.

### 2 Applications

- Automotive Electronics
- Infotainment
- Cluster
- ADAS

### 3 Description

The TPS22968-Q1 is a small, dual-channel load switch with configurable rise time. The device contains two N-channel MOSFETs that can operate over an input voltage range of 0.8 to 5.5 V and can support a maximum continuous current of 4 A per channel. Each switch is independently controlled by an on/off input (ON1 and ON2), which is capable of interfacing directly with low-voltage control signals. The TPS22968-Q1 includes a 270-Ω on-chip resistor for quick output discharge when the switch is turned off.

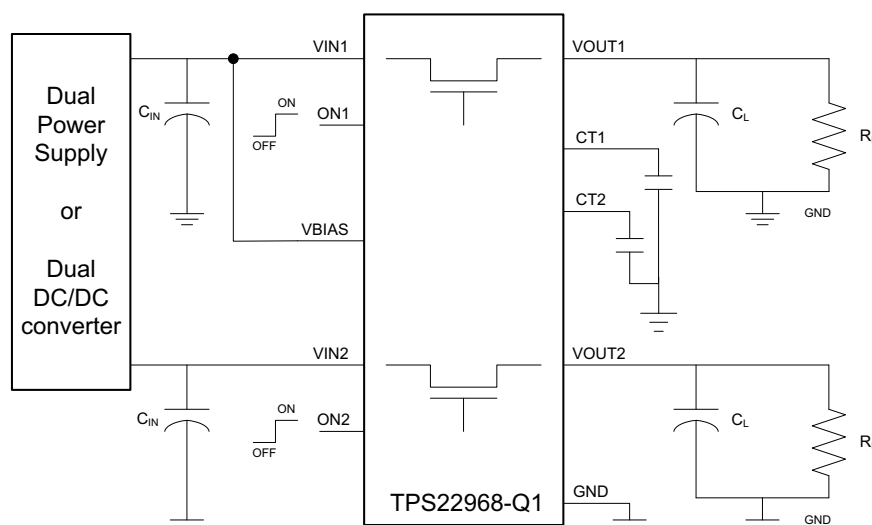
The TPS22968-Q1 is available in a small, space-saving package (DMG) with wettable flanks and an integrated thermal pad. The wettable flanks allow for visual solder inspection. The device is characterized for operation over the free-air temperature range of  $-40$  to  $125^{\circ}\text{C}$ .

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22968-Q1	WSON (10)	2.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Typical Application Schematic



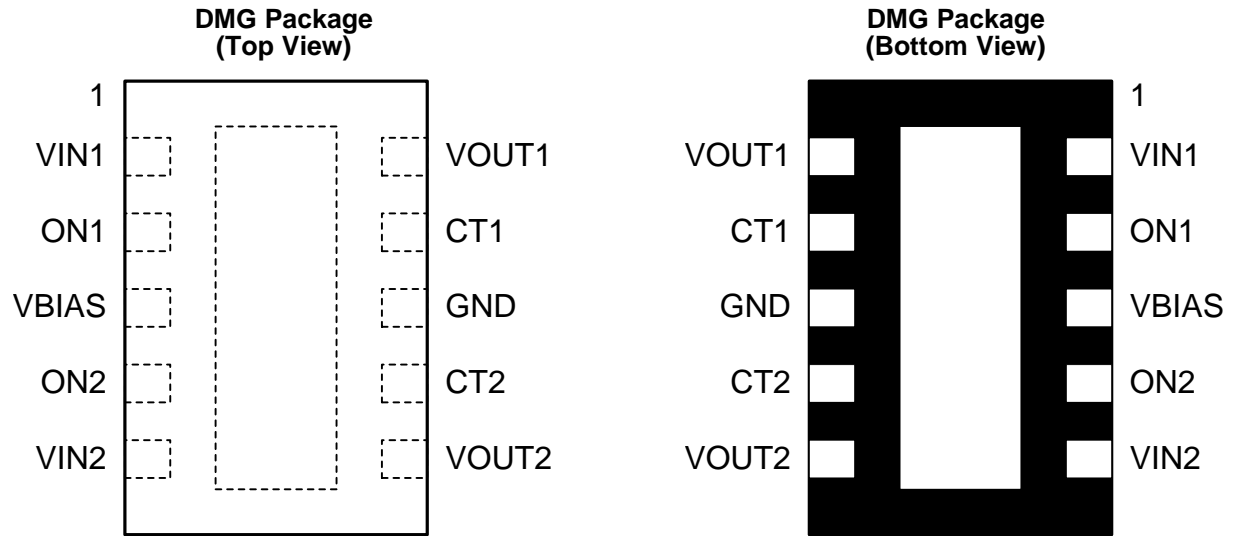
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## 4 Revision History

Changes from Original (November 2014) to Revision A	Page
• Changed device status to production data .....	1

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN1	1	I	Switch 1 input. Bypass this input with a ceramic capacitor to GND.
ON1	2	I	Active-high switch 1 control input. Do not leave floating.
VBIAS	3	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 to 5.5 V. See <a href="#">VIN and VBIAS Voltage Range</a> .
ON2	4	I	Active-high switch 2 control input. Do not leave floating.
VIN2	5	I	Switch 2 input. Bypass this input with a ceramic capacitor to GND.
VOUT2	6	O	Switch 2 output
CT2	7	O	Switch 2 slew rate control. Can be left floating.
GND	8	—	Ground
CT1	9	O	Switch 1 slew rate control. Can be left floating.
VOUT1	10	O	Switch 1 output
Thermal Pad	—	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See <a href="#">Layout Guidelines</a> .

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup>

		MIN	MAX	UNIT
V <sub>IN1,2</sub>	Input voltage	−0.3	6	V
V <sub>BIAS</sub>	Bias voltage	−0.3	6	V
V <sub>OUT1,2</sub>	Output voltage	−0.3	6	V
V <sub>ON1,2</sub>	ON voltage	−0.3	6	V
I <sub>MAX</sub>	Maximum continuous switch current per channel, T <sub>A</sub> = 50 °C		4	A
I <sub>PLS</sub>	Maximum pulsed switch current, pulse <300 μs, 2% duty cycle		6	A
T <sub>J</sub>	Maximum junction temperature		150	°C
T <sub>LEAD</sub>	Maximum lead temperature (10-s soldering time)		300	°C
T <sub>stg</sub>	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000
		Charged-Device Model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V <sub>IN1,2</sub>	Input voltage range		0.8	V <sub>BIAS</sub>	V
V <sub>BIAS</sub>	Bias voltage range		2.5	5.5	V
V <sub>ON1,2</sub>	ON voltage range		0	5.5	V
V <sub>OUT1,2</sub>	Output voltage range			V <sub>IN</sub>	V
V <sub>IH, ON1,2</sub>	High-level input voltage, ON1,2	V <sub>BIAS</sub> = 2.5 to 5.5 V	1.2	5.5	V
V <sub>IL, ON1,2</sub>	Low-level input voltage, ON1,2	V <sub>BIAS</sub> = 2.5 to 5.5 V	0	0.5	V
C <sub>IN1,2</sub>	Input capacitor		1 <sup>(1)</sup>		μF
T <sub>A</sub>	Operating free-air temperature <sup>(2)</sup>		−40	125	°C

- (1) Refer to [Application Information](#).
- (2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T<sub>A(max)</sub>] is dependent on the maximum operating junction temperature [T<sub>J(max)</sub>], the maximum power dissipation of the device in the application [P<sub>D(max)</sub>], and the junction-to-ambient thermal resistance of the part/package in the application (R<sub>θJA</sub>), as given by the following equation: T<sub>A(max)</sub> = T<sub>J(max)</sub> − (R<sub>θJA</sub> × P<sub>D(max)</sub>).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup> (2)		TPS22968-Q1	UNIT
		DMG (10 PINS)	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	55.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	71.0	
R <sub>θJB</sub>	Junction-to-board thermal resistance	21.7	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.9	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	21.7	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	7.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).

## 6.5 Electrical Characteristics (V<sub>BIAS</sub> = 5 V)

V<sub>BIAS</sub> = 5 V. Typical values are for T<sub>A</sub> = 25°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
<b>POWER SUPPLIES AND CURRENTS</b>							
I <sub>Q</sub> , V <sub>BIAS</sub>	V <sub>BIAS</sub> quiescent current (both channels)	I <sub>OUT1</sub> = I <sub>OUT2</sub> = 0 A, V <sub>IN1,2</sub> = V <sub>ON1,2</sub> = V <sub>BIAS</sub> = 5 V	–40°C to 85°C	58	70		μA
			–40°C to 125°C		70		
	V <sub>BIAS</sub> quiescent current (single channel)	I <sub>OUT1</sub> = I <sub>OUT2</sub> = 0 A, V <sub>ON2</sub> = 0 V, V <sub>IN1,2</sub> = V <sub>ON1</sub> = V <sub>BIAS</sub> = 5.0 V	–40°C to 85°C	58	68		μA
			–40°C to 125°C		68		
I <sub>SD</sub> , V <sub>BIAS</sub>	V <sub>BIAS</sub> shutdown current	V <sub>ON1,2</sub> = 0 V, V <sub>OUT1,2</sub> = 0 V	–40°C to 85°C	1	2		μA
			–40°C to 125°C		2		
I <sub>SD</sub> , V <sub>IN1,2</sub>	V <sub>IN1,2</sub> shutdown current (per channel)	V <sub>ON1,2</sub> = 0 V, V <sub>OUT1,2</sub> = 0 V	V <sub>IN1,2</sub> = 5 V	–40°C to 85°C	0.5	8	μA
				–40°C to 125°C		36	
			V <sub>IN1,2</sub> = 3.3 V	–40°C to 85°C	0.1	3	
				–40°C to 125°C		13	
			V <sub>IN1,2</sub> = 1.8 V	–40°C to 85°C	0.07	2	
				–40°C to 125°C		6	
			V <sub>IN1,2</sub> = 1.2 V	–40°C to 85°C	0.05	1	
				–40°C to 125°C		4	
			V <sub>IN1,2</sub> = 0.8 V	–40°C to 85°C	0.04	1	
				–40°C to 125°C		4	
I <sub>ON1,2</sub>	ON pin input leakage current	V <sub>ON</sub> = 5.5 V	–40°C to 125°C		0.1		μA
<b>RESISTANCE CHARACTERISTICS</b>							
R <sub>ON</sub>	ON-state resistance	I <sub>OUT</sub> = –200 mA, V <sub>BIAS</sub> = 5 V	V <sub>IN</sub> = 5 V	25°C	29	35	mΩ
				–40°C to 85°C		40	
				–40°C to 125°C		43	
			V <sub>IN</sub> = 3.3 V	25°C	27	32	mΩ
				–40°C to 85°C		36	
				–40°C to 125°C		40	
			V <sub>IN</sub> = 1.8 V	25°C	26	32	mΩ
				–40°C to 85°C		36	
				–40°C to 125°C		39	
			V <sub>IN</sub> = 1.2 V	25°C	26	32	mΩ
				–40°C to 85°C		36	
				–40°C to 125°C		39	
			V <sub>IN</sub> = 0.8 V	25°C	26	32	mΩ
				–40°C to 85°C		36	
				–40°C to 125°C		39	
R <sub>PD</sub>	Output pulldown resistance	V <sub>IN</sub> = 5 V, V <sub>ON</sub> = 0 V, I <sub>OUT</sub> = 5 mA	–40°C to 125°C		270	320	Ω

**TPS22968-Q1**

SLVSCP7A–NOVEMBER 2014–REVISED FEBRUARY 2015

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**6.6 Electrical Characteristics ( $V_{BIAS} = 3.3\text{ V}$ )**
 $V_{BIAS} = 3.3\text{ V}$ . Typical values are for  $T_A = 25^\circ\text{C}$ , unless otherwise noted

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>POWER SUPPLIES AND CURRENTS</b>							
$I_Q$ , $V_{BIAS}$	$V_{BIAS}$ quiescent current (both channels)	$I_{OUT1} = I_{OUT2} = 0\text{ A}$ , $V_{IN1,2} = V_{ON1,2} = V_{BIAS} = 3.3\text{ V}$	$-40^\circ\text{C}$ to $85^\circ\text{C}$		27	40	$\mu\text{A}$
			$-40^\circ\text{C}$ to $125^\circ\text{C}$			40	
	$V_{BIAS}$ quiescent current (single channel)	$I_{OUT1} = I_{OUT2} = 0\text{ A}$ , $V_{ON2} = 0\text{ V}$ , $V_{IN1,2} = V_{ON1} = V_{BIAS} = 3.3\text{ V}$	$-40^\circ\text{C}$ to $85^\circ\text{C}$		27	40	$\mu\text{A}$
			$-40^\circ\text{C}$ to $125^\circ\text{C}$			40	
$I_{SD}$ , $V_{BIAS}$	$V_{BIAS}$ shutdown current	$V_{ON1,2} = 0\text{ V}$ , $V_{OUT1,2} = 0\text{ V}$	$-40^\circ\text{C}$ to $85^\circ\text{C}$		0.5	1	$\mu\text{A}$
			$-40^\circ\text{C}$ to $125^\circ\text{C}$			1	
$I_{SD}$ , $V_{IN1,2}$	$V_{IN1,2}$ shutdown current (per channel)	$V_{ON1,2} = 0\text{ V}$ , $V_{OUT1,2} = 0\text{ V}$	$V_{IN1,2} = 3.3\text{ V}$	$-40^\circ\text{C}$ to $85^\circ\text{C}$	0.1	3	$\mu\text{A}$
				$-40^\circ\text{C}$ to $125^\circ\text{C}$		13	
			$V_{IN1,2} = 1.8\text{ V}$	$-40^\circ\text{C}$ to $85^\circ\text{C}$	0.07	2	
				$-40^\circ\text{C}$ to $125^\circ\text{C}$		6	
			$V_{IN1,2} = 1.2\text{ V}$	$-40^\circ\text{C}$ to $85^\circ\text{C}$	0.05	1	
				$-40^\circ\text{C}$ to $125^\circ\text{C}$		4	
			$V_{IN1,2} = 0.8\text{ V}$	$-40^\circ\text{C}$ to $85^\circ\text{C}$	0.04	1	
				$-40^\circ\text{C}$ to $125^\circ\text{C}$		4	
$I_{ON1,2}$	ON pin input leakage current	$V_{ON} = 5.5\text{ V}$	$-40^\circ\text{C}$ to $125^\circ\text{C}$			0.1	$\mu\text{A}$
<b>RESISTANCE CHARACTERISTICS</b>							
$R_{ON}$	ON-state resistance	$I_{OUT} = -200\text{ mA}$ , $V_{BIAS} = 3.3\text{ V}$	$V_{IN} = 3.3\text{ V}$	$25^\circ\text{C}$	32	38	$\text{m}\Omega$
				$-40^\circ\text{C}$ to $85^\circ\text{C}$		44	
				$-40^\circ\text{C}$ to $125^\circ\text{C}$		48	
			$V_{IN} = 1.8\text{ V}$	$25^\circ\text{C}$	28	33	$\text{m}\Omega$
				$-40^\circ\text{C}$ to $85^\circ\text{C}$		38	
				$-40^\circ\text{C}$ to $125^\circ\text{C}$		42	
			$V_{IN} = 1.2\text{ V}$	$25^\circ\text{C}$	27	33	$\text{m}\Omega$
				$-40^\circ\text{C}$ to $85^\circ\text{C}$		38	
				$-40^\circ\text{C}$ to $125^\circ\text{C}$		41	
			$V_{IN} = 0.8\text{ V}$	$25^\circ\text{C}$	27	32	$\text{m}\Omega$
				$-40^\circ\text{C}$ to $85^\circ\text{C}$		37	
				$-40^\circ\text{C}$ to $125^\circ\text{C}$		40	
$R_{PD}$	Output pulldown resistance	$V_{IN} = 3.3\text{ V}$ , $V_{ON} = 0\text{ V}$ , $I_{OUT} = 5\text{ mA}$	$-40^\circ\text{C}$ to $125^\circ\text{C}$		270	320	$\Omega$

## 6.7 Electrical Characteristics ( $V_{BIAS} = 2.5\text{ V}$ )

$V_{BIAS} = 2.5\text{ V}$ . Typical values are for  $T_A = 25^\circ\text{C}$ , unless otherwise noted

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>POWER SUPPLIES AND CURRENTS</b>							
$I_Q$ , $V_{BIAS}$	$V_{BIAS}$ quiescent current (both channels)	$I_{OUT1} = I_{OUT2} = 0$ , $V_{IN1,2} = V_{ON1,2} = V_{BIAS} = 2.5\text{ V}$	$-40^\circ\text{C}$ to $85^\circ\text{C}$	19	27		$\mu\text{A}$
			$-40^\circ\text{C}$ to $125^\circ\text{C}$			27	
	$V_{BIAS}$ quiescent current (single channel)	$I_{OUT1} = I_{OUT2} = 0$ , $V_{ON2} = 0\text{ V}$ , $V_{IN1,2} = V_{ON1} = V_{BIAS} = 2.5\text{ V}$	$-40^\circ\text{C}$ to $85^\circ\text{C}$	19	27		$\mu\text{A}$
			$-40^\circ\text{C}$ to $125^\circ\text{C}$			27	
$I_{SD}$ , $V_{BIAS}$	$V_{BIAS}$ shutdown current	$V_{ON1,2} = 0\text{ V}$ , $V_{OUT1,2} = 0\text{ V}$	$-40^\circ\text{C}$ to $85^\circ\text{C}$	0.4		1	$\mu\text{A}$
			$-40^\circ\text{C}$ to $125^\circ\text{C}$			1	
$I_{SD}$ , $V_{IN1,2}$	$V_{IN1,2}$ shutdown current (per channel)	$V_{ON1,2} = 0\text{ V}$ , $V_{OUT1,2} = 0\text{ V}$	$V_{IN1,2} = 2.5\text{ V}$	$-40^\circ\text{C}$ to $85^\circ\text{C}$	0.1	2	$\mu\text{A}$
			$V_{IN1,2} = 2.5\text{ V}$	$-40^\circ\text{C}$ to $125^\circ\text{C}$		9	
			$V_{IN1,2} = 1.8\text{ V}$	$-40^\circ\text{C}$ to $85^\circ\text{C}$	0.07	2	
			$V_{IN1,2} = 1.8\text{ V}$	$-40^\circ\text{C}$ to $125^\circ\text{C}$		6	
			$V_{IN1,2} = 1.2\text{ V}$	$-40^\circ\text{C}$ to $85^\circ\text{C}$	0.05	1	
			$V_{IN1,2} = 1.2\text{ V}$	$-40^\circ\text{C}$ to $125^\circ\text{C}$		4	
			$V_{IN1,2} = 0.8\text{ V}$	$-40^\circ\text{C}$ to $85^\circ\text{C}$	0.04	1	
			$V_{IN1,2} = 0.8\text{ V}$	$-40^\circ\text{C}$ to $125^\circ\text{C}$		4	
$I_{ON1,2}$	ON pin input leakage current	$V_{ON} = 5.5\text{ V}$	$-40^\circ\text{C}$ to $125^\circ\text{C}$			0.1	$\mu\text{A}$
<b>RESISTANCE CHARACTERISTICS</b>							
$R_{ON}$	ON-state resistance	$I_{OUT} = -200\text{ mA}$ , $V_{BIAS} = 2.5\text{ V}$	$V_{IN} = 2.5\text{ V}$	$25^\circ\text{C}$	39	45	$\text{m}\Omega$
				$-40^\circ\text{C}$ to $85^\circ\text{C}$		52	
				$-40^\circ\text{C}$ to $125^\circ\text{C}$		57	
			$V_{IN} = 1.8\text{ V}$	$25^\circ\text{C}$	34	39	$\text{m}\Omega$
				$-40^\circ\text{C}$ to $85^\circ\text{C}$		46	
				$-40^\circ\text{C}$ to $125^\circ\text{C}$		50	
			$V_{IN} = 1.2\text{ V}$	$25^\circ\text{C}$	31	37	$\text{m}\Omega$
				$-40^\circ\text{C}$ to $85^\circ\text{C}$		42	
				$-40^\circ\text{C}$ to $125^\circ\text{C}$		46	
			$V_{IN} = 0.8\text{ V}$	$25^\circ\text{C}$	30	35	$\text{m}\Omega$
				$-40^\circ\text{C}$ to $85^\circ\text{C}$		41	
				$-40^\circ\text{C}$ to $125^\circ\text{C}$		44	
$R_{PD}$	Output pulldown resistance	$V_{IN} = 2.5\text{ V}$ , $V_{ON} = 0\text{ V}$ , $I_{OUT} = 5\text{ mA}$	$-40^\circ\text{C}$ to $125^\circ\text{C}$		270	320	$\Omega$

## 6.8 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN = VON = VBIAS = 5 V, TA = 25 °C (unless otherwise noted)						
tON	Turn-on time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		1150		μs
tOFF	Turn-off time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		4		
tR	VOUT rise time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		1400		
tF	VOUT fall time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		2		
tD	ON delay time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		469		
VIN = 0.8 V, VON = VBIAS = 5 V, TA = 25 °C (unless otherwise noted)						
tON	Turn-on time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		514		μs
tOFF	Turn-off time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		31		
tR	VOUT rise time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		271		
tF	VOUT fall time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		2		
tD	ON delay time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		382		
VIN = 3.3 V, VON = 5 V, VBIAS = 3.3 V, TA = 25 °C (unless otherwise noted)						
tON	Turn-on time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		1455		μs
tOFF	Turn-off time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		5		
tR	VOUT rise time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		1592		
tF	VOUT fall time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		2		
tD	ON delay time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		681		
VIN = 0.8 V, VON = 5 V, VBIAS = 3.3 V, TA = 25 °C (unless otherwise noted)						
tON	Turn-on time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		805		μs
tOFF	Turn-off time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		31		
tR	VOUT rise time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		455		
tF	VOUT fall time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		2		
tD	ON delay time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		577		
VIN = 2.5 V, VON = 5 V, VBIAS = 2.5 V, TA = 25 °C (unless otherwise noted)						
tON	Turn-on time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		1800		μs
tOFF	Turn-off time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		6		
tR	VOUT rise time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		1830		
tF	VOUT fall time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		2		
tD	ON delay time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		909		
VIN = 0.8 V, VON = 5 V, VBIAS = 2.5 V, TA = 25 °C (unless otherwise noted)						
tON	Turn-on time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		1140		μs
tOFF	Turn-off time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		28		
tR	VOUT rise time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		664		
tF	VOUT fall time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		2		
tD	ON delay time	RL = 10 Ω, CL = 0.1 μF, CT = 1000 pF		798		



## 6.9 Typical DC Characteristics

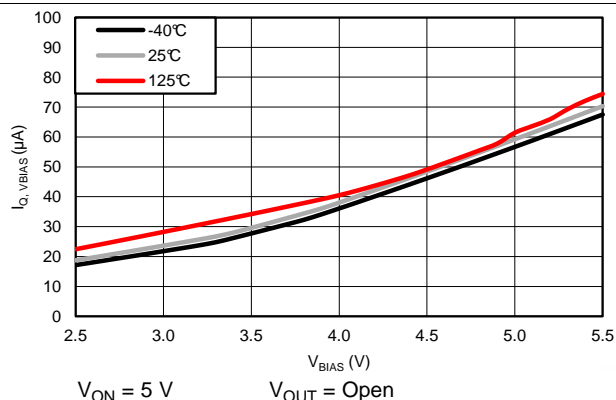


Figure 1.  $I_{Q, V_{BIAS}}$  vs  $V_{BIAS}$  (Single Channel)

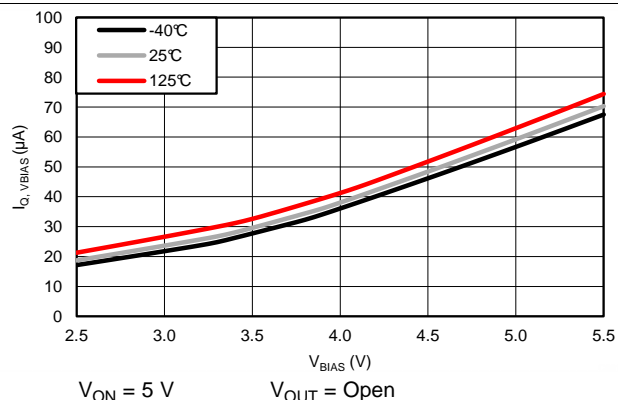


Figure 2.  $I_{Q, V_{BIAS}}$  vs  $V_{BIAS}$  (Dual Channel)

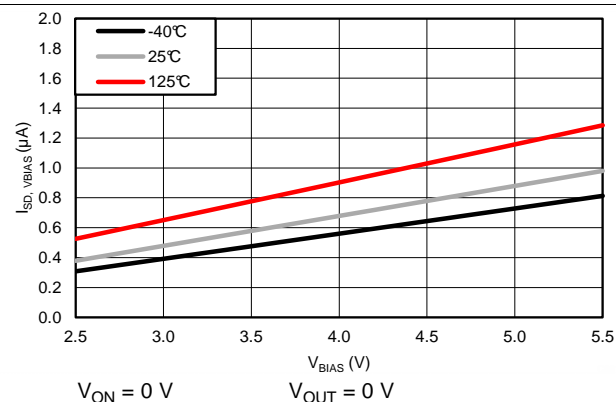


Figure 3.  $I_{SD, V_{BIAS}}$  vs  $V_{BIAS}$

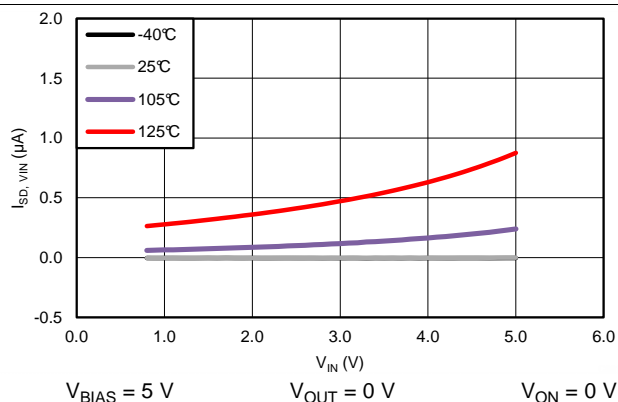


Figure 4.  $I_{SD, V_{IN}}$  vs  $V_{IN}$  (One Channel)

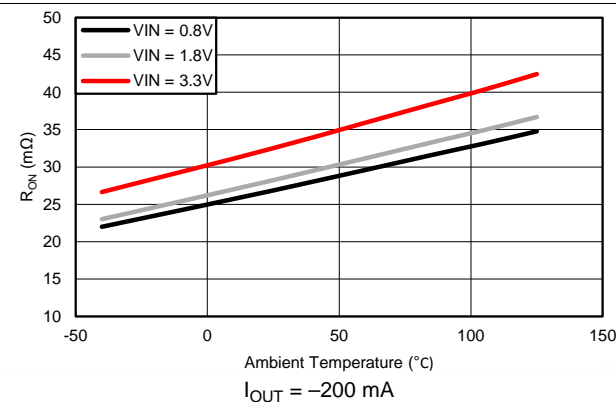


Figure 5.  $R_{ON}$  vs Ambient Temperature,  $V_{BIAS} = 3.3\text{ V}$

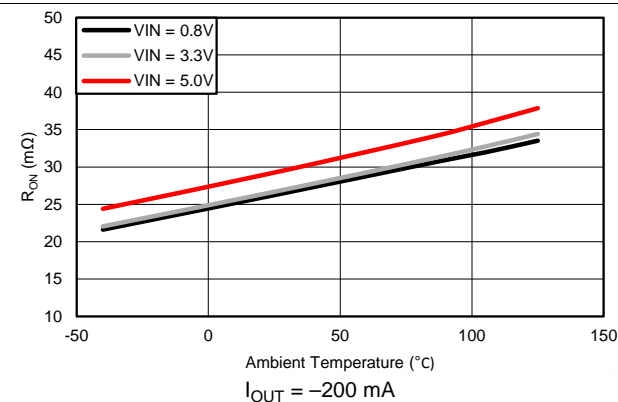


Figure 6.  $R_{ON}$  vs Ambient Temperature,  $V_{BIAS} = 5\text{ V}$

## Typical DC Characteristics (continued)

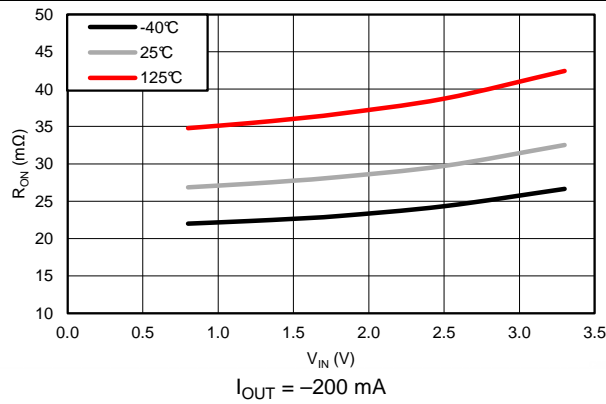


Figure 7.  $R_{ON}$  vs  $V_{IN}$ ,  $V_{BIAS} = 3.3$  V

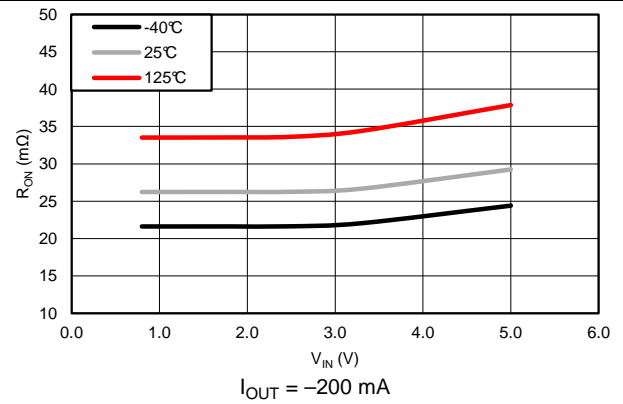


Figure 8.  $R_{ON}$  vs  $V_{IN}$ ,  $V_{BIAS} = 5$  V

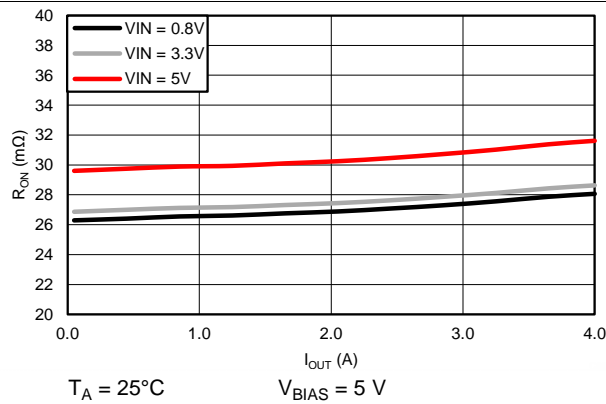


Figure 9.  $R_{ON}$  vs  $I_{OUT}$

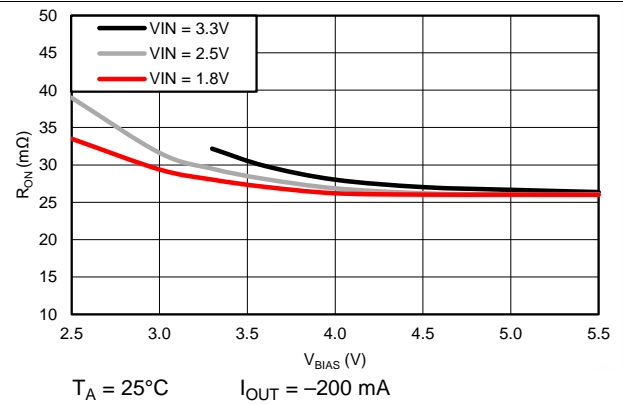


Figure 10.  $R_{ON}$  vs  $V_{BIAS}$

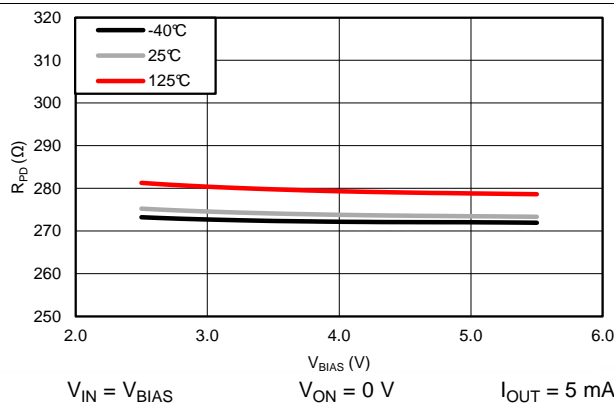


Figure 11.  $R_{PD}$  vs  $V_{BIAS}$

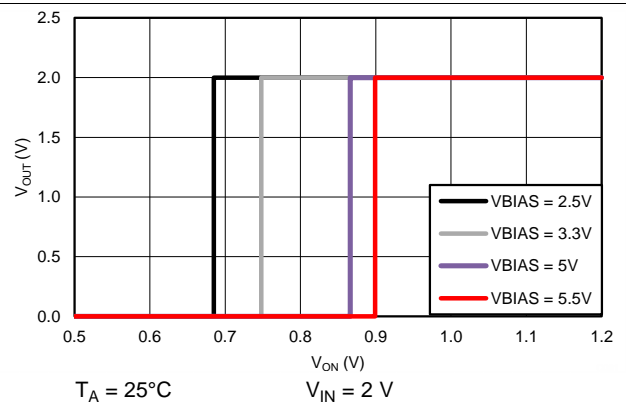


Figure 12.  $V_{OUT}$  vs  $V_{ON}$

## 6.10 Typical AC Characteristics

$C_{IN} = 1 \mu F$ ,  $C_L = 0.1 \mu F$ ,  $R_L = 10 \Omega$ ,  $C_T = 1 \text{ nF}$  (unless otherwise specified)

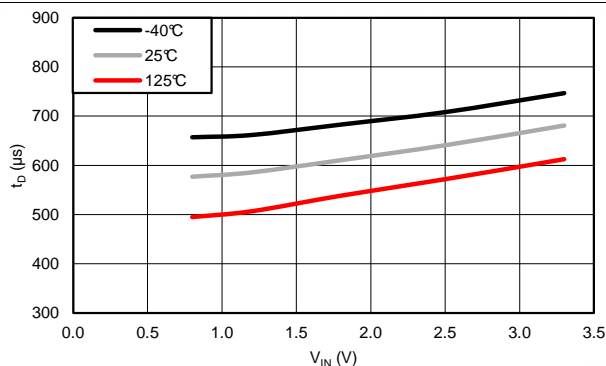


Figure 13.  $t_D$  vs  $V_{IN}$ ,  $V_{BIAS} = 3.3 \text{ V}$

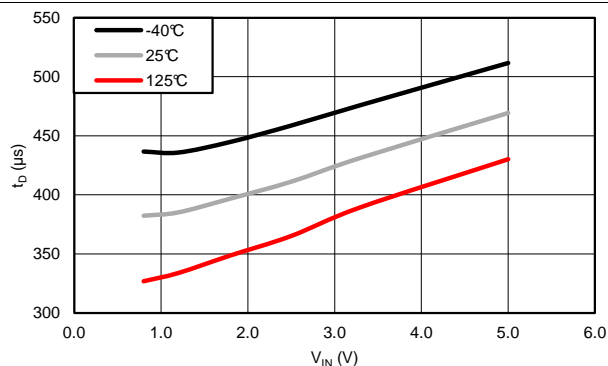


Figure 14.  $t_D$  vs  $V_{IN}$ ,  $V_{BIAS} = 5 \text{ V}$

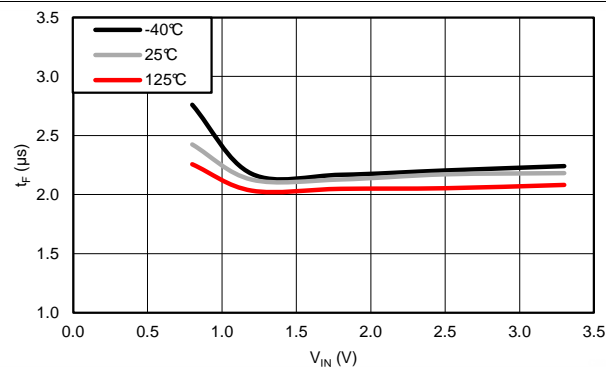


Figure 15.  $t_F$  vs  $V_{IN}$ ,  $V_{BIAS} = 3.3 \text{ V}$

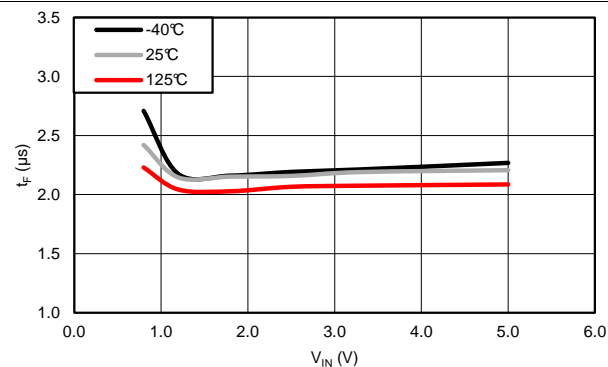


Figure 16.  $t_F$  vs  $V_{IN}$ ,  $V_{BIAS} = 5 \text{ V}$

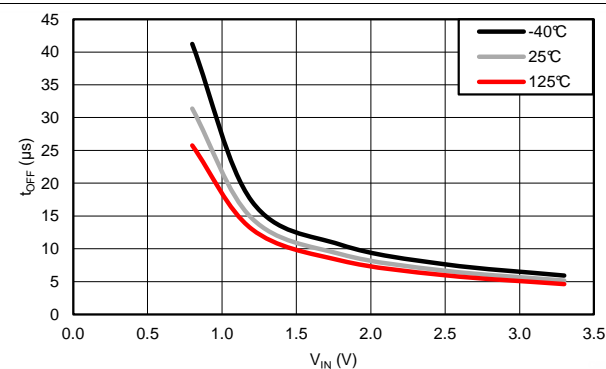


Figure 17.  $t_{OFF}$  vs  $V_{IN}$ ,  $V_{BIAS} = 3.3 \text{ V}$

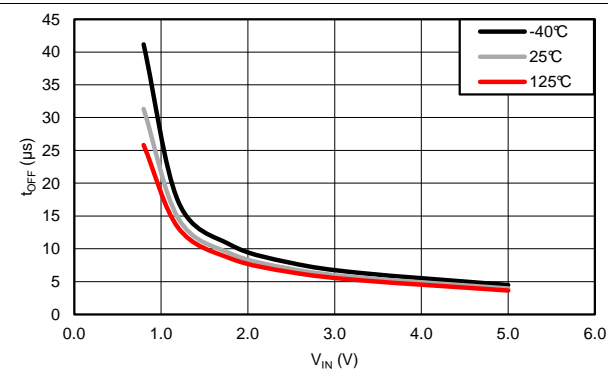
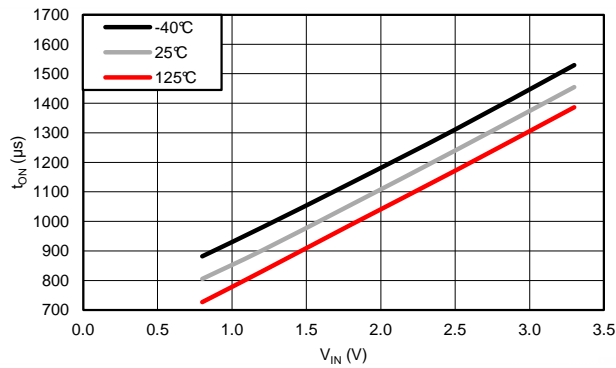
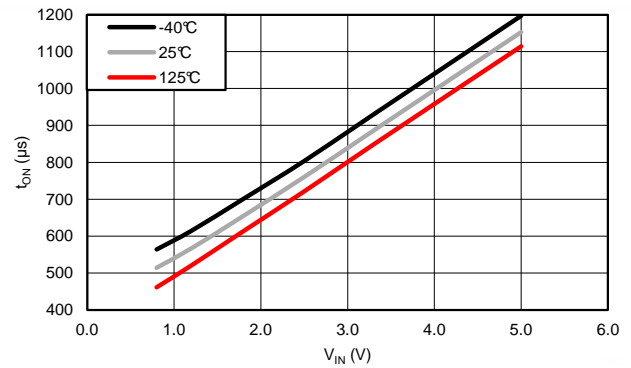
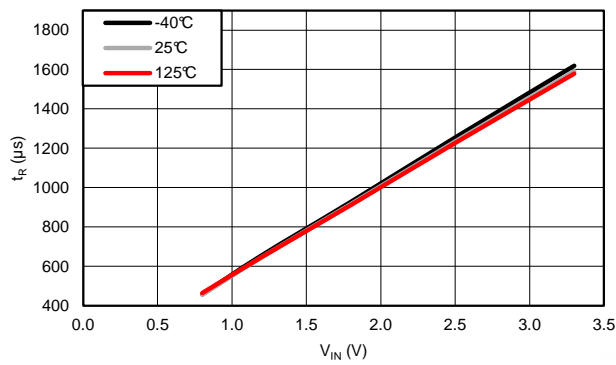
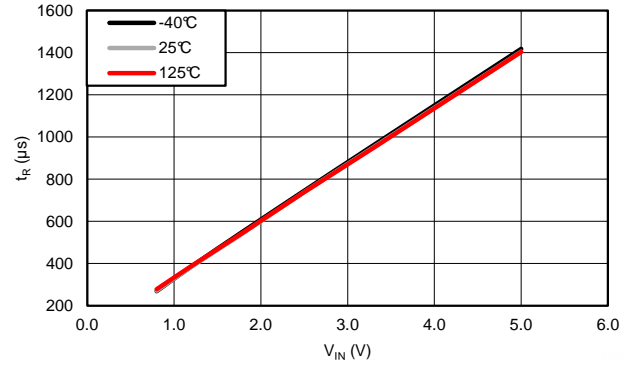
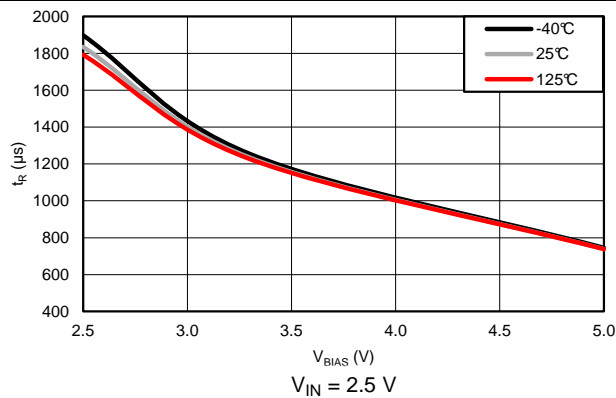
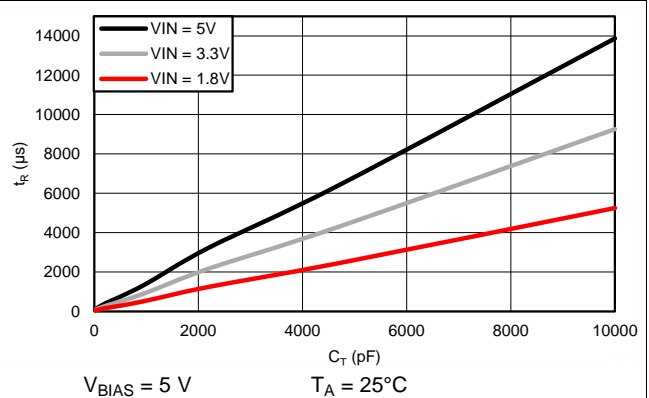


Figure 18.  $t_{OFF}$  vs  $V_{IN}$ ,  $V_{BIAS} = 5 \text{ V}$

## Typical AC Characteristics (continued)

 $C_{IN} = 1\ \mu\text{F}$ ,  $C_L = 0.1\ \mu\text{F}$ ,  $R_L = 10\ \Omega$ ,  $C_T = 1\ \text{nF}$  (unless otherwise specified)

**Figure 19.  $t_{ON}$  vs  $V_{IN}$ ,  $V_{BIAS} = 3.3\ \text{V}$** 

**Figure 20.  $t_{ON}$  vs  $V_{IN}$ ,  $V_{BIAS} = 5\ \text{V}$** 

**Figure 21.  $t_R$  vs  $V_{IN}$ ,  $V_{BIAS} = 3.3\ \text{V}$** 

**Figure 22.  $t_R$  vs  $V_{IN}$ ,  $V_{BIAS} = 5\ \text{V}$** 

**Figure 23.  $t_R$  vs  $V_{BIAS}$** 

**Figure 24.  $t_R$  vs  $C_T$**

## Typical AC Characteristics (continued)

$C_{IN} = 1\ \mu\text{F}$ ,  $C_L = 0.1\ \mu\text{F}$ ,  $R_L = 10\ \Omega$ ,  $C_T = 1\ \text{nF}$  (unless otherwise specified)

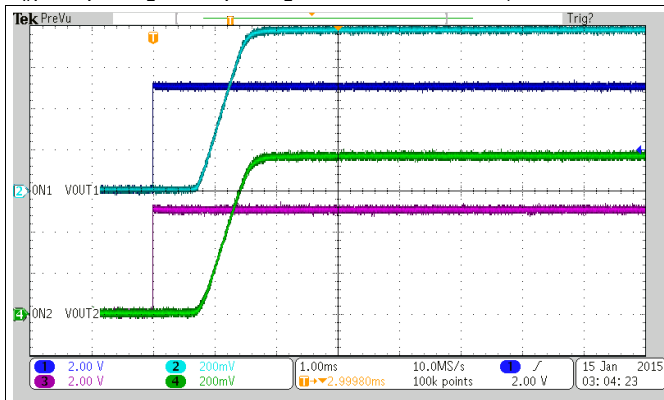


Figure 25. Turn-On Response Time  
( $V_{IN} = 0.8\ \text{V}$ ,  $V_{BIAS} = 2.5\ \text{V}$ )

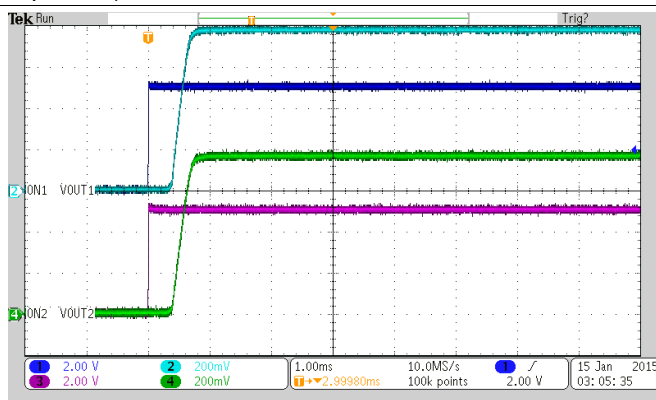


Figure 26. Turn-On Response Time  
( $V_{IN} = 0.8\ \text{V}$ ,  $V_{BIAS} = 5\ \text{V}$ )

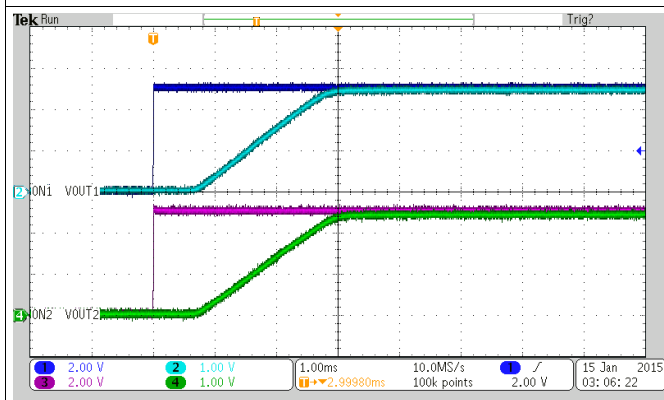


Figure 27. Turn-On Response Time  
( $V_{IN} = 2.5\ \text{V}$ ,  $V_{BIAS} = 2.5\ \text{V}$ )

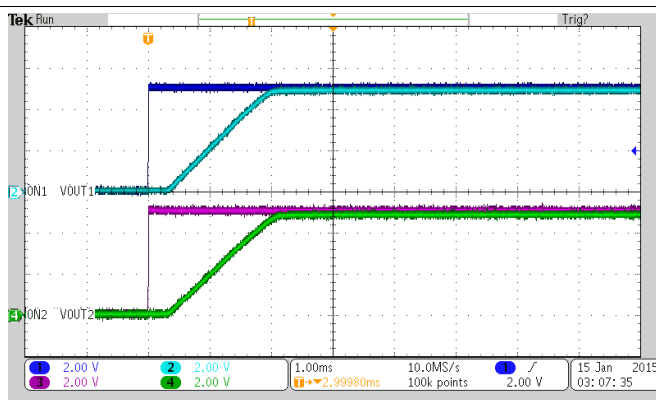


Figure 28. Turn-On Response Time  
( $V_{IN} = 5\ \text{V}$ ,  $V_{BIAS} = 5\ \text{V}$ )

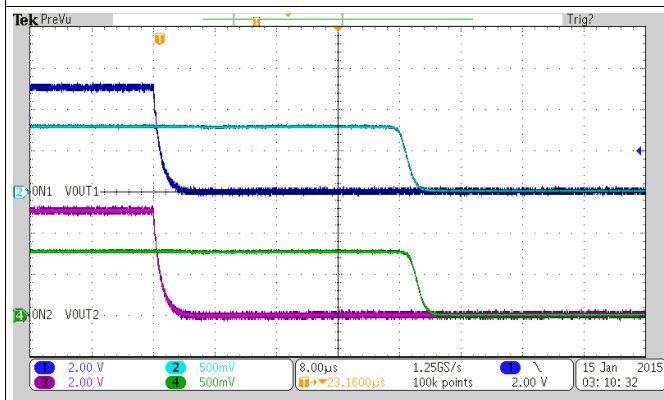


Figure 29. Turn-Off Response Time  
( $V_{IN} = 0.8\ \text{V}$ ,  $V_{BIAS} = 2.5\ \text{V}$ )

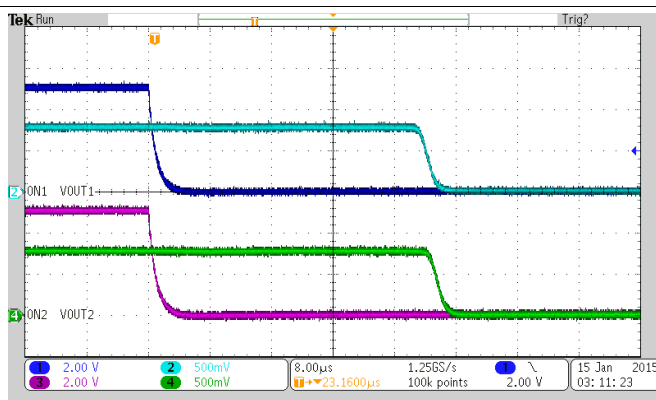
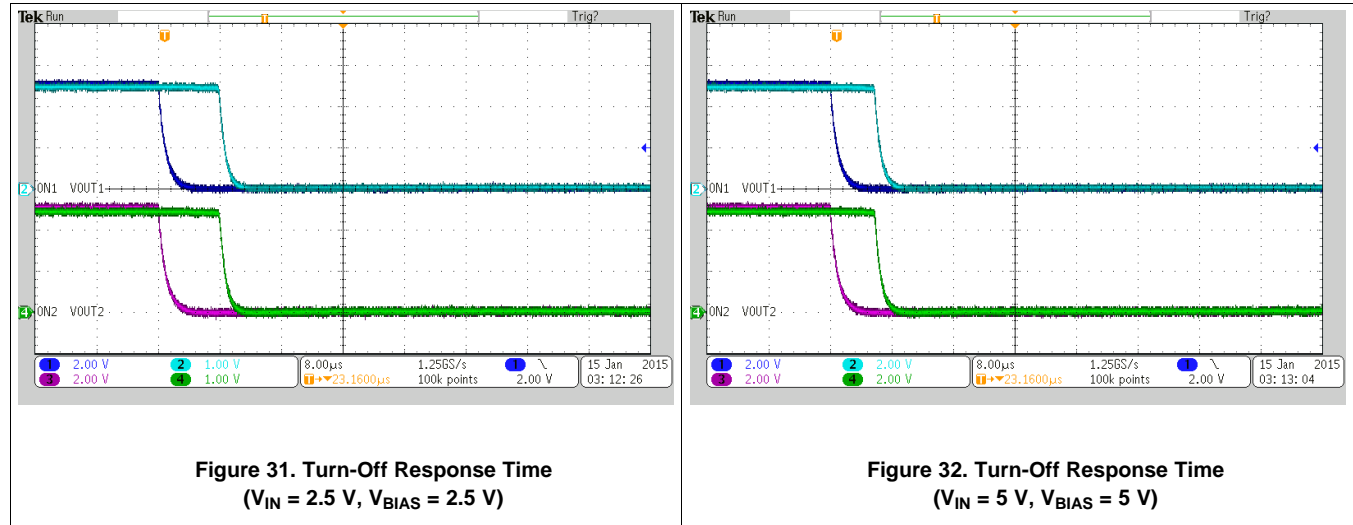
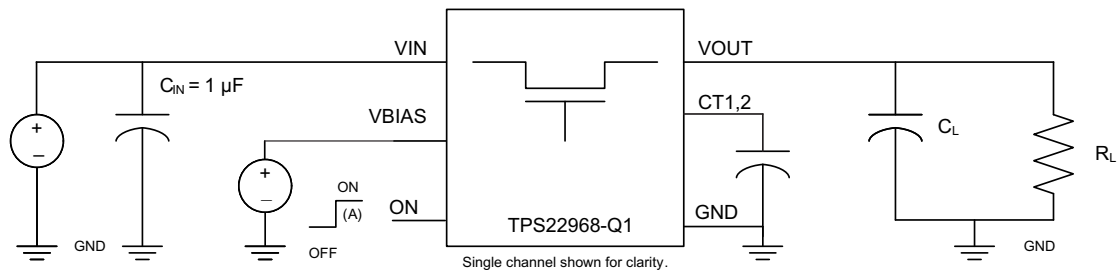


Figure 30. Turn-Off Response Time  
( $V_{IN} = 0.8\ \text{V}$ ,  $V_{BIAS} = 5\ \text{V}$ )

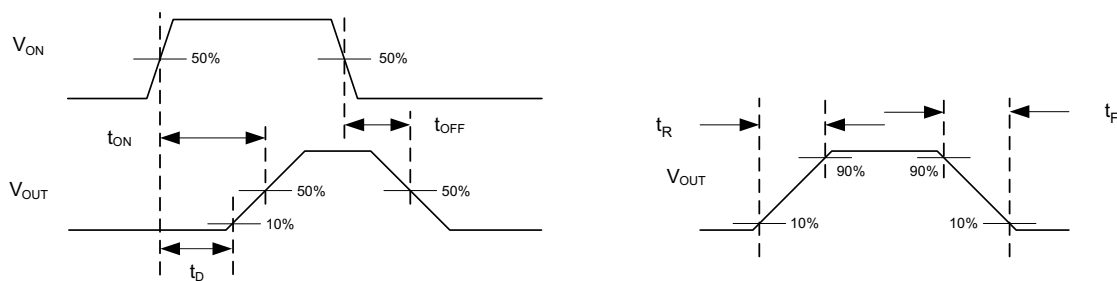
## Typical AC Characteristics (continued)

 $C_{IN} = 1\ \mu\text{F}$ ,  $C_L = 0.1\ \mu\text{F}$ ,  $R_L = 10\ \Omega$ ,  $C_T = 1\ \text{nF}$  (unless otherwise specified)


## 7 Parameter Measurement Information



Test Circuit



Timing Waveforms

- A. Rise and fall times of the control signal is 100 ns.

**Figure 33. Test Circuit and Timing Waveforms**

## 8 Detailed Description

### 8.1 Overview

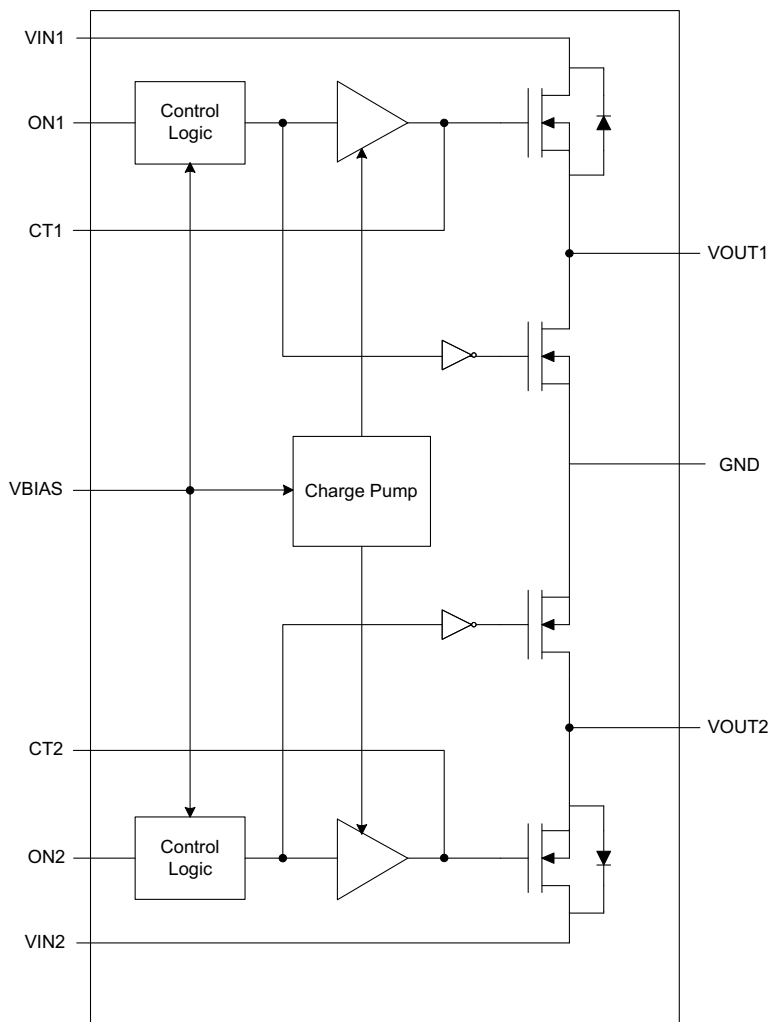
The device is a 5.5-V, 4-A, dual-channel ultra-low  $R_{ON}$  load switch with controlled turn on. The device contains two N-channel MOSFETs. Each channel can support a maximum continuous current of 4 A. Each channel is controlled by an on/off GPIO-compatible input. The ON pin must be connected and cannot be left floating. The device is designed to control the turn-on rate and therefore the inrush current. By controlling the inrush current, power supply sag can be reduced during turn-on. The slew rate for each channel is set by connecting a capacitor to GND on the CT pins.

The slew rate is proportional to the capacitor on the CT pin. Refer to [Adjustable Rise Time](#) to determine the correct CT value for a desired rise time.

The internal circuitry is powered by the VBIAS pin, which supports voltages from 2.5 to 5.5 V. This circuitry includes the charge pump, QOD, and control logic. For these internal blocks to function correctly, a voltage between 2.5 and 5.5 V must be supplied to VBIAS.

When a voltage is supplied to VBIAS and the ON1, 2 pin goes low, the QOD turns on. This connects VOUT1, 2 to GND through an on-chip resistor. The typical pulldown resistance ( $R_{PD}$ ) is 270  $\Omega$ .

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 ON/OFF Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

### 8.3.2 Quick Output Discharge (QOD)

The TPS22968-Q1 includes a QOD feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 270  $\Omega$  and prevents the output from floating while the switch is disabled.

### 8.3.3 Adjustable Rise Time

A capacitor to GND on the CT pins sets the slew rate for each channel. The capacitor to GND on the CT pins should be rated for 25 V and above. An approximate formula for the relationship between CT and slew rate with  $V_{BIAS} = 5$  V is:

$$SR = 0.35 \times CT + 25$$

where

- SR = slew rate (in  $\mu$ S/V)
- CT = the capacitance value on the CT pin (in pF)
- The units for the constant 25 is in  $\mu$ S/V.

(1)

Rise time can be calculated by multiplying the input voltage by the slew rate. [Table 1](#) contains rise time values measured on a typical device.

**Table 1. Rise Time Table**

CTx (pF)	Rise Time ( $\mu$ S) <sup>(1) (2)</sup>					
	$V_{IN} = 5$ V	$V_{IN} = 3.3$ V	$V_{IN} = 2.5$ V	$V_{IN} = 1.8$ V	$V_{IN} = 1.2$ V	$V_{IN} = 0.8$ V
0	84	63	52	43	35	27
220	418	285	223	168	122	88
470	711	479	372	276	196	139
1000	1405	952	738	545	385	271
2200	3236	2174	1684	1246	876	615
4700	6415	4306	3317	2454	1725	1217
10000	13872	9261	7150	5253	3694	2591

(1) 10% - 90%,  $C_L = 0.1$   $\mu$ F,  $C_{IN} = 1$   $\mu$ F,  $R_L = 10$   $\Omega$ ,  $V_{BIAS} = 5$  V

(2) Typical values at 25°C with a 25-V X7R 10% ceramic capacitor on CT

## 8.4 Device Functional Modes

**Table 2. Functional Table**

ONx	VINx to VOUTx	VOUTx to GND
L	Off	On
H	On	Off



## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

This section highlights some of the design considerations for implementing this device in various applications. A PSPICE model for this device is also available on the [product page](#) for further aid.

#### 9.1.1 Input Capacitor (Optional)

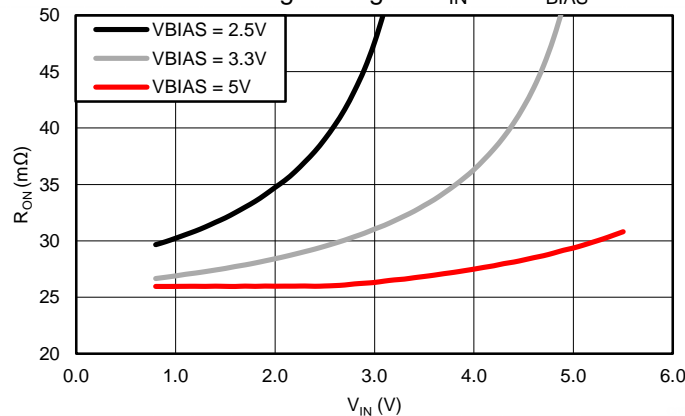
To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor must be placed between VIN and GND. A 1-μF ceramic capacitor, CIN, placed close to the pins, is usually sufficient. Higher values of CIN can be used to further reduce the voltage drop during high-current applications. When switching heavy loads, TI recommends to have an input capacitor about 10x higher than the output capacitor to avoid excessive voltage drop.

#### 9.1.2 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, TI highly recommends a CIN greater than CL. A CL greater than CIN can cause the voltage on VOUT to exceed VIN when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. TI recommends a CIN to CL ratio of 10 to 1 for minimizing VIN dip caused by inrush currents during startup.

#### 9.1.3 VIN and VBIAS Voltage Range

For optimal RON performance, make sure  $V_{IN} \leq V_{BIAS}$ . The device is still functional if  $V_{IN} > V_{BIAS}$ , but it will exhibit RON greater than what is listed in the [Electrical Characteristics \( \$V\_{BIAS} = 5\text{ V}\$ \)](#) and [Electrical Characteristics \( \$V\_{BIAS} = 2.5\text{ V}\$ \)](#). See [Figure 34](#) for an example of a typical device. Notice the increasing RON as VIN exceeds VBIAS voltage. Be sure to never exceed the maximum voltage rating for VIN and VBIAS.



$T_A = 25^\circ\text{C}$

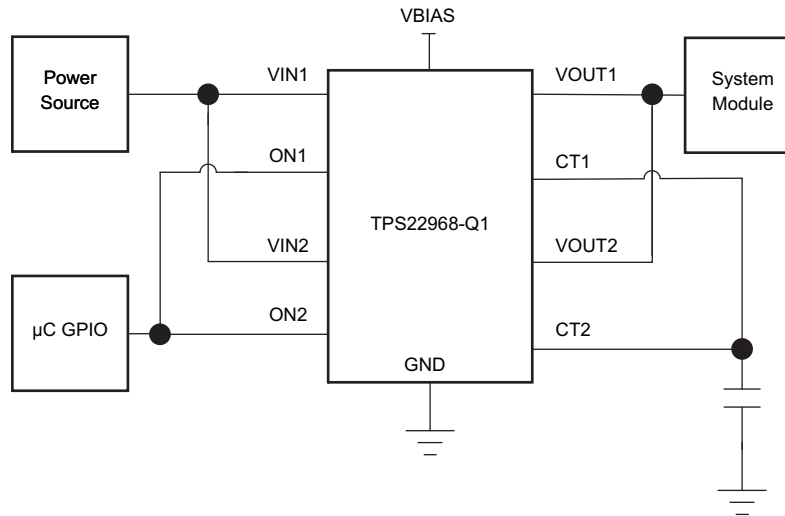
$I_{OUT} = -200\text{ mA}$

Figure 34. RON vs VIN

## Application Information (continued)

### 9.1.3.1 Parallel Configuration

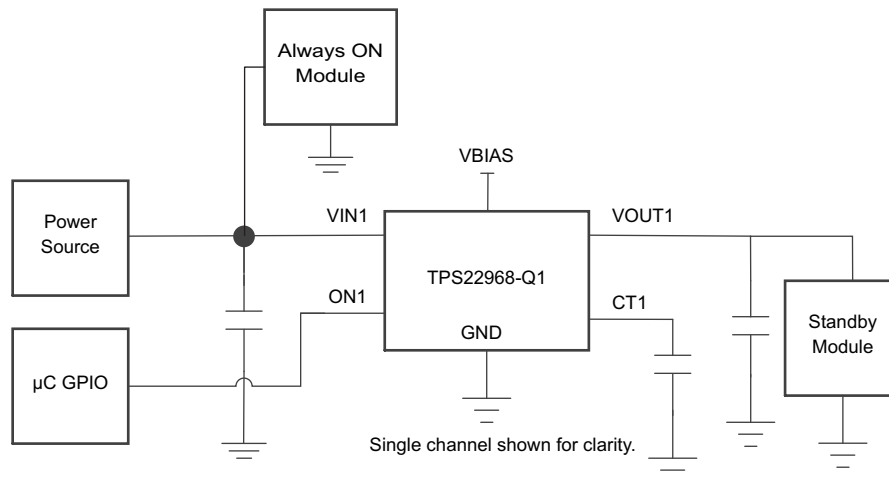
To increase the current capabilities and lower the  $R_{ON}$  by approximately 50%, both channels can be placed in parallel as shown in Figure 35 (parallel configuration). With this configuration, the CT1 and CT2 pins can be tied together to use one capacitor, CT, as shown in Figure 35. With a single CT capacitor, the rise time will be half of the typical rise-time value. Refer to the Table 1 for typical timing values.



**Figure 35. Parallel Configuration Schematic**

### 9.1.3.2 Standby Power Reduction

TPS22968-Q1 can help to reduce the standby power consumption of a module. Some loads will consume a non-trivial amount of power when turned off. If the power to the load is removed by the load switch, the standby power consumption can be significantly reduced.

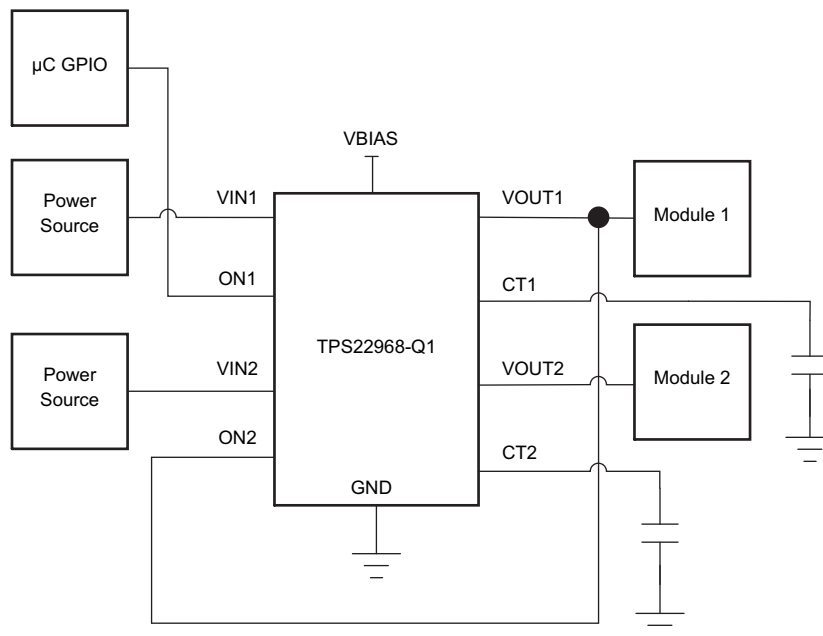


**Figure 36. Standby Power Reduction Schematic**

## Application Information (continued)

### 9.1.3.3 Power Supply Sequencing Without a GPIO Input

In many end equipments, there is a need to power up various modules in a predetermined manner. TPS22968-Q1 can solve the problem of power sequencing without adding any complexity to the overall system.

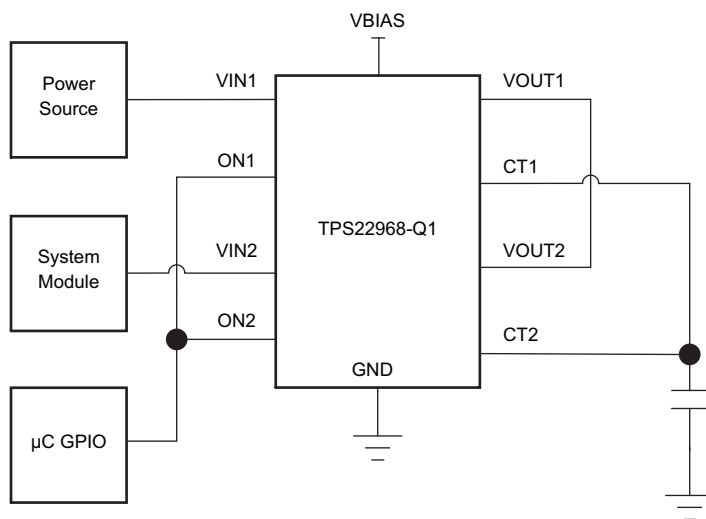


A. VIN1 must be greater  $V_{IH}$ .

**Figure 37. Power Sequencing Without a GPIO Input Schematic**

### 9.1.3.4 Reverse Current Blocking

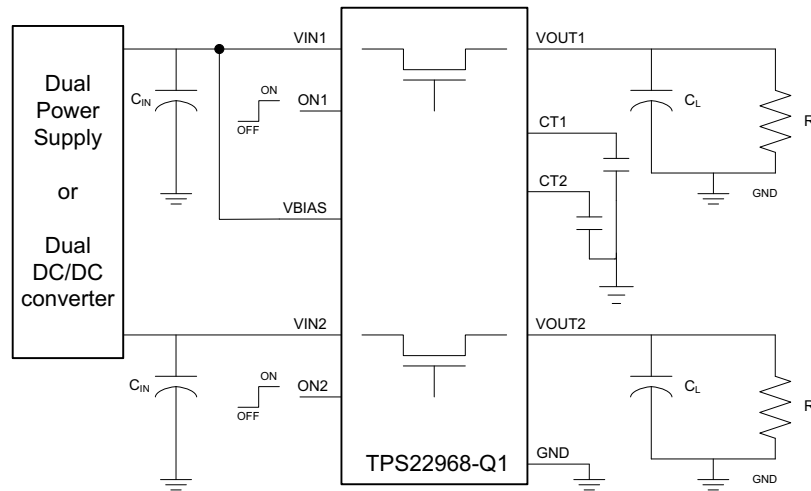
In certain applications, it may be desirable to have reverse current blocking. Reverse current blocking prevents current from flowing from the output to the input of the load switch when the device is disabled. With the following configuration, the TPS22968-Q1 can be converted into a single-channel switch with reverse current blocking. In this configuration, VIN1 or VIN2 can be used as the input and VIN2 or VIN1 is the output.



**Figure 38. Reverse Current Blocking Schematic**

## 9.2 Typical Application

This application demonstrates how the TPS22968-Q1 can be used to power a downstream load with a large capacitance. The example in [Figure 39](#) is powering a 22-μF capacitive output load.



**Figure 39. Typical Application Schematic for Powering a Downstream Module**

### 9.2.1 Design Requirements

For this design example, use the following as the input parameters.

**Table 3. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
V <sub>IN</sub>	3.3 V
V <sub>BIAS</sub>	5.0 V
Output capacitance (C <sub>L</sub> )	22 μF
Allowable inrush current on VOUT	0.400 A

### 9.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- V<sub>IN</sub> voltage
- V<sub>BIAS</sub> voltage
- Output capacitance (C<sub>L</sub>)
- Allowable inrush current on VOUT due to C<sub>L</sub> capacitor

#### 9.2.2.1 Inrush Current

To determine how much inrush current will be caused by the C<sub>L</sub> capacitor, use [Equation 2](#).

$$I_{\text{INRUSH}} = C_L \times \frac{dV_{\text{OUT}}}{dt}$$

where

- I<sub>INRUSH</sub> = amount of inrush current caused by C<sub>L</sub>
- C<sub>L</sub> = capacitance on VOUT
- dt = V<sub>OUT</sub> rise time
- dV<sub>OUT</sub> = increase in V<sub>OUT</sub> during the rise time

Inrush current is proportional to rise time. The rise time is adjustable by use of the CT capacitor. The appropriate rise time can be calculated using the design requirements and the inrush current equation ([Equation 2](#)).

$$400 \text{ mA} = 22 \text{ μF} \times 3.3 \text{ V} / dt \quad (3)$$

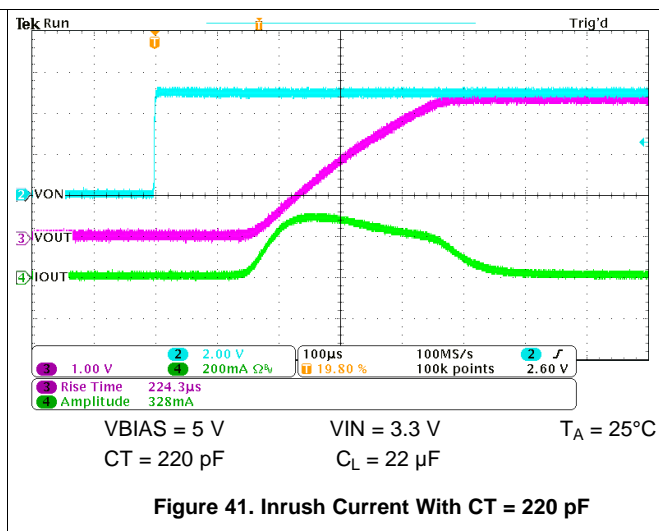
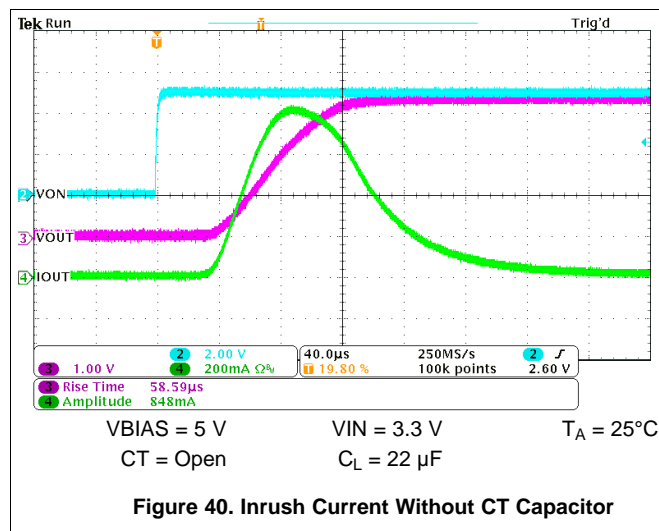
$$dt = 182 \text{ μs} \quad (4)$$

To ensure an inrush current of less than 400 mA, choose a CT capacitor value that will yield a rise time of more than 182  $\mu$ s. See the oscilloscope captures in the [Application Curves](#) for an example of how the CT capacitor can be used to reduce inrush current. See [Table 1](#) for correlation between rise times and CT values.

An appropriate  $C_L$  value should be placed on VOUT such that the  $I_{MAX}$  and  $I_{PLS}$  specifications of the device are not violated.

### 9.2.3 Application Curves

The two scope captures below show how the CT capacitor can be used to reduce inrush current.



## 10 Power Supply Recommendations

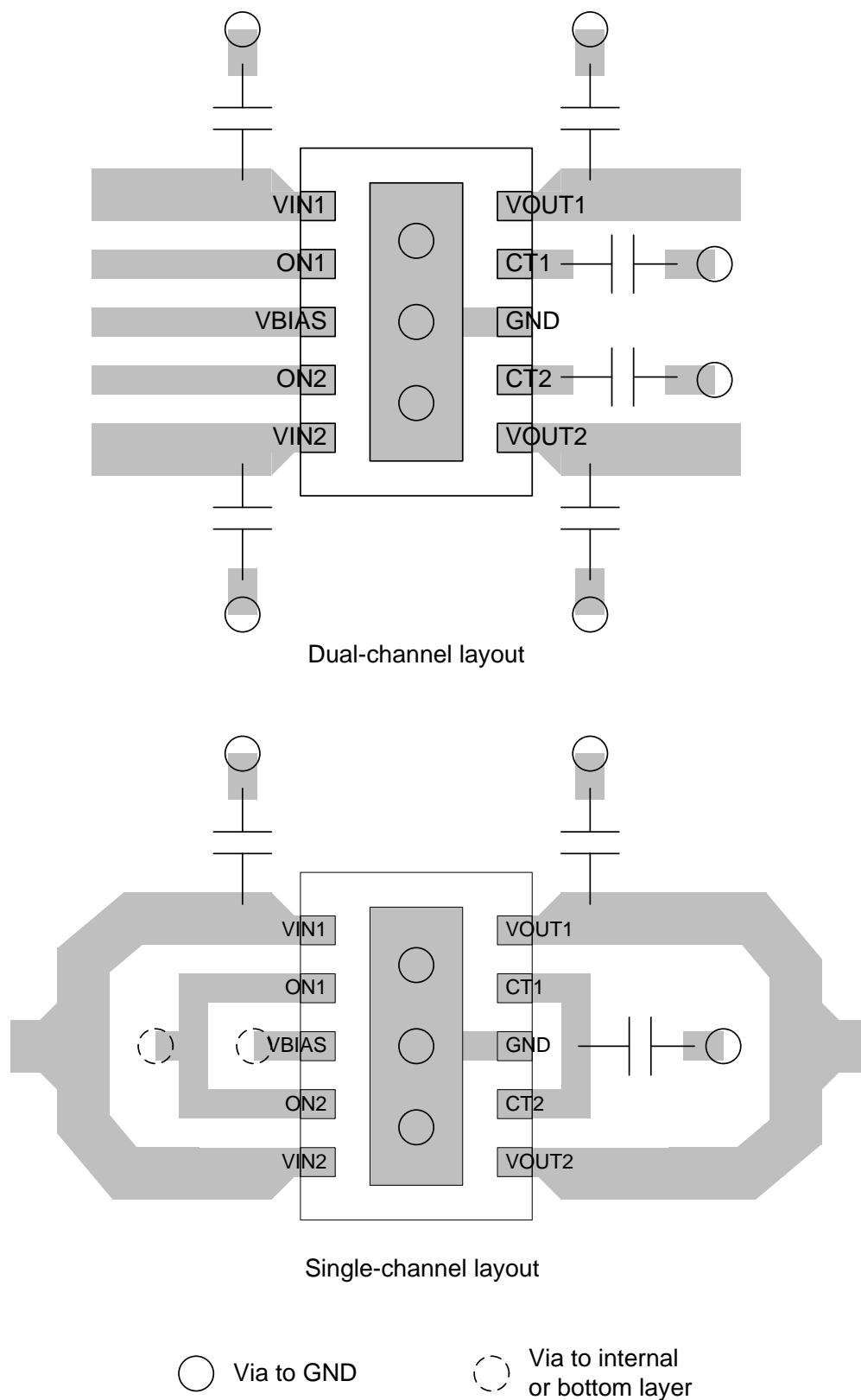
The device is designed to operate from a  $V_{BIAS}$  range of 2.5 to 5.5 V and  $V_{IN}$  range of 0.8 to 5.5 V. This supply must be well regulated and placed as close to the device pin as possible with the recommended 1- $\mu$ F bypass capacitor. If the supply is located more than a few inches from the device pins, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10  $\mu$ F may be sufficient.

## 11 Layout

### 11.1 Layout Guidelines

- VIN and VOUT traces should be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- VINx pins should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1- $\mu$ F ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- VOUTx pins should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VINx bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.
- The VBIAS pin should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 0.1- $\mu$ F ceramic with X5R or X7R dielectric.
- The CTx capacitors should be placed as close to the device pins as possible. The typical recommended CTx capacitance is a capacitor of X5R or X7R dielectric rating with a rating of 25 V or higher.

## 11.2 Layout Example



**Figure 42. Layout Schematic**

### 11.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. To calculate the maximum allowable dissipation,  $P_{D(max)}$  for a given ambient temperature, use [Equation 5](#).

$$P_{D(max)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}}$$

where

- $P_{D(max)}$  = maximum allowable power dissipation
- $T_{J(max)}$  = maximum allowable junction temperature (150°C for the TPS22968-Q1)
- $T_A$  = ambient temperature of the device
- $R_{\theta JA}$  = junction to air thermal impedance. See [Thermal Information](#). This parameter is highly dependent upon board layout. (5)

Following are two examples demonstrating how to use the above information: For  $V_{BIAS} = 5\text{ V}$ ,  $V_{IN} = 5\text{ V}$ , the maximum allowable ambient temperature with a 3-A load through each channel can be determined by using the following calculations.

#### NOTE

When calculating power dissipation in the switch, it is important to use the correct  $R_{ON}$  value.  $R_{ON}$  is dependent on the junction temperature of the device.

$$P_D = I^2 \times R \times 2 \text{ (multiplied by 2 because there are two channels)} \quad (6)$$

$$2 \times I^2 \times R = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (7)$$

$$T_A = T_{J(MAX)} - R_{\theta JA} \times 2 \times I^2 \times R \quad (8)$$

$$T_A = 150^\circ\text{C} - 55.6^\circ\text{C/W} \times 2 \times (3\text{ A})^2 \times 45\text{ m}\Omega = 105^\circ\text{C} \quad (9)$$

For  $V_{BIAS} = 5\text{ V}$ ,  $V_{IN} = 5\text{ V}$ , the maximum continuous current for an ambient temperature of 85°C with the same current flowing through each channel can be determined by using the following calculation:

$$2 \times I^2 \times R = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (10)$$

$$I = \sqrt{\frac{T_{J(MAX)} - T_A}{2 \times R \times R_{\theta JA}}} \quad (11)$$

$$I = \sqrt{\frac{150^\circ\text{C} - 85^\circ\text{C}}{2 \times 45\text{ m}\Omega \times 55.6^\circ\text{C/W}}} = 3.6\text{ A} \quad (12)$$



## 12 Device and Documentation Support

### 12.1 Trademarks

All trademarks are the property of their respective owners.

### 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22968QDMGRQ1	ACTIVE	WSO	DMG	10	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	SIV	<a href="#">Samples</a>
TPS22968QDMGTQ1	ACTIVE	WSO	DMG	10	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	SIV	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TPS22968-Q1 :**

- Catalog: [TPS22968](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22968QDMGRQ1	WSO	DMG	10	3000	179.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
TPS22968QDMGTQ1	WSO	DMG	10	250	179.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS

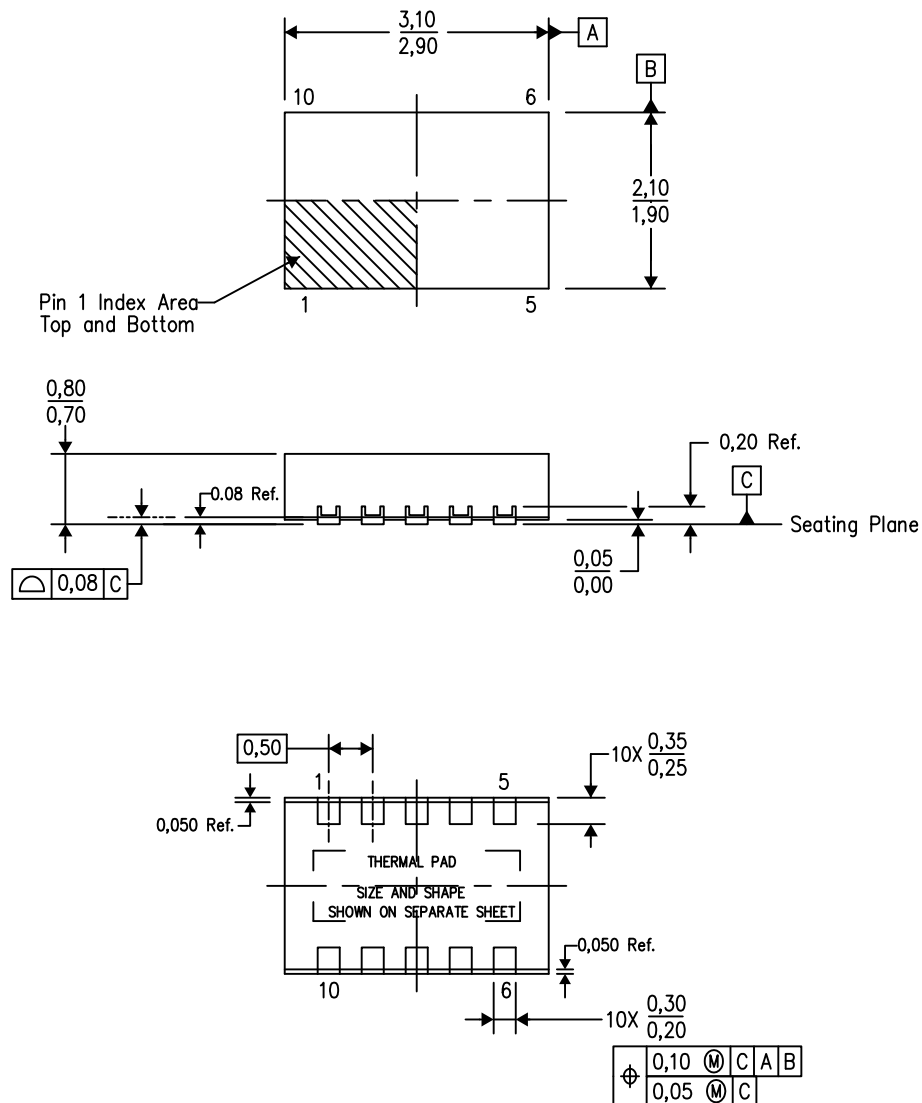


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22968QDMGRQ1	WSN	DMG	10	3000	195.0	200.0	45.0
TPS22968QDMGTQ1	WSN	DMG	10	250	195.0	200.0	45.0

DMG (R-PWSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



4221635/B 07/14

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - SON (Small Outline No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Side Lead Plating Process-1, matte tin only.

## THERMAL PAD MECHANICAL DATA

DMG (R-PWSON-N10)

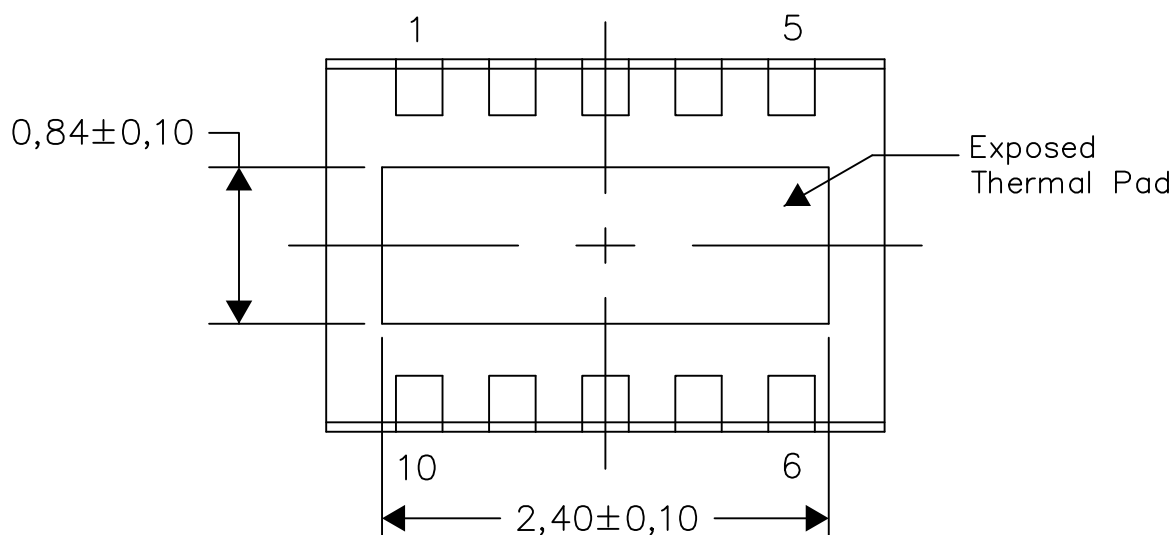
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4221653/A 07/14

NOTES: All linear dimensions are in millimeters

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