Abstract

As the complexity of new designs increases it becomes necessary to identify redundancies in the development process which may be abstracted out in future development efforts. Such abstractions in the design and validation process are apparent in the evolution of logic design methodologies from transistor level to gate level (1970s),  gate level to register level (1990s), and today’s ongoing push to adopt transaction level. My work at Intel has been centered on developing a preprocessor for enabling an emerging logic design methodology, System Verilog Extension (SVX), which provides greater abstraction than register level methodology, without sacrificing necessary granularity.