$valid

@0: A,

@1:

@2:

@3:

@4:

@5:

@6:

@7:

@8:

@9:

@10: U,

Gating condition at stages:

?valid

@12

@13

@14

@15

@16

@17

@18

?mem\_op

@14

@15

@16

@17

@18

@19

@20

@21

@22

?arith\_op

@20

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Stage | Numeric Representation | Assigned Ranges | Used Ranges | Transition Type | Transition Range | Gating condition |
| 0H | 0 | \* |  |  |  |  |
| 0L | 1 |  |  | F1 | \* | N/A |
| 1H | 2 |  |  | F2 | \* | N/A |
| 1L | 3 |  |  | F1 | \* | N/A |
| 2H | 4 |  |  | F2 | \* | N/A |
| 2L | 5 |  |  | F1 | \* | N/A |
| 3H | 6 |  |  | F2 | \* | N/A |
| 3L | 7 |  |  | F1 | \* | N/A |
| 4H | 8 |  |  | F2 | \* | N/A |
| 4L | 9 |  |  | F1 | \* | N/A |
| 5H | 10 |  | \* | F2 | \* | N/A |
| 5L | 11 |  |  | F1 | \* | N/A |
| 6H | 12 |  | \*(Clk) | F2 | \* | N/A |

$raw\_inst

?valid

@12: A[28:0], U[28:27],

?mem\_op

@14: U[15:0],

@15:

@16:

@17:

@18:

@19:

@20:

@21:

@22: U[18:9],

?arith\_op

@20: U,

raw\_inst\_UX6H\_valid[28:0] = (valid\_UX6H) ? … : X;

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Stage | Numeric Representation | Assigned Ranges | Used Ranges | Transition Type | Transition Range | Gating condition |
| 6H | 12 | [28:0] | [28:27] |  |  | valid\_UX6H |
| 6L | 13 |  |  | F1 | \* |  |
| 7H | 14 |  | [18:0](Clk) | F2 | \* | valid\_UX7H |
| 7L | 15 |  |  | F1 | \* |  |
| 8H | 16 |  |  | F2 | \* | valid\_UX8H |
| 8L | 17 |  |  | F1 | \* |  |
| 9H | 18 |  |  | F2 | \* | valid\_UX9H |
| 9L | 19 |  |  | F1 | \* |  |
| 10H | 20 |  | \*(Clk) | F2 | \* | valid\_UX10H |

raw\_inst\_UX7H\_valid\_AND\_mem\_op[18:0] = (valid\_AND\_mem\_op\_UX7H) ? raw\_inst\_UX7H\_valid[18:0]: X;

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Stage | Numeric Representation | Assigned Ranges | Used Ranges | Transition Type | Transition Range | Gating condition |
| 7H | 14 |  | [15:0] |  | [18:0] | valid\_AND\_mem\_op\_UX7H |
| 7L | 15 |  |  | F1 | [18:9] |  |
| 8H | 16 |  |  | F2 | [18:9] | valid\_AND\_mem\_op\_UX8H |
| 8L | 17 |  |  | F1 | [18:9] |  |
| 9H | 18 |  |  | F2 | [18:9] | valid\_AND\_mem\_op\_UX9H |
| 9L | 19 |  |  | F1 | [18:9] |  |
| 10H | 20 |  |  | F2 | [18:9] | valid\_AND\_mem\_op\_UX10H |
| 10L | 21 |  |  | F1 | [18:9] |  |
| 11H | 22 |  | [18:9] | F2 | [18:9] | valid\_AND\_mem\_op\_UX11H |

raw\_inst\_UX10H\_valid\_AND\_arith\_op = ?(valid\_AND\_arith\_op\_UX10H) raw\_inst\_valid\_UX10H: X;

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Stage | Numeric Representation | Assigned Ranges | Used Ranges | Transition Type | Transition Range | Gating condition |
| 10H | 20 |  | [15:0] |  |  |  |