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Urządzenia Cyfrowe i Systemy Wbudowane

Licznik rewersyjny 0-1-7-2-3-4-5-6

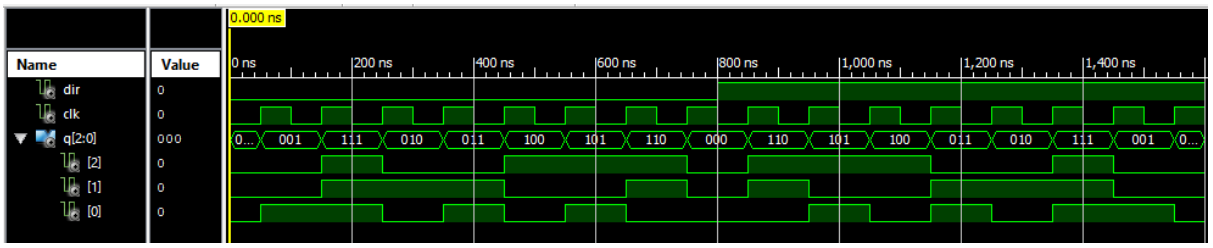
1. Projekt VHDL

```
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22
23  -- Uncomment the following library declaration if using
24  -- arithmetic functions with Signed or Unsigned values
25  --use IEEE.NUMERIC_STD.ALL;
26
27  -- Uncomment the following library declaration if instantiating
28  -- any Xilinx primitives in this code.
29  library UNISIM;
30  use UNISIM.VComponents.all;
31
32  entity lab3_2 is
33      Port ( DIR : in  STD_LOGIC;
34             CLK : in  STD_LOGIC;
35             Q : out  STD_LOGIC_VECTOR (2 downto 0));
36  end lab3_2;
37
38  architecture Behavioral of lab3_2 is
39  signal D_Int : STD_LOGIC_VECTOR (3 downto 0); -- current internal state
40  signal Q_Int : STD_LOGIC_VECTOR (2 downto 0); -- future internal state
41
42  begin
43     D_1 : FDCE port map (CLR => '0', CE => '1', C => CLK, D => Q_Int(0), Q => D_Int(0));
44     D_2 : FDCE port map (CLR => '0', CE => '1', C => CLK, D => Q_Int(1), Q => D_Int(1));
45     D_3 : FDCE port map (CLR => '0', CE => '1', C => CLK, D => Q_Int(2), Q => D_Int(2));
46
47     D_Int(3) <= DIR;
48
49     with D_Int select
50        Q_Int <= "001" when "0000" | "1111",
51                 "111" when "0001" | "1010",
52                 "011" when "0010" | "1100",
53                 "100" when "0011" | "1101",
54                 "101" when "0100" | "1110",
55                 "110" when "0101" | "1000",
56                 "000" when "0110" | "1001",
57                 "010" when "0111" | "1011",
58                 "000" when others;
59
60     Q(2) <= D_Int(2);
61     Q(1) <= D_Int(1);
62     Q(0) <= D_Int(0);
63  end architecture Behavioral;
64
```

2. Test Bench

```
28  LIBRARY ieee;
29  USE ieee.std_logic_1164.ALL;
30
31  -- Uncomment the following library declaration if using
32  -- arithmetic functions with Signed or Unsigned values
33  --USE ieee.numeric_std.ALL;
34
35  ENTITY lab3_2_test IS
36  END lab3_2_test;
37
38  ARCHITECTURE behavior OF lab3_2_test IS
39
40      -- Component Declaration for the Unit Under Test (UUT)
41
42      COMPONENT lab3_2
43      PORT(
44           DIR : IN  std_logic;
45           CLK : IN  std_logic;
46           Q : OUT  std_logic_vector(2 downto 0)
47          );
48      END COMPONENT;
49
50
51     --Inputs
52     signal DIR : std_logic := '0';
53     signal CLK : std_logic := '0';
54
55     --Outputs
56     signal Q : std_logic_vector(2 downto 0);
57
58  BEGIN
59
60     -- Instantiate the Unit Under Test (UUT)
61     uut: lab3_2 PORT MAP (
62             DIR => DIR,
63             CLK => CLK,
64             Q => Q
65           );
66
67    CLK <= not CLK after 50 ns;
68    DIR <= '0', '1' after 800 ns;
69
70  END;
71
```

3. Wyniki symulacji behawioralnej



4. Wnioski

Układ został poprawnie zaprojektowany na zajęciach nie starczyło jednak czasu na przeprowadzenie symulacji behawioralnej.