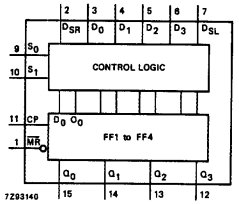

Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
reset (clear)	X	L	X	X	X	X	X	L	L	L	L
hold ("do nothing")	X	H	l	l	X	X	X	q_0	q_1	q_2	q_3
shift left	↑	H	h	l	X	l	X	q_1	q_2	q_3	L
	↑	H	h	l	X	h	X	q_1	q_2	q_3	H
shift right	↑	H	l	h	l	X	X	L	q_0	q_1	q_2
	↑	H	l	h	h	X	X	H	q_0	q_1	q_2
parallel load	↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

Notes

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
   q,d = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition
   X = don't care
   ↑ = LOW-to-HIGH CP transition

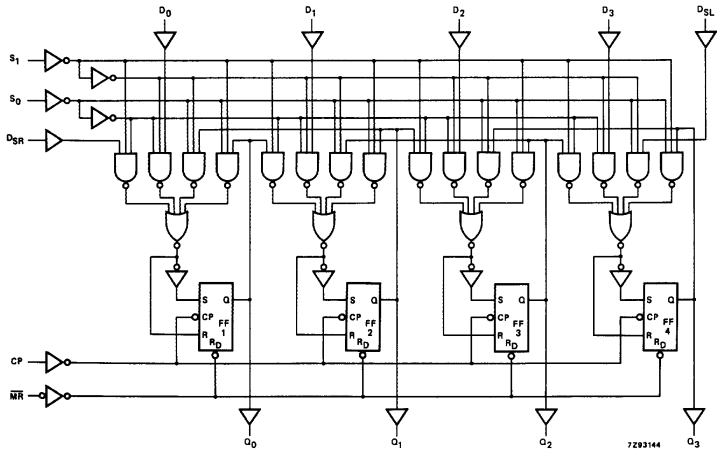

Fig.5 Logic diagram.

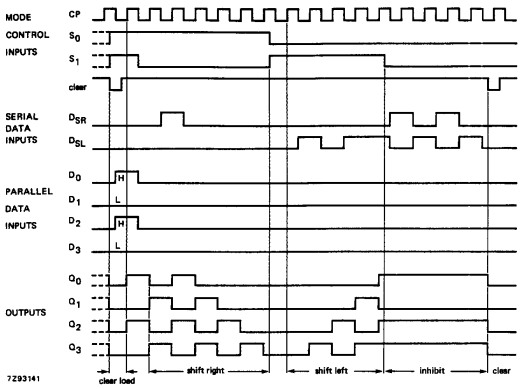

Fig.6 Typical clear, clear-load, shift-right, shift-left, inhibit and clear timing sequences.

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT194
4-bit bidirectional universal shift register

Product specification
File under Integrated Circuits, IC06

December 1990

Philips Semiconductors

PHILIPS

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset input (active LOW)
2	D_{SR}	serial data input (shift right)
3, 4, 5, 6	D_0 to D_3	parallel data inputs
7	D_{SL}	serial data input (shift left)
8	GND	ground (0 V)
9, 10	S_0, S_1	mode control inputs
11	CP	clock input (LOW-to-HIGH edge-triggered)
15, 14, 13, 12	Q_0 to Q_3	parallel outputs
16	V_{CC}	positive supply voltage

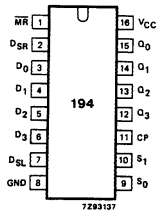

Fig.1 Pin configuration.

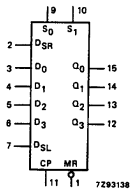

Fig.2 Logic symbol.

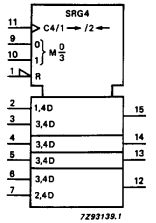

Fig.3 IEC logic symbol.