DATA SHEET

74HC74; 74HCT74
Dual D-type flip-flop with set and reset; positive-edge trigger

Product specification
Supersedes data of 1998 Feb 23

2003 Jul 10

PINNING

PIN	SYMBOL	DESCRIPTION
1	$1\overline{R}D$	asynchronous reset-direct input (active LOW)
2	1D	data input
3	1CP	clock input (LOW-to-HIGH, edge-triggered)
4	$1\overline{S}D$	asynchronous set-direct input (active LOW)
5	1Q	true flip-flop output
6	$1\overline{Q}$	complement flip-flop output
7	GND	ground (0 V)
8	$2\overline{Q}$	complement flip-flop output
9	2Q	true flip-flop output
10	$2\overline{S}D$	asynchronous set-direct input (active LOW)
11	2CP	clock input (LOW-to-HIGH, edge-triggered)
12	2D	data input
13	$2\overline{R}D$	asynchronous reset-direct input (active LOW)
14	V_{CC}	positive supply voltage

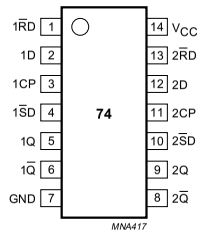
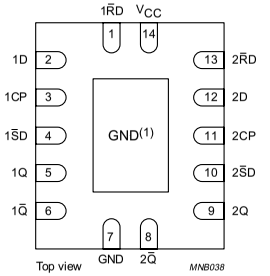


Fig.1 Pin configuration DIP14, SO14 and (T)SSOP14.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

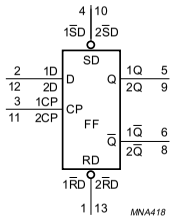


Fig.3 Logic symbol.

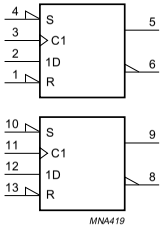


Fig.4 IEC logic symbol.

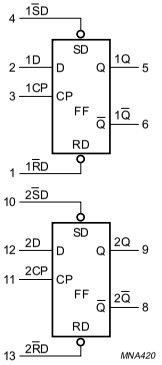


Fig.5 Functional diagram.