# 8-bit serial-in/parallel-out shift register

# 74HC/HCT164



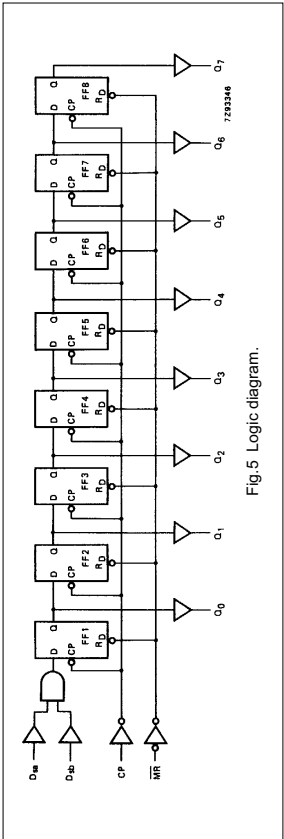Fig.4 Functional diagram.
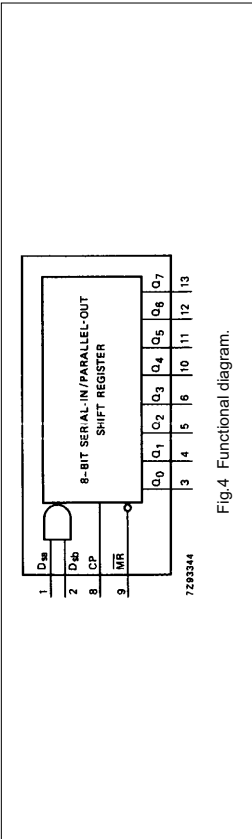
## APPLICATIONS

- Serial data transfer

## FUNCTION TABLE

| OPERATING MODES | INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| | $\overline{MR}$ | CP | $D_{sa}$ | $D_{sb}$ | $Q_0$ | $Q_1 - Q_7$ |
| reset (clear) | L | X | X | X | L | L – L |
| shift | H | ↑ | l | l | L | $q_0 - q_6$ |
| | H | ↑ | l | h | L | $q_0 - q_6$ |
| | H | ↑ | h | l | L | $q_0 - q_6$ |
| | H | ↑ | h | h | H | $q_0 - q_6$ |

**Note**

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
   q = lower case letters indicate the state of the referenced input one set-up time prior to the
   LOW-to-HIGH clock transition
   ↑ = LOW-to-HIGH clock transition



Fig.5 Logic diagram.

## PIN DESCRIPTION

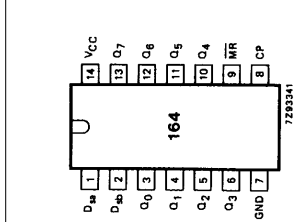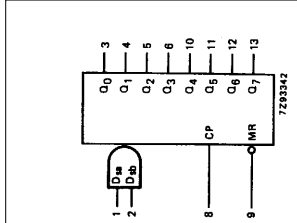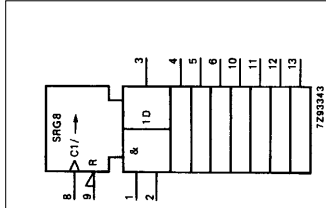| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1, 2 | $D_{sa}$, $D_{sb}$ | data inputs |
| 3, 4, 5, 6, 10, 11, 12, 13 | $Q_0$ to $Q_7$ | outputs |
| 7 | GND | ground (0 V) |
| 8 | CP | clock input (LOW-to-HIGH, edge-triggered) |
| 9 | $\overline{MR}$ | master reset input (active LOW) |
| 14 | $V_{CC}$ | positive supply voltage |



Fig.1 Pin configuration.



Fig.2 Logic symbol.



Fig.3 IEC logic symbol.

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INTEGRATED CIRCUITS

# DATA SHEET

For a complete data sheet, please also download:

• The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
• The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
• The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

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Product specification
File under Integrated Circuits, IC06

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