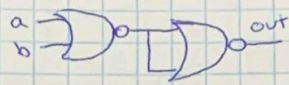


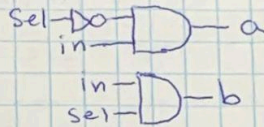
CSCE312 LE1 + Project 1 Gate Drawings

Tiernan Lindsay
134003853

And

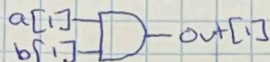
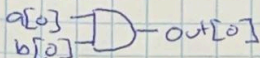


DMux



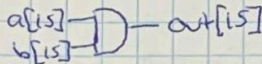
(gates are alphabetical)

And16

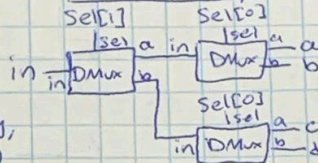


⋮

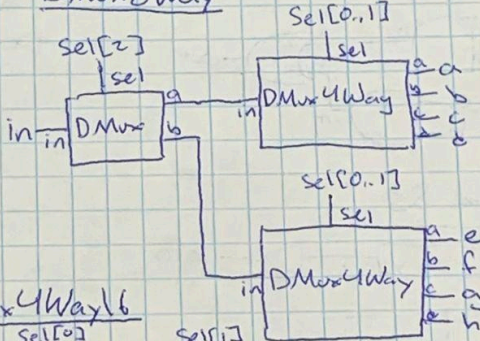
(removed for brevity, but same pattern)



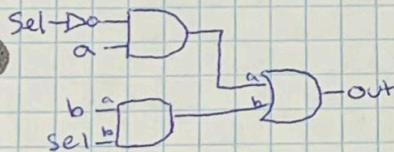
DMux 4Way



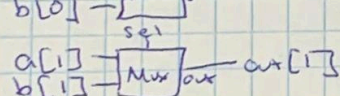
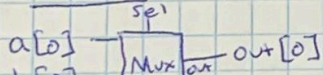
DMux 8Way



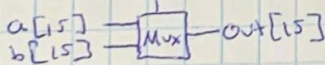
Mux



Mux16



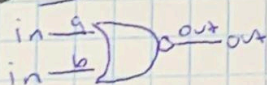
⋮



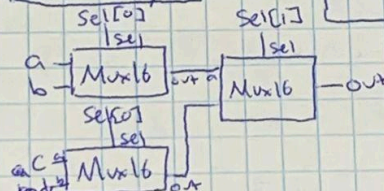
Nor

(already implemented)

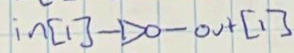
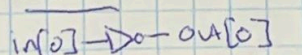
Not



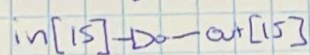
Mux 4Way16



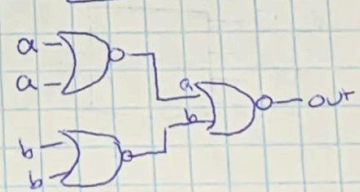
Not16



⋮

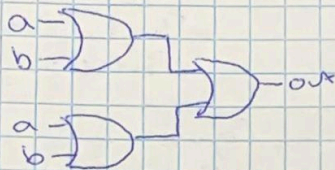


Or

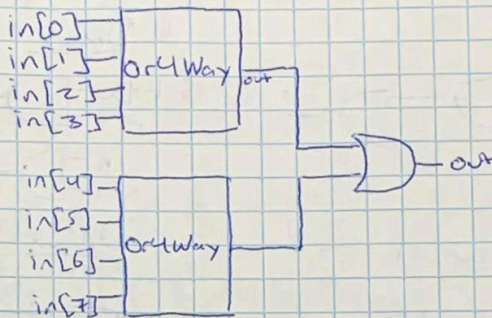


(Encoder 83 on back page)

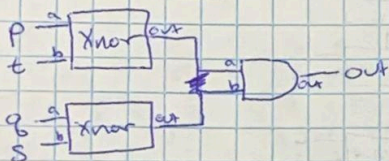
Or4Way



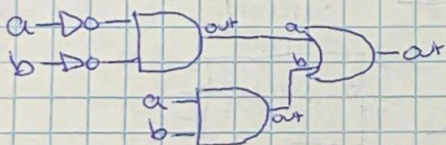
Or8Way



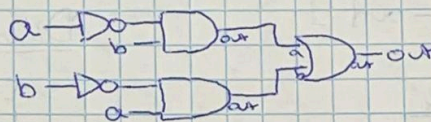
Palindrone



Xnor



Xor



Encoder 83

