Files needed

Make a folder and keep these file – run.tcl

- #### Template Script for RTL->Gate-Level Flow (generated from GENUS 17.10-p007_1)

- ##
- ## Library setup
- ##

- set_db / .library {"../LIB/slow.lib" "../LIB/fast.lib"}
- ## PLE
- set_db / .lef_library { "../LEF/gsclib045_tech.lef" "../LEF/gsclib045_macro.lef" }
- ## Provide either cap_table_file or the qrc_tech_file
- ##set_db / .cap_table_file <file>
- #set_db / .qrc_tech_file <file>

- ##set_db / .lp_insert_clock_gating true

- if {[file exists /proc/cpuinfo]}{
- sh grep "model name" /proc/cpuinfo
- sh grep "cpu MHz" /proc/cpuinfo
- }

- puts "Hostname : [info hostname]"

Keep this under RTL folder counter_4b.v

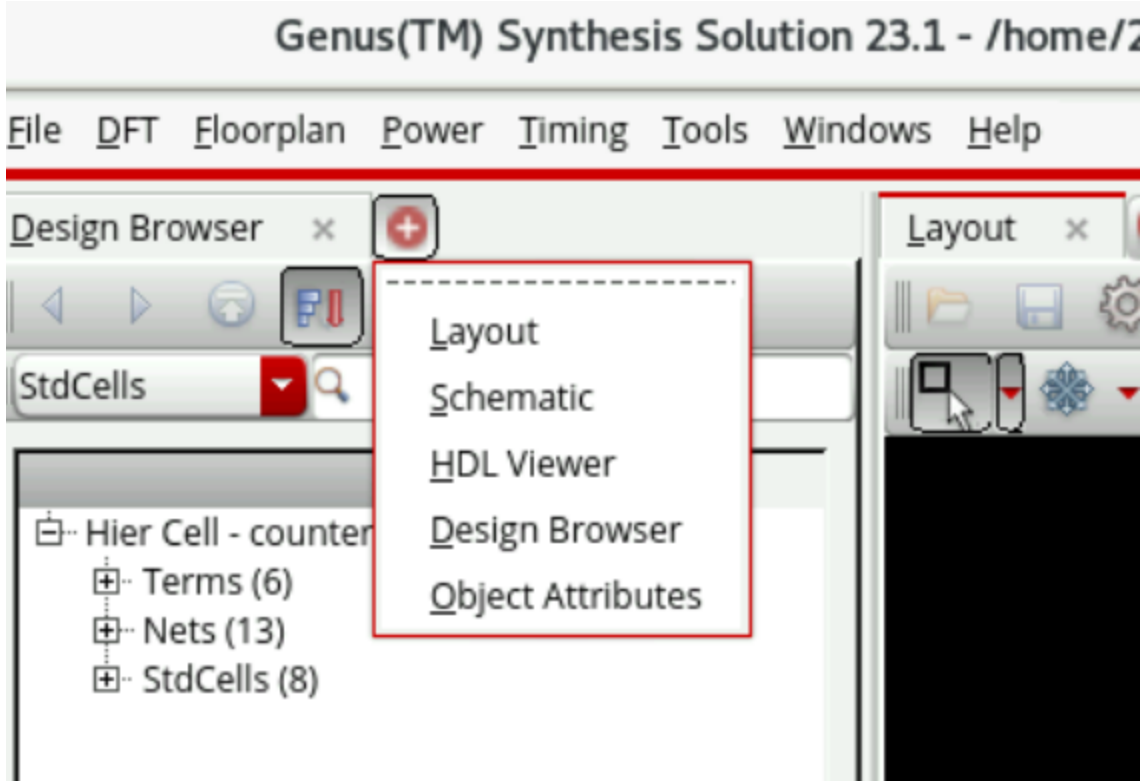
- `timescale 1ns/1ps
- module counter_4b(lclk,lrst,count);
- input lclk,lrst;
- output reg [3:0] count;
- always @(posedge lclk or posedge lrst)
- begin
- if(lrst)
- count=0;
- else
- count=count+1;
- end
- endmodule

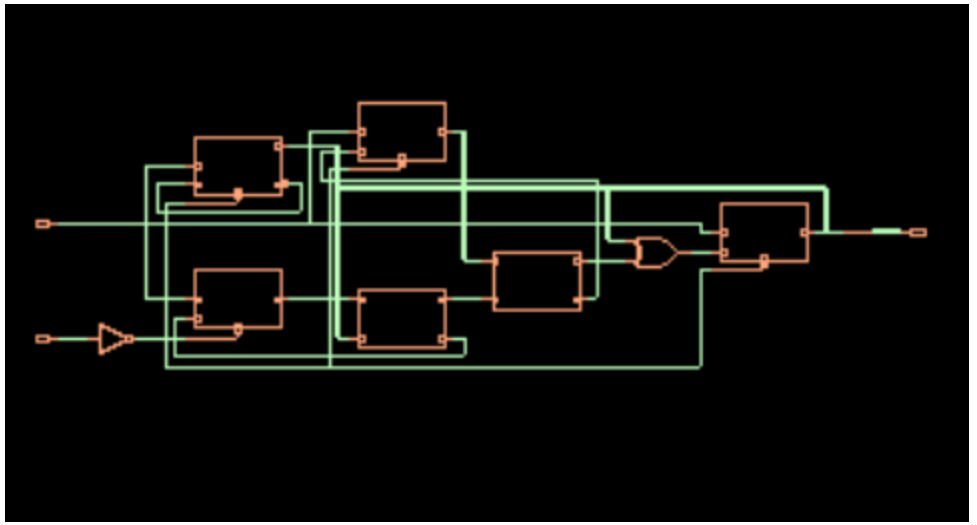
Under constraints counter_4b.sdc

- create_clock -name lclk -period 8.0 -waveform {0 4} [get_ports "lclk"]
- set_clock_transition -rise 0.1 "lclk"
- set_clock_transition -fall 0.1 "lclk"
- set_clock_uncertainty 0.1 "lclk"
- set_input_delay -max 1 [get_ports "lrst"] -clock [get_clocks "lclk"]
- set_output_delay -max 1 [get_ports "count"] -clock [get_clocks "lclk"]

Start from cadence terminal

- Cmd >csh
- Cmd >source cshrc
- Go to design folder
- cmd>genus –f run.tcl
- Cmd>gui_show
- Click + select schematic
- You will see sch– similar to this `
- Cmd> innovus
- New window will open… leave it as is


Genus(TM) Synthesis Solution 23.1 - /home/2
File DFT Floorplan Power Timing Tools Windows Help
Design Browser
Layout
StdCells
Layout
Schematic
HDL Viewer
Design Browser
Object Attributes
Hier Cell - counter
Terms (6)
Nets (13)
StdCells (8)



Create this file under workarea Default.globals

- set conf_qxconf_file {NULL}
- set conf_qxlib_file {NULL}
- set defHierChar {/}
- set init_design_settop 0
- set init_gnd_net {VSS}
- set init_pwr_net {VDD}
- set init_lef_file {"../LEF/gsclib045_tech.lef" "../LEF/gsclib045_macro.lef"}

Create this file in workarea Default.view

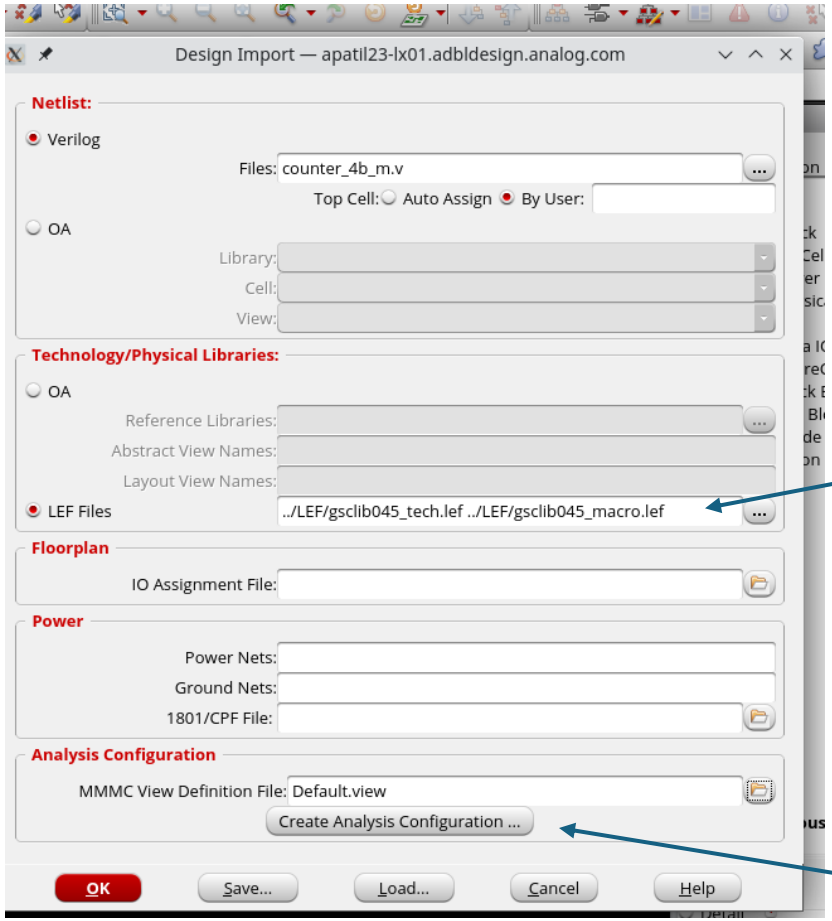
- # Version:1.0 MMMC View Definition File
- # Do Not Remove Above Line
- create_library_set -name MAX_lib -timing "../LIB/slow.lib"
- create_library_set -name MIN_lib -timing "../LIB/fast.lib"
- create_constraint_mode -name Constraints -sdc_files {counter_4b_m.sdc}
- create_constraint_mode -name Constraints2 -sdc_files {counter_4b_m.sdc}
- create_timing_condition -name worst_t -library_sets MAX_lib
- create_timing_condition -name best_t -library_sets MIN_lib

- create_delay_corner -name worst -timing_condition {worst_t}
- create_delay_corner -name best -timing_condition {best_t}
- create_analysis_view -name Worst_delay -constraint_mode {Constraints} -delay_corner {worst}
- create_analysis_view -name Best_delay -constraint_mode {Constraints2} -delay_corner {best}
- set_analysis_view -setup {Worst_delay} -hold {Best_delay}

On innovus terminal copy past these

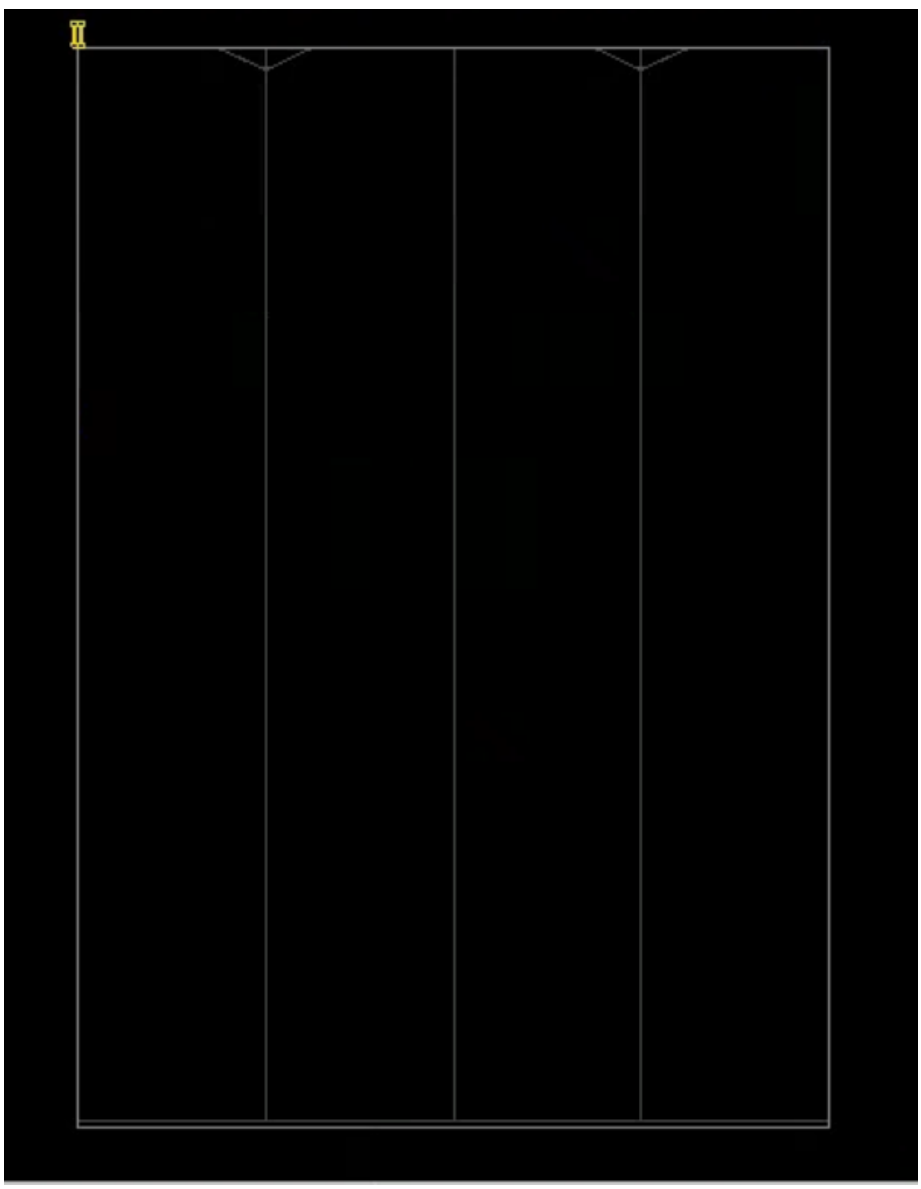
- cmd>source Default.globals

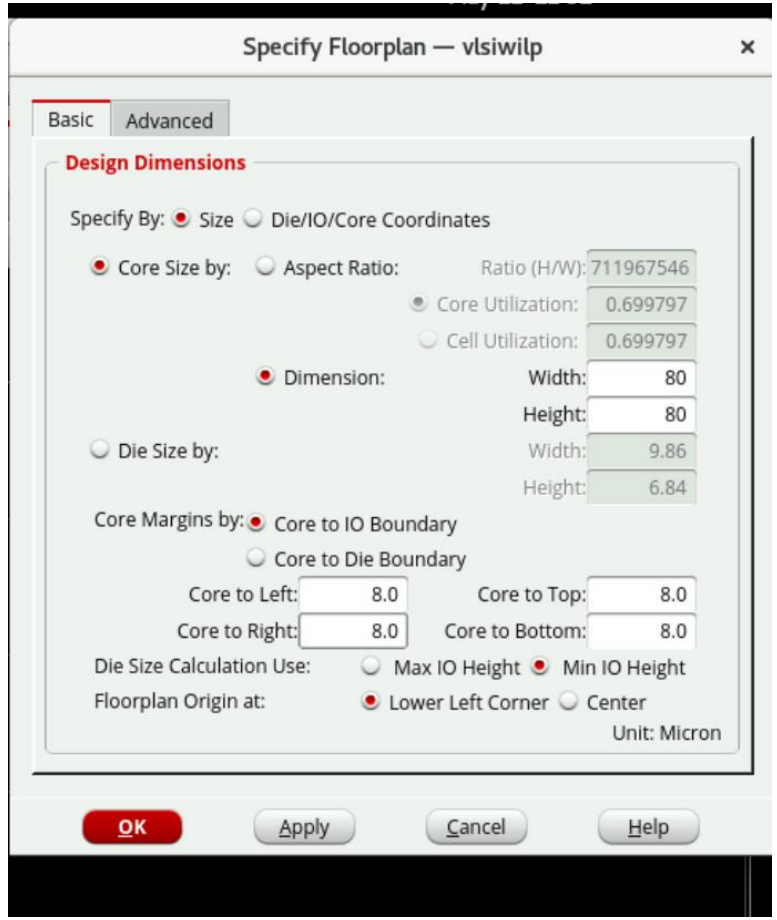
Now Import design (_m.v is in the project folder not output folder)

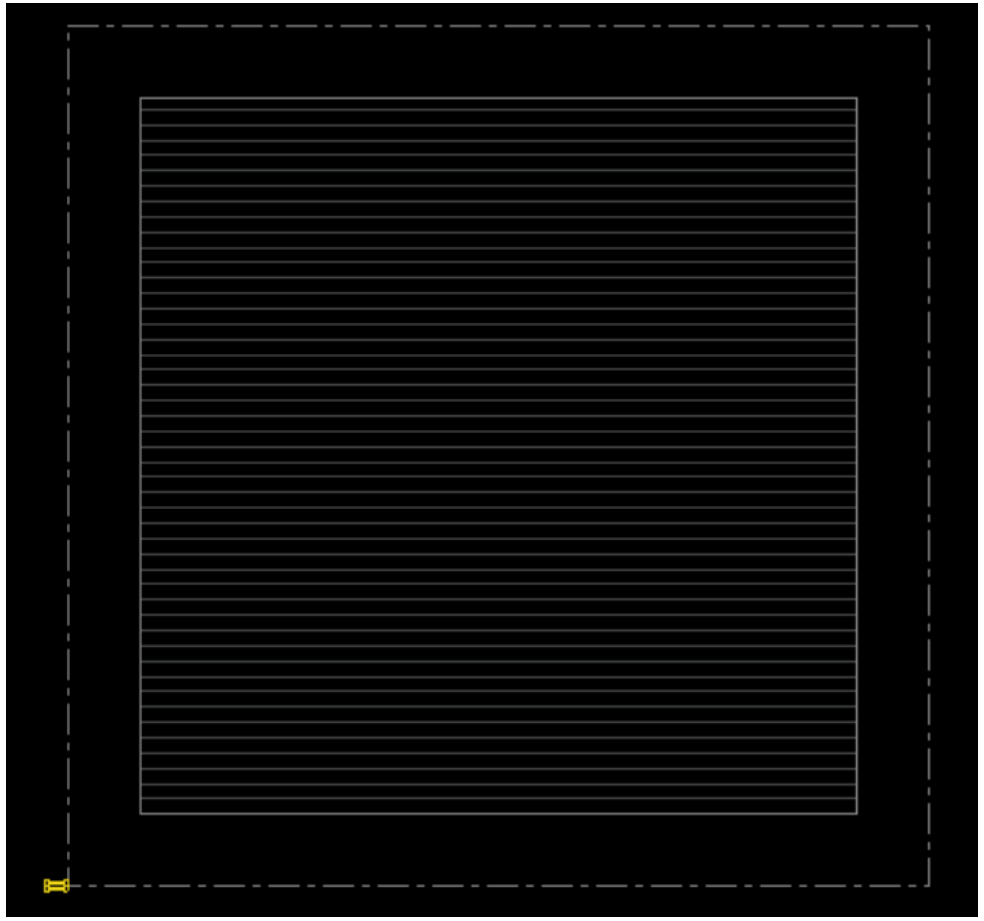


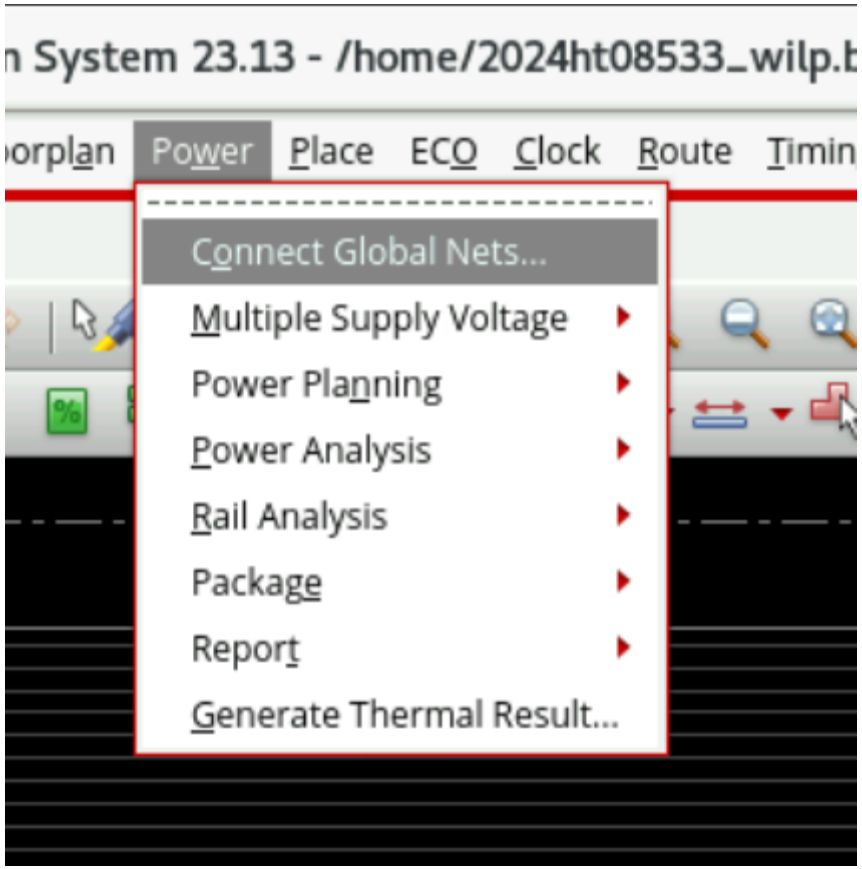
Seq is important

Do not click this
Else you have to create the file aga

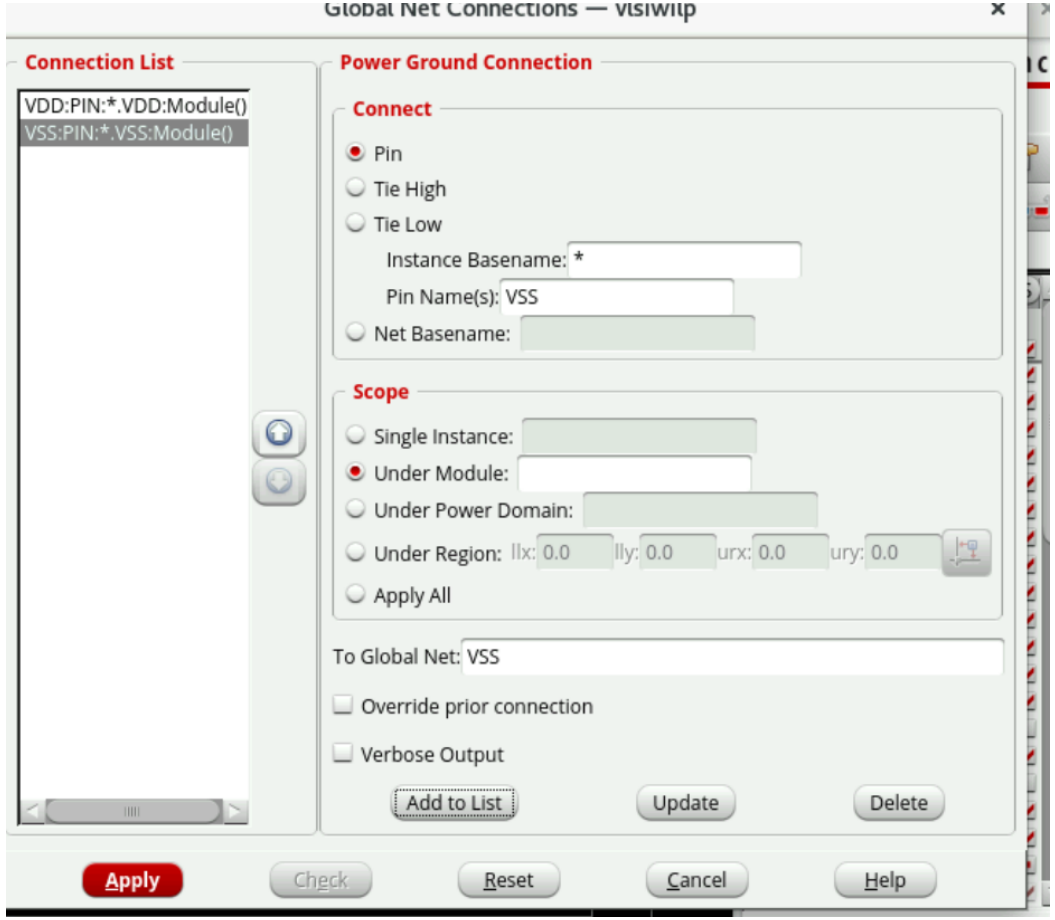



Specify Floorplan — vlsiwilp
Basic
Advanced
Design Dimensions
Specify By: Size Die/IO/Core Coordinates
Core Size by: Aspect Ratio: Ratio (H/W): 711967546
Core Utilization: 0.699797
Cell Utilization: 0.699797
Dimension: Width: 80
Height: 80
Die Size by: Width: 9.86
Height: 6.84
Core Margins by: Core to IO Boundary
Core to Die Boundary
Core to Left: 8.0
Core to Top: 8.0
Core to Right: 8.0
Core to Bottom: 8.0
Die Size Calculation Use: Max IO Height Min IO Height
Floorplan Origin at: Lower Left Corner Center
Unit: Micron
OK
Apply
Cancel
Help

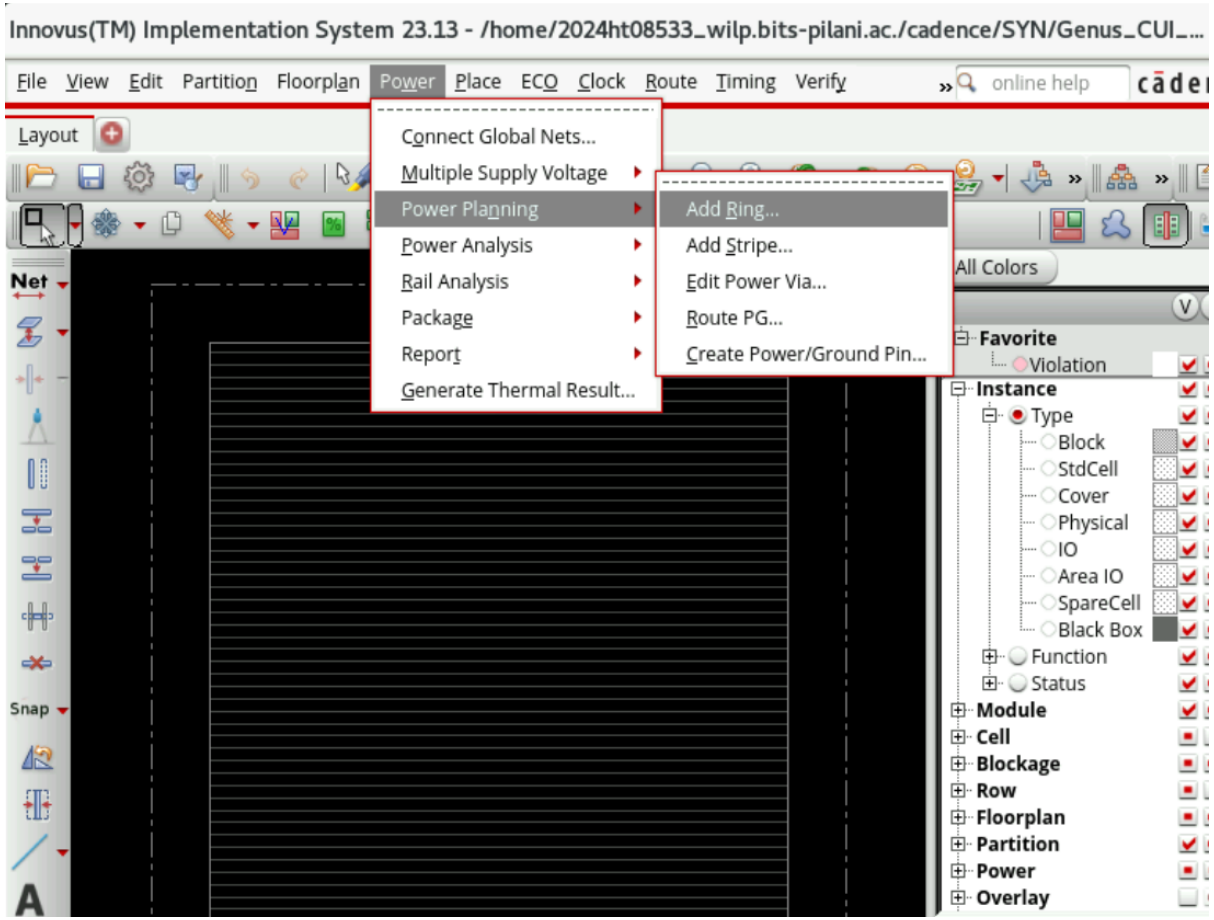



n System 23.13 - /home/2024ht08533_wilp.b
orplan
Power
Place
ECO
Clock
Route
Timin
Connect Global Nets...
Multiple Supply Voltage
Power Planning
Power Analysis
Rail Analysis
Package
Report
Generate Thermal Result...

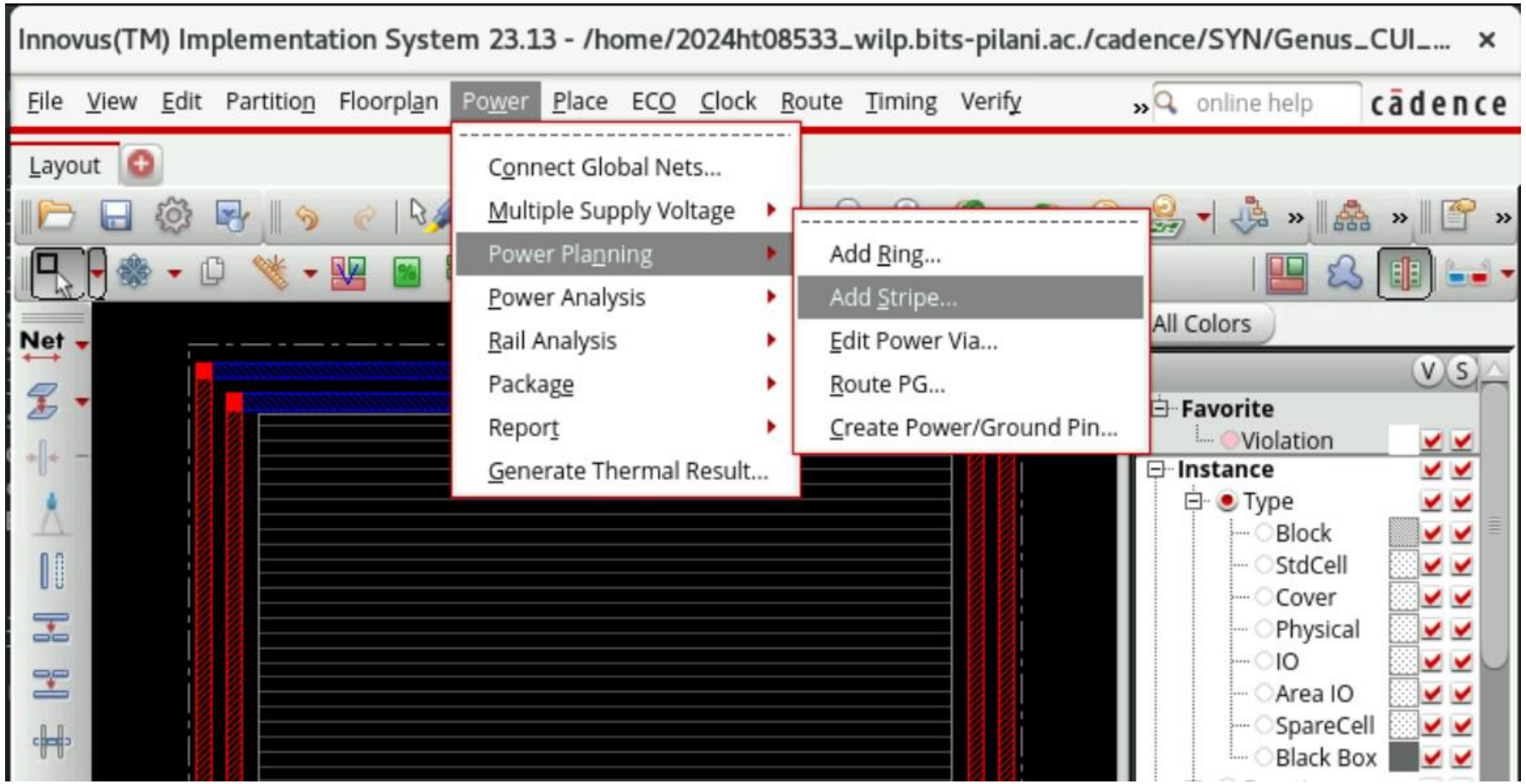
VDD and VSS to be added separately



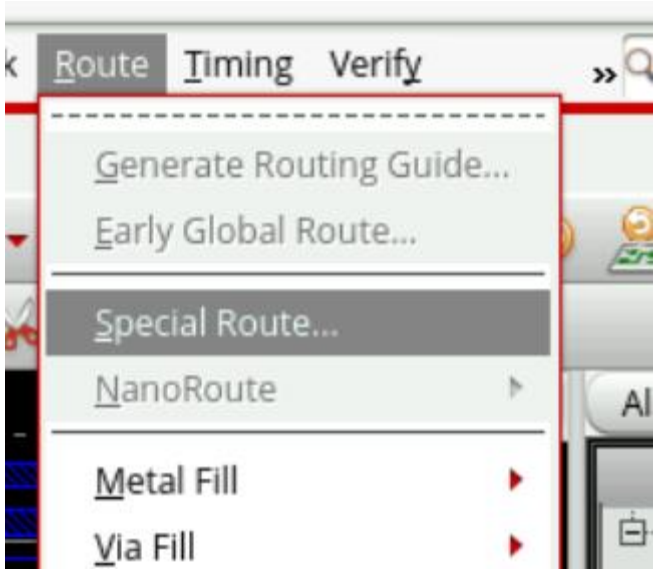
Add net VSS VDD rest leave as is

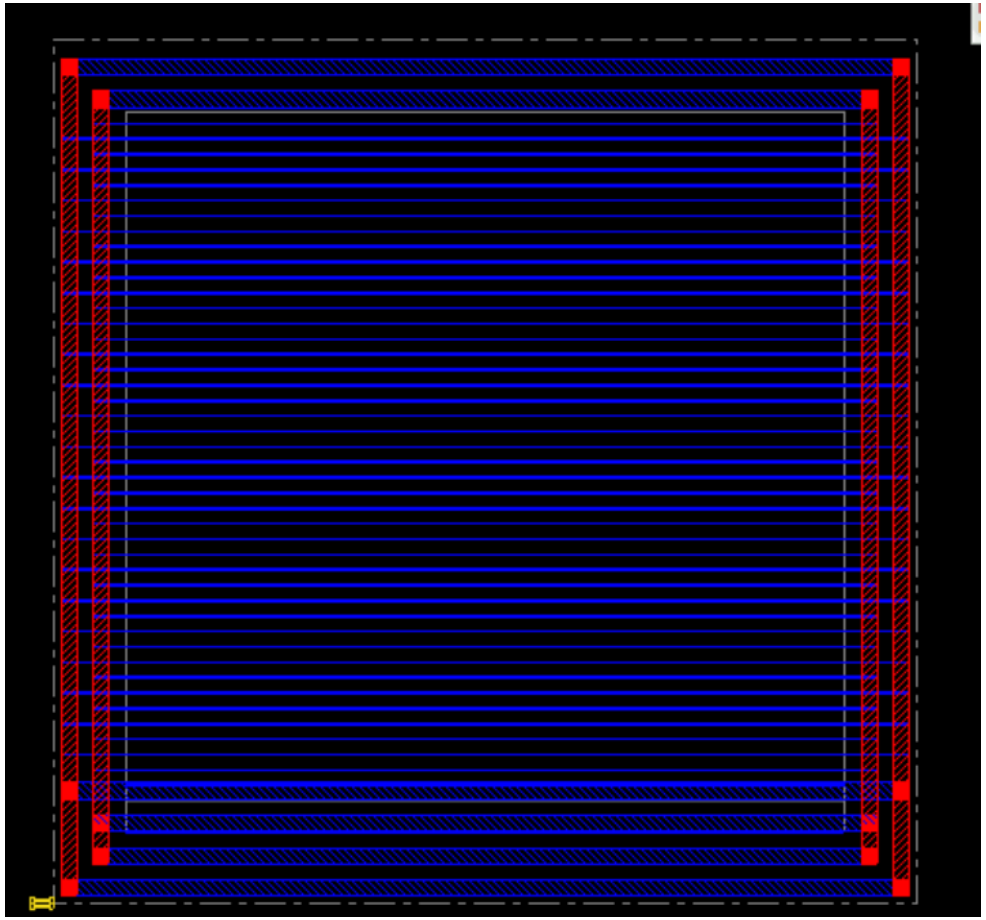


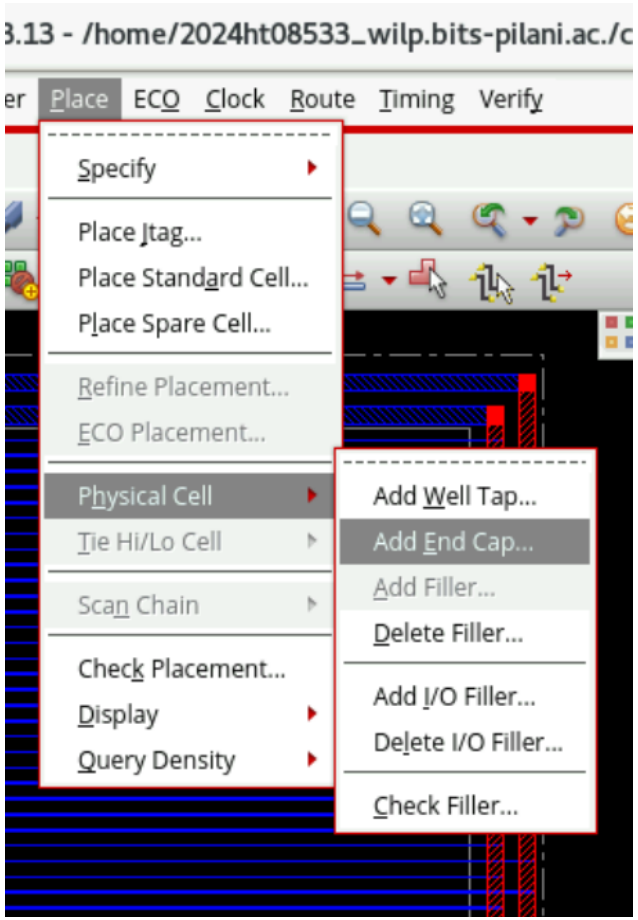
Add net VSS VDD rest leave as is

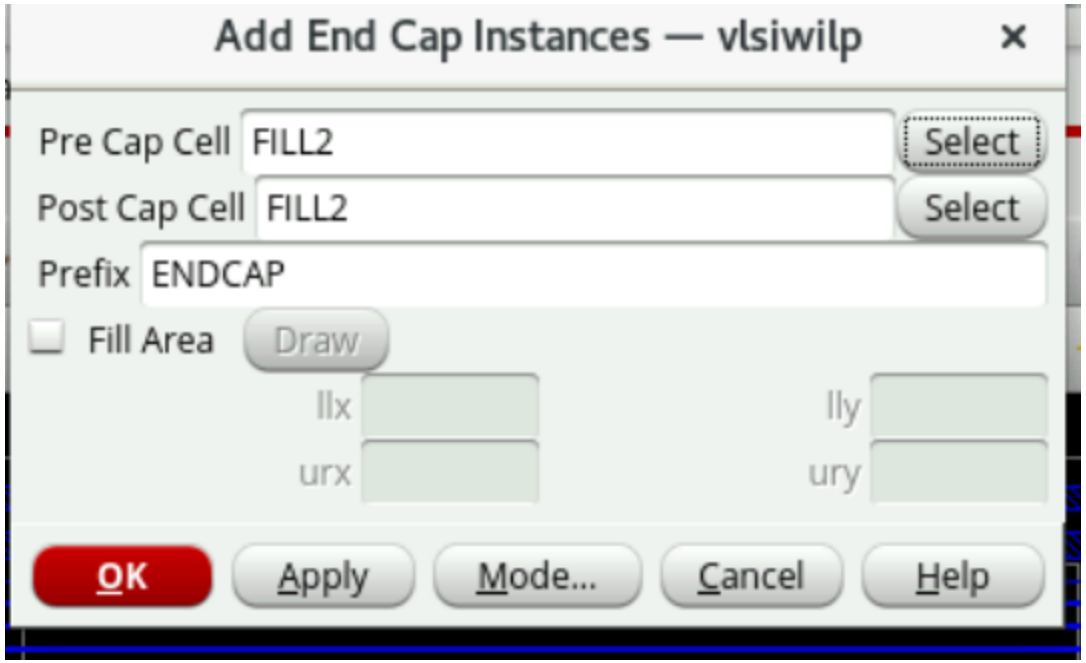


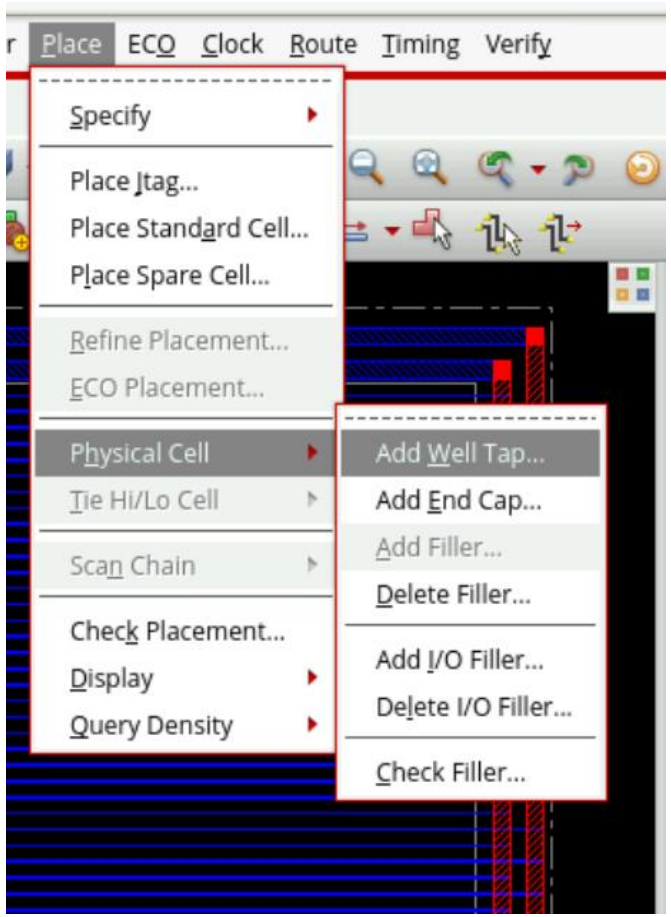
Add net VSS VDD rest leave as is

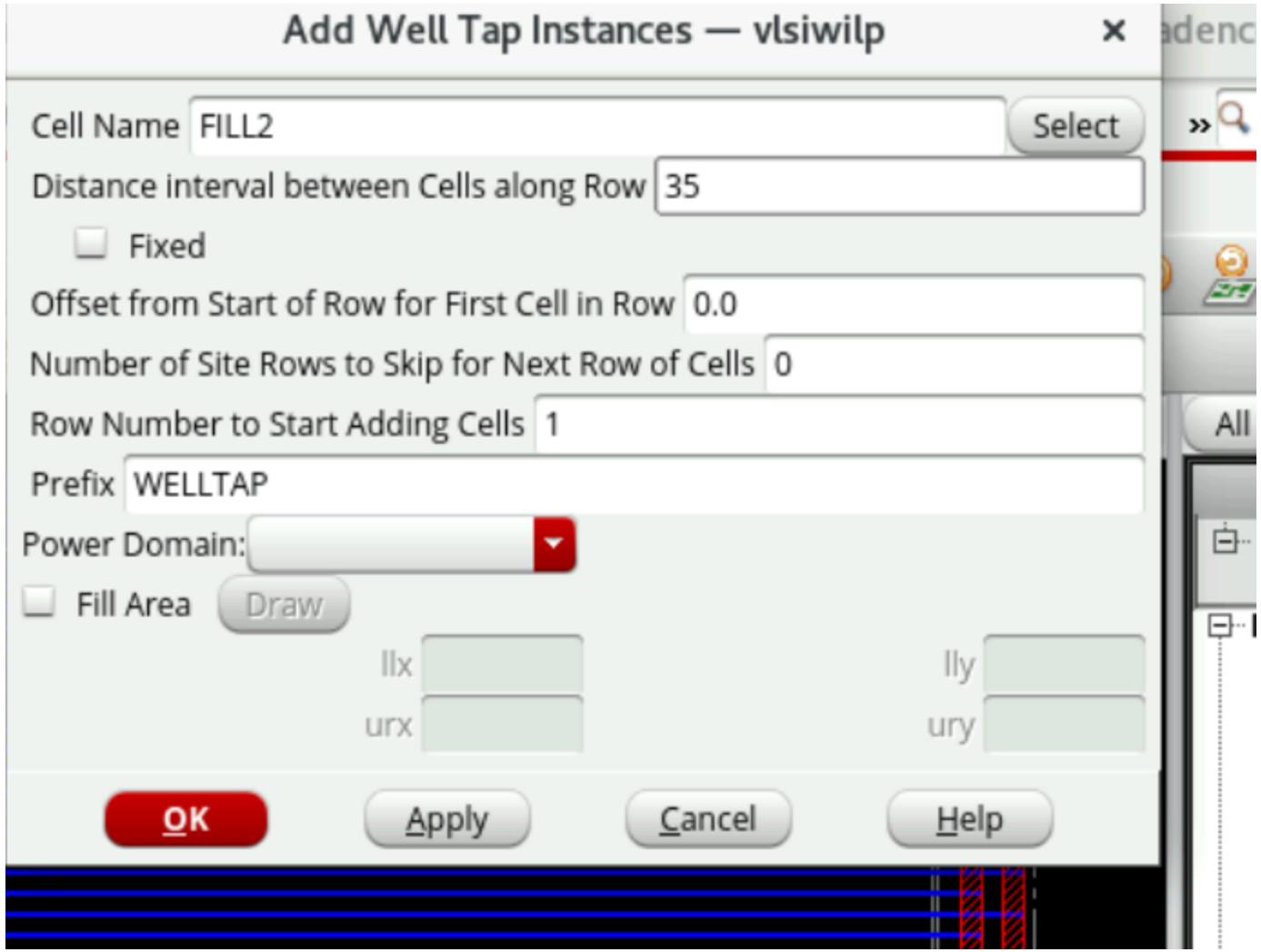


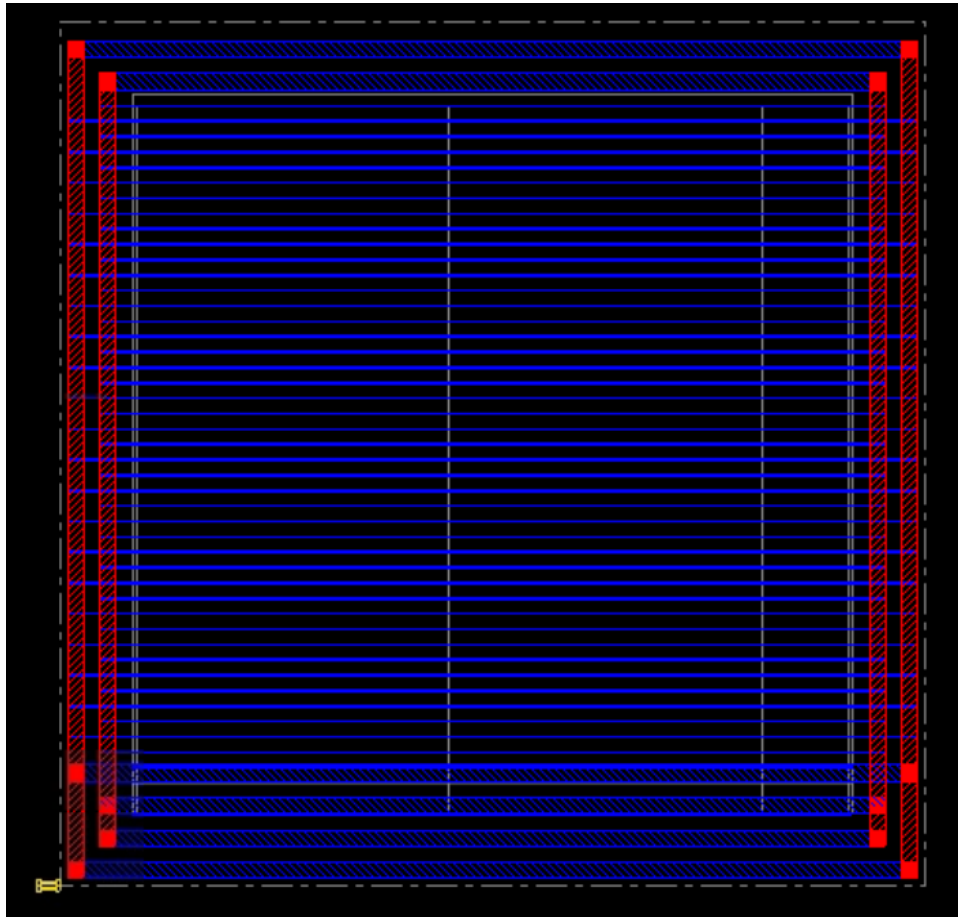


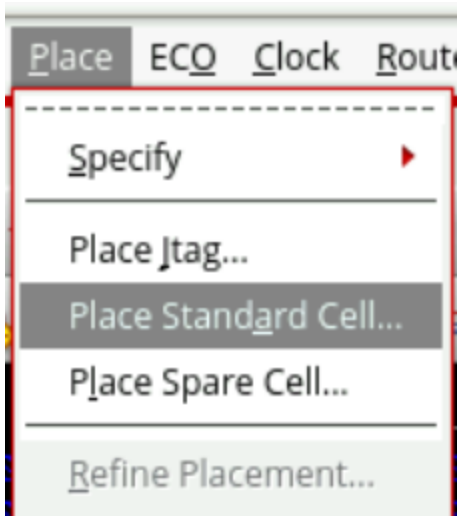

3.13 - /home/2024ht08533_wilp.bits-pilani.ac./c
er
Place
ECO
Clock
Route
Timing
Verify
Specify
Place Jtag...
Place Standard Cell...
Place Spare Cell...
Refine Placement...
ECO Placement...
Physical Cell
Tie Hi/Lo Cell
Scan Chain
Check Placement...
Display
Query Density
Add Well Tap...
Add End Cap...
Add Filler...
Delete Filler...
Add I/O Filler...
Delete I/O Filler...
Check Filler...

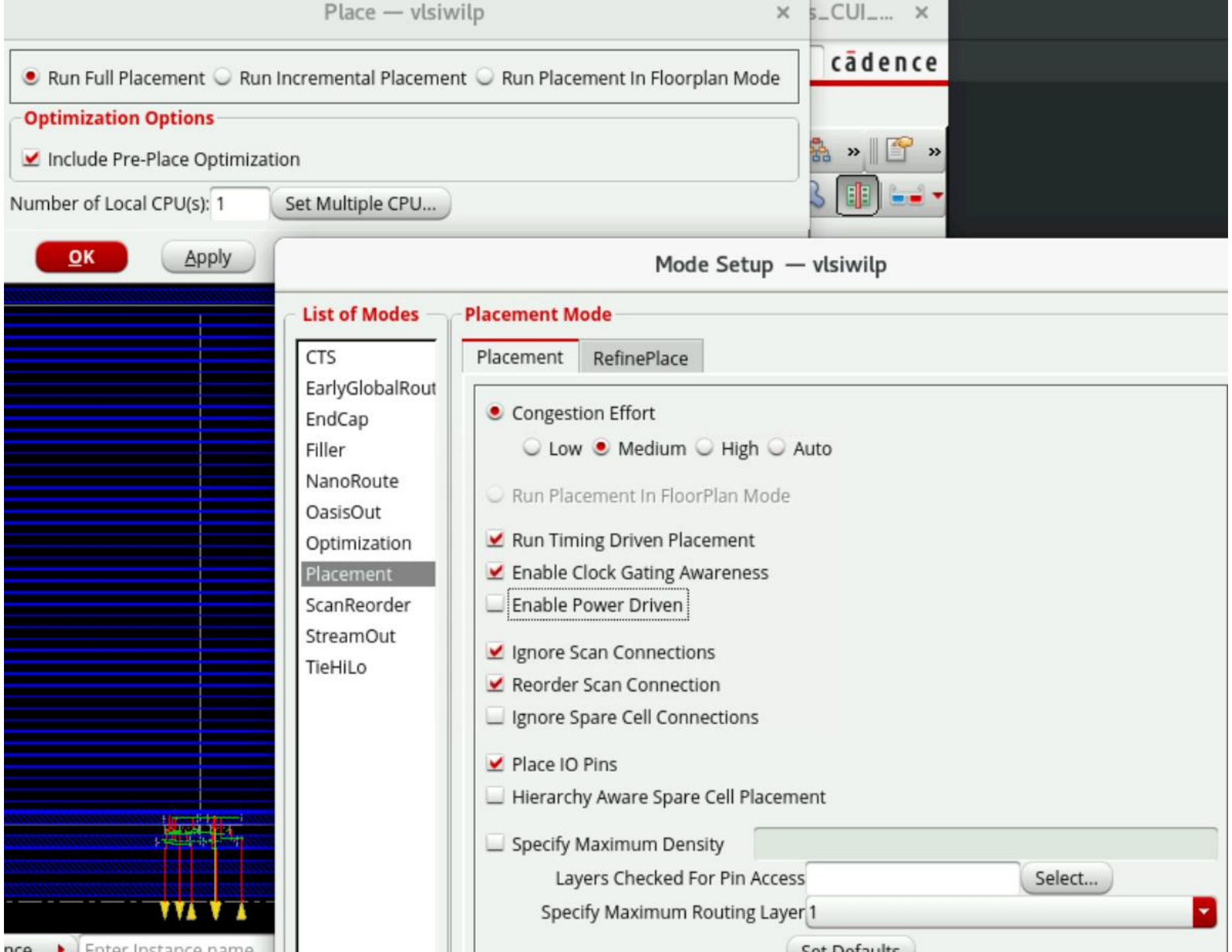

Add End Cap Instances — vlsiwilp
Pre Cap Cell
FILL2
Select
Post Cap Cell
FILL2
Select
Prefix
ENDCAP
Fill Area
Draw
llx
lly
urx
ury
OK
Apply
Mode...
Cancel
Help


Place
ECO
Clock
Route
Timing
Verify
Specify
Place Jtag...
Place Standard Cell...
Place Spare Cell...
Refine Placement...
ECO Placement...
Physical Cell
Tie Hi/Lo Cell
Scan Chain
Check Placement...
Display
Query Density
Add Well Tap...
Add End Cap...
Add Filler...
Delete Filler...
Add I/O Filler...
Delete I/O Filler...
Check Filler...

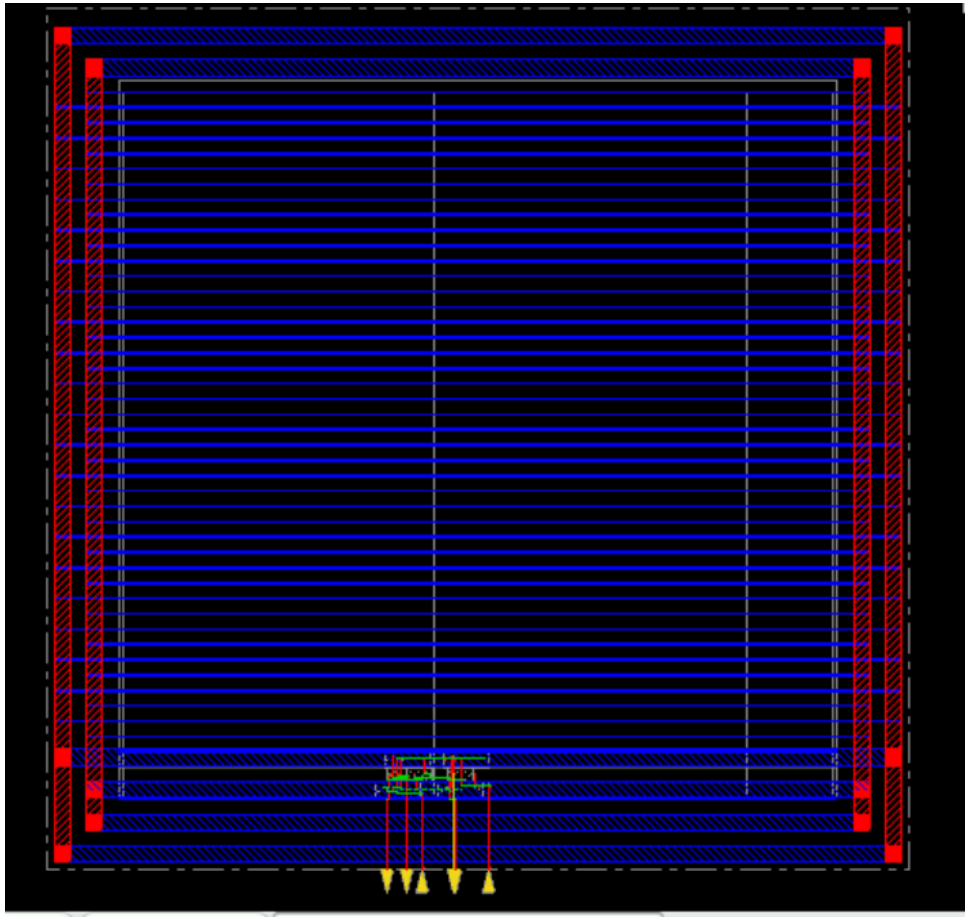

Add Well Tap Instances — vlsiwilp
Cell Name
FILL2
Select
Distance interval between Cells along Row
35
Fixed
Offset from Start of Row for First Cell in Row
0.0
Number of Site Rows to Skip for Next Row of Cells
0
Row Number to Start Adding Cells
1
Prefix
WELLTAP
Power Domain:
Fill Area
Draw
llx
lly
urx
ury
OK
Apply
Cancel
Help
All



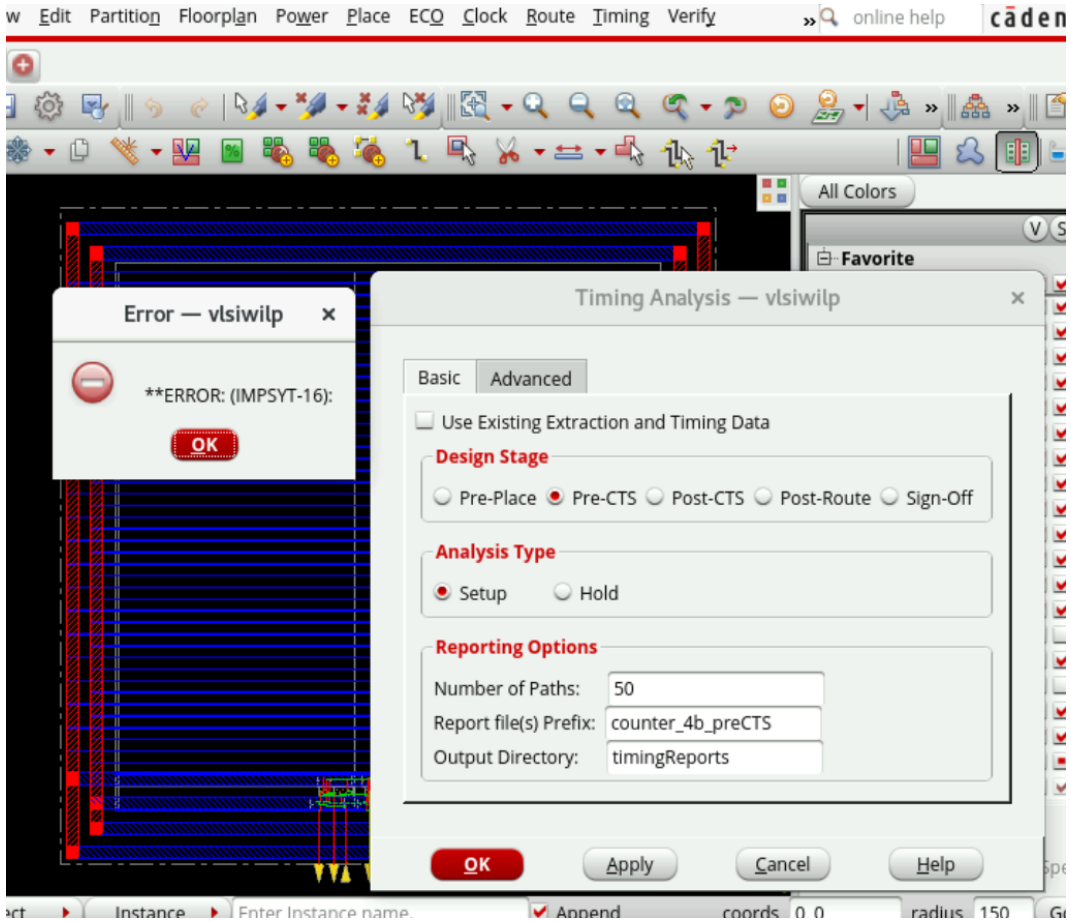

Place
ECO
Clock
Specify
Place Jtag...
Place Standard Cell...
Place Spare Cell...
Refine Placement...


Place — vlsiwilp
Run Full Placement
Run Incremental Placement
Run Placement In Floorplan Mode
Optimization Options
Include Pre-Place Optimization
Number of Local CPU(s): 1
Set Multiple CPU...
OK
Apply
cadence
Mode Setup — vlsiwilp
List of Modes
CTS
EarlyGlobalRout
EndCap
Filler
NanoRoute
OasisOut
Optimization
Placement
ScanReorder
StreamOut
TieHiLo
Placement Mode
Placement
RefinePlace
Congestion Effort
Low
Medium
High
Auto
Run Placement In FloorPlan Mode
Run Timing Driven Placement
Enable Clock Gating Awareness
Enable Power Driven
Ignore Scan Connections
Reorder Scan Connection
Ignore Spare Cell Connections
Place IO Pins
Hierarchy Aware Spare Cell Placement
Specify Maximum Density
Layers Checked For Pin Access
Select...
Specify Maximum Routing Layer 1

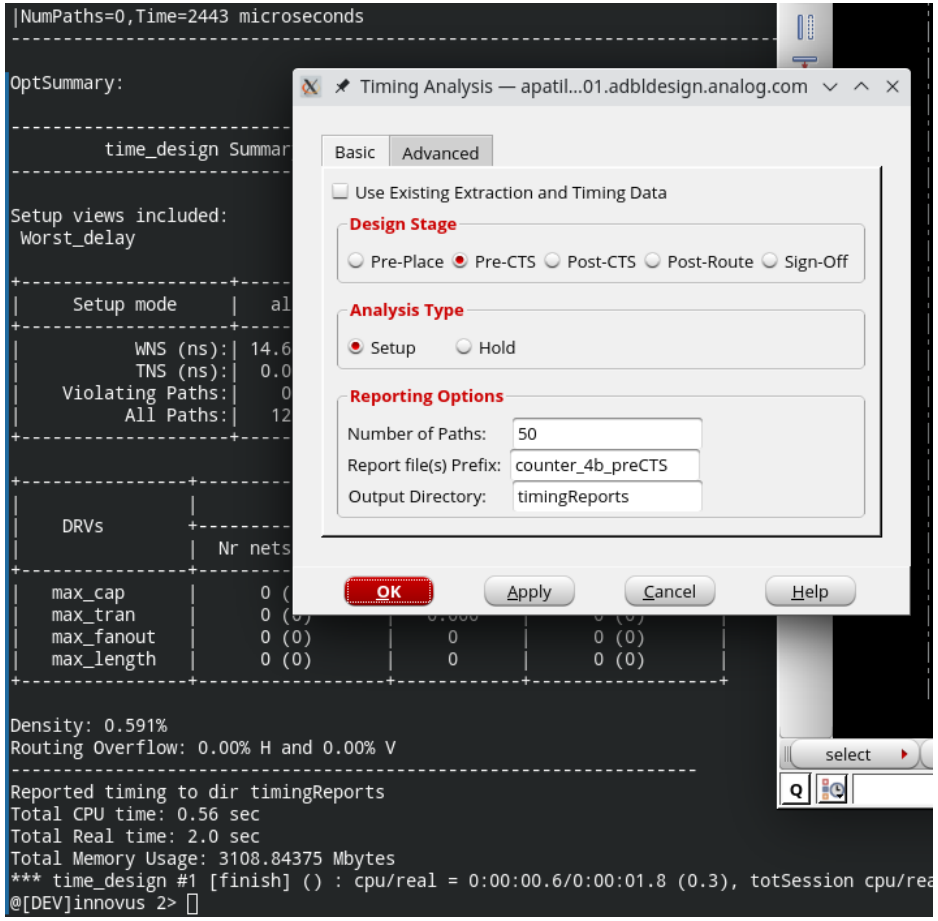
Zoom in and out you will see small ckt



Timing report_timing =pre_cts

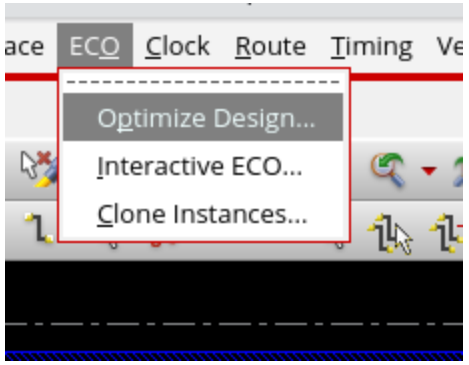


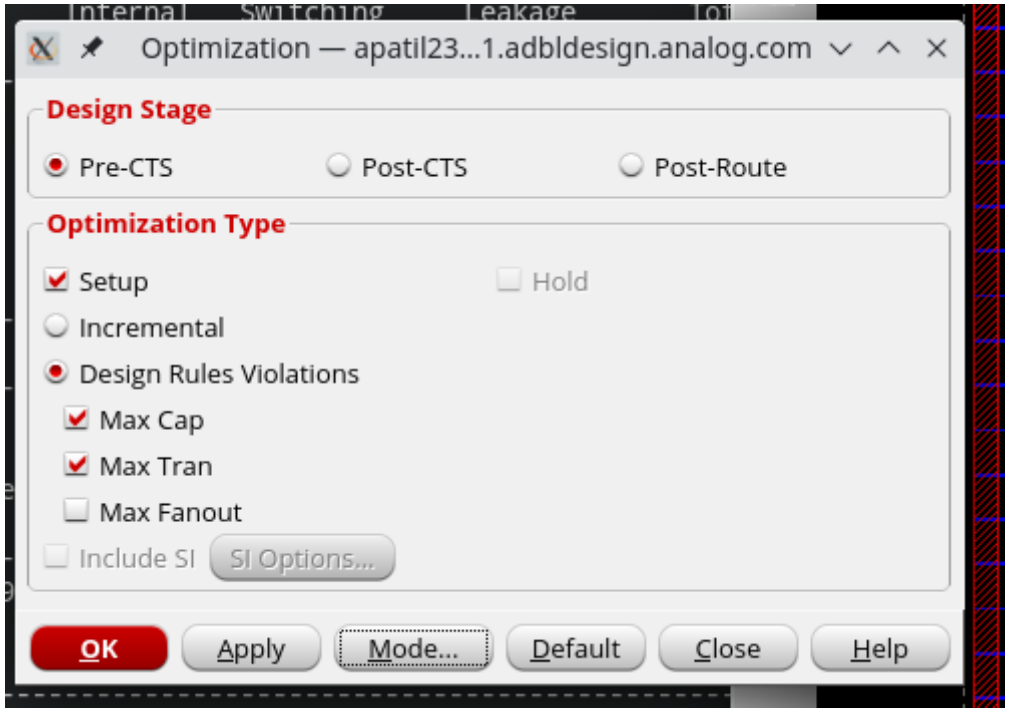
Timing –report_timing –pre_cts works



- On innovus command prompt type
- Cmd> report_area
- Cmd>report_power

Otimization – this will run for some time – just wait





Copy this on innovus_command line – does not work still

- create_route_rule -width {M1: 0.12 M2 0.14 M3 0.14 M4 0.14 M5 0.14 M6 0.14 M7 0.14 M8 0.14 M9 0.14} -spacing {M1 0.12 M2 0.14 M3 0.14 M4 0.14 M5 0.14 M6 0.14 M7 0.14 M8 0.14 M9 0.14} -name 2w2s

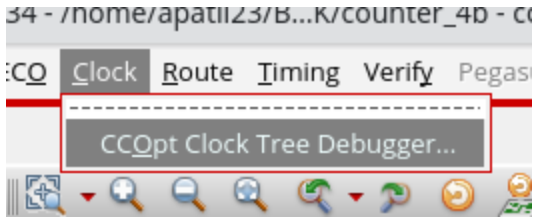
- create_route_type -name clkroute -route_rule 2w2s -bottom_preferred_layer M5 -top_preferred_layer M6
- set_ccopt_property route_type clk route -net_type trunk
- set_ccopt_property route_type clkroute -net_type leaf
- set_ccopt_property buffer_cells {CLKBUFX8 CLKBUFX12}
- set_ccopt_property inverter_cells {CLKINVX8 CLKINVX12}
- set_ccopt_property clock_gating_cells TLATNTSCA*
- create_ccopt_clock_tree_spec -file ccopt.spec

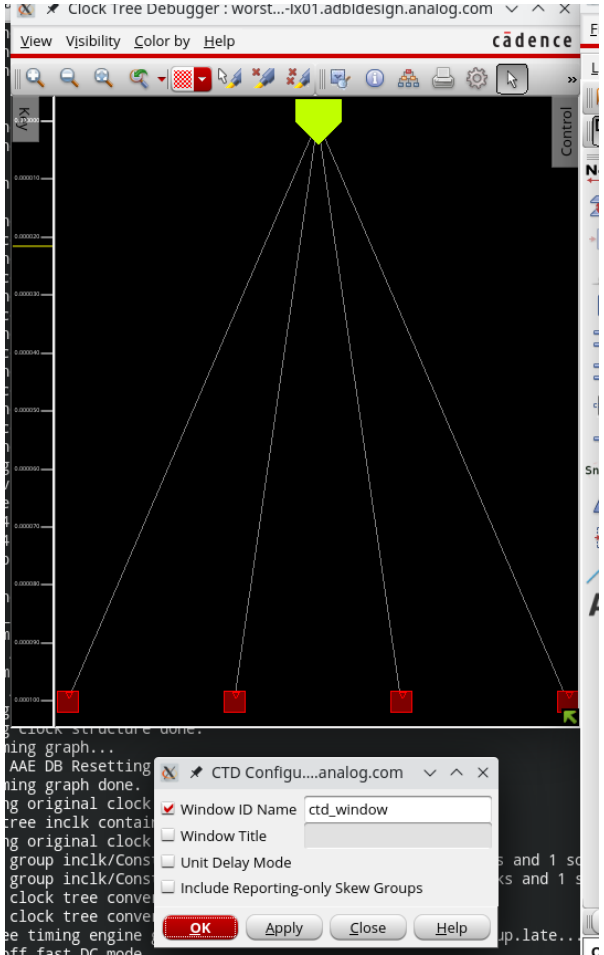
Next – does not work still for completeness sake

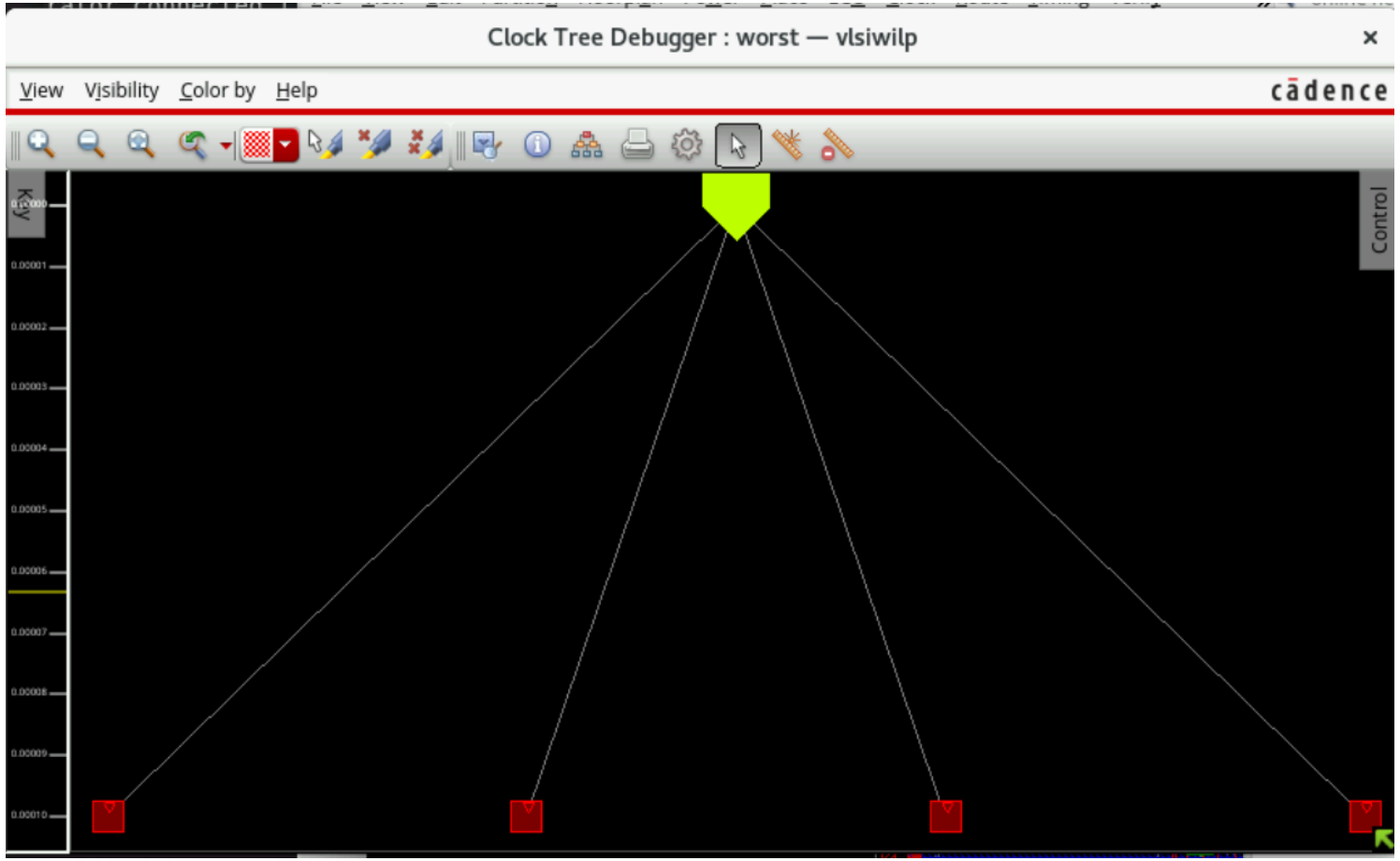
- Cmd>source ccopt.spec

Since previous setup doe not work as to use default setup

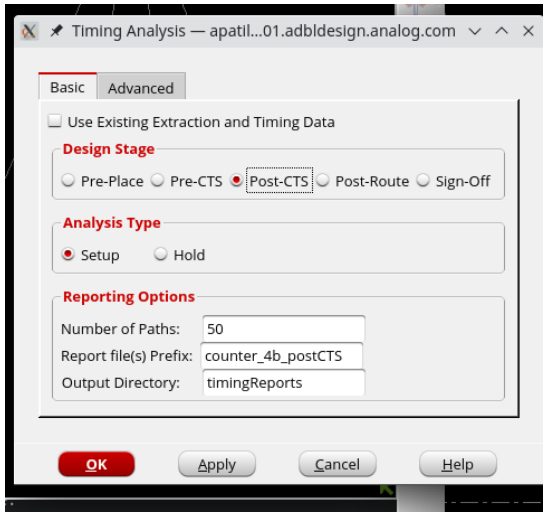
When u say okay you will see clock tree

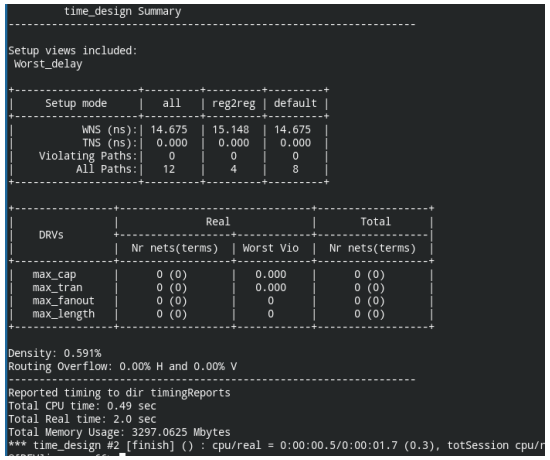


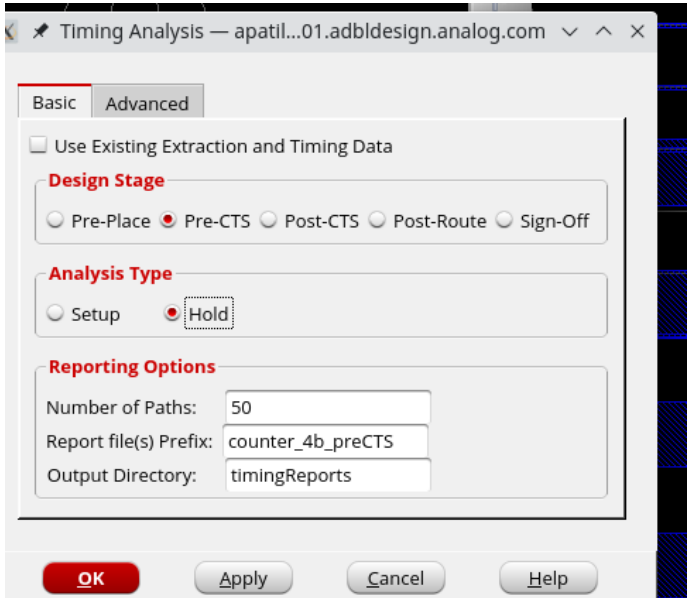


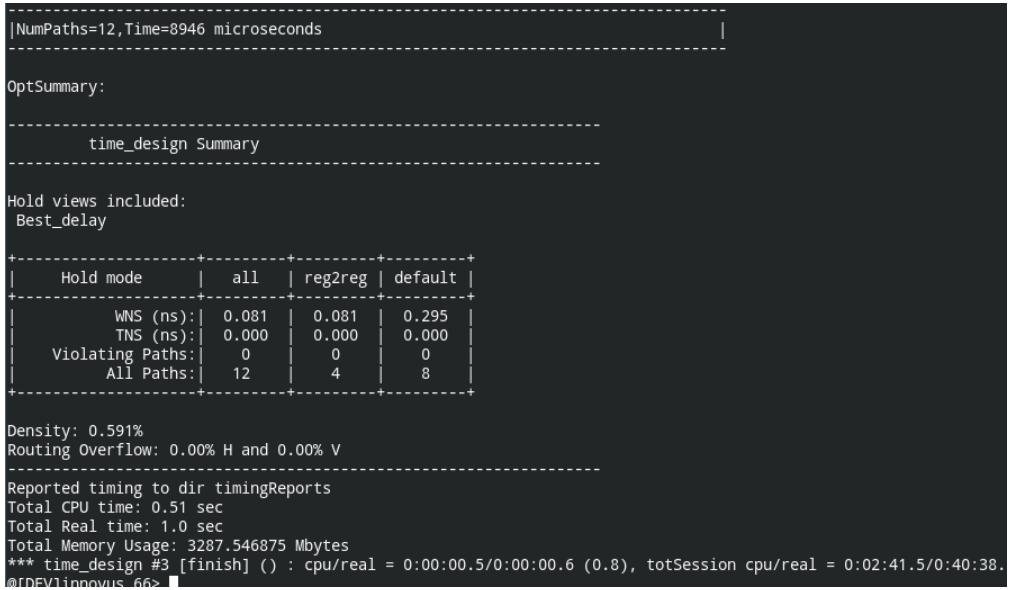

Clock Tree Debugger : worst — vlsiwilp
View
Visibility
Color by
Help
cadence
Key
Control
0.00001
0.00002
0.00003
0.00004
0.00005
0.00006
0.00007
0.00008
0.00009
0.00010

Post CTS setup and hold– you should see log



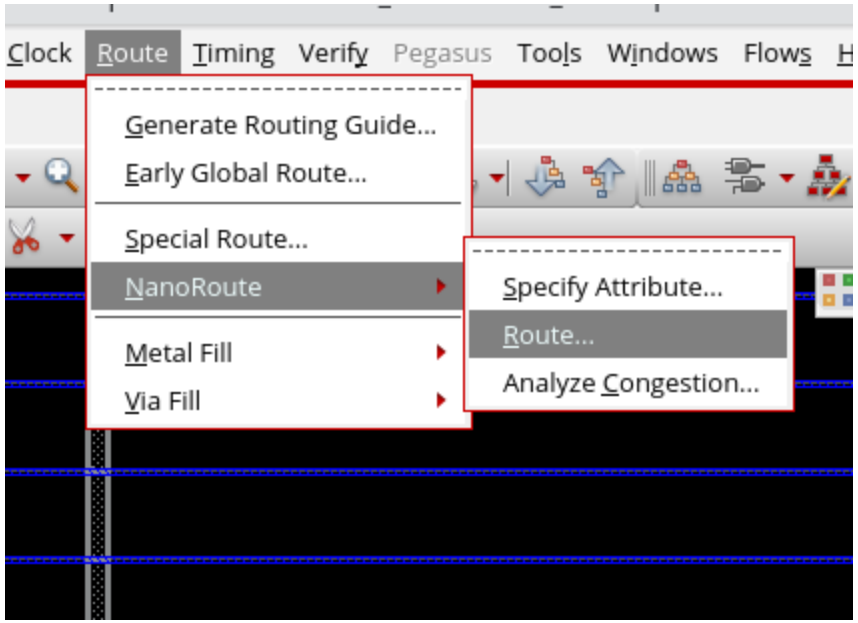


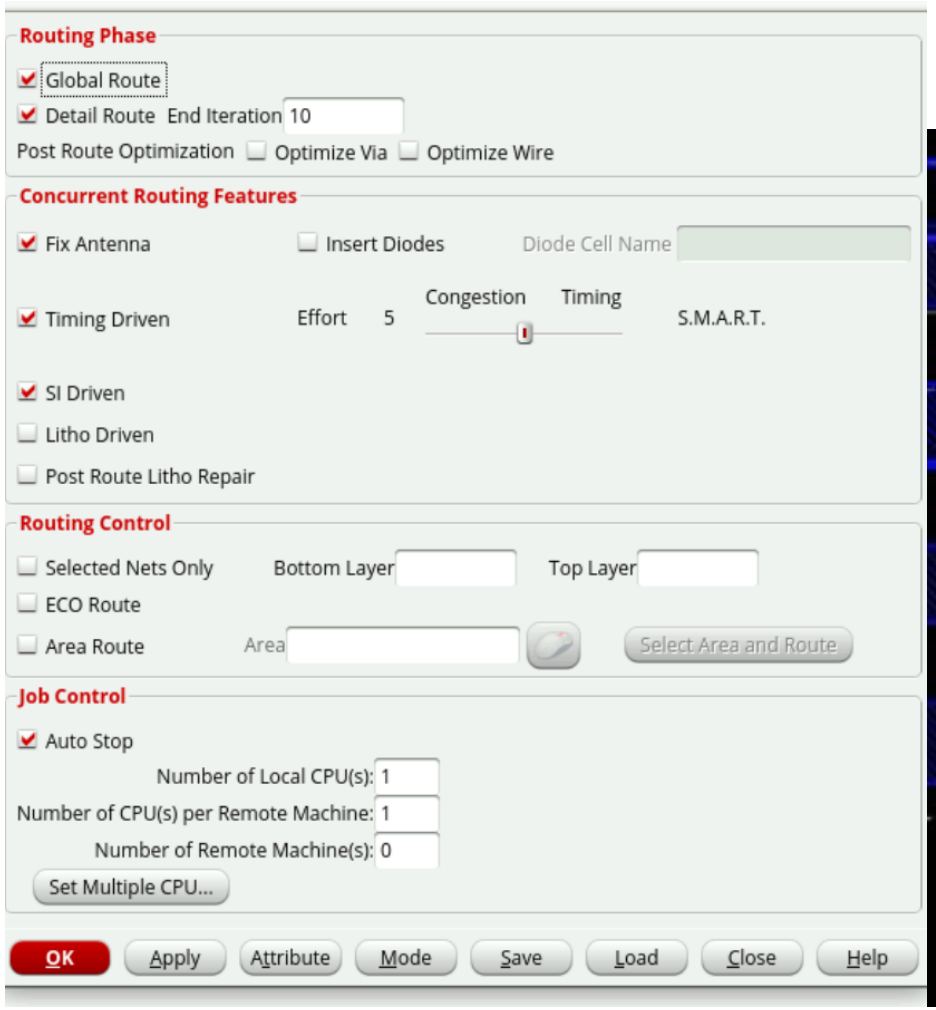


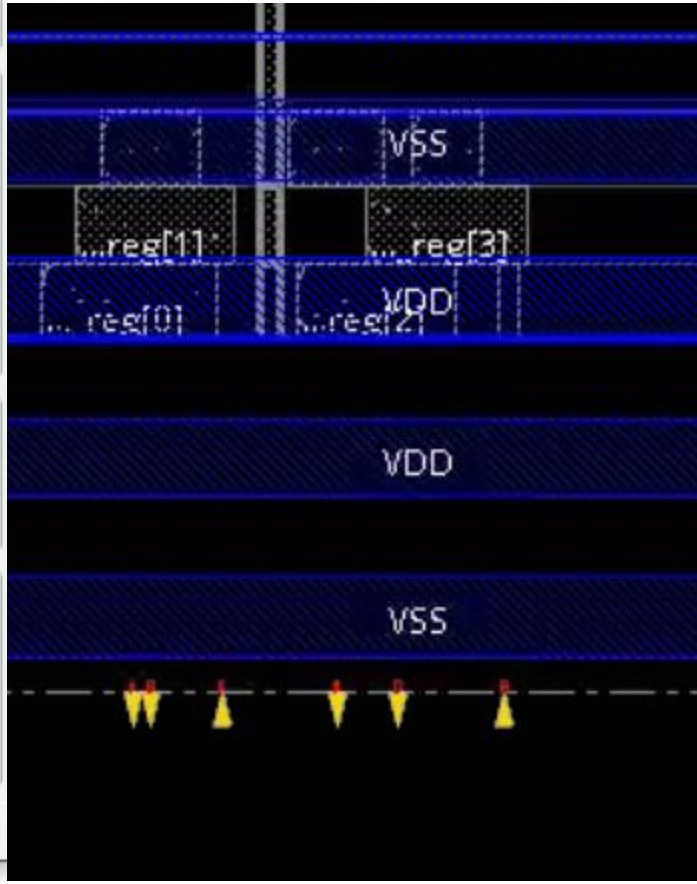


- Cmd> report_area
- Cmd>report_power

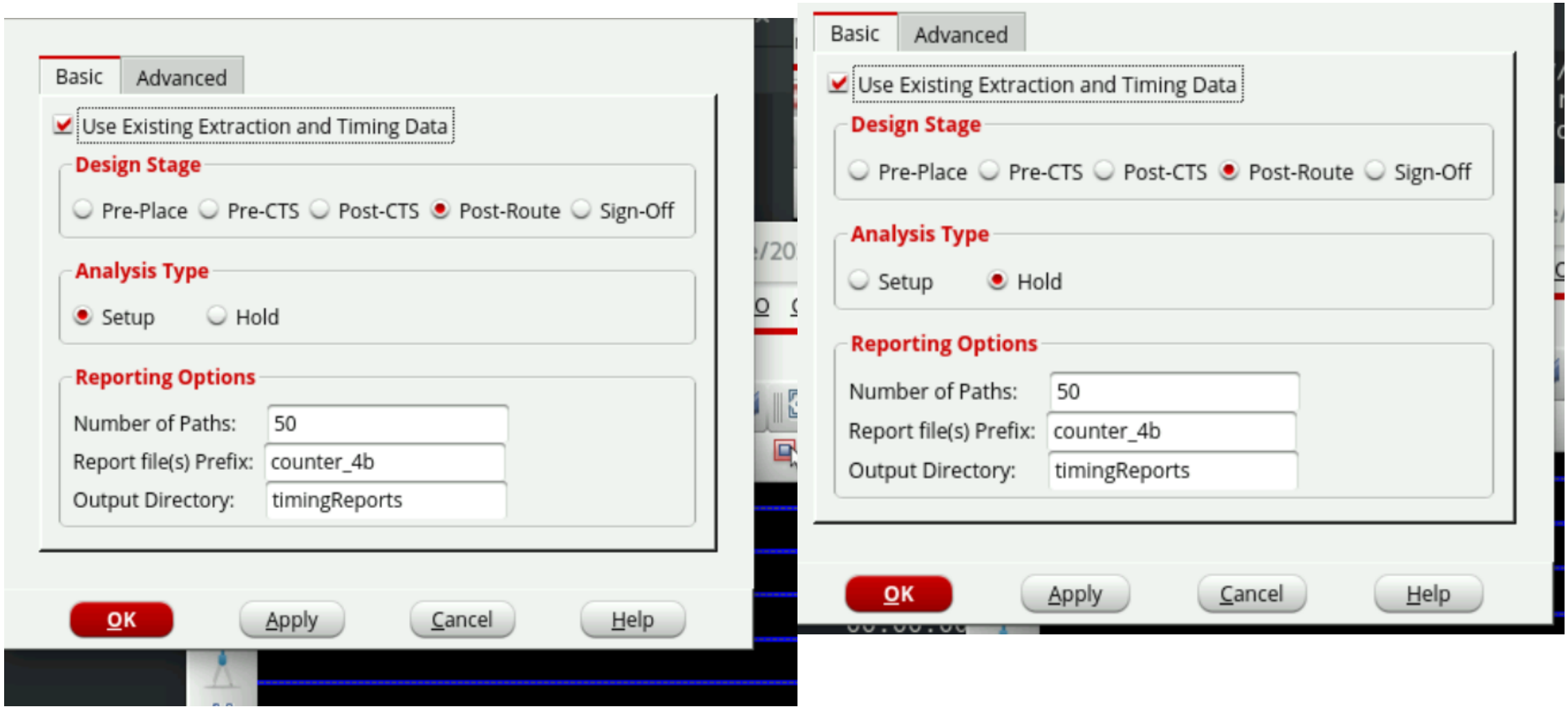
Routing optimization – will take some time for running



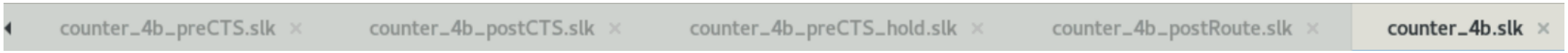




Post routing setup /hold/area /power report



Logs available



Save design and netlist & gds.. Gives some error.. Just ingoring for the time