1. **Consider existing Lab testcase design "dtmf_recvr_core" to perform following tasks, describe what was done and publish results by capturing snapshots of tool.**
    a. **Synthesis: Publish 3 worst timing paths (start and end points) in the design and respective timing slacks for Case-1 and Case-2.**
        i. **Case-1: Clocks and respective frequencies are o refclk, m_clk are of 62.5 mhz o m_rcc_clk, m_spi_clk, m_dsram_clk, m_ram_clk, m_digit_clk are of 31.25 mhz**
        ii. **Case-2: All clocks frequencies are increased by 2X (doubled).**

constraints_case1.sdc

```
create_clock -name refclk -period 16.0 [get_ports refclk]

create_clock -name m_clk -period 16.0 [get_ports m_clk]

create_clock -name m_rcc_clk -period 32.0 [get_ports m_rcc_clk]

create_clock -name m_spi_clk -period 32.0 [get_ports m_spi_clk]

create_clock -name m_dsram_clk -period 32.0 [get_ports m_dsram_clk]

create_clock -name m_ram_clk -period 32.0 [get_ports m_ram_clk]

create_clock -name m_digit_clk -period 32.0 [get_ports m_digit_clk]
```

constraints_case2.sdc

```
create_clock -name refclk -period 8.0 [get_ports refclk]

create_clock -name m_clk -period 8.0 [get_ports m_clk]

create_clock -name m_rcc_clk -period 16.0 [get_ports m_rcc_clk]

create_clock -name m_spi_clk -period 16.0 [get_ports m_spi_clk]

create_clock -name m_dsram_clk -period 16.0 [get_ports m_dsram_clk]

create_clock -name m_ram_clk -period 16.0 [get_ports m_ram_clk]

create_clock -name m_digit_clk -period 16.0 [get_ports m_digit_clk]
```

run_case1.tcl

```
# Load libraries

set_db / .library { ./LIB/slow.lib ./LIB/pll.lib ./LIB/CDK_S128x16.lib ./LIB/CDK_S256x16.lib
./LIB/CDK_R512x16.lib }

set_db / .lef_library { ./LEF/gsclib045_tech.lef ./LEF/gsclib045_macro.lef ./LEF/pll.lef
./LEF/CDK_S128x16.lef ./LEF/CDK_S256x16.lef ./LEF/CDK_R512x16.lef }
```

```
# Read HDL (explicit list)
read_hdl {
  ./RTL/pllclk.v ./RTL/accum_stat.v ./RTL/alu_32.v ./RTL/arb.v
  ./RTL/data_bus_mach.v ./RTL/data_sample_mux.v ./RTL/decode_i.v ./RTL/decoder.v
  ./RTL/digit_reg.v ./RTL/conv_subreg.v ./RTL/dma.v ./RTL/dtmf_recvr_core.v
  ./RTL/execute_i.v ./RTL/m16x16.v ./RTL/mult_32_dp.v ./RTL/port_bus_mach.v
  ./RTL/prog_bus_mach.v ./RTL/ram_128x16_test.v ./RTL/ram_256x16_test.v
  ./RTL/results_conv.v ./RTL/spi.v ./RTL/tdsp_core_glue.v ./RTL/tdsp_core_mach.v
  ./RTL/tdsp_core.v ./RTL/tdsp_data_mux.v ./RTL/tdsp_ds_cs.v
  ./RTL/test_control.v ./RTL/ulaw_lin_conv.v ./RTL/power_manager.v
}

# Elaborate the design with top-level module name
elaborate dtmf_recvr_core
check_design -unresolved

# Read constraints for Case-1
read_sdc constraints_case1.sdc

# Synthesis flow
set_db syn_generic_effort medium
syn_generic

set_db syn_map_effort medium
set_db syn_opt_effort medium
syn_map
syn_opt

# Outputs
write_hdl > design_syn_case1.v
```

write_sdc > design_syn_case1.sdc

report_timing -max_paths 3 > top3paths_case1.rpt

run_case2.tcl

Load libraries

set_db / .library { ./LIB/slow.lib ./LIB/pll.lib ./LIB/CDK_S128x16.lib ./LIB/CDK_S256x16.lib ./LIB/CDK_R512x16.lib }

set_db / .lef_library { ./LEF/gsclib045_tech.lef ./LEF/gsclib045_macro.lef ./LEF/pll.lef ./LEF/CDK_S128x16.lef ./LEF/CDK_S256x16.lef ./LEF/CDK_R512x16.lef }

Read HDL (explicit list)

read_hdl {

./RTL/pllclk.v ./RTL/accum_stat.v ./RTL/alu_32.v ./RTL/arb.v

./RTL/data_bus_mach.v ./RTL/data_sample_mux.v ./RTL/decode_i.v ./RTL/decoder.v

./RTL/digit_reg.v ./RTL/conv_subreg.v ./RTL/dma.v ./RTL/dtmf_recvr_core.v

./RTL/execute_i.v ./RTL/m16x16.v ./RTL/mult_32_dp.v ./RTL/port_bus_mach.v

./RTL/prog_bus_mach.v ./RTL/ram_128x16_test.v ./RTL/ram_256x16_test.v

./RTL/results_conv.v ./RTL/spi.v ./RTL/tdsp_core_glue.v ./RTL/tdsp_core_mach.v

./RTL/tdsp_core.v ./RTL/tdsp_data_mux.v ./RTL/tdsp_ds_cs.v

./RTL/test_control.v ./RTL/ulaw_lin_conv.v ./RTL/power_manager.v

}

Elaborate the design with top-level module name

elaborate dtmf_recvr_core

check_design -unresolved

Read constraints for Case-1

read_sdc constraints_case2.sdc

Synthesis flow

set_db syn_generic_effort medium

syn_generic

```
set_db syn_map_effort medium
set_db syn_opt_effort medium
syn_map
syn_opt

# Outputs
write_hdl > design_syn_case1.v
write_sdc > design_syn_case1.sdc
report_timing -max_paths 3 > top3paths_case2.rpt
```

top3paths_case1.rpt

```
============================================================
 Generated by:         Genus(TM) Synthesis Solution 23.13-s073_1
 Generated on:         May 10 2025  10:25:46 am
 Module:               dtmf_recvr_core
 Operating conditions:   slow
 Interconnect mode:      global
 Area mode:            physical library
============================================================


Path 1: MET (771 ps) Setup Check with Pin TDSP_CORE_INST_EXECUTE_INST_acc_reg[15]/CK->D
       Group: refclk
  Startpoint: (R) TDSP_CORE_INST_EXECUTE_INST_sel_op_b_reg[0]/CK
       Clock: (R) refclk
    Endpoint: (F) TDSP_CORE_INST_EXECUTE_INST_acc_reg[15]/D
       Clock: (R) refclk
```

	Capture	Launch
Clock Edge:+	16000	0
Src Latency:+	0	0
Net Latency:+	0 (I)	0 (I)
Arrival:=	16000	0

Setup:-	322
Required Time:=	15678
Launch Clock:-	0
Data Path:-	14907
Slack:=	771

#---

Timing Point Flags Arc Edge Cell Fanout Load Trans Delay Arrival Instance

(fF) (ps) (ps) (ps) Location

#---

TDSP_CORE_INST_EXECUTE_INST_sel_op_b_reg[0]/CK - - R (arrival) 256 - 0 0 0 (-,-)

TDSP_CORE_INST_EXECUTE_INST_sel_op_b_reg[0]/Q - CK->Q R SDFFRHQX1 4 12.4 203 339 339 (-,-)

g72898/Y - A->Y F INVX1 2 6.9 138 140 479 (-,-)

g72855__105935/Y - A->Y F AND2X1 33 87.8 1450 825 1304 (-,-)

g72953__2346/Y - B->Y R NOR2BX1 16 45.9 1366 1174 2478 (-,-)

g72641__5107/Y - A1N->Y R OAI2BB1X1 1 4.5 130 600 3078 (-,-)

g72599__5526/Y - B0->Y R AO21X1 28 80.0 1188 679 3756 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3641/Y - B->Y R XNOR2X1 1 5.8 117 549 4305 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3624/CO - CI->CO R ADDFX1 1 5.8 129 249 4554 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3623/CO - CI->CO R ADDFX1 1 5.8 128 253 4807 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3622/CO - CI->CO R ADDFX1 1 5.8 128 252 5060 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3621/CO - CI->CO R ADDFX1 1 5.8 128 252 5312 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3620/CO - CI->CO R ADDFX1 1 5.8 128 252 5565 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3619/CO - CI->CO R ADDFX1 1 5.8 128 252 5817 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3618/CO - CI->CO R ADDFX1 1 5.8 128 252 6070 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3617/CO - CI->CO R ADDFX1 1 5.8 128 252 6322 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3616/CO - CI->CO R ADDFX1 1 5.8 128 252 6575 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3615/CO - CI->CO R ADDFX1 1 5.8 128 252 6827 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3614/CO - CI->CO R ADDFX1 1 5.8 128 252 7080 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3613/CO - CI->CO R ADDFX1 1 5.8 128 252 7332 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3612/CO - CI->CO R ADDFX1 1 5.8 128 252 7585 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3611/CO - CI->CO R ADDFX1 1 5.8 128 252 7837 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3610/CO - CI->CO R ADDFX1 1 5.8 128 252 8090 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3609/CO - CI->CO R ADDFX1 1 5.8 128 252 8342 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3608/CO - CI->CO R ADDFX1 1 5.8 128 252 8595 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3607/CO - CI->CO R ADDFX1 1 5.8 128 252 8847 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3606/CO - CI->CO R ADDFX1 1 5.8 128 252 9100 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3605/CO - CI->CO R ADDFX1 1 5.8 128 252 9352 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3604/CO - CI->CO R ADDFX1 1 5.8 128 252 9605 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3603/CO - CI->CO R ADDFX1 1 5.8 128 252 9857 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3602/CO - CI->CO R ADDFX1 1 5.8 128 252 10110 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3601/CO - CI->CO R ADDFX1 1 5.8 128 252 10362 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3600/CO - CI->CO R ADDFX1 1 5.8 128 252 10615 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3599/CO - CI->CO R ADDFX1 1 5.8 128 252 10867 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3598/CO - CI->CO R ADDFX1 1 5.8 128 252 11120 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3597/CO - CI->CO R ADDFX1 1 5.8 128 252 11372 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3596/CO - CI->CO R ADDFX1 1 5.8 128 252 11625 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3595/CO - CI->CO R ADDFX1 1 5.8 128 252 11877 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3594/CO - CI->CO R ADDFX1 1 5.0 116 246 12124 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3593/Y - B->Y F XNOR2X1 1 4.8 107 197 12321 (-,-)

g103040__5107/Y - C1->Y R AOI222X1 2 7.8 453 260 12581 (-,-)

g103033__1666/Y - B->Y F NOR2X1 3 9.9 382 263 12844 (-,-)

g103023__1881/Y - A1->Y F OA21X1 31 88.1 1461 954 13798 (-,-)

g102980__5526/Y - B1->Y R AOI222X1 1 4.5 430 624 14422 (-,-)

g102911__6417/Y - D->Y F NAND4XL 1 4.7 1127 485 14907 (-,-)

TDSP_CORE_INST_EXECUTE_INST_acc_reg[15]/D - - F DFFRHQX1 1 - - 0 14907 (-,-)

#---

Path 2: MET (825 ps) Setup Check with Pin TDSP_CORE_INST_EXECUTE_INST_acc_reg[0]/CK->D

Group: refclk

Startpoint: (R) TDSP_CORE_INST_EXECUTE_INST_sel_op_b_reg[0]/CK

Clock: (R) refclk

Endpoint: (F) TDSP_CORE_INST_EXECUTE_INST_acc_reg[0]/D

Clock: (R) refclk

	Capture	Launch
Clock Edge:+	16000	0
Src Latency:+	0	0
Net Latency:+	0 (I)	0 (I)
Arrival:=	16000	0

Setup:-	322
Required Time:=	15678
Launch Clock:-	0
Data Path:-	14852
Slack:=	825

#---

# Timing Point	Flags	Arc	Edge	Cell	Fanout	Load	Trans	Delay	Arrival	Instance
#						(fF)	(ps)	(ps)	(ps)	Location
TDSP_CORE_INST_EXECUTE_INST_sel_op_b_reg[0]/CK	-	-	R	(arrival)	256	-	0	0	0	(-,-)
TDSP_CORE_INST_EXECUTE_INST_sel_op_b_reg[0]/Q	-	CK->Q	R	SDFFRHQX1	4	12.4	203	339	339	(-,-)
g72898/Y	-	A->Y	F	INVX1	2	6.9	138	140	479	(-,-)

g72855__105935/Y - A->Y F AND2X1 33 87.8 1450 825 1304 (-,-)

g72953__2346/Y - B->Y R NOR2BX1 16 45.9 1366 1174 2478 (-,-)

g72641__5107/Y - A1N->Y R OAI2BB1X1 1 4.5 130 600 3078 (-,-)

g72599__5526/Y - B0->Y R AO21X1 28 80.0 1188 679 3756 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3641/Y - B->Y R XNOR2X1 1 5.8 117 549 4305 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3624/CO - CI->CO R ADDFX1 1 5.8 129 249 4554 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3623/CO - CI->CO R ADDFX1 1 5.8 128 253 4807 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3622/CO - CI->CO R ADDFX1 1 5.8 128 252 5060 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3621/CO - CI->CO R ADDFX1 1 5.8 128 252 5312 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3620/CO - CI->CO R ADDFX1 1 5.8 128 252 5565 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3619/CO - CI->CO R ADDFX1 1 5.8 128 252 5817 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3618/CO - CI->CO R ADDFX1 1 5.8 128 252 6070 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3617/CO - CI->CO R ADDFX1 1 5.8 128 252 6322 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3616/CO - CI->CO R ADDFX1 1 5.8 128 252 6575 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3615/CO - CI->CO R ADDFX1 1 5.8 128 252 6827 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3614/CO - CI->CO R ADDFX1 1 5.8 128 252 7080 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3613/CO - CI->CO R ADDFX1 1 5.8 128 252 7332 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3612/CO - CI->CO R ADDFX1 1 5.8 128 252 7585 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3611/CO - CI->CO R ADDFX1 1 5.8 128 252 7837 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3610/CO - CI->CO R ADDFX1 1 5.8 128 252 8090 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3609/CO - CI->CO R ADDFX1 1 5.8 128 252 8342 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3608/CO - CI->CO R ADDFX1 1 5.8 128 252 8595 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3607/CO - CI->CO R ADDFX1 1 5.8 128 252 8847 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3606/CO - CI->CO R ADDFX1 1 5.8 128 252 9100 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3605/CO - CI->CO R ADDFX1 1 5.8 128 252 9352 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3604/CO - CI->CO R ADDFX1 1 5.8 128 252 9605 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3603/CO - CI->CO R ADDFX1 1 5.8 128 252 9857 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3602/CO - CI->CO R ADDFX1 1 5.8 128 252 10110 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3601/CO - CI->CO R ADDFX1 1 5.8 128 252 10362 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3600/CO - CI->CO R ADDFX1 1 5.8 128 252 10615 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3599/CO - CI->CO R ADDFX1 1 5.8 128 252 10867 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3598/CO - CI->CO R ADDFX1 1 5.8 128 252 11120 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3597/CO - CI->CO R ADDFX1 1 5.8 128 252 11372 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3596/CO - CI->CO R ADDFX1 1 5.8 128 252 11625 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3595/CO - CI->CO R ADDFX1 1 5.8 128 252 11877 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3594/CO - CI->CO R ADDFX1 1 5.0 116 246 12124 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3593/Y - B->Y F XNOR2X1 1 4.8 107 197 12321 (-,-)

g103040__5107/Y - C1->Y R AOI222X1 2 7.8 453 260 12581 (-,-)

g103033__1666/Y - B->Y F NOR2X1 3 9.9 382 263 12844 (-,-)

g103023__1881/Y - A1->Y F OA21X1 31 88.1 1461 954 13798 (-,-)

g102986__1705/Y - A1->Y R AOI22X1 1 4.5 414 575 14372 (-,-)

g102961__5115/Y - D->Y F NAND4XL 1 4.7 1127 480 14852 (-,-)

TDSP_CORE_INST_EXECUTE_INST_acc_reg[0]/D - - F DFFRHQX1
1 - - 0 14852 (-,-)

#----------

Path 3: MET (1232 ps) Setup Check with Pin TDSP_CORE_INST_EXECUTE_INST_acc_reg[8]/CK->D

Group: refclk

Startpoint: (R) TDSP_CORE_INST_EXECUTE_INST_sel_op_b_reg[0]/CK

Clock: (R) refclk

Endpoint: (F) TDSP_CORE_INST_EXECUTE_INST_acc_reg[8]/D

Clock: (R) refclk

	Capture	Launch
Clock Edge:+	16000	0
Src Latency:+	0	0
Net Latency:+	0 (I)	0 (I)
Arrival:=	16000	0

Setup:- 118

Required Time:= 15882

Launch Clock:- 0

Data Path:- 14651

Slack:= 1232

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Timing Point Flags Arc Edge Cell Fanout Load Trans Delay Arrival Instance

(fF) (ps) (ps) (ps) Location

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TDSP_CORE_INST_EXECUTE_INST_sel_op_b_reg[0]/CK - - R (arrival) 256 - 0 0 0 (-,-)

TDSP_CORE_INST_EXECUTE_INST_sel_op_b_reg[0]/Q - CK->Q R SDFFRHQX1 4 12.4 203 339 339 (-,-)

g72898/Y - A->Y F INVX1 2 6.9 138 140 479 (-,-)

g72855__105935/Y - A->Y F AND2X1 33 87.8 1450 825 1304 (-,-)

g72953__2346/Y - B->Y R NOR2BX1 16 45.9 1366 1174 2478 (-,-)

g72641__5107/Y - A1N->Y R OAI2BB1X1 1 4.5 130 600 3078 (-,-)

g72599__5526/Y - B0->Y R AO21X1 28 80.0 1188 679 3756 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3641/Y - B->Y R XNOR2X1 1 5.8 117 549 4305 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3624/CO - CI->CO R ADDFX1 1 5.8 129 249 4554 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3623/CO - CI->CO R ADDFX1 1 5.8 128 253 4807 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3622/CO - CI->CO R ADDFX1 1 5.8 128 252 5060 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3621/CO - CI->CO R ADDFX1 1 5.8 128 252 5312 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3620/CO - CI->CO R ADDFX1 1 5.8 128 252 5565 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g3619/CO - CI->CO R ADDFX1 1 5.8 128 252 5817 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3618/CO - CI->CO R ADDFX1 1 5.8 128 252 6070 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3617/CO - CI->CO R ADDFX1 1 5.8 128 252 6322 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3616/CO - CI->CO R ADDFX1 1 5.8 128 252 6575 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3615/CO - CI->CO R ADDFX1 1 5.8 128 252 6827 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3614/CO - CI->CO R ADDFX1 1 5.8 128 252 7080 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3613/CO - CI->CO R ADDFX1 1 5.8 128 252 7332 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3612/CO - CI->CO R ADDFX1 1 5.8 128 252 7585 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3611/CO - CI->CO R ADDFX1 1 5.8 128 252 7837 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3610/CO - CI->CO R ADDFX1 1 5.8 128 252 8090 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3609/CO - CI->CO R ADDFX1 1 5.8 128 252 8342 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3608/CO - CI->CO R ADDFX1 1 5.8 128 252 8595 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3607/CO - CI->CO R ADDFX1 1 5.8 128 252 8847 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3606/CO - CI->CO R ADDFX1 1 5.8 128 252 9100 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3605/CO - CI->CO R ADDFX1 1 5.8 128 252 9352 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3604/CO - CI->CO R ADDFX1 1 5.8 128 252 9605 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3603/CO - CI->CO R ADDFX1 1 5.8 128 252 9857 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3602/CO - CI->CO R ADDFX1 1 5.8 128 252 10110 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3601/CO - CI->CO R ADDFX1 1 5.8 128 252 10362 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3600/CO - CI->CO R ADDFX1 1 5.8 128 252 10615 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3599/CO - CI->CO R ADDFX1 1 5.8 128 252 10867 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3598/CO - CI->CO R ADDFX1 1 5.8 128 252 11120 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3597/CO - CI->CO R ADDFX1 1 5.8 128 252 11372 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3596/CO - CI->CO R ADDFX1 1 5.8 128 252 11625 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3595/CO - CI->CO R ADDFX1 1 5.8 128 252 11877 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3594/CO - CI->CO R ADDFX1 1 5.0 116 246 12124 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g
3593/Y - B->Y F XNOR2X1 1 4.8 107 197 12321 (-,-)

g103040__5107/Y - C1->Y R AOI222X1 2 7.8 453
260 12581 (-,-)

g103033__1666/Y - B->Y F NOR2X1 3 9.9 382 263 12844 (-,-)

g103023__1881/Y - A1->Y F OA21X1 31 88.1 1461 954 13798 (-,-)

g102994__4733/Y - A1->Y R AOI22X1 1 4.8 380 579 14377 (-,-)

g102954__2802/Y - C->Y F NAND3X1 1 4.7 364 274 14651 (-,-)

TDSP_CORE_INST_EXECUTE_INST_acc_reg[8]/D - - F DFFRHQX1 1 - - 0 14651 (-,-)

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top3paths_case2.rpt

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Generated by: Genus(TM) Synthesis Solution 23.13-s073_1

Generated on: May 10 2025 10:34:42 am

Module: dtmf_recvr_core

Operating conditions: slow

Interconnect mode: global

Area mode: physical library

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Path 1: MET (1 ps) Setup Check with Pin TDSP_CORE_INST_EXECUTE_INST_p_reg[31]/CK->D

Group: refclk

Startpoint: (R) TDSP_CORE_INST_EXECUTE_INST_sel_op_b_reg[2]/CK

Clock: (R) refclk

Endpoint: (R) TDSP_CORE_INST_EXECUTE_INST_p_reg[31]/D

Clock: (R) refclk

Capture Launch

Clock Edge:+ 8000 0

Src Latency:+ 0 0

Net Latency:+ 0 (I) 0 (I)

Arrival:= 8000 0

Setup:- 137

Required Time:= 7863

Launch Clock:- 0

Data Path:- 7862

Slack:= 1

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Timing Point Flags Arc Edge Cell Fanout Load Trans Delay Arrival Instance

(fF) (ps) (ps) (ps) Location

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TDSP_CORE_INST_EXECUTE_INST_sel_op_b_reg[2]/CK - - R (arrival) 256 - 0 0 0 (-,-)

TDSP_CORE_INST_EXECUTE_INST_sel_op_b_reg[2]/Q - CK->Q F SDFFRHQX1 4 15.9 274 366 366 (-,-)

g106202/Y - A->Y R INVX1 2 8.0 156 166 532 (-,-)

g73359__9945/Y - A->Y F NOR2X2 1 8.4 99 108 639 (-,-)

g73278__4319/Y - B->Y R NAND2X6 6 21.9 98 72 711 (-,-)

g73250/Y - A->Y F CLKINVX6 8 26.9 94 82 793 (-,-)

g73169__8246/Y - B1->Y R AOI22X4 1 10.4 195 93 886 (-,-)

g73009__3680/Y - B->Y F NAND3X8 26 78.0 527 355 1241 (-,-)

g72987__7482/Y - B->Y R NOR2X4 2 13.9 219 228 1469 (-,-)

g106282/Y - A->Y F INVX3 2 9.5 93 113 1582 (-,-)

g72946__3680/Y - A1N->Y F AOI2BB1X2 1 5.3 87 170 1752 (-,-)

g72881__9315/Y - B->Y R XOR2X4 9 33.0 171 258 2011 (-,-)

csa_tree_SUB_TC_OP_groupi_g7384/Y - A->Y F CLKINVX6 4 14.6 77 88 2098 (-,-)

csa_tree_SUB_TC_OP_groupi_g7306/Y - A1->Y R AOI22X2 2 8.0 181 132 2230 (-,-)

csa_tree_SUB_TC_OP_groupi_g7193/Y - B1->Y F OAI22X2 1 6.1 180 144 2375 (-,-)

csa_tree_SUB_TC_OP_groupi_g6989/S - CI->S R ADDFHX1 1 6.8 132 326 2700 (-,-)

csa_tree_SUB_TC_OP_groupi_g6947/CO - B->CO R ADDFHX2 1 6.0 87 231 2932 (-,-)

csa_tree_SUB_TC_OP_groupi_g6914/CO - CI->CO R ADDFHXL 2 9.3 203 254 3185 (-,-)

csa_tree_SUB_TC_OP_groupi_g6903/Y - A1->Y F AOI21X4 2 8.0 122 134 3319 (-,-)

g106176/Y - A1N->Y F AOI2BB1X4 2 7.5 70 170 3489 (-,-)

g106182/Y - A1->Y F OA21X2 3 12.4 135 200 3689 (-,-)

csa_tree_SUB_TC_OP_groupi_g6836/Y - B->Y R NOR2X4 2 9.7 108 96 3784 (-,-)

csa_tree_SUB_TC_OP_groupi_g6823/Y - B->Y F NAND2X4 1 7.0 91 85 3869 (-,-)

csa_tree_SUB_TC_OP_groupi_g6799/Y - A1->Y R AOI21X4 1 6.9 90 86 3955 (-,-)

csa_tree_SUB_TC_OP_groupi_g6797/Y - A1->Y F OAI21X4 1 7.0 100 92 4047 (-,-)

csa_tree_SUB_TC_OP_groupi_g7519/Y - B->Y R NAND2X4 3 12.7 90 69 4116 (-,-)

csa_tree_SUB_TC_OP_groupi_g7499/Y - B->Y F NAND2X4 2 8.2 99 84 4199 (-,-)

csa_tree_SUB_TC_OP_groupi_g6790/Y - B->Y R NOR2X2 1 5.5 110 89 4288 (-,-)

csa_tree_SUB_TC_OP_groupi_g6785/Y - A1->Y F OAI21X2 1 7.0 158 129 4417 (-,-)

csa_tree_SUB_TC_OP_groupi_g6783/Y - A1->Y R AOI21X4 1 6.9 93 107 4524 (-,-)

csa_tree_SUB_TC_OP_groupi_g6782/Y - B->Y F NOR2X4 2 9.5 65 64 4588 (-,-)

csa_tree_SUB_TC_OP_groupi_g6780/Y - B->Y R NOR2X4 2 8.2 91 67 4655 (-,-)

csa_tree_SUB_TC_OP_groupi_g7399/Y - B->Y F NAND2BX2 1 7.0 144 108 4763 (-,-)

csa_tree_SUB_TC_OP_groupi_g6772/Y - A1->Y R AOI21X4 1 6.9 91 102 4866 (-,-)

csa_tree_SUB_TC_OP_groupi_g6770/Y - A1->Y F OAI21X4 1 8.4 117 98 4964 (-,-)

csa_tree_SUB_TC_OP_groupi_g6769/Y - B->Y R NAND2X6 3 13.5 85 68 5032 (-,-)

csa_tree_SUB_TC_OP_groupi_g6767/Y - B->Y F NAND2X6 2 7.9 79 71 5102 (-,-)

csa_tree_SUB_TC_OP_groupi_g6762/Y - A1->Y R OAI21X2 1 4.8 113 88 5190 (-,-)

csa_tree_SUB_TC_OP_groupi_g6758/Y - A1->Y F AOI21X1 1 5.5 222 165 5355 (-,-)

csa_tree_SUB_TC_OP_groupi_g6756/Y - A1->Y R OAI21X2 1 6.1 145 145 5500 (-,-)

csa_tree_SUB_TC_OP_groupi_g6755/CO - CI->CO R ADDFHX2 1 6.1 88 224 5723 (-,-)

csa_tree_SUB_TC_OP_groupi_g6754/CO - CI->CO R ADDFHX2 1 6.1 88 204 5928 (-,-)

csa_tree_SUB_TC_OP_groupi_g6753/CO - CI->CO R ADDFHX2 1 6.1 88 204 6132 (-,-)

csa_tree_SUB_TC_OP_groupi_g6752/CO - CI->CO R ADDFHX2 1 6.1 88 204 6336 (-,-)

csa_tree_SUB_TC_OP_groupi_g6751/CO - CI->CO R ADDFHX2 1 6.4 90 206 6542 (-,-)

csa_tree_SUB_TC_OP_groupi_g6750/CO - CI->CO R ADDFHX4 1 6.0 74 201 6743 (-,-)

csa_tree_SUB_TC_OP_groupi_g6749/S - CI->S F ADDFHXL 1 5.2 141 285 7029 (-,-)

g73510__1617/Y - S0->Y F MXI2X2 2 7.4 79 258 7287 (-,-)

SUB_UNS_OP2_g769/Y - A->Y R INVX1 1 5.2 87 73 7360 (-,-)

SUB_UNS_OP2_g709/CO - A->CO R ADDHX1 1 5.0 99 171 7530 (-,-)

SUB_UNS_OP2_g708/Y - B->Y R XNOR2X1 1 4.5 95 166 7696 (-,-)

g103681__5477/Y - A1N->Y R OAI2BB1X1 1 4.7 134 165 7862 (-,-)

TDSP_CORE_INST_EXECUTE_INST_p_reg[31]/D - - R DFFRHQX1 1 - - 0 7862 (-,-)

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Path 2: MET (14 ps) Setup Check with Pin TDSP_CORE_INST_EXECUTE_INST_acc_reg[30]/CK->D

Group: refclk

Startpoint: (R) TDSP_CORE_INST_DECODE_INST_ir_reg[8]/CK

Clock: (R) refclk

Endpoint: (F) TDSP_CORE_INST_EXECUTE_INST_acc_reg[30]/D

Clock: (R) refclk

	Capture	Launch
Clock Edge:+	8000	0
Src Latency:+	0	0
Net Latency:+	0 (I)	0 (I)
Arrival:=	8000	0

Setup:-	234
Required Time:=	7766
Launch Clock:-	0
Data Path:-	7752
Slack:=	14

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Timing Point Flags Arc Edge Cell Fanout Load Trans Delay Arrival Instance

(fF) (ps) (ps) (ps) Location

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TDSP_CORE_INST_DECODE_INST_ir_reg[8]/CK - - R (arrival) 256 - 0 0 0 (-,-)

TDSP_CORE_INST_DECODE_INST_ir_reg[8]/Q - CK->Q F SDFFSHQX8 46 144.9 320 453 453 (-,-)

TDSP_CORE_INST_TDSP_CORE_GLUE_INST_sll_120_49_g1540/Y - A->Y R CLKINVX16 21 61.7 123 141 594 (-,-)

g106174/Y - B1->Y R AO22X4 2 7.8 74 176 770 (-,-)

g106154/Y - AN->Y R NOR2BX2 2 10.3 251 182 952 (-,-)

TDSP_CORE_INST_TDSP_CORE_GLUE_INST_sll_120_49_g106218/Y - B->Y F NAND2X4 2 8.2 125 138 1089 (-,-)

TDSP_CORE_INST_TDSP_CORE_GLUE_INST_sll_120_49_g1477/Y - B->Y R NOR2X2 1 7.0 164 109 1198 (-,-)

g73437__4733/Y - B->Y F NAND2X4 1 7.0 108 104 1302 (-,-)

g73421__5122/Y - B->Y R NAND2X4 5 18.5 138 82 1384 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1578/Y - S0->Y R MXI2X1 2 7.5 273 222 1606 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1492/Y - B->Y F NAND2X1 2 8.1 298 244 1850 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1435/Y - B0->Y R OAI21X2 2 8.3 165 144 1995 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1431/Y - A->Y F INVX2 1 6.9 82 98 2092 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1429/Y - A1->Y R OAI21X4 2 8.3 122 83 2176 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1428/Y - A->Y F INVX2 1 6.9 75 81 2257 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1426/Y - A1->Y R OAI21X4 3 10.8 129 90 2347 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1425/Y - A->Y F INVX2 1 6.9 76 84 2431 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1423/Y - A1->Y R OAI21X4 1 6.1 103 73 2504 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1420/CO - CI->CO R ADDFHX2 2 7.6 99 215 2719 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1418/Y - A1N->Y R OAI2BB1X4 3 11.1 126 174 2893 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1415/Y - A1->Y F AOI21X2 2 8.4 189 144 3038 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1412/Y - B->Y R NOR2X2 3 10.0 184 152 3190 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1407/Y - A1->Y R AO21X2 3 10.9 114 241 3431 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1399/Y - B1->Y F AOI221X2 2 8.4 222 147 3578 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1395/Y - B->Y R NOR2X2 3 10.0 189 163 3741 (-,-)

g106166/Y - AN->Y R NOR4BBX1 1 4.5 362 328 4069 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1388/Y - B->Y R OR2X1 2 7.8 130 232 4301 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1387/Y - A->Y F INVX2 2 8.3 87 90 4391 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1380/Y - A1->Y R OAI221X2 1 5.8 179 115 4506 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1375/CO - CI->CO R ADDFX1 1 5.8 128 270 4776 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1374/CO - CI->CO R ADDFX1 1 5.8 128 253 5029 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1373/CO - CI->CO R ADDFX1 1 5.8 128 253 5282 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1372/CO - CI->CO R ADDFX1 1 5.8 128 253 5534 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1371/CO - CI->CO R ADDFX1 1 5.0 116 246 5780 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1370/Y - B->Y F XNOR2X1 1 4.8 107 197 5978 (-,-)

g103651__5477/Y - A1->Y R AOI21X1 2 7.5 262 179 6157 (-,-)

g103539__3680/Y - B->Y R OR2X1 3 9.7 166 213 6369 (-,-)

g103523__2346/Y - B0->Y F OAI2BB1X1 1 4.5 178 157 6526 (-,-)

g103477__5122/Y - B->Y F AND2X2 31 87.8 736 490 7016 (-,-)

g103400__9945/Y - B->Y R NAND2X1 1 4.5 217 316 7332 (-,-)

g103209__5107/Y - D->Y F NAND4XL 1 4.7 798 421 7752 (-,-)

TDSP_CORE_INST_EXECUTE_INST_acc_reg[30]/D - - F DFFRHQX1 1 - - 0 7752 (-,-)

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Path 3: MET (14 ps) Setup Check with Pin TDSP_CORE_INST_EXECUTE_INST_acc_reg[29]/CK->D

Group: refclk

Startpoint: (R) TDSP_CORE_INST_DECODE_INST_ir_reg[8]/CK

Clock: (R) refclk

Endpoint: (F) TDSP_CORE_INST_EXECUTE_INST_acc_reg[29]/D

Clock: (R) refclk

	Capture	Launch
Clock Edge:+	8000	0
Src Latency:+	0	0
Net Latency:+	0 (I)	0 (I)
Arrival:=	8000	0
Setup:-	234	
Required Time:=	7766	
Launch Clock:-	0	
Data Path:-	7752	
Slack:=	14	

#---

# Timing Point	Flags	Arc	Edge	Cell	Fanout	Load	Trans	Delay	Arrival	Instance
#						(fF)	(ps)	(ps)	(ps)	Location
TDSP_CORE_INST_DECODE_INST_ir_reg[8]/CK	-	-	R	(arrival)	256	-	0	0	0	(-,-)
TDSP_CORE_INST_DECODE_INST_ir_reg[8]/Q	-	CK->Q	F	SDFFSHQX8	46	144.9	320	453	453	(-,-)
TDSP_CORE_INST_TDSP_CORE_GLUE_INST_sll_120_49_g1540/Y	-	A->Y	R	CLKINVX16	21	61.7	123	141	594	(-,-)
g106174/Y	-	B1->Y	R	AO22X4	2	7.8	74	176	770	(-,-)
g106154/Y	-	AN->Y	R	NOR2BX2	2	10.3	251	182	952	(-,-)

TDSP_CORE_INST_TDSP_CORE_GLUE_INST_sll_120_49_g106218/Y - B->Y F NAND2X4 2 8.2 125 138 1089 (-,-)

TDSP_CORE_INST_TDSP_CORE_GLUE_INST_sll_120_49_g1477/Y - B->Y R NOR2X2 1 7.0 164 109 1198 (-,-)

g73437__4733/Y - B->Y F NAND2X4 1 7.0 108 104 1302 (-,-)

g73421__5122/Y - B->Y R NAND2X4 5 18.5 138 82 1384 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1578/Y - S0->Y R MXI2X1 2 7.5 273 222 1606 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1492/Y - B->Y F NAND2X1 2 8.1 298 244 1850 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1435/Y - B0->Y R OAI21X2 2 8.3 165 144 1995 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1431/Y - A->Y F INVX2 1 6.9 82 98 2092 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1429/Y - A1->Y R OAI21X4 2 8.3 122 83 2176 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1428/Y - A->Y F INVX2 1 6.9 75 81 2257 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1426/Y - A1->Y R OAI21X4 3 10.8 129 90 2347 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1425/Y - A->Y F INVX2 1 6.9 76 84 2431 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1423/Y - A1->Y R OAI21X4 1 6.1 103 73 2504 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1420/CO - CI->CO R ADDFHX2 2 7.6 99 215 2719 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1418/Y - A1N->Y R OAI2BB1X4 3 11.1 126 174 2893 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1415/Y - A1->Y F AOI21X2 2 8.4 189 144 3038 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1412/Y - B->Y R NOR2X2 3 10.0 184 152 3190 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1407/Y - A1->Y R AO21X2 3 10.9 114 241 3431 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1399/Y - B1->Y F AOI221X2 2 8.4 222 147 3578 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1395/Y - B->Y R NOR2X2 3 10.0 189 163 3741 (-,-)

g106166/Y - AN->Y R NOR4BBX1 1 4.5 362 328 4069 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1388/Y - B->Y R OR2X1 2 7.8 130 232 4301 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1387/Y - A->Y F INVX2 2 8.3 87 90 4391 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1380/Y - A1->Y R OAI221X2 1 5.8 179 115 4506 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1375/CO - CI->CO R ADDFX1 1 5.8 128 270 4776 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1374/CO - CI->CO R ADDFX1 1 5.8 128 253 5029 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1373/CO - CI->CO R ADDFX1 1 5.8 128 253 5282 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1372/CO - CI->CO R ADDFX1 1 5.8 128 253 5534 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1371/CO - CI->CO R ADDFX1 1 5.0 116 246 5780 (-,-)

TDSP_CORE_INST_ALU_32_INST_sub_84_22_Y_TDSP_CORE_INST_ALU_32_INST_add_81_22_g1370/Y - B->Y F XNOR2X1 1 4.8 107 197 5978 (-,-)

g103651__5477/Y - A1->Y R AOI21X1 2 7.5 262 179 6157 (-,-)

g103539__3680/Y - B->Y R OR2X1 3 9.7 166 213 6369 (-,-)

g103523__2346/Y - B0->Y F OAI2BB1X1 1 4.5 178 157 6526 (-,-)

g103477__5122/Y - B->Y F AND2X2 31 87.8 736 490 7016 (-,-)

g103398__6161/Y - B->Y R NAND2X1 1 4.5 217 316 7332 (-,-)

g103215__3680/Y - D->Y F NAND4XL 1 4.7 798 421 7752 (-,-)

TDSP_CORE_INST_EXECUTE_INST_acc_reg[29]/D - - F DFFRHQX1 1 - - 0 7752 (-,-)

#---

Top-3 worst paths (summary)

Case	Slack #1	Slack #2	Slack #3	Meets timing?
1	**0.771 ns**	**0.825 ns**	**1.232 ns**	Comfortable margin
2	**0.001 ns** (1 ps)	**0.014 ns**	**0.014 ns**	Barely – borderline

b. DFT: Insert seperate scan chains for positive edge and negative edge flipflops in the design. And publish number of scan flops, number of scan chains and length of each scan chain.

run_dft.tcl

```
# ========================

# Load Libraries

# ========================

set_db / .library [list \
```

```
  ./LIB/slow.lib \
  ./LIB/pll.lib \
  ./LIB/CDK_S128x16.lib \
  ./LIB/CDK_S256x16.lib \
  ./LIB/CDK_R512x16.lib ]

set_db / .lef_library [list \
  ./LEF/gsclib045_tech.lef \
  ./LEF/gsclib045_macro.lef \
  ./LEF/pll.lef \
  ./LEF/CDK_S128x16.lef \
  ./LEF/CDK_S256x16.lef \
  ./LEF/CDK_R512x16.lef ]

# ========================
# Read Synthesizable RTL Files
# ========================
read_hdl [list \
  ./RTL/pllclk.v \
  ./RTL/accum_stat.v \
  ./RTL/alu_32.v \
  ./RTL/arb.v \
  ./RTL/data_bus_mach.v \
  ./RTL/data_sample_mux.v \
  ./RTL/decode_i.v \
  ./RTL/decoder.v \
  ./RTL/digit_reg.v \
  ./RTL/conv_subreg.v \
  ./RTL/dma.v \
  ./RTL/dtmf_recvr_core.v \
  ./RTL/execute_i.v \
```

```
 ./RTL/m16x16.v \
 ./RTL/mult_32_dp.v \
 ./RTL/port_bus_mach.v \
 ./RTL/prog_bus_mach.v \
 ./RTL/ram_128x16_test.v \
 ./RTL/ram_256x16_test.v \
 ./RTL/results_conv.v \
 ./RTL/spi.v \
 ./RTL/tdsp_core_glue.v \
 ./RTL/tdsp_core_mach.v \
 ./RTL/tdsp_core.v \
 ./RTL/tdsp_data_mux.v \
 ./RTL/tdsp_ds_cs.v \
 ./RTL/test_control.v \
 ./RTL/ulaw_lin_conv.v \
 ./RTL/power_manager.v ]

# ========================
# Elaborate and Load Constraints
# ========================
elaborate
read_sdc ./constraints/dtmf_recvr_core_gate.sdc
current_design dtmf_recvr_core

# ========================
# DFT Setup
# ========================
set_db / .dft_scan_style muxed_scan
set_db / .dft_prefix DFT_
set_db "design:dtmf_recvr_core" .dft_mix_clock_edges_in_scan_chains false
```

```
define_test_clock -name scanclk -period 18000 scan_clk
define_shift_enable -name se -active high scan_en
define_test_mode -name tm -active high test_mode
define_scan_chain -name top_chain -sdi scan_in -sdo scan_out -shift_enable se -create_ports

# --- Ensure scan FFs are inserted ---
set_db "design:dtmf_recvr_core" .dft_scan_map_mode tdrc_pass
set_db / .use_scan_seqs_for_non_dft false
set_db "design:dtmf_recvr_core" .dft_connect_shift_enable_during_mapping tie_off
set_db "design:dtmf_recvr_core" .dft_connect_scan_data_pins_during_mapping loopback

# ========================
# Synthesis
# ========================
set_db syn_generic_effort medium
syn_generic

set_db syn_map_effort medium
syn_map

set_db syn_opt_effort medium
syn_opt

# ========================
# Scan Chain Setup
# ========================
check_dft_rules -advanced
convert_to_scan
connect_scan_chains -auto_create_chains

# ========================
```

Reports and Output

========================

report_scan_chains

report_scan_registers

report_scan_setup

write_scandef dtmf_recvr_core > scan_chain.def

write_design -base_name synthesized_netlist

dft_summary

Summary:

Total registers that pass DFT rules: 517

Total registers that fail DFT rules: 0

Total registers that are marked preserved or dont-scan: 0

Total registers that are marked Abstract Segment dont-scan: 0

Total registers that are part of shift register segments: 0

Total registers that are lockup elements: 0

Total registers that are level-sensitive: 0

Total registers that are misc. non-scan: 3

Total registers that pass dft rule checks and are not a part of scan chains: 0

Total abstract segments that pass dft rule checks and are not a part of scan chains: 0

@file(run_dft.tcl) 102: report_scan_setup

Design Name

dtmf_recvr_core

Scan Style

muxed_scan

Design has a valid DFT rule check status

Global Constraints

Minimum number of scan chains: no_value

Maximum length of scan chains: no_value

Lock-up element type: preferred_level_sensitive

Mix clock edges in scan chain: false

Prefix for unnamed scan objects: DFT_

Test signal objects

shift_enable:

- object name: se
- pin name: scan_en
- hookup_pin: scan_en
- hookup_polarity: non_inverted
- function: shift_enable
- active: high
- ideal: false
- user defined: true

test_mode:

- object name: tm
- pin name: test_mode
- hookup_pin: test_mode

```
    hookup_polarity: non_inverted
    function: test_mode
    active: high
    ideal: false
    user defined: true

test_mode:
    object name: reset
    pin name: reset
    hookup_pin: reset
    hookup_polarity: non_inverted
    function: async_set_reset
    active: low
    ideal: false
    user defined: false

test_mode:
    object name: spi_fs
    pin name: spi_fs
    hookup_pin: spi_fs
    hookup_polarity: non_inverted
    function: async_set_reset
    active: low
    ideal: false
    user defined: false


# Test clock objects

test_clock:
    object name: scanclk
```

test_clock_domain: scanclk

user defined: true

source: scan_clk

root source: scan_clk

root source polarity: non_inverting

hookup_pin: scan_clk

period: 18000.0

DFT controllable objects

DFT don't scan objects

DFT abstract don't scan objects

DFT scan segment constraints

DFT scan chain constraints

User Chain:

object name: top_chain

scan-in: scan_in_1

scan-in hookup_pin: scan_in_1

scan-out: scan_out_2

scan-out hookup_pin: scan_out_2

shared out: false

shift_enable object name: se

max length: no_value

complete: false

DFT actual scan chains

Actual Chain:

object name: top_chain

scan-in: scan_in_1

scan-in hookup_pin: scan_in_1

scan-out: scan_out_2

scan-out hookup_pin: scan_out_2

shared out: false

shift_enable: scan_en

length: 129

segment objects: none

analyzed: false

test_clock domain: scanclk

test_clock edge: fall

Actual Chain:

object name: AutoChain_1

scan-in: DFT_sdi_1

scan-in hookup_pin: DFT_sdi_1

scan-out: DFT_sdo_1

scan-out hookup_pin: DFT_sdo_1

shared out: false

shift_enable: scan_en

length: 388

segment objects: none

analyzed: false

test_clock domain: scanclk

test_clock edge: rise

@file(run_dft.tcl) 104: write_scandef dtmf_recvr_core > scan_chain.def

@file(run_dft.tcl) 105: write_design -base_name synthesized_netlist

(write_design): Writing Genus content. Constraint interface is 'smsc'

Exporting design data for 'dtmf_recvr_core' to ./synthesized_netlist...

%# Begin write_design (05/10 11:44:33, mem=2002.28M)

Setting attribute of root '/': 'set_boundary_change' =

File ./synthesized_netlist.mmmc.tcl has been written.

Finished SDC export (command execution time mm\:ss (real) = 00:01).

Info: file ./synthesized_netlist.default_emulate_constraint_mode.sdc has been written

Info: file ./synthesized_netlist.default_emulate_constraint_mode.sdc has been written

** To load the database source ./synthesized_netlist.genus_setup.tcl in an Genus(TM) Synthesis Solution session.

Finished exporting design data for 'dtmf_recvr_core' (command execution time mm\:ss cpu = 00:00, real = 00:02).

.

%# End write_design (05/10 11:44:35, total cpu=03:00:00, real=03:00:02, peak res=999.20M, current mem=2004.28M)

\#@ End verbose source ./run_dft.tcl

Scan-DFT Statistics for dtmf_recvr_core

Item	**Value**
Total scan-enabled flip-flops	517
Total scan chains	2
Chain #1 (negative-edge flops)	129 FFs (clock edge = fall)
Chain #2 (positive-edge flops)	388 FFs (clock edge = rise)

Chain	**Clock edge (via report_scan_chains)**	**Length (flip-flops)**
top_chain	Falling edge of scanclk	129
AutoChain_1	Rising edge of scanclk	388

c. LEC: run flat LEC between synthesis netlist and post scan netlist. Publish results snippet.

flat_lec.tcl

```
tclmode

vpxmode


set undefined cell black_box -noascend -both

add notranslate modules \

 CDK_S256x16 \

 CDK_R512x16 \

 CDK_S128x16 \

 pll \

 -library -both


read library -statetable -liberty \

 ./LEC/libs/gsclib045_v3.5/timing/slow.lib \

 ./LEC/libs/macro_libs/pllclk_slow.lib \

 ./LEC/libs/macro_libs/CDK_S128x16.lib \

 ./LEC/libs/macro_libs/CDK_S256x16.lib \

 ./LEC/libs/macro_libs/CDK_R512x16.lib \

 -both


read design -verilog ./design_syn_case1.v -golden -lastmod

set root module dtmf_recvr_core -golden


read design -verilog ./synthesized_netlist.v -revised -lastmod

set root module dtmf_recvr_core -revised


uniquify -all -nolib
```

```
set flatten model -seq_constant -seq_constant_x_to 0
set flatten model -nodff_to_dlat_zero -nodff_to_dlat_feedback

set system mode lec

add compared points -all
compare

report compare data -class nonequivalent -class abort -class notcompared >
lec_compare_data.txt
report verification -verbose > lec_verification.txt
report statistics > lec_statistics.txt
report unmapped points -summary > lec_unmapped_summary.txt
report unmapped points -extra -unreachable -notmapped > lec_unmapped_detailed.txt

tclmode
puts "No of compare points = [get_compare_points -count]"
puts "No of diff points    = [get_compare_points -diff -count]"
puts "No of abort points   = [get_compare_points -abort -count]"
puts "No of unknown points = [get_compare_points -unknown -count]"

exit
```

Summary

```
Extra          2     2       4
================================================================================
// Command: add compared points -all
// 557 compared points added to compare list
// Command: compare
```

```
================================================================================
==========
Compared points     PO    DFF   BBOX    Total
--------------------------------------------------------------------------------
Equivalent          36    0     4       40
--------------------------------------------------------------------------------
Non-equivalent      0     517   0       517
================================================================================
==========
// Warning: (COMP3) There are extra POs in Revised
// Command: report compare data -class nonequivalent -class abort -class
notcompared > lec_compare_data.txt
// Command: report verification -verbose > lec_verification.txt
// Command: report statistics > lec_statistics.txt
// Command: report unmapped points -summary > lec_unmapped_summary.txt
// Command: report unmapped points -extra -unreachable -notmapped >
lec_unmapped_detailed.txt
// Command: tclmode
// Command: puts "No of compare points = [get_compare_points -count]"
No of compare points = 557
// Command: puts "No of diff points    = [get_compare_points -diff -count]"
No of diff points    = 517
// Command: puts "No of abort points   = [get_compare_points -abort -count]"
No of abort points   = 0
// Command: puts "No of unknown points = [get_compare_points -unknown -count]"
No of unknown points = 0
// Command: exit
```