EAST WEST UNIVERSITY
Department of Computer Science and Engineering
B.Sc. in Computer Science and Engineering Program
Mid Term I Examination, Fall2021

Course: CSE360 – Computer Architecture, Section-4
Instructor: Dr. Md. Sawkat Ali, Assistant Professor, CSE Department
Full Mark: 25
Time: 1 Hour and 20 Minutes

Note: There are FIVE questions, answer ALL of them. Course outcomes (CO), cognitive levels and marks of each question are mentioned at the right margin.

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1. The hypothetical machine has three instructions: [CO1,C2, Mark: 6]
   0100 = Load AC from I/O
   0101 = Store AC to I/O
   0110 = Add AC to Memory
   In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 1) for the following program:
   a) Load AC from device 14
   b) Sub contents of memory location 940
   c) Load AC from device 14
   d) Store AC to device 17
   Assume that the next value retrieved from device 14 is 10 and that location 940 contains a value of 5.

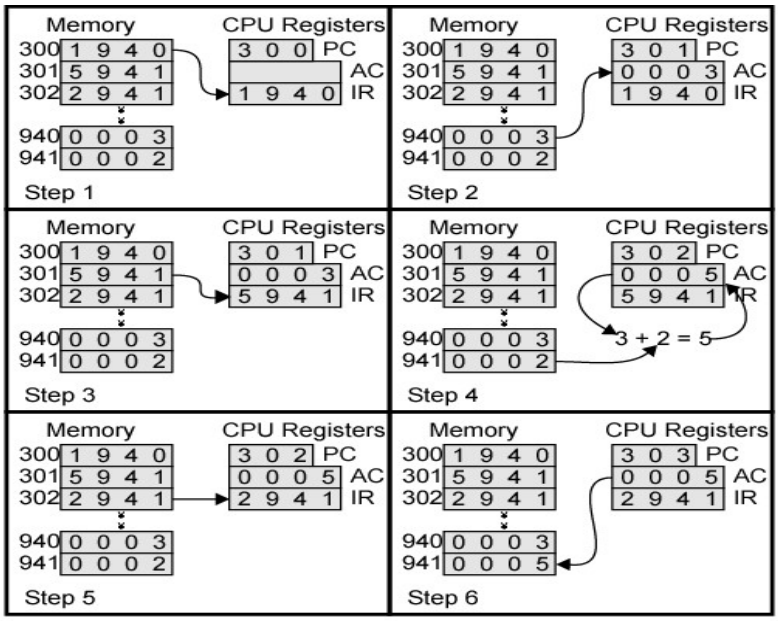

Figure 01

2. Consider a hypothetical microprocessor generating a 'X'-bit address (for example, assume that the program counter and the address registers are 16 bits wide) and having a 16-bit data bus. Note that, 'X' is the two digits addition value **(2+5=7)** (marked as red color in the example) of your student ID (**example:** 2014-2-60-2**25**). [CO2,C3 Mark: 3+3]
   a) What is the maximum memory address space that the processor can access directly if it is connected to a "16-bit memory"?
   b) What is the maximum memory address space that the processor can access directly if it is connected to an "8-bit memory"?

c) If an input and an output instruction can specify an 'X'-bit I/O port number, how many 16-bit I/O ports can the microprocessor support? How many 32-bit I/O ports? Explain.

3. A microprocessor has an increment memory direct instruction, which adds 3 to the value in a memory location. The instruction has five stages: fetch opcode (2 bus clock cycle), fetch operand address (4 bus clock cycle), fetch operand (8 bus clock cycle), add 3 to operand (5 clock cycle), and store operand (7 clock cycle). [CO1,C2, Mark: 3+2]

   a) By what amount in percent will the duration of the instruction increase if we insert two bus wait states in each memory write operations?
   b) Repeat assuming that the increment operation taken 10 clock cycles instead of 5 clock cycles.

4. A CPU operates at a clock frequency of 125 GHz, requires an average of 77 CPI for executing one instruction, **what** is the performance (in MIPS) of the CPU? [CO1, C3, Mark: 3]

5. Consider a microprocessor that has a memory read timing as shown in Figure 02. After some analysis, a designer found that the memory read the data 180 ns before of the assigned time. [CO1, C3, Mark: 2+ 3]

   a) How many wait states (clock cycles) need to be inserted for proper system operation if the bus clocking rate is 10 MHz?

   b) To enforce the wait states, a Ready status line is employed. Once the processor has issued a Read command, it must wait until the Ready line is asserted before attempting to read data. At what time interval must we keep the Ready line low in order to force the processor to insert the required number of wait states?

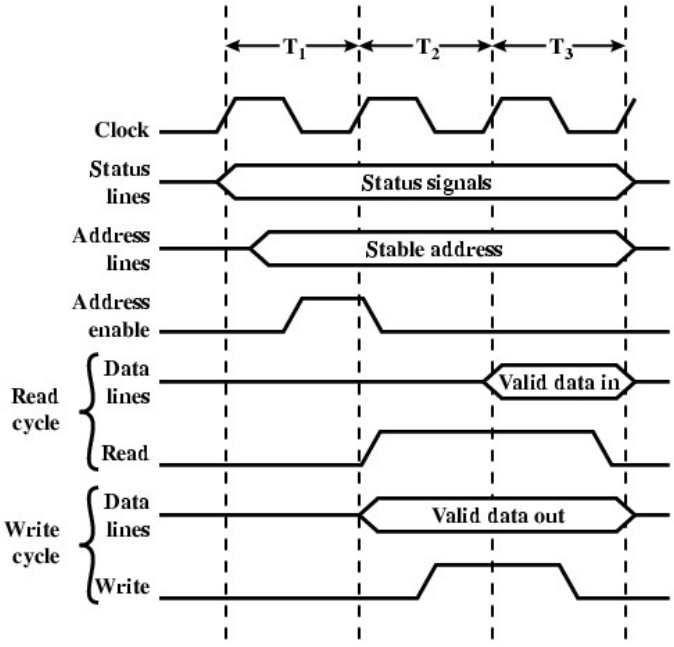

Figure 02