P116C Homework 2

Due 4/22/2021 at 5PM

1. A Verilog module defines A,B, and C as follows

```
reg [3:0] A=4'b0110;
reg [3:0] B=4'b1011;
reg [3:0] C;
```

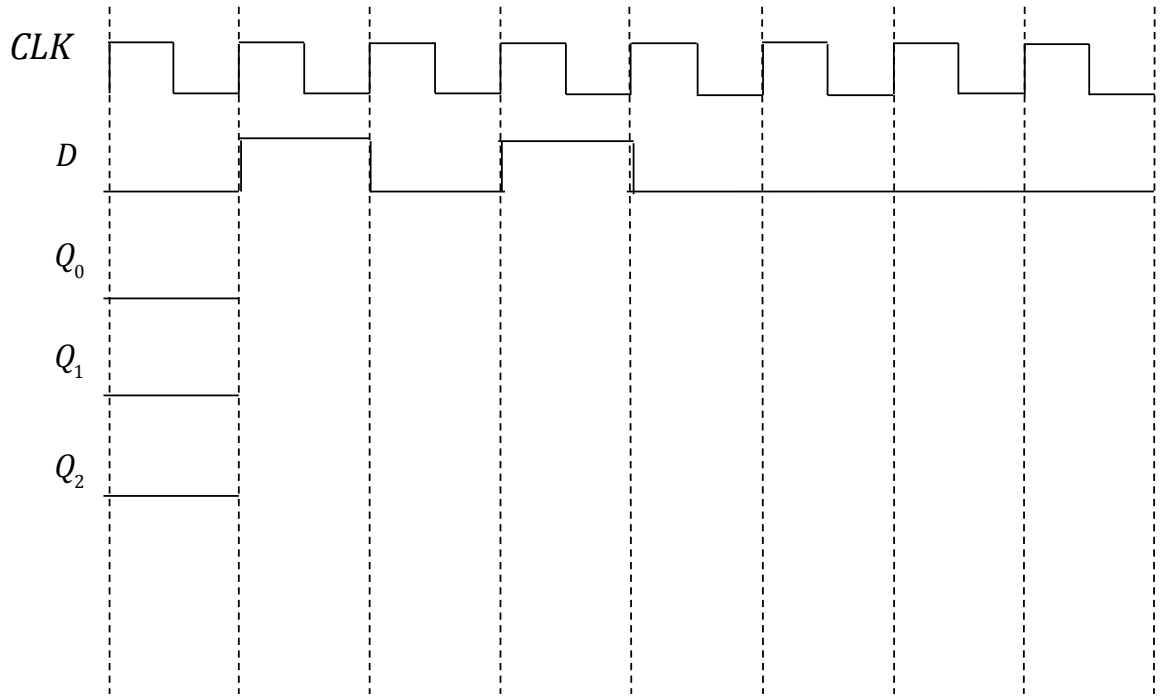
   Assuming A and B remain unchanged, evaluate the binary value of C for each of the following cases:

   - `C=A+B;`
   - `C={B[2:1],A[1:0]};`
   - `C=A|B;`
   - `C=A&B;`
   - `C=A^B;`
   - `C=A<<2;`
   - `C=B>>1;`
   - `C=|A;`
   - `C=&B;`
   - `C=(~A)|B;`

2. For the following module

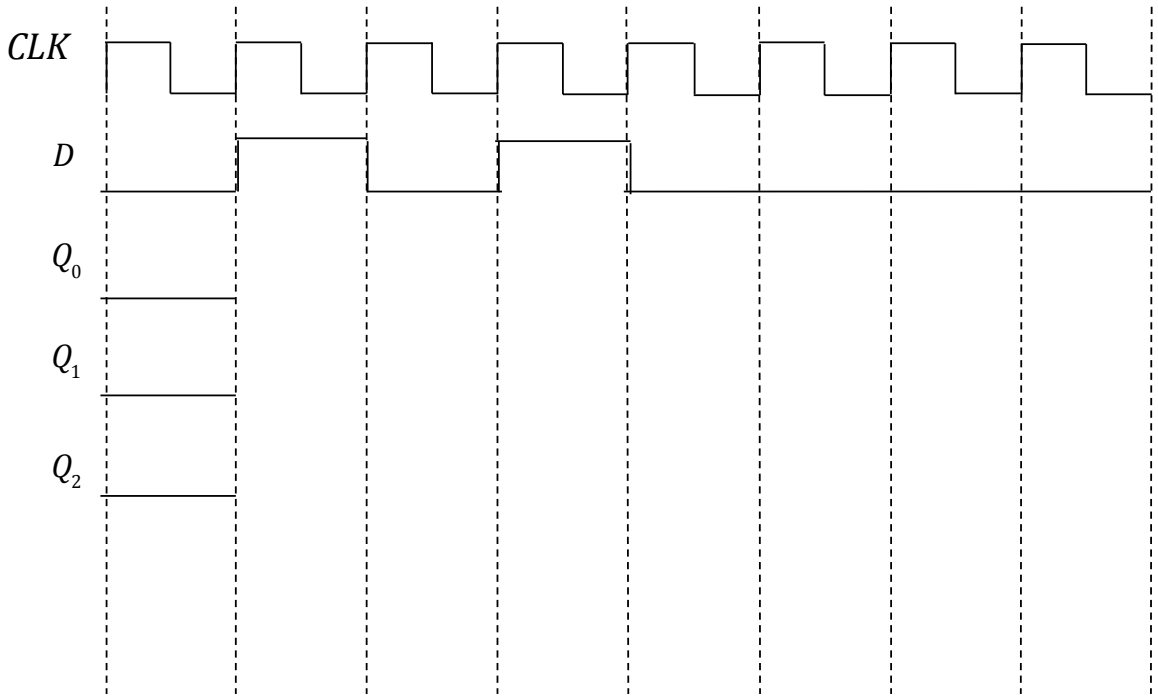
```
module hw2 (
  input clk,          // system clock
  input D,
  output reg Q0=0,
  output reg Q1=0,
  output reg Q2=0);    // Serial data bit

  always @(posedge clk) begin
    Q0 <= D;          // non-bloacking statements
    Q1 <= Q0|D;
    Q2 <= Q0&Q1;
  end

endmodule
```

   Complete the following time line, assuming $Q1$, $Q2$ and $Q3$ all start at 0, and that D changes state just *after* the clock edge. You can code this up in EDA Playground if you'd like.



Now Repeat the problem if the non-blocking statements are replaced with blocking statements.

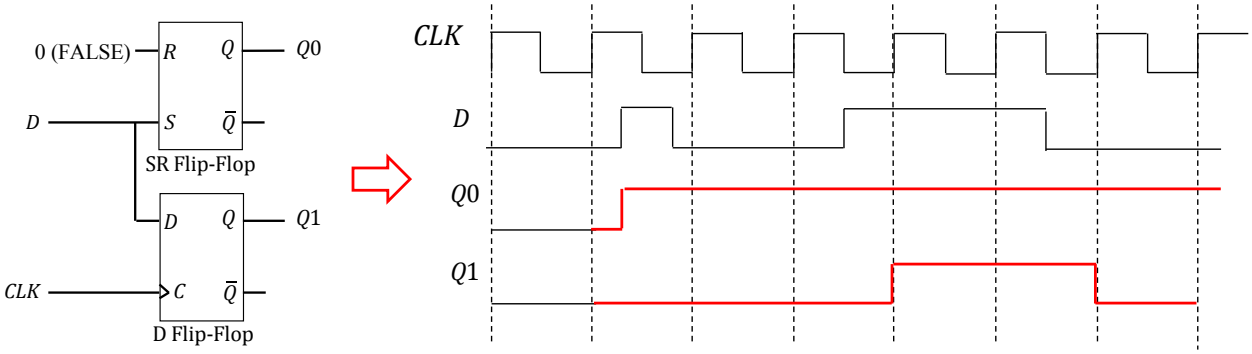
```
module hw2 (
  input clk,          // system clock
  input D,
  output reg Q0=0,
  output reg Q1=0,
  output reg Q2=0);    // Serial data bit

  always @(posedge clk) begin
    Q0 = D;          // blocking statements
    Q1 = Q0|D;
    Q2 = Q0&Q1;
  end

endmodule
```



3. Write a Verilog module with the following interface

```
module hw2 (
  input clk,          // system clock
  input D,
  output reg Q0=0,
  output reg Q1=0);
//...Your code.../
 endmodule
```

that will emulate the following circuit:



Put it into EDAPlayground and set up a test bench to test it with a 10ns clock period. You timings for the D bit can be approximate, provided it rises and falls between the appropriate clock edges, as shown. Turn in your code for the module and testbench (screenshots are acceptable) as well as the resulting waveforms. (Hint: write a separate `always` block for each flip flop.)

4. I have and 10-bit unipolar DAC with a 4V reference voltage

(a) What voltage change is associated with the least significant bit (LSB) changing from 0 to 1?

(b) What voltage change is associated with the most significant bit (MSB) changing from 0 to 1?

(c) What will be the output for a DAC setting of 450 (decimal)?

5. I want to design a bipolar ADC to operate between -5V and +5V.

(a) If I want the LSB to be equal to or less than 1mV, what's the least number of bits I need to use?

(b) Assuming this ADC uses "offset binary" for the output, what will be the nearest decimal value for an input of +2V?