CSE 151A HW 01

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Contents

1 Preface

This project explores a subset of the ARM instruction set. A custom instruction set inspired by the ARM architecture was designed with a custom assembler. The architecture was implemented in hardware as an RTL model, whose functionality was verified.

The assembler was implemented in Python, and the RTL model was implemented using SystemVerilog.

2 ISA Design

3 Assembler

4 Instruction Memory

5 Program Counter

6 Program Counter Adder

7 Register File

8 Data Memory

9 ALU

10 ALU Control

11 FPU

12 FPU Control