

组成原理 Lab_0

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我的代码：

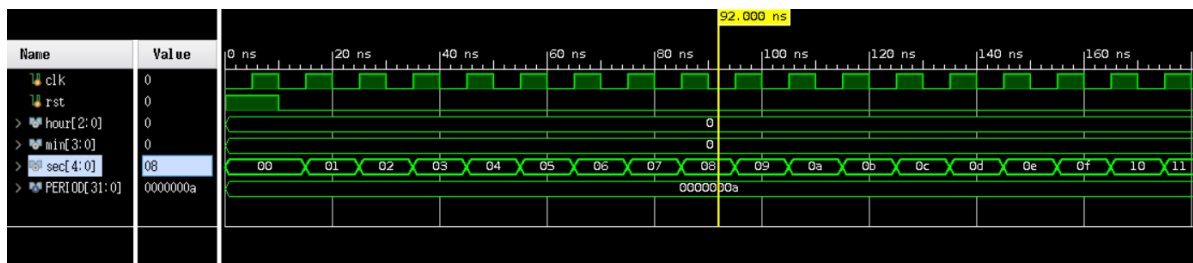
```
1  module clock(  
2      input clk,  
3      input rst,  
4      output [2:0] hour,  
5      output [3:0] min,  
6      output [4:0] sec  
7  );  
8  
9      Sec Sec(.clk(clk),.rst(rst),.sec(sec));  
10     Min Min(.clk(clk),.rst(rst),.sec(sec),.min(min));  
11     Hour Hour(.clk(clk),.rst(rst),.sec(sec),.min(min),.hour(hour));  
12  
13 endmodule  
14  
15 module Sec (  
16     input clk,  
17     input rst,  
18     output reg [4:0] sec  
19 );  
20     always @(posedge clk or posedge rst) begin  
21         if(rst==1)  
22             sec<=0;  
23         else begin  
24             if(sec==5'h13)  
25                 sec<=5'h0;  
26             else  
27                 sec<=sec+1;  
28         end  
29     end  
30 endmodule  
31  
32 module Min (  
33     input clk,  
34     input rst,  
35     input [4:0] sec,  
36     output reg [3:0] min  
37 );  
38     always @(posedge clk or posedge rst) begin  
39         if(rst==1)  
40             min<=0;  
41         else begin  
42             if (min==4'h9 && sec==5'h13)  
43                 min<=4'h0;  
44             else begin  
45                 if(sec==5'h13)  
46                     min<=min+1;
```

```

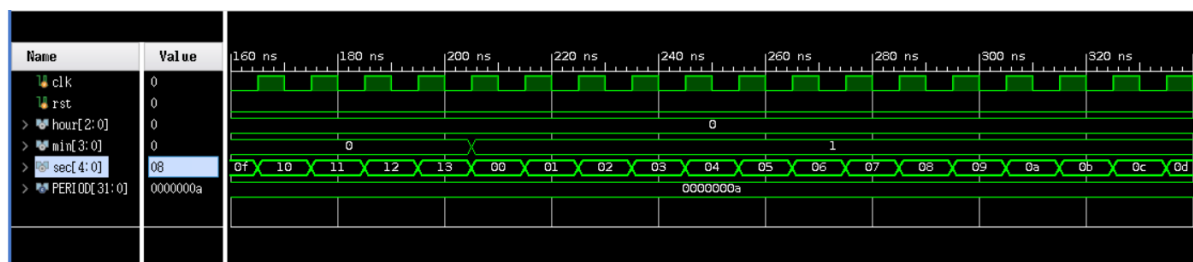
47         end
48     end
49 end
50 endmodule
51
52 module Hour (
53     input clk,
54     input rst,
55     input [3:0] min,
56     input [4:0] sec,
57     output reg [2:0] hour
58 );
59     always @(posedge clk or posedge rst) begin
60         if(rst==1)
61             hour<=0;
62         else begin
63             if(hour==3'h4 && min==4'h9 && sec==5'h13)
64                 hour<=3'h0;
65             else begin
66                 if(min==4'h9 && sec==5'h13)
67                     hour<=hour+1;
68             end
69         end
70     end
71 endmodule

```

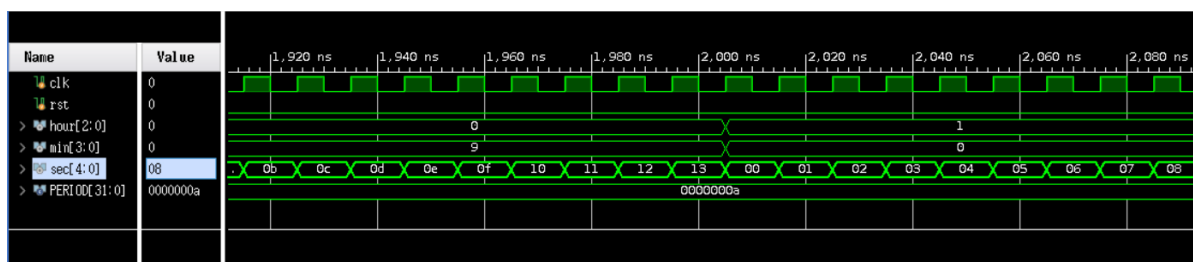
所有模块的仿真波形：



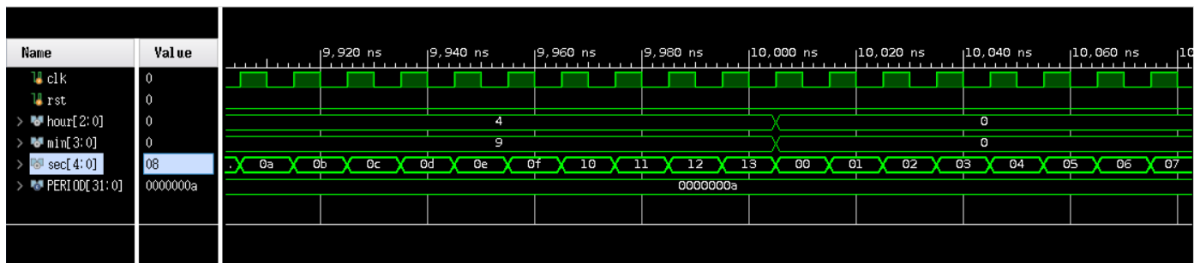
初始波形



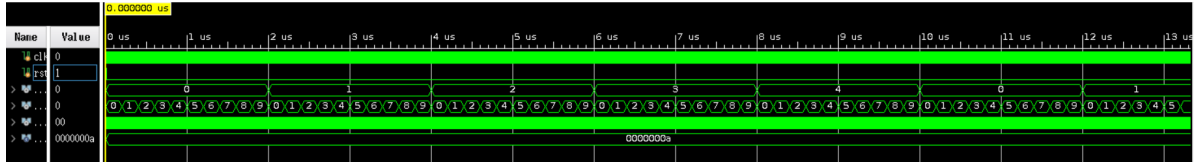
0分钟 -> 1分钟



0小时 -> 1小时

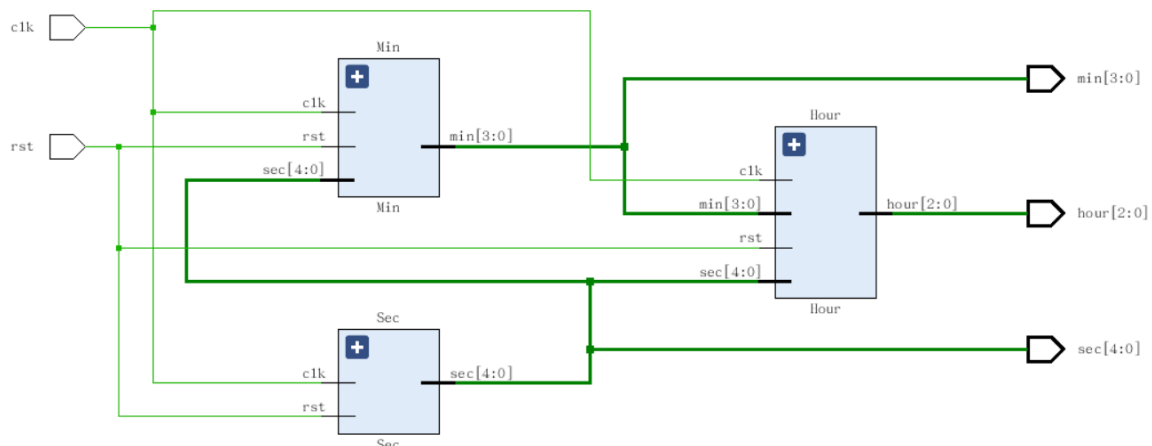


4小时9分钟19秒 -> 0小时0分钟0秒

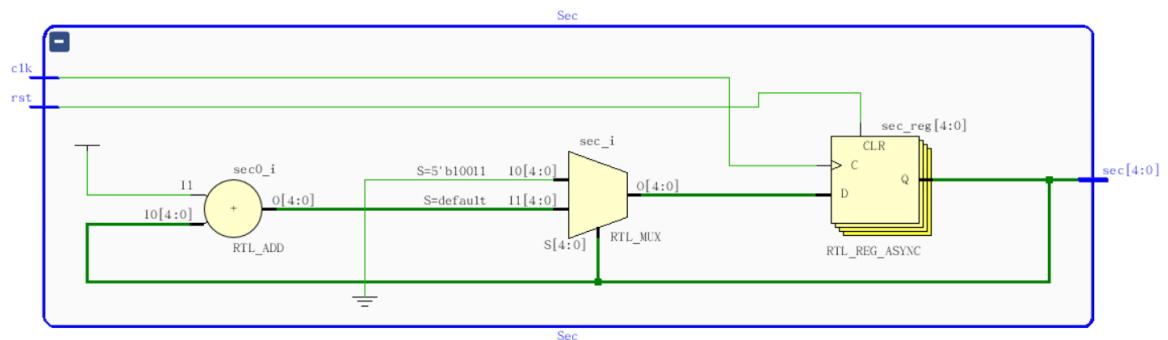


总体波形

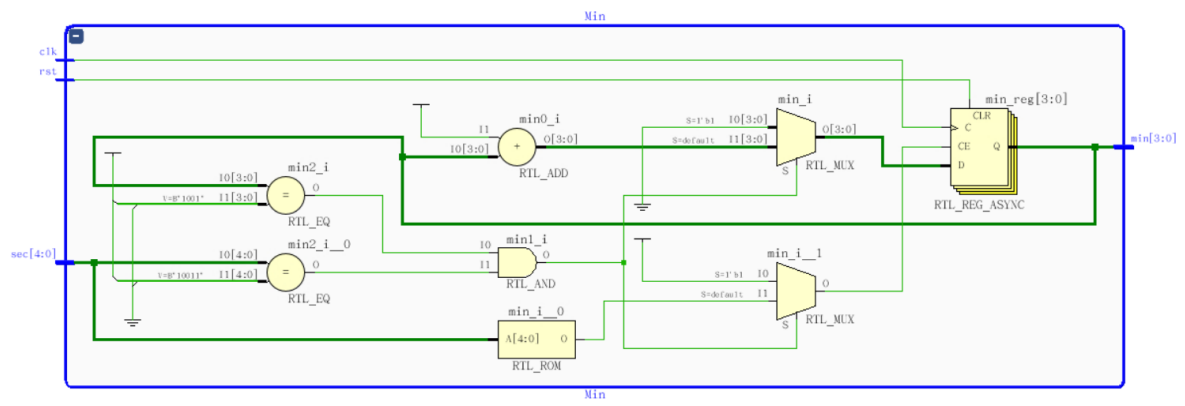
生成的电路图：



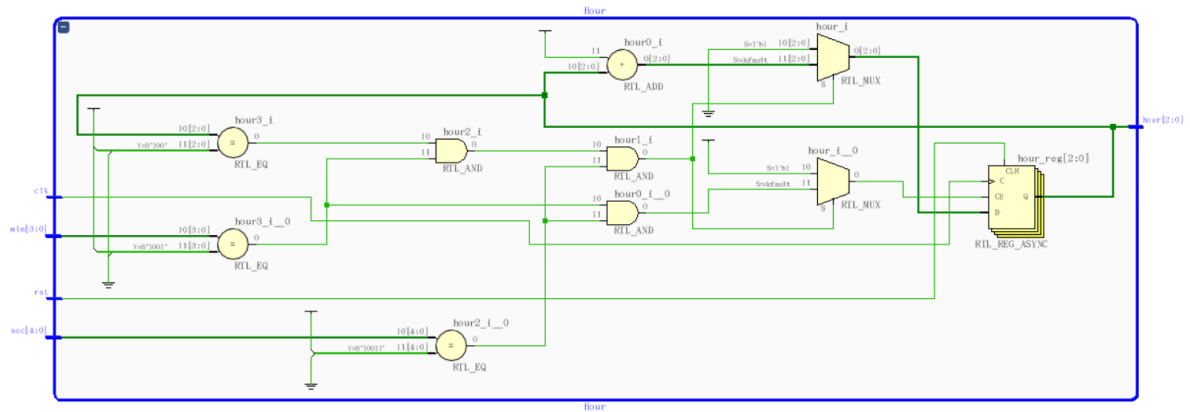
Clock模块总体电路



Sec模块电路



Min模块电路



Hour模块电路

实验反馈：

挺好，没想出什么毛病。