组成原理 Lab_0

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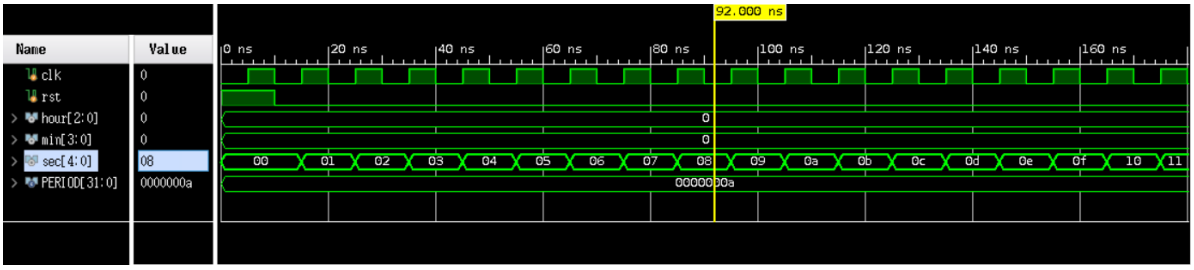
我的代码：

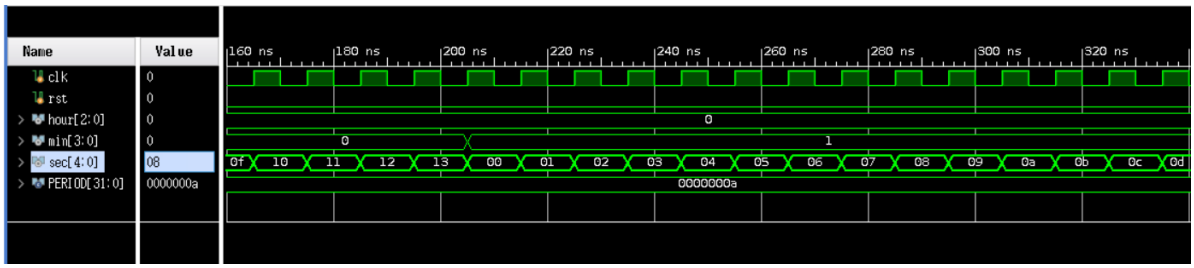
```
module Clock(
    input clk,
    input rst,
    output [2:0] hour,
    output [3:0] min,
    output [4:0] sec
);

    Sec Sec(.clk(clk),.rst(rst),.sec(sec));
    Min Min(.clk(clk),.rst(rst),.sec(sec),.min(min));
    Hour Hour(.clk(clk),.rst(rst),.sec(sec),.min(min),.hour(hour));

endmodule

module Sec (
    input clk,
    input rst,
    output reg [4:0] sec
);
    always @(posedge clk or posedge rst) begin
        if(rst==1)
            sec<=0;
        else begin
            if(sec==5'h13)
                sec<=5'h0;
            else
            sec<=sec+1;
        end
    end
endmodule

module Min (
    input clk,
    input rst,
    input  [4:0] sec,
    output reg [3:0] min
);
    always @(posedge clk or posedge rst) begin
        if(rst==1)
            min<=0;
        else begin
            if (min==4'h9 && sec==5'h13)
                min<=4'h0;
            else begin
                if(sec==5'h13)
                    min<=min+1;
```

```
            end
        end
    end
endmodule

module Hour (
    input clk,
    input rst,
    input [3:0] min,
    input [4:0] sec,
    output reg [2:0] hour
);
    always @(posedge clk or posedge rst) begin
        if(rst==1)
            hour<=0;
        else begin
            if(hour==3'h4 && min==4'h9 && sec==5'h13)
                hour<=3'h0;
            else begin
                if(min==4'h9 && sec==5'h13)
                    hour<=hour+1;
            end
        end
    end
endmodule
```

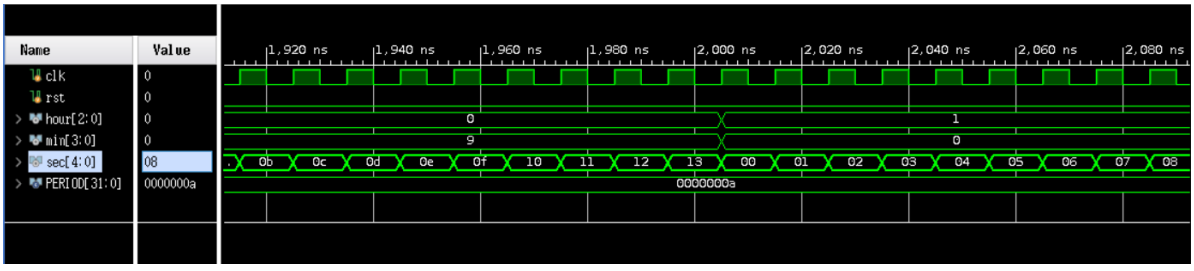
所有模块的仿真波形：



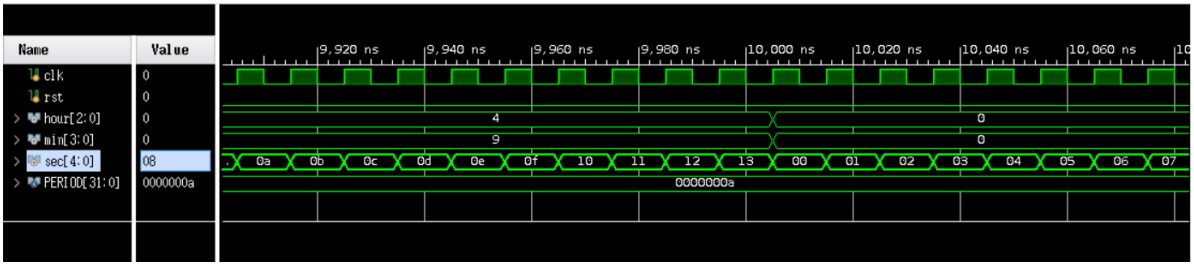
初始波形



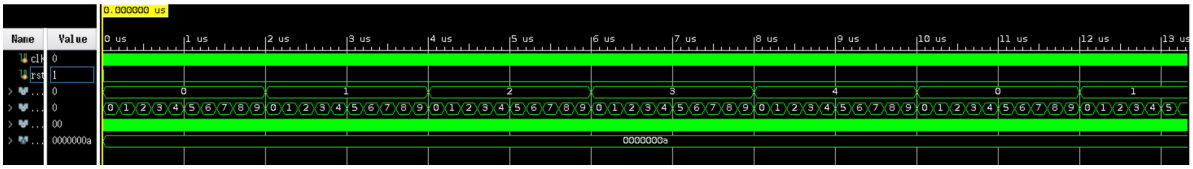
0分钟 -> 1分钟



0小时 -> 1小时

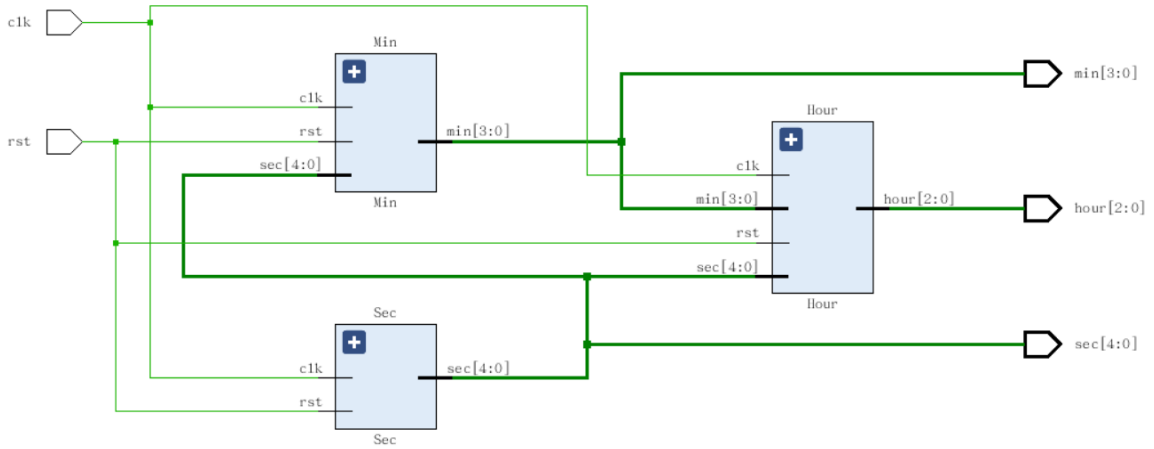


4小时9分钟19秒 -> 0小时0分钟0秒

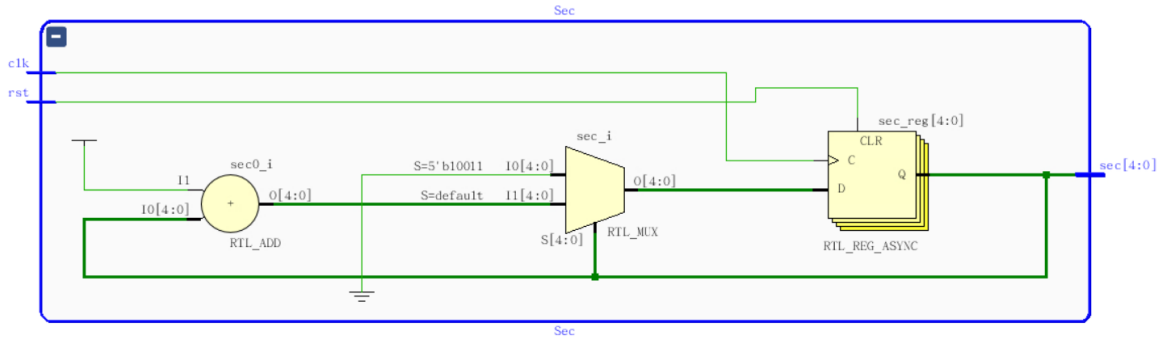


总体波形

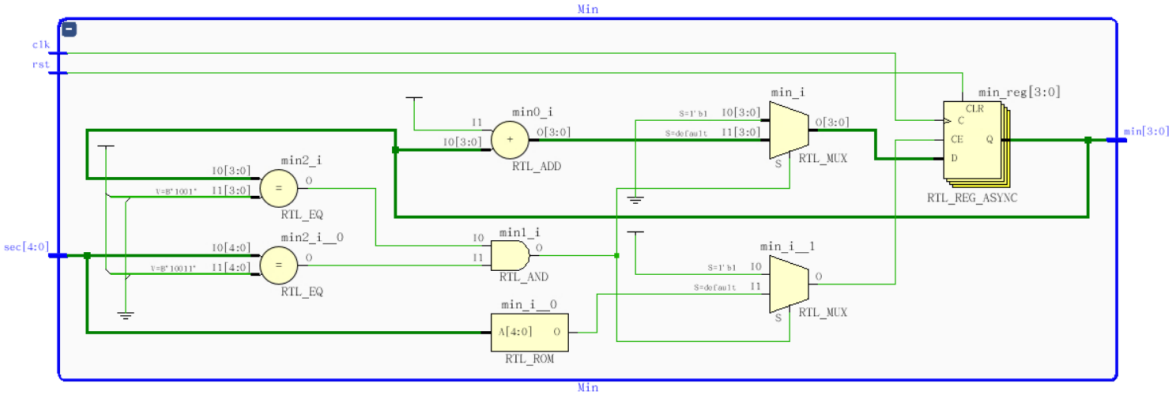
生成的电路图：



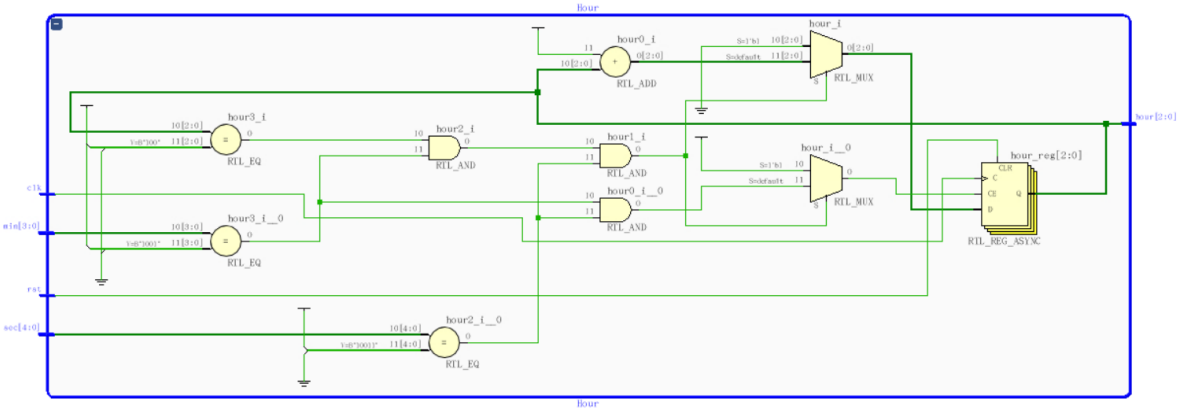
Clock模块总体电路



Sec模块电路



Min模块电路



Hour模块电路

实验反馈：

挺好，没想出什么毛病。