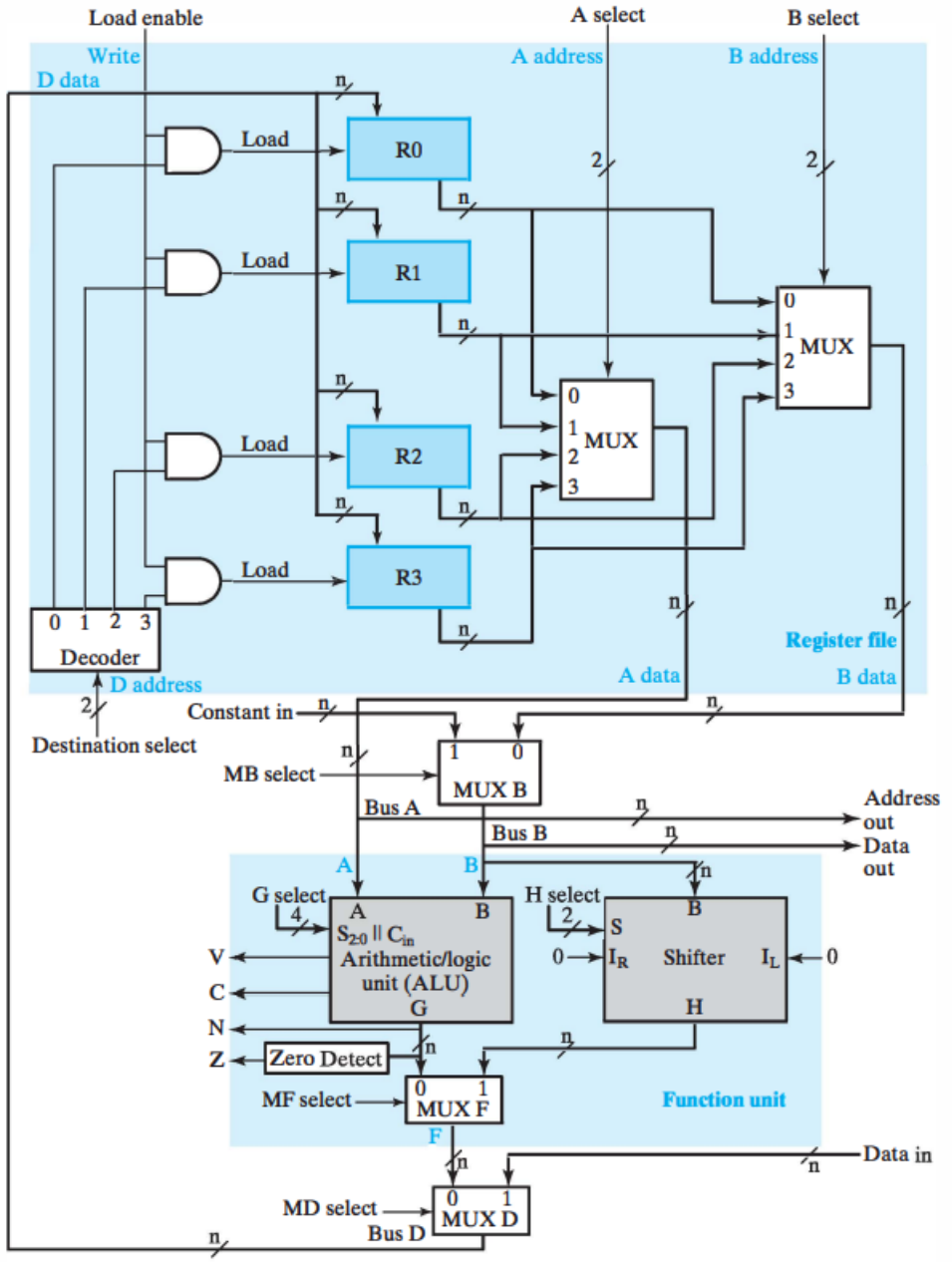
RISC CPU DESIGN

with sorting application

Taeyeop Lee

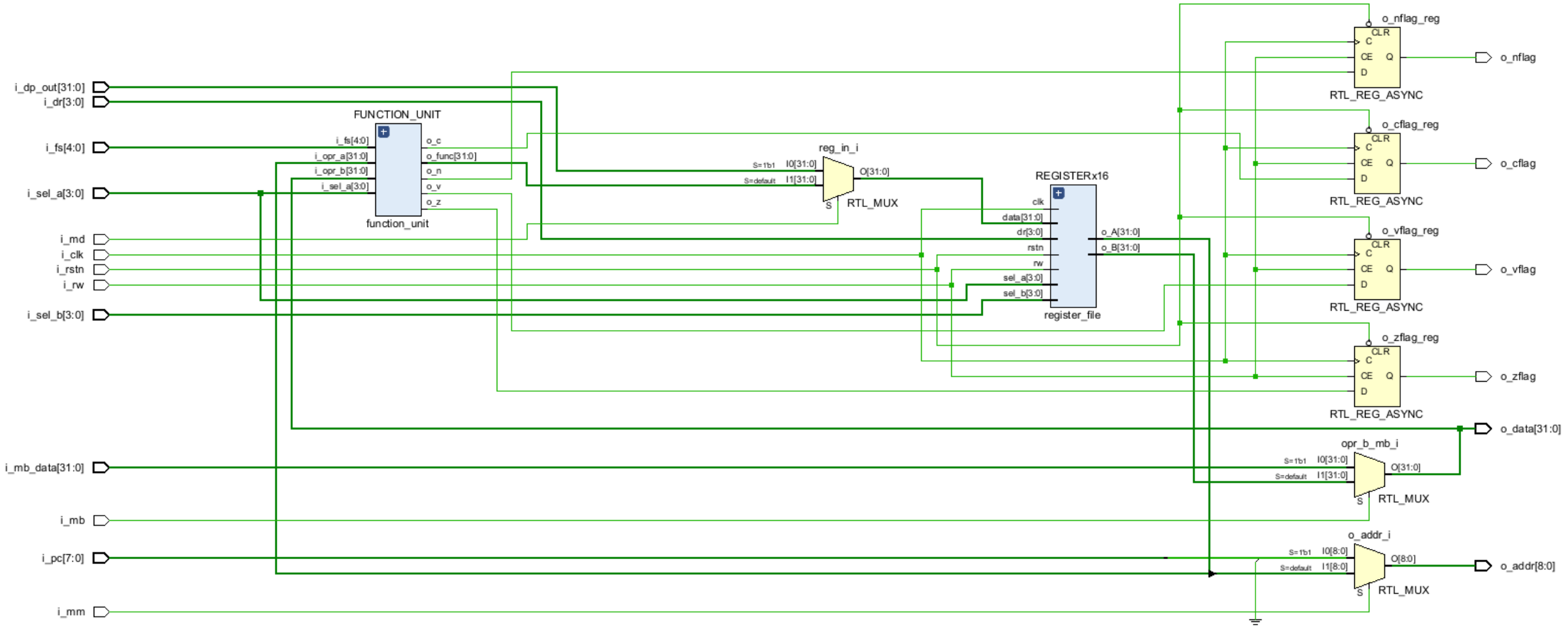
Datapath

Basic Structure



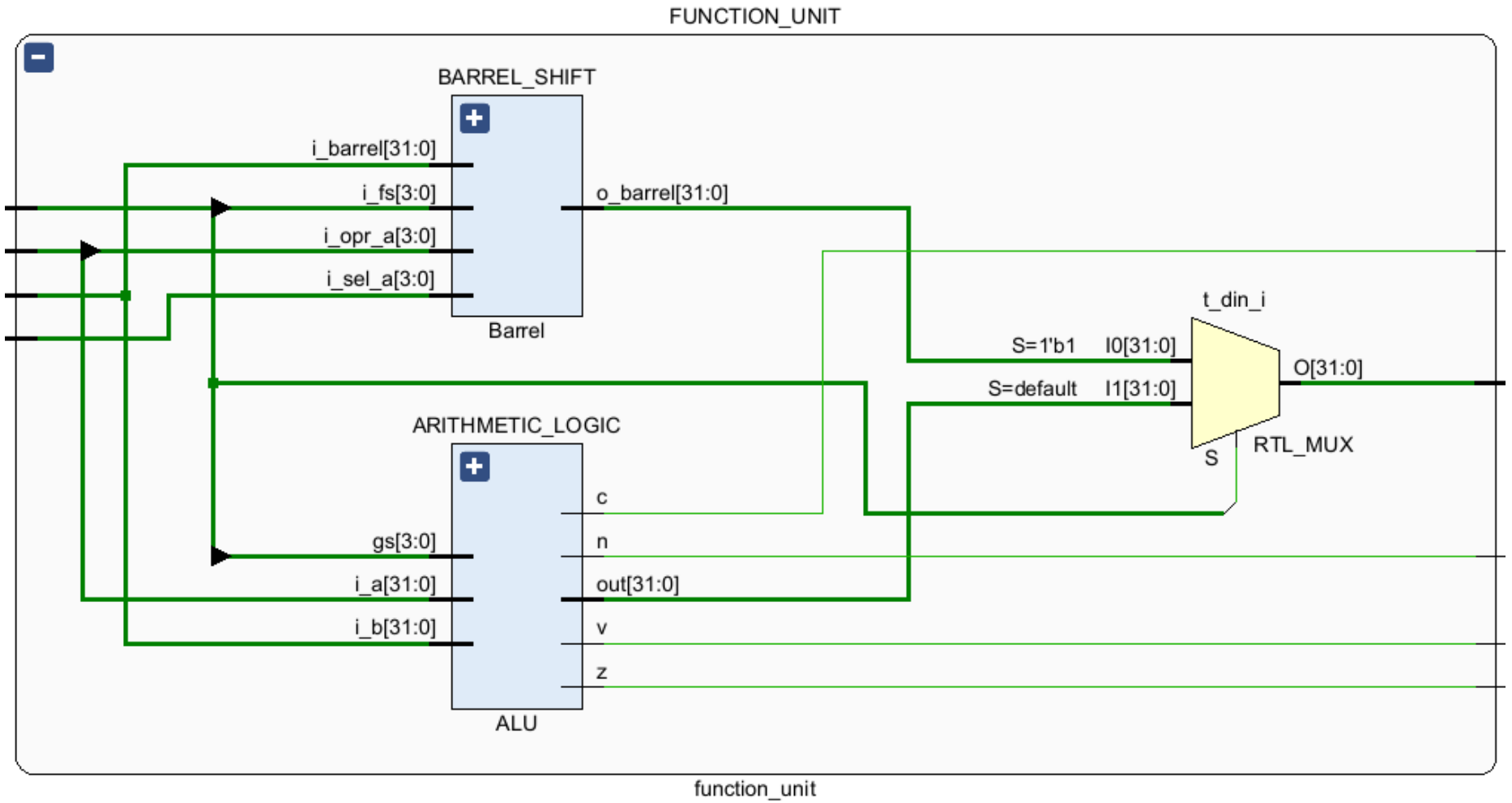
Datapath

Implementation



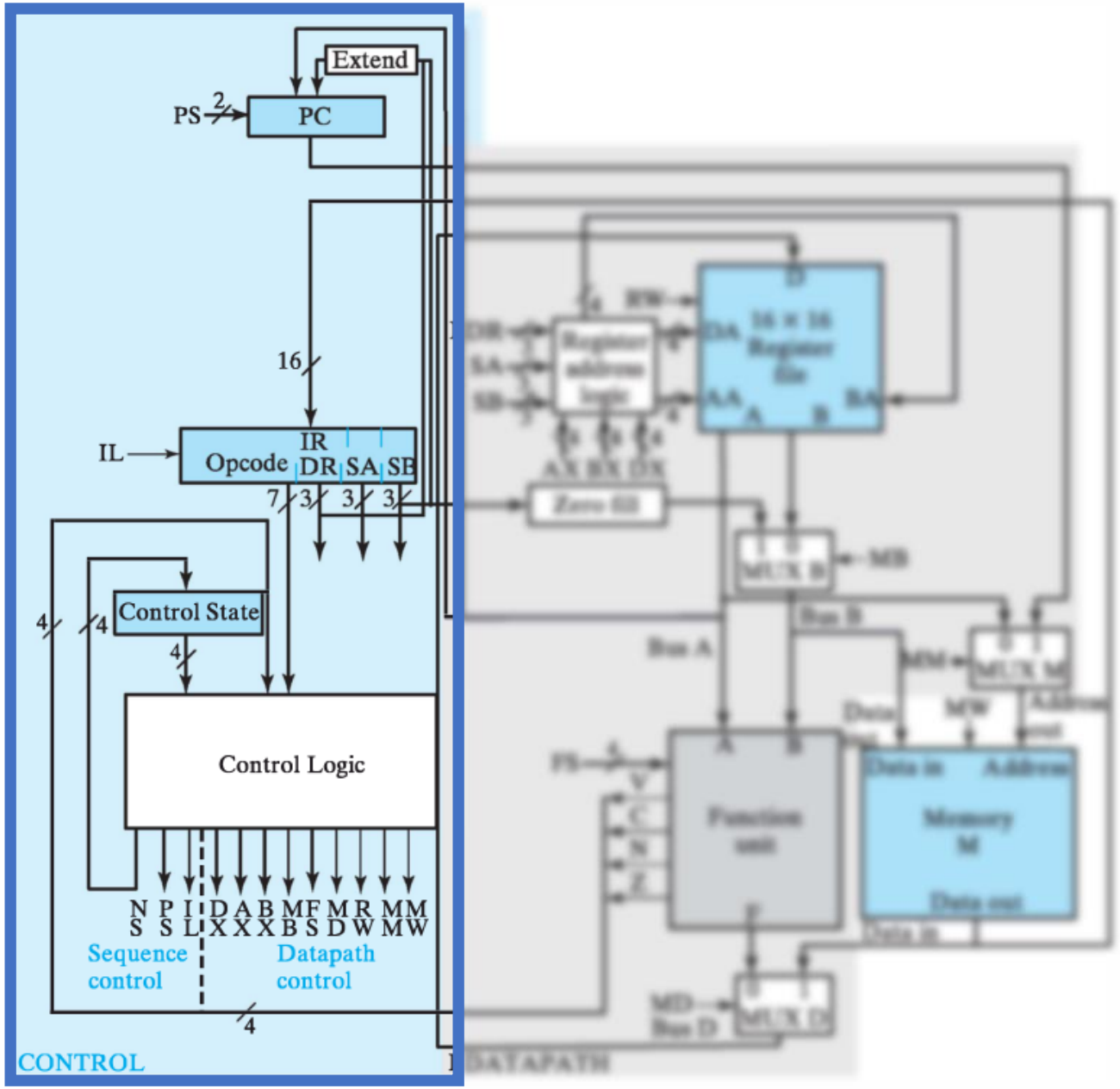
Function Unit

zoom view



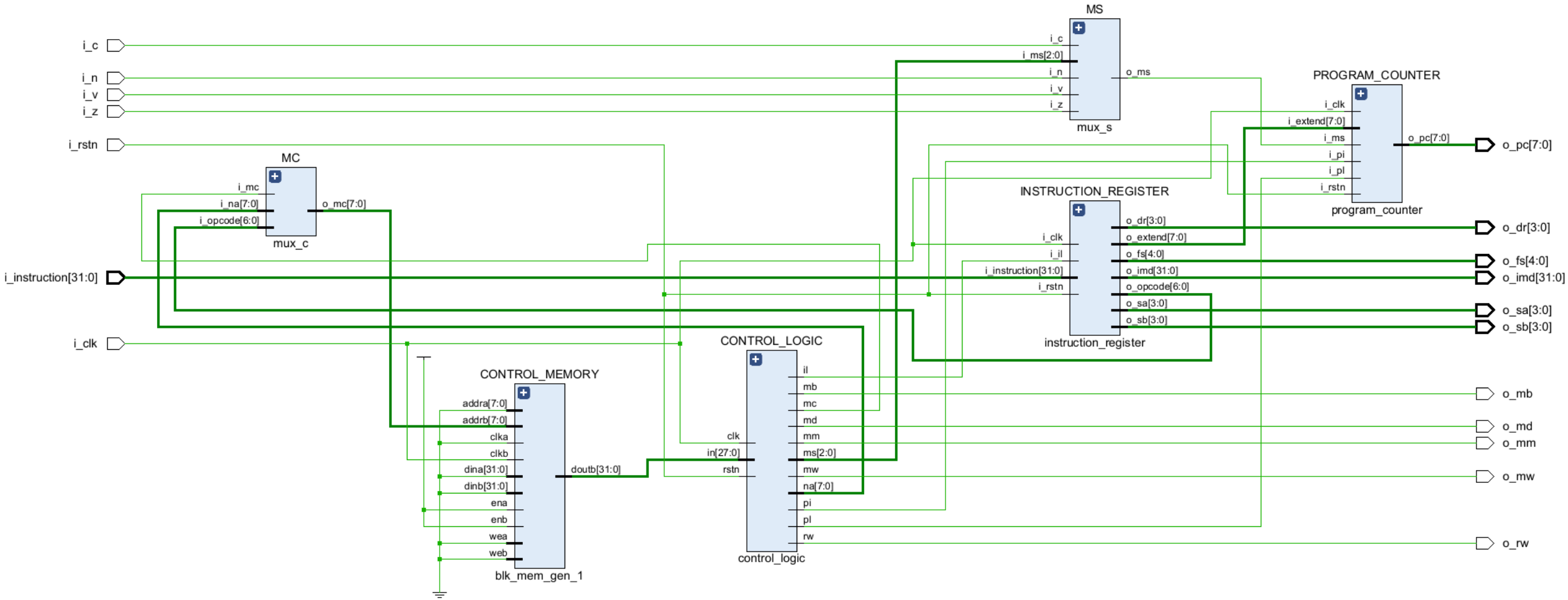
Control

Basic Structure



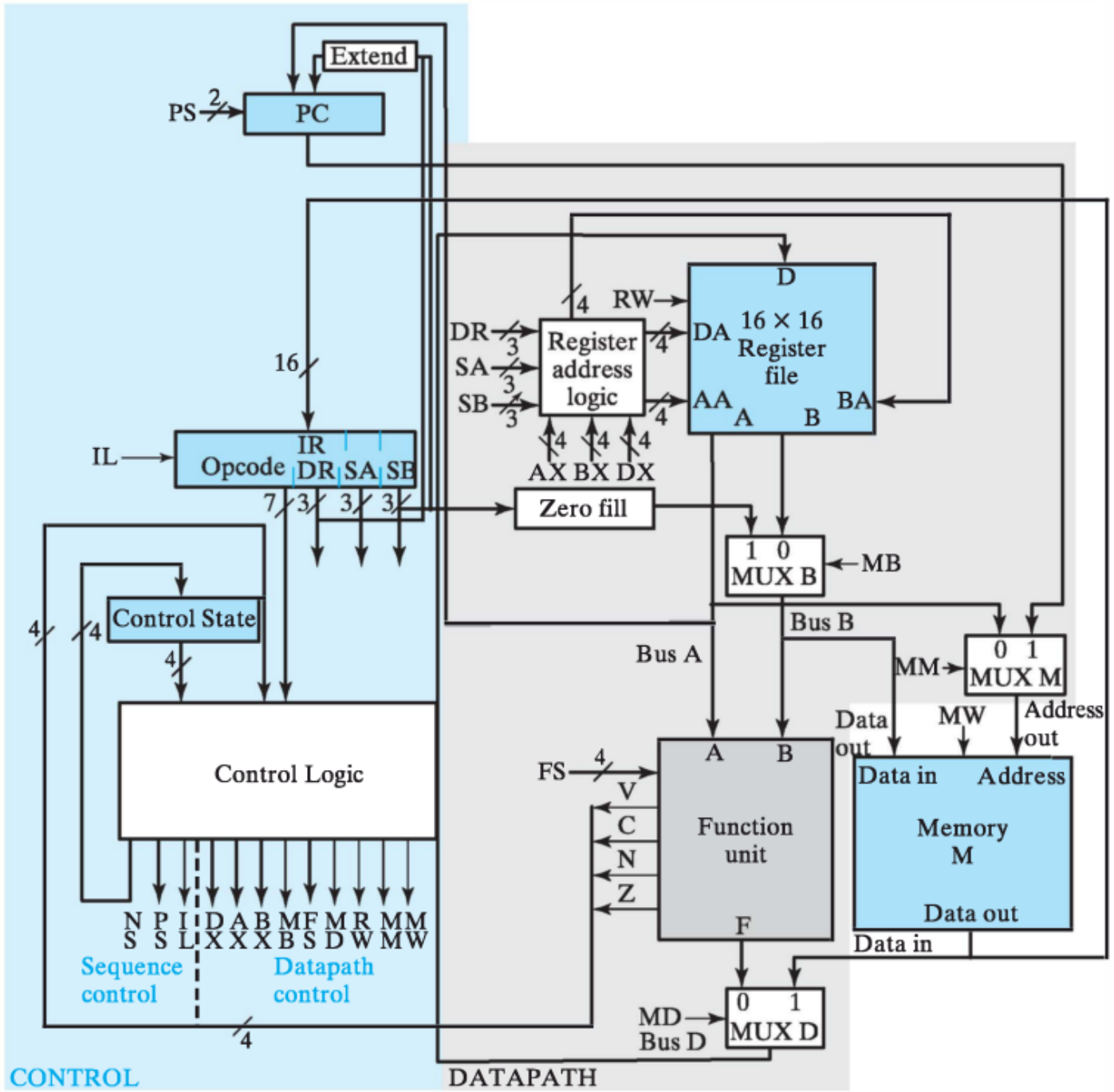
Control

Implementation



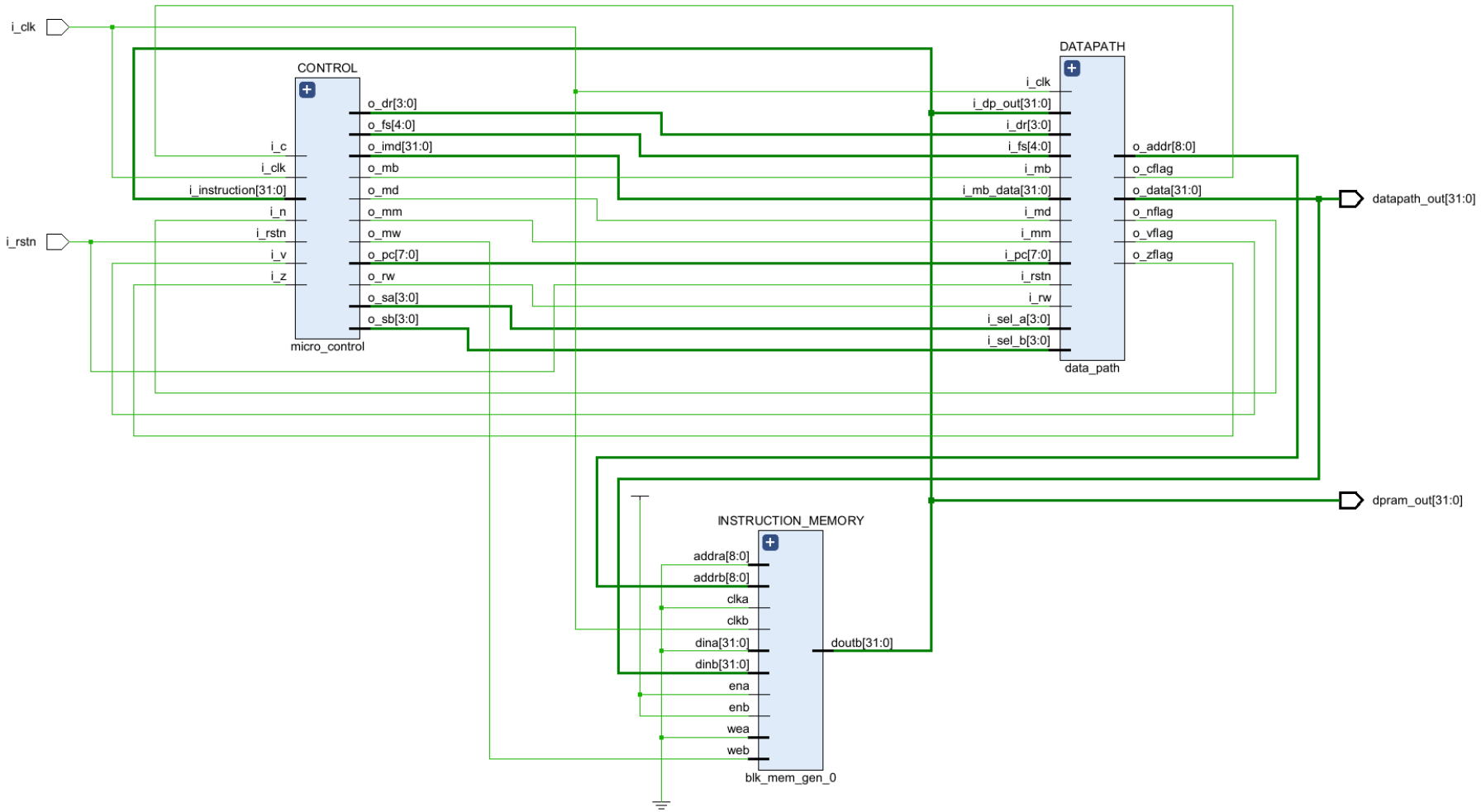
top_CPU

Basic Structure



top_CPU

Implementation



Instructions

opcode	symbol	description
00000	MVA	F = A
00001	INC	F = A + 1
00010	ADD	F = A + B
00011	AD1	F = A + B + 1
00100	SB1	F = A + B'
00101	SUB	F = A + B' + 1
00110	DEC	F = A - 1
00111	MVA	F = A
01000	AND	F = A and B
01010	OR	F = A or B
01100	XOR	F = A xor B
01110	NOT	F = A'
10000	MVB	F = B
10010	LSL	F = lsl
10100	LSR	F = lsr
10110	ASR	F = asr
10111	ABSR	F = absr (arith barrel shift right)
11000	RL	F = rl B
11010	RR	F = rr B
11100	BRR	F = barrel rotate right by SA[3:0]
11101	BRL	F = barrel rotate left by SA[3:0]
11110	BSR	F = barrel shift right by SA[3:0]
11111	BSL	F = barrel shift left by SA[3:0]

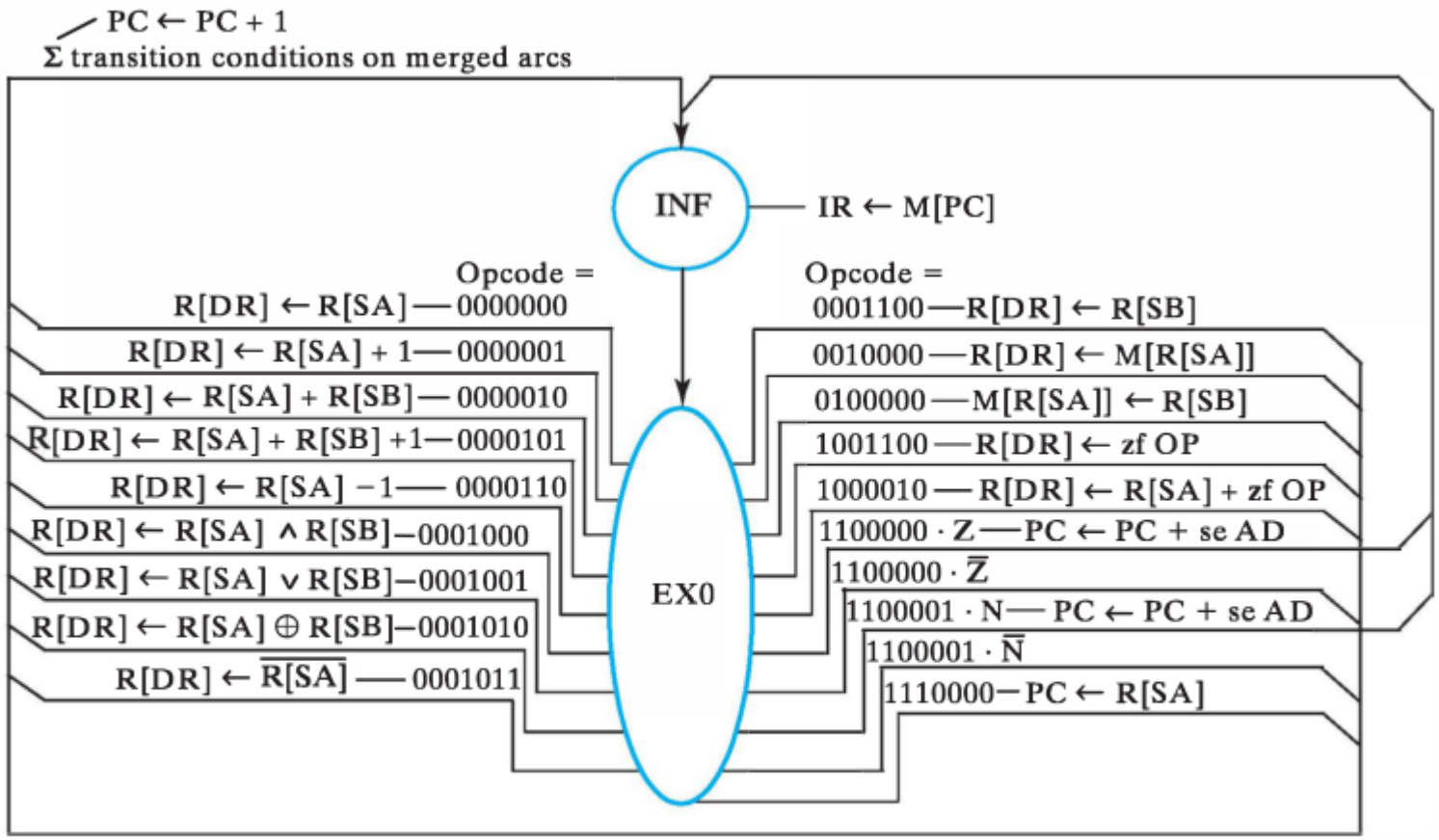


FIGURE 9-20
Partial State Machine Diagram for Multiple-Cycle Computer

Sorting

Algorithm

Order	Operation	opr[31:19]	opcode[18:12]	dr[11:8]	sa[7:4]	sb[3:0]	pc	Control_Memory_Address
0	MVBI R7 #383	000000010111	1010000	0111	0000	1111	0	00BD070F
1	MVBI R7 #256	000000010000	1010000	0101	0000	0000	1	00850500
2	MVA R3 R7	000000000000	0000000	0011	0111	0000	2	00000370
3	MVA R4 R3	000000000000	0000000	0100	0011	0000	3	00000430
4	DEC R3 R3	000000000000	0000110	0011	0011	0000	4	00006330
5	LD R1 M[R3]	000000000000	0110000	0001	0011	0000	5	00030130
6	LD R2 M[R4]	000000000000	0110000	0010	0100	0000	6	00030240
7	SUB R6 R1 R2	000000000000	0000101	0110	0001	0010	7	00005612
8	BRNC + 2	000000000000	1100110	0000	0010	0000	8	00066020
9	ST M[R3] R2	000000000000	0100000	0000	0011	0010	9	00020032
10	ST M[R4] R1	000000000000	0100000	0000	0100	0001	A	00020041
11	SUB R6 R3 R5	000000000000	0000101	0110	0011	0101	B	00005635
12	BRNZ -10	000000000000	1100111	1111	0110	0000	C	00067F60
13	INC R5 R5	000000000000	0000001	0101	0101	0000	D	00001550
14	SUB R6 R5 R7	000000000000	0000001	0110	0101	0111	E	00005657
15	BRNZ -14	000000000000	1100111	1111	0000	0000	F	00067F20
16	BR -1 (HOLD)	000000000000	1100001	1111	1111	0000	10	00061FF0
17	No Operation	000000000000	0000000	0000	0000	0000	11	00000000

top_CPU Testbench

Given :
128 Random Numbers

>>>

Result :
Sorted in Ascending Order