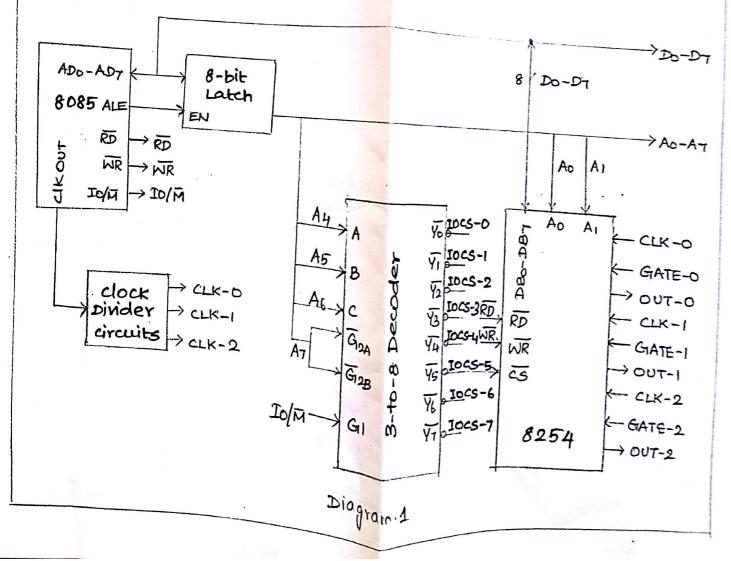
Design an Interfacing tor interfacing the 8254 and 8085 processor is shown in diagram. I the 8254 the 8254 can be either memory mapped or Ic-mapped in the system. In the schematic shown in diagram. I the 8254 is Io-mapped in the system. The chip select signals for Io-mapped devices are generated by using a 3-to-8 decoder. The address sines AH, A5 and A6 are decoded to generate eight chip select signals (Iocs-0 to Iois-7) and in this, the chip select Iocs-5 is used to select the 8254. The address sine A7 and the control signal Io/M are used to enable the decoder.



connected to Ao and A, of the 8254 to provide the internal address. The IO addresses alloted to the internal devices of 8254 at listed in below table. The data lines Do-DT, RD and WR signals of the 8254 are connected to the Do-DT, RD and WR of the Processor respectively to achieve parallel data transfer.

Table: 10 Addresses of 8254 interfaced to 8085 As shown in diagram. 1

Internal device	Dec	oder	BINARY A Input enable		Input to address pins of 8254				Hexa address
	A7	AL	A5	AH	Az	A ₂	Aı	Ao	
counter-o	0	1	0	1	X	χ	0	0	50
counter-1	0	ţ	O	,	X	X	0	,	51
counter_2	0	ſ	0	ı	X	X	ı	6	52
control Register	0	ſ	0	1	х	X	1	l	53

Note: Don't care "x" is considered as zero.

The clock signals required for the counters can be obtained either from the processor clock output or from an external clock source. The clock signal from a 8085 can also be divided to lower values by using clock divider circuits and then applied to clock input of counters.

```
A switch is connected to Pin 72.7, write a program
to monitor the status of and perform the following:
a) If BW=0, the stepper motor moves clockwise
b) If GW=1, the otepper motor moves counter clockwise.
PROGRAMI.
                 ; starting address
  ORG
       OH
MAIN?
                 ; make an input
  SETB P2.7
       Ar #66H; storking phose value
  MOV
                  ; send value to port
   MOV
         PLA
TURNI
                  ; check switch result
  JNB
         P2-7,CW
                   ; notate right
   RR
      · A
                    call delay
   A CALL DELAY
                    write value to port
       PIA
   MOV
                    repeat
   SJMP TURN
                  ; rotate left
CW: RL
         A
   A CALL DELAY
                  ; call delay
                  ; Write value to port
   MOV PILA
                  ; repeat
   SJMP TURN
DELAYI
       R2,#100
   MOV
       R3,#255
HI: MOV
H2: DJNZ
       R3, H2
        R2, H1
   DJNZ
   RET
   END
```

Algorithm:

- 1. start
- 2-Make an input P2.7
- phase value and send the value to port 3. Start the
- 4. Check the switch result and notate to right
- 5. call a delay and write the value to port and repeat
- 6, rotate left again and call a delay.
- 7. write the values to port and repeat the process