Imperas Peripheral Model Guide

Model Specific Information for freescale.ovpworld.org / KinetisMPU

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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

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1.0 Model Specific Information

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers, other component parts, and configuration options and general information for peripheral modeling with Imperas OVP.

1.1 Description

Model of the MPU peripheral used on the Freescale Kinetis platform

1.2 Limitations

Provides the base behaviour for the OVP Freescale Kinetis platforms

1.3 Reference

www.freescale.com/Kinetis

1.4 Licensing

Open Source Apache 2.0

1.5 Location

The KinetisMPU peripheral model is located in an Imperas/OVP installation at the VLNV: freescale.ovpworld.org / peripheral / KinetisMPU / 1.0.

2.0 Net Ports

This model has the following net ports:

Table 1. Net Ports

Name	Type	Must Be Connected	Description
Reset	input	F (False)	

3.0 Bus Slave Ports

This model has the following bus slave ports:

3.1 Bus Slave Port: bport1

Table 2. Bus Slave Port: bport1

Name	Size (bytes)	Must Be Connected	Description
bport1	0x1000	F (False)	

Table 3. Bus Slave Port: bport1 Registers:

Name	Offset	Width (bits)	Description	R/W	is Volatile
ab_CESR	0x0	32			

ab_EAR0	0x10	32	Error Address Register, Slave Port n, array offset: 0x10, array step: 0x8		
ab_EDR0	0x14	32	Error Detail Register, Slave Port n, array offset: 0x14, array step: 0x8		
ab_EAR1	0x18	32	Error Address Register, Slave Port n, array offset: 0x10, array step: 0x8		
ab_EDR1	0x1c	32	Error Detail Register, Slave Port n, array offset: 0x14, array step: 0x8		
ab_EAR2	0x20	32	Error Address Register, Slave Port n, array offset: 0x10, array step: 0x8		
ab_EDR2	0x24	32	Error Detail Register, Slave Port n, array offset: 0x14, array step: 0x8		
ab_EAR3	0x28	32	Error Address Register, Slave Port n, array offset: 0x10, array step: 0x8		
ab_EDR3	0x2c	32	Error Detail Register, Slave Port n, array offset: 0x14, array step: 0x8		
ab_EAR4	0x30	32	Error Address Register, Slave Port n, array offset: 0x10, array step: 0x8		
ab_EDR4	0x34	32	Error Detail Register, Slave Port n, array offset: 0x14, array step: 0x8		
RGD0_WORD0	0x400	32	Region Descriptor		
RGD0_WORD1	0x404	32	Region Descriptor		
RGD0_WORD2	0x408	32	Region Descriptor		
RGD0_WORD3	0x40c	32	Region Descriptor		
RGD1_WORD0	0x410	32	Region Descriptor		
RGD1_WORD1	0x414	32	Region Descriptor		
RGD1_WORD2	0x418	32	Region Descriptor		
RGD1_WORD3	0x41c	32	Region Descriptor		
RGD2_WORD0	0x420	32	Region Descriptor		
RGD2_WORD1	0x424	32	Region Descriptor		
RGD2_WORD2	0x428	32	Region Descriptor		
RGD2_WORD3	0x42c	32	Region Descriptor		
RGD3_WORD0	0x430	32	Region Descriptor		
RGD3_WORD1	0x434	32	Region Descriptor		
RGD3_WORD2	0x438	32	Region Descriptor		
RGD3_WORD3	0x43c	32	Region Descriptor		
RGD4_WORD0	0x440	32	Region Descriptor		
RGD4_WORD1	0x444	32	Region Descriptor		
RGD4_WORD2	0x448	32	Region Descriptor		
RGD4_WORD3	0x44c	32	Region Descriptor		
RGD5_WORD0	0x450	32	Region Descriptor		
RGD5_WORD1	0x454	32	Region Descriptor		
RGD5_WORD2	0x458	32	Region Descriptor		

RGD5_WORD3	0x45c	32	Region Descriptor		
RGD6_WORD0	0x460	32	Region Descriptor		
RGD6_WORD1	0x464	32	Region Descriptor		
RGD6_WORD2	0x468	32	Region Descriptor		
RGD6_WORD3	0x46c	32	Region Descriptor		
RGD7_WORD0	0x470	32	Region Descriptor		
RGD7_WORD1	0x474	32	Region Descriptor		
RGD7_WORD2	0x478	32	Region Descriptor		
RGD7_WORD3	0x47c	32	Region Descriptor		
RGD8_WORD0	0x480	32	Region Descriptor		
RGD8_WORD1	0x484	32	Region Descriptor		
RGD8_WORD2	0x488	32	Region Descriptor		
RGD8_WORD3	0x48c	32	Region Descriptor		
RGD9_WORD0	0x490	32	Region Descriptor		
RGD9_WORD1	0x494	32	Region Descriptor		
RGD9_WORD2	0x498	32	Region Descriptor		
RGD9_WORD3	0x49c	32	Region Descriptor		
RGD10_WORD0	0x4a0	32	Region Descriptor		
RGD10_WORD1	0x4a4	32	Region Descriptor		
RGD10_WORD2	0x4a8	32	Region Descriptor		
RGD10_WORD3	0x4ac	32	Region Descriptor		
RGD11_WORD0	0x4b0	32	Region Descriptor		
RGD11_WORD1	0x4b4	32	Region Descriptor		
RGD11_WORD2	0x4b8	32	Region Descriptor		
RGD11_WORD3	0x4bc	32	Region Descriptor		
RGD12_WORD0	0x4c0	32	Region Descriptor		
RGD12_WORD1	0x4c4	32	Region Descriptor		
RGD12_WORD2	0x4c8	32	Region Descriptor		
RGD12_WORD3	0x4cc	32	Region Descriptor		
RGD13_WORD0	0x4d0	32	Region Descriptor		
RGD13_WORD1	0x4d4	32	Region Descriptor		
RGD13_WORD2	0x4d8	32	Region Descriptor		
RGD13_WORD3	0x4dc	32	Region Descriptor		
RGD14_WORD0	0x4e0	32	Region Descriptor		
RGD14_WORD1	0x4e4	32	Region Descriptor		
RGD14_WORD2	0x4e8	32	Region Descriptor		
RGD14_WORD3	0x4ec	32	Region Descriptor		
RGD15_WORD0	0x4f0	32	Region Descriptor		
RGD15_WORD1	0x4f4	32	Region Descriptor		
RGD15_WORD2	0x4f8	32	Region Descriptor		
RGD15_WORD3	0x4fc	32	Region Descriptor		
AAC_RGDAAC0	0xbc0	32	Region Descriptor Alternate Access Control		
AAC_RGDAAC1	0xbc4	32	Region Descriptor Alternate Access Control		
AAC_RGDAAC2	0xbc8	32	Region Descriptor Alternate Access Control		
AAC_RGDAAC3	0xbcc	32	Region Descriptor Alternate Access Control		

AAC_RGDAAC4	0xbd0	32	Region Descriptor Alternate Access Control		
AAC_RGDAAC5	0xbd4	32	Region Descriptor Alternate Access Control		
AAC_RGDAAC6	0xbd8	32	Region Descriptor Alternate Access Control		
AAC_RGDAAC7	0xbdc	32	Region Descriptor Alternate Access Control		
AAC_RGDAAC8	0xbe0	32	Region Descriptor Alternate Access Control		
AAC_RGDAAC9	0xbe4	32	Region Descriptor Alternate Access Control		
AAC_RGDAAC10	0xbe8	32	Region Descriptor Alternate Access Control		
AAC_RGDAAC11	0xbec	32	Region Descriptor Alternate Access Control		
AAC_RGDAAC12	0xbf0	32	Region Descriptor Alternate Access Control		
AAC_RGDAAC13	0xbf4	32	Region Descriptor Alternate Access Control		
AAC_RGDAAC14	0xbf8	32	Region Descriptor Alternate Access Control		
AAC_RGDAAC15	0xbfc	32	Region Descriptor Alternate Access Control		

4.0 Platforms that use this peripheral component

Peripheral components can be used in many different platforms, including those developed by Imperas or by other users of OVP. You can use this peripheral in your own platforms.

Table 4. Publicly available platforms using peripheral 'KinetisMPU'

Platform Name	Vendor
FreescaleKinetis60	freescale.ovpworld.org
FreescaleKinetis64	freescale.ovpworld.org

5.0 Peripheral components in the library

Table 5. Publicly available Imperas/OVP peripheral models (224 models)

Peripheral	Peripheral	Peripheral
freescale.ovpworld.org/KinetisNFC	freescale.ovpworld.org/KinetisOSC	freescale.ovpworld.org/KinetisPDB
freescale.ovpworld.org/KinetisPIT	freescale.ovpworld.org/KinetisPMC	freescale.ovpworld.org/KinetisPORT
freescale.ovpworld.org/KinetisRCM	freescale.ovpworld.org/KinetisRFSYS	freescale.ovpworld.org/KinetisRFVBAT
freescale.ovpworld.org/KinetisRNG	freescale.ovpworld.org/KinetisRTC	freescale.ovpworld.org/KinetisSDHC
freescale.ovpworld.org/KinetisSIM	freescale.ovpworld.org/KinetisSMC	freescale.ovpworld.org/KinetisSPI
freescale.ovpworld.org/KinetisTSI	freescale.ovpworld.org/KinetisUART	freescale.ovpworld.org/KinetisUSB
freescale.ovpworld.org/KinetisUSBDCD	freescale.ovpworld.org/KinetisUSBHS	freescale.ovpworld.org/KinetisVREF
freescale.ovpworld.org/KinetisWDOG	freescale.ovpworld.org/Uart	freescale.ovpworld.org/VybridADC
freescale.ovpworld.org/VybridANADIG	freescale.ovpworld.org/VybridCCM	freescale.ovpworld.org/VybridDMA
freescale.ovpworld.org/VybridGPIO	freescale.ovpworld.org/VybridI2C	freescale.ovpworld.org/VybridLCD
freescale.ovpworld.org/VybridQUADSPI	freescale.ovpworld.org/VybridSDHC	freescale.ovpworld.org/VybridSPI
freescale.ovpworld.org/VybridUART	freescale.ovpworld.org/VybridUSB	imperas.ovpworld.org/frameBuffer
imperas.ovpworld.org/uart	imperas.ovpworld.org/usecCounter	intel.ovpworld.org/82077AA
intel.ovpworld.org/82371EB	intel.ovpworld.org/8253	intel.ovpworld.org/8259A
intel.ovpworld.org/NorFlash48F4400	intel.ovpworld.org/PciIDE	intel.ovpworld.org/PciPM
intel.ovpworld.org/PciUSB	intel.ovpworld.org/Ps2Control	marvell.ovpworld.org/GT6412x
maxim.ovpworld.org/max673x	microsemi.ovpworld.org/CoreUARTapb	mips.ovpworld.org/16450C
mips.ovpworld.org/MaltaFPGA	mips.ovpworld.org/SmartLoaderLinux	motorola.ovpworld.org/MC146818
national.ovpworld.org/16450	national.ovpworld.org/16550	national.ovpworld.org/16550_4bytes
nxp.ovpworld.org/iMX6_Analog	nxp.ovpworld.org/iMX6_CCM	nxp.ovpworld.org/iMX6_GPC
nxp.ovpworld.org/iMX6_GPIO	nxp.ovpworld.org/iMX6_GPT	nxp.ovpworld.org/iMX6_MMDC
nxp.ovpworld.org/iMX6_SDHC	nxp.ovpworld.org/iMX6_SRC	nxp.ovpworld.org/iMX6_UART
nxp.ovpworld.org/iMX6_WDOG	ovpworld.org/Alpha2x16Display	ovpworld.org/DynamicBridge
ovpworld.org/FlashDevice	ovpworld.org/ledRegister	ovpworld.org/SerInt
ovpworld.org/SimpleDma	ovpworld.org/switchRegister	ovpworld.org/temperatureSensor
ovpworld.org/trap	ovpworld.org/trap4K	ovpworld.org/vEthernet_Bridge
ovpworld.org/VirtioBlkMMIO	ovpworld.org/VirtioNetMMIO	philips.ovpworld.org/ISP1761
renesas.ovpworld.org/adc	renesas.ovpworld.org/bcu	renesas.ovpworld.org/brg
renesas.ovpworld.org/can	renesas.ovpworld.org/can	renesas.ovpworld.org/clkgen
renesas.ovpworld.org/crc	renesas.ovpworld.org/csib	renesas.ovpworld.org/csie
renesas.ovpworld.org/dma	renesas.ovpworld.org/intc	renesas.ovpworld.org/memc
renesas.ovpworld.org/rng	renesas.ovpworld.org/taa	renesas.ovpworld.org/tms
renesas.ovpworld.org/tmt	renesas.ovpworld.org/uartc	renesas.ovpworld.org/UPD70F3441Logic
riscv.ovpworld.org/CLINT	riscv.ovpworld.org/PLIC	riscv.ovpworld.org/SmartLoaderRV64Linux
safepower.ovpworld.org/node	safepower.ovpworld.org/NostrumNode	safepower.ovpworld.org/ring_oscillator
safepower.ovpworld.org/TTELNode	sifive.ovpworld.org/gpio	sifive.ovpworld.org/MSEL
sifive.ovpworld.org/PRCI	sifive.ovpworld.org/pwm	sifive.ovpworld.org/spi
sifive.ovpworld.org/teststatus	sifive.ovpworld.org/UART	smsc.ovpworld.org/LAN9118
smsc.ovpworld.org/LAN91C111	ti.ovpworld.org/tca6416a	ti.ovpworld.org/UartInterface
ti.ovpworld.org/ucd9012a	ti.ovpworld.org/ucd9248	vendor.com/fifo
xilinx.ovpworld.org/axi-gpio	xilinx.ovpworld.org/axi-intc	xilinx.ovpworld.org/axi-pcie
xilinx.ovpworld.org/axi-timer	xilinx.ovpworld.org/logicore-fit	xilinx.ovpworld.org/mdm
xilinx.ovpworld.org/mpmc	xilinx.ovpworld.org/xps-gpio	xilinx.ovpworld.org/xps-iic

xilinx.ovpworld.org/xps-intc	xilinx.ovpworld.org/xps-ll-temac	xilinx.ovpworld.org/xps-mch-emc
xilinx.ovpworld.org/xps-sysace	xilinx.ovpworld.org/xps-timer	xilinx.ovpworld.org/xps-uartlite
xilinx.ovpworld.org/zynq_7000-can	xilinx.ovpworld.org/zynq_7000-ddrc	xilinx.ovpworld.org/zynq_7000-devcfg
xilinx.ovpworld.org/zynq_7000-dmac	xilinx.ovpworld.org/zynq_7000-gpio	xilinx.ovpworld.org/zynq_7000-iic
xilinx.ovpworld.org/zynq_7000-ocm	xilinx.ovpworld.org/zynq_7000-qos301	xilinx.ovpworld.org/zynq_7000-qspi
xilinx.ovpworld.org/zynq_7000-sdio	xilinx.ovpworld.org/zynq_7000-slcr	xilinx.ovpworld.org/zynq_7000-spi
xilinx.ovpworld.org/zynq_7000-swdt	xilinx.ovpworld.org/zynq_7000-ttc	xilinx.ovpworld.org/zynq_7000-tz_GPVsecurity
xilinx.ovpworld.org/zynq_7000-tz_security	xilinx.ovpworld.org/zynq_7000-usb	altera.ovpworld.org/dw-apb-timer
altera.ovpworld.org/dw-apb-uart	altera.ovpworld.org/IntervalTimer32Core	altera.ovpworld.org/IntervalTimer64Core
altera.ovpworld.org/JtagUart	altera.ovpworld.org/PerformanceCounterCore	altera.ovpworld.org/RSTMGR
altera.ovpworld.org/SystemIDCore	altera.ovpworld.org/Uart	amd.ovpworld.org/79C970
andes.ovpworld.org/ATCUART100	andes.ovpworld.org/NCEPLIC100	andes.ovpworld.org/NCEPLMT100
arm.ovpworld.org/AaciPL041	arm.ovpworld.org/CompactFlashRegs	arm.ovpworld.org/CoreModule9x6
arm.ovpworld.org/DebugLedAndDipSwitch	arm.ovpworld.org/DMemCtrlPL341	arm.ovpworld.org/IcpControl
arm.ovpworld.org/IcpCounterTimer	arm.ovpworld.org/IntICP	arm.ovpworld.org/IntICP
arm.ovpworld.org/KbPL050	arm.ovpworld.org/L2CachePL310	arm.ovpworld.org/LcdPL110
arm.ovpworld.org/MmciPL181	arm.ovpworld.org/RtcPL031	arm.ovpworld.org/SerBusDviRegs
arm.ovpworld.org/SmartLoaderArm64Linux	arm.ovpworld.org/SmartLoaderArmLinux	arm.ovpworld.org/SMemCtrlPL354
arm.ovpworld.org/SysCtrlSP810	arm.ovpworld.org/TimerSP804	arm.ovpworld.org/TzpcBP147
arm.ovpworld.org/UartPL011	arm.ovpworld.org/VexpressSysRegs	arm.ovpworld.org/WdtSP805
atmel.ovpworld.org/AdvancedInterruptController	atmel.ovpworld.org/ParallelIOController	atmel.ovpworld.org/PowerSaving
atmel.ovpworld.org/SpecialFunction	atmel.ovpworld.org/TimerCounter	atmel.ovpworld.org/UsartInterface
atmel.ovpworld.org/WatchdogTimer	cadence.ovpworld.org/gem	cadence.ovpworld.org/uart
cirrus.ovpworld.org/GD5446	freescale.ovpworld.org/KinetisADC	freescale.ovpworld.org/KinetisAIPS
freescale.ovpworld.org/KinetisAXBS	freescale.ovpworld.org/KinetisCAN	freescale.ovpworld.org/KinetisCMP
freescale.ovpworld.org/KinetisCMT	freescale.ovpworld.org/KinetisCRC	freescale.ovpworld.org/KinetisDAC
freescale.ovpworld.org/KinetisDDR	freescale.ovpworld.org/KinetisDMA	freescale.ovpworld.org/KinetisDMAC
freescale.ovpworld.org/KinetisDMAMUX	freescale.ovpworld.org/KinetisENET	freescale.ovpworld.org/KinetisEWM
freescale.ovpworld.org/KinetisFB	freescale.ovpworld.org/KinetisFMC	freescale.ovpworld.org/KinetisFTFE
freescale.ovpworld.org/KinetisFTM	freescale.ovpworld.org/KinetisGPIO	freescale.ovpworld.org/KinetisI2C
freescale.ovpworld.org/KinetisI2S	freescale.ovpworld.org/KinetisLLWU	freescale.ovpworld.org/KinetisLPTMR
freescale.ovpworld.org/KinetisMCG	freescale.ovpworld.org/KinetisMPU	

6.0 General Information on Peripheral Models

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers etc. and configuration options and general information for peripheral modeling with Imperas OVP.

6.1 Background

Imperas OVP simulation technology enables very high performance simulation, debug and analysis of platforms containing multiple processors and peripheral models. The technology is designed to be extensible: you can create new models of processors, peripherals and other platform components using interfaces and libraries defined by OVP.

The peripheral models created using the OVP APIs run on the Peripheral Simulation Engine (PSE).

The model is typically written in C and compiled into an executable for the PSE processor architecture. The model is compiled for speed of execution and to protect IP. It is dynamically loaded by the simulator at run time.

7.0 Building peripherals easily with Imperas iGen

To aid with model creation, Imperas products include iGen, a model generation tool. iGen takes the laborious and error-prone task of constructing the various hardware model and software element files required for a typical model, and automates this process. iGen creates the needed C files. iGen also creates the C++ SystemC TLM2 interface files needed to run peripheral models in SystemC simulations.

iGen takes as input a simple script specification that includes device internals such as registers and memories, port information, component descriptors, and other elements. iGen then builds the C code model files and user editable templates. These include model frameworks with registers, function calls, memory map, and other items. It ensures that all component parts of the model are well-structured using best practices, and are consistent throughout the files, thus eliminating a common source of errors.

More information on iGen can be found: imperas.com/products.

8.0 Peripheral model internals

Each instance of a peripheral model runs on its own virtual machine with an address space large enough for the model. This processor (the PSE) and its memory are separate from any processors, memories and buses in the platform being simulated; they exist only to execute the code of the peripheral model.

Interception of functions defined in the peripheral model allows the use of features of the host system in the

implementation of the behavior of a peripheral. As an example, a real platform might contain a video display device. When simulating this system, it is generally more convenient not to simulate the complete video display device but to use a video package available on the host machine, such as SDL, and to use this to render to the host display. Also models of uarts, ethernet devices and USB components can make use of the host PC resources during simulation, to allow, for example, a simulation to browse the real internet, or the simulation to connect to a real USB device.

9.0 Parts of peripheral models

9.1 Configuring the Peripheral Instance with Parameters

A peripheral can include the behaviour of several configurations. These are controlled when the peripheral is instanced in the platform by setting parameters defined on the peripheral.

9.2 Net Ports

Peripherals may be connected to other peripherals or processors with signal wires (nets). These can be used to act as interrupt signals or used to control behavior between peripherals.
The wires are created in the platform as nets and this net is connected into the peripheral using a net port.

9.3 Bus master ports

A bus master port initiates (and controls the address of) a bus cycle. Bus cycles are generated by behavioral code within the peripheral model.

9.4 Bus slave ports

A peripheral can be defined as having several bus slave ports. The bus slave ports can be split into several address blocks. Each address block be either local memory or memory mapped registers. Both of these can have associated callback functions. A memory mapped register can also be defined as specific read/write access, whether it is volatile, and also whether it is associated with a reset pin and mask. A memory mapped register can also have specific bit fields defined.

9.5 Packetnets

A peripheral can be defined as being connected to packetnet ports. A packetnet is used to model packet based communication such as Ethernet, CAN bus or GSM. A packetnet is created in a platform, then connected to packetnet ports on model instances. A packetnet can have many connections, each able to send or receive packets. A packetnet is used as an efficient method of communication within OVP models.

For more information on modeling with packetnets, please see the peripheral modeling documentation: OVP_Peripheral_Modeling_Guide.pdf, OVPsim_and_CpuManager_User_Guide.pdf and the example: $IMPERAS_HOME/Examples/Models/Peripherals/packetnet.

10.0 More information (documentation) on peripheral models and modeling

More information on modeling and APIs can be found at: OVPworld.org/technology_apis.

Specifics on modeling peripherals can be found: OVP_Peripheral_Modeling_Guide.pdf.

A full list of the currently available OVP documentation is available: OVPworld.org/documentation.
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