

OVP Guide to Using Processor Models

Model specific information for ARM_MultiCluster

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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

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Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.

The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners. There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

This model implements an ARM system containing clusters of MPCore processors communicating using a common GICv2 or GICv3 block.

By default, the system contains Cortex-A53MPx4 and Cortex-A57MPx4 clusters, but this can be changed using parameter "override_clusterVariants". This parameter is a comma-separated list of cluster components (e.g. "Cortex-A53MPx4,Cortex-A57MPx4"). Note that if a GICv2 is selected, the total number of PEs must not exceed 8.

1.2 Licensing

This document describes the interface to the MultiCluster only. Refer to documentation of individual clusters for information regarding implemented features, licensing and limitations.

1.3 Limitations

1.4 Features

By default, the model implements a GICv2. Parameter enable GICv3 can be used to select a GICv3 instead.

Configuration

2.1 Location

This model's VLNV is arm.ovpworld.org/processor/arm/1.0.
The model source is usually at:
\$IMPERAS_HOME/ImperasLib/source/arm.ovpworld.org/processor/arm/1.0
The model binary is usually at:
\$IMPERAS_HOME/lib/\$IMPERAS_ARCH/ImperasLib/arm.ovpworld.org/processor/arm/1.0

2.2 Asymmetric Multicore Processor

This processor contains more than one core of differing architectures

All Variants in this model

This model has these variants

Variant	Description
ARMv4T	
ARMv4xM	
ARMv4	
ARMv4TxM	
ARMv5xM	
ARMv5	
ARMv5TxM	
ARMv5T	
ARMv5TExP	
ARMv5TE	
ARMv5TEJ	
ARMv6	
ARMv6K	
ARMv6T2	
ARMv6KZ	
ARMv7	
ARM7TDMI	
ARM7EJ-S	
ARM720T	
ARM920T	
ARM922T	
ARM926EJ-S	
ARM940T	
ARM946E	
ARM966E	
ARM968E-S	
ARM1020E	
ARM1022E	
ARM1026EJ-S	
ARM1136J-S	
ARM1156T2-S	

	7
ARM1176JZ-S	
Cortex-R4	
Cortex-R4F	
Cortex-A5UP	
Cortex-A5MPx1	
Cortex-A5MPx2	
Cortex-A5MPx3	
Cortex-A5MPx4	
Cortex-A8	
Cortex-A9UP	
Cortex-A9MPx1	
Cortex-A9MPx2	
Cortex-A9MPx3	
Cortex-A9MPx4	
Cortex-A7UP	
Cortex-A7MPx1	
Cortex-A7MPx2	
Cortex-A7MPx3	
Cortex-A7MPx4	
Cortex-A15UP	
Cortex-A15MPx1	
Cortex-A15MPx2	
Cortex-A15MPx3	
Cortex-A15MPx4	
Cortex-A17MPx1	
Cortex-A17MPx2	
Cortex-A17MPx3	
Cortex-A17MPx4	
AArch32	
AArch64	
Cortex-A32MPx1	
Cortex-A32MPx2	
Cortex-A32MPx3	
Cortex-A32MPx4	
Cortex-A35MPx1	
Cortex-A35MPx2	
Cortex-A35MPx3	
Cortex-A35MPx4	
Cortex-A53MPx1	
Cortex-A53MPx2	
Cortex-A53MPx3	
Cortex-A53MPx4	
Cortex-A55MPx1	
Cortex-A55MPx2	
Cortex-A55MPx3	

Cortex-A55MPx4	
Cortex-A57MPx1	
Cortex-A57MPx2	
Cortex-A57MPx3	
Cortex-A57MPx4	
Cortex-A72MPx1	
Cortex-A72MPx2	
Cortex-A72MPx3	
Cortex-A72MPx4	
Cortex-A73MPx1	
Cortex-A73MPx2	
Cortex-A73MPx3	
Cortex-A73MPx4	
Cortex-A75MPx1	
Cortex-A75MPx2	
Cortex-A75MPx3	
Cortex-A75MPx4	
MultiCluster	(described in this document)

Table 3.1: All Variants in this model

Bus Master Ports

This model has these bus master ports.

Name	min	max	Connect?	Description
INSTRUCTION	32	53	mandatory	
DATA	32	53	optional	
GICRegisters	32	32	optional	GIC memory-mapped register block

Table 4.1: Bus Master Ports

Bus Slave Ports

This model has no bus slave ports.

Net Ports

This model has these net ports.

Name	Type	Connect?	Description
SPI32	input	optional	Shared peripheral interrupt
SPI33	input	optional	Shared peripheral interrupt
SPI34	input	optional	Shared peripheral interrupt
SPI35	input	optional	Shared peripheral interrupt
SPI36	input	optional	Shared peripheral interrupt
SPI37	input	optional	Shared peripheral interrupt
SPI38	input	optional	Shared peripheral interrupt
SPI39	input	optional	Shared peripheral interrupt
SPI40	input	optional	Shared peripheral interrupt
SPI41	input	optional	Shared peripheral interrupt
SPI42	input	optional	Shared peripheral interrupt
SPI43	input	optional	Shared peripheral interrupt
SPI44	input	optional	Shared peripheral interrupt
SPI45	input	optional	Shared peripheral interrupt
SPI46	input	optional	Shared peripheral interrupt
SPI47	input	optional	Shared peripheral interrupt
SPI48	input	optional	Shared peripheral interrupt
SPI49	input	optional	Shared peripheral interrupt
SPI50	input	optional	Shared peripheral interrupt
SPI51	input	optional	Shared peripheral interrupt
SPI52	input	optional	Shared peripheral interrupt
SPI53	input	optional	Shared peripheral interrupt
SPI54	input	optional	Shared peripheral interrupt
SPI55	input	optional	Shared peripheral interrupt
SPI56	input	optional	Shared peripheral interrupt
SPI57	input	optional	Shared peripheral interrupt
SPI58	input	optional	Shared peripheral interrupt
SPI59	input	optional	Shared peripheral interrupt
SPI60	input	optional	Shared peripheral interrupt
SPI61	input	optional	Shared peripheral interrupt
SPI62	input	optional	Shared peripheral interrupt

CDIAO	Ι	1	
SPI63	input	optional	Shared peripheral interrupt
SPI64	input	optional	Shared peripheral interrupt
SPI65	input	optional	Shared peripheral interrupt
SPI66	input	optional	Shared peripheral interrupt
SPI67	input	optional	Shared peripheral interrupt
SPI68	input	optional	Shared peripheral interrupt
SPI69	input	optional	Shared peripheral interrupt
SPI70	input	optional	Shared peripheral interrupt
SPI71	input	optional	Shared peripheral interrupt
SPI72	input	optional	Shared peripheral interrupt
SPI73	input	optional	Shared peripheral interrupt
SPI74	input	optional	Shared peripheral interrupt
SPI75	input	optional	Shared peripheral interrupt
SPI76	input	optional	Shared peripheral interrupt
SPI77	input	optional	Shared peripheral interrupt
SPI78	input	optional	Shared peripheral interrupt
SPI79	input	optional	Shared peripheral interrupt
SPI80	input	optional	Shared peripheral interrupt
SPI81	input	optional	Shared peripheral interrupt
SPI82	input	optional	Shared peripheral interrupt
SPI83	input	optional	Shared peripheral interrupt
SPI84	input	optional	Shared peripheral interrupt
SPI85	input	optional	Shared peripheral interrupt
SPI86	input	optional	Shared peripheral interrupt
SPI87	input	optional	Shared peripheral interrupt
SPI88	input	optional	Shared peripheral interrupt
SPI89	input	optional	Shared peripheral interrupt
SPI90	input	optional	Shared peripheral interrupt
SPI91	input	optional	Shared peripheral interrupt
SPI92	input	optional	Shared peripheral interrupt
SPI93	input	optional	Shared peripheral interrupt
SPI94	input	optional	Shared peripheral interrupt
SPI95	input	optional	Shared peripheral interrupt
SPIVector	input	optional	Shared peripheral interrupt vectorized in-
		_	put
periphReset	input	optional	Peripheral reset (active high)
CFGSDISABLE	input	optional	Secure configuration lockdown (active
			high)
GICCDISABLE	input	optional	GIC CPU interface logic disable (active
			high, sampled on rising edge of periphRe-
			set)
EVENTI	input	optional	Event input signal, active on rising edge
EVENTO	output	optional	Event output signal, active on rising edge
PPI16_C0_0	input	optional	Private peripheral interrupt
PPI17_C0_0	input	optional	Private peripheral interrupt

wasi CO O	innut	ontional	Vintual greature amon interment active as
vsei_C0_0	input	optional	Virtual system error interrupt, active on
AVI CLUEDD CO O	. ,	4. 1	rising edge (negation of nVSEI)
AXI_SLVERR_C0_0	input	optional	AXI external abort type (DECERR=0,
	:	4:1	SLVERR=1)
CP15SDISABLE_C0_0	input	optional	CP15SDISABLE (active high)
PMUIRQ_C0_0	output	optional	Performance monitor event (active high)
SMPEN_C0_0	output	optional	CPUECTLR.SMPEN current value
PPI16_C0_1	input	optional	Private peripheral interrupt
PPI17_C0_1	input	optional	Private peripheral interrupt
PPI18_C0_1	input	optional	Private peripheral interrupt
PPI19_C0_1	input	optional	Private peripheral interrupt
PPI20_C0_1	input	optional	Private peripheral interrupt
PPI21_C0_1	input	optional	Private peripheral interrupt
PPI22_C0_1	input	optional	Private peripheral interrupt
PPI23_C0_1	input	optional	Private peripheral interrupt
PPI24_C0_1	input	optional	Private peripheral interrupt
PPI25_C0_1	input	optional	Private peripheral interrupt
PPI26_C0_1	input	optional	Private peripheral interrupt
PPI27_C0_1	input	optional	Private peripheral interrupt
PPI28_C0_1	input	optional	Private peripheral interrupt
PPI29_C0_1	input	optional	Private peripheral interrupt
PPI30_C0_1	input	optional	Private peripheral interrupt
PPI31_C0_1	input	optional	Private peripheral interrupt
CNTVIRQ_C0_1	output	optional	Virtual timer event (active high)
CNTPSIRQ_C0_1	output	optional	Secure physical timer event (active high)
CNTPNSIRQ_C0_1	output	optional	Non-secure physical timer event (active
•		_	high)
CNTPHPIRQ_C0_1	output	optional	Hypervisor physical timer event (active
_	_	_	high)
IRQOUT_C0_1	output	optional	IRQ wakeup
FIQOUT_C0_1	output	optional	FIQ wakeup
RVBARADDRx_C0_1	input	optional	Configure AArch64 Reset Vector Base Ad-
	1	1	dress at reset
AA64nAA32_C0_1	input	optional	Register width state at reset
VINITHI_C0_1	input	optional	Configure HIVECS mode (SCTLR.V)
CFGEND_C0_1	input	optional	Configure exception endianness
	III G	op monar	(SCTLR.EE)
CFGTE_C0_1	input	optional	Configure exception state at reset
			(SCTLR.TE)
reset_C0_1	input	optional	Processor reset, active high
$fiq_{-}C0_{-}1$	input	optional	FIQ interrupt, active high (negation of
			nFIQ)
irq_C0_1	input	optional	IRQ interrupt, active high (negation of
			nIRQ)

sei_C0_1	input	optional	System error interrupt, active on rising
		_	edge (negation of nSEI)
vfiq_C0_1	input	optional	Virtual FIQ interrupt, active high (nega-
•		1	tion of nVFIQ)
virq_C0_1	input	optional	Virtual IRQ interrupt, active high (nega-
4		· F	tion of nVIRQ)
vsei_C0_1	input	optional	Virtual system error interrupt, active on
	1	1	rising edge (negation of nVSEI)
AXI_SLVERR_C0_1	input	optional	AXI external abort type (DECERR=0,
	in par	орогона	SLVERR=1)
CP15SDISABLE_C0_1	input	optional	CP15SDISABLE (active high)
PMUIRQ_C0_1	output	optional	Performance monitor event (active high)
SMPEN_C0_1	output	optional	CPUECTLR.SMPEN current value
PPI16_C0_2	input	optional	Private peripheral interrupt
PPI17_C0_2	input	optional	Private peripheral interrupt
PPI18_C0_2	input	optional	Private peripheral interrupt
PPI19_C0_2	input	optional	Private peripheral interrupt
PPI20_C0_2	input	optional	Private peripheral interrupt
PPI21_C0_2	input	optional	Private peripheral interrupt
PPI22_C0_2	input	optional	Private peripheral interrupt
PPI23_C0_2	input	optional	Private peripheral interrupt
PPI24_C0_2	input	optional	Private peripheral interrupt
PPI25_C0_2	input	optional	Private peripheral interrupt
PPI26_C0_2	input	optional	Private peripheral interrupt
PPI27_C0_2	input	optional	Private peripheral interrupt
PPI28_C0_2	input	optional	Private peripheral interrupt
PPI29_C0_2	input	optional	Private peripheral interrupt
PPI30_C0_2	input	optional	Private peripheral interrupt
PPI31_C0_2	input	optional	Private peripheral interrupt
CNTVIRQ_C0_2	output	optional	Virtual timer event (active high)
CNTPSIRQ_C0_2	output	optional	Secure physical timer event (active high)
CNTPNSIRQ_C0_2	output	optional	Non-secure physical timer event (active
	1	1	high)
CNTPHPIRQ_C0_2	output	optional	Hypervisor physical timer event (active
	1	1	high)
IRQOUT_C0_2	output	optional	IRQ wakeup
FIQOUT_C0_2	output	optional	FIQ wakeup
RVBARADDRx_C0_2	input	optional	Configure AArch64 Reset Vector Base Ad-
-		* **	dress at reset
AA64nAA32_C0_2	input	optional	Register width state at reset
VINITHI_C0_2	input	optional	Configure HIVECS mode (SCTLR.V)
CFGEND_C0_2	input	optional	Configure exception endianness
		*	(SCTLR.EE)
CFGTE_C0_2	input	optional	Configure exception state at reset
	1 1	_	(SCTLR.TE)

reset_C0_2	input	optional	Processor reset, active high
fiq_C0_2	input	optional	FIQ interrupt, active high (negation of
•	1	•	nFIQ)
irq_C0_2	input	optional	IRQ interrupt, active high (negation of
_	_	_	nIRQ)
sei_C0_2	input	optional	System error interrupt, active on rising
			edge (negation of nSEI)
vfiq_C0_2	input	optional	Virtual FIQ interrupt, active high (nega-
			tion of nVFIQ)
virq_C0_2	input	optional	Virtual IRQ interrupt, active high (nega-
			tion of nVIRQ)
vsei_C0_2	input	optional	Virtual system error interrupt, active on
			rising edge (negation of nVSEI)
AXI_SLVERR_C0_2	input	optional	AXI external abort type (DECERR=0,
			SLVERR=1)
CP15SDISABLE_C0_2	input	optional	CP15SDISABLE (active high)
PMUIRQ_C0_2	output	optional	Performance monitor event (active high)
SMPEN_C0_2	output	optional	CPUECTLR.SMPEN current value
PPI16_C0_3	input	optional	Private peripheral interrupt
PPI17_C0_3	input	optional	Private peripheral interrupt
PPI18_C0_3	input	optional	Private peripheral interrupt
PPI19_C0_3	input	optional	Private peripheral interrupt
PPI20_C0_3	input	optional	Private peripheral interrupt
PPI21_C0_3	input	optional	Private peripheral interrupt
PPI22_C0_3	input	optional	Private peripheral interrupt
PPI23_C0_3	input	optional	Private peripheral interrupt
PPI24_C0_3	input	optional	Private peripheral interrupt
PPI25_C0_3	input	optional	Private peripheral interrupt
PPI26_C0_3	input	optional	Private peripheral interrupt
PPI27_C0_3	input	optional	Private peripheral interrupt
PPI28_C0_3	input	optional	Private peripheral interrupt
PPI29_C0_3	input	optional	Private peripheral interrupt
PPI30_C0_3	input	optional	Private peripheral interrupt
PPI31_C0_3	input	optional	Private peripheral interrupt
CNTVIRQ_C0_3	output	optional	Virtual timer event (active high)
CNTPSIRQ_C0_3	output	optional	Secure physical timer event (active high)
CNTPNSIRQ_C0_3	output	optional	Non-secure physical timer event (active
			high)
CNTPHPIRQ_C0_3	output	optional	Hypervisor physical timer event (active
			high)
IRQOUT_C0_3	output	optional	IRQ wakeup
FIQOUT_C0_3	output	optional	FIQ wakeup
RVBARADDRx_C0_3	input	optional	Configure AArch64 Reset Vector Base Ad-
			dress at reset
AA64nAA32_C0_3	input	optional	Register width state at reset

VINITHI_C0_3	input	optional	Configure HIVECS mode (SCTLR.V)
CFGEND_C0_3	input	optional	Configure exception endianness
			(SCTLR.EE)
CFGTE_C0_3	input	optional	Configure exception state at reset
			(SCTLR.TE)
reset_C0_3	input	optional	Processor reset, active high
fiq_C0_3	input	optional	FIQ interrupt, active high (negation of
			nFIQ)
irq_C0_3	input	optional	IRQ interrupt, active high (negation of
			nIRQ)
sei_C0_3	input	optional	System error interrupt, active on rising
			edge (negation of nSEI)
vfiq_C0_3	input	optional	Virtual FIQ interrupt, active high (nega-
			tion of nVFIQ)
virq_C0_3	input	optional	Virtual IRQ interrupt, active high (nega-
			tion of nVIRQ)
vsei_C0_3	input	optional	Virtual system error interrupt, active on
			rising edge (negation of nVSEI)
AXI_SLVERR_C0_3	input	optional	AXI external abort type (DECERR=0,
			SLVERR=1)
CP15SDISABLE_C0_3	input	optional	CP15SDISABLE (active high)
PMUIRQ_C0_3	output	optional	Performance monitor event (active high)
SMPEN_C0_3	output	optional	CPUECTLR.SMPEN current value
PPI16_C1_0	input	optional	Private peripheral interrupt
PPI17_C1_0	input	optional	Private peripheral interrupt
PPI18_C1_0	input	optional	Private peripheral interrupt
PPI19_C1_0	input	optional	Private peripheral interrupt
PPI20_C1_0	input	optional	Private peripheral interrupt
PPI21_C1_0	input	optional	Private peripheral interrupt
PPI22_C1_0	input	optional	Private peripheral interrupt
PPI23_C1_0	input	optional	Private peripheral interrupt
PPI24_C1_0	input	optional	Private peripheral interrupt
PPI25_C1_0	input	optional	Private peripheral interrupt
PPI26_C1_0	input	optional	Private peripheral interrupt
PPI27_C1_0	input	optional	Private peripheral interrupt
PPI28_C1_0	input	optional	Private peripheral interrupt
PPI29_C1_0	input	optional	Private peripheral interrupt
PPI30_C1_0	input	optional	Private peripheral interrupt
PPI31_C1_0	input	optional	Private peripheral interrupt
CNTVIRQ_C1_0	output	optional	Virtual timer event (active high)
CNTPSIRQ_C1_0	output	optional	Secure physical timer event (active high)
CNTPNSIRQ_C1_0	output	optional	Non-secure physical timer event (active
			high)
CNTPHPIRQ_C1_0	output	optional	Hypervisor physical timer event (active
			high)

IRQOUT_C1_0	output	optional	IRQ wakeup
FIQOUT_C1_0	output	optional	FIQ wakeup
CLUSTERIDAFF1_C1	input	optional	Configure MPIDR.Aff1
CLUSTERIDAFF2_C1	input	optional	Configure MPIDR.Aff2
CLUSTERIDAFF3_C1	input	optional	Configure MPIDR.Aff3
RVBARADDRx_C1_0	input	optional	Configure AArch64 Reset Vector Base Ad-
	1	•	dress at reset
AA64nAA32_C1_0	input	optional	Register width state at reset
VINITHI_C1_0	input	optional	Configure HIVECS mode (SCTLR.V)
CFGEND_C1_0	input	optional	Configure exception endianness
			(SCTLR.EE)
CFGTE_C1_0	input	optional	Configure exception state at reset (SCTLR.TE)
reset_C1_0	input	optional	Processor reset, active high
fiq_C1_0	input	optional	FIQ interrupt, active high (negation of
			nFIQ)
irq_C1_0	input	optional	IRQ interrupt, active high (negation of
			nIRQ)
sei_C1_0	input	optional	System error interrupt, active on rising
			edge (negation of nSEI)
vfiq_C1_0	input	optional	Virtual FIQ interrupt, active high (nega-
			tion of nVFIQ)
virq_C1_0	input	optional	Virtual IRQ interrupt, active high (nega-
			tion of nVIRQ)
vsei_C1_0	input	optional	Virtual system error interrupt, active on
A WI GILLED D. Ct. o			rising edge (negation of nVSEI)
AXI_SLVERR_C1_0	input	optional	AXI external abort type (DECERR=0,
CD4FCDICADI E C1 0		1	SLVERR=1)
CP15SDISABLE_C1_0	input	optional	CP15SDISABLE (active high)
PMUIRQ_C1_0	output	optional	Performance monitor event (active high)
SMPEN_C1_0	output	optional	CPUECTLR.SMPEN current value
PPI16_C1_1	input	optional	Private peripheral interrupt
PPI17_C1_1	input	optional	Private peripheral interrupt
PPI18_C1_1	input	optional	Private peripheral interrupt
PPI19_C1_1	input	optional	Private peripheral interrupt
PPI20_C1_1	input	optional	Private peripheral interrupt
PPI21_C1_1 PPI22_C1_1	input	optional	Private peripheral interrupt
PPI22_C1_1 PPI23_C1_1	input	optional optional	Private peripheral interrupt Private peripheral interrupt
PPI23_C1_1 PPI24_C1_1	input	optional	Private peripheral interrupt Private peripheral interrupt
PPI24_C1_1 PPI25_C1_1	input		
PPI25_C1_1 PPI26_C1_1	input	optional	Private peripheral interrupt Private peripheral interrupt
PPI26_C1_1 PPI27_C1_1	input	optional	Private peripheral interrupt Private peripheral interrupt
PPI27_C1_1 PPI28_C1_1	input	optional optional	Private peripheral interrupt Private peripheral interrupt
PPI28_C1_1 PPI29_C1_1	input	_	
FF129_U1_1	input	optional	Private peripheral interrupt

Prist.Cl.1 input optional Private peripheral interrupt CNTVIRQ.Cl.1 output optional Virtual timer event (active high) CNTPNSIRQ.Cl.1 output optional Non-secure physical timer event (active high) CNTPNSIRQ.Cl.1 output optional Non-secure physical timer event (active high) CNTPNSIRQ.Cl.1 output optional Hypervisor physical timer event (active high) IRQOUT.Cl.1 output optional IRQ wakeup FIQUIT Cl.1 output optional FIQ wakeup FIQUIT Cl.1 input optional Private peripheral interrupt FIQUIT Cl.1 input optional Configure AArch64 Reset Vector Base Address at reset AA64nAA32.Cl.1 input optional Configure exception endianness (SCTLR.EE) CFGEND.Cl.1 input optional Configure exception state at reset (SCTLR.TE) reset.Cl.1 input optional FIQ interrupt, active high (negation of nFIQ) req.Cl.1 input optional FIQ interrupt, active high (negation of nFIQ) virq.Cl.1 input optional Virtual FIQ interrupt, active high (negation of nVFIQ) virq.Cl.1 input optional Virtual IRQ interrupt, active high (negation of nVFIQ) virq.Cl.1 input optional Virtual System error interrupt, active on rising edge (negation of nVFIQ) virq.Cl.1 input optional Virtual System error interrupt, active on rising edge (negation of nVFIQ) virq.Cl.1 input optional Virtual System error interrupt, active on rising edge (negation of nVFIQ) virq.Cl.1 input optional Virtual System error interrupt, active on rising edge (negation of nVFIQ) virq.Cl.1 input optional Virtual System error interrupt, active on rising edge (negation of nVFIQ) virq.Cl.1 input optional Private peripheral interrupt PPIIO.Cl.2 input o	PPI30_C1_1	innut	ontional	Private peripheral interrupt
CNTVIRQ_C1_1		input	optional	= = =
CNTPSIRQ.C1.1 output optional Secure physical timer event (active high) CNTPNSIRQ.C1.1 output optional high) RVBARADDRX.C1.1 output optional FIQ wakeup RVBARADDRX.C1.1 input optional Register width state at reset VINITHI.C1.1 input optional Configure AArch64 Reset Vector Base Address at reset VINITHI.C1.1 input optional Configure HIVECS mode (SCTLR.V) CFGEND.C1.1 input optional Configure exception endianness (SCTLR.EE) CFGTE.C1.1 input optional FIQ interrupt, active high (negation of nFIQ) irq.C1.1 input optional FIQ interrupt, active high (negation of nFIQ) reset.C1.1 input optional FIQ interrupt, active high (negation of nFIQ) reset.C1.1 input optional System error interrupt, active on rising edge (negation of nSEI) vfiq.C1.1 input optional Virtual FIQ interrupt, active high (negation of nVFIQ) vrq.C1.1 input optional Virtual System error interrupt, active on rising edge (negation of nVFIQ) vrq.C1.1 input optional Virtual System error interrupt, active on rising edge (negation of nVFIQ) vrq.C1.1 input optional Virtual System error interrupt, active on rising edge (negation of nVFIQ) vrq.C1.1 input optional Virtual System error interrupt, active on rising edge (negation of nVFIQ) vrq.C1.1 input optional Virtual System error interrupt, active on rising edge (negation of nVFIQ) vrq.C1.1 input optional Private peripheral interrupt PMURQ.C1.1 output optional Private peripheral interrupt PPH16.C1.2 input optional Private peripheral interrupt PPH17.C1.2 input optional Private peripheral interrupt PPH19.C1.2 input optional Private peripheral interrupt PPH20.C1.2 input optional Private peripheral interrupt PPH21.C1.2 input optional Private peripheral interrupt PPH21.C1.2 input optional Private peripheral interrupt PPH22.C1.2 input optional Private peripheral interrupt PPH23.C1.2 input optional Private peripheral interrupt PPH23.C1.2 input optional Private peripheral interrupt PPH23.C1.2 input optional Private peripheral interrupt				
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RQOUT_C1_1 output optional IRQ wakeup	CNTPHPIRQ_C1_1	output	optional	
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PPI21_C1_2 input optional Private peripheral interrupt PPI22_C1_2 input optional Private peripheral interrupt PPI23_C1_2 input optional Private peripheral interrupt PPI24_C1_2 input optional Private peripheral interrupt PPI24_C1_2 input optional Private peripheral interrupt		input	optional	Private peripheral interrupt
PPI22_C1_2 input optional Private peripheral interrupt PPI23_C1_2 input optional Private peripheral interrupt PPI24_C1_2 input optional Private peripheral interrupt	PPI20_C1_2	input	optional	Private peripheral interrupt
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PPI23_C1_2 input optional Private peripheral interrupt PPI24_C1_2 input optional Private peripheral interrupt	PPI22_C1_2	input	optional	
PPI24_C1_2 input optional Private peripheral interrupt	PPI23_C1_2	_		
	PPI24_C1_2	_		
	PPI25_C1_2	_	optional	Private peripheral interrupt

PPI26.C1.2 input optional Private peripheral interrupt PPI27.C1.2 input optional Private peripheral interrupt PPI29.C1.2 input optional Private peripheral interrupt PPI29.C1.2 input optional Private peripheral interrupt PPI30.C1.2 input optional Private peripheral interrupt PPI30.C1.2 input optional Private peripheral interrupt PPI31.C1.2 input optional Private peripheral interrupt PPI31.C1.2 input optional Private peripheral interrupt CNTVIRQ.C1.2 output optional Private peripheral interrupt CNTPSIRQ.C1.2 output optional Secure physical timer event (active high) CNTPNSIRQ.C1.2 output optional Hypervisor physical timer event (active high) CNTPHPIRQ.C1.2 output optional Hypervisor physical timer event (active high) IRQOUT.C1.2 output optional Hypervisor physical timer event (active high) IRQOUT.C1.2 output optional FIQ wakeup FIQOUT.C1.2 input optional Configure AArch64 Reset Vector Base Address at reset AA64nAA32.C1.2 input optional Register width state at reset VINITHI.C1.2 input optional Configure Exception endianness (SCTLR.EE) CFGTE.C1.2 input optional Configure exception state at reset (SCTLR.EE) CFGTE.C1.2 input optional Configure exception state at reset (SCTLR.TE) reset.C1.2 input optional FIQ interrupt, active high (negation of nFIQ) irq.C1.2 input optional FIQ interrupt, active high (negation of nFIQ) viq.C1.2 input optional Virtual FIQ interrupt, active on rising edge (negation of nSEI) viq.C1.2 input optional Virtual FIQ interrupt, active on rising edge (negation of nSEI) AXI.SIVERR.C1.2 input optional Virtual System error interrupt, active on rising edge (negation of nSEI) AXI.SIVERR.C1.2 input optional Private peripheral interrupt PPHI6.C1.3 input optional Private peripheral interrupt PPHI7.C1.3 input optional Private peripheral interrupt PPHI7.C1.3 input optional Private peripheral interrupt PPHI8.C1.3 input optional Private peripheral interrupt PPHI7.C1.3 input optional Private peripheral interrupt PPHI7.C1.3 input optional Private peripheral interrupt PPHI7.C1.3 input optional Priv	DDIac Ct a	:	4:1	D-itilt
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PPI29_C1_2		_		
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CNTPHPIRQ_C1_2 output optional Hypervisor physical timer event (active high)		_	_	,
CNTPHPIRQ_C1.2 output optional Hypervisor physical timer event (active high)	CNTPNSIRQ_C1_2	output	optional	2 0
FIQOUT_C1_2 output	CNTPHPIRQ_C1_2	output	optional	Hypervisor physical timer event (active
RVBARADDRx_C1.2 input optional dress at reset AA64nAA32_C1_2 input optional optional configure AArch64 Reset Vector Base Address at reset VINITHL_C1_2 input optional configure HIVECS mode (SCTLR.V) CFGEND_C1_2 input optional Configure exception endianness (SCTLR_EE) CFGTE_C1_2 input optional FIQ interrupt, active high (negation of nFIQ) irq_C1_2 input optional input optional System error interrupt, active high (negation of nIRQ) sei_C1_2 input optional Virtual FIQ interrupt, active high (negation of nIRQ) virq_C1_2 input optional Virtual FIQ interrupt, active high (negation of nVFIQ) virq_C1_2 input optional Virtual IRQ interrupt, active high (negation of nVFIQ) virq_C1_2 input optional Virtual IRQ interrupt, active high (negation of nVFIQ) virq_C1_2 input optional Virtual system error interrupt, active on rising edge (negation of nVFIQ) virq_C1_2 input optional Virtual system error interrupt, active on rising edge (negation of nVSEI) AXI_SIVERR_C1_2 input optional Virtual system error interrupt, active on rising edge (negation of nVSEI) AXI_SIVERR_C1_2 input optional Optional Sivernal abort type (DECERR=0, SIVERR=1) CP15SDISABLE_C1_2 input optional Performance monitor event (active high) SMPEN_C1_2 output optional Private peripheral interrupt PP116_C1_3 input optional Private peripheral interrupt PP118_C1_3 input optional Private peripheral interrupt PP19C1_C1_3 input optional Private peripheral interrupt PP19C1_C1_3 input optional Private peripheral interrupt PP19C1_C1_3 input optional Private peripheral interrupt	IRQOUT_C1_2	output	optional	IRQ wakeup
AA64nAA32_C1.2 input optional Register width state at reset	FIQOUT_C1_2	output	optional	FIQ wakeup
AA64nAA32_C1_2 input optional Register width state at reset	RVBARADDRx_C1_2	input	optional	Configure AArch64 Reset Vector Base Ad-
VINITHI.C1.2 input optional Configure HIVECS mode (SCTLR.V) CFGEND.C1.2 input optional Configure exception endianness (SCTLR.EE) CFGTE.C1.2 input optional Processor reset, active high (SCTLR.TE) reset.C1.2 input optional FIQ interrupt, active high (negation of nFIQ) irq.C1.2 input optional System error interrupt, active on rising edge (negation of nSEI) vfiq.C1.2 input optional Virtual FIQ interrupt, active high (negation of nVFIQ) virq.C1.2 input optional Virtual IRQ interrupt, active high (negation of nVFIQ) virq.C1.2 input optional Virtual IRQ interrupt, active high (negation of nVIRQ) vsei.C1.2 input optional Virtual system error interrupt, active on rising edge (negation of nVIRQ) vsei.C1.2 input optional Virtual system error interrupt, active on rising edge (negation of nVSEI) AXI.SLVERR.C1.2 input optional AXI external abort type (DECERR=0, SLVERR=1) CP15SDISABLE.C1.2 input optional CP15SDISABLE (active high) PMUIRQ.C1.2 output optional Performance monitor event (active high) SMPEN.C1.2 output optional CPUECTLR.SMPEN current value PPI16.C1.3 input optional Private peripheral interrupt PPI17.C1.3 input optional Private peripheral interrupt PPI18.C1.3 input optional Private peripheral interrupt PPI19.C1.3 input optional Private peripheral interrupt				dress at reset
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CFGTE_C1_2 input optional Configure exception state at reset (SCTLR.TE) reset_C1_2 input optional Processor reset, active high (negation of nFIQ) irq_C1_2 input optional IRQ interrupt, active high (negation of nIRQ) sei_C1_2 input optional System error interrupt, active on rising edge (negation of nSEI) vfiq_C1_2 input optional Virtual FIQ interrupt, active high (negation of nVFIQ) virq_C1_2 input optional Virtual IRQ interrupt, active high (negation of nVFIQ) virq_C1_2 input optional Virtual IRQ interrupt, active high (negation of nVFIQ) vsei_C1_2 input optional Virtual IRQ interrupt, active high (negation of nVIRQ) vsei_C1_2 input optional Virtual system error interrupt, active on rising edge (negation of nVSEI) AXI_SLVERR_C1_2 input optional AXI external abort type (DECERR=0, SLVERR=1) CP15SDISABLE_C1_2 input optional CP15SDISABLE (active high) PMUIRQ_C1_2 output optional Performance monitor event (active high) SMPEN_C1_2 output optional Private peripheral interrupt PP116_C1_3 input optional Private peripheral interrupt PP118_C1_3 input optional Private peripheral interrupt PP119_C1_3 input optional Private peripheral interrupt PP119_C1_3 input optional Private peripheral interrupt PP120_C1_3 input optional Private peripheral interrupt	CFGEND_C1_2	input	optional	
inq.C1.2 input optional FIQ interrupt, active high (negation of nFIQ) sei.C1.2 input optional System error interrupt, active on rising edge (negation of nSEI) vfiq.C1.2 input optional Virtual FIQ interrupt, active high (negation of nVFIQ) virq.C1.2 input optional Virtual IRQ interrupt, active high (negation of nVFIQ) virq.C1.2 input optional Virtual IRQ interrupt, active high (negation of nVIRQ) vsei.C1.2 input optional Virtual system error interrupt, active on rising edge (negation of nVSEI) AXI.SI.VERR.C1.2 input optional AXI external abort type (DECERR=0, SLVERR=1) CP15SDISABLE.C1.2 input optional CP15SDISABLE (active high) PMUIRQ.C1.2 output optional Performance monitor event (active high) SMPEN.C1.2 output optional CPUECTLR.SMPEN current value PP16.C1.3 input optional Private peripheral interrupt PP17.C1.3 input optional Private peripheral interrupt PP18.C1.3 input optional Private peripheral interrupt PP19.C1.3 input optional Private peripheral interrupt	CFGTE_C1_2	input	optional	Configure exception state at reset
inq.C1.2 input optional IRQ interrupt, active high (negation of nIRQ) sei.C1.2 input optional System error interrupt, active on rising edge (negation of nSEI) vfiq.C1.2 input optional Virtual FIQ interrupt, active high (negation of nVFIQ) virq.C1.2 input optional Virtual IRQ interrupt, active high (negation of nVIRQ) vsei.C1.2 input optional Virtual system error interrupt, active on rising edge (negation of nVSEI) AXI.SLVERR.C1.2 input optional AXI external abort type (DECERR=0, SLVERR=1) CP15SDISABLE.C1.2 input optional CP15SDISABLE (active high) PMUIRQ.C1.2 output optional Performance monitor event (active high) SMPEN.C1.2 output optional CPUECTLR.SMPEN current value PPI16_C1.3 input optional Private peripheral interrupt PPI17.C1.3 input optional Private peripheral interrupt PPI18.C1.3 input optional Private peripheral interrupt PPI19.C1.3 input optional Private peripheral interrupt PPI19.C1.3 input optional Private peripheral interrupt PPI19.C1.3 input optional Private peripheral interrupt PPI20.C1.3 input optional Private peripheral interrupt PPI20.C1.3 input optional Private peripheral interrupt PPI20.C1.3 input optional Private peripheral interrupt	reset_C1_2	input	optional	Processor reset, active high
irq_C1_2 input optional IRQ interrupt, active high (negation of nIRQ) sei_C1_2 input optional System error interrupt, active on rising edge (negation of nSEI) vfiq_C1_2 input optional Virtual FIQ interrupt, active high (negation of nVFIQ) virq_C1_2 input optional Virtual IRQ interrupt, active high (negation of nVIRQ) vsei_C1_2 input optional Virtual system error interrupt, active on rising edge (negation of nVSEI) AXI_SLVERR_C1_2 input optional AXI external abort type (DECERR=0, SLVERR=1) CP15SDISABLE_C1_2 input optional CP15SDISABLE (active high) PMUIRQ_C1_2 output optional Performance monitor event (active high) SMPEN_C1_2 output optional CPUECTLR_SMPEN current value PPI6_C1_3 input optional Private peripheral interrupt PPI17_C1_3 input optional Private peripheral interrupt PPI18_C1_3 input optional Private peripheral interrupt PPI19_C1_3 input optional Private peripheral interrupt PPI19_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt	fiq_C1_2	input	optional	FIQ interrupt, active high (negation of
sei_C1_2 input optional System error interrupt, active on rising edge (negation of nSEI) vfiq_C1_2 input optional Virtual FIQ interrupt, active high (negation of nVFIQ) virq_C1_2 input optional Virtual IRQ interrupt, active high (negation of nVIRQ) vsei_C1_2 input optional Virtual system error interrupt, active on rising edge (negation of nVSEI) AXI_SLVERR_C1_2 input optional AXI external abort type (DECERR=0, SLVERR=1) CP15SDISABLE_C1_2 input optional CP15SDISABLE (active high) PMUIRQ_C1_2 output optional Performance monitor event (active high) SMPEN_C1_2 output optional CPUECTLR.SMPEN current value PPI16_C1_3 input optional Private peripheral interrupt PPI17_C1_3 input optional Private peripheral interrupt PPI18_C1_3 input optional Private peripheral interrupt PPI19_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt	irq_C1_2	input	optional	
vfiq_C1_2 input optional Virtual FIQ interrupt, active high (negation of nVFIQ) virq_C1_2 input optional Virtual IRQ interrupt, active high (negation of nVIRQ) vsei_C1_2 input optional Virtual system error interrupt, active on rising edge (negation of nVSEI) AXI_SLVERR_C1_2 input optional AXI external abort type (DECERR=0, SLVERR=1) CP15SDISABLE_C1_2 input optional CP15SDISABLE (active high) PMUIRQ_C1_2 output optional Performance monitor event (active high) SMPEN_C1_2 output optional CPUECTLR_SMPEN current value PPI16_C1_3 input optional Private peripheral interrupt PPI17_C1_3 input optional Private peripheral interrupt PPI18_C1_3 input optional Private peripheral interrupt PPI19_C1_3 input optional Private peripheral interrupt PPI19_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt	sei_C1_2	input	optional	System error interrupt, active on rising
virq_C1_2 input optional Virtual IRQ interrupt, active high (negation of nVIRQ) vsei_C1_2 input optional Virtual system error interrupt, active on rising edge (negation of nVSEI) AXI_SLVERR_C1_2 input optional AXI external abort type (DECERR=0, SLVERR=1) CP15SDISABLE_C1_2 input optional CP15SDISABLE (active high) PMUIRQ_C1_2 output optional Performance monitor event (active high) SMPEN_C1_2 output optional CPUECTLR.SMPEN current value PPI16_C1_3 input optional Private peripheral interrupt PPI17_C1_3 input optional Private peripheral interrupt PPI18_C1_3 input optional Private peripheral interrupt PPI19_C1_3 input optional Private peripheral interrupt PPI19_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt	vfiq_C1_2	input	optional	Virtual FIQ interrupt, active high (nega-
vsei_C1_2 input optional Virtual system error interrupt, active on rising edge (negation of nVSEI) AXI_SLVERR_C1_2 input optional AXI external abort type (DECERR=0, SLVERR=1) CP15SDISABLE_C1_2 input optional CP15SDISABLE (active high) PMUIRQ_C1_2 output optional Performance monitor event (active high) SMPEN_C1_2 output optional CPUECTLR.SMPEN current value PPI16_C1_3 input optional Private peripheral interrupt PPI17_C1_3 input optional Private peripheral interrupt PPI18_C1_3 input optional Private peripheral interrupt PPI19_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt	virq_C1_2	input	optional	Virtual IRQ interrupt, active high (nega-
AXI_SLVERR_C1_2 input optional AXI external abort type (DECERR=0, SLVERR=1) CP15SDISABLE_C1_2 input optional CP15SDISABLE (active high) PMUIRQ_C1_2 output optional Performance monitor event (active high) SMPEN_C1_2 output optional CPUECTLR.SMPEN current value PPI16_C1_3 input optional Private peripheral interrupt PPI17_C1_3 input optional Private peripheral interrupt PPI18_C1_3 input optional Private peripheral interrupt PPI19_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt	vsei_C1_2	input	optional	Virtual system error interrupt, active on
CP15SDISABLE_C1_2 input optional CP15SDISABLE (active high) PMUIRQ_C1_2 output optional Performance monitor event (active high) SMPEN_C1_2 output optional CPUECTLR.SMPEN current value PPI16_C1_3 input optional Private peripheral interrupt PPI17_C1_3 input optional Private peripheral interrupt PPI18_C1_3 input optional Private peripheral interrupt PPI19_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt	AXI_SLVERR_C1_2	input	optional	AXI external abort type (DECERR=0,
PMUIRQ_C1_2 output optional Performance monitor event (active high) SMPEN_C1_2 output optional CPUECTLR.SMPEN current value PPI16_C1_3 input optional Private peripheral interrupt PPI17_C1_3 input optional Private peripheral interrupt PPI18_C1_3 input optional Private peripheral interrupt PPI19_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt	CP15SDISABLE_C1_2	input	optional	,
SMPEN_C1_2 output optional CPUECTLR.SMPEN current value PPI16_C1_3 input optional Private peripheral interrupt PPI17_C1_3 input optional Private peripheral interrupt PPI18_C1_3 input optional Private peripheral interrupt PPI19_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt		_		(,
PPI16_C1_3 input optional Private peripheral interrupt PPI17_C1_3 input optional Private peripheral interrupt PPI18_C1_3 input optional Private peripheral interrupt PPI19_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt	•	_		
PPI17_C1_3 input optional Private peripheral interrupt PPI18_C1_3 input optional Private peripheral interrupt PPI19_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt		_	_	Private peripheral interrupt
PPI18_C1_3 input optional Private peripheral interrupt PPI19_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt				
PPI19_C1_3 input optional Private peripheral interrupt PPI20_C1_3 input optional Private peripheral interrupt		_		
PPI20_C1_3 input optional Private peripheral interrupt		_		= =
		_	_	= = =
	PPI21_C1_3	_	optional	Private peripheral interrupt

PPI22_C1_3	input	optional	Private peripheral interrupt
PPI23_C1_3	input	optional	Private peripheral interrupt
PPI24_C1_3	input	optional	Private peripheral interrupt
PPI25_C1_3	input	optional	Private peripheral interrupt
PPI26_C1_3	input	optional	Private peripheral interrupt
PPI27_C1_3	input	optional	Private peripheral interrupt
PPI28_C1_3	input	optional	Private peripheral interrupt
PPI29_C1_3	input	optional	Private peripheral interrupt
PPI30_C1_3	input	optional	Private peripheral interrupt
PPI31_C1_3	input	optional	Private peripheral interrupt
CNTVIRQ_C1_3	output	optional	Virtual timer event (active high)
CNTPSIRQ_C1_3	output	optional	Secure physical timer event (active high)
CNTPNSIRQ_C1_3	output	optional	Non-secure physical timer event (active
·	1	1	high)
CNTPHPIRQ_C1_3	output	optional	Hypervisor physical timer event (active
·	•	•	high)
IRQOUT_C1_3	output	optional	IRQ wakeup
FIQOUT_C1_3	output	optional	FIQ wakeup
RVBARADDRx_C1_3	input	optional	Configure AArch64 Reset Vector Base Ad-
	_	_	dress at reset
AA64nAA32_C1_3	input	optional	Register width state at reset
VINITHI_C1_3	input	optional	Configure HIVECS mode (SCTLR.V)
CFGEND_C1_3	input	optional	Configure exception endianness (SCTLR.EE)
CFGTE_C1_3	input	optional	Configure exception state at reset (SCTLR.TE)
reset_C1_3	input	optional	Processor reset, active high
fiq_C1_3	input	optional	FIQ interrupt, active high (negation of nFIQ)
irq_C1_3	input	optional	IRQ interrupt, active high (negation of nIRQ)
sei_C1_3	input	optional	System error interrupt, active on rising edge (negation of nSEI)
vfiq_C1_3	input	optional	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C1_3	input	optional	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C1_3	input	optional	Virtual system error interrupt, active on rising edge (negation of nVSEI)
AXI_SLVERR_C1_3	input	optional	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C1_3	input	optional	CP15SDISABLE (active high)
PMUIRQ_C1_3	output	optional	Performance monitor event (active high)
SMPEN_C1_3	output	optional	CPUECTLR.SMPEN current value

Table 6.1: Net Ports

FIFO Ports

This model has no FIFO ports.

Formal Parameters

variant Enumeration Selects variant (either a generic ISA or a specific model) disableGICModel Boolean Disable the internal GIC model entirely enableGICV2.64kB_Page Boolean Enable/disable GICv3 support supportSTATUSR Boolean Enable/disable support for GICv3 GIC[CDV].STATUSR registers distinctMTCores Boolean Enable/disable support for GICv3 GIC[CDV].STATUSR registers distinctMTCores Boolean For multi-threaded (MT) processors, simulate threads as separate cores (otherwise, simulate MT threads as a single entity) override_clusterVariants String Specifies a comma-separated list of cluster variant names in this multicluster override_timerScaleFactor Uns32 Specifies the fraction of MIPS rate to use for MPCore timers (generic timers or global/local/watchdogs depending on implementation). Defaults to 20 for generic timers, 2 for others override_GICD_NSACRPresent Boolean Specifies that optional GICD_NSACR distributor registers are present (GICv2 only) override_GICD_SPISRPresent Boolean Specifies that implementation-specific GICD_SPISR distributor register is present (GICv1 ICDSPIS/ICSPISR) override_GICO_SPISRPresent Boolean Specifies that implementation-specific GICD_SPISR distributor registers are present (GICv1 ICDSPIS/ICSPISR) override_GIC	Name	Type	Description
disableGICModel Boolean Disable the internal GIC model entirely			
enableGICv2.64kB_Page Boolean Enable 64kB page size for GICv2 memory-mapped register groups (Xilinx Zynq Ultrascale support) supportSTATUSR Boolean Enable_disable support for GICv3 GIC[CDV]_STATUSR registers distinctMTCores Boolean For multi-threaded (MT) processors, simulate threads as separate cores (otherwise, simulate MT threads as a single entity) override_clusterVariants String Specifies a comma-separated list of cluster variant names in this multicluster override_discorrect Uns32 Specifies the fraction of MIPS rate to use for MPCore timers (generic timers or global/local/watchdogs depending on implementation). Defaults to 20 for generic timers, 2 for others override_GICD_NSACRPresent Boolean Specifies that optional GICD_NSACR distributor registers are present (GICv2 only) override_GICD_SPISRPresent Boolean Specifies that implementation-specific GICD_SPISR distributor register is present (GICv1 ICDPPIS/ICPPISR, GICv1 and GICv2 only) override_GICv3_DistributorBase Uns64 Specify distributor register block base address (GICv3 only) override_GIC_JPIMask Uns32 Specifies that GICR_CTLR_EINWF is implemented (GICv3 only) override_GIC_DISABLE Boolean Specify initial value of GICCDISABLE override_GICD_TYPER Uns32 Override GICD_TYPER register (GICv1 ICDIDTR) override_GICD_TYPER_ITLines Uns32 Override GICD_TYPER register (GICv1 ICDICTR) override_GICD_LIDR Uns32 Override GICD_LIDR register (GICv1 ICDICTR) override_GICD_LIDR Uns32 Override GICL_UIDR register (GICv3 and later) override_GICR_LIDR override_GICR_LIDR (Uns32 Override GICL_UIDR register (GICv3 and later) override_GICR_LIDR override_GICR_LIDR Override_GICR_LIDR register (GICv3 and later)	disableGICModel	Boolean	
supportSTATUSR Boolean Enable/disable support for GICv3 GIC[CDV]_STATUSR registers distinctMTCores Boolean Specifies a comma-separated list of cluster variant names in this multicluster override_clusterVariants String Specifies a comma-separated list of cluster variant names in this multicluster override_timerScaleFactor Uns32 Specifies the fraction of MIPS rate to use for MPCore timers (generic timers or global/local/watchdogs depending on implementation). Defaults to 20 for generic timers, 2 for others override_GICD_NSACRPresent Boolean Specifies that optional GICD_NSACR distributor registers are present (GICv2 only) override_GICD_SPISRPresent Boolean Specifies that implementation-specific GICD_PPISR distributor register is present (GICv1 ICDPPIS/ICPPISR, GICv1 and GICv2 only) override_GICV3_DistributorBase Uns64 Specify distributor register block base address (GICv3 only) override_GICV3_EINWFPresent Boolean Specifies that GICR_CTLR_EINWF is implemented (GICv3 only) override_GIC_PPIMask Uns32 Specify bitmask of implemented PPIs in the GIC (e.g. ID16 is 0x0001, ID31 is 0x8000) override_GICC_DIDR Uns32 Override_GICC_TIPPER register (GICv1 ICDIDR) override_GICD_TYPER Uns32 Override_GIC_TYPER register (GICv1 ICDICTR) override_GICD_TYPER_ITLines (GICv1 ICDICTR) override_GICD_ICFGRN Uns32 Override GICD_ICFGR1CDICFGR2GICD_ICFGRn override_GICR_LIDR Uns32 Override GICL_IDR register (GICv1 ICDICTR) override_GICR_LIDR Uns32 Override GICL_IDR register (GICv1 ICDICTR) override_GICR_LIDR Uns32 Override GICR_IDR register (GICv1 ICDICTR) override_GICR_IDR Uns32 Override GICR_IDR register (GICv1 ICDILDR) override_GICR_IDR Uns32 Override GICR_IDR register (GICv3 and later) override_GICR_IDR	enableGICv3	Boolean	Enable/disable GICv3 support
SupportSTATUSR Boolean Enable/disable support for GICv3 GIC[CDV]_STATUSR registers	enableGICv2_64kB_Page	Boolean	Enable 64kB page size for GICv2 memory-mapped register
distinctMTCores Boolean Boolean String Override_clusterVariants String Override_timerScaleFactor Override_differ_GICD_NSACRPresent Override_GICD_NSACRPresent Override_GICD_PPISRPresent Boolean Override_GICD_SPISRPresent Override_GICV3_DistributorBase Override_GICV3_E1NWFPresent Override_GICD_PIMask Override_GICD_PIMask Override_GICD_PIMask Override_GICD_DISABLE Override_GICD_ISABLE Boolean Override_GICD_ISABLE Boolean Specify distributor register block base address (GICV3 only) Override_GICC_IDR Override_GICC_IDR Override_GICC_IDR Override_GICD_TYPER Uns32 Override_GICD_TYPER Uns32 Override_GICD_TYPER Override_GICD_TYPER Uns32 Override_GICD_TYPER register Override_GICD_TYPER register Override_GICD_IDR Override_GICD_TYPER Uns32 Override_GICD_TIDR Override_GICD_TIDR Override_GICD_TIDR Override_GICD_TIDR Override_GICD_TIDR Override_GICD_TIDR Override_GICD_TIDR Override_GICD_TIDR Override_GICD_TYPER_ITLines Override_GICD_TIDR Ove			groups (Xilinx Zynq Ultrascale support)
distinctMTCores Boolean For multi-threaded (MT) processors, simulate threads as separate cores (otherwise, simulate MT threads as a single entity) override.clusterVariants String Specifies a comma-separated list of cluster variant names in this multicluster override.timerScaleFactor Override.GICD_NSACRPresent Override.GICD_NSACRPresent Boolean Override.GICD_PPISRPresent Boolean Override.GICD_PPISRPresent Override.GICD_SPISRPresent Boolean Override.GICD_SPISRPresent Override.GICD_SPISRPresent Override.GICV3_DistributorBase Override.GICV3_DistributorBa	supportSTATUSR	Boolean	Enable/disable support for GICv3 GIC[CDV]_STATUSR reg-
arate cores (otherwise, simulate MT threads as a single entity) override_clusterVariants String Specifies a comma_separated list of cluster variant names in this multicluster override_timerScaleFactor Uns32 Specifies the fraction of MIPS rate to use for MPCore timers (generic timers or global/local/watchdogs depending on implementation). Defaults to 20 for generic timers, 2 for others override_GICD_NSACRPresent Boolean override_GICD_PPISRPresent override_GICD_PPISRPresent Boolean override_GICD_SPISRPresent Boolean Specifies that implementation-specific GICD_PPISR distributor register is present (GICv2 only) override_GICV3_DistributorBase override_GICV3_DistributorBase override_GICV3_DistributorBase override_GICV3_DistributorBase override_GICV3_DistributorBase override_GICV3_DistributorBase override_GIC_TPIMask Uns32 Specifies that GICR_CTLR_ENWF is implemented (GICv3 only) override_GIC_DISABLE boolean override_GIC_DIDR override_GIC_TIDR override_GIC_TIDR override_GIC_TYPER Uns32 Override_GIC_TIDR register (GICv1 ICDIDR) override_GICD_TYPER_ITLines override_GICD_TYPER_ITLines override_GICD_TYPER_ITLINES override_GIC_TIDR override_GIC_TIDR override_GIC_TIDR override_GIC_TIDR override_GIC_TIDR override_GIC_TIDR override_GIC_TIDR override_GIC_TIDR override_GIC_TIDR override_GIC_TYPER_Uns32 override_GIC_TYPER_register (GICv1 ICDIDCTR) override_GIC_TYPER_ITLINES override_GIC_TIDR register (GICv1 ICDIDCTR) override_GIC_TYPER_Uns32 override_GIC_TIDR register (GICv1 ICDIDCTR) override_GIC_TIDR override_GIC_TI			
override_clusterVariants String Specifies a comma-separated list of cluster variant names in this multicluster Override_timerScaleFactor Uns32 Specifies the fraction of MIPS rate to use for MPCore timers (generic timers or global/local/watchdogs depending on implementation). Defaults to 20 for generic timers, 2 for others Specifies that optional GICD_NSACR distributor registers are present (GICv2 only) override_GICD_PPISRPresent Boolean Specifies that optional GICD_NSACR distributor registers are present (GICv2 only) override_GICD_SPISRPresent Boolean Override_GICV3_DISTRPRESENT Boolean Specifies that implementation-specific GICD_SPISR distributor register is present (GICv1 ICDSPIS/ICSPISR) override_GICV3_DISTRIBUTORBASE Override_GICV3_DISTRIBUTORBASE Override_GICV3_DISTRIBUTORBASE Override_GICV3_DISTRIBUTORBASE Override_GICV3_DISTRIBUTORBASE Override_GICV3_DISTRIBUTORBASE Override_GICC_DISABLE Boolean Specify distributor register block base address (GICv3 only) Specify bitmask of implemented PPIs in the GIC (e.g. ID16 is 0x0001, ID31 is 0x8000) override_GICC_DISABLE Override_GICC_DISABLE Override_GICC_TIDR Override_GICD_TYPER Uns32 Override_GICD_TYPER register (GICv1 ICDIDTR) override_GICD_TYPER Uns32 Override_GICD_TYPER register (GICv1 ICDICTR) override_GICD_TYPER_ITLines Override_GICD_TYPER_ITLIBES Override_GICD_TYPER_register (GICv1 ICDIDTR) Override_GICD_TYPER_Uns32 Override_GICD_TYPER_Uns32 Override_GICD_TYPER_Uns32 Override_GICD_TIDR register (GICv1 ICDIDTR) override_GICD_TIDR Override_GICD_TIDR Override_GICD_TIDR register (GICv3 and later) override_GICR_IIDR Override_GICR_IIDR Override_GICR_IIDR Uns32 Override_GICR_IIDR register (GICv3 and later) Override_GITS_IIDR register (GICv3 and later) Override_GITS_TYPER Override_GITS_TYPER register (GICv3 and later)	distinctMTCores	Boolean	
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override_GICD_IIDR Uns32 Override GICD_IIDR register (GICv1 ICDIIDR) override_GICH_VTR Uns32 Override GICH_VTR register override_GICR_IIDR Uns32 Override GICR_IIDR register (GICv3 and later) override_GITS_IIDR Uns32 Override GITS_IIDR register (GICv3 and later) override_GITS_TYPER Uns64 Override GITS_TYPER register (GICv3 and later)			
override_GICH_VTR Uns32 Override GICH_VTR register override_GICR_IIDR Uns32 Override GICR_IIDR register (GICv3 and later) override_GITS_IIDR Uns32 Override GITS_IIDR register (GICv3 and later) override_GITS_TYPER Uns64 Override GITS_TYPER register (GICv3 and later)	override_GICD_IIDR	Uns32	
override_GICR_IIDR Uns32 Override GICR_IIDR register (GICv3 and later) override_GITS_IIDR Uns32 Override GITS_IIDR register (GICv3 and later) override_GITS_TYPER Uns64 Override GITS_TYPER register (GICv3 and later)	override_GICH_VTR	Uns32	
override_GITS_TYPER Uns64 Override GITS_TYPER register (GICv3 and later)	override_GICR_IIDR	Uns32	Override GICR_IIDR register (GICv3 and later)
	override_GITS_IIDR	Uns32	Override GITS_IIDR register (GICv3 and later)
override ICCPMRRits Uns32 Specify the number of writable bits in CICC PMR (CICy)	override_GITS_TYPER	Uns64	Override GITS_TYPER register (GICv3 and later)
	override_ICCPMRBits	Uns32	Specify the number of writable bits in GICC_PMR (GICv1
ICCPMR)			ICCPMR)

override_minICCBPR	Uns32	Specify the minimum possible value for GICC_BPR (GICv1
		ICCBPR)

Table 8.1: Parameters that can be set in: CLUSTER_GROUP

Model Commands

A Processor model can implement one or more **Model Commands** available to be invoked from the simulator command line, from the OP API or from the Imperas Multiprocessor Debugger.

9.1 Level 1: CLUSTER_GROUP

9.1.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 9.1: isync command arguments

9.1.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 9.2: itrace command arguments

Registers

10.1 Level 1: CLUSTER_GROUP

No registers.