

OVP Guide to Using Processor Models

Model specific information for MIPS_1004Kc

Imperas Software Limited Imperas Buildings, North Weston Thame, Oxfordshire, OX9 2HA, U.K. docs@imperas.com



Author	Imperas Software Limited
Version	20210408.0
Filename	OVP_Model_Specific_Information_mips32_r1r5_1004Kc.pdf
Created	5 May 2021
Status	OVP Standard Release

Copyright Notice

Copyright (c) 2021 Imperas Software Limited. All rights reserved. This software and documentation contain information that is the property of Imperas Software Limited. The software and documentation are furnished under a license agreement and may be used or copied only in accordance with the terms of the license agreement. No part of the software and documentation may be reproduced, transmitted, or translated, in any form or by any means, electronic, mechanical, manual, optical, or otherwise, without prior written permission of Imperas Software Limited, or as expressly provided by the license agreement.

Right to Copy Documentation

The license agreement with Imperas permits licensee to make copies of the documentation for its internal use only. Each copy shall include all copyrights, trademarks, service marks, and proprietary rights notices, if any.

Destination Control Statement

All technical data contained in this publication is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the readers responsibility to determine the applicable regulations and to comply with them.

Disclaimer

IMPERAS SOFTWARE LIMITED, AND ITS LICENSORS MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

Contents

1	Overview	1
	1.1 Description	. 1
	1.2 Licensing	. 1
	1.3 Limitations	. 1
	1.4 Verification	. 2
	1.5 Features	. 2
	1.6 Description	. 2
	1.7 Licensing	. 2
	1.8 Limitations	. 2
	1.9 Verification	. 2
	1.10 Features	. 3
	1.11 Description	. 3
	1.12 Licensing	. 3
	1.13 Limitations	. 3
	1.14 Verification	. 3
	1.15 Features	. 3
	1.16 Description	. 4
	1.17 Licensing	. 4
	1.18 Limitations	. 4
	1.19 Verification	. 4
	1.20 Features	. 4
2	Configuration	5
	2.1 Location	. 5
	2.2 GDB Path	
	2.3 Semi-Host Library	
	2.4 Processor Endian-ness	
	2.5 QuantumLeap Support	
	2.6 Processor ELF code	
3	All Variants in this model	6
4	Bus Master Ports	8
5	Bus Slave Ports	9
6	Net Ports	10

7	FIF) Ports	15
8	Forn	nal Parameters	16
9	Exec	cution Modes	33
10	Exce	eptions	34
11	Hier	archy of the model	37
	11.1	Level 1: CMP	37
	11.2	Level 2: CPU	37
	11.3	Level 3: VPE	37
	11.4	Level 4: TC	38
12	Mod	el Commands	39
	12.1	Level 1: CMP	39
			39
		·	39
	12.2		39
			39
		·	40
	12.3		40
			40
			40
	12.4		41
			41
		·	41
			41
		•	41
			41
		•	41
		*	42
		•	42
			42
			42
		12.4.8.1 Argument description	
			$\frac{12}{42}$
		1	$\frac{12}{42}$
		1 0 0	43
		1 0	43
		1 "	43
		1 1	43
		· · · · · · · · · · · · · · · · · · ·	43
			43
			43
		12. Into Importation 1 and 1 a	10
13	Reg	sters	45
	13.1	Level 1: CMP	45
	13.2	Level 2: CPU	45

Imperas OVP Fast Processor Model Documentation for MIPS_1004Kc

13.3	Level 3	3:	VPE) .									 										45
	13.3.1	\mathbf{C}	OP0										 										45
	13.3.2	\mathbf{C}	MP_{-}	.GC	$^{\circ}$ R								 										46
	13.3.3	\mathbf{C}	MP_{-}	.CP	\mathbf{C}																		47
	13.3.4	\mathbf{C}	MP_{-}	.GI	С.								 										47
13.4	Level 4	4: '	ΓC										 										61
	13.4.1	\mathbf{C}	ore																				61
	13.4.2	D	SP										 										61
	13.4.3	\mathbf{C}	OP0	١.									 										62
	13.4.4	\mathbf{C}	MP_{-}	.GC	$^{\circ}$ R																		63
	13.4.5	\mathbf{C}	MP_{-}	.CP	\mathbf{C}																		64
	13.4.6	\mathbf{C}	MP_{-}	.GI	С.								 										64
	13.4.7	In	tegr	atic	on_s	ur	opc	rt					 										77

Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.

The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners. There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

MIPS32 Configurable Processor Model

1.2 Licensing

Usage of binary model under license governing simulator usage. Source of model available under Imperas Software License Agreement.

1.3 Limitations

If this model is not part of your installation, then it is available for download from www.OVPworld.org/MIPSuser.

Cache model does not implement coherency

1.4 Verification

Models have been validated correct as part of the MIPS Verified program and run through the MIPS AVP test programs

1.5 Features

only MIPS32 Instruction set implemented

MMU Type: Standard TLB

L1 I and D cache model in either full or tag-only mode implemented (disabled by default)

Vectored interrupts implemented

MIPS16e ASE implemented

MT ASE implemented

DSP ASE implemented

1.6 Description

MIPS32 Configurable Processor Model

1.7 Licensing

Usage of binary model under license governing simulator usage. Source of model available under Imperas Software License Agreement.

1.8 Limitations

If this model is not part of your installation, then it is available for download from www.OVPworld.org/MIPSuser.

Cache model does not implement coherency

1.9 Verification

Models have been validated correct as part of the MIPS Verified program and run through the MIPS AVP test programs

1.10 Features

only MIPS32 Instruction set implemented

MMU Type: Standard TLB

L1 I and D cache model in either full or tag-only mode implemented (disabled by default)

Vectored interrupts implemented

MIPS16e ASE implemented

MT ASE implemented

DSP ASE implemented

1.11 Description

MIPS32 Configurable Processor Model

1.12 Licensing

Usage of binary model under license governing simulator usage. Source of model available under Imperas Software License Agreement.

1.13 Limitations

If this model is not part of your installation, then it is available for download from www.OVPworld.org/MIPSuser.

Cache model does not implement coherency

1.14 Verification

Models have been validated correct as part of the MIPS Verified program and run through the MIPS AVP test programs

1.15 Features

only MIPS32 Instruction set implemented

MMU Type: Standard TLB

L1 I and D cache model in either full or tag-only mode implemented (disabled by default)

Vectored interrupts implemented

MIPS16e ASE implemented

MT ASE implemented

DSP ASE implemented

1.16 Description

MIPS32 Configurable Processor Model

1.17 Licensing

Usage of binary model under license governing simulator usage. Source of model available under Imperas Software License Agreement.

1.18 Limitations

If this model is not part of your installation, then it is available for download from www.OVPworld.org/MIPSuser.

Cache model does not implement coherency

1.19 Verification

Models have been validated correct as part of the MIPS Verified program and run through the MIPS AVP test programs

1.20 Features

only MIPS32 Instruction set implemented

MMU Type: Standard TLB

L1 I and D cache model in either full or tag-only mode implemented (disabled by default)

Vectored interrupts implemented

MIPS16e ASE implemented

MT ASE implemented

DSP ASE implemented

Configuration

2.1 Location

This model's VLNV is mips.ovpworld.org/processor/mips32_r1r5/1.0.

The model source is usually at:

\$IMPERAS_HOME/ImperasLib/source/mips.ovpworld.org/processor/mips32_r1r5/1.0

The model binary is usually at:

\$IMPERAS_HOME/lib/\$IMPERAS_ARCH/ImperasLib/mips.ovpworld.org/processor/mips32_r1r5/1.0

2.2 GDB Path

The default GDB for this model is: \$IMPERAS_HOME/lib/\$IMPERAS_ARCH/gdb/mips-sde-elf-gdb.

2.3 Semi-Host Library

The default semi-host library file is mips.ovpworld.org/semihosting/mips32Newlib/1.0

2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

2.6 Processor ELF code

The ELF code supported by this model is: 0x8.

All Variants in this model

This model has these variants

Variant	Description
ISA	
M14K	
M14KcTLB	
M14KcFMM	
4KEc	
4KEm	
4KEp	
M4K	
4Kc	
4Km	
4Kp	
24Kc	
24Kf	
24KEc	
24KEf	
34Kc	
34Kf	
34Kn	
74Kc	
74Kf	
1004Kc	(described in this document)
1004Kf	
1074Kc	
1074Kf	
microAptivC	
microAptivP	
microAptivCF	
interAptiv	
interAptivUP	
proAptiv	

Table 3.1: All Variants in this model

Bus Master Ports

This model has these bus master ports.

Name	min	max	Connect?	Description
INSTRUCTION	12	36	mandatory	
DATA	12	36	optional	

Table 4.1: Bus Master Ports

Bus Slave Ports

This model has no bus slave ports.

Net Ports

This model has these net ports.

Name	Type	Connect?	Description
reset	input	optional	CMP reset
dint	input	optional	Debug external interrupt
int0	input	optional	GIC external interrupt
int1	input	optional	GIC external interrupt
int2	input	optional	GIC external interrupt
int3	input	optional	GIC external interrupt
int4	input	optional	GIC external interrupt
int5	input	optional	GIC external interrupt
int6	input	optional	GIC external interrupt
int7	input	optional	GIC external interrupt
int8	input	optional	GIC external interrupt
int9	input	optional	GIC external interrupt
int10	input	optional	GIC external interrupt
int11	input	optional	GIC external interrupt
int12	input	optional	GIC external interrupt
int13	input	optional	GIC external interrupt
int14	input	optional	GIC external interrupt
int15	input	optional	GIC external interrupt
int16	input	optional	GIC external interrupt
int17	input	optional	GIC external interrupt
int18	input	optional	GIC external interrupt
int19	input	optional	GIC external interrupt
int20	input	optional	GIC external interrupt
int21	input	optional	GIC external interrupt
int22	input	optional	GIC external interrupt
int23	input	optional	GIC external interrupt
int24	input	optional	GIC external interrupt
int25	input	optional	GIC external interrupt
int26	input	optional	GIC external interrupt
int27	input	optional	GIC external interrupt
int28	input	optional	GIC external interrupt

int29 input optional GIC external interrupt int31 input optional GIC external interrupt int31 input optional GIC external interrupt int32 input optional GIC external interrupt int33 input optional GIC external interrupt int33 input optional GIC external interrupt int34 input optional GIC external interrupt int35 input optional GIC external interrupt int36 input optional GIC external interrupt int37 input optional GIC external interrupt int38 input optional GIC external interrupt int39 input optional Yield qualifier yq0.CPU0 input optional Yield qualifier yq1.CPU0 input optional Yield qualifier yq2.CPU0 input optional Yield qualifier yq4.CPU0 input optional Yield qualifier yq5.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq7.CPU0 input optional Yield qualifier yq8.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq11.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq13.CPU0 input optional Yield qualifier yq14.CPU0 input optional Yield qualifier yq15.CPU0 input optional Yield qualifier yq15.CPU0 input optional External interrupt hwint3.CPU0.VPE0 input optional External interrupt hwint4.CPU0.VPE0 input optional External interrupt hwint5.CPU0.VPE0 input optional External interrupt input optional External interrupt for compatibility vc.run.CPU0.VPE0 input optional External interrupt input optional External interrupt for compatibility vc.run.CPU0.VPE1 input optional External interrupt input option	. 100		,· 1	CIC 1 1:1
int31 input optional GIC external interrupt int32 input optional GIC external interrupt int33 input optional GIC external interrupt int34 input optional GIC external interrupt int35 input optional GIC external interrupt int35 input optional GIC external interrupt int36 input optional GIC external interrupt int37 input optional GIC external interrupt int38 input optional GIC external interrupt int39 input optional Yield qualifier yq1.CPU0 input optional Yield qualifier yq2.CPU0 input optional Yield qualifier yq2.CPU0 input optional Yield qualifier yq3.CPU0 input optional Yield qualifier yq4.CPU0 input optional Yield qualifier yq5.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq7.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq11.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq13.CPU0 input optional Yield qualifier yq13.CPU0 input optional Yield qualifier yq14.CPU0 input optional External interrupt hwint2.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE0 input optional External interrupt hwint3.CPU0.VPE0 input optional External interrupt hwint4.CPU0.VPE0 input optional External interrupt hwint5.CPU0.VPE0 input optional External interrupt hwint0.CPU0.VPE1 input optional External interrupt hwint1.CPU0.VPE1 input optional External interrupt hwint2.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint4.CPU0.VPE1 input optional External interrupt hwint4.CPU0.VPE1 input o		_	•	_
int32 input optional GIC external interrupt int33 input optional GIC external interrupt int34 input optional GIC external interrupt int35 input optional GIC external interrupt int36 input optional GIC external interrupt int36 input optional GIC external interrupt int37 input optional GIC external interrupt int38 input optional GIC external interrupt int38 input optional GIC external interrupt int39 input optional GIC external interrupt int39 input optional GIC external interrupt int39 input optional Yield qualifier yq0.CPU0 input optional Yield qualifier yq1.CPU0 input optional Yield qualifier yq2.CPU0 input optional Yield qualifier yq3.CPU0 input optional Yield qualifier yq4.CPU0 input optional Yield qualifier yq4.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq7.CPU0 input optional Yield qualifier yq8.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq1.CPU0 input optional Yield qualifier yq1.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq13.CPU0 input optional Yield qualifier yq14.CPU0 input optional Yield qualifier yq15.CPU0 input optional Yield qualifier hwint0.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE0 input optional External interrupt hwint3.CPU0.VPE0 input optional External interrupt hwint4.CPU0.VPE0 input optional External interrupt hwint5.CPU0.VPE0 input optional External interrupt for compatibility vc.run.CPU0.VPE0 input optional External interrupt for compatibility vc.run.CPU0.VPE0 input optional External interrupt hwint0.CPU0.VPE1 input optional External interrupt hwint1.CPU0.VPE1 input optional External interrupt hwint2.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint4.CPU0.VPE1 input optional External interrupt hwint4.CPU0.VPE1 input optional External interrupt		_	_	-
int33 input optional GIC external interrupt int34 input optional GIC external interrupt int35 input optional GIC external interrupt int36 input optional GIC external interrupt int37 input optional GIC external interrupt int38 input optional GIC external interrupt int38 input optional GIC external interrupt int39 input optional Yield qualifier yq0.CPU0 input optional Yield qualifier yq1.CPU0 input optional Yield qualifier yq3.CPU0 input optional Yield qualifier yq3.CPU0 input optional Yield qualifier yq4.CPU0 input optional Yield qualifier yq5.CPU0 input optional Yield qualifier yq7.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq11.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq13.CPU0 input optional Yield qualifier yq14.CPU0 input optional Yield qualifier yq15.CPU0 input optional External interrupt hwint2.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE0 input optional External interrupt hwint4.CPU0.VPE0 input optional External interrupt input optional External interrupt for compatibility vc.run.CPU0.VPE0 input optional External interrupt for compatibility vc.run.CPU0.VPE1 input optional External interrupt hwint1.CPU0.VPE1 input optional External interrupt hwint2.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint4.CPU0.VPE1 input optiona		_	-	-
int34 input optional GIC external interrupt int35 input optional GIC external interrupt int36 input optional GIC external interrupt int37 input optional GIC external interrupt int38 input optional GIC external interrupt int38 input optional GIC external interrupt int39 input optional GIC external interrupt int39 input optional GIC external interrupt int39 input optional Yield qualifier yq0.CPU0 input optional Yield qualifier yq1.CPU0 input optional Yield qualifier yq2.CPU0 input optional Yield qualifier yq3.CPU0 input optional Yield qualifier yq4.CPU0 input optional Yield qualifier yq5.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq7.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq1.CPU0 input optional External interrupt hwint3.CPU0.VPE0 input optional External interrupt hwint3.CPU0.VPE0 input optional External interrupt hwint5.CPU0.VPE0 input optional External interrupt input optional External interrupt hwint5.CPU0.VPE0 input optional External interrupt hwint0.CPU0.VPE0 input optional External interrupt input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE0 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint4.CPU0.VPE1 input optional External interrupt hwint4.CPU0.VPE1 input optional Exte		_	-	
int35 input optional GIC external interrupt int36 input optional GIC external interrupt int37 input optional GIC external interrupt int38 input optional GIC external interrupt int39 input optional GIC external interrupt int39 input optional GIC external interrupt int39 input optional GIC external interrupt yq0.CPU0 input optional Yield qualifier yq1.CPU0 input optional Yield qualifier yq2.CPU0 input optional Yield qualifier yq3.CPU0 input optional Yield qualifier yq3.CPU0 input optional Yield qualifier yq4.CPU0 input optional Yield qualifier yq5.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq7.CPU0 input optional Yield qualifier yq8.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq11.CPU0 input optional Yield qualifier yq11.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq14.CPU0 input optional Yield qualifier yq14.CPU0 input optional Yield qualifier yq15.CPU0 input optional Yield qualifier wq15.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE0 input optional External interrupt hwint3.CPU0.VPE0 input optional External interrupt hwint4.CPU0.VPE0 input optional External interrupt hwint5.CPU0.VPE0 input optional External interrupt hwint6.CPU0.VPE0 input optional External interrupt hwint7.CPU0.VPE0 input optional External interrupt hwint6.CPU0.VPE0 input optional External interrupt for compatibility vc.run.CPU0.VPE0 input optional External interrupt for compatibility vc.run.CPU0.VPE1 input optional External interrupt hwint6.CPU0.VPE1 input optional Externa			•	_
int36 input optional GIC external interrupt int37 input optional GIC external interrupt int38 input optional GIC external interrupt int38 input optional GIC external interrupt int39 input optional GIC external interrupt int39 input optional GIC external interrupt int39 input optional Yield qualifier yq0.CPU0 input optional Yield qualifier yq1.CPU0 input optional Yield qualifier yq3.CPU0 input optional Yield qualifier yq3.CPU0 input optional Yield qualifier yq4.CPU0 input optional Yield qualifier yq5.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq7.CPU0 input optional Yield qualifier yq8.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq11.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq13.CPU0 input optional Yield qualifier yq14.CPU0 input optional Yield qualifier yq14.CPU0 input optional Yield qualifier yq15.CPU0 input optional Xield qualifier input optional Xield qualifier yq15.CPU0 input optional Xield qualifier yq15.CPU0 input optional Xield qualifier input optional External interrupt hwint0.CPU0.VPE0 input optional External interrupt hwint3.CPU0.VPE0 input optional External interrupt hwint5.CPU0.VPE0 input optional External interrupt input optional External interrupt for compatibility vc.run.CPU0.VPE0 input optional External interrupt for compatibility vc.run.CPU0.VPE0 input optional External interrupt for compatibility vc.run.CPU0.VPE1 input optional External interrupt hwint0.CPU0.VPE1 input optional External interrupt hwint1.CPU0.VPE1 input optional External interrupt hwint2.CPU0.VPE1 input optional External interrupt hwint4.CPU0.VPE1 input optional External interrupt hwint4.CPU0.VPE1 input optional External interrupt		input	_	-
int37 input optional GIC external interrupt int38 input optional GIC external interrupt int39 input optional GIC external interrupt yq.CPU0 input optional Yield qualifier yq0.CPU0 input optional Yield qualifier yq1.CPU0 input optional Yield qualifier yq2.CPU0 input optional Yield qualifier yq3.CPU0 input optional Yield qualifier yq4.CPU0 input optional Yield qualifier yq5.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq7.CPU0 input optional Yield qualifier yq8.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq10.CPU0 input optional Yield qualifier yq11.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq13.CPU0 input optional Yield qualifier yq14.CPU0 input optional Yield qualifier yq15.CPU0 input optional Xield qualifier yq15.CPU0 input optional Xield qualifier yq15.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE0 input optional External interrupt hwint3.CPU0.VPE0 input optional External interrupt hwint4.CPU0.VPE0 input optional External interrupt hwint5.CPU0.VPE0 input optional External interrupt hwint0 input optional External interrupt hwint0 input optional External interrupt for compatibility vc.run.CPU0.VPE0 input optional External interrupt for compatibility vc.run.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint4.CPU0.VPE1 input optional External interrupt		input	optional	-
int38 input optional GIC external interrupt int39 input optional GIC external interrupt yq.CPU0 input optional Yield qualifier yq1.CPU0 input optional Yield qualifier yq2.CPU0 input optional Yield qualifier yq3.CPU0 input optional Yield qualifier yq4.CPU0 input optional Yield qualifier yq5.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq7.CPU0 input optional Yield qualifier yq8.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq10.CPU0 input optional Yield qualifier yq11.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq13.CPU0 input optional Yield qualifier yq14.CPU0 input optional Yield qualifier yq14.CPU0 input optional Yield qualifier yq15.CPU0 input optional Yield qualifier yq15.CPU0 input optional Yield qualifier yq14.CPU0 input optional Yield qualifier hwint0.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE0 input optional External interrupt hwint3.CPU0.VPE0 input optional External interrupt hwint4.CPU0.VPE0 input optional External interrupt hwint5.CPU0.VPE0 input optional External interrupt hwint0 input optional External interrupt hwint0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt		input	_	
int39 input optional yield qualifier yq1.CPU0 input optional yield qualifier yq2.CPU0 input optional yield qualifier yq2.CPU0 input optional yield qualifier yq3.CPU0 input optional yield qualifier yq4.CPU0 input optional yield qualifier yq4.CPU0 input optional yield qualifier yq4.CPU0 input optional yield qualifier yq5.CPU0 input optional yield qualifier yq6.CPU0 input optional yield qualifier yq7.CPU0 input optional yield qualifier yq8.CPU0 input optional yield qualifier yq9.CPU0 input optional yield qualifier yq9.CPU0 input optional yield qualifier yq10.CPU0 input optional yield qualifier yq11.CPU0 input optional yield qualifier yq12.CPU0 input optional yield qualifier yq14.CPU0 input optional yield qualifier yq15.CPU0 input optional yield qualifier yq14.CPU0 input optional yield qualifier yq15.CPU0 input optional yield qualifier yq14.CPU0 input optional yield qualifier yq15.CPU0 input optional yield qualifier hwint0.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE0 input optional External interrupt hwint3.CPU0.VPE0 input optional External interrupt hwint0 input optional External interrupt hwint0 input optional External interrupt hwint0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint4.CPU0.VPE1 input optional External interrupt	int37	input	optional	-
yq.CPU0 input optional Yield qualifier yq0.CPU0 input optional Yield qualifier yq1.CPU0 input optional Yield qualifier yq2.CPU0 input optional Yield qualifier yq3.CPU0 input optional Yield qualifier yq4.CPU0 input optional Yield qualifier yq4.CPU0 input optional Yield qualifier yq5.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq7.CPU0 input optional Yield qualifier yq8.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq10.CPU0 input optional Yield qualifier yq11.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq14.CPU0 input optional Yield qualifier yq14.CPU0 input optional Yield qualifier yq15.CPU0 input optional Yield qualifier yq16.CPU0 input optional Yield qualifier yq11.CPU0 input optional Yield qualifier yq11.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq14.CPU0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE0 input optional External interrupt hwint3.CPU0.VPE0 input optional External interrupt hwint4.CPU0.VPE0 input optional External interrupt hwint5.CPU0.VPE0 input optional External interrupt hwint5.CPU0.VPE0 input optional External interrupt hwint0.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint0.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint0.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE1 input optional External interrupt hwint2.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt	int38	input	optional	GIC external interrupt
yq0.CPU0 input optional Yield qualifier yq1.CPU0 input optional Yield qualifier yq2.CPU0 input optional Yield qualifier yq3.CPU0 input optional Yield qualifier yq4.CPU0 input optional Yield qualifier yq4.CPU0 input optional Yield qualifier yq5.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq7.CPU0 input optional Yield qualifier yq8.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq10.CPU0 input optional Yield qualifier yq11.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq13.CPU0 input optional Yield qualifier yq14.CPU0 input optional Yield qualifier yq15.CPU0 input optional Yield qualifier yq15.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE0 input optional External interrupt hwint3.CPU0.VPE0 input optional External interrupt hwint4.CPU0.VPE0 input optional External interrupt hwint5.CPU0.VPE0 input optional External interrupt hwint6.CPU0.VPE0 input optional External interrupt hwint7.CPU0.VPE0 input optional External interrupt hwint6.CPU0.VPE0 input optional External interrupt hwint7.CPU0.VPE0 input optional External interrupt hwint8.CPU0.VPE0 input optional External interrupt hwint9 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE1 input optional External interrupt hwint1.CPU0.VPE1 input optional External interrupt hwint2.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt	int39	input	optional	GIC external interrupt
yq1.CPU0inputoptionalYield qualifieryq2.CPU0inputoptionalYield qualifieryq3.CPU0inputoptionalYield qualifieryq4.CPU0inputoptionalYield qualifieryq5.CPU0inputoptionalYield qualifieryq6.CPU0inputoptionalYield qualifieryq7.CPU0inputoptionalYield qualifieryq8.CPU0inputoptionalYield qualifieryq9.CPU0inputoptionalYield qualifieryq10.CPU0inputoptionalYield qualifieryq11.CPU0inputoptionalYield qualifieryq12.CPU0inputoptionalYield qualifieryq13.CPU0inputoptionalYield qualifieryq14.CPU0inputoptionalYield qualifieryq15.CPU0inputoptionalYield qualifieryq15.CPU0.VPE0inputoptionalExternal interrupthwint1.CPU0.VPE0inputoptionalExternal interrupthwint2.CPU0.VPE0inputoptionalExternal interrupthwint3.CPU0.VPE0inputoptionalExternal interrupthwint4.CPU0.VPE0inputoptionalExternal interrupthwint5.CPU0.VPE0inputoptionalExternal interrupt for compatibilityvc_run_CPU0.VPE0inputoptionalExternal interrupthwint0.CPU0.VPE1inputoptionalExternal interrupthwint1.CPU0.VPE1inputoptionalE		input	optional	Yield qualifier
yq2_CPU0input inputoptional optionalYield qualifieryq3_CPU0input inputoptional optionalYield qualifieryq4_CPU0input inputoptional optionalYield qualifieryq6_CPU0input inputoptional optionalYield qualifieryq7_CPU0input inputoptional optionalYield qualifieryq9_CPU0input inputoptional optionalYield qualifieryq1_CPU0input inputoptional optionalYield qualifieryq1_CPU0input inputoptional optionalYield qualifieryq1_CPU0input inputoptional optionalYield qualifieryq1_CPU0input inputoptional optionalYield qualifieryq1_CPU0input inputoptionalYield qualifierhwint0_CPU0_VPE0input inputoptionalExternal interrupthwint1_CPU0_VPE0input inputoptionalExternal interrupthwint3_CPU0_VPE0input inputoptionalExternal interrupthwint4_CPU0_VPE0input inputoptionalExternal interrupthwint5_CPU0_VPE0input inputoptionalExternal interrupthwint0input inputoptionalExternal interrupthwint0_CPU0_VPE0input inputoptionalExternal interrupthwint0_CPU0_VPE1input inputoptionalExternal interrupthwint1_CPU0_VPE1input inputoptionalExternal interrupt <td></td> <td>input</td> <td>optional</td> <td>Yield qualifier</td>		input	optional	Yield qualifier
yq3.CPU0 input optional Yield qualifier yq4.CPU0 input optional Yield qualifier yq5.CPU0 input optional Yield qualifier yq6.CPU0 input optional Yield qualifier yq7.CPU0 input optional Yield qualifier yq8.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq9.CPU0 input optional Yield qualifier yq1.CPU0 input optional Yield qualifier yq11.CPU0 input optional Yield qualifier yq12.CPU0 input optional Yield qualifier yq13.CPU0 input optional Yield qualifier yq14.CPU0 input optional Yield qualifier yq15.CPU0 input optional Yield qualifier yq15.CPU0 input optional Yield qualifier hwint0.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint3.CPU0.VPE0 input optional External interrupt hwint4.CPU0.VPE0 input optional External interrupt hwint5.CPU0.VPE0 input optional External interrupt hwint0.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE0 input optional External interrupt hwint2.CPU0.VPE0 input optional External interrupt hwint3.CPU0.VPE0 input optional External interrupt hwint0.CPU0.VPE0 input optional External interrupt hwint0 input optional External interrupt hwint0.CPU0.VPE0 input optional External interrupt hwint0.CPU0.VPE0 input optional External interrupt hwint0.CPU0.VPE0 input optional External interrupt hwint1.CPU0.VPE1 input optional External interrupt hwint1.CPU0.VPE1 input optional External interrupt hwint2.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt hwint3.CPU0.VPE1 input optional External interrupt	yq1_CPU0	input	optional	Yield qualifier
yq4.CPU0inputoptionalYield qualifieryq5.CPU0inputoptionalYield qualifieryq6.CPU0inputoptionalYield qualifieryq7.CPU0inputoptionalYield qualifieryq8.CPU0inputoptionalYield qualifieryq9.CPU0inputoptionalYield qualifieryq10.CPU0inputoptionalYield qualifieryq11.CPU0inputoptionalYield qualifieryq12.CPU0inputoptionalYield qualifieryq13.CPU0inputoptionalYield qualifieryq14.CPU0inputoptionalYield qualifieryq15.CPU0inputoptionalYield qualifierhwint0.CPU0.VPE0inputoptionalExternal interrupthwint1.CPU0.VPE0inputoptionalExternal interrupthwint2.CPU0.VPE0inputoptionalExternal interrupthwint3.CPU0.VPE0inputoptionalExternal interrupthwint4.CPU0.VPE0inputoptionalExternal interrupthwint0inputoptionalExternal interrupthwint0inputoptionalExternal interrupt for compatibilityvc_run_CPU0.VPE0inputoptionalExternal interrupthwint1.CPU0.VPE1inputoptionalExternal interrupthwint2.CPU0.VPE1inputoptionalExternal interrupthwint3.CPU0.VPE1inputoptionalExternal interrupthwint3.CPU0.VPE1inputopt	yq2_CPU0	input	optional	Yield qualifier
yq5_CPU0 input optional Yield qualifier yq6_CPU0 input optional Yield qualifier yq7_CPU0 input optional Yield qualifier yq8_CPU0 input optional Yield qualifier yq9_CPU0 input optional Yield qualifier yq1_CPU0 input optional External interrupt hwint0_CPU0_VPE0 input optional External interrupt hwint1_CPU0_VPE0 input optional External interrupt hwint3_CPU0_VPE0 input optional External interrupt hwint4_CPU0_VPE0 input optional External interrupt hwint5_CPU0_VPE0 input optional External interrupt hwint6 input optional External interrupt hwint0 input optional External interrupt hwint0 input optional External interrupt hwint0 input optional External interrupt hwint1_CPU0_VPE0 input optional External interrupt hwint0 input optional External interrupt hwint1_CPU0_VPE0 input optional External interrupt hwint2_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt	yq3_CPU0	input	optional	Yield qualifier
yq6-CPU0 input optional Yield qualifier yq7-CPU0 input optional Yield qualifier yq8-CPU0 input optional Yield qualifier yq9-CPU0 input optional Yield qualifier yq10-CPU0 input optional Yield qualifier yq11-CPU0 input optional Yield qualifier yq12-CPU0 input optional Yield qualifier yq13-CPU0 input optional Yield qualifier yq14-CPU0 input optional Yield qualifier yq15-CPU0 input optional Yield qualifier yq15-CPU0 input optional Yield qualifier yq15-CPU0 input optional Yield qualifier hwint0-CPU0-VPE0 input optional External interrupt hwint1-CPU0-VPE0 input optional External interrupt hwint2-CPU0-VPE0 input optional External interrupt hwint3-CPU0-VPE0 input optional External interrupt hwint5-CPU0-VPE0 input optional External interrupt hwint5-CPU0-VPE0 input optional External interrupt hwint0 input optional External interrupt hwint1-CPU0-VPE0 input optional External interrupt hwint1-CPU0-VPE1 input optional External interrupt hwint2-CPU0-VPE1 input optional External interrupt hwint3-CPU0-VPE1 input optional External interrupt hwint3-CPU0-VPE1 input optional External interrupt hwint3-CPU0-VPE1 input optional External interrupt	yq4_CPU0	input	optional	Yield qualifier
yq7_CPU0 input optional Yield qualifier yq8_CPU0 input optional Yield qualifier yq9_CPU0 input optional Yield qualifier yq10_CPU0 input optional Yield qualifier yq11_CPU0 input optional Yield qualifier yq11_CPU0 input optional Yield qualifier yq12_CPU0 input optional Yield qualifier yq13_CPU0 input optional Yield qualifier yq14_CPU0 input optional Yield qualifier yq14_CPU0 input optional Yield qualifier yq15_CPU0 input optional Yield qualifier yq15_CPU0 input optional Yield qualifier hwint0_CPU0_VPE0 input optional External interrupt hwint1_CPU0_VPE0 input optional External interrupt hwint3_CPU0_VPE0 input optional External interrupt hwint4_CPU0_VPE0 input optional External interrupt hwint5_CPU0_VPE0 input optional External interrupt hwint0 input optional External interrupt for compatibility vc_run_CPU0_VPE0 input optional External interrupt for compatibility vc_run_CPU0_VPE0 input optional External interrupt hwint1_CPU0_VPE1 input optional External interrupt hwint1_CPU0_VPE1 input optional External interrupt hwint2_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt	yq5_CPU0	input	optional	Yield qualifier
yq8_CPU0inputoptionalYield qualifieryq9_CPU0inputoptionalYield qualifieryq10_CPU0inputoptionalYield qualifieryq11_CPU0inputoptionalYield qualifieryq12_CPU0inputoptionalYield qualifieryq13_CPU0inputoptionalYield qualifieryq14_CPU0inputoptionalYield qualifieryq15_CPU0inputoptionalYield qualifierhwint0_CPU0_VPE0inputoptionalExternal interrupthwint1_CPU0_VPE0inputoptionalExternal interrupthwint3_CPU0_VPE0inputoptionalExternal interrupthwint4_CPU0_VPE0inputoptionalExternal interrupthwint5_CPU0_VPE0inputoptionalExternal interrupthwint0inputoptionalExternal interrupt for compatibilityvc_run_CPU0_VPE0inputoptionalExternal interrupt for compatibilityvc_run_CPU0_VPE0inputoptionalExternal interrupthwint0_CPU0_VPE1inputoptionalExternal interrupthwint1_CPU0_VPE1inputoptionalExternal interrupthwint3_CPU0_VPE1inputoptionalExternal interrupthwint4_CPU0_VPE1inputoptionalExternal interrupthwint4_CPU0_VPE1inputoptionalExternal interrupt	yq6_CPU0	input	optional	Yield qualifier
yq9_CPU0 input optional Yield qualifier yq10_CPU0 input optional Yield qualifier yq11_CPU0 input optional Yield qualifier yq12_CPU0 input optional Yield qualifier yq13_CPU0 input optional Yield qualifier yq14_CPU0 input optional Yield qualifier yq15_CPU0 input optional Yield qualifier yq15_CPU0 input optional Yield qualifier yq15_CPU0 input optional Yield qualifier hwint0_CPU0_VPE0 input optional External interrupt hwint1_CPU0_VPE0 input optional External interrupt hwint3_CPU0_VPE0 input optional External interrupt hwint4_CPU0_VPE0 input optional External interrupt hwint5_CPU0_VPE0 input optional External interrupt hwint0 input optional External interrupt hwint0 input optional External interrupt for compatibility vc_run_CPU0_VPE0 input optional External interrupt for compatibility vc_run_CPU0_VPE0 input optional External interrupt hwint0 External interrupt for compatibility vc_run_CPU0_VPE0 input optional External interrupt hwint1_CPU0_VPE1 input optional External interrupt hwint1_CPU0_VPE1 input optional External interrupt hwint2_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt	yq7_CPU0	input	optional	Yield qualifier
yq10_CPU0inputoptionalYield qualifieryq11_CPU0inputoptionalYield qualifieryq12_CPU0inputoptionalYield qualifieryq13_CPU0inputoptionalYield qualifieryq14_CPU0inputoptionalYield qualifieryq15_CPU0inputoptionalExternal interrupthwint0_CPU0_VPE0inputoptionalExternal interrupthwint1_CPU0_VPE0inputoptionalExternal interrupthwint3_CPU0_VPE0inputoptionalExternal interrupthwint4_CPU0_VPE0inputoptionalExternal interrupthwint5_CPU0_VPE0inputoptionalExternal interrupthwint0inputoptionalExternal interrupt for compatibilityvc_run_CPU0_VPE0inputoptionalExternal interrupt for compatibilityvk_run_CPU0_VPE1inputoptionalExternal interrupthwint1_CPU0_VPE1inputoptionalExternal interrupthwint2_CPU0_VPE1inputoptionalExternal interrupthwint3_CPU0_VPE1inputoptionalExternal interrupthwint4_CPU0_VPE1inputoptionalExternal interrupthwint4_CPU0_VPE1inputoptionalExternal interrupt	yq8_CPU0	input	optional	Yield qualifier
yq11_CPU0 input optional Yield qualifier yq12_CPU0 input optional Yield qualifier yq13_CPU0 input optional Yield qualifier yq14_CPU0 input optional Yield qualifier yq15_CPU0 input optional Yield qualifier hwint0_CPU0_VPE0 input optional External interrupt hwint1_CPU0_VPE0 input optional External interrupt hwint3_CPU0_VPE0 input optional External interrupt hwint4_CPU0_VPE0 input optional External interrupt hwint5_CPU0_VPE0 input optional External interrupt hwint5_CPU0_VPE0 input optional External interrupt hwint0 input optional External interrupt hwint0 input optional External interrupt for compatibility vc_run_CPU0_VPE0 input optional External interrupt for compatibility vc_run_CPU0_VPE0 input optional External interrupt for compatibility External interrupt	yq9_CPU0	input	optional	Yield qualifier
yq12_CPU0 input optional Yield qualifier yq13_CPU0 input optional Yield qualifier yq14_CPU0 input optional Yield qualifier yq15_CPU0 input optional Yield qualifier hwint0_CPU0_VPE0 input optional External interrupt hwint1_CPU0_VPE0 input optional External interrupt hwint3_CPU0_VPE0 input optional External interrupt hwint4_CPU0_VPE0 input optional External interrupt hwint5_CPU0_VPE0 input optional External interrupt hwint5_CPU0_VPE0 input optional External interrupt hwint6_CPU0_VPE0 input optional External interrupt hwint0 input optional External interrupt for compatibility vc_run_CPU0_VPE0 input optional External interrupt for compatibility hwint0 External interrupt for compatibility External interrupt	yq10_CPU0	input	optional	Yield qualifier
yq13_CPU0 input optional Yield qualifier yq14_CPU0 input optional Yield qualifier yq15_CPU0 input optional Yield qualifier hwint0_CPU0_VPE0 input optional External interrupt hwint1_CPU0_VPE0 input optional External interrupt hwint3_CPU0_VPE0 input optional External interrupt hwint4_CPU0_VPE0 input optional External interrupt hwint5_CPU0_VPE0 input optional External interrupt hwint5_CPU0_VPE0 input optional External interrupt hwint0 input optional External interrupt hwint0 input optional External interrupt for compatibility vc_run_CPU0_VPE0 input optional Set to force stop of execution on processor VPE (simulation control only) hwint0_CPU0_VPE1 input optional External interrupt hwint1_CPU0_VPE1 input optional External interrupt hwint1_CPU0_VPE1 input optional External interrupt hwint1_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt	yq11_CPU0	input	optional	Yield qualifier
yq14_CPU0 input optional Yield qualifier yq15_CPU0_linput optional External interrupt hwint0_CPU0_VPE0 input optional External interrupt hwint1_CPU0_VPE0 input optional External interrupt hwint3_CPU0_VPE0 input optional External interrupt hwint4_CPU0_VPE0 input optional External interrupt hwint5_CPU0_VPE0 input optional External interrupt hwint5_CPU0_VPE0 input optional External interrupt hwint0 input optional External interrupt for compatibility vc_run_CPU0_VPE0 input optional External interrupt for compatibility vc_run_CPU0_VPE0 input optional External interrupt for compatibility hwint0 input optional External interrupt for compatibility vc_run_CPU0_VPE0 input optional External interrupt hwint1_CPU0_VPE1 input optional External interrupt hwint1_CPU0_VPE1 input optional External interrupt hwint2_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt	yq12_CPU0	input	optional	Yield qualifier
yq15_CPU0inputoptionalYield qualifierhwint0_CPU0_VPE0inputoptionalExternal interrupthwint1_CPU0_VPE0inputoptionalExternal interrupthwint2_CPU0_VPE0inputoptionalExternal interrupthwint3_CPU0_VPE0inputoptionalExternal interrupthwint5_CPU0_VPE0inputoptionalExternal interruptnmi_CPU0_VPE0inputoptionalNon-maskable external interrupthwint0inputoptionalExternal interrupt for compatibilityvc_run_CPU0_VPE0inputoptionalSet to force stop of execution on processorVPE (simulation control only)hwint0_CPU0_VPE1inputoptionalExternal interrupthwint1_CPU0_VPE1inputoptionalExternal interrupthwint2_CPU0_VPE1inputoptionalExternal interrupthwint3_CPU0_VPE1inputoptionalExternal interrupthwint4_CPU0_VPE1inputoptionalExternal interrupt	yq13_CPU0	input	optional	Yield qualifier
hwint0_CPU0_VPE0 input optional External interrupt hwint1_CPU0_VPE0 input optional External interrupt hwint2_CPU0_VPE0 input optional External interrupt hwint3_CPU0_VPE0 input optional External interrupt hwint5_CPU0_VPE0 input optional External interrupt hwint5_CPU0_VPE0 input optional External interrupt nmi_CPU0_VPE0 input optional External interrupt hwint0 input optional External interrupt for compatibility vc_run_CPU0_VPE0 input optional External interrupt for compatibility vc_run_CPU0_VPE0 input optional External interrupt for compatibility hwint0_CPU0_VPE0 input optional External interrupt bwint1_CPU0_VPE1 input optional External interrupt hwint1_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt External interrupt hwint4_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt	yq14_CPU0	input	optional	Yield qualifier
hwint0_CPU0_VPE0inputoptionalExternal interrupthwint1_CPU0_VPE0inputoptionalExternal interrupthwint2_CPU0_VPE0inputoptionalExternal interrupthwint3_CPU0_VPE0inputoptionalExternal interrupthwint4_CPU0_VPE0inputoptionalExternal interrupthwint5_CPU0_VPE0inputoptionalExternal interruptnmi_CPU0_VPE0inputoptionalExternal interrupt for compatibilityvc_run_CPU0_VPE0inputoptionalExternal interrupt for compatibilityhwint0_CPU0_VPE0inputoptionalExternal interrupt for compatibilityhwint1_CPU0_VPE1inputoptionalExternal interrupthwint1_CPU0_VPE1inputoptionalExternal interrupthwint2_CPU0_VPE1inputoptionalExternal interrupthwint3_CPU0_VPE1inputoptionalExternal interrupthwint4_CPU0_VPE1inputoptionalExternal interrupt	yq15_CPU0	input	optional	Yield qualifier
hwint2_CPU0_VPE0 input optional External interrupt hwint3_CPU0_VPE0 input optional External interrupt hwint4_CPU0_VPE0 input optional External interrupt hwint5_CPU0_VPE0 input optional External interrupt nmi_CPU0_VPE0 input optional Non-maskable external interrupt hwint0 input optional External interrupt for compatibility vc_run_CPU0_VPE0 input optional Set to force stop of execution on processor VPE (simulation control only) hwint0_CPU0_VPE1 input optional External interrupt hwint1_CPU0_VPE1 input optional External interrupt hwint2_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt External interrupt hwint4_CPU0_VPE1 input optional External interrupt External interrupt hwint4_CPU0_VPE1 input optional External interrupt External interrupt	hwint0_CPU0_VPE0		optional	External interrupt
hwint3_CPU0_VPE0 input optional External interrupt hwint4_CPU0_VPE0 input optional External interrupt hwint5_CPU0_VPE0 input optional External interrupt nmi_CPU0_VPE0 input optional Non-maskable external interrupt hwint0 input optional External interrupt for compatibility vc_run_CPU0_VPE0 input optional Set to force stop of execution on processor VPE (simulation control only) hwint0_CPU0_VPE1 input optional External interrupt hwint1_CPU0_VPE1 input optional External interrupt hwint2_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt External interrupt hwint4_CPU0_VPE1 input optional External interrupt	hwint1_CPU0_VPE0	input	optional	External interrupt
hwint4_CPU0_VPE0inputoptionalExternal interrupthwint5_CPU0_VPE0inputoptionalExternal interruptnmi_CPU0_VPE0inputoptionalNon-maskable external interrupthwint0inputoptionalExternal interrupt for compatibilityvc_run_CPU0_VPE0inputoptionalSet to force stop of execution on processor VPE (simulation control only)hwint0_CPU0_VPE1inputoptionalExternal interrupthwint1_CPU0_VPE1inputoptionalExternal interrupthwint2_CPU0_VPE1inputoptionalExternal interrupthwint3_CPU0_VPE1inputoptionalExternal interrupthwint4_CPU0_VPE1inputoptionalExternal interrupt	hwint2_CPU0_VPE0	input	optional	External interrupt
hwint5_CPU0_VPE0inputoptionalExternal interruptnmi_CPU0_VPE0inputoptionalNon-maskable external interrupthwint0inputoptionalExternal interrupt for compatibilityvc_run_CPU0_VPE0inputoptionalSet to force stop of execution on processor VPE (simulation control only)hwint0_CPU0_VPE1inputoptionalExternal interrupthwint1_CPU0_VPE1inputoptionalExternal interrupthwint2_CPU0_VPE1inputoptionalExternal interrupthwint3_CPU0_VPE1inputoptionalExternal interrupthwint4_CPU0_VPE1inputoptionalExternal interrupt	hwint3_CPU0_VPE0	input	optional	External interrupt
nmi_CPU0_VPE0inputoptionalNon-maskable external interrupthwint0inputoptionalExternal interrupt for compatibilityvc_run_CPU0_VPE0inputoptionalSet to force stop of execution on processor VPE (simulation control only)hwint0_CPU0_VPE1inputoptionalExternal interrupthwint1_CPU0_VPE1inputoptionalExternal interrupthwint2_CPU0_VPE1inputoptionalExternal interrupthwint3_CPU0_VPE1inputoptionalExternal interrupthwint4_CPU0_VPE1inputoptionalExternal interrupt	hwint4_CPU0_VPE0	input	optional	External interrupt
nmi_CPU0_VPE0inputoptionalNon-maskable external interrupthwint0inputoptionalExternal interrupt for compatibilityvc_run_CPU0_VPE0inputoptionalSet to force stop of execution on processor VPE (simulation control only)hwint0_CPU0_VPE1inputoptionalExternal interrupthwint1_CPU0_VPE1inputoptionalExternal interrupthwint2_CPU0_VPE1inputoptionalExternal interrupthwint3_CPU0_VPE1inputoptionalExternal interrupthwint4_CPU0_VPE1inputoptionalExternal interrupt	hwint5_CPU0_VPE0	input	optional	External interrupt
vc_run_CPU0_VPE0inputoptionalSet to force stop of execution on processor VPE (simulation control only)hwint0_CPU0_VPE1inputoptionalExternal interrupthwint1_CPU0_VPE1inputoptionalExternal interrupthwint2_CPU0_VPE1inputoptionalExternal interrupthwint3_CPU0_VPE1inputoptionalExternal interrupthwint4_CPU0_VPE1inputoptionalExternal interrupt	nmi_CPU0_VPE0	input	optional	Non-maskable external interrupt
hwint0_CPU0_VPE1inputoptionalExternal interrupthwint1_CPU0_VPE1inputoptionalExternal interrupthwint2_CPU0_VPE1inputoptionalExternal interrupthwint3_CPU0_VPE1inputoptionalExternal interrupthwint4_CPU0_VPE1inputoptionalExternal interrupthwint4_CPU0_VPE1inputoptionalExternal interrupt	hwint0	input	optional	External interrupt for compatibility
hwint0_CPU0_VPE1 input optional External interrupt hwint1_CPU0_VPE1 input optional External interrupt hwint2_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt	vc_run_CPU0_VPE0	input	optional	Set to force stop of execution on processor
hwint1_CPU0_VPE1 input optional External interrupt hwint2_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt				
hwint1_CPU0_VPE1 input optional External interrupt hwint2_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt	hwint0_CPU0_VPE1	input	optional	External interrupt
hwint2_CPU0_VPE1 input optional External interrupt hwint3_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt	hwint1_CPU0_VPE1		optional	External interrupt
hwint3_CPU0_VPE1 input optional External interrupt hwint4_CPU0_VPE1 input optional External interrupt	hwint2_CPU0_VPE1			_
hwint4_CPU0_VPE1 input optional External interrupt	hwint3_CPU0_VPE1		_	External interrupt
	hwint4_CPU0_VPE1			
	hwint5_CPU0_VPE1	input		External interrupt
nmi_CPU0_VPE1 input optional Non-maskable external interrupt	nmi_CPU0_VPE1		optional	_

vc_run_CPU0_VPE1	input	optional	Set to force stop of execution on processor
verunier corvini	Impac	optionar	VPE (simulation control only)
yq_CPU1	input	optional	Yield qualifier
yq0_CPU1	input	optional	Yield qualifier
yq1_CPU1	input	optional	Yield qualifier
yq2_CPU1	input	optional	Yield qualifier
yq3_CPU1	input	optional	Yield qualifier
yq4_CPU1	input	optional	Yield qualifier
yq5_CPU1	input	optional	Yield qualifier
yq6_CPU1	input	optional	Yield qualifier
yq7_CPU1	input	optional	Yield qualifier
yq8_CPU1	input	optional	Yield qualifier
yq9_CPU1	input	optional	Yield qualifier
yq10_CPU1	input	optional	Yield qualifier
yq11_CPU1	input	optional	Yield qualifier
yq12_CPU1	input	optional	Yield qualifier
yq13_CPU1	input	optional	Yield qualifier
yq14_CPU1	input	optional	Yield qualifier
yq15_CPU1	input	optional	Yield qualifier
hwint0_CPU1_VPE0	input	optional	External interrupt
hwint1_CPU1_VPE0	input	optional	External interrupt
hwint2_CPU1_VPE0	input	optional	External interrupt
hwint3_CPU1_VPE0	input	optional	External interrupt
hwint4_CPU1_VPE0	input	optional	External interrupt
hwint5_CPU1_VPE0	input	optional	External interrupt
nmi_CPU1_VPE0	input	optional	Non-maskable external interrupt
vc_run_CPU1_VPE0	input	optional	Set to force stop of execution on processor
		_	VPE (simulation control only)
hwint0_CPU1_VPE1	input	optional	External interrupt
hwint1_CPU1_VPE1	input	optional	External interrupt
hwint2_CPU1_VPE1	input	optional	External interrupt
hwint3_CPU1_VPE1	input	optional	External interrupt
hwint4_CPU1_VPE1	input	optional	External interrupt
hwint5_CPU1_VPE1	input	optional	External interrupt
nmi_CPU1_VPE1	input	optional	Non-maskable external interrupt
vc_run_CPU1_VPE1	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)
yq_CPU2	input	optional	Yield qualifier
yq0_CPU2	input	optional	Yield qualifier
yq1_CPU2	input	optional	Yield qualifier
yq2_CPU2	input	optional	Yield qualifier
yq3_CPU2	input	optional	Yield qualifier
yq4_CPU2	input	optional	Yield qualifier
yq5_CPU2	input	optional	Yield qualifier
yq6_CPU2	input	optional	Yield qualifier

yq7_CPU2	input	optional	Yield qualifier
yq8_CPU2			Yield qualifier
yq9_CPU2	input	optional optional	Yield qualifier
yq10_CPU2	input	optional	Yield qualifier
yq10_CF 02 yq11_CPU2	input		
yq12_CPU2	input	optional	Yield qualifier Violat qualifier
	input	optional	Yield qualifier
yq13_CPU2	input	optional	Yield qualifier
yq14_CPU2	input	optional	Yield qualifier
yq15_CPU2	input	optional	Yield qualifier
hwint0_CPU2_VPE0	input	optional	External interrupt
hwint1_CPU2_VPE0	input	optional	External interrupt
hwint2_CPU2_VPE0	input	optional	External interrupt
hwint3_CPU2_VPE0	input	optional	External interrupt
hwint4_CPU2_VPE0	input	optional	External interrupt
hwint5_CPU2_VPE0	input	optional	External interrupt
nmi_CPU2_VPE0	input	optional	Non-maskable external interrupt
vc_run_CPU2_VPE0	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)
hwint0_CPU2_VPE1	input	optional	External interrupt
hwint1_CPU2_VPE1	input	optional	External interrupt
hwint2_CPU2_VPE1	input	optional	External interrupt
hwint3_CPU2_VPE1	input	optional	External interrupt
hwint4_CPU2_VPE1	input	optional	External interrupt
hwint5_CPU2_VPE1	input	optional	External interrupt
nmi_CPU2_VPE1	input	optional	Non-maskable external interrupt
vc_run_CPU2_VPE1	input	optional	Set to force stop of execution on processor
		_	VPE (simulation control only)
yq_CPU3	input	optional	Yield qualifier
yq0_CPU3	input	optional	Yield qualifier
yq1_CPU3	input	optional	Yield qualifier
yq2_CPU3	input	optional	Yield qualifier
yq3_CPU3	input	optional	Yield qualifier
yq4_CPU3	input	optional	Yield qualifier
yq5_CPU3	input	optional	Yield qualifier
yq6_CPU3	input	optional	Yield qualifier
yq7_CPU3	input	optional	Yield qualifier
yq8_CPU3	input	optional	Yield qualifier
yq9_CPU3	input	optional	Yield qualifier
yq10_CPU3	input	optional	Yield qualifier
yq11_CPU3	input	optional	Yield qualifier
yq12_CPU3	input	optional	Yield qualifier
yq13_CPU3	input	optional	Yield qualifier
yq14_CPU3	input	optional	Yield qualifier
yq15_CPU3	input	optional	Yield qualifier
hwint0_CPU3_VPE0	_	optional	External interrupt
IIWIIIUU_CI U3_V F EU	input	орионаг	External interrupt

hwint1_CPU3_VPE0	input	optional	External interrupt
hwint2_CPU3_VPE0	input	optional	External interrupt
hwint3_CPU3_VPE0	input	optional	External interrupt
hwint4_CPU3_VPE0	input	optional	External interrupt
hwint5_CPU3_VPE0	input	optional	External interrupt
nmi_CPU3_VPE0	input	optional	Non-maskable external interrupt
vc_run_CPU3_VPE0	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)
hwint0_CPU3_VPE1	input	optional	External interrupt
hwint1_CPU3_VPE1	input	optional	External interrupt
hwint2_CPU3_VPE1	input	optional	External interrupt
hwint3_CPU3_VPE1	input	optional	External interrupt
hwint4_CPU3_VPE1	input	optional	External interrupt
hwint5_CPU3_VPE1	input	optional	External interrupt
nmi_CPU3_VPE1	input	optional	Non-maskable external interrupt
vc_run_CPU3_VPE1	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)

Table 6.1: Net Ports

FIFO Ports

This model has no FIFO ports.

Formal Parameters

Name	Type	Description
variant	Enumeration	Processor variant
endian	Endian	Model endian
cacheenable	Enumeration	Select cache model mode (default, tag or full)
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info structure
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for
		AVP test termination)
cacheIndexBypassTLB	Boolean	When set, cache index ops do not generate TLB exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
supervisorMode	Boolean	Override whether processor implements supervisor mode
busErrors	Boolean	Override bus error exception behavior. When true, ac-
		cesses of memory not defined by platform will cause bus
		error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when
		true (sets Config.MT=3, Config.KU/K23=2 and Con-
		fig1.MMUSizeM1=0)
removeDSP	Boolean	Override the DSP-present configuration when true (sets
		Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true (sets
		Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true (sets
		Config1.FP to 0)
isISA	Boolean	Enable to specify ISA model (reset address from ELF, all
		coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to maximum
		value to improve performance
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores only)
ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC imple-
		mentation (MT cores only)
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior, 2:new
		mttc1 behavior)
supportDenormals	Boolean	Enable to specify that the FPU supports denormal
		operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0
mpuRegions	Uns32	Number of regions for memory protection unit
mpuType	Uns32	Type of MPU implementation
mpuEnable	Boolean	Enable MPU2 segment control at reset
mpuSegment0	Uns32	Attributes for segment 0 in MPU2 SegmentControl_0 reg-
		ister

	Uns32	Attributes for segment 1 in MPU2 SegmentControl_0 reg-
mpuSegment1		ister
mpuSegment2	Uns32	Attributes for segment 2 in MPU2 SegmentControl_0 register
mpuSegment3	Uns32	Attributes for segment 3 in MPU2 SegmentControl_0 register
mpuSegment4	Uns32	Attributes for segment 4 in MPU2 SegmentControl_1 register
mpuSegment5	Uns32	Attributes for segment 5 in MPU2 SegmentControl_1 register
mpuSegment6	Uns32	Attributes for segment 6 in MPU2 SegmentControl_1 register
mpuSegment7	Uns32	Attributes for segment 7 in MPU2 SegmentControl_1 register
mpuSegment8	Uns32	Attributes for segment 8 in MPU2 SegmentControl_2 register
mpuSegment9	Uns32	Attributes for segment 9 in MPU2 SegmentControl_2 register
mpuSegment10	Uns32	Attributes for segment 10 in MPU2 SegmentControl_2 register
mpuSegment11	Uns32	Attributes for segment 11 in MPU2 SegmentControl_2 register
mpuSegment12	Uns32	Attributes for segment 12 in MPU2 SegmentControl_3 register
mpuSegment13	Uns32	Attributes for segment 13 in MPU2 SegmentControl_3 register
mpuSegment14	Uns32	Attributes for segment 14 in MPU2 SegmentControl_3 register
mpuSegment15	Uns32	Attributes for segment 15 in MPU2 SegmentControl_3 register
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
hasFDC	Uns32	Specify the size of Fast Debug Channel register block
statusFR	Boolean	Override power on value in Status.FR (Floating point register mode)
configDSP	Boolean	Override Config.DSP (data scratchpad RAM present)
configISP	Boolean	Override Config.ISP (instruction scratchpad RAM present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0 cacheability)
configKU	Uns32	Override power on value of Config.KU (set Useg cacheability)
configK23	Uns32	Override power on value of Config.K23 (set Kseg23 cacheability)
configMDU	Boolean	Override Config.MDU (iterative multiply/divide unit)
configMM	Boolean	Override Config.MM (merging mode for write)
configMT	Uns32	Override Config.MT
configSB	Boolean	Override Config.SB (simple bus transfers only)
MIPS16eASE	Boolean	Override Config1.CA (enables the MIPS16e ASE)
config1DA	Uns32	Override Config1.DA (Deache associativity)
config1DL	Uns32	Override Config1.DL (Deache line size)
	Uns32	Override Config1.DS (Deache sets per way)
CONTIGILIS		
config1DS config1EP	Boolean	Override Config1.EP (EJTag present)

config1IL	Uns32	Override Config1.IL (Icache line size)
config1IS	Uns32	Override Config1.IS (Icache sets per way)
config1MMUSizeM1	Uns32	Override Config1.MMUSizeM1 (number of MMU entries-
-		1)
config1WR	Boolean	Override Config1.WR (watchpoint registers present)
config1FP	Boolean	Override Config1.FP (FPU present)
config3BI	Boolean	Override Config3.BI
config3BP	Boolean	Override Config3.BP
config3CDMM	Boolean	Override Config3.CDMM
config3CTXTC	Boolean	Override Config3.CTXTC
config3DSPP	Boolean	Override Config3.DSPP
config3DSP2P	Boolean	Override Config3.DSP2P
config3IPLW	Uns32	Override Config3.IPLW
config3ISA	Uns32	Override Config3.ISA
config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3ITL	Boolean	Override Config3.ITL
config3MCU	Boolean	Override Config3.MCU
config3MMAR	Uns32	Override Config3.MMAR
config3RXI	Boolean	Override Config3.RXI
config3SC	Boolean	Override Config3.SC
config3ULRI	Boolean	Override Config3.ULRI
externalinterrupt	Boolean	Override Config3.VEIC (enables the use of an external in-
externamierrapt	Boolean	terrupt controller)
vectoredinterrupt	Boolean	Override Config3.VInt (enables vectored interrupts)
config3VZ	Boolean	Override Config3.VZ
config4AE	Boolean	Override Config4.AE
config4IE	Uns32	Override Config4.IE Override Config4.IE
config4MMUConfig	Uns32	Override Config 4.MMUConfig field (interpretation de-
coming invitate coming	0.11502	pends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.VTLBSizeExt
config5EVA	Boolean	Override Config5.EVA
config5NFExists	Boolean	Override Config5.NFExists
config5MSAEn	Boolean	Override Config5.MSAEn
config6FTLBEn	Boolean	Override power on value of Config6.FTLBEn
config7AR	Boolean	Override Config7.AR (Alias removed Data cache)
config7DCIDX_MODE	Uns32	Override Config7.DCIDX_MODE
config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initialization)
config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)
fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant with
105111252000	Boolean	IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/SNaN encodings match
	20010411	IEEE 754-2008 recommendation)
firPS	Boolean	Override FIR.PS (PS floating point type implemented)
firHas2008	Boolean	Override FIR.Has2008 (one or more IEEE 754-2008 fea-
	20010411	tures present)
intctlIPFDC	Uns32	Override IntCtl.IPFDC
intctllPTI	Uns32	Override IntCtl.IPTI
pridRevision	Uns32	Override PRId.Revision
srsctlHSS	Uns32	Override SRSCtl.HSS (number of shadow register sets)
ExceptionBase	Uns32	
		GCR_Cx_RESET_BASE on CMP processors)
UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the correspond-
		ing BEV address bits

first BEVException Base Mask Bit	Uns32	Specify LSB position of GCR_Cx_RESET_EXT_BASE. BEVExceptionBaseMask field. Only used when SegCtl
		present
EVAReset	Boolean	Set to one to reset into non-legacy address map and BEV location. Only used when non-CMP and SegCtl present
ExceptionBaseMask	Uns32	Specify the ExceptionBaseMask value used for bits [27:firstBEVExceptionBaseMaskBit]. Only used when non-CMP and SegCtl present
ExceptionBasePA	Uns32	Bits [35:29] of the physical address for the BEV overlays. Only used when non-CMP and SegCtl present
GIC_EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable within cluster
GCR_PCORES	Uns32	CMP system only: override GCR_CONFIG.PCORES (number of cores-1)
GCR_BASE	Uns32	CMP system only: override GCR_BASE.GCR_BASE (default GCR register address)
GCR_MINOR_REV	Uns32	CMP system only: override GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	CMP system only: override GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MAJOR_REV
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MAJOR_REV
GIC_NUMINTERRUPTS	Uns32	CMP system only: override GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MAJOR_REV
GIC_PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPES
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY
CPC_RESETLEN	Uns32	CMP system only: override CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override CPC_REVISION.MAJOR_REV
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 3
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 0. Only used when SegCtl present
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 1. Only used when SegCtl present

GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core
		2. Only used when SegCtl present
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core
		3. Only used when SegCtl present
EIC_OPTION	Uns32	Override the external interrupt controller EIC_OPTION
ISPRAM_SIZE	Uns32	Encoded size of the ISPRAM region (log2(<ispram size<="" td=""></ispram>
		in bytes>) - 11)
ISPRAM_BASE	Uns64	Starting physical address of the ISPRAM region
ISPRAM_ENABLE	Boolean	Set the enable bit of the ISPRAM region's tag (used to
		enable the ISPRAM region prior to reset)
ISPRAM_FILE	String	Load a MIPS hex file into the ISPRAM region prior to
		reset
DSPRAM_SIZE	Uns32	Encoded size of the DSPRAM region (log2(<dspram< td=""></dspram<>
		size in bytes>) - 11)
DSPRAM_BASE	Uns64	Starting physical address of the DSPRAM region
DSPRAM_ENABLE	Boolean	Set the enable bit of the DSPRAM region's tag (used to
		enable the DSPRAM region prior to reset)

Table 8.1: Parameters that can be set in: CMP

Name	Type	Description
endian	Endian	Model endian
cacheenable	Enumeration	Select cache model mode (default, tag or full)
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info structure
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for AVP test termination)
cacheIndexBypassTLB	Boolean	When set, cache index ops do not generate TLB exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
supervisorMode	Boolean	Override whether processor implements supervisor mode
busErrors	Boolean	Override bus error exception behavior. When true, accesses of memory not defined by platform will cause bus error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when true (sets Config.MT=3, Config.KU/K23=2 and Config1.MMUSizeM1=0)
removeDSP	Boolean	Override the DSP-present configuration when true (sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true (sets Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true (sets Config1.FP to 0)
isISA	Boolean	Enable to specify ISA model (reset address from ELF, all coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to maximum value to improve performance
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores only)
ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC implementation (MT cores only)
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior, 2:new mttc1 behavior)
support Denormals	Boolean	Enable to specify that the FPU supports denormal operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0
mpuRegions	Uns32	Number of regions for memory protection unit

mpuType	Uns32	Type of MPU implementation
mpuEnable	Boolean	Enable MPU2 segment control at reset
mpuSegment0	Uns32	Attributes for segment 0 in MPU2 SegmentControl_0 reg-
		ister
mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentControl_0 reg-
		ister
mpuSegment2	Uns32	Attributes for segment 2 in MPU2 SegmentControl_0 reg-
		ister
mpuSegment3	Uns32	Attributes for segment 3 in MPU2 SegmentControl_0 reg-
		ister
mpuSegment4	Uns32	Attributes for segment 4 in MPU2 SegmentControl_1 reg-
		ister
mpuSegment5	Uns32	Attributes for segment 5 in MPU2 SegmentControl_1 reg-
		ister
mpuSegment6	Uns32	Attributes for segment 6 in MPU2 SegmentControl_1 reg-
G	11 00	ister
mpuSegment7	Uns32	Attributes for segment 7 in MPU2 SegmentControl_1 reg-
G 10	II 20	Attributes for segment 8 in MPU2 SegmentControl_2 reg-
mpuSegment8	Uns32	Attributes for segment 8 in MPO2 SegmentControl_2 register
mpuSegment9	Uns32	Attributes for segment 9 in MPU2 SegmentControl_2 reg-
mpusegments	Ulis52	ister
mpuSegment10	Uns32	Attributes for segment 10 in MPU2 SegmentControl_2 reg-
mpusegmentio	011852	ister
mpuSegment11	Uns32	Attributes for segment 11 in MPU2 SegmentControl_2 reg-
mpusegment11	011852	ister
mpuSegment12	Uns32	Attributes for segment 12 in MPU2 SegmentControl_3 reg-
inpusegment12	0.11502	ister
mpuSegment13	Uns32	Attributes for segment 13 in MPU2 SegmentControl_3 reg-
	0 0	ister
mpuSegment14	Uns32	Attributes for segment 14 in MPU2 SegmentControl_3 reg-
		ister
mpuSegment15	Uns32	Attributes for segment 15 in MPU2 SegmentControl_3 reg-
		ister
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
hasFDC	Uns32	Specify the size of Fast Debug Channel register block
statusFR	Boolean	Override power on value in Status.FR (Floating point reg-
		ister mode)
configDSP	Boolean	Override Config.DSP (data scratchpad RAM present)
configISP	Boolean	Override Config.ISP (instruction scratchpad RAM
		present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0 cacheabil-
		ity)
configKU	Uns32	Override power on value of Config.KU (set Useg cacheabil-
6 1700	TT 00	ity)
configK23	Uns32	Override power on value of Config.K23 (set Kseg23
C MDII	D 1	cacheability)
configMDU	Boolean	Override Config.MDU (iterative multiply/divide unit)
configMM	Boolean	Override Config.MM (merging mode for write)
configMT	Uns32	Override Config.MT
configSB	Boolean	Override Config.SB (simple bus transfers only)
MIPS16eASE	Boolean	Override Config1.CA (enables the MIPS16e ASE) Override Config1.DA (Deache associativity)
config1DA	Uns32	Override Comigr.DA (Deache associativity)

config1DL	Uns32	Override Config1.DL (Deache line size)
config1DS	Uns32	Override Config1.DS (Deache sets per way)
config1EP	Boolean	Override Config1.EP (EJTag present)
config1IA	Uns32	Override Config1.IA (Icache associativity)
config1IL	Uns32	Override Config1.IL (Icache line size)
config1IS	Uns32	Override Config1.IS (Icache ests per way)
		Override Config1.MMUSizeM1 (number of MMU entries-
config1MMUSizeM1	Uns32	- '
C 4HID	D 1	1)
config1WR	Boolean	Override Config1.WR (watchpoint registers present)
config1FP	Boolean	Override Config1.FP (FPU present)
config3BI	Boolean	Override Config3.BI
config3BP	Boolean	Override Config3.BP
config3CDMM	Boolean	Override Config3.CDMM
config3CTXTC	Boolean	Override Config3.CTXTC
config3DSPP	Boolean	Override Config3.DSPP
config3DSP2P	Boolean	Override Config3.DSP2P
config3IPLW	Uns32	Override Config3.IPLW
config3ISA	Uns32	Override Config3.ISA
config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3ITL	Boolean	Override Config3.ITL
config3MCU	Boolean	Override Config3.MCU
config3MMAR	Uns32	Override Config3.MMAR
config3RXI	Boolean	Override Config3.RXI
config3SC	Boolean	Override Config3.SC
config3ULRI	Boolean	Override Config3.ULRI
externalinterrupt	Boolean	Override Config3.VEIC (enables the use of an external in-
externamiterrupt	Doolean	terrupt controller)
vectoredinterrupt	Boolean	Override Config3.VInt (enables vectored interrupts)
config3VZ	Boolean	Override Config3.VZ
config4AE	Boolean	Override Config4.AE
config4IE	Uns32	Override Config4.IE
config4MMUConfig	Uns32	Override Config4.MMUConfig field (interpretation de-
come min come	0 11502	pends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.VTLBSizeExt
config5EVA	Boolean	Override Config5.EVA
config5NFExists	Boolean	Override Config5.NFExists
config5MSAEn	Boolean	Override Config5.MSAEn
	Boolean	
config6FTLBEn		Override power on value of Config6.FTLBEn
config7AR	Boolean	Override Config7.AR (Alias removed Data cache)
config7DCIDX_MODE	Uns32	Override Config7.DCIDX_MODE
config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initialization)
config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)
fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant with
		IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/SNaN encodings match
		IEEE 754-2008 recommendation)
firPS	Boolean	Override FIR.PS (PS floating point type implemented)
firHas2008	Boolean	Override FIR.Has2008 (one or more IEEE 754-2008 fea-
		tures present)
intctlIPFDC	Uns32	Override IntCtl.IPFDC
intctlIPTI	Uns32	Override IntCtl.IPTI
pridRevision	Uns32	Override PRId.Revision
srsctlHSS	Uns32	Override SRSCtl.HSS (number of shadow register sets)
2120011100	011502	2. STITES STEED (HUIIDOL OF SHEEDW TOSISHOL SCIS)

ExceptionBase	Uns32	Specify the BEV Exception Base address. (use GCR_Cx_RESET_BASE on CMP processors)
UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the corresponding BEV address bits
first BEVException Base Mask Bit	Uns32	Specify LSB position of GCR_Cx_RESET_EXT_BASE. BEVExceptionBaseMask field. Only used when SegCtl present
EVAReset	Boolean	Set to one to reset into non-legacy address map and BEV location. Only used when non-CMP and SegCtl present
ExceptionBaseMask	Uns32	Specify the ExceptionBaseMask value used for bits [27:firstBEVExceptionBaseMaskBit]. Only used when non-CMP and SegCtl present
ExceptionBasePA	Uns32	Bits [35:29] of the physical address for the BEV overlays. Only used when non-CMP and SegCtl present
GIC_EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable within cluster
GCR_PCORES	Uns32	CMP system only: override GCR_CONFIG.PCORES (number of cores-1)
GCR_BASE	Uns32	CMP system only: override GCR_BASE.GCR_BASE (default GCR register address)
GCR_MINOR_REV	Uns32	CMP system only: override GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	CMP system only: override GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MAJOR_REV
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MAJOR_REV
GIC_NUMINTERRUPTS	Uns32	CMP system only: override GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MAJOR_REV
GIC_PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPES
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY
CPC_RESETLEN	Uns32	CMP system only: override CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override CPC_REVISION.MAJOR_REV
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 3

GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core
		0. Only used when SegCtl present
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core
		1. Only used when SegCtl present
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core
		2. Only used when SegCtl present
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core
		3. Only used when SegCtl present
EIC_OPTION	Uns32	Override the external interrupt controller EIC_OPTION
ISPRAM_SIZE	Uns32	Encoded size of the ISPRAM region (log2(<ispram size<="" td=""></ispram>
		in bytes>) - 11)
ISPRAM_BASE	Uns64	Starting physical address of the ISPRAM region
ISPRAM_ENABLE	Boolean	Set the enable bit of the ISPRAM region's tag (used to
		enable the ISPRAM region prior to reset)
ISPRAM_FILE	String	Load a MIPS hex file into the ISPRAM region prior to
		reset
DSPRAM_SIZE	Uns32	Encoded size of the DSPRAM region (log2(<dspram< td=""></dspram<>
		size in bytes>) - 11)
DSPRAM_BASE	Uns64	Starting physical address of the DSPRAM region
DSPRAM_ENABLE	Boolean	Set the enable bit of the DSPRAM region's tag (used to
		enable the DSPRAM region prior to reset)

Table 8.2: Parameters that can be set in: CPU

Name	Type	Description
endian	Endian	Model endian
cacheenable	Enumeration	Select cache model mode (default, tag or full)
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info structure
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for
		AVP test termination)
cacheIndexBypassTLB	Boolean	When set, cache index ops do not generate TLB exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
supervisorMode	Boolean	Override whether processor implements supervisor mode
busErrors	Boolean	Override bus error exception behavior. When true, ac-
		cesses of memory not defined by platform will cause bus
		error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when
		true (sets Config.MT=3, Config.KU/K23=2 and Con-
		fig1.MMUSizeM1=0)
removeDSP	Boolean	Override the DSP-present configuration when true (sets
		Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true (sets
		Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true (sets
. 70.1		Config1.FP to 0)
isISA	Boolean	Enable to specify ISA model (reset address from ELF, all
1:11 TDLD 4:	D. I	coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to maximum
TOTAL TO A	11 00	value to improve performance
ITCNumEntries ITCNumFIFO	Uns32	Specify number of ITC cells present (MT cores only)
11 CNUMFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC implementation (MT cores cells)
MEEDII	II20	mentation (MT cores only)
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior, 2:new mttc1 behavior)
		muter behavior)

support Denormals	Boolean	Enable to specify that the FPU supports denormal operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0
mpuRegions	Uns32	Number of regions for memory protection unit
mpuType	Uns32	Type of MPU implementation
mpuEnable	Boolean	Enable MPU2 segment control at reset
	Uns32	Attributes for segment 0 in MPU2 SegmentControl_0 reg-
mpuSegment0		ister
mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentControl_0 register
mpuSegment2	Uns32	Attributes for segment 2 in MPU2 SegmentControl_0 register
mpuSegment3	Uns32	Attributes for segment 3 in MPU2 SegmentControl_0 register
mpuSegment4	Uns32	Attributes for segment 4 in MPU2 SegmentControl_1 register
mpuSegment5	Uns32	Attributes for segment 5 in MPU2 SegmentControl_1 register
mpuSegment6	Uns32	Attributes for segment 6 in MPU2 SegmentControl_1 register
mpuSegment7	Uns32	Attributes for segment 7 in MPU2 SegmentControl_1 register
mpuSegment8	Uns32	Attributes for segment 8 in MPU2 SegmentControl_2 register
mpuSegment9	Uns32	Attributes for segment 9 in MPU2 SegmentControl_2 register
mpuSegment10	Uns32	Attributes for segment 10 in MPU2 SegmentControl_2 register
mpuSegment11	Uns32	Attributes for segment 11 in MPU2 SegmentControl_2 register
mpuSegment12	Uns32	Attributes for segment 12 in MPU2 SegmentControl_3 register
mpuSegment13	Uns32	Attributes for segment 13 in MPU2 SegmentControl_3 register
mpuSegment14	Uns32	Attributes for segment 14 in MPU2 SegmentControl_3 register
mpuSegment15	Uns32	Attributes for segment 15 in MPU2 SegmentControl_3 register
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
hasFDC	Uns32	Specify the size of Fast Debug Channel register block
statusFR	Boolean	Override power on value in Status.FR (Floating point register mode)
configDSP	Boolean	Override Config.DSP (data scratchpad RAM present)
configISP	Boolean	Override Config.ISP (instruction scratchpad RAM present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0 cacheability)
configKU	Uns32	Override power on value of Config.KU (set Useg cacheability)
configK23	Uns32	Override power on value of Config.K23 (set Kseg23 cacheability)
configMDU	Boolean	Override Config.MDU (iterative multiply/divide unit)
configMM	Boolean	Override Config.MM (merging mode for write)

Doubleman Doub	configMT	Uns32	Override Config.MT
MIPS16eASE			
config1DA			
config1DL Uns32			,
Description			
config1IA Uns32 Override Config1IA (Icache associativity)			
config1IL Uns32 Override Config1.II. (Icache line size)			
config1IM			
config1MMUSizeM1			
1) 10 10 10 10 10 10 10			
config1WR config1FP Boolean Override Config1.WR (watchpoint registers present) Config1FP Boolean Override Config1.FP (FPU present) Override Config3.BI Boolean Override Config3.BP Config3BP Boolean Override Config3.DP Config3CDMM Boolean Override Config3.CDMM Override Config3.CDMM Config3CTXTC Boolean Override Config3.CDMM Config3DSPP Boolean Override Config3.DSPP Config3DSPP Boolean Override Config3.DSPP Config3DSPP Config3DSPP Boolean Override Config3.DSPP Config3ISA Uns32 Override Config3.ISA Config3ISA Uns32 Override Config3.ISA Config3ISA Uns32 Override Config3.ISA Config3ITL Config3MCU Boolean Override Config3.ITL Config3MCU Boolean Override Config3.MCU Config3MCI Boolean Override Config3.RXI Config3RXI Config3RXI Boolean Override Config3.RXI Config3BC Boolean Override Config3.RXI Config3SC Override Config3.NCU Config3ACU Config3AC Override Config3.VEIC (enables the use of an external terrupt controller) vectoredinterrupt Boolean Override Config3.VInt (enables vectored interrupts) Config4AC Config5AC Config5AC Config5AC Config5AC Config5AC Config5AC Config5AC Config6AC Co	ConngTWIVIOSizeWII	Ulisaz	_ ,
Config3IFP Boolean Override Config3.IFP (FPU present)	config1WB	Rooloan	1 /
Config3BI			
Config3DP			
Config3CDMM			
config3CTXTC Boolean Override Config3.CTXTC config3DSPP Boolean Override Config3.DSP2P config3IPLW Uns32 Override Config3.ISP2W config3ISAOnExc Boolean Override Config3.ISA config3ISAOnExc Boolean Override Config3.ITL config3MCU Boolean Override Config3.MCU config3MAR Uns32 Override Config3.MCU config3MXI Boolean Override Config3.MXI config3SC Boolean Override Config3.RXI config3ULRI Boolean Override Config3.VEIC (enables the use of an external terrupt controller) vectoredinterrupt Boolean Override Config3.VIC (enables vectored interrupts) config4DE Uns32 Override Config3.VIC (enables vectored interrupts) config4BE Uns32 Override Config3.VIX config4BE Uns32 Override Config4.AE config4MMUConfig Uns32 Override Config4.MMUConfig field (interpretation pends on MULExtDef value) config4MTLBSizeExt Uns32 Override Config4.MMUConfig field (interpretation pends on MULExtDef value) config5NSAEn			
config3DSPP Boolean Override Config3DSPP config3DSP2P Boolean Override Config3.DSPP config3ISA Uns32 Override Config3.IFLW config3ISA Uns32 Override Config3.ISA config3ISA Boolean Override Config3.ISA config3ISAOnExc Boolean Override Config3.ISAOnExc config3MCU Boolean Override Config3.MCU config3MMAR Uns32 Override Config3.MCU config3RXI Boolean Override Config3.MAR config3SC Boolean Override Config3.SVI config3ULRI Boolean Override Config3.VEIC (enables the use of an external terrupt controller) vectoredinterrupt Boolean Override Config3.VInt (enables vectored interrupts) config3VZ Boolean Override Config4.VIC (enables the use of an external terrupt confroller) config4ME Boolean Override Config4.AE config4MMUConfig Uns32 Override Config4.AE config4MMUExtDef Uns32 Override Config4.MMUConfig field (interpretation pends on MMUExtDef value) config5MSAEn Boolean <			
config3BP2P Boolean Override Config3.DSP2P config3IPAW Uns32 Override Config3.ISA config3ISA onExc Boolean Override Config3.ISA OnExc config3ITL Boolean Override Config3.ISAOnExc config3MCU Boolean Override Config3.ITL config3MMAR Uns32 Override Config3.MMAR config3RXI Boolean Override Config3.MMAR config3ULRI Boolean Override Config3.ULRI externalinterrupt Boolean Override Config3.VEIC (enables the use of an external terrupt controller) vectoredinterrupt Boolean Override Config3.VEIC (enables the use of an external terrupt controller) vectoredinterrupt Boolean Override Config3.VInt (enables vectored interrupts) config3VZ Boolean Override Config3.VZ config4E Uns32 Override Config4.MMUConfig (interpretation pends on MMUExtDef value) config4MMUConfig Uns32 Override Config4.MMUExtDef config4MMUExtDef Uns32 Override Config5.WA config5EVA Boolean Override Config5.NFExists config5MSAEn			
Config3IPLW	0		
config3ISA Uns32 Override Config3.ISA config3ISAOnExc Boolean Override Config3.ISAOnExc config3ITL Boolean Override Config3.ITL config3MCU Boolean Override Config3.MCU config3MMAR Uns32 Override Config3.MMAR config3RXI Boolean Override Config3.XXI config3ULRI Boolean Override Config3.VEIC (enables the use of an external terrupt controller) vectoredinterrupt Boolean Override Config3.VEIC (enables the use of an external terrupt controller) vectoredinterrupt Boolean Override Config3.VIII (enables vectored interrupts) config3VZ Boolean Override Config3.VI config4HE Uns32 Override Config4.AE config4MMUConfig Uns32 Override Config4.MMUConfig field (interpretation pends on MMUExtDef value) config4MMUExtDef Uns32 Override Config4.WTLBSizeExt config5EVA Boolean Override Config5.NFExists config5MSAEn Boolean Override Config5.NFExists config5MSAEn Boolean Override Config7.MSAEn config7AR			
config3ISAOnExc Boolean Override Config3.ISAOnExc config3TL Boolean Override Config3.ITL config3MCU Boolean Override Config3.MCU config3MMAR Uns32 Override Config3.MMAR config3RXI Boolean Override Config3.RXI config3SC Boolean Override Config3.VEIC (enables the use of an external terrupt controller) externalinterrupt Boolean Override Config3.VIII (enables vectored interrupts) vectoredinterrupt Boolean Override Config3.VIII (enables vectored interrupts) vectoredinterrupt Boolean Override Config3.VIII (enables vectored interrupts) venfig3VZ Boolean Override Config3.VIII (enables vectored interrupts) config4AE Boolean Override Config4.AE config4IE Uns32 Override Config4.AE config4MMUExtDef Uns32 Override Config4.MMUConfig field (interpretation pends on MMUExtDef value) config4WTLBSizeExt Uns32 Override Config5.WEA config5EVA Boolean Override Config5.EVA config5NSAEn Boolean Override Config5.NExists			
config3ITL Boolean Override Config3.ITL config3MCU Boolean Override Config3.MCU config3MMAR Uns32 Override Config3.MMAR config3SC Boolean Override Config3.SC config3ULRI Boolean Override Config3.VEIC (enables the use of an external terrupt controller) vectoredinterrupt Boolean Override Config3.VIII (enables vectored interrupts) config3VZ Boolean Override Config3.VI config4AE Boolean Override Config4.NV config4IE Uns32 Override Config4.AE config4MMUConfig Uns32 Override Config4.MMUConfig field (interpretation pends on MMUExtDef value) config4WTLBSizeExt Uns32 Override Config4.VTLBSizeExt config5EVA Boolean Override Config5.EVA config5MSAEn Boolean Override Config5.NFExists config6FTLBEn Boolean Override power on value of Config6.FTLBEn config6FTLBEn Boolean Override Config7.AR (Alias removed Data cache) config7AR Boolean Override Config7.DCIDX.MODE config7HCI Boolean			
config3MCU Boolean Override Config3.MCU config3MMAR Uns32 Override Config3.MMAR config3RXI Boolean Override Config3.RXI config3ULRI Boolean Override Config3.VERI externalinterrupt Boolean Override Config3.VEIC (enables the use of an external terrupt controller) vectoredinterrupt Boolean Override Config3.VInt (enables vectored interrupts) config3VZ Boolean Override Config3.VZ config4AE Boolean Override Config4.AE config4MUConfig Uns32 Override Config4.MMUConfig field (interpretation pends on MMUExtDef value) config4MMUExtDef Uns32 Override Config4.MMUExtDef config5VA Boolean Override Config5.EVA config5EVA Boolean Override Config5.EVA config5NFExists Boolean Override Config5.NFExists config6FTLBEn Boolean Override Config7.MA config6FTLBEn Boolean Override Config7.AR (Alias removed Data cache) config7AR Boolean Override Config7.HCI (Hardware Cache Initialization) config7IAR B			
config3MMAR Uns32 Override Config3.MMAR config3RXI Boolean Override Config3.RXI config3ULRI Boolean Override Config3.SC config3ULRI Boolean Override Config3.VLRI externalinterrupt Boolean Override Config3.VEIC (enables the use of an external terrupt controller) vectoredinterrupt Boolean Override Config3.VInt (enables vectored interrupts) config3VZ Boolean Override Config3.VI config4AE Boolean Override Config4.M config4IE Uns32 Override Config4.MM UConfig field (interpretation pends on MMUExtDef value) config4MMUExtDef Uns32 Override Config4.MMUExtDef config4VTLBSizeExt Uns32 Override Config4.MTLBSizeExt config5EVA Boolean Override Config5.EVA config5NFExists Boolean Override Config5.NFExists config6FTLBEn Boolean Override Config5.MSAEn config6FTLBEn Boolean Override Config7.MR (Alias removed Data cache) config7AR Boolean Override Config7.DCIDX.MODE config7WII Boolean			
config3RXI Boolean Override Config3.RXI config3SC Boolean Override Config3.SC config3ULRI Boolean Override Config3.VEIC (enables the use of an external terrupt controller) vectoredinterrupt Boolean Override Config3.VEIC (enables the use of an external terrupt controller) vectoredinterrupt Boolean Override Config3.VII (enables vectored interrupts) config3VZ Boolean Override Config3.VIX config4AE Boolean Override Config4.ME config4MMUConfig Uns32 Override Config4.ME config4MMUExtDef Uns32 Override Config4.MMUConfig field (interpretation pends on MMUExtDef value) config4VTLBSizeExt Uns32 Override Config4.WTLBSizeExt config5VA Boolean Override Config5.VA config5NFExists Boolean Override Config5.NFExists config5NFExists Boolean Override Config5.NFExists config6FTLBEn Boolean Override Config5.NFExists config6FTLBEn Boolean Override Config5.NFAA (Alias removed Data cache) config7AR Boolean Override Config7.AR (Alias removed Instruct			
config3ULRI Boolean Override Config3.ULRI externalinterrupt Boolean Override Config3.ULRI externalinterrupt Boolean Override Config3.VEIC (enables the use of an external terrupt controller) vectoredinterrupt Boolean Override Config3.VInt (enables vectored interrupts) config3VZ Boolean Override Config3.VZ config4AE Boolean Override Config4.AE config4IE Uns32 Override Config4.IE config4MMUConfig Uns32 Override Config4.MMUConfig field (interpretation pends on MMUExtDef value) config4VTLBSizeExt Uns32 Override Config4.VTLBSizeExt config5EVA Boolean Override Config5.EVA config5NFExists Boolean Override Config5.NFExists config5MSAEn Boolean Override Config5.MSAEn config6FTLBEn Boolean Override Config7.AR (Alias removed Data cache) config7AR Boolean Override Config7.HCI (Hardware Cache Initialization) config7IAR Boolean Override Config7.HCI (Hardware Cache Initialization) ficsrABS2008 Boolean Override FCSR.ABS2008 (QNaN/SNaN encodings material properties of the power on type implemented firHas2008 Override FIR.Has2008 (one or more IEEE 754-2008) Override FIR.Has2008 (one or more IEEE 754-2008)			
config3ULRI Boolean Override Config3.ULRI externalinterrupt Boolean Override Config3.VEIC (enables the use of an external terrupt controller) vectoredinterrupt Boolean Override Config3.VInt (enables vectored interrupts) config3VZ Boolean Override Config3.VZ config4AE Boolean Override Config4.AE config4IE Uns32 Override Config4.IE config4MMUConfig Uns32 Override Config4.MMUConfig field (interpretation pends on MMUExtDef value) config4MMUExtDef Uns32 Override Config4.MMUExtDef config5EVA Boolean Override Config4.VTLBSizeExt config5EVA Boolean Override Config5.NFExists config5NFExists Boolean Override Config5.NFExists config6FTLBEn Boolean Override Config5.MSAEn config6FTLBEn Boolean Override Config7.AR (Alias removed Data cache) config7DCIDX_MODE Uns32 Override Config7.DCIDX_MODE config7HCI Boolean Override Config7.AR (Alias removed Data cache) config7IAR Boolean Override Config7.HCI (Hardware Cache Initialization) config7IAR Boolean Override Config7.HCI (Hardware Cache Initialization) config7WII Boolean Override FCSR.ABS2008 (ABS/NEG compliant w IEEE 754-2008) fcsrNAN2008 Boolean Override FCSR.ABS2008 (QNaN/SNaN encodings ma IEEE 754-2008) fcsrNAN2008 Boolean Override FIR.PS (PS floating point type implemented firHas2008 Override FIR.PS (PS floating point type implemented firHas2008 Override FIR.PS (PS floating point type implemented firHas2008 Override FIR.Has2008 (one or more IEEE 754-2008)			
externalinterrupt Boolean Override Config3.VEIC (enables the use of an external terrupt controller) vectoredinterrupt Boolean Override Config3.VInt (enables vectored interrupts) Boolean Override Config3.VI config4AE Boolean Override Config4.AE config4MMUConfig Uns32 Override Config4.MMUConfig field (interpretation pends on MMUExtDef value) config4MMUExtDef config4VTLBSizeExt Uns32 Override Config4.MMUExtDef config5EVA Boolean Override Config5.EVA config5NFExists Boolean Override Config5.NFExists config5MSAEn config6FTLBEn Boolean Override Config5.MSAEn config7DCIDX.MODE Uns32 Override Config7.AR (Alias removed Data cache) config7HCI Boolean Override Config7.HCI (Hardware Cache Initialization) config7IAR Boolean Override Config7.HCI (Hardware Cache Initialization) ficsrABS2008 Boolean Override FCSR.ABS2008 (ABS/NEG compliant w IEEE 754-2008) Boolean Override FIR.PS (PS floating point type implemented firHas2008 Override FIR.PS (PS floating point type implemented firHas2008)			
vectoredinterrupt boolean vectoredinterrupt boolean verride Config3.VInt (enables vectored interrupts) config3VZ boolean verride Config3.VZ config4AE boolean verride Config4.AE config4IE verride Config4.AE config4MMUConfig verride Config4.MMUConfig field (interpretation pends on MMUExtDef value) config4MMUExtDef verride Config4.WMUExtDef config4VTLBSizeExt verride Config4.VTLBSizeExt verride Config4.VTLBSizeExt verride Config4.VTLBSizeExt config5EVA boolean verride Config5.EVA config5NFExists config5MSAEn config5MSAEn config6FTLBEn boolean verride Config5.NFExists config7AR boolean verride Config7.AR (Alias removed Data cache) config7DCIDX.MODE verride Config7.HCI (Hardware Cache Initialization) config7IAR boolean verride Config7.HCI (Hardware Cache Initialization) config7IAR boolean verride Config7.WII (wait IE/IXMT ignore) fesrABS2008 boolean verride FCSR.ABS2008 (ABS/NEG compliant wait IEEE 754-2008) fesrNAN2008 boolean verride FCSR.NAN2008 (QNaN/SNaN encodings mait IEEE 754-2008 (QNaN/SNaN encodings mait IEEE 754-2008 (pond) for more IEEE 754-2008 (p			
vectoredinterrupt Boolean Override Config3.VInt (enables vectored interrupts) config3VZ Boolean Override Config3.VZ config4AE Boolean Override Config4.AE config4IE Uns32 Override Config4.MMUConfig field (interpretation pends on MMUExtDef value) config4MMUExtDef Uns32 Override Config4.MMUExtDef config4VTLBSizeExt Uns32 Override Config4.VTLBSizeExt config5EVA Boolean Override Config5.EVA config5MFExists Boolean Override Config5.MFExists config6MSAEn Boolean Override Config5.MSAEn config7AR Boolean Override power on value of Config6.FTLBEn config7DCIDX_MODE Uns32 Override Config7.AR (Alias removed Data cache) config7HCI Boolean Override Config7.DCIDX_MODE config7IAR Boolean Override Config7.HCI (Hardware Cache Initialization) config7WII Boolean Override FCSR.ABS2008 (ABS/NEG compliant was proved in the provention of the config7.WII (wait IE/IXMT ignore) fcsrNAN2008 Boolean Override FCSR.NAN2008 (QNaN/SNaN encodings manal EEE 754-2008) fcryAans B	externalinterrupt	Boolean	
config3VZ config4AE config4AE config4IE config4MMUConfig Uns32 Coverride Config4.ME config4MMUExtDef config4MMUExtDef config4VTLBSizeExt config5EVA config5NFExists config5MSAEn config6FTLBEn config6FTLBEn config7AR config7DCIDX_MODE config7HCI config7HCI config7HCI config7MI boolean config7MI boolean config7MI boolean config7MI boolean config7NEX config7NEX boolean config7NEX config4MMUConfig field (interpretation pends) config4MMUConfig field (interpretation pends (inte	vectoredinterrupt	Boolean	
config4AE Boolean Override Config4.AE config4IE Uns32 Override Config4.IE config4MMUConfig Uns32 Override Config4.MMUConfig field (interpretation pends on MMUExtDef value) config4MMUExtDef Uns32 Override Config4.WTLBSizeExt config5VTLBSizeExt Uns32 Override Config4.VTLBSizeExt config5NFExists Boolean Override Config5.EVA config5NFExists Boolean Override Config5.NFExists config6FTLBEn Boolean Override Config5.MSAEn config6FTLBEn Boolean Override Config7.AR (Alias removed Data cache) config7AR Boolean Override Config7.DCIDX.MODE config7HCI Boolean Override Config7.HCI (Hardware Cache Initialization) config7IAR Boolean Override Config7.HA (Alias removed Instruction cache Config7.WII (wait IE/IXMT ignore) fcsrABS2008 Boolean Override FCSR.ABS2008 (ABS/NEG compliant was IEEE 754-2008 fcsrNAN2008 Boolean Override FCSR.NAN2008 (QNaN/SNaN encodings mate IEEE 754-2008 recommendation) firPS Boolean Override FIR.PS (PS floating point type implemented Override FIR.PS (DS floating point type implemented Ove		Boolean	
config4IE config4MMUConfig Uns32 Override Config4.MMUConfig field (interpretation pends on MMUExtDef value) config4MMUExtDef Uns32 Override Config4.MMUExtDef config4VTLBSizeExt Uns32 Override Config4.WTLBSizeExt config5EVA Config5EVA Config5NFExists Boolean Override Config5.NFExists config5MSAEn Config6FTLBEn Config6FTLBEn Boolean Override Config5.MSAEn Config7AR Boolean Override Config7.AR (Alias removed Data cache) config7DCIDX_MODE Uns32 Override Config7.HCI (Hardware Cache Initialization) config7IAR Boolean Override Config7.IAR (Alias removed Instruction cache config7WII Boolean Override Config7.WII (wait IE/IXMT ignore) fcsrABS2008 Boolean Override FCSR.ABS2008 (ABS/NEG compliant was IEEE 754-2008) Boolean Override FCSR.NAN2008 (QNaN/SNaN encodings mas IEEE 754-2008) Boolean Override FIR.PS (PS floating point type implemented firHas2008) Override FIR.Has2008 (one or more IEEE 754-2008)			
config4MMUConfig Uns32 Override Config4.MMUConfig field (interpretation pends on MMUExtDef value) config4MMUExtDef config4VTLBSizeExt Uns32 Override Config4.MMUExtDef config5EVA Boolean Override Config5.EVA config5NFExists Boolean Override Config5.NFExists config5MSAEn config6FTLBEn Boolean Override Config5.MSAEn config6FTLBEn Boolean Override Config7.MR (Alias removed Data cache) config7DCIDX_MODE Uns32 Override Config7.DCIDX_MODE config7HCI Boolean Override Config7.HCI (Hardware Cache Initialization) config7WII Boolean Override Config7.WII (wait IE/IXMT ignore) fcsrABS2008 Boolean Override FCSR.ABS2008 (ABS/NEG compliant was IEEE 754-2008) fcsrNAN2008 Boolean Override FIR.PS (PS floating point type implemented firHas2008) Override FIR.Has2008 (one or more IEEE 754-2008)			
pends on MMUExtDef value) config4MMUExtDef Uns32 Override Config4.MMUExtDef config4VTLBSizeExt Uns32 Override Config4.VTLBSizeExt config5EVA Boolean Override Config5.EVA config5NFExists Boolean Override Config5.NFExists config5MSAEn Boolean Override Config5.MSAEn config6FTLBEn Boolean Override power on value of Config6.FTLBEn config7AR Boolean Override Config7.AR (Alias removed Data cache) config7DCIDX_MODE Uns32 Override Config7.DCIDX_MODE config7HCI Boolean Override Config7.HCI (Hardware Cache Initialization) config7IAR Boolean Override Config7.IAR (Alias removed Instruction cache) config7WII Boolean Override Config7.WII (wait IE/IXMT ignore) fcsrABS2008 Boolean Override FCSR.ABS2008 (ABS/NEG compliant was IEEE 754-2008) fcsrNAN2008 Boolean Override FCSR.NAN2008 (QNaN/SNaN encodings mas IEEE 754-2008 recommendation) firPS Boolean Override FIR.PS (PS floating point type implemented firHas2008)			
config4VTLBSizeExtUns32Override Config4.VTLBSizeExtconfig5EVABooleanOverride Config5.EVAconfig5NFExistsBooleanOverride Config5.NFExistsconfig5MSAEnBooleanOverride Config5.MSAEnconfig6FTLBEnBooleanOverride power on value of Config6.FTLBEnconfig7ARBooleanOverride Config7.AR (Alias removed Data cache)config7DCIDX_MODEUns32Override Config7.DCIDX_MODEconfig7HCIBooleanOverride Config7.HCI (Hardware Cache Initialization)config7IARBooleanOverride Config7.IAR (Alias removed Instruction cachconfig7WIIBooleanOverride Config7.WII (wait IE/IXMT ignore)fcsrABS2008BooleanOverride FCSR.ABS2008 (ABS/NEG compliant w IEEE 754-2008)fcsrNAN2008BooleanOverride FCSR.NAN2008 (QNaN/SNaN encodings ma IEEE 754-2008 recommendation)firPSBooleanOverride FIR.PS (PS floating point type implemented FIR.Has2008 (one or more IEEE 754-2008)			pends on MMUExtDef value)
config5EVABooleanOverride Config5.EVAconfig5NFExistsBooleanOverride Config5.NFExistsconfig5MSAEnBooleanOverride Config5.MSAEnconfig6FTLBEnBooleanOverride power on value of Config6.FTLBEnconfig7ARBooleanOverride Config7.AR (Alias removed Data cache)config7DCIDX_MODEUns32Override Config7.DCIDX_MODEconfig7HCIBooleanOverride Config7.HCI (Hardware Cache Initialization)config7IARBooleanOverride Config7.IAR (Alias removed Instruction cachconfig7WIIBooleanOverride FCSR.ABS2008 (ABS/NEG compliant w IEEE 754-2008)fcsrNAN2008BooleanOverride FCSR.NAN2008 (QNaN/SNaN encodings ma IEEE 754-2008 recommendation)firPSBooleanOverride FIR.PS (PS floating point type implemented FIR.Has2008 (one or more IEEE 754-2008)		Uns32	
config5NFExistsBooleanOverride Config5.NFExistsconfig5MSAEnBooleanOverride Config5.MSAEnconfig6FTLBEnBooleanOverride power on value of Config6.FTLBEnconfig7ARBooleanOverride Config7.AR (Alias removed Data cache)config7DCIDX_MODEUns32Override Config7.DCIDX_MODEconfig7HCIBooleanOverride Config7.HCI (Hardware Cache Initialization)config7IARBooleanOverride Config7.IAR (Alias removed Instruction cacheconfig7WIIBooleanOverride Config7.WII (wait IE/IXMT ignore)fcsrABS2008BooleanOverride FCSR.ABS2008 (ABS/NEG compliant wait IEEE 754-2008)fcsrNAN2008BooleanOverride FCSR.NAN2008 (QNaN/SNaN encodings mate IEEE 754-2008 recommendation)firPSBooleanOverride FIR.PS (PS floating point type implemented FirHas2008)forHas2008BooleanOverride FIR.Has2008 (one or more IEEE 754-2008)	config4VTLBSizeExt	Uns32	
config5MSAEnBooleanOverride Config5.MSAEnconfig6FTLBEnBooleanOverride power on value of Config6.FTLBEnconfig7ARBooleanOverride Config7.AR (Alias removed Data cache)config7DCIDX_MODEUns32Override Config7.DCIDX_MODEconfig7HCIBooleanOverride Config7.HCI (Hardware Cache Initialization)config7IARBooleanOverride Config7.IAR (Alias removed Instruction cacheconfig7WIIBooleanOverride Config7.WII (wait IE/IXMT ignore)fcsrABS2008BooleanOverride FCSR.ABS2008 (ABS/NEG compliant wait IEEE 754-2008)fcsrNAN2008BooleanOverride FCSR.NAN2008 (QNaN/SNaN encodings mait IEEE 754-2008 recommendation)firPSBooleanOverride FIR.PS (PS floating point type implemented BooleanfirHas2008BooleanOverride FIR.Has2008 (one or more IEEE 754-2008)	config5EVA	Boolean	Override Config5.EVA
config6FTLBEnBooleanOverride power on value of Config6.FTLBEnconfig7ARBooleanOverride Config7.AR (Alias removed Data cache)config7DCIDX_MODEUns32Override Config7.DCIDX_MODEconfig7HCIBooleanOverride Config7.HCI (Hardware Cache Initialization)config7IARBooleanOverride Config7.IAR (Alias removed Instruction cacheconfig7WIIBooleanOverride Config7.WII (wait IE/IXMT ignore)fcsrABS2008BooleanOverride FCSR.ABS2008 (ABS/NEG compliant was IEEE 754-2008)fcsrNAN2008BooleanOverride FCSR.NAN2008 (QNaN/SNaN encodings mas IEEE 754-2008 recommendation)firPSBooleanOverride FIR.PS (PS floating point type implemented Boolean)firHas2008BooleanOverride FIR.Has2008 (one or more IEEE 754-2008 recommendation)	config5NFExists	Boolean	
config7ARBooleanOverride Config7.AR (Alias removed Data cache)config7DCIDX_MODEUns32Override Config7.DCIDX_MODEconfig7HCIBooleanOverride Config7.HCI (Hardware Cache Initialization)config7IARBooleanOverride Config7.IAR (Alias removed Instruction cacheconfig7WIIBooleanOverride Config7.WII (wait IE/IXMT ignore)fcsrABS2008BooleanOverride FCSR.ABS2008 (ABS/NEG compliant wait IEEE 754-2008)fcsrNAN2008BooleanOverride FCSR.NAN2008 (QNaN/SNaN encodings mait IEEE 754-2008 recommendation)firPSBooleanOverride FIR.PS (PS floating point type implemented BooleanfirHas2008BooleanOverride FIR.Has2008 (one or more IEEE 754-2008 recommendation)			
config7DCIDX_MODEUns32Override Config7.DCIDX_MODEconfig7HCIBooleanOverride Config7.HCI (Hardware Cache Initialization)config7IARBooleanOverride Config7.IAR (Alias removed Instruction cachconfig7WIIBooleanOverride Config7.WII (wait IE/IXMT ignore)fcsrABS2008BooleanOverride FCSR.ABS2008 (ABS/NEG compliant waite FCSR.NAN2008)fcsrNAN2008BooleanOverride FCSR.NAN2008 (QNaN/SNaN encodings maite FCSR.NAN2008)firPSBooleanOverride FIR.PS (PS floating point type implemented firHas2008)forHas2008BooleanOverride FIR.Has2008 (one or more IEEE 754-2008)		Boolean	
config7HCIBooleanOverride Config7.HCI (Hardware Cache Initialization)config7IARBooleanOverride Config7.IAR (Alias removed Instruction cachconfig7WIIBooleanOverride Config7.WII (wait IE/IXMT ignore)fcsrABS2008BooleanOverride FCSR.ABS2008 (ABS/NEG compliant was IEEE 754-2008)fcsrNAN2008BooleanOverride FCSR.NAN2008 (QNaN/SNaN encodings mass IEEE 754-2008 recommendation)firPSBooleanOverride FIR.PS (PS floating point type implemented Boolean)firHas2008BooleanOverride FIR.Has2008 (one or more IEEE 754-2008 recommendation)	config7AR	Boolean	
config7HCIBooleanOverride Config7.HCI (Hardware Cache Initialization)config7IARBooleanOverride Config7.IAR (Alias removed Instruction cachconfig7WIIBooleanOverride Config7.WII (wait IE/IXMT ignore)fcsrABS2008BooleanOverride FCSR.ABS2008 (ABS/NEG compliant was IEEE 754-2008)fcsrNAN2008BooleanOverride FCSR.NAN2008 (QNaN/SNaN encodings mass IEEE 754-2008 recommendation)firPSBooleanOverride FIR.PS (PS floating point type implemented Boolean)firHas2008BooleanOverride FIR.Has2008 (one or more IEEE 754-2008 recommendation)	config7DCIDX_MODE	Uns32	Override Config7.DCIDX_MODE
config7WII Boolean Override Config7.WII (wait IE/IXMT ignore) fcsrABS2008 Boolean Override FCSR.ABS2008 (ABS/NEG compliant was IEEE 754-2008) fcsrNAN2008 Boolean Override FCSR.NAN2008 (QNaN/SNaN encodings mas IEEE 754-2008 recommendation) firPS Boolean Override FIR.PS (PS floating point type implemented firHas2008) Boolean Override FIR.Has2008 (one or more IEEE 754-2008)	config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initialization)
fcsrABS2008 Boolean Override FCSR.ABS2008 (ABS/NEG compliant w IEEE 754-2008) fcsrNAN2008 Boolean Override FCSR.NAN2008 (QNaN/SNaN encodings ma IEEE 754-2008 recommendation) firPS Boolean Override FIR.PS (PS floating point type implemented firHas2008 Boolean Override FIR.Has2008 (one or more IEEE 754-2008 seconds)	config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction cache)
fcsrABS2008 Boolean Override FCSR.ABS2008 (ABS/NEG compliant w IEEE 754-2008) fcsrNAN2008 Boolean Override FCSR.NAN2008 (QNaN/SNaN encodings ma IEEE 754-2008 recommendation) firPS Boolean Override FIR.PS (PS floating point type implemented firHas2008 Boolean Override FIR.Has2008 (one or more IEEE 754-2008 seconds)		Boolean	
fcsrNAN2008 Boolean Override FCSR.NAN2008 (QNaN/SNaN encodings made in items in it	fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant with IEEE 754-2008)
firPS Boolean Override FIR.PS (PS floating point type implemented firHas2008 Boolean Override FIR.Has2008 (one or more IEEE 754-2008)	fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/SNaN encodings match
firHas2008 Boolean Override FIR.Has2008 (one or more IEEE 754-2008 :	firPS	Roologn	
t three diesent	111111111111111111111111111111111111111	Doolean	tures present)
intctlIPFDC Uns32 Override IntCtl.IPFDC	intctllPFDC	Uns32	

intctlIPTI	Uns32	Override IntCtl.IPTI
pridRevision	Uns32	Override PRId.Revision
srsctlHSS	Uns32	Override SRSCtl.HSS (number of shadow register sets)
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use
		GCR_Cx_RESET_BASE on CMP processors)
UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the correspond-
		ing BEV address bits
firstBEVExceptionBaseMaskBit	Uns32	Specify LSB position of GCR_Cx_RESET_EXT_BASE.
		BEVExceptionBaseMask field. Only used when SegCtl
		present
EVAReset	Boolean	Set to one to reset into non-legacy address map and BEV
		location. Only used when non-CMP and SegCtl present
ExceptionBaseMask	Uns32	Specify the ExceptionBaseMask value used for bits
		[27:firstBEVExceptionBaseMaskBit]. Only used when
		non-CMP and SegCtl present
ExceptionBasePA	Uns32	Bits [35:29] of the physical address for the BEV overlays.
		Only used when non-CMP and SegCtl present
GIC_EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable within
		cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable within clus-
aan naanna	77 00	ter
GCR_PCORES	Uns32	CMP system only: override GCR_CONFIG.PCORES
CCD DACE	11 00	(number of cores-1)
GCR_BASE	Uns32	CMP system only: override GCR_BASE.GCR_BASE (de-
GCR_MINOR_REV	Uns32	fault GCR register address) CMP system only: override GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	CMP system only: override GCR_REV.MINOR_REV CMP system only: override GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override GCK_REV.MAJOK_REV CMP system only: override
GCR_CACHE_MINOR_REV	Ulisaz	GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override
GCIL-CACIIE-MAJOIL-ILEV	Ulisaz	GCR_CACHE_REV.MAJOR_REV
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override
doit 1000 11 min voit 11 th	0.11592	GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override
001020001211110010202	011502	GCR_IOCU1_REV.MAJOR_REV
GIC_NUMINTERRUPTS	Uns32	CMP system only: override
		GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override
		GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override
		GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override
		GIC_SH_REVISION.MAJOR_REV
GIC_PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPES
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY
CPC_RESETLEN	Uns32	CMP system only: override
		CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override
		CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override
		CPC_REVISION.MAJOR_REV
GCR_C0_RESET_BASE	Uns32	CPC_REVISION.MAJOR_REV CMP system only: GCR_CL_RESET_BASE for core 0 CMP system only: GCR_CL_RESET_BASE for core 1

GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 3
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core
		0. Only used when SegCtl present
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core
		1. Only used when SegCtl present
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core
		2. Only used when SegCtl present
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core
		3. Only used when SegCtl present
EIC_OPTION	Uns32	Override the external interrupt controller EIC_OPTION
ISPRAM_SIZE	Uns32	Encoded size of the ISPRAM region (log2(<ispram size<="" td=""></ispram>
		in bytes>) - 11)
ISPRAM_BASE	Uns64	Starting physical address of the ISPRAM region
ISPRAM_ENABLE	Boolean	Set the enable bit of the ISPRAM region's tag (used to
		enable the ISPRAM region prior to reset)
ISPRAM_FILE	String	Load a MIPS hex file into the ISPRAM region prior to
		reset
DSPRAM_SIZE	Uns32	Encoded size of the DSPRAM region (log2(<dspram td="" <=""></dspram>
		size in bytes>) - 11)
DSPRAM_BASE	Uns64	Starting physical address of the DSPRAM region
DSPRAM_ENABLE	Boolean	Set the enable bit of the DSPRAM region's tag (used to
		enable the DSPRAM region prior to reset)

Table 8.3: Parameters that can be set in: VPE

Name	Type	Description
endian	Endian	Model endian
cacheenable	Enumeration	Select cache model mode (default, tag or full)
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info structure
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for
		AVP test termination)
cacheIndexBypassTLB	Boolean	When set, cache index ops do not generate TLB exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
supervisorMode	Boolean	Override whether processor implements supervisor mode
busErrors	Boolean	Override bus error exception behavior. When true, ac-
		cesses of memory not defined by platform will cause bus
		error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when
		true (sets Config.MT=3, Config.KU/K23=2 and Con-
		fig1.MMUSizeM1=0)
removeDSP	Boolean	Override the DSP-present configuration when true (sets
		Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true (sets
		Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true (sets
		Config1.FP to 0)
isISA	Boolean	Enable to specify ISA model (reset address from ELF, all
		coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to maximum
		value to improve performance
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores only)
ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC imple-
		mentation (MT cores only)

MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior, 2:new mttc1 behavior)
supportDenormals	Boolean	Enable to specify that the FPU supports denormal
supportDenormals	Doolean	operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0
mpuRegions	Uns32	Number of regions for memory protection unit
mpuType	Uns32	Type of MPU implementation
mpuEnable	Boolean	Enable MPU2 segment control at reset
mpuSegment0	Uns32	Attributes for segment 0 in MPU2 SegmentControl_0 reg-
mpusegmento	011502	ister
mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentControl_0 reg-
	0 0	ister
mpuSegment2	Uns32	Attributes for segment 2 in MPU2 SegmentControl_0 reg-
1 0		ister
mpuSegment3	Uns32	Attributes for segment 3 in MPU2 SegmentControl_0 reg-
1 0		ister
mpuSegment4	Uns32	Attributes for segment 4 in MPU2 SegmentControl_1 reg-
1 0		ister
mpuSegment5	Uns32	Attributes for segment 5 in MPU2 SegmentControl_1 reg-
•		ister
mpuSegment6	Uns32	Attributes for segment 6 in MPU2 SegmentControl_1 reg-
•		ister
mpuSegment7	Uns32	Attributes for segment 7 in MPU2 SegmentControl_1 reg-
		ister
mpuSegment8	Uns32	Attributes for segment 8 in MPU2 SegmentControl_2 reg-
		ister
mpuSegment9	Uns32	Attributes for segment 9 in MPU2 SegmentControl_2 reg-
		ister
mpuSegment10	Uns32	Attributes for segment 10 in MPU2 SegmentControl_2 reg-
		ister
mpuSegment11	Uns32	Attributes for segment 11 in MPU2 SegmentControl_2 reg-
		ister
mpuSegment12	Uns32	Attributes for segment 12 in MPU2 SegmentControl_3 reg-
		ister
mpuSegment13	Uns32	Attributes for segment 13 in MPU2 SegmentControl_3 reg-
		ister
mpuSegment14	Uns32	Attributes for segment 14 in MPU2 SegmentControl_3 reg-
		ister
mpuSegment15	Uns32	Attributes for segment 15 in MPU2 SegmentControl_3 reg-
		ister
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
hasFDC	Uns32	Specify the size of Fast Debug Channel register block
statusFR	Boolean	Override power on value in Status.FR (Floating point reg-
		ister mode)
configDSP	Boolean	Override Config.DSP (data scratchpad RAM present)
configISP	Boolean	Override Config.ISP (instruction scratchpad RAM
		present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0 cacheabil-
		ity)
configKU	Uns32	Override power on value of Config.KU (set Useg cacheabil-
		ity)
configK23	Uns32	Override power on value of Config.K23 (set Kseg23
		cacheability)

configMDU	Boolean	Override Config.MDU (iterative multiply/divide unit)
configMM	Boolean	Override Config.MM (merging mode for write)
configMT	Uns32	Override Config.MT
configSB	Boolean	Override Config.SB (simple bus transfers only)
MIPS16eASE	Boolean	Override Config1.CA (enables the MIPS16e ASE)
config1DA	Uns32	Override Config1.DA (Deache associativity)
config1DL	Uns32	Override Config1.DL (Deache line size)
config1DS	Uns32	Override Config1.DS (Deache sets per way)
config1EP	Boolean	Override Config1.EP (EJTag present)
config1IA	Uns32	Override Config1.IA (Icache associativity)
config1IL	Uns32	Override Config1.IL (Icache line size)
config1IS	Uns32	Override Config1.IS (Icache sets per way)
config1MMUSizeM1	Uns32	Override Config1.MMUSizeM1 (number of MMU entries-
Comignitivi	011392	1)
config1WR	Boolean	Override Config1.WR (watchpoint registers present)
config1FP	Boolean	Override Config1.FP (FPU present)
config3BI	Boolean	Override Config3.BI
config3BP	Boolean	Override Configs.BP
config3CDMM	Boolean	Override Configs.CDMM
config3CTXTC	Boolean	Override Config3.CTXTC
config3DSPP	Boolean	Override Config3.DSPP
config3DSP2P	Boolean	Override Config3.DSP2P
config3IPLW	Uns32	Override Config3.IPLW Override Config3.IPLW
config3ISA	Uns32	Override Config3.ISA
config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3ITL	Boolean	Override Config3.ITL
config3MCU	Boolean	Override Config3.MCU
config3MMAR	Uns32	Override Config3.MMAR
config3RXI	Boolean	Override Config3.RXI
config3SC	Boolean	Override Config3.SC
config3ULRI	Boolean	Override Config3.ULRI
externalinterrupt	Boolean	Override Config3.VEIC (enables the use of an external in-
externamiterrupt	Doolean	terrupt controller)
vectoredinterrupt	Boolean	Override Config3.VInt (enables vectored interrupts)
config3VZ	Boolean	Override Config3.VZ Override Config3.VZ
config4AE	Boolean	Override Config. VZ Override Config. AE
config4AE config4IE	Uns32	Override Config4.AE Override Config4.IE
config4MMUConfig	Uns32	Override Config4.MMUConfig field (interpretation de-
Conngamino Conng	Ulisaz	pends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.WMOExtDei Override Config4.VTLBSizeExt
config5EVA	Boolean	Override Config5.EVA
config5NFExists	Boolean	Override Config5.NFExists
config5MSAEn	Boolean	Override Config5.MSAEn
config6FTLBEn	Boolean	Override Conngo.MSAEn Override power on value of Config6.FTLBEn
config7AR		
config7DCIDX_MODE	Boolean Uns32	Override Config7.AR (Alias removed Data cache) Override Config7.DCIDX_MODE
config7HCI		Override Config. HCI (Hardware Cache Initialization)
	Boolean	
config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)
fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant with
C NIANIOGO	D 1	IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/SNaN encodings match
c pg	D '	IEEE 754-2008 recommendation)
firPS	Boolean	Override FIR.PS (PS floating point type implemented)

firHas2008	Boolean	Override FIR.Has2008 (one or more IEEE 754-2008 features present)
intctlIPFDC	Uns32	Override IntCtl.IPFDC
intetlIPTI	Uns32	Override IntCtl.IFTI
	Uns32	Override PRId.Revision
pridRevision srsctlHSS	Uns32	
		Override SRSCtl.HSS (number of shadow register sets)
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use GCR_Cx_RESET_BASE on CMP processors)
UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the corresponding BEV address bits
first BEVException Base Mask Bit	Uns32	Specify LSB position of GCR_Cx_RESET_EXT_BASE. BEVExceptionBaseMask field. Only used when SegCtl present
EVAReset	Boolean	Set to one to reset into non-legacy address map and BEV location. Only used when non-CMP and SegCtl present
ExceptionBaseMask	Uns32	Specify the ExceptionBaseMask value used for bits [27:firstBEVExceptionBaseMaskBit]. Only used when non-CMP and SegCtl present
ExceptionBasePA	Uns32	Bits [35:29] of the physical address for the BEV overlays. Only used when non-CMP and SegCtl present
GIC_EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable within cluster
GCR_PCORES	Uns32	CMP system only: override GCR_CONFIG.PCORES (number of cores-1)
GCR_BASE	Uns32	CMP system only: override GCR_BASE.GCR_BASE (default GCR register address)
GCR_MINOR_REV	Uns32	CMP system only: override GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	CMP system only: override GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MAJOR_REV
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MAJOR_REV
GIC_NUMINTERRUPTS	Uns32	CMP system only: override GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MAJOR_REV
GIC_PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPES
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY
CPC_RESETLEN	Uns32	CMP system only: override CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override CPC_REVISION.MINOR_REV

CPC_MAJOR_REV	Uns32	CMP system only: override
		CPC_REVISION.MAJOR_REV
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 3
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core
		0. Only used when SegCtl present
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core
		1. Only used when SegCtl present
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core
		2. Only used when SegCtl present
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core
		3. Only used when SegCtl present
EIC_OPTION	Uns32	Override the external interrupt controller EIC_OPTION
ISPRAM_SIZE	Uns32	Encoded size of the ISPRAM region (log2(<ispram size<="" td=""></ispram>
		in bytes>) - 11)
ISPRAM_BASE	Uns64	Starting physical address of the ISPRAM region
ISPRAM_ENABLE	Boolean	Set the enable bit of the ISPRAM region's tag (used to
		enable the ISPRAM region prior to reset)
ISPRAM_FILE	String	Load a MIPS hex file into the ISPRAM region prior to
		reset
DSPRAM_SIZE	Uns32	Encoded size of the DSPRAM region (log2(<dspram< td=""></dspram<>
		size in bytes>) - 11)
DSPRAM_BASE	Uns64	Starting physical address of the DSPRAM region
DSPRAM_ENABLE	Boolean	Set the enable bit of the DSPRAM region's tag (used to
		enable the DSPRAM region prior to reset)

Table 8.4: Parameters that can be set in: TC

Execution Modes

Mode	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3

Table 9.1: Modes implemented in: CMP

Mode	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3

Table 9.2: Modes implemented in: CPU

Mode	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3

Table 9.3: Modes implemented in: VPE

Mode	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3

Table 9.4: Modes implemented in: TC

Exceptions

Int Mod TLBL TLBS	0 1 2 3 4
TLBL TLBS	2 3 4
TLBS	3 4
	4
V TIEL	
AdEL	
AdES	5
IBE	6
DBE	7
Sys	8
Вр	9
RI	10
CpU	11
Ov	12
Tr	13
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
Prot	29
CacheErr	30

Table 10.1: Exceptions implemented in: CMP $\,$

Exception	Code

Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Вр	9
RI	10
CpU	11
Ov	12
Tr	13
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
Prot	29
CacheErr	30

Table 10.2: Exceptions implemented in: CPU

Exception	Code
Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Вр	9
RI	10
CpU	11
Ov	12
Tr	13

FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
Prot	29
CacheErr	30

Table 10.3: Exceptions implemented in: \overline{VPE}

Exception	Code
Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Вр	9
RI	10
CpU	11
Ov	12
Tr	13
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
Prot	29
CacheErr	30

Table 10.4: Exceptions implemented in: TC

Hierarchy of the model

A CPU core may be configured to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.

OVP processor models can be written to include SMP blocks and to have many levels of hierarchy. Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

11.1 Level 1: CMP

This level in the model hierarchy has 2 commands. This level in the model hierarchy has no register groups. This level in the model hierarchy has 4 children: CPU0, CPU1, CPU2 and CPU3.

11.2 Level 2: CPU

This level in the model hierarchy has 2 commands. This level in the model hierarchy has no register groups. This level in the model hierarchy has 2 children: CPU0_VPE0 and CPU0_VPE1.

11.3 Level 3: VPE

This level in the model hierarchy has 2 commands. This level in the model hierarchy has 4 register groups:

Group name	Registers
COP0	50
CMP_GCR	27

CMP_CPC	11
CMP_GIC	746

Table 11.1: Register groups

This level in the model hierarchy has one child: CPU0_TC0 $\,$

11.4 Level 4: TC

This level in the model hierarchy has 16 commands. This level in the model hierarchy has 7 register groups:

Group name	Registers
Core	33
DSP	9
COP0	64
CMP_GCR	27
CMP_CPC	11
CMP_GIC	746
$Integration_support$	1

Table 11.2: Register groups

This level in the model hierarchy has no children.

Model Commands

A Processor model can implement one or more **Model Commands** available to be invoked from the simulator command line, from the OP API or from the Imperas Multiprocessor Debugger.

12.1 Level 1: CMP

12.1.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.1: isync command arguments

12.1.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.2: itrace command arguments

12.2 Level 2: CPU

12.2.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.3: isync command arguments

12.2.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.4: itrace command arguments

12.3 Level 3: VPE

12.3.1 isync

specify instruction address range for synchronous execution

Argument		*
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.5: isync command arguments

12.3.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.6: itrace command arguments

12.4 Level 4: TC

12.4.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.7: isync command arguments

12.4.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.8: itrace command arguments

12.4.3 mipsCOP0

query a COP0 register value using <register><select>

Argument	Type	Description
-register	Uns32	specify the COP0 register number
-select	Uns32	specify the COP0 register select

Table 12.9: mipsCOP0 command arguments

12.4.4 mipsCacheDisable

12.4.4.1 Argument description

Disables tag or full cache model

12.4.5 mipsCacheEnable

enable tag or full cache model

Argument	Type	Description
-debug	Uns32	set cache model debug flags
-full	Boolean	enable full cache model
-tag	Boolean	enable cache tag line only model

Table 12.10: mipsCacheEnable command arguments

12.4.6 mipsCacheRatio

Report current hit ratio for selected cache

Argument	Type	Description			
-dcache	Boolean	report hit ratio for dcache			
-icache	Boolean	report hit ratio for icache			

Table 12.11: mipsCacheRatio command arguments

12.4.7 mipsCacheReport

12.4.7.1 Argument description

Report current cache statistics

12.4.8 mipsCacheReset

12.4.8.1 Argument description

reset the cache model

12.4.9 mipsCacheTrace

Control the tracing of cache accesses

Argument	Type	Description			
-noartifact	Boolean	filter artifact accesses			
-nocached	Boolean	filter cached accesses			
-nodcache	Boolean	filter dcache accesses			
-noicache	Boolean	filter icache accesses			
-notrue	Boolean	filter true accesses			
-nouncached	Boolean	filter uncached accesses			
-off	Boolean	turn off the cache tracing			
-on	Boolean	turn on the cache tracing			

Table 12.12: mipsCacheTrace command arguments

12.4.10 mipsDebugFlags

Set the processor model debug flags to <value>

Argument	Type	Description			
-value	Uns32	specify model debug flags			

Table 12.13: mipsDebugFlags command arguments

12.4.11 mipsReadRegister

Read a processor register using <resource><offset>

Argument	Type	Description			
-offset	Uns32	the processor register offset			
-resource	Uns32	the processor register resource number			

Table 12.14: mipsReadRegister command arguments

12.4.12 mipsReadTLBEntry

read a TLB entry specified by the index

Argument	Type	Description		
-index	Uns64	select the TLB entry		

Table 12.15: mipsReadTLBEntry command arguments

12.4.13 mipsTLBDump

12.4.13.1 Argument description

Dumps the current contents of the TLB

12.4.14 mipsTLBGetPhys

Reports the entry(s) in the TLB that match the given virtual address and ASID

Argument	Type	Description			
-asid	Uns64	ASID			
-va	Uns64	virtual address			

Table 12.16: mipsTLBGetPhys command arguments

12.4.15 mipsWriteRegister

Write to a processor register using <resource><offset><value>

Argument	Type	Description		
-offset	Uns32	the register offset number		
-resource	Uns32	the register resource number		
-value	Uns64	the register value to be written		

Table 12.17: mipsWriteRegister command arguments

12.4.16 mipsWriteTLBEntry

Writes values to a TLB entry using the index, lo0, lo1, hi0 and mask fields

Argument	Type	Description
----------	------	-------------

-hi0	Uns64	the TLB entry high address
-index	Uns64	the TLB entry index
-lo0	Uns64	the TLB entry low address 0
-lo1	Uns64	the TLB entry low address 1
-mask	Uns64	the TLB entry mask

Table 12.18: mipsWriteTLBEntry command arguments

Registers

13.1 Level 1: CMP

No registers.

13.2 Level 2: CPU

No registers.

13.3 Level 3: VPE

13.3.1 COP0

Registers at level:3, type: VPE group: COP0 $\,$

Name	Bits	Initial-Hex	RW	Description
bad	32	0	rw	CP0 register 8/0 (badvaaddr)
cause	32	0	rw	CP0 register 13/0 (cause)
index	32	0	rw	CP0 register 0/0
mvpcontrol	32	0	rw	CP0 register 0/1
mvpconf0	32	88008401	rw	CP0 register 0/2
mvpconf1	32	0	rw	CP0 register 0/3
random	32	0	rw	CP0 register 1/0
vpecontrol	32	0	rw	CP0 register 1/1
vpeconf0	32	80000003	rw	CP0 register 1/2
vpeconf1	32	0	rw	CP0 register 1/3
yqmask	32	0	rw	CP0 register 1/4
vpeschedule	32	0	rw	CP0 register 1/5
vpeschefback	32	0	rw	CP0 register 1/6
vpeopt	32	0	rw	CP0 register 1/7
entrylo0	32	0	rw	CP0 register 2/0
entrylo1	32	0	rw	CP0 register 3/0
context	32	0	rw	CP0 register 4/0
pagemask	32	0	rw	CP0 register 5/0
wired	32	0	rw	CP0 register 6/0
srsconf0	32	3ffffff	rw	CP0 register 6/1
hwrena	32	0	rw	CP0 register 7/0
badvaddr	32	0	rw	CP0 register 8/0
count	32	0	rw	CP0 register 9/0

compare	32	0	rw	CP0 register 11/0
intctl	32	e0000000	rw	CP0 register 12/1
srsctl	32	0	rw	CP0 register 12/2
srsmap	32	0	rw	CP0 register 12/3
epc	32	0	rw	CP0 register 14/0
prid	32	19900	rw	CP0 register 15/0
ebase	32	80000000	rw	CP0 register 15/1
cmgcrbase	32	1fbf800	rw	CP0 register 15/3
config	32	80048482	rw	CP0 register 16/0
config1	32	9e231186	rw	CP0 register 16/1
config2	32	80000000	rw	CP0 register 16/2
config3	32	20002424	rw	CP0 register 16/3
config7	32	80080100	rw	CP0 register 16/7
depc	32	0	rw	CP0 register 24/0
errctl	32	0	rw	CP0 register 26/0
itaglo	32	0	rw	CP0 register 28/0
idatalo	32	0	rw	CP0 register 28/1
dtaglo	32	0	rw	CP0 register 28/2
ddatalo	32	0	rw	CP0 register 28/3
l23taglo	32	0	rw	CP0 register 28/4
l23datalo	32	0	rw	CP0 register 28/5
itaghi	32	0	rw	CP0 register 29/0
idatahi	32	0	rw	CP0 register 29/1
dtaghi	32	0	rw	CP0 register 29/2
l23datahi	32	0	rw	CP0 register 29/5
errorepc	32	0	rw	CP0 register 30/0
desave	32	0	rw	CP0 register 31/0

Table 13.1: Registers at level 3, type:VPE group:COP0

13.3.2 CMP_GCR

Registers at level:3, type:VPE group:CMP_GCR

Name	Bits	Initial-Hex	RW	Description
GCR_CONFIG	32	3	r-	
GCR_BASE	32	1fbf8000	rw	
GCR_CONTROL	32	10001	rw	
GCR_ACCESS	32	ff	rw	
GCR_REV	32	0	r-	
GCR_ERROR_MASK	32	0	rw	
GCR_ERROR_CAUSE	32	0	rw	
GCR_ERROR_ADDR	32	0	rw	
GCR_ERROR_MULT	32	0	rw	
GCR_GIC_BASE	32	0	rw	
GCR_CPC_BASE	32	0	rw	
GCR_GIC_STATUS	32	1	r-	
GCR_CACHE_REV	32	0	r-	
GCR_CPC_STATUS	32	1	r-	
GCR_IOCU1_REV	32	0	r-	
GCR_CL_RESET_RELEASE_L	32	0	-w	
GCR_CL_COHERENCE_L	32	0	rw	
GCR_CL_CONFIG_L	32	1	r-	
GCR_CL_OTHER_L	32	0	rw	
GCR_CL_RESET_BASE_L	32	bfc00000	rw	
GCR_CL_ID_L	32	0	r-	

GCR_CL_RESET_RELEASE_O	32	0	-w	
GCR_CL_COHERENCE_O	32	0	rw	
GCR_CL_CONFIG_O	32	1	r-	
GCR_CL_OTHER_O	32	0	rw	
GCR_CL_RESET_BASE_O	32	bfc00000	rw	
GCR_CL_ID_O	32	0	r-	

Table 13.2: Registers at level 3, type:VPE group:CMP_GCR

13.3.3 CMP_CPC

Registers at level:3, type:VPE group:CMP_CPC

Name	Bits	Initial-Hex	RW	Description
CPC_ACCESS	32	ff	rw	
CPC_SEQDEL	32	0	rw	
CPC_RAIL	32	0	rw	
CPC_RESETLEN	32	0	rw	
CPC_REVISION	32	0	r-	
CPC_CMD_L	32	0	rw	
CPC_STAT_CONF_L	32	380200	rw	
CPC_OTHER_L	32	0	rw	
CPC_CMD_O	32	0	rw	
CPC_STAT_CONF_O	32	380200	rw	
CPC_OTHER_O	32	0	rw	

Table 13.3: Registers at level 3, type:VPE group:CMP_CPC

13.3.4 CMP_GIC

Registers at level:3, type:VPE group:CMP_GIC

Name	Bits	Initial-Hex	RW	Description
GIC_SH_CONFIG	32	8040007	rw	
GIC_CounterLo	32	0	rw	
GIC_CounterHi	32	0	rw	
GIC_SH_REVISION	32	0	r-	
GIC_SH_POL31_0	32	0	rw	
GIC_SH_POL63_32	32	0	rw	
GIC_SH_POL95_64	32	0	rw	
GIC_SH_POL127_96	32	0	rw	
GIC_SH_POL159_128	32	0	rw	
GIC_SH_POL191_160	32	0	rw	
GIC_SH_POL223_192	32	0	rw	
GIC_SH_POL255_224	32	0	rw	
GIC_SH_TRIG31_0	32	0	rw	
GIC_SH_TRIG63_32	32	0	rw	
GIC_SH_TRIG95_64	32	0	rw	
GIC_SH_TRIG127_96	32	0	rw	
GIC_SH_TRIG159_128	32	0	rw	
GIC_SH_TRIG191_160	32	0	rw	
GIC_SH_TRIG223_192	32	0	rw	
GIC_SH_TRIG255_224	32	0	rw	
GIC_SH_DUAL31_0	32	0	rw	
GIC_SH_DUAL63_32	32	0	rw	

GIC SH DUAL127 96 GIC SH DUAL191,160 GIC SH DUAL191,160 GIC SH DUAL191,160 GIC SH DUAL191,160 GIC SH DUAL252,224 32 0 rw GIC SH DUAL255,224 32 0 rw GIC SH WEDGE GIC SH WEDGE 32 0 -w GIC SH WEDGE 32 0 -w GIC SH RMASK31.0 32 0 -w GIC SH RMASK159,128 GIC SH RMASK159,128 GIC SH RMASK191,160 GIC SH RMASK195,64 GIC SH RMASK195,64 GIC SH SMASK195,64 GIC SH SMASK197,66 GIC SH SMASK197,67 GIC SH SMASK197 GIC SH SMASK197,67 GIC SH SMASK197 GIC SH SMASK			T _	1	T
GIC SH DUALI91 160 32 0 PW GIC SH DUALI91 160 32 0 PW GIC SH DUAL23192 32 0 PW GIC SH DUAL235 224 32 0 PW GIC SH DUAL255 224 32 0 PW GIC SH DUAL255 224 32 0 PW GIC SH RMASK01 32 0 PW GIC SH RMASK03 32 32 0 PW GIC SH RMASK05 34 32 0 PW GIC SH RMASK127 96 32 0 PW GIC SH RMASK223,192 32 0 PW GIC SH RMASK223,192 32 0 PW GIC SH RMASK223 192 32 0 PW GIC SH RMASK230 10 PW GIC SH RMASK230 PW GIC SH RMASK230 PW GIC SH RMASK230 PW GIC SH RMASK230 PW GIC	GIC_SH_DUAL95_64	32	0	rw	
GIC.SH.DUAL191.160 GIC.SH.DUAL255.221 GIC.SH.DUAL255.221 GIC.SH.WEDGE GIC.SH.WASK81.0 GIC.SH.WASK81.0 GIC.SH.WASK83.32 GIC.SH.WASK95.64 GIC.SH.WASK825.64 GIC.SH.WASK825.64 GIC.SH.SMASK159.160 GIC.SH.SMASK159.180 GIC.SH.SMASK159.180 GIC.SH.WASK83.32 GIC.SH.SMASK83.32 GIC.SH.SMASK33.0 GIC.SH.SMASK33.0 GIC.SH.SMASK33.0 GIC.SH.SMASK33.0 GIC.SH.SMASK33.0 GIC.SH.SMASK33.0 GIC.SH.SMASK33.0 GIC.SH.SMASK33.0 GIC.SH.SMASK33.0 GIC.SH.SMASK33.2 GIC.SH.SMASK33.0 GIC.SH.MASK33.0 GIC.SH.MAP00.2PIN GIC.SH.MAP00		_		rw	
GIC SH_DUAL225.224 32		-	_	rw	
GIC SH_WEDGE GIC SH_RMASK31.0 32 0 -w GIC SH_RMASK03.2 32 0 -w GIC SH_RMASK03.2 32 0 -w GIC SH_RMASK05.64 32 0 -w GIC SH_RMASK15.0 GIC SH_RMASK23.192 GIC SH_RMASK23.192 GIC SH_RMASK23.0 GIC SH_RMASK23.0 GIC SH_RMASK23.0 GIC SH_RMASK23.0 GIC SH_RMASK23.0 GIC SH_SMASK31.0 GIC SH_SMASK179.66 32 0 -w GIC SH_SMASK179.61 GIC SH_SMASK179.06 GIC SH_MAPOO.PIN	GIC_SH_DUAL191_160	32	0	rw	
GIC SH WEDGE 32		_	-	rw	
GIC SH.RMASK63.10 32 0 -w	GIC_SH_DUAL255_224	32	0	rw	
GIC SH RMASK63 32 GIC.SH.RMASK195.64 GIC.SH.RMASK197.96 GIC.SH.RMASK191.98 GIC.SH.RMASK191.160 GIC.SH.RMASK191.160 GIC.SH.RMASK191.160 GIC.SH.RMASK231.192 GIC.SH.RMASK231.192 GIC.SH.RMASK23.192 GIC.SH.RMASK23.192 GIC.SH.RMASK23.192 GIC.SH.RMASK33.10 GIC.SH.RMASK33.10 GIC.SH.SMASK35.24 GIC.SH.SMASK35.24 GIC.SH.SMASK191.160 GIC.SH.SMASK191.160 GIC.SH.SMASK191.160 GIC.SH.SMASK191.160 GIC.SH.SMASK23.192 GIC.SH.SMASK33.2 GIC.SH.SMASK33.3 GIC.SH.MAPO03.PIN GIC.SH.MAP	GIC_SH_WEDGE	32	0	-w	
GIC SH RMASK195 64 GIC SH RMASK195 128 GIC SH RMASK191 160 GIC SH RMASK191 160 GIC SH RMASK191 160 GIC SH RMASK191 160 GIC SH RMASK23192 GIC SH RMASK2310 GIC SH SMASK310 GIC SH SMASK195,64 GIC SH SMASK195,128 GIC SH SMASK195,128 GIC SH SMASK195,128 GIC SH SMASK23192 GIC SH SMASK23192 GIC SH SMASK23192 GIC SH SMASK2310 GIC SH SMASK310 GIC SH SMAS		32	0	-w	
GIC. SH.RMASK19.128 32 0w GIC. SH.RMASK19.128 32 0w GIC. SH.RMASK19.160 32 0w GIC. SH.RMASK23.192 32 0w GIC. SH.RMASK25.224 32 0w GIC. SH.RMASK25.224 32 0w GIC. SH.RMASK25.224 32 0w GIC. SH.SMASK3.10 32 0w GIC. SH.SMASK19.180 32 0w GIC. SH.SMASK19.128 32 0w GIC. SH.SMASK3.10 32 0w GIC. SH.SMASK3.20 0w GIC. SH.SMASK3.	GIC_SH_RMASK63_32	32	0	-w	
GIC SH RMASK191.160 32 0 -w GIC SH RMASK191.160 32 0 -w GIC SH RMASK23.192 32 0 -w GIC SH RMASK255.224 32 0 -w GIC SH RMASK255.224 32 0 -w GIC SH RMASK33.10 32 0 -w GIC SH SMASK33.2 32 0 -w GIC SH SMASK3.32 32 0 -w GIC SH SMASK19.186 32 0 -w GIC SH SMASK3.30 32 0 -w GIC SH SMASK3.30 32 0 -r GIC SH SMASK3.32 32 0 -r GIC SH MASK3.30 32 0 -r GIC SH MASK255.224 32 0 -r GIC SH MASK255.224 32 0 -r GIC SH PEND3.30 32 0 -r GIC SH MAP00.40 70 32 80000000 70 GIC SH MAP00.40 70 3	GIC_SH_RMASK95_64	32	0	-w	
GIC SH RMASK191_160 32 0 -w GIC SH RMASK231.92 32 0 -w GIC SH RMASK231.92 32 0 -w GIC SH SMASK31.0 32 0 -w GIC SH SMASK19.64 32 0 -w GIC SH SMASK19.160 32 0 -w GIC SH SMASK191.160 32 0 -w GIC SH SMASK191.160 32 0 -w GIC SH SMASK23.192 32 0 -w GIC SH SMASK23.192 32 0 -w GIC SH SMASK31.0 32 0 -r GIC SH MASK31.0 32 0 -r GIC SH PEND1.0 32 0 -r GIC SH MAPO0.0 PIN 32 8000000 rw GIC SH MAPO0.1 PIN 32 8000000 rw GIC SH MAPO0.2 PIN 32 8000000 rw GIC SH MAPO0.7 PIN 32 80000000 rw GIC SH MAPO0.7 PIN 32 80000000 rw GIC SH MAPO0	GIC_SH_RMASK127_96	32	0	-w	
GIC.SH.RMASK223.192	GIC_SH_RMASK159_128	32	0	-w	
GIC.SH.RMASK25.224 32 0 -w GIC.SH.SMASK31.0 32 0 -w GIC.SH.SMASK63.32 32 0 -w GIC.SH.SMASK65.64 32 0 -w GIC.SH.SMASK159.128 32 0 -w GIC.SH.SMASK191.160 32 0 -w GIC.SH.SMASK191.160 32 0 -w GIC.SH.SMASK25.224 32 0 -w GIC.SH.SMASK31.0 32 0 -w GIC.SH.SMASK31.0 32 0 -r GIC.SH.MASK32.3 2 0 -r GIC.SH.MASK31.0 32 0 -r GIC.SH.MASK31.0 32 0 -r GIC.SH.MASK32.3 2 0 -r GIC.SH.MASK32.3 2 0 -r GIC.SH.MASK32.3 2 0 -r GIC.SH.MASK32 32 0 -r GIC.SH.MASK32	GIC_SH_RMASK191_160	32	0	-w	
GIC.SH.SMASK63.10 GIC.SH.SMASK63.32 GIC.SH.SMASK65.64 GIC.SH.SMASK127.96 GIC.SH.SMASK159.128 GIC.SH.SMASK159.128 GIC.SH.SMASK159.128 GIC.SH.SMASK19.160 GIC.SH.SMASK19.160 GIC.SH.SMASK231.192 GIC.SH.SMASK231.192 GIC.SH.SMASK231.192 GIC.SH.SMASK231.192 GIC.SH.SMASK231.192 GIC.SH.SMASK231.192 GIC.SH.MASK33.2 GIC.SH.SMASK23.2 GIC.SH.MASK33.2 GIC.SH.MASK33.2 GIC.SH.MASK33.2 GIC.SH.MASK25.24 GIC.SH.M	GIC_SH_RMASK223_192	32	0	-w	
GIC.SH.SMASK63.32	GIC_SH_RMASK255_224	32	0	-w	
GIC.SH.SMASK127.96 32 0w GIC.SH.SMASK127.96 32 0w GIC.SH.SMASK191.160 32 0w GIC.SH.SMASK191.160 32 0w GIC.SH.SMASK231.192 32 0w GIC.SH.SMASK231.192 32 0w GIC.SH.SMASK231.192 32 0w GIC.SH.SMASK231.0 32 0 -r- GIC.SH.MASK31.0 32 0 -r- GIC.SH.MASK31.0 32 0 -r- GIC.SH.MASK31.0 32 0 -r- GIC.SH.MASK31.0 32 0 -r- GIC.SH.MASK197.96 32 0 -r- GIC.SH.MASK197.96 32 0 -r- GIC.SH.MASK191.160 32 0 -r- GIC.SH.MASK191.160 32 0 -r- GIC.SH.MASK191.160 32 0 -r- GIC.SH.MASK231.192 32 0 -r- GIC.SH.MASK255.224 32 0 -r- GIC.SH.MASK255.224 32 0 -r- GIC.SH.PEND31.0 32 0 -r- GIC.SH.PEND31.0 32 0 -r- GIC.SH.PEND95.64 32 0 -r- GIC.SH.PEND189.182 32 0 -r- GIC.SH.PEND192.832 32 0 -r- GIC.SH.PEND192.96 32 0 -r- GIC.SH.PEND192.98 32 0 -r- GIC.SH.PEND191.160 32 0 -r- GIC.SH.PEND192.193 32 0 -r- GIC.SH.PEND192.194 32 0 -r- GIC.SH.PEND23.192 32 0 -r- GIC.SH.PEND193.195 32 0 -r- GIC.SH.PEND23.192 32 0 -r- GIC.SH.PEND191.160 32 0 -r- GIC.SH.MAP000.PIN 32 8000000 rw GIC.SH.MAP000.PIN 32 8000000 rw GIC.SH.MAP000.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 80000000 rw	GIC_SH_SMASK31_0	32	0	-w	
GIC.SH.SMASK127.96 GIC.SH.SMASK159.128 GIC.SH.SMASK191.160 GIC.SH.SMASK19.128 GIC.SH.SMASK19.129 GIC.SH.SMASK23.192 GIC.SH.SMASK23.192 GIC.SH.SMASK255.224 GIC.SH.SMASK325.224 GIC.SH.MASK3.32 GIC.SH.MASK3.32 GIC.SH.MASK3.32 GIC.SH.MASK3.32 GIC.SH.MASK127.96 GIC.SH.MASK19.128 GIC.SH.MASK19.128 GIC.SH.MASK19.128 GIC.SH.MASK19.128 GIC.SH.MASK23.192 GIC.SH.MASK23.192 GIC.SH.MASK23.192 GIC.SH.MASK23.192 GIC.SH.PEND31.0 GIC.SH.PEND31.0 GIC.SH.PEND31.0 GIC.SH.PEND31.0 GIC.SH.PEND31.0 GIC.SH.PEND31.0 GIC.SH.PEND31.0 GIC.SH.PEND31.28 GIC.SH.PEND31.29 GIC.SH.PEND31.29 GIC.SH.PEND31.29 GIC.SH.PEND31.29 GIC.SH.PEND31.28 GIC.SH.PEND3.31 GIC.SH.PEND3.31 GIC.SH.PEND3.31 GIC.SH.PEND3.31 GIC.SH.PEND3.31 GIC.SH.PEND3.31 GIC.SH.MAP000.PIN GIC.SH.MAP000.PIN GIC.SH.MAP001.PIN GIC.SH.MAP001.PIN GIC.SH.MAP003.PIN GIC.SH.MAP003.PIN GIC.SH.MAP005.PIN GIC.SH.MAP006.PIN GIC.SH.MAP006.PIN GIC.SH.MAP006.PIN GIC.SH.MAP007.PIN GIC.SH.MAP008.PIN GIC.SH.MAP008.PIN GIC.SH.MAP008.PIN GIC.SH.MAP008.PIN GIC.SH.MAP009.PIN GIC.SH.MAP008.PIN GIC.SH.MAP009.PIN GIC	GIC_SH_SMASK63_32	32	0	-w	
GIC.SH.SMASK159.128 32 0 -w GIC.SH.SMASK191.160 32 0 -w GIC.SH.SMASK233.192 32 0 -w GIC.SH.SMASK233.192 32 0 -w GIC.SH.SMASK233.192 32 0 -r GIC.SH.MASK31.0 32 0 r- GIC.SH.MASK33.2 32 0 r- GIC.SH.MASK33.2 32 0 r- GIC.SH.MASK191.60 32 0 r- GIC.SH.MASK191.88 32 0 r- GIC.SH.MASK19.128 32 0 r- GIC.SH.MASK19.128 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MASK23.190 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.PEND31.0 32 0 r- GIC.SH.PEND31.0 32 0 r- GIC.SH.PEND127.96 32 0 r- GIC.SH.PEND127.96 32 0 r- GIC.SH.PEND127.96 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.PEND23.192 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.MAP000.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP003.PIN 32 8000000 rw GIC.SH.MAP004.PIN 32 8000000 rw GIC.SH.MAP005.PIN 32 8000000 rw GIC.SH.MAP006.PIN 32 8000000 rw GIC.SH.MAP006.PIN 32 8000000 rw GIC.SH.MAP009.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP011.PIN 32 8000000 rw GIC.SH.MAP011.PIN 32 80000000 rw	GIC_SH_SMASK95_64	32	0	-w	
GIC.SH.SMASK159.128 32 0 -w GIC.SH.SMASK191.160 32 0 -w GIC.SH.SMASK233.192 32 0 -w GIC.SH.SMASK233.192 32 0 -w GIC.SH.SMASK233.192 32 0 -r GIC.SH.MASK31.0 32 0 r- GIC.SH.MASK33.2 32 0 r- GIC.SH.MASK33.2 32 0 r- GIC.SH.MASK191.60 32 0 r- GIC.SH.MASK191.88 32 0 r- GIC.SH.MASK19.128 32 0 r- GIC.SH.MASK19.128 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MASK23.190 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.PEND31.0 32 0 r- GIC.SH.PEND31.0 32 0 r- GIC.SH.PEND127.96 32 0 r- GIC.SH.PEND127.96 32 0 r- GIC.SH.PEND127.96 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.PEND23.192 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.MAP000.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP003.PIN 32 8000000 rw GIC.SH.MAP004.PIN 32 8000000 rw GIC.SH.MAP005.PIN 32 8000000 rw GIC.SH.MAP006.PIN 32 8000000 rw GIC.SH.MAP006.PIN 32 8000000 rw GIC.SH.MAP009.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP011.PIN 32 8000000 rw GIC.SH.MAP011.PIN 32 80000000 rw		32	0	-	
GIC.SH.SMASK191.160 32 0 -w GIC.SH.SMASK223.192 32 0 -w GIC.SH.SMASK225.224 32 0 -r GIC.SH.MASK31.0 32 0 r- GIC.SH.MASK63.2 32 0 r- GIC.SH.MASK63.2 32 0 r- GIC.SH.MASK95.64 32 0 r- GIC.SH.MASK159.128 32 0 r- GIC.SH.MASK159.128 32 0 r- GIC.SH.MASK191.160 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MASK25.224 32 0 r- GIC.SH.PEND63.32 32 0 r- GIC.SH.PEND63.32 32 0 r- GIC.SH.PEND191.0 32 0 r- GIC.SH.PEND191.0 32 0 r- GIC.SH.PEND195.64 32 0 r- GIC.SH.PEND195.64 32 0 r- GIC.SH.PEND195.128 32 0 r- GIC.SH.PEND195.128 32 0 r- GIC.SH.PEND195.128 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.PEND195.128 32 0 r- GIC.SH.PEND191.180 32 0 r- GIC.SH.PEND191.180 32 0 r- GIC.SH.PEND191.180 32 0 r- GIC.SH.MAP000.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP003.PIN 32 8000000 rw GIC.SH.MAP004.PIN 32 8000000 rw GIC.SH.MAP005.PIN 32 8000000 rw GIC.SH.MAP006.PIN 32 8000000 rw GIC.SH.MAP006.PIN 32 8000000 rw GIC.SH.MAP007.PIN 32 8000000 rw GIC.SH.MAP008.PIN 32 8000000 rw GIC.SH.MAP009.PIN 32 8000000 rw GIC.SH.MAP011.PIN 32 80000000 rw		_	-	-	
GIC.SH.SMASK223.192 32 0 -w GIC.SH.SMASK255.224 32 0 -w GIC.SH.MASK31.0 32 0 r- GIC.SH.MASK63.32 32 0 r- GIC.SH.MASK95.64 32 0 r- GIC.SH.MASK17.96 32 0 r- GIC.SH.MASK19.188 32 0 r- GIC.SH.MASK19.189 32 0 r- GIC.SH.MASK19.180 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.PEND63.32 0 r- GIC.SH.PEND63.32 0 r- GIC.SH.PEND127.96 32 0 r- GIC.SH.PEND117.96 32 0 r- GIC.SH.PEND159.128 32 0 r- GIC.SH.PEND159.128 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.PEND23.192 32 0 r- GIC.SH.MAP000.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP003.PIN 32 8000000 rw GIC.SH.MAP004.PIN 32 8000000 rw GIC.SH.MAP005.PIN 32 8000000 rw GIC.SH.MAP005.PIN 32 8000000 rw GIC.SH.MAP006.PIN 32 8000000 rw GIC.SH.MAP006.PIN 32 8000000 rw GIC.SH.MAP008.PIN 32 8000000 rw GIC.SH.MAP008.PIN 32 8000000 rw GIC.SH.MAP009.PIN 32 8000000 rw GIC.SH.MAP010.PIN 32 8000000 rw					
GIC.SH.SMASK255.224 32 0 r- GIC.SH.MASK31.0 32 0 r- GIC.SH.MASK332 32 0 r- GIC.SH.MASK35.64 32 0 r- GIC.SH.MASK17.96 32 0 r- GIC.SH.MASK19.128 32 0 r- GIC.SH.MASK19.128 32 0 r- GIC.SH.MASK19.128 32 0 r- GIC.SH.MASK19.128 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MASK255.224 32 0 r- GIC.SH.PEND31.0 32 0 r- GIC.SH.PEND31.0 32 0 r- GIC.SH.PEND195.64 32 0 r- GIC.SH.PEND195.64 32 0 r- GIC.SH.PEND197.66 32 0 r- GIC.SH.PEND191.60 32 0 r- GIC.SH.PEND199.18 32 0 r- GIC.SH.PEND191.10 32 0 r- GIC.SH.MAP000.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP005.PIN 32 8000000 rw GIC.SH.MAP005.PIN 32 8000000 rw GIC.SH.MAP006.PIN 32 8000000 rw GIC.SH.MAP006.PIN 32 8000000 rw GIC.SH.MAP006.PIN 32 8000000 rw GIC.SH.MAP006.PIN 32 8000000 rw GIC.SH.MAP007.PIN 32 8000000 rw GIC.SH.MAP008.PIN 32 8000000 rw GIC.SH.MAP008.PIN 32 8000000 rw GIC.SH.MAP009.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP011.PIN 32 80000000 rw		32	0		
GIC.SH.MASK63.32 32 0 r- GIC.SH.MASK63.32 32 0 r- GIC.SH.MASK63.32 0 r- GIC.SH.MASK159.64 32 0 r- GIC.SH.MASK159.128 32 0 r- GIC.SH.MASK191.160 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MSK255.224 32 0 r- GIC.SH.PEND31.0 32 0 r- GIC.SH.PEND63.32 32 0 r- GIC.SH.PEND95.64 32 0 r- GIC.SH.PEND127.96 32 0 r- GIC.SH.PEND159.128 32 0 r- GIC.SH.PEND159.128 32 0 r- GIC.SH.PEND255.224 32 0 r- GIC.SH.PEND255.224 32 0 r- GIC.SH.PEND1019.160 32 0 r- GIC.SH.PEND255.224 32 0 r- GIC.SH.PEND255.224 32 0 r- GIC.SH.PEND255.224 32 0 r- GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP004.PIN 32 80000000 rw GIC.SH.MAP005.PIN 32 80000000 rw GIC.SH.MAP005.PIN 32 80000000 rw GIC.SH.MAP006.PIN 32 80000000 rw GIC.SH.MAP006.PIN 32 80000000 rw GIC.SH.MAP007.PIN 32 80000000 rw GIC.SH.MAP007.PIN 32 80000000 rw GIC.SH.MAP008.PIN 32 80000000 rw GIC.SH.MAP007.PIN 32 80000000 rw GIC.SH.MAP007.PIN 32 80000000 rw GIC.SH.MAP008.PIN 32 80000000 rw GIC.SH.MAP009.PIN 32 80000000 rw GIC.SH.MAP009.PIN 32 80000000 rw GIC.SH.MAP009.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP011.PIN 32 80000000 rw			-	+	
GIC.SH.MASK63.32		_	-	+	
GIC.SH.MASK197.96 32 0 r- GIC.SH.MASK197.96 32 0 r- GIC.SH.MASK191.160 32 0 r- GIC.SH.MASK191.160 32 0 r- GIC.SH.MASK231.192 32 0 r- GIC.SH.MASK255.224 32 0 r- GIC.SH.PEND31.0 32 0 r- GIC.SH.PEND197.96 32 0 r- GIC.SH.PEND197.96 32 0 r- GIC.SH.PEND197.96 32 0 r- GIC.SH.PEND197.96 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.MAP000.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP004.PIN 32 80000000 rw GIC.SH.MAP004.PIN 32 80000000 rw GIC.SH.MAP005.PIN 32 80000000 rw GIC.SH.MAP005.PIN 32 80000000 rw GIC.SH.MAP005.PIN 32 80000000 rw GIC.SH.MAP005.PIN 32 80000000 rw GIC.SH.MAP008.PIN 32 80000000 rw GIC.SH.MAP008.PIN 32 80000000 rw GIC.SH.MAP009.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP011.PIN 32 80000000 rw		_	_		
GIC_SH_MASK127_96 32 0 r- GIC_SH_MASK191_160 32 0 r- GIC_SH_MASK191_160 32 0 r- GIC_SH_MASK223_192 32 0 r- GIC_SH_MASK255_224 32 0 r- GIC_SH_PEND31_0 32 0 r- GIC_SH_PEND31_0 32 0 r- GIC_SH_PEND63.32 32 0 r- GIC_SH_PEND63.32 32 0 r- GIC_SH_PEND195_64 32 0 r- GIC_SH_PEND127_96 32 0 r- GIC_SH_PEND127_96 32 0 r- GIC_SH_PEND191_160 32 0 r- GIC_SH_PEND191_160 32 0 r- GIC_SH_PEND223_192 32 0 r- GIC_SH_PEND255_224 32 0 r- GIC_SH_PEND255_224 32 0 r- GIC_SH_PEND255_224 32 0 r- GIC_SH_MAP000_PIN 32 80000000 rw GIC_SH_MAP001_PIN 32 80000000 rw GIC_SH_MAP003_PIN 32 80000000 rw GIC_SH_MAP004_PIN 32 80000000 rw GIC_SH_MAP004_PIN 32 80000000 rw GIC_SH_MAP005_PIN 32 80000000 rw GIC_SH_MAP001_PIN 32 80000000 rw GIC_SH_MAP001_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw			-	-	
GIC.SH.MASK159.128 32 0 r- GIC.SH.MASK23.192 32 0 r- GIC.SH.MASK223.192 32 0 r- GIC.SH.PEND31.0 32 0 r- GIC.SH.PEND31.0 32 0 r- GIC.SH.PEND63.32 32 0 r- GIC.SH.PEND95.64 32 0 r- GIC.SH.PEND127.96 32 0 r- GIC.SH.PEND159.128 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.PEND23.192 32 0 r- GIC.SH.PEND23.192 32 0 r- GIC.SH.PEND255.224 32 0 r- GIC.SH.MAP000.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP003.PIN 32 8000000 rw GIC.SH.MAP004.PIN 32 8000000 rw GIC.SH.MAP011.PIN 32 80000000 rw GIC.SH.MAP014.PIN 32 80000000 rw GIC.SH.MAP015.PIN 32 80000000 rw			-	-	
GIC_SH_MASK191_160 32 0 r- GIC_SH_MASK223_192 32 0 r- GIC_SH_MASK255_224 32 0 r- GIC_SH_PEND31_0 32 0 r- GIC_SH_PEND31_0 32 0 r- GIC_SH_PEND63_32 32 0 r- GIC_SH_PEND63_32 32 0 r- GIC_SH_PEND19_160 32 0 r- GIC_SH_PEND19_18 32 0 r- GIC_SH_PEND19_18 32 0 r- GIC_SH_PEND19_18 32 0 r- GIC_SH_PEND23_192 32 0 r- GIC_SH_PEND23_192 32 0 r- GIC_SH_PEND23_192 32 0 r- GIC_SH_PEND23_191 32 0 r- GIC_SH_PEND23_191 32 80000000 rw GIC_SH_MAP00_PIN 32 80000000 rw GIC_SH_MAP01_PIN 32 80000000 rw		_	_		
GIC.SH.MASK223.192 32 0 r- GIC.SH.MASK255.224 32 0 r- GIC.SH.PEND31.0 32 0 r- GIC.SH.PEND63.32 32 0 r- GIC.SH.PEND63.32 32 0 r- GIC.SH.PEND95.64 32 0 r- GIC.SH.PEND127.96 32 0 r- GIC.SH.PEND159.128 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.PEND23.192 32 0 r- GIC.SH.PEND23.192 32 0 r- GIC.SH.PEND23.192 32 0 r- GIC.SH.MAP000.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP003.PIN 32 8000000 rw GIC.SH.MAP004.PIN 32 8000000 rw GIC.SH.MAP005.PIN 32 8000000 rw GIC.SH.MAP006.PIN 32 8000000 rw GIC.SH.MAP006.PIN 32 8000000 rw GIC.SH.MAP006.PIN 32 8000000 rw GIC.SH.MAP009.PIN 32 8000000 rw GIC.SH.MAP001.PIN 32 8000000 rw GIC.SH.MAP01.PIN 32 80000000 rw		_	-	-	
GIC.SH.MASK255.224 32 0 r- GIC.SH.PEND63.32 32 0 r- GIC.SH.PEND95.64 32 0 r- GIC.SH.PEND127.96 32 0 r- GIC.SH.PEND195.128 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.PEND23.192 32 0 r- GIC.SH.PEND23.192 32 0 r- GIC.SH.PEND255.224 32 0 r- GIC.SH.MAP000.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP003.PIN 32 80000000 rw GIC.SH.MAP004.PIN 32 80000000 rw GIC.SH.MAP004.PIN 32 80000000 rw GIC.SH.MAP005.PIN 32 80000000 rw GIC.SH.MAP006.PIN 32 80000000 rw GIC.SH.MAP009.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP011.PIN 32 80000000 rw GIC.SH.MAP013.PIN 32 80000000 rw GIC.SH.MAP013.PIN 32 80000000 rw GIC.SH.MAP013.PIN 32 80000000 rw GIC.SH.MAP013.PIN 32 80000000 rw GIC.SH.MAP014.PIN 32 80000000 rw GIC.SH.MAP014.PIN 32 80000000 rw				-	
GIC_SH_PEND31_0 GIC_SH_PEND63_32 GIC_SH_PEND95_64 GIC_SH_PEND127_96 GIC_SH_PEND127_96 GIC_SH_PEND159_128 GIC_SH_PEND159_128 GIC_SH_PEND191_160 32 0 r- GIC_SH_PEND23_192 GIC_SH_PEND23_192 GIC_SH_PEND23_192 GIC_SH_PEND255_224 GIC_SH_PEND255_224 GIC_SH_MAP000_PIN 32 80000000 rw GIC_SH_MAP001_PIN 32 80000000 rw GIC_SH_MAP001_PIN 32 80000000 rw GIC_SH_MAP004_PIN 32 80000000 rw GIC_SH_MAP004_PIN 32 80000000 rw GIC_SH_MAP004_PIN 32 80000000 rw GIC_SH_MAP004_PIN 32 80000000 rw GIC_SH_MAP005_PIN 32 80000000 rw GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw			-	-	
GIC.SH.PEND63.32 32 0 r- GIC.SH.PEND195.64 32 0 r- GIC.SH.PEND127.96 32 0 r- GIC.SH.PEND159.128 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.PEND223.192 32 0 r- GIC.SH.PEND223.192 32 0 r- GIC.SH.PEND225.224 32 0 r- GIC.SH.MAP000.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP004.PIN 32 80000000 rw GIC.SH.MAP004.PIN 32 80000000 rw GIC.SH.MAP005.PIN 32 80000000 rw GIC.SH.MAP005.PIN 32 80000000 rw GIC.SH.MAP006.PIN 32 80000000 rw GIC.SH.MAP007.PIN 32 80000000 rw GIC.SH.MAP009.PIN 32 80000000 rw GIC.SH.MAP011.PIN 32 80000000 rw GIC.SH.MAP013.PIN 32 80000000 rw GIC.SH.MAP013.PIN 32 80000000 rw GIC.SH.MAP013.PIN 32 80000000 rw GIC.SH.MAP014.PIN 32 80000000 rw GIC.SH.MAP014.PIN 32 80000000 rw GIC.SH.MAP014.PIN 32 80000000 rw GIC.SH.MAP015.PIN 32 80000000 rw GIC.SH.MAP015.PIN 32 80000000 rw		_	_		
GIC_SH_PEND95_64 GIC_SH_PEND127_96 GIC_SH_PEND159_128 32 0 r- GIC_SH_PEND191_160 32 0 r- GIC_SH_PEND191_160 32 0 r- GIC_SH_PEND23_192 32 0 r- GIC_SH_PEND23_192 32 0 r- GIC_SH_PEND255_224 32 0 r- GIC_SH_MAP000_PIN 32 80000000 rw GIC_SH_MAP001_PIN 32 80000000 rw GIC_SH_MAP003_PIN 32 80000000 rw GIC_SH_MAP003_PIN 32 80000000 rw GIC_SH_MAP004_PIN 32 80000000 rw GIC_SH_MAP005_PIN 32 80000000 rw GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP005_PIN 32 80000000 rw GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP007_PIN 32 80000000 rw GIC_SH_MAP008_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw			-	-	
GIC_SH_PEND127_96 32 0 r- GIC_SH_PEND159_128 32 0 r- GIC_SH_PEND191_160 32 0 r- GIC_SH_PEND223_192 32 0 r- GIC_SH_PEND255_224 32 0 r- GIC_SH_MAP000_PIN 32 80000000 rw GIC_SH_MAP001_PIN 32 80000000 rw GIC_SH_MAP002_PIN 32 80000000 rw GIC_SH_MAP003_PIN 32 80000000 rw GIC_SH_MAP004_PIN 32 80000000 rw GIC_SH_MAP005_PIN 32 80000000 rw GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP008_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP012_PIN 32 80000000 rw GIC_SH_MAP014_		_		+	
GIC.SH.PEND159.128 32 0 r- GIC.SH.PEND191.160 32 0 r- GIC.SH.PEND223.192 32 0 r- GIC.SH.PEND255.224 32 0 r- GIC.SH.MAP000.PIN 32 80000000 rw GIC.SH.MAP001.PIN 32 80000000 rw GIC.SH.MAP002.PIN 32 80000000 rw GIC.SH.MAP003.PIN 32 80000000 rw GIC.SH.MAP004.PIN 32 80000000 rw GIC.SH.MAP005.PIN 32 80000000 rw GIC.SH.MAP006.PIN 32 80000000 rw GIC.SH.MAP009.PIN 32 80000000 rw GIC.SH.MAP010.PIN 32 80000000 rw GIC.SH.MAP011.PIN 32 80000000 rw GIC.SH.MAP012.PIN 32 80000000 rw GIC.SH.MAP013.PIN 32 80000000 rw GIC.SH.MAP015.PIN 32 80000000 rw		_	_		
GIC_SH_PEND191_160					
GIC_SH_PEND23_192 32 0 r- GIC_SH_MAP000_PIN 32 80000000 rw GIC_SH_MAP001_PIN 32 80000000 rw GIC_SH_MAP001_PIN 32 80000000 rw GIC_SH_MAP003_PIN 32 80000000 rw GIC_SH_MAP004_PIN 32 80000000 rw GIC_SH_MAP005_PIN 32 80000000 rw GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP007_PIN 32 80000000 rw GIC_SH_MAP008_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP001_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw			-	-	
GIC_SH_PEND255_224 32 0 r- GIC_SH_MAP000_PIN 32 80000000 rw GIC_SH_MAP001_PIN 32 80000000 rw GIC_SH_MAP002_PIN 32 80000000 rw GIC_SH_MAP004_PIN 32 80000000 rw GIC_SH_MAP005_PIN 32 80000000 rw GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP007_PIN 32 80000000 rw GIC_SH_MAP008_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw		_	-	-	
GIC_SH_MAP000_PIN 32 80000000 rw GIC_SH_MAP001_PIN 32 80000000 rw GIC_SH_MAP002_PIN 32 80000000 rw GIC_SH_MAP003_PIN 32 80000000 rw GIC_SH_MAP005_PIN 32 80000000 rw GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP007_PIN 32 80000000 rw GIC_SH_MAP008_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw		_	-		
GIC_SH_MAP001_PIN 32 80000000 rw GIC_SH_MAP002_PIN 32 80000000 rw GIC_SH_MAP003_PIN 32 80000000 rw GIC_SH_MAP004_PIN 32 80000000 rw GIC_SH_MAP005_PIN 32 80000000 rw GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP007_PIN 32 80000000 rw GIC_SH_MAP008_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw			, ,	-	
GIC_SH_MAP002_PIN 32 80000000 rw GIC_SH_MAP003_PIN 32 80000000 rw GIC_SH_MAP004_PIN 32 80000000 rw GIC_SH_MAP005_PIN 32 80000000 rw GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP007_PIN 32 80000000 rw GIC_SH_MAP008_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw				-	
GIC_SH_MAP003_PIN 32 80000000 rw GIC_SH_MAP004_PIN 32 80000000 rw GIC_SH_MAP005_PIN 32 80000000 rw GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP007_PIN 32 80000000 rw GIC_SH_MAP008_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw					
GIC_SH_MAP004_PIN 32 80000000 rw GIC_SH_MAP005_PIN 32 80000000 rw GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP007_PIN 32 80000000 rw GIC_SH_MAP008_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP012_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw				1	
GIC_SH_MAP005_PIN 32 80000000 rw GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP007_PIN 32 80000000 rw GIC_SH_MAP008_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP012_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw				+	
GIC_SH_MAP006_PIN 32 80000000 rw GIC_SH_MAP007_PIN 32 80000000 rw GIC_SH_MAP008_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP012_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw		1		+	
GIC_SH_MAP007_PIN 32 80000000 rw GIC_SH_MAP008_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP012_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw					
GIC_SH_MAP008_PIN 32 80000000 rw GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP012_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw				-	
GIC_SH_MAP009_PIN 32 80000000 rw GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP012_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw				-	
GIC_SH_MAP010_PIN 32 80000000 rw GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP012_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw					
GIC_SH_MAP011_PIN 32 80000000 rw GIC_SH_MAP012_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw				+	
GIC_SH_MAP012_PIN 32 80000000 rw GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw				+	
GIC_SH_MAP013_PIN 32 80000000 rw GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw				rw	
GIC_SH_MAP014_PIN 32 80000000 rw GIC_SH_MAP015_PIN 32 80000000 rw				rw	
GIC_SH_MAP015_PIN 32 80000000 rw		1		rw	
				rw	
GIC SH MAP016 PIN 32 80000000 rw				rw	
010_011_1111 010_1 111	GIC_SH_MAP016_PIN	32	80000000	rw	

		T	1	
GIC_SH_MAP017_PIN	32	80000000	rw	
GIC_SH_MAP018_PIN	32	80000000	rw	
GIC_SH_MAP019_PIN	32	80000000	rw	
GIC_SH_MAP020_PIN	32	80000000	rw	
GIC_SH_MAP021_PIN	32	80000000	rw	
GIC_SH_MAP022_PIN	32	80000000	rw	
GIC_SH_MAP023_PIN	32	80000000	rw	
GIC_SH_MAP024_PIN	32	80000000	rw	
GIC_SH_MAP025_PIN	32	80000000	rw	
GIC_SH_MAP026_PIN	32	80000000	rw	
GIC_SH_MAP027_PIN	32	80000000	rw	
GIC_SH_MAP028_PIN	32	80000000	rw	
GIC_SH_MAP029_PIN	32	80000000	rw	
GIC_SH_MAP030_PIN	32	80000000	rw	
GIC_SH_MAP031_PIN	32	80000000	rw	
GIC_SH_MAP032_PIN	32	80000000	rw	
GIC_SH_MAP033_PIN	32	80000000	rw	
GIC_SH_MAP034_PIN	32	80000000	rw	
GIC_SH_MAP035_PIN	32	80000000	rw	
GIC_SH_MAP036_PIN	32	80000000	rw	
GIC_SH_MAP037_PIN	32	80000000	rw	
GIC_SH_MAP038_PIN	32	80000000		
GIC_SH_MAP039_PIN	32		rw	
		80000000	rw	
GIC_SH_MAP040_PIN	32	80000000	rw	
GIC_SH_MAP041_PIN	32	80000000	rw	
GIC_SH_MAP042_PIN	32	80000000	rw	
GIC_SH_MAP043_PIN	32	80000000	rw	
GIC_SH_MAP044_PIN	32	80000000	rw	
GIC_SH_MAP045_PIN	32	80000000	rw	
GIC_SH_MAP046_PIN	32	80000000	rw	
GIC_SH_MAP047_PIN	32	80000000	rw	
GIC_SH_MAP048_PIN	32	80000000	rw	
GIC_SH_MAP049_PIN	32	80000000	rw	
GIC_SH_MAP050_PIN	32	80000000	rw	
GIC_SH_MAP051_PIN	32	80000000	rw	
GIC_SH_MAP052_PIN	32	80000000	rw	
GIC_SH_MAP053_PIN	32	80000000	rw	
GIC_SH_MAP054_PIN	32	80000000	rw	
GIC_SH_MAP055_PIN	32	80000000	rw	
GIC_SH_MAP056_PIN	32	80000000	rw	
GIC_SH_MAP057_PIN	32	80000000	rw	
GIC_SH_MAP058_PIN	32	80000000	rw	
GIC_SH_MAP059_PIN	32	80000000	rw	
GIC_SH_MAP060_PIN	32	80000000	rw	
GIC_SH_MAP061_PIN	32	80000000	rw	
GIC_SH_MAP062_PIN	32	80000000	rw	
GIC_SH_MAP063_PIN	32	80000000		
GIC_SH_MAP063_PIN GIC_SH_MAP064_PIN	32		rw	
		80000000	rw	
GIC_SH_MAP065_PIN	32	80000000	rw	
GIC_SH_MAP066_PIN	32	80000000	rw	
GIC_SH_MAP067_PIN	32	80000000	rw	
GIC_SH_MAP068_PIN	32	80000000	rw	
GIC_SH_MAP069_PIN	32	80000000	rw	
GIC_SH_MAP070_PIN	32	80000000	rw	
GIC_SH_MAP071_PIN	32	80000000	rw	
GIC_SH_MAP072_PIN	32	80000000	rw	I and the second

		T	1	
GIC_SH_MAP073_PIN	32	80000000	rw	
GIC_SH_MAP074_PIN	32	80000000	rw	
GIC_SH_MAP075_PIN	32	80000000	rw	
GIC_SH_MAP076_PIN	32	80000000	rw	
GIC_SH_MAP077_PIN	32	80000000	rw	
GIC_SH_MAP078_PIN	32	80000000	rw	
GIC_SH_MAP079_PIN	32	80000000	rw	
GIC_SH_MAP080_PIN	32	80000000	rw	
GIC_SH_MAP081_PIN	32	80000000	rw	
GIC_SH_MAP082_PIN	32	80000000	rw	
GIC_SH_MAP083_PIN	32	80000000	rw	
GIC_SH_MAP084_PIN	32	80000000	rw	
GIC_SH_MAP085_PIN	32	80000000	rw	
GIC_SH_MAP086_PIN	32	80000000	rw	
GIC_SH_MAP087_PIN	32	80000000	rw	
GIC_SH_MAP088_PIN	32	80000000	rw	
GIC_SH_MAP089_PIN	32	80000000	rw	
GIC_SH_MAP090_PIN	32	80000000	rw	
GIC_SH_MAP091_PIN	32	80000000		
			rw	
GIC_SH_MAP092_PIN	32	80000000	rw	1
GIC_SH_MAP093_PIN	32	80000000	rw	
GIC_SH_MAP094_PIN	32	80000000	rw	
GIC_SH_MAP095_PIN	32	80000000	rw	
GIC_SH_MAP096_PIN	32	80000000	rw	
GIC_SH_MAP097_PIN	32	80000000	rw	
GIC_SH_MAP098_PIN	32	80000000	rw	
GIC_SH_MAP099_PIN	32	80000000	rw	
GIC_SH_MAP100_PIN	32	80000000	rw	
GIC_SH_MAP101_PIN	32	80000000	rw	
GIC_SH_MAP102_PIN	32	80000000	rw	
GIC_SH_MAP103_PIN	32	80000000	rw	
GIC_SH_MAP104_PIN	32	80000000	rw	
GIC_SH_MAP105_PIN	32	80000000	rw	
GIC_SH_MAP106_PIN	32	80000000	rw	
GIC_SH_MAP107_PIN	32	80000000	rw	
GIC_SH_MAP108_PIN	32	80000000	rw	
GIC_SH_MAP109_PIN	32	80000000	rw	
GIC_SH_MAP110_PIN	32	80000000	rw	
GIC_SH_MAP111_PIN	32	80000000	rw	
GIC_SH_MAP112_PIN	32	80000000	rw	
GIC_SH_MAP113_PIN	32	80000000	rw	
GIC_SH_MAP114_PIN	32	80000000	rw	
GIC_SH_MAP115_PIN	32	80000000		
GIC_SH_MAP116_PIN	32	8000000	rw	
GIC_SH_MAP116_PIN GIC_SH_MAP117_PIN	32		rw	
		80000000	rw	
GIC_SH_MAP118_PIN	32	80000000	rw	
GIC_SH_MAP119_PIN	32	80000000	rw	
GIC_SH_MAP120_PIN	32	80000000	rw	
GIC_SH_MAP121_PIN	32	80000000	rw	
GIC_SH_MAP122_PIN	32	80000000	rw	
GIC_SH_MAP123_PIN	32	80000000	rw	
GIC_SH_MAP124_PIN	32	80000000	rw	
GIC_SH_MAP125_PIN	32	80000000	rw	
GIC_SH_MAP126_PIN	32	80000000	rw	
GIC_SH_MAP127_PIN	32	80000000	rw	
GIC_SH_MAP128_PIN	32	80000000	rw	
	-	1	1	

		T		T
GIC_SH_MAP129_PIN	32	80000000	rw	
GIC_SH_MAP130_PIN	32	80000000	rw	
GIC_SH_MAP131_PIN	32	80000000	rw	
GIC_SH_MAP132_PIN	32	80000000	rw	
GIC_SH_MAP133_PIN	32	80000000	rw	
GIC_SH_MAP134_PIN	32	80000000	rw	
GIC_SH_MAP135_PIN	32	80000000	rw	
GIC_SH_MAP136_PIN	32	80000000	rw	
GIC_SH_MAP137_PIN	32	80000000	rw	
GIC_SH_MAP138_PIN	32	80000000	rw	
GIC_SH_MAP139_PIN	32	80000000	rw	
GIC_SH_MAP140_PIN	32	80000000	rw	
GIC_SH_MAP141_PIN	32	80000000	rw	
GIC_SH_MAP142_PIN	32	80000000	rw	
GIC_SH_MAP143_PIN	32	80000000	rw	
GIC_SH_MAP144_PIN	32	80000000		
GIC_SH_MAP145_PIN	32	80000000	rw	
			rw	
GIC_SH_MAP146_PIN	32	80000000	rw	
GIC_SH_MAP147_PIN	32	80000000	rw	
GIC_SH_MAP148_PIN	32	80000000	rw	
GIC_SH_MAP149_PIN	32	80000000	rw	
GIC_SH_MAP150_PIN	32	80000000	rw	
GIC_SH_MAP151_PIN	32	80000000	rw	
GIC_SH_MAP152_PIN	32	80000000	rw	
GIC_SH_MAP153_PIN	32	80000000	rw	
GIC_SH_MAP154_PIN	32	80000000	rw	
GIC_SH_MAP155_PIN	32	80000000	rw	
GIC_SH_MAP156_PIN	32	80000000	rw	
GIC_SH_MAP157_PIN	32	80000000	rw	
GIC_SH_MAP158_PIN	32	80000000	rw	
GIC_SH_MAP159_PIN	32	80000000	rw	
GIC_SH_MAP160_PIN	32	80000000	rw	
GIC_SH_MAP161_PIN	32	80000000	rw	
GIC SH MAP162 PIN	32	80000000	rw	
GIC_SH_MAP163_PIN	32	80000000	rw	
GIC_SH_MAP164_PIN	32	80000000	rw	
GIC_SH_MAP165_PIN	32	80000000		
GIC_SH_MAP166_PIN	32	80000000	rw	
GIC_SH_MAP160_PIN		80000000	rw	
	32		rw	
GIC_SH_MAP168_PIN	32	80000000	rw	
GIC_SH_MAP169_PIN	32	80000000	rw	
GIC_SH_MAP170_PIN	32	80000000	rw	
GIC_SH_MAP171_PIN	32	80000000	rw	
GIC_SH_MAP172_PIN	32	80000000	rw	
GIC_SH_MAP173_PIN	32	80000000	rw	
GIC_SH_MAP174_PIN	32	80000000	rw	
GIC_SH_MAP175_PIN	32	80000000	rw	
GIC_SH_MAP176_PIN	32	80000000	rw	
GIC_SH_MAP177_PIN	32	80000000	rw	
GIC_SH_MAP178_PIN	32	80000000	rw	
GIC_SH_MAP179_PIN	32	80000000	rw	
GIC_SH_MAP180_PIN	32	80000000	rw	
GIC_SH_MAP181_PIN	32	80000000	rw	
GIC_SH_MAP182_PIN	32	80000000	rw	
GIC_SH_MAP183_PIN	32	80000000	+	
GIC_SH_MAP183_PIN	32	80000000	rw	
G10_511_WAF 104_F1N	32	30000000	rw	

		T		1
GIC_SH_MAP185_PIN	32	80000000	rw	
GIC_SH_MAP186_PIN	32	80000000	rw	
GIC_SH_MAP187_PIN	32	80000000	rw	
GIC_SH_MAP188_PIN	32	80000000	rw	
GIC_SH_MAP189_PIN	32	80000000	rw	
GIC_SH_MAP190_PIN	32	80000000	rw	
GIC_SH_MAP191_PIN	32	80000000	rw	
GIC_SH_MAP192_PIN	32	80000000	rw	
GIC_SH_MAP193_PIN	32	80000000	rw	
GIC_SH_MAP194_PIN	32	80000000	rw	
GIC_SH_MAP195_PIN	32	80000000	rw	
GIC_SH_MAP196_PIN	32	80000000	rw	
GIC_SH_MAP197_PIN	32	80000000	rw	
GIC_SH_MAP198_PIN	32	80000000	rw	
GIC_SH_MAP199_PIN	32	80000000	rw	
GIC_SH_MAP200_PIN	32	80000000		
GIC_SH_MAP201_PIN	32	80000000	rw	
			rw	
GIC_SH_MAP202_PIN	32	80000000	rw	
GIC_SH_MAP203_PIN	32	80000000	rw	
GIC_SH_MAP204_PIN	32	80000000	rw	
GIC_SH_MAP205_PIN	32	80000000	rw	
GIC_SH_MAP206_PIN	32	80000000	rw	
GIC_SH_MAP207_PIN	32	80000000	rw	
GIC_SH_MAP208_PIN	32	80000000	rw	
GIC_SH_MAP209_PIN	32	80000000	rw	
GIC_SH_MAP210_PIN	32	80000000	rw	
GIC_SH_MAP211_PIN	32	80000000	rw	
GIC_SH_MAP212_PIN	32	80000000	rw	
GIC_SH_MAP213_PIN	32	80000000	rw	
GIC_SH_MAP214_PIN	32	80000000	rw	
GIC_SH_MAP215_PIN	32	80000000	rw	
GIC_SH_MAP216_PIN	32	80000000	rw	
GIC_SH_MAP217_PIN	32	80000000	rw	
GIC_SH_MAP218_PIN	32	80000000	rw	
GIC_SH_MAP219_PIN	32	80000000	rw	
GIC_SH_MAP220_PIN	32	80000000	rw	
GIC_SH_MAP221_PIN	32	80000000	rw	
GIC SH MAP222 PIN	32	80000000	+	
GIC_SH_MAP223_PIN	32	80000000	rw	
GIC_SH_MAP224_PIN			rw	
	32	80000000	rw	
GIC_SH_MAP225_PIN	32	80000000	rw	
GIC_SH_MAP226_PIN	32	80000000	rw	
GIC_SH_MAP227_PIN	32	80000000	rw	
GIC_SH_MAP228_PIN	32	80000000	rw	
GIC_SH_MAP229_PIN	32	80000000	rw	
GIC_SH_MAP230_PIN	32	80000000	rw	
GIC_SH_MAP231_PIN	32	80000000	rw	
GIC_SH_MAP232_PIN	32	80000000	rw	
GIC_SH_MAP233_PIN	32	80000000	rw	
GIC_SH_MAP234_PIN	32	80000000	rw	
GIC_SH_MAP235_PIN	32	80000000	rw	
GIC_SH_MAP236_PIN	32	80000000	rw	
GIC_SH_MAP237_PIN	32	80000000	rw	
GIC_SH_MAP238_PIN	32	80000000	rw	
GIC_SH_MAP239_PIN	32	80000000	rw	
GIC_SH_MAP240_PIN	32	80000000	rw	
010_011_WITH 240_1 11V	1 02	30000000	1 VV	<u> </u>

	1	T		T
GIC_SH_MAP241_PIN	32	80000000	rw	
GIC_SH_MAP242_PIN	32	80000000	rw	
GIC_SH_MAP243_PIN	32	80000000	rw	
GIC_SH_MAP244_PIN	32	80000000	rw	
GIC_SH_MAP245_PIN	32	80000000	rw	
GIC_SH_MAP246_PIN	32	80000000	rw	
GIC_SH_MAP247_PIN	32	80000000	rw	
GIC_SH_MAP248_PIN	32	80000000	rw	
GIC_SH_MAP249_PIN	32	80000000	rw	
GIC_SH_MAP250_PIN	32	80000000	rw	
GIC_SH_MAP251_PIN	32	80000000	rw	
GIC_SH_MAP252_PIN	32	80000000	rw	
GIC_SH_MAP253_PIN	32	80000000	rw	
GIC_SH_MAP254_PIN	32	80000000	rw	
GIC_SH_MAP255_PIN	32	80000000	rw	
GIC_SH_MAP000_VPE31_0	32	0	+	
GIC_SH_MAP001_VPE31_0	32	0	rw	
	32	-	rw	
GIC_SH_MAP002_VPE31_0		0	rw	
GIC_SH_MAP003_VPE31_0	32	0	rw	
GIC_SH_MAP004_VPE31_0	32	0	rw	
GIC_SH_MAP005_VPE31_0	32	0	rw	
GIC_SH_MAP006_VPE31_0	32	0	rw	
GIC_SH_MAP007_VPE31_0	32	0	rw	
GIC_SH_MAP008_VPE31_0	32	0	rw	
GIC_SH_MAP009_VPE31_0	32	0	rw	
GIC_SH_MAP010_VPE31_0	32	0	rw	
GIC_SH_MAP011_VPE31_0	32	0	rw	
GIC_SH_MAP012_VPE31_0	32	0	rw	
GIC_SH_MAP013_VPE31_0	32	0	rw	
GIC_SH_MAP014_VPE31_0	32	0	rw	
GIC_SH_MAP015_VPE31_0	32	0	rw	
GIC_SH_MAP016_VPE31_0	32	0	rw	
GIC_SH_MAP017_VPE31_0	32	0	rw	
GIC_SH_MAP018_VPE31_0	32	0	rw	
GIC_SH_MAP019_VPE31_0	32	0	rw	
GIC_SH_MAP020_VPE31_0	32	0	rw	
GIC_SH_MAP021_VPE31_0	32	0	+	
GIC_SH_MAP022_VPE31_0	32	0	rw	
GIC_SH_MAP022_VPE31_0	32	0	rw	
		ŭ.	rw	
GIC_SH_MAP024_VPE31_0	32	0	rw	
GIC_SH_MAP025_VPE31_0	32	0	rw	
GIC_SH_MAP026_VPE31_0	32	0	rw	
GIC_SH_MAP027_VPE31_0	32	0	rw	
GIC_SH_MAP028_VPE31_0	32	0	rw	
GIC_SH_MAP029_VPE31_0	32	0	rw	
GIC_SH_MAP030_VPE31_0	32	0	rw	
GIC_SH_MAP031_VPE31_0	32	0	rw	
GIC_SH_MAP032_VPE31_0	32	0	rw	
GIC_SH_MAP033_VPE31_0	32	0	rw	
GIC_SH_MAP034_VPE31_0	32	0	rw	
GIC_SH_MAP035_VPE31_0	32	0	rw	
GIC_SH_MAP036_VPE31_0	32	0	rw	
GIC_SH_MAP037_VPE31_0	32	0	rw	
GIC_SH_MAP038_VPE31_0	32	0	rw	
GIC_SH_MAP039_VPE31_0	32	0	rw	
GIC_SH_MAP040_VPE31_0	32	0	rw	
010_011_WITH 040_V1 E01_0	1 52	J	1 VV	

GIC_SH_MAP041_VPE31_0	32	0	rw	
GIC_SH_MAP042_VPE31_0	32	0	rw	
GIC_SH_MAP043_VPE31_0	32	0	rw	
GIC_SH_MAP044_VPE31_0	32	0	rw	
GIC_SH_MAP045_VPE31_0	32	0	rw	
GIC_SH_MAP046_VPE31_0	32	0	rw	
GIC_SH_MAP047_VPE31_0	32	0	rw	
GIC_SH_MAP048_VPE31_0	32	0	rw	
GIC_SH_MAP049_VPE31_0	32	0	rw	
GIC_SH_MAP050_VPE31_0	32	0	rw	
GIC_SH_MAP051_VPE31_0	32	0	rw	
GIC_SH_MAP052_VPE31_0	32	0	rw	
GIC_SH_MAP053_VPE31_0	32	0	rw	
GIC_SH_MAP054_VPE31_0	32	0	rw	
GIC_SH_MAP055_VPE31_0	32	0	rw	
GIC_SH_MAP056_VPE31_0	32	0	-	
GIC_SH_MAP057_VPE31_0	32	0	rw	
	32	0	rw	
GIC_SH_MAP058_VPE31_0		-	rw	
GIC_SH_MAP059_VPE31_0	32	0	rw	
GIC_SH_MAP060_VPE31_0	32	0	rw	
GIC_SH_MAP061_VPE31_0	32	0	rw	
GIC_SH_MAP062_VPE31_0	32	0	rw	
GIC_SH_MAP063_VPE31_0	32	0	rw	
GIC_SH_MAP064_VPE31_0	32	0	rw	
GIC_SH_MAP065_VPE31_0	32	0	rw	
GIC_SH_MAP066_VPE31_0	32	0	rw	
GIC_SH_MAP067_VPE31_0	32	0	rw	
GIC_SH_MAP068_VPE31_0	32	0	rw	
GIC_SH_MAP069_VPE31_0	32	0	rw	
GIC_SH_MAP070_VPE31_0	32	0	rw	
GIC_SH_MAP071_VPE31_0	32	0	rw	
GIC_SH_MAP072_VPE31_0	32	0	rw	
GIC_SH_MAP073_VPE31_0	32	0	rw	
GIC_SH_MAP074_VPE31_0	32	0	rw	
GIC_SH_MAP075_VPE31_0	32	0	rw	
GIC_SH_MAP076_VPE31_0	32	0	rw	
GIC_SH_MAP077_VPE31_0	32	0	rw	
GIC_SH_MAP078_VPE31_0	32	0	_	
GIC_SH_MAP079_VPE31_0	32	0	rw	
		ű.	rw	
GIC_SH_MAP080_VPE31_0	32	0	rw	
GIC_SH_MAP081_VPE31_0	32	0	rw	
GIC_SH_MAP082_VPE31_0	32	0	rw	
GIC_SH_MAP083_VPE31_0	32	0	rw	
GIC_SH_MAP084_VPE31_0	32	0	rw	
GIC_SH_MAP085_VPE31_0	32	0	rw	
GIC_SH_MAP086_VPE31_0	32	0	rw	
GIC_SH_MAP087_VPE31_0	32	0	rw	
GIC_SH_MAP088_VPE31_0	32	0	rw	
GIC_SH_MAP089_VPE31_0	32	0	rw	
GIC_SH_MAP090_VPE31_0	32	0	rw	
GIC_SH_MAP091_VPE31_0	32	0	rw	
GIC_SH_MAP092_VPE31_0	32	0	rw	
GIC_SH_MAP093_VPE31_0	32	0	rw	
GIC_SH_MAP094_VPE31_0	32	0	rw	
GIC_SH_MAP095_VPE31_0	32	0	rw	
GIC_SH_MAP096_VPE31_0	32	0	rw	
010_011_1111 000_ VI LI01_0	1 52		T 44	

GIC_SH_MAP097_VPE31_0	32	0	rw	
GIC_SH_MAP098_VPE31_0	32	0	rw	
GIC_SH_MAP099_VPE31_0	32	0	rw	
GIC_SH_MAP100_VPE31_0	32	0	rw	
GIC_SH_MAP101_VPE31_0	32	0	rw	
GIC_SH_MAP102_VPE31_0	32	0	rw	
GIC_SH_MAP103_VPE31_0	32	0	rw	
GIC_SH_MAP104_VPE31_0	32	0	rw	
GIC_SH_MAP105_VPE31_0	32	0	rw	
GIC_SH_MAP106_VPE31_0	32	0	rw	
GIC_SH_MAP107_VPE31_0	32	0	rw	
GIC_SH_MAP108_VPE31_0	32	0	rw	
GIC_SH_MAP109_VPE31_0	32	0	rw	
GIC_SH_MAP110_VPE31_0	32	0	rw	
GIC_SH_MAP111_VPE31_0	32	0	rw	
GIC_SH_MAP112_VPE31_0	32	0	rw	
GIC_SH_MAP113_VPE31_0	32	0	rw	
GIC_SH_MAP114_VPE31_0	32	0		
GIC_SH_MAP115_VPE31_0	32	0	rw	
GIC_SH_MAP116_VPE31_0	32	0	rw	
GIC_SH_MAP110_VPE31_0	32	0	rw	
		-	rw	
GIC_SH_MAP118_VPE31_0	32	0	rw	
GIC_SH_MAP119_VPE31_0	32	0	rw	
GIC_SH_MAP120_VPE31_0	32	0	rw	
GIC_SH_MAP121_VPE31_0	32	0	rw	
GIC_SH_MAP122_VPE31_0	32	0	rw	
GIC_SH_MAP123_VPE31_0	32	0	rw	
GIC_SH_MAP124_VPE31_0	32	0	rw	
GIC_SH_MAP125_VPE31_0	32	0	rw	
GIC_SH_MAP126_VPE31_0	32	0	rw	
GIC_SH_MAP127_VPE31_0	32	0	rw	
GIC_SH_MAP128_VPE31_0	32	0	rw	
GIC_SH_MAP129_VPE31_0	32	0	rw	
GIC_SH_MAP130_VPE31_0	32	0	rw	
GIC_SH_MAP131_VPE31_0	32	0	rw	
GIC_SH_MAP132_VPE31_0	32	0	rw	
GIC_SH_MAP133_VPE31_0	32	0	rw	
GIC_SH_MAP134_VPE31_0	32	0	rw	
GIC_SH_MAP135_VPE31_0	32	0	rw	
GIC_SH_MAP136_VPE31_0	32	0	rw	
GIC_SH_MAP137_VPE31_0	32	0	rw	
GIC_SH_MAP138_VPE31_0	32	0	rw	
GIC_SH_MAP139_VPE31_0	32	0	rw	
GIC_SH_MAP140_VPE31_0	32	0	rw	
GIC_SH_MAP141_VPE31_0	32	0	rw	
GIC_SH_MAP142_VPE31_0	32	0		
GIC_SH_MAP143_VPE31_0	32	0	rw	
GIC_SH_MAP143_VPE31_0 GIC_SH_MAP144_VPE31_0	32	0	rw	
	32	0	rw	
GIC_SH_MAP145_VPE31_0		_	rw	
GIC_SH_MAP146_VPE31_0	32	0	rw	
GIC_SH_MAP147_VPE31_0	32	0	rw	
GIC_SH_MAP148_VPE31_0	32	0	rw	
GIC_SH_MAP149_VPE31_0	32	0	rw	
GIC_SH_MAP150_VPE31_0	32	0	rw	
GIC_SH_MAP151_VPE31_0	32	0	rw	
GIC_SH_MAP152_VPE31_0	32	0	rw	

GIC_SH_MAP153_VPE31_0	32	0	rw	
GIC_SH_MAP154_VPE31_0	32	0	rw	
GIC_SH_MAP155_VPE31_0	32	0	rw	
GIC_SH_MAP156_VPE31_0	32	0	rw	
GIC_SH_MAP157_VPE31_0	32	0	rw	
GIC_SH_MAP158_VPE31_0	32	0	rw	
GIC_SH_MAP159_VPE31_0	32	0	rw	
GIC_SH_MAP160_VPE31_0	32	0	rw	
GIC_SH_MAP161_VPE31_0	32	0	rw	
GIC_SH_MAP162_VPE31_0	32	0	rw	
GIC_SH_MAP163_VPE31_0	32	0	rw	
GIC_SH_MAP164_VPE31_0	32	0	rw	
GIC_SH_MAP165_VPE31_0	32	0	rw	
GIC_SH_MAP166_VPE31_0	32	0	rw	
GIC_SH_MAP167_VPE31_0	32	0	rw	
GIC_SH_MAP168_VPE31_0	32	0	rw	
GIC_SH_MAP169_VPE31_0	32	0	+	
GIC_SH_MAP170_VPE31_0	32	0	rw	
	32	0	rw	
GIC_SH_MAP171_VPE31_0		_	rw	
GIC_SH_MAP172_VPE31_0	32	0	rw	
GIC_SH_MAP173_VPE31_0	32	0	rw	
GIC_SH_MAP174_VPE31_0	32	0	rw	
GIC_SH_MAP175_VPE31_0	32	0	rw	
GIC_SH_MAP176_VPE31_0	32	0	rw	
GIC_SH_MAP177_VPE31_0	32	0	rw	
GIC_SH_MAP178_VPE31_0	32	0	rw	
GIC_SH_MAP179_VPE31_0	32	0	rw	
GIC_SH_MAP180_VPE31_0	32	0	rw	
GIC_SH_MAP181_VPE31_0	32	0	rw	
GIC_SH_MAP182_VPE31_0	32	0	rw	
GIC_SH_MAP183_VPE31_0	32	0	rw	
GIC_SH_MAP184_VPE31_0	32	0	rw	
GIC_SH_MAP185_VPE31_0	32	0	rw	
GIC_SH_MAP186_VPE31_0	32	0	rw	
GIC_SH_MAP187_VPE31_0	32	0	rw	
GIC_SH_MAP188_VPE31_0	32	0	rw	
GIC_SH_MAP189_VPE31_0	32	0	rw	
GIC_SH_MAP190_VPE31_0	32	0	rw	
GIC_SH_MAP191_VPE31_0	32	0	rw	
GIC_SH_MAP192_VPE31_0	32	0	rw	
GIC_SH_MAP193_VPE31_0	32	0	rw	
GIC_SH_MAP194_VPE31_0	32	0	rw	
GIC_SH_MAP195_VPE31_0	32	0	rw	
GIC_SH_MAP196_VPE31_0	32	0	rw	
GIC_SH_MAP197_VPE31_0	32	0	+	
GIC_SH_MAP197_VPE31_0	32	0	rw	
GIC_SH_MAP198_VPE31_0 GIC_SH_MAP199_VPE31_0	32	0	rw	
		-	rw	
GIC_SH_MAP200_VPE31_0	32	0	rw	
GIC_SH_MAP201_VPE31_0	32	0	rw	
GIC_SH_MAP202_VPE31_0	32	0	rw	
GIC_SH_MAP203_VPE31_0	32	0	rw	
GIC_SH_MAP204_VPE31_0	32	0	rw	
GIC_SH_MAP205_VPE31_0	32	0	rw	
GIC_SH_MAP206_VPE31_0	32	0	rw	
GIC_SH_MAP207_VPE31_0	32	0	rw	
GIC_SH_MAP208_VPE31_0	32	0	rw	
•	•	•		•

GIC_SH_MAP209_VPE31_0	32	0	rw	
GIC_SH_MAP210_VPE31_0	32	0	rw	
GIC_SH_MAP211_VPE31_0	32	0	rw	
GIC_SH_MAP212_VPE31_0	32	0	rw	
GIC_SH_MAP213_VPE31_0	32	0	rw	
GIC_SH_MAP214_VPE31_0	32	0	rw	
GIC_SH_MAP215_VPE31_0	32	0	rw	
GIC_SH_MAP216_VPE31_0	32	0	rw	
GIC_SH_MAP217_VPE31_0	32	0	rw	
GIC_SH_MAP218_VPE31_0	32	0	rw	
GIC_SH_MAP219_VPE31_0	32	0	rw	
GIC_SH_MAP220_VPE31_0	32	0	rw	
GIC_SH_MAP221_VPE31_0	32	0	rw	
GIC_SH_MAP222_VPE31_0	32	0	rw	
GIC_SH_MAP223_VPE31_0	32	0	rw	
GIC_SH_MAP224_VPE31_0	32	0	rw	
GIC_SH_MAP225_VPE31_0	32	0	rw	
GIC_SH_MAP226_VPE31_0	32	0	rw	
GIC_SH_MAP227_VPE31_0	32	0		
GIC_SH_MAP228_VPE31_0	32	0	rw	
GIC_SH_MAP229_VPE31_0	32	0	rw	
GIC_SH_MAP230_VPE31_0	32	-	rw	
GIC_SH_MAP230_VPE31_0	32	0	rw	
	-	-	rw	
GIC_SH_MAP232_VPE31_0	32	0	rw	
GIC_SH_MAP233_VPE31_0	32	0	rw	
GIC_SH_MAP234_VPE31_0	32	0	rw	
GIC_SH_MAP235_VPE31_0	32	0	rw	
GIC_SH_MAP236_VPE31_0	32	0	rw	
GIC_SH_MAP237_VPE31_0	32	0	rw	
GIC_SH_MAP238_VPE31_0	32	0	rw	
GIC_SH_MAP239_VPE31_0	32	0	rw	
GIC_SH_MAP240_VPE31_0	32	0	rw	
GIC_SH_MAP241_VPE31_0	32	0	rw	
GIC_SH_MAP242_VPE31_0	32	0	rw	
GIC_SH_MAP243_VPE31_0	32	0	rw	
GIC_SH_MAP244_VPE31_0	32	0	rw	
GIC_SH_MAP245_VPE31_0	32	0	rw	
GIC_SH_MAP246_VPE31_0	32	0	rw	
GIC_SH_MAP247_VPE31_0	32	0	rw	
GIC_SH_MAP248_VPE31_0	32	0	rw	
GIC_SH_MAP249_VPE31_0	32	0	rw	
GIC_SH_MAP250_VPE31_0	32	0	rw	
GIC_SH_MAP251_VPE31_0	32	0	rw	
GIC_SH_MAP252_VPE31_0	32	0	rw	
GIC_SH_MAP253_VPE31_0	32	0	rw	
GIC_SH_MAP254_VPE31_0	32	0	rw	
GIC_SH_MAP255_VPE31_0	32	0	rw	
GIC_VB_DINT_SEND	32	0	-w	
GIC_VPE_CTL_L	32	a	rw	
GIC_VPE_PEND_L	32	0	r-	
GIC_VPE_MASK_L	32	7f	r-	
GIC_VPE_RMASK_L	32	0	-w	
GIC_VPE_SMASK_L	32	0	-w	
GIC_VPE_WD_MAP_L	32	40000000	rw	
GIC_VPE_COMPARE_MAP_L	32	0	rw	
GIC_VPE_TIMER_MAP_L	32	80000005	rw	
		2000000	1 11	1

GIG I'DD DD G I LLD I	T 00			
GIC_VPE_FDC_MAP_L	32	8000003e	rw	
GIC_VPE_PERFCTR_MAP_L	32	80000005	rw	
GIC_VPE_SWInt0_MAP_L	32	80000000	rw	
GIC_VPE_SWInt1_MAP_L	32	80000000	rw	
GIC_VPE_OTHER_ADDRESS_L	32	0	rw	
GIC_VPE_IDENT_L	32	0	r-	
GIC_VPE_WD_CONFIG_L	32	0	rw	
GIC_VPE_WD_COUNT_L	32	0	r-	
GIC_VPE_WD_INITIAL_L	32	0	rw	
GIC_VPE_CompareLo_L	32	fffffff	rw	
GIC_VPE_CompareHi_L	32	fffffff	rw	
GIC_VPE_EICSS00_L	32	0	rw	
GIC_VPE_EICSS01_L	32	0	rw	
GIC_VPE_EICSS02_L	32	0	rw	
GIC_VPE_EICSS03_L	32	0	rw	
GIC_VPE_EICSS04_L	32	0	rw	
GIC_VPE_EICSS05_L	32	0	rw	
GIC_VPE_EICSS06_L	32	0	rw	
GIC_VPE_EICSS07_L	32	0	rw	
GIC_VPE_EICSS08_L	32	0	rw	
GIC_VPE_EICSS09_L	32	0	rw	
GIC-VPE-EICSS10-L	32	0	rw	
GIC-VPE-EICSS10-E	32	0	rw	
GIC_VPE_EICSS11_L	32	0	+	
GIC_VPE_EICSS12_L	32	0	rw	
GIC_VPE_EICSS13_L	32	0	rw	
GIC_VPE_EICSS14_L GIC_VPE_EICSS15_L	32	0	rw	
		-	rw	
GIC_VPE_EICSS16_L	32	0	rw	
GIC_VPE_EICSS17_L	32	0	rw	
GIC_VPE_EICSS18_L	32	0	rw	
GIC_VPE_EICSS19_L	32	0	rw	
GIC_VPE_EICSS20_L	32	0	rw	
GIC_VPE_EICSS21_L	32	0	rw	
GIC_VPE_EICSS22_L	32	0	rw	
GIC_VPE_EICSS23_L	32	0	rw	
GIC_VPE_EICSS24_L	32	0	rw	
GIC_VPE_EICSS25_L	32	0	rw	
GIC_VPE_EICSS26_L	32	0	rw	
GIC_VPE_EICSS27_L	32	0	rw	
GIC_VPE_EICSS28_L	32	0	rw	
GIC_VPE_EICSS29_L	32	0	rw	
GIC_VPE_EICSS30_L	32	0	rw	
GIC_VPE_EICSS31_L	32	0	rw	
GIC_VPE_EICSS32_L	32	0	rw	
GIC_VPE_EICSS33_L	32	0	rw	
GIC_VPE_EICSS34_L	32	0	rw	
GIC_VPE_EICSS35_L	32	0	rw	
GIC-VPE_EICSS36_L	32	0	rw	
GIC_VPE_EICSS30_L	32	0	rw	
GIC_VPE_EICSS37_L	32	0	_	+
GIC_VPE_EICSS36_L GIC_VPE_EICSS39_L	32	0	rw	
GIC_VPE_EICSS39_L GIC_VPE_EICSS40_L	32	0	rw	
	_	-	rw	
GIC_VPE_EICSS41_L	32	0	rw	
GIC_VPE_EICSS42_L	32	0	rw	
GIC_VPE_EICSS43_L	32	0	rw	
GIC_VPE_EICSS44_L	32	0	rw	

GIC_VPE_EICSS45_L	32	0	rw	
GIC_VPE_EICSS46_L	32	0	rw	
GIC_VPE_EICSS47_L	32	0	rw	
GIC_VPE_EICSS48_L	32	0	rw	
GIC_VPE_EICSS49_L	32	0	rw	
GIC_VPE_EICSS50_L	32	0	rw	
GIC_VPE_EICSS51_L	32	0	rw	
GIC_VPE_EICSS52_L	32	0	rw	
GIC_VPE_EICSS53_L	32	0	rw	
GIC_VPE_EICSS54_L	32	0	rw	
GIC_VPE_EICSS55_L	32	0	rw	
GIC_VPE_EICSS56_L	32	0	rw	
GIC_VPE_EICSS57_L	32	0	rw	
GIC_VPE_EICSS58_L	32	0	rw	
GIC_VPE_EICSS59_L	32	0	rw	
GIC_VPE_EICSS60_L	32	0	rw	
GIC_VPE_EICSS61_L	32	0	rw	
GIC_VPE_EICSS62_L	32	0	rw	
GIC-VPE-EICSS63-L	32	0	rw	
GIC-VX-DINT-PART-L	32	1	rw	
GIC_Cx_BRK_GROUP_L	32	0	rw	
GIC-VPE-CTL-O	32			
GIC_VPE_CTE_O GIC_VPE_PEND_O	32	a 0	rw	
GIC_VPE_PEND_O GIC_VPE_MASK_O	32	7f	r-	
	_		r-	
GIC_VPE_RMASK_O	32	0	-W	
GIC_VPE_SMASK_O	32	0	-W	
GIC_VPE_WD_MAP_O	32	40000000	rw	
GIC_VPE_COMPARE_MAP_O	32	0	rw	
GIC_VPE_TIMER_MAP_O	32	80000005	rw	
GIC_VPE_FDC_MAP_O	32	8000003e	rw	
GIC_VPE_PERFCTR_MAP_O	32	80000005	rw	
GIC_VPE_SWInt0_MAP_O	32	80000000	rw	
GIC_VPE_SWInt1_MAP_O	32	80000000	rw	
GIC_VPE_OTHER_ADDRESS_O	32	0	rw	
GIC_VPE_IDENT_O	32	0	r-	
GIC_VPE_WD_CONFIG_O	32	0	rw	
GIC_VPE_WD_COUNT_O	32	0	r-	
GIC_VPE_WD_INITIAL_O	32	0	rw	
GIC_VPE_CompareLo_O	32	fffffff	rw	
GIC_VPE_CompareHi_O	32	fffffff	rw	
GIC_VPE_EICSS00_O	32	0	rw	
GIC_VPE_EICSS01_O	32	0	rw	
GIC_VPE_EICSS02_O	32	0	rw	
GIC_VPE_EICSS03_O	32	0	rw	
GIC_VPE_EICSS04_O	32	0	rw	
GIC_VPE_EICSS05_O	32	0	rw	
GIC_VPE_EICSS06_O	32	0	rw	
GIC_VPE_EICSS07_O	32	0	rw	
GIC_VPE_EICSS08_O	32	0	rw	
GIC_VPE_EICSS09_O	32	0		
GIC_VPE_EICSS09_O	32	0	rw	
GIC_VPE_EICSS10_O	32	0	rw	
GIC_VPE_EICSS11_O GIC_VPE_EICSS12_O			rw	
	32	0	rw	
GIC_VPE_EICSS13_O	32	0	rw	
GIC_VPE_EICSS14_O	32	0	rw	
GIC_VPE_EICSS15_O	32	0	rw	

GIC_VPE_EICSS16_O	32	0	2277	
GIC-VPE-EICSS10-O	32	0	rw	
GIC-VPE-EICSS17-O	32	0	rw	
GIC_VPE_EICSS18_O	32	0	rw	
GIC_VPE_EICSS19_O	32	0	rw	
GIC_VPE_EICSS20_O	32	0	rw	
	32	0	rw	
GIC_VPE_EICSS22_O		-	rw	
GIC_VPE_EICSS23_O	32	0	rw	
GIC_VPE_EICSS24_O	32	0	rw	
GIC_VPE_EICSS25_O	32	0	rw	
GIC_VPE_EICSS26_O	32	0	rw	
GIC_VPE_EICSS27_O	32	0	rw	
GIC_VPE_EICSS28_O	32	0	rw	
GIC_VPE_EICSS29_O	32	0	rw	
GIC_VPE_EICSS30_O	32	0	rw	
GIC_VPE_EICSS31_O	32	0	rw	
GIC_VPE_EICSS32_O	32	0	rw	
GIC_VPE_EICSS33_O	32	0	rw	
GIC_VPE_EICSS34_O	32	0	rw	
GIC_VPE_EICSS35_O	32	0	rw	
GIC_VPE_EICSS36_O	32	0	rw	
GIC_VPE_EICSS37_O	32	0	rw	
GIC_VPE_EICSS38_O	32	0	rw	
GIC_VPE_EICSS39_O	32	0	rw	
GIC_VPE_EICSS40_O	32	0	rw	
GIC_VPE_EICSS41_O	32	0	rw	
GIC_VPE_EICSS42_O	32	0	rw	
GIC_VPE_EICSS43_O	32	0	rw	
GIC_VPE_EICSS44_O	32	0	rw	
GIC_VPE_EICSS45_O	32	0	rw	
GIC_VPE_EICSS46_O	32	0	rw	
GIC_VPE_EICSS47_O	32	0	rw	
GIC_VPE_EICSS48_O	32	0	rw	
GIC_VPE_EICSS49_O	32	0	rw	
GIC_VPE_EICSS50_O	32	0	rw	
GIC_VPE_EICSS51_O	32	0	rw	
GIC_VPE_EICSS52_O	32	0	rw	
GIC_VPE_EICSS53_O	32	0	rw	
GIC_VPE_EICSS54_O	32	0	rw	
GIC_VPE_EICSS55_O	32	0	rw	
GIC_VPE_EICSS56_O	32	0	rw	
GIC_VPE_EICSS57_O	32	0	rw	
GIC_VPE_EICSS58_O	32	0	rw	
GIC_VPE_EICSS59_O	32	0	rw	
GIC_VPE_EICSS60_O	32	0	rw	
GIC_VPE_EICSS61_O	32	0	rw	
GIC_VPE_EICSS01_O	32	0	rw	
GIC_VPE_EICSS02_O GIC_VPE_EICSS63_O	32	0		
GIC_VFE_EICSS05_O GIC_Vx_DINT_PART_O	32	1	rw	
GIC_Cx_BRK_GROUP_O	32	0	rw	
GIC_Cx_BRK_GROUP_O GIC_CounterLoUser	32	0	rw	
GIC_CounterLoUser GIC_CounterHiUser	32	0	r-	
G1C_Countern1User	32	U	r-	

Table 13.4: Registers at level 3, type:VPE group:CMP_GIC

13.4 Level 4: TC

13.4.1 Core

Registers at level:4, type:TC group:Core

Name	Bits	Initial-Hex	RW	Description
zero	32	0	r-	constant zero
at	32	0	rw	
v0	32	0	rw	
v1	32	0	rw	
a0	32	0	rw	
a1	32	0	rw	
a2	32	0	rw	
a3	32	0	rw	
t0	32	0	rw	
t1	32	0	rw	
t2	32	0	rw	
t3	32	0	rw	
t4	32	0	rw	
t5	32	0	rw	
t6	32	0	rw	
t7	32	0	rw	
s0	32	0	rw	
s1	32	0	rw	
s2	32	0	rw	
s3	32	0	rw	
s4	32	0	rw	
s5	32	0	rw	
s6	32	0	rw	
s7	32	0	rw	
t8	32	0	rw	
t9	32	0	rw	
k0	32	0	rw	
k1	32	0	rw	
gp	32	0	rw	
$_{\mathrm{sp}}$	32	0	rw	stack pointer
s8	32	0	rw	frame pointer
ra	32	0	rw	
pc	32	bfc00000	rw	program counter

Table 13.5: Registers at level 4, type:TC group:Core

13.4.2 DSP

Registers at level:4, type:TC group:DSP

Name	Bits	Initial-Hex	RW	Description
lo	32	0	rw	
hi	32	0	rw	
lo1	32	0	rw	
hi1	32	0	rw	
lo2	32	0	rw	
hi2	32	0	rw	
lo3	32	0	rw	
hi3	32	0	rw	

dspctl	32	0	rw	DSP control

Table 13.6: Registers at level 4, type:TC group:DSP

13.4.3 COP0

Registers at level:4, type:TC group:COP0

Name	Bits	Initial-Hex	RW	Description
sr	32	400004	rw	CP0 register 12/0 (status)
bad	32	0	rw	CP0 register 8/0 (badvaaddr)
cause	32	0	rw	CP0 register 13/0 (cause)
index	32	0	rw	CP0 register 0/0
mvpcontrol	32	0	rw	CP0 register 0/1
mvpconf0	32	88008401	rw	CP0 register 0/2
mvpconf1	32	0	rw	CP0 register 0/3
random	32	0	rw	CP0 register 1/0
vpecontrol	32	0	rw	CP0 register 1/1
vpeconf0	32	80000003	rw	CP0 register 1/2
vpeconf1	32	0	rw	CP0 register 1/3
yqmask	32	0	rw	CP0 register 1/4
vpeschedule	32	0	rw	CP0 register 1/5
vpeschefback	32	0	rw	CP0 register 1/6
vpeopt	32	0	rw	CP0 register 1/7
entrylo0	32	0	rw	CP0 register 2/0
tcstatus	32	2000	rw	CP0 register 2/1
tcbind	32	0	rw	CP0 register 2/2
tcrestart	32	0	rw	CP0 register 2/3
tchalt	32	0	rw	CP0 register 2/4
tccontext	32	0	rw	CP0 register 2/5
tcschedule	32	0	rw	CP0 register 2/6
tcschefback	32	0	rw	CP0 register 2/7
entrylo1	32	0	rw	CP0 register 3/0
tcopt	32	0	rw	CP0 register 3/7
context	32	0	rw	CP0 register 4/0
userlocal	32	0	rw	CP0 register 4/2
pagemask	32	0	rw	CP0 register 5/0
wired	32	0	rw	CP0 register 6/0
srsconf0	32	3ffffff	rw	CP0 register 6/1
hwrena	32	0	rw	CP0 register 7/0
badvaddr	32	0	rw	CP0 register 8/0
count	32	0	rw	CP0 register 9/0
entryhi	32	0	rw	CP0 register 10/0
compare	32	0	rw	CP0 register 11/0
status	32	400004	rw	CP0 register 12/0
intctl	32	e0000000	rw	CP0 register 12/1
srsctl	32	0	rw	CP0 register 12/2
srsmap	32	0	rw	CP0 register 12/3
epc	32	0	rw	CP0 register 14/0
prid	32	19900	rw	CP0 register 15/0
ebase	32	80000000	rw	CP0 register 15/1
cmgcrbase	32	1fbf800	rw	CP0 register 15/3
config	32	80048482	rw	CP0 register 16/0
config1	32	9e231186	rw	CP0 register 16/1
config2	32	80000000	rw	CP0 register 16/2
config3	32	20002424	rw	CP0 register 16/3

config7	32	80080100	rw	CP0 register 16/7
lladdr	32	0	rw	CP0 register 17/0
debug	32	2028000	rw	CP0 register 23/0
depc	32	0	rw	CP0 register 24/0
errctl	32	0	rw	CP0 register 26/0
itaglo	32	0	rw	CP0 register 28/0
idatalo	32	0	rw	CP0 register 28/1
dtaglo	32	0	rw	CP0 register 28/2
ddatalo	32	0	rw	CP0 register 28/3
l23taglo	32	0	rw	CP0 register 28/4
l23datalo	32	0	rw	CP0 register 28/5
itaghi	32	0	rw	CP0 register 29/0
idatahi	32	0	rw	CP0 register 29/1
dtaghi	32	0	rw	CP0 register 29/2
l23datahi	32	0	rw	CP0 register 29/5
errorepc	32	0	rw	CP0 register 30/0
desave	32	0	rw	CP0 register 31/0

Table 13.7: Registers at level 4, type:TC group:COP0

13.4.4 CMP_GCR

Registers at level:4, type:TC group:CMP_GCR

Name	Bits	Initial-Hex	RW	Description
GCR_CONFIG	32	3	r-	
GCR_BASE	32	1fbf8000	rw	
GCR_CONTROL	32	10001	rw	
GCR_ACCESS	32	ff	rw	
GCR_REV	32	0	r-	
GCR_ERROR_MASK	32	0	rw	
GCR_ERROR_CAUSE	32	0	rw	
GCR_ERROR_ADDR	32	0	rw	
GCR_ERROR_MULT	32	0	rw	
GCR_GIC_BASE	32	0	rw	
GCR_CPC_BASE	32	0	rw	
GCR_GIC_STATUS	32	1	r-	
GCR_CACHE_REV	32	0	r-	
GCR_CPC_STATUS	32	1	r-	
GCR_IOCU1_REV	32	0	r-	
GCR_CL_RESET_RELEASE_L	32	0	-w	
GCR_CL_COHERENCE_L	32	0	rw	
GCR_CL_CONFIG_L	32	1	r-	
GCR_CL_OTHER_L	32	0	rw	
GCR_CL_RESET_BASE_L	32	bfc00000	rw	
GCR_CL_ID_L	32	0	r-	
GCR_CL_RESET_RELEASE_O	32	0	-w	
GCR_CL_COHERENCE_O	32	0	rw	
GCR_CL_CONFIG_O	32	1	r-	
GCR_CL_OTHER_O	32	0	rw	
GCR_CL_RESET_BASE_O	32	bfc00000	rw	
GCR_CL_ID_O	32	0	r-	

Table 13.8: Registers at level 4, type:TC group:CMP_GCR

13.4.5 CMP_CPC

Registers at level:4, type:TC group:CMP_CPC

Name	Bits	Initial-Hex	RW	Description
CPC_ACCESS	32	ff	rw	
CPC_SEQDEL	32	0	rw	
CPC_RAIL	32	0	rw	
CPC_RESETLEN	32	0	rw	
CPC_REVISION	32	0	r-	
CPC_CMD_L	32	0	rw	
CPC_STAT_CONF_L	32	380200	rw	
CPC_OTHER_L	32	0	rw	
CPC_CMD_O	32	0	rw	
CPC_STAT_CONF_O	32	380200	rw	
CPC_OTHER_O	32	0	rw	

Table 13.9: Registers at level 4, type:TC group:CMP_CPC

13.4.6 CMP_GIC

Registers at level:4, type:TC group:CMP_GIC

Name	Bits	Initial-Hex	RW	Description
GIC_SH_CONFIG	32	8040007	rw	-
GIC_CounterLo	32	0	rw	
GIC_CounterHi	32	0	rw	
GIC_SH_REVISION	32	0	r-	
GIC_SH_POL31_0	32	0	rw	
GIC_SH_POL63_32	32	0	rw	
GIC_SH_POL95_64	32	0	rw	
GIC_SH_POL127_96	32	0	rw	
GIC_SH_POL159_128	32	0	rw	
GIC_SH_POL191_160	32	0	rw	
GIC_SH_POL223_192	32	0	rw	
GIC_SH_POL255_224	32	0	rw	
GIC_SH_TRIG31_0	32	0	rw	
GIC_SH_TRIG63_32	32	0	rw	
GIC_SH_TRIG95_64	32	0	rw	
GIC_SH_TRIG127_96	32	0	rw	
GIC_SH_TRIG159_128	32	0	rw	
GIC_SH_TRIG191_160	32	0	rw	
GIC_SH_TRIG223_192	32	0	rw	
GIC_SH_TRIG255_224	32	0	rw	
GIC_SH_DUAL31_0	32	0	rw	
GIC_SH_DUAL63_32	32	0	rw	
GIC_SH_DUAL95_64	32	0	rw	
GIC_SH_DUAL127_96	32	0	rw	
GIC_SH_DUAL159_128	32	0	rw	
GIC_SH_DUAL191_160	32	0	rw	
GIC_SH_DUAL223_192	32	0	rw	
GIC_SH_DUAL255_224	32	0	rw	
GIC_SH_WEDGE	32	0	-w	
GIC_SH_RMASK31_0	32	0	-w	
GIC_SH_RMASK63_32	32	0	-w	
GIC_SH_RMASK95_64	32	0	-w	

		T		T
GIC_SH_RMASK127_96	32	0	-w	
GIC_SH_RMASK159_128	32	0	-w	
GIC_SH_RMASK191_160	32	0	-w	
GIC_SH_RMASK223_192	32	0	-w	
GIC_SH_RMASK255_224	32	0	-w	
GIC_SH_SMASK31_0	32	0	-w	
GIC_SH_SMASK63_32	32	0	-w	
GIC_SH_SMASK95_64	32	0	-w	
GIC_SH_SMASK127_96	32	0	-w	
GIC_SH_SMASK159_128	32	0	-w	
GIC_SH_SMASK191_160	32	0	-w	
GIC_SH_SMASK223_192	32	0	-w	
GIC_SH_SMASK255_224	32	0	-w	
GIC_SH_MASK31_0	32	0	r-	
GIC_SH_MASK63_32	32	0	r-	
GIC_SH_MASK95_64	32	0	+	
GIC_SH_MASK127_96	32	0	r-	
GIC_SH_MASK159_128	32		r-	
		0	r-	
GIC_SH_MASK191_160	32	0	r-	
GIC_SH_MASK223_192	32	0	r-	
GIC_SH_MASK255_224	32	0	r-	
GIC_SH_PEND31_0	32	0	r-	
GIC_SH_PEND63_32	32	0	r-	
GIC_SH_PEND95_64	32	0	r-	
GIC_SH_PEND127_96	32	0	r-	
GIC_SH_PEND159_128	32	0	r-	
GIC_SH_PEND191_160	32	0	r-	
GIC_SH_PEND223_192	32	0	r-	
GIC_SH_PEND255_224	32	0	r-	
GIC_SH_MAP000_PIN	32	80000000	rw	
GIC_SH_MAP001_PIN	32	80000000	rw	
GIC_SH_MAP002_PIN	32	80000000	rw	
GIC_SH_MAP003_PIN	32	80000000	rw	
GIC_SH_MAP004_PIN	32	80000000	rw	
GIC_SH_MAP005_PIN	32	80000000	rw	
GIC_SH_MAP006_PIN	32	80000000	rw	
GIC_SH_MAP007_PIN	32	80000000	+	
GIC_SH_MAP008_PIN	32		rw	
GIC_SH_MAP009_PIN	_	80000000 80000000	rw	
	32		rw	
GIC_SH_MAP010_PIN	32	80000000	rw	
GIC_SH_MAP011_PIN	32	80000000	rw	
GIC_SH_MAP012_PIN	32	80000000	rw	
GIC_SH_MAP013_PIN	32	80000000	rw	
GIC_SH_MAP014_PIN	32	80000000	rw	
GIC_SH_MAP015_PIN	32	80000000	rw	
GIC_SH_MAP016_PIN	32	80000000	rw	
GIC_SH_MAP017_PIN	32	80000000	rw	
GIC_SH_MAP018_PIN	32	80000000	rw	
GIC_SH_MAP019_PIN	32	80000000	rw	
GIC_SH_MAP020_PIN	32	80000000	rw	
GIC_SH_MAP021_PIN	32	80000000	rw	
GIC_SH_MAP022_PIN	32	80000000	rw	
GIC_SH_MAP023_PIN	32	80000000	rw	
GIC_SH_MAP024_PIN	32	80000000	rw	
GIC_SH_MAP025_PIN	32	80000000	+	
GIC_SH_MAP026_PIN	32	80000000	rw	
GIO_DII_IVIAI UZU_F IIV	192	30000000	rw	

				T
GIC_SH_MAP027_PIN	32	80000000	rw	
GIC_SH_MAP028_PIN	32	80000000	rw	
GIC_SH_MAP029_PIN	32	80000000	rw	
GIC_SH_MAP030_PIN	32	80000000	rw	
GIC_SH_MAP031_PIN	32	80000000	rw	
GIC_SH_MAP032_PIN	32	80000000	rw	
GIC_SH_MAP033_PIN	32	80000000	rw	
GIC_SH_MAP034_PIN	32	80000000	rw	
GIC_SH_MAP035_PIN	32	80000000	rw	
GIC_SH_MAP036_PIN	32	80000000	rw	
GIC_SH_MAP037_PIN	32	80000000	rw	
GIC_SH_MAP038_PIN	32	80000000	rw	
GIC_SH_MAP039_PIN	32	80000000	rw	
GIC_SH_MAP040_PIN	32	80000000	rw	
GIC_SH_MAP041_PIN	32	80000000	rw	
GIC_SH_MAP042_PIN	32	80000000	rw	
GIC_SH_MAP043_PIN	32	80000000	rw	
GIC_SH_MAP044_PIN	32	80000000	rw	
GIC_SH_MAP045_PIN	32	80000000	rw	
GIC_SH_MAP046_PIN	32	80000000	rw	
GIC_SH_MAP047_PIN	32	80000000	rw	
GIC_SH_MAP048_PIN	32	80000000	rw	
GIC_SH_MAP049_PIN	32	80000000	rw	
GIC_SH_MAP050_PIN	32	80000000	rw	
GIC_SH_MAP051_PIN	32	80000000	rw	
GIC_SH_MAP052_PIN	32	80000000	rw	
GIC_SH_MAP053_PIN	32	80000000	rw	
GIC_SH_MAP054_PIN	32	80000000	rw	
GIC_SH_MAP055_PIN	32	80000000	rw	
GIC_SH_MAP056_PIN	32	80000000	rw	
GIC_SH_MAP057_PIN	32	80000000	rw	
GIC_SH_MAP058_PIN	32	80000000	rw	
GIC_SH_MAP059_PIN	32	80000000	rw	
GIC_SH_MAP060_PIN	32	80000000	rw	
GIC_SH_MAP061_PIN	32	80000000	rw	
GIC_SH_MAP062_PIN	32	80000000	rw	
GIC_SH_MAP063_PIN	32	80000000	rw	
GIC_SH_MAP064_PIN	32	80000000	rw	
GIC_SH_MAP065_PIN	32	80000000	rw	
GIC_SH_MAP066_PIN	32	80000000	+	
GIC_SH_MAP065_PIN GIC_SH_MAP067_PIN	32	80000000	rw	
GIC_SH_MAP067_PIN GIC_SH_MAP068_PIN	32	80000000	rw	
			rw	
GIC_SH_MAP069_PIN	32	80000000 80000000	rw	
GIC_SH_MAP070_PIN GIC_SH_MAP071_PIN			rw	
GIC_SH_MAP071_PIN GIC_SH_MAP072_PIN	32	80000000	rw	
	32	80000000	rw	
GIC_SH_MAP073_PIN	32	80000000	rw	
GIC_SH_MAP074_PIN	32	80000000	rw	
GIC_SH_MAP075_PIN	32	80000000	rw	
GIC_SH_MAP076_PIN	32	80000000	rw	
GIC_SH_MAP077_PIN	32	80000000	rw	
GIC_SH_MAP078_PIN	32	80000000	rw	
GIC_SH_MAP079_PIN	32	80000000	rw	
GIC_SH_MAP080_PIN	32	80000000	rw	
GIC_SH_MAP081_PIN	32	80000000	rw	
GIC_SH_MAP082_PIN	32	80000000	rw	

		Г		T
GIC_SH_MAP083_PIN	32	80000000	rw	
GIC_SH_MAP084_PIN	32	80000000	rw	
GIC_SH_MAP085_PIN	32	80000000	rw	
GIC_SH_MAP086_PIN	32	80000000	rw	
GIC_SH_MAP087_PIN	32	80000000	rw	
GIC_SH_MAP088_PIN	32	80000000	rw	
GIC_SH_MAP089_PIN	32	80000000	rw	
GIC_SH_MAP090_PIN	32	80000000	rw	
GIC_SH_MAP091_PIN	32	80000000	rw	
GIC_SH_MAP092_PIN	32	80000000	rw	
GIC_SH_MAP093_PIN	32	80000000	rw	
GIC_SH_MAP094_PIN	32	80000000	rw	
GIC_SH_MAP095_PIN	32	80000000	rw	
GIC_SH_MAP096_PIN	32	80000000	rw	
GIC_SH_MAP097_PIN	32	80000000	rw	
GIC_SH_MAP098_PIN	32	80000000	rw	
GIC_SH_MAP099_PIN	32	80000000	rw	
GIC_SH_MAP100_PIN	32	80000000	rw	
GIC_SH_MAP101_PIN	32	80000000	rw	
GIC_SH_MAP102_PIN	32	80000000	rw	
GIC_SH_MAP103_PIN	32	80000000	rw	
GIC_SH_MAP104_PIN	32	80000000	rw	
GIC_SH_MAP105_PIN	32	80000000	rw	
GIC_SH_MAP106_PIN	32	80000000	rw	
GIC_SH_MAP107_PIN	32	80000000	rw	
GIC_SH_MAP108_PIN	32	80000000	rw	
GIC_SH_MAP109_PIN	32	80000000	rw	
GIC_SH_MAP110_PIN	32	80000000	rw	
GIC_SH_MAP111_PIN	32	80000000	rw	
GIC_SH_MAP112_PIN	32	80000000	rw	
GIC_SH_MAP113_PIN	32	80000000	rw	
GIC_SH_MAP114_PIN	32	80000000	rw	
GIC_SH_MAP115_PIN	32	80000000	rw	
GIC_SH_MAP116_PIN	32	80000000	rw	
GIC_SH_MAP117_PIN	32	80000000	rw	
GIC_SH_MAP118_PIN	32	8000000		
GIC_SH_MAP119_PIN	32	8000000	rw	
GIC_SH_MAP120_PIN	32	80000000	rw	
GIC_SH_MAP121_PIN	32	8000000	rw	
GIC_SH_MAP122_PIN	32	8000000	rw	
GIC_SH_MAP123_PIN	32	80000000	rw	
GIC_SH_MAP123_PIN GIC_SH_MAP124_PIN	32	80000000	rw	
			rw	
GIC_SH_MAP125_PIN GIC_SH_MAP126_PIN	32	80000000	rw	
	32	80000000	rw	
GIC_SH_MAP127_PIN GIC_SH_MAP128_PIN		80000000	rw	
	32	80000000	rw	
GIC_SH_MAP129_PIN	32	80000000	rw	
GIC_SH_MAP130_PIN	32	80000000	rw	
GIC_SH_MAP131_PIN	32	80000000	rw	
GIC_SH_MAP132_PIN	32	80000000	rw	
GIC_SH_MAP133_PIN	32	80000000	rw	
GIC_SH_MAP134_PIN	32	80000000	rw	
GIC_SH_MAP135_PIN	32	80000000	rw	
GIC_SH_MAP136_PIN	32	80000000	rw	
GIC_SH_MAP137_PIN	32	80000000	rw	
GIC_SH_MAP138_PIN	32	80000000	rw	

GIC_SH_MAP139_PIN	32	80000000	rw	
GIC_SH_MAP140_PIN	32	80000000	rw	
GIC_SH_MAP141_PIN	32	80000000	rw	
GIC_SH_MAP142_PIN	32	80000000	rw	
GIC_SH_MAP143_PIN	32	80000000	rw	
GIC_SH_MAP144_PIN	32	80000000	rw	
GIC_SH_MAP145_PIN	32	80000000	rw	
GIC_SH_MAP146_PIN	32	80000000	rw	
GIC_SH_MAP147_PIN	32	80000000	rw	
GIC_SH_MAP148_PIN	32	80000000	rw	
GIC_SH_MAP149_PIN	32	80000000	rw	
GIC_SH_MAP150_PIN	32	80000000	rw	
GIC_SH_MAP151_PIN	32	80000000	rw	
GIC_SH_MAP152_PIN	32	80000000	rw	
GIC_SH_MAP153_PIN	32	80000000	rw	
GIC_SH_MAP154_PIN	32	80000000	rw	
GIC_SH_MAP155_PIN	32	80000000	rw	
GIC_SH_MAP156_PIN	32	80000000	rw	
GIC_SH_MAP157_PIN	32	80000000	rw	
GIC_SH_MAP158_PIN	32	80000000	rw	
GIC_SH_MAP159_PIN	32	80000000	rw	
GIC_SH_MAP160_PIN	32	80000000	rw	
GIC_SH_MAP161_PIN	32	80000000	rw	
GIC_SH_MAP162_PIN	32	80000000	rw	
GIC_SH_MAP163_PIN	32	80000000	rw	
GIC_SH_MAP164_PIN	32	80000000	rw	
GIC_SH_MAP165_PIN	32	80000000	rw	
GIC_SH_MAP166_PIN	32	80000000	rw	
GIC_SH_MAP167_PIN	32	80000000	rw	
GIC_SH_MAP168_PIN	32	80000000	rw	
GIC_SH_MAP169_PIN	32	80000000	rw	
GIC_SH_MAP170_PIN	32	80000000	rw	
GIC_SH_MAP171_PIN	32	80000000	rw	
GIC_SH_MAP172_PIN	32	80000000	rw	
GIC_SH_MAP173_PIN	32	80000000	rw	
GIC_SH_MAP174_PIN	32	80000000		
GIC_SH_MAP175_PIN	32	80000000	rw	
GIC_SH_MAP176_PIN	32	80000000	rw	
GIC_SH_MAP177_PIN	32	80000000	rw	
			rw	
GIC_SH_MAP178_PIN	32	80000000	rw	
GIC_SH_MAP179_PIN	32	80000000	rw	
GIC_SH_MAP180_PIN		80000000	rw	
GIC_SH_MAP181_PIN	32	80000000	rw	
GIC_SH_MAP182_PIN	32	80000000	rw	
GIC_SH_MAP183_PIN	32	80000000	rw	
GIC_SH_MAP184_PIN	32	80000000	rw	
GIC_SH_MAP185_PIN	32	80000000	rw	
GIC_SH_MAP186_PIN	32	80000000	rw	
GIC_SH_MAP187_PIN	32	80000000	rw	
GIC_SH_MAP188_PIN	32	80000000	rw	
GIC_SH_MAP189_PIN	32	80000000	rw	
GIC_SH_MAP190_PIN	32	80000000	rw	
GIC_SH_MAP191_PIN	32	80000000	rw	
GIC_SH_MAP192_PIN	32	80000000	rw	
GIC_SH_MAP193_PIN	32	80000000	rw	
GIC_SH_MAP194_PIN	32	80000000	rw	

		T		
GIC_SH_MAP195_PIN	32	80000000	rw	
GIC_SH_MAP196_PIN	32	80000000	rw	
GIC_SH_MAP197_PIN	32	80000000	rw	
GIC_SH_MAP198_PIN	32	80000000	rw	
GIC_SH_MAP199_PIN	32	80000000	rw	
GIC_SH_MAP200_PIN	32	80000000	rw	
GIC_SH_MAP201_PIN	32	80000000	rw	
GIC_SH_MAP202_PIN	32	80000000	rw	
GIC_SH_MAP203_PIN	32	80000000	rw	
GIC_SH_MAP204_PIN	32	80000000	rw	
GIC_SH_MAP205_PIN	32	80000000	rw	
GIC_SH_MAP206_PIN	32	80000000	rw	
GIC_SH_MAP207_PIN	32	80000000	rw	
GIC_SH_MAP208_PIN	32	80000000	rw	
GIC_SH_MAP209_PIN	32	80000000	rw	
GIC_SH_MAP210_PIN	32	80000000	+	
GIC SH MAP211 PIN	32	80000000	rw	
0.10 0.010 1.1111		8000000	rw	
GIC_SH_MAP212_PIN	32		rw	
GIC_SH_MAP213_PIN	32	80000000	rw	
GIC_SH_MAP214_PIN	32	80000000	rw	
GIC_SH_MAP215_PIN	32	80000000	rw	
GIC_SH_MAP216_PIN	32	80000000	rw	
GIC_SH_MAP217_PIN	32	80000000	rw	
GIC_SH_MAP218_PIN	32	80000000	rw	
GIC_SH_MAP219_PIN	32	80000000	rw	
GIC_SH_MAP220_PIN	32	80000000	rw	
GIC_SH_MAP221_PIN	32	80000000	rw	
GIC_SH_MAP222_PIN	32	80000000	rw	
GIC_SH_MAP223_PIN	32	80000000	rw	
GIC_SH_MAP224_PIN	32	80000000	rw	
GIC_SH_MAP225_PIN	32	80000000	rw	
GIC_SH_MAP226_PIN	32	80000000	rw	
GIC_SH_MAP227_PIN	32	80000000	rw	
GIC_SH_MAP228_PIN	32	80000000	rw	
GIC_SH_MAP229_PIN	32	80000000	rw	
GIC_SH_MAP230_PIN	32	80000000	rw	
GIC_SH_MAP231_PIN	32	80000000	rw	
GIC_SH_MAP232_PIN	32	80000000	+	
GIC_SH_MAP233_PIN	32	80000000	rw	
			rw	
GIC_SH_MAP234_PIN	32	80000000	rw	
GIC_SH_MAP235_PIN	32	80000000	rw	
GIC_SH_MAP236_PIN	32	80000000	rw	
GIC_SH_MAP237_PIN	32	80000000	rw	
GIC_SH_MAP238_PIN	32	80000000	rw	
GIC_SH_MAP239_PIN	32	80000000	rw	
GIC_SH_MAP240_PIN	32	80000000	rw	
GIC_SH_MAP241_PIN	32	80000000	rw	
GIC_SH_MAP242_PIN	32	80000000	rw	
GIC_SH_MAP243_PIN	32	80000000	rw	
GIC_SH_MAP244_PIN	32	80000000	rw	
GIC_SH_MAP245_PIN	32	80000000	rw	
GIC_SH_MAP246_PIN	32	80000000	rw	
GIC_SH_MAP247_PIN	32	80000000	rw	
GIC_SH_MAP248_PIN	32	80000000	rw	
GIC_SH_MAP249_PIN	32	80000000	rw	
GIC_SH_MAP250_PIN	32	80000000	rw	
CICLOII IVIII 200 I IIV	1 92	00000000	T 4A	

Gra grand bank prov	1 00			т
GIC_SH_MAP251_PIN	32	80000000	rw	
GIC_SH_MAP252_PIN	32	80000000	rw	
GIC_SH_MAP253_PIN	32	80000000	rw	
GIC_SH_MAP254_PIN	32	80000000	rw	
GIC_SH_MAP255_PIN	32	80000000	rw	
GIC_SH_MAP000_VPE31_0	32	0	rw	
GIC_SH_MAP001_VPE31_0	32	0	rw	
GIC_SH_MAP002_VPE31_0	32	0	rw	
GIC_SH_MAP003_VPE31_0	32	0	rw	
GIC_SH_MAP004_VPE31_0	32	0	rw	
GIC_SH_MAP005_VPE31_0	32	0	rw	
GIC_SH_MAP006_VPE31_0	32	0	rw	
GIC_SH_MAP007_VPE31_0	32	0	rw	
GIC_SH_MAP008_VPE31_0	32	0	rw	
GIC_SH_MAP009_VPE31_0	32	0	rw	
GIC_SH_MAP010_VPE31_0	32	0	rw	
GIC_SH_MAP011_VPE31_0	32	0	rw	
GIC_SH_MAP012_VPE31_0	32	0	rw	
GIC_SH_MAP013_VPE31_0	32	0	rw	
GIC_SH_MAP014_VPE31_0	32	0	rw	
GIC_SH_MAP015_VPE31_0	32	0		
GIC_SH_MAP016_VPE31_0	32	0	rw	
GIC_SH_MAP010_VPE31_0	32	0	rw	
		-	rw	
GIC_SH_MAP018_VPE31_0	32	0	rw	
GIC_SH_MAP019_VPE31_0	32	0	rw	
GIC_SH_MAP020_VPE31_0	32	0	rw	
GIC_SH_MAP021_VPE31_0	32	0	rw	
GIC_SH_MAP022_VPE31_0	32	0	rw	
GIC_SH_MAP023_VPE31_0	32	0	rw	
GIC_SH_MAP024_VPE31_0	32	0	rw	
GIC_SH_MAP025_VPE31_0	32	0	rw	
GIC_SH_MAP026_VPE31_0	32	0	rw	
GIC_SH_MAP027_VPE31_0	32	0	rw	
GIC_SH_MAP028_VPE31_0	32	0	rw	
GIC_SH_MAP029_VPE31_0	32	0	rw	
GIC_SH_MAP030_VPE31_0	32	0	rw	
GIC_SH_MAP031_VPE31_0	32	0	rw	
GIC_SH_MAP032_VPE31_0	32	0	rw	
GIC_SH_MAP033_VPE31_0	32	0	rw	
GIC_SH_MAP034_VPE31_0	32	0	rw	
GIC_SH_MAP035_VPE31_0	32	0	rw	
GIC_SH_MAP036_VPE31_0	32	0	rw	
GIC_SH_MAP037_VPE31_0	32	0		
GIC_SH_MAP038_VPE31_0	32	0	rw	
GIC_SH_MAP038_VPE31_0 GIC_SH_MAP039_VPE31_0	32	0	rw	
GIC_SH_MAP039_VPE31_0 GIC_SH_MAP040_VPE31_0	32	0	rw	
		-	rw	
GIC_SH_MAP041_VPE31_0	32	0	rw	
GIC_SH_MAP042_VPE31_0	32	0	rw	
GIC_SH_MAP043_VPE31_0	32	0	rw	
GIC_SH_MAP044_VPE31_0	32	0	rw	
GIC_SH_MAP045_VPE31_0	32	0	rw	
GIC_SH_MAP046_VPE31_0	32	0	rw	
GIC_SH_MAP047_VPE31_0	32	0	rw	
GIC_SH_MAP048_VPE31_0	32	0	rw	
GIC_SH_MAP049_VPE31_0	32	0	rw	
GIC_SH_MAP050_VPE31_0	32	0	rw	
		1		1

GIC_SH_MAP051_VPE31_0	32	0	rw	
GIC_SH_MAP052_VPE31_0	32	0	rw	
GIC_SH_MAP053_VPE31_0	32	0	rw	
GIC_SH_MAP054_VPE31_0	32	0	rw	
GIC_SH_MAP055_VPE31_0	32	0	rw	
GIC_SH_MAP056_VPE31_0	32	0	rw	
GIC_SH_MAP057_VPE31_0	32	0	rw	
GIC_SH_MAP058_VPE31_0	32	0	rw	
GIC_SH_MAP059_VPE31_0	32	0	rw	
GIC_SH_MAP060_VPE31_0	32	0	rw	
GIC_SH_MAP061_VPE31_0	32	0	rw	
GIC_SH_MAP062_VPE31_0	32	0	rw	
GIC_SH_MAP063_VPE31_0	32	0	rw	
GIC_SH_MAP064_VPE31_0	32	0	rw	
GIC_SH_MAP065_VPE31_0	32	0	rw	
GIC_SH_MAP066_VPE31_0	32	0	rw	
GIC_SH_MAP067_VPE31_0	32	0	rw	
GIC_SH_MAP068_VPE31_0	32	0	rw	
GIC_SH_MAP069_VPE31_0	32	0	rw	
GIC_SH_MAP070_VPE31_0	32	0		
GIC_SH_MAP071_VPE31_0	32	0	rw	
GIC_SH_MAP072_VPE31_0	32	0	rw	
GIC_SH_MAP073_VPE31_0	32	0	rw	
GIC_SH_MAP074_VPE31_0	32	0	rw	
GIC_SH_MAP075_VPE31_0	32	0	rw	
	32		rw	
GIC_SH_MAP076_VPE31_0	-	0	rw	
GIC_SH_MAP077_VPE31_0	32	0	rw	
GIC_SH_MAP078_VPE31_0	32	0	rw	
GIC_SH_MAP079_VPE31_0	32	0	rw	
GIC_SH_MAP080_VPE31_0	32	0	rw	
GIC_SH_MAP081_VPE31_0	32	0	rw	
GIC_SH_MAP082_VPE31_0	32	0	rw	
GIC_SH_MAP083_VPE31_0	32	0	rw	
GIC_SH_MAP084_VPE31_0	32	0	rw	
GIC_SH_MAP085_VPE31_0	32	0	rw	
GIC_SH_MAP086_VPE31_0	32	0	rw	
GIC_SH_MAP087_VPE31_0	32	0	rw	
GIC_SH_MAP088_VPE31_0	32	0	rw	
GIC_SH_MAP089_VPE31_0	32	0	rw	
GIC_SH_MAP090_VPE31_0	32	0	rw	
GIC_SH_MAP091_VPE31_0	32	0	rw	
GIC_SH_MAP092_VPE31_0	32	0	rw	
GIC_SH_MAP093_VPE31_0	32	0	rw	
GIC_SH_MAP094_VPE31_0	32	0	rw	
GIC_SH_MAP095_VPE31_0	32	0	rw	
GIC_SH_MAP096_VPE31_0	32	0	rw	
GIC_SH_MAP097_VPE31_0	32	0	rw	
GIC_SH_MAP098_VPE31_0	32	0	rw	
GIC_SH_MAP099_VPE31_0	32	0	rw	
GIC_SH_MAP100_VPE31_0	32	0	rw	
GIC_SH_MAP101_VPE31_0	32	0	rw	
GIC_SH_MAP102_VPE31_0	32	0	rw	
GIC_SH_MAP103_VPE31_0	32	0	rw	
GIC_SH_MAP104_VPE31_0	32	0	rw	
GIC_SH_MAP105_VPE31_0	32	0	rw	
GIC_SH_MAP106_VPE31_0	32	0	rw	
- 3 - 3 - 1 - 1 - 3 - 3 - 1 - 1 - 3 - 3				

GIC_SH_MAP107_VPE31_0	32	0	rw	
GIC_SH_MAP108_VPE31_0	32	0	rw	
GIC_SH_MAP109_VPE31_0	32	0	rw	
GIC_SH_MAP110_VPE31_0	32	0	rw	
GIC_SH_MAP111_VPE31_0	32	0	rw	
GIC_SH_MAP112_VPE31_0	32	0	rw	
GIC_SH_MAP113_VPE31_0	32	0	rw	
GIC_SH_MAP114_VPE31_0	32	0	rw	
GIC_SH_MAP115_VPE31_0	32	0	rw	
GIC_SH_MAP116_VPE31_0	32	0	rw	
GIC_SH_MAP117_VPE31_0	32	0	rw	
GIC_SH_MAP118_VPE31_0	32	0	rw	
GIC_SH_MAP119_VPE31_0	32	0	rw	
GIC_SH_MAP120_VPE31_0	32	0	rw	
GIC_SH_MAP121_VPE31_0	32	0	rw	
GIC_SH_MAP122_VPE31_0	32	0	rw	
GIC_SH_MAP123_VPE31_0	32	0	rw	
GIC_SH_MAP124_VPE31_0	32	0	rw	
GIC_SH_MAP125_VPE31_0	32	0	rw	
GIC SH MAP126 VPE31 0	32	0		
GIC_SH_MAP127_VPE31_0	32	0	rw	
GIC_SH_MAP128_VPE31_0	32	0	rw	
		_	rw	
GIC_SH_MAP129_VPE31_0	32	0	rw	
GIC_SH_MAP130_VPE31_0	32	0	rw	
GIC_SH_MAP131_VPE31_0	32	0	rw	
GIC_SH_MAP132_VPE31_0	32	0	rw	
GIC_SH_MAP133_VPE31_0	32	0	rw	
GIC_SH_MAP134_VPE31_0	32	0	rw	
GIC_SH_MAP135_VPE31_0	32	0	rw	
GIC_SH_MAP136_VPE31_0	32	0	rw	
GIC_SH_MAP137_VPE31_0	32	0	rw	
GIC_SH_MAP138_VPE31_0	32	0	rw	
GIC_SH_MAP139_VPE31_0	32	0	rw	
GIC_SH_MAP140_VPE31_0	32	0	rw	
GIC_SH_MAP141_VPE31_0	32	0	rw	
GIC_SH_MAP142_VPE31_0	32	0	rw	
GIC_SH_MAP143_VPE31_0	32	0	rw	
GIC_SH_MAP144_VPE31_0	32	0	rw	
GIC_SH_MAP145_VPE31_0	32	0	rw	
GIC_SH_MAP146_VPE31_0	32	0	rw	
GIC_SH_MAP147_VPE31_0	32	0	rw	
GIC_SH_MAP148_VPE31_0	32	0	rw	
GIC_SH_MAP149_VPE31_0	32	0	rw	
GIC_SH_MAP150_VPE31_0	32	0	rw	
GIC_SH_MAP151_VPE31_0	32	0	rw	
GIC_SH_MAP152_VPE31_0	32	0	rw	
GIC_SH_MAP153_VPE31_0	32	0	rw	
GIC_SH_MAP154_VPE31_0	32	0		
GIC_SH_MAP154_VPE31_0	32	0	rw rw	
GIC_SH_MAP156_VPE31_0	32	0		
GIC_SH_MAP150_VPE31_0 GIC_SH_MAP157_VPE31_0	32	0	rw	
		_	rw	
GIC_SH_MAP158_VPE31_0	32	0	rw	
GIC_SH_MAP159_VPE31_0	32	0	rw	
GIC_SH_MAP161_VPE31_0	32	0	rw	
GIC_SH_MAP161_VPE31_0	32	0	rw	
GIC_SH_MAP162_VPE31_0	32	0	rw	

		Т		
GIC_SH_MAP163_VPE31_0	32	0	rw	
GIC_SH_MAP164_VPE31_0	32	0	rw	
GIC_SH_MAP165_VPE31_0	32	0	rw	
GIC_SH_MAP166_VPE31_0	32	0	rw	
GIC_SH_MAP167_VPE31_0	32	0	rw	
GIC_SH_MAP168_VPE31_0	32	0	rw	
GIC_SH_MAP169_VPE31_0	32	0	rw	
GIC_SH_MAP170_VPE31_0	32	0	rw	
GIC_SH_MAP171_VPE31_0	32	0	rw	
GIC_SH_MAP172_VPE31_0	32	0	rw	
GIC_SH_MAP173_VPE31_0	32	0		
			rw	
GIC_SH_MAP174_VPE31_0	32	0	rw	
GIC_SH_MAP175_VPE31_0	32	0	rw	
GIC_SH_MAP176_VPE31_0	32	0	rw	
GIC_SH_MAP177_VPE31_0	32	0	rw	
GIC_SH_MAP178_VPE31_0	32	0	rw	
GIC_SH_MAP179_VPE31_0	32	0	rw	
GIC_SH_MAP180_VPE31_0	32	0	rw	
GIC_SH_MAP181_VPE31_0	32	0	rw	
GIC_SH_MAP182_VPE31_0	32	0	rw	
GIC_SH_MAP183_VPE31_0	32	0	rw	
GIC_SH_MAP184_VPE31_0	32	0	rw	
GIC_SH_MAP185_VPE31_0	32	0	rw	
GIC_SH_MAP186_VPE31_0	32	0	rw	
GIC_SH_MAP187_VPE31_0	32	0	rw	
GIC_SH_MAP188_VPE31_0	32	0	rw	
GIC_SH_MAP189_VPE31_0	32	0	rw	
GIC_SH_MAP190_VPE31_0	32	0	rw	
GIC_SH_MAP191_VPE31_0	32	0		
GIC_SH_MAP192_VPE31_0	32	0	rw	
GIC_SH_MAP193_VPE31_0	32	0	rw	
GIC_SH_MAP194_VPE31_0	32	0	rw	
			rw	
GIC_SH_MAP195_VPE31_0	32	0	rw	
GIC_SH_MAP196_VPE31_0	32	0	rw	
GIC_SH_MAP197_VPE31_0	32	0	rw	
GIC_SH_MAP198_VPE31_0	32	0	rw	
GIC_SH_MAP199_VPE31_0	32	0	rw	
GIC_SH_MAP200_VPE31_0	32	0	rw	
GIC_SH_MAP201_VPE31_0	32	0	rw	
GIC_SH_MAP202_VPE31_0	32	0	rw	
GIC_SH_MAP203_VPE31_0	32	0	rw	
GIC_SH_MAP204_VPE31_0	32	0	rw	
GIC_SH_MAP205_VPE31_0	32	0	rw	
GIC_SH_MAP206_VPE31_0	32	0	rw	
GIC_SH_MAP207_VPE31_0	32	0	rw	
GIC_SH_MAP208_VPE31_0	32	0	rw	
GIC_SH_MAP209_VPE31_0	32	0	rw	
GIC_SH_MAP210_VPE31_0	32	0		
GIC_SH_MAP211_VPE31_0	32	0	rw	
GIC_SH_MAP211_VPE31_0	32	-	rw	
		0	rw	
GIC_SH_MAP214_V/PE21_0	32	0	rw	
GIC_SH_MAP214_VPE31_0	32	0	rw	
GIC_SH_MAP215_VPE31_0	32	0	rw	
GIC_SH_MAP216_VPE31_0	32	0	rw	
GIC_SH_MAP217_VPE31_0	32	0	rw	
GIC_SH_MAP218_VPE31_0	32	0	rw	

GIC_SH_MAP219_VPE31_0	32	0	rw	
GIC_SH_MAP220_VPE31_0	32	0	rw	
GIC_SH_MAP221_VPE31_0	32	0	rw	
GIC_SH_MAP222_VPE31_0	32	0	rw	
GIC_SH_MAP223_VPE31_0	32	0	rw	
GIC_SH_MAP224_VPE31_0	32	0	rw	
GIC_SH_MAP225_VPE31_0	32	0	rw	
GIC_SH_MAP226_VPE31_0	32	0	rw	
GIC_SH_MAP227_VPE31_0	32	0	rw	
GIC_SH_MAP228_VPE31_0	32	0	rw	
GIC_SH_MAP229_VPE31_0	32	0	rw	
GIC_SH_MAP230_VPE31_0	32	0	rw	
GIC_SH_MAP231_VPE31_0	32	0	rw	
GIC_SH_MAP232_VPE31_0	32	0	rw	
GIC_SH_MAP233_VPE31_0	32	0	rw	
GIC_SH_MAP234_VPE31_0	32	0	rw	
GIC_SH_MAP235_VPE31_0	32	0	rw	
GIC_SH_MAP236_VPE31_0	32	0	rw	
GIC_SH_MAP237_VPE31_0	32	0	rw	
GIC SH MAP238 VPE31 0	32	0	rw	
GIC_SH_MAP239_VPE31_0	32	0	rw	
GIC_SH_MAP240_VPE31_0	32	0	rw	
GIC_SH_MAP241_VPE31_0	32	0	rw	
GIC_SH_MAP242_VPE31_0	32	0	rw	
GIC_SH_MAP243_VPE31_0	32	0	rw	
GIC_SH_MAP244_VPE31_0	32	0	rw	
GIC_SH_MAP245_VPE31_0	32	0	rw	
GIC_SH_MAP246_VPE31_0	32	0	rw	
GIC_SH_MAP247_VPE31_0	32	0	rw	
GIC_SH_MAP248_VPE31_0	32	0	rw	
GIC_SH_MAP249_VPE31_0	32	0	rw	
GIC_SH_MAP250_VPE31_0	32	0	rw	
GIC_SH_MAP251_VPE31_0	32	0	rw	
GIC_SH_MAP252_VPE31_0	32	0	rw	
GIC_SH_MAP253_VPE31_0	32	0	rw	
GIC_SH_MAP254_VPE31_0	32	0	rw	
GIC_SH_MAP255_VPE31_0	32	0	rw	
GIC_VB_DINT_SEND	32	0	-W	
GIC_VPE_CTL_L	32	a	rw	
GIC_VPE_PEND_L	32	0	r-	
GIC-VPE-MASK-L	32	7f	r-	
GIC_VPE_RMASK_L	32	0	-	
GIC_VPE_RMASK_L GIC_VPE_SMASK_L	32	0	-W	
GIC_VPE_SMASK_L GIC_VPE_WD_MAP_L	32	40000000	-W	
GIC_VPE_WD_MAP_L GIC_VPE_COMPARE_MAP_L	32	0	rw	
GIC_VPE_COMPARE_MAP_L GIC_VPE_TIMER_MAP_L	32	80000005	rw	
GIC_VPE_TIMER_MAP_L GIC_VPE_FDC_MAP_L	32	8000003e	rw	
GIC_VPE_FDC_MAP_L GIC_VPE_PERFCTR_MAP_L			rw	
	32	80000005	rw	
GIC_VPE_SWInt0_MAP_L	32	80000000	rw	
GIC_VPE_SWInt1_MAP_L	32	80000000	rw	
GIC_VPE_OTHER_ADDRESS_L	32	0	rw	
GIC_VPE_IDENT_L	32	0	r-	
GIC_VPE_WD_CONFIG_L	32	0	rw	
GIC_VPE_WD_COUNT_L	32	0	r-	
GIC_VPE_WD_INITIAL_L	32	0	rw	
GIC_VPE_CompareLo_L	32	fffffff	rw	

GIG LIDE G III I	0.0	ararar .		I
GIC_VPE_CompareHi_L	32	fffffff	rw	
GIC_VPE_EICSS00_L	32	0	rw	
GIC_VPE_EICSS01_L	32	0	rw	
GIC_VPE_EICSS02_L	32	0	rw	
GIC_VPE_EICSS03_L	32	0	rw	
GIC_VPE_EICSS04_L	32	0	rw	
GIC_VPE_EICSS05_L	32	0	rw	
GIC_VPE_EICSS06_L	32	0	rw	
GIC_VPE_EICSS07_L	32	0	rw	
GIC_VPE_EICSS08_L	32	0	rw	
GIC_VPE_EICSS09_L	32	0	rw	
GIC_VPE_EICSS10_L	32	0	rw	
GIC_VPE_EICSS11_L	32	0	rw	
GIC_VPE_EICSS12_L	32	0	rw	
GIC_VPE_EICSS13_L	32	0	rw	
GIC_VPE_EICSS14_L	32	0	rw	
GIC_VPE_EICSS15_L	32	0	rw	
GIC_VPE_EICSS16_L	32	0	rw	
GIC_VPE_EICSS17_L	32	0	rw	
GIC-VPE-EICSS18-L	32	0	rw	
GIC_VPE_EICSS19_L	32	0	rw	
GIC_VPE_EICSS19_E	32	0		
GIC-VPE-EICSS20-L	32	0	rw	
GIC_VPE_EICSS21_L	32	0	rw	
GIC_VPE_EICSS22_L GIC_VPE_EICSS23_L	32	-	rw	
GIC_VPE_EICSS23_L GIC_VPE_EICSS24_L		0	rw	
	32	0	rw	
GIC_VPE_EICSS25_L	32	0	rw	
GIC_VPE_EICSS26_L	32	0	rw	
GIC_VPE_EICSS27_L	32	0	rw	
GIC_VPE_EICSS28_L	32	0	rw	
GIC_VPE_EICSS29_L	32	0	rw	
GIC_VPE_EICSS30_L	32	0	rw	
GIC_VPE_EICSS31_L	32	0	rw	
GIC_VPE_EICSS32_L	32	0	rw	
GIC_VPE_EICSS33_L	32	0	rw	
GIC_VPE_EICSS34_L	32	0	rw	
GIC_VPE_EICSS35_L	32	0	rw	
GIC_VPE_EICSS36_L	32	0	rw	
GIC_VPE_EICSS37_L	32	0	rw	
GIC_VPE_EICSS38_L	32	0	rw	
GIC_VPE_EICSS39_L	32	0	rw	
GIC_VPE_EICSS40_L	32	0	rw	
GIC_VPE_EICSS41_L	32	0	rw	
GIC_VPE_EICSS42_L	32	0	rw	
GIC_VPE_EICSS43_L	32	0	rw	
GIC_VPE_EICSS44_L	32	0	rw	
GIC_VPE_EICSS44_L	32	0	rw	
GIC_VPE_EICSS45_L	32	0		
GIC_VPE_EICSS40_L GIC_VPE_EICSS47_L	32	0	rw	
GIC_VPE_EICSS47_L GIC_VPE_EICSS48_L	-	_	rw	
	32	0	rw	
GIC_VPE_EICSS49_L	32	0	rw	
GIC_VPE_EICSS50_L	32	0	rw	
GIC_VPE_EICSS51_L	32	0	rw	
GIC_VPE_EICSS52_L	32	0	rw	
GIC_VPE_EICSS53_L	32	0	rw	
GIC_VPE_EICSS54_L	32	0	rw	

GIC_VPE_EICSS55_L	32	0	rw	
GIC_VPE_EICSS56_L	32	0	rw	
GIC_VPE_EICSS57_L	32	0	rw	
GIC_VPE_EICSS58_L	32	0	rw	
GIC_VPE_EICSS59_L	32	0	rw	
GIC_VPE_EICSS60_L	32	0	rw	
GIC_VPE_EICSS61_L	32	0	rw	
GIC_VPE_EICSS62_L	32	0	rw	
GIC_VPE_EICSS63_L	32	0	rw	
GIC_Vx_DINT_PART_L	32	1	rw	
GIC_Cx_BRK_GROUP_L	32	0	rw	
GIC_VPE_CTL_O	32	a	rw	
GIC_VPE_PEND_O	32	0	r-	
GIC_VPE_MASK_O	32	7f	r-	
GIC_VPE_RMASK_O	32	0	-w	
GIC_VPE_SMASK_O	32	0	-w	
GIC_VPE_WD_MAP_O	32	40000000	rw	
GIC_VPE_COMPARE_MAP_O	32	0	rw	
GIC_VPE_TIMER_MAP_O	32	80000005	rw	
GIC_VPE_FDC_MAP_O	32	8000003e	rw	
GIC_VPE_PERFCTR_MAP_O	32	80000005	rw	
GIC_VPE_SWInt0_MAP_O	32	80000000	rw	
GIC_VPE_SWInt1_MAP_O	32	80000000	rw	
GIC_VPE_OTHER_ADDRESS_O	32	0	rw	
GIC_VPE_IDENT_O	32	0	r-	
GIC_VPE_WD_CONFIG_O	32	0	rw	
GIC_VPE_WD_COUNT_O	32	0	r-	
GIC_VPE_WD_INITIAL_O	32	0	rw	
GIC_VPE_CompareLo_O	32	fffffff	rw	
GIC_VPE_CompareHi_O	32	fffffff	rw	
GIC_VPE_EICSS00_O	32	0	rw	
GIC_VPE_EICSS01_O	32	0	rw	
GIC_VPE_EICSS02_O	32	0	rw	
GIC_VPE_EICSS03_O	32	0	rw	
GIC_VPE_EICSS04_O	32	0	rw	
GIC_VPE_EICSS05_O	32	0	rw	
GIC_VPE_EICSS06_O	32	0	rw	
GIC_VPE_EICSS07_O	32	0	rw	
GIC_VPE_EICSS08_O	32	0	rw	
GIC_VPE_EICSS09_O	32	0	rw	
GIC-VPE_EICSS10_O	32	0	rw	
GIC_VPE_EICSS11_O	32	0	rw	
GIC-VPE-EICSS12-O	32	0		
GIC_VPE_EICSS12_O	32	0	rw	
GIC_VPE_EICSS13_O	32	0	+	
GIC_VPE_EICSS14_O	32	0	rw	
GIC_VPE_EICSS15_O	32	0	rw	
GIC_VPE_EICSS16_O	32	0	rw	
GIC_VPE_EICSS17_O	32	0	rw	
GIC_VPE_EICSS18_O	32	0	rw	
			rw	
GIC_VPE_EICSS20_O	32	0	rw	
GIC_VPE_EICSS21_O	32	0	rw	
GIC_VPE_EICSS22_O	32	0	rw	
GIC_VPE_EICSS23_O	32	0	rw	
GIC_VPE_EICSS24_O	32	0	rw	
GIC_VPE_EICSS25_O	32	0	rw	

			1	
GIC_VPE_EICSS26_O	32	0	rw	
GIC_VPE_EICSS27_O	32	0	rw	
GIC_VPE_EICSS28_O	32	0	rw	
GIC_VPE_EICSS29_O	32	0	rw	
GIC_VPE_EICSS30_O	32	0	rw	
GIC_VPE_EICSS31_O	32	0	rw	
GIC_VPE_EICSS32_O	32	0	rw	
GIC_VPE_EICSS33_O	32	0	rw	
GIC_VPE_EICSS34_O	32	0	rw	
GIC_VPE_EICSS35_O	32	0	rw	
GIC_VPE_EICSS36_O	32	0	rw	
GIC_VPE_EICSS37_O	32	0	rw	
GIC_VPE_EICSS38_O	32	0	rw	
GIC_VPE_EICSS39_O	32	0	rw	
GIC_VPE_EICSS40_O	32	0	rw	
GIC_VPE_EICSS41_O	32	0	rw	
GIC_VPE_EICSS42_O	32	0	rw	
GIC_VPE_EICSS43_O	32	0	rw	
GIC_VPE_EICSS44_O	32	0	rw	
GIC_VPE_EICSS45_O	32	0	rw	
GIC_VPE_EICSS46_O	32	0	rw	
GIC_VPE_EICSS47_O	32	0	rw	
GIC_VPE_EICSS48_O	32	0	rw	
GIC_VPE_EICSS49_O	32	0	rw	
GIC_VPE_EICSS50_O	32	0	rw	
GIC_VPE_EICSS51_O	32	0	rw	
GIC_VPE_EICSS52_O	32	0	rw	
GIC_VPE_EICSS53_O	32	0	rw	
GIC_VPE_EICSS54_O	32	0	rw	
GIC_VPE_EICSS55_O	32	0	rw	
GIC_VPE_EICSS56_O	32	0	rw	
GIC_VPE_EICSS57_O	32	0	rw	
GIC_VPE_EICSS58_O	32	0	rw	
GIC_VPE_EICSS59_O	32	0	rw	
GIC_VPE_EICSS60_O	32	0	rw	
GIC_VPE_EICSS61_O	32	0	rw	
GIC_VPE_EICSS62_O	32	0	rw	
GIC_VPE_EICSS63_O	32	0	rw	
GIC_Vx_DINT_PART_O	32	1	rw	
GIC_Cx_BRK_GROUP_O	32	0	rw	
GIC_CounterLoUser	32	0	r-	
GIC_CounterHiUser	32	0	r-	
55555555555555			1 *	

Table 13.10: Registers at level 4, type:TC group:CMP_GIC

13.4.7 Integration_support

Registers at level:4, type:TC group:Integration_support

Name	Bits	Initial-Hex	RW	Description
stop	32	0	rw	write with non-zero to stop processor

Table 13.11: Registers at level 4, type:TC group:Integration_support