Imperas Peripheral Model Guide

Model Specific Information for nxp.ovpworld.org / iMX6_SDHC

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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

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1.0 Model Specific Information

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers, other component parts, and configuration options and general information for peripheral modeling with Imperas OVP.

1.1 Description

NXP i.MX6 SDHC Ultra Secured Digital Host Controller

1.2 Licensing

Open Source Apache 2.0

1.3 Limitations

Not Complete. Register interface only.

Support only for memory card features.

1.4 Reference

i.MX 6Solo/6DualLite Applications Processor Reference Manual (IMX6SDLRM_Ref_Manual.pdf

1.5 Location

The iMX6_SDHC peripheral model is located in an Imperas/OVP installation at the VLNV: nxp.ovpworld.org / peripheral / iMX6_SDHC / 1.0.

2.0 Peripheral Instance Parameters

This model accepts the following parameters:

Table 1. Peripheral Parameters

Name	Type	Description
SD_DRIVE	string	The name of the Image file used for the SD Drive
SD_DRIVE_DELTA	bool	If present the SD Drive uses delta writes

3.0 Net Ports

This model has the following net ports:

Table 2. Net Ports

Name	Type	Must Be Connected	Description
interrupt	output	F (False)	Interrupt Output
CD	input	F (False)	SD Card Detect
WP	input	F (False)	SD Card Write Protect
LCTL	output	F (False)	SD Card Interface busy LED drive

reset	input	F (False)	

4.0 Bus Master Ports

This model has the following bus master ports:

4.1 Bus Master Port: mport

Table 3. mport

Name	Address Width (bits)	Description
mport	32	Master port for DMA accesses

5.0 Bus Slave Ports

This model has the following bus slave ports:

5.1 Bus Slave Port: bport1

Table 4. Bus Slave Port: bport1

Name	Size (bytes)	Must Be Connected	Description
bport1	0x4000	T (True)	Slave port for register and data accesses

Table 5. Bus Slave Port: bport1 Registers:

Name	Offset	Width (bits)	Description	R/W	is Volatile
ab_uSDHC_DS_ADDR	0x0	32	Description DMA System Address Blocks Count For Current Transfer Transfer Block Size		
ab_uSDHC_BLK_ATT	0x4	32	Block Attributes		
ab_uSDHC_CMD_ARG	0x8	32	Command Argument		
ab_uSDHC_CMD_XFR_TYP	0xc	32	Description Command Transfer Type Command Index Command Type Data Present Select Command Index Check Enable Command CRC Check Enable Response Type Select		
ab_uSDHC_CMD_RSP0	0x10	32	Command Response0		
ab_uSDHC_CMD_RSP1	0x14	32	Command Response1		
ab_uSDHC_CMD_RSP2	0x18	32	Command Response2		
ab_uSDHC_CMD_RSP3	0x1c	32	Command Response3		
ab_uSDHC_DATA_BUFF_ACC_PORT	0x20	32	Data Buffer Access Port		
ab_uSDHC_PRES_STATE	0x24	32	Description Present State Data Line Signal Level CMD Line Signal Level Write Protect Switch Pin Level Card Detect Pin Level Card Inserted Re-Tuning Request (only for SD3.0 SDR104 mode) Buffer Read Enable Buffer Write Enable Read		

			Transfer Active Write Transfer Active SD Clock Gated Off Internally IPG_PERCLK Gated Off Internally HCLK Gated Off Internally IPG_CLK Gated Off Internally SD Clock Stable Data Line Active Command Inhibit (DATA) Command Inhibit (CMD)		
ab_uSDHC_PROT_CTRL	0x28	32	Description Protocol Control Current block read is non-exact block read. It is only used for SDIO. BURST length enable for INCR, INCR4 / INCR8 / INCR16, INCR4-WRAP / INCR8-WRAP / INCR16-WRAP Wakeup Event Enable On SD Card Removal Wakeup Event Enable On SD Card Insertion Wakeup Event Enable On Card Interrupt Read done no 8 clock Interrupt At Block Gap Read Wait Control Continue Request Stop At Block Gap Request DMA Select Card Detect Signal Selection Card Detect Test Level Endian Mode DATA3 as Card Detection Pin Data Transfer Width LED Control		
ab_uSDHC_SYS_CTRL	0x2c	32	Description System Control Initialization Active Software Reset For DATA Line Software Reset For CMD Line Software Reset For ALL hardware reset of the card Data Timeout Counter Value SDCLK Frequency Select Divisor		
ab_uSDHC_INT_STATUS	0x30	32	Description Interrupt Status DMA Error Tuning Error: (only for SD3.0 SDR104 mode) Auto CMD12 Error Data End Bit Error Data CRC Error Data Timeout Error Command Index Error Command End Bit Error Command CRC Error Command Timeout Error Tuning Pass:(only for SD3.0 SDR104 mode) Re-Tuning Event: (only for SD3.0 SDR104 mode)		

			Card Interrupt Card Removal Card Insertion Buffer Read Ready Buffer Write Ready DMA Interrupt Block Gap Event Transfer Complete Command Complete		
ab_uSDHC_INT_STATUS_EN	0x34	32	Description Interrupt Status Enable DMA Error Tuning Error: (only for SD3.0 SDR104 mode) Auto CMD12 Error Data End Bit Error Data CRC Error Data Timeout Error Command Index Error Command End Bit Error Command CRC Error Command Timeout Error Tuning Pass:(only for SD3.0 SDR104 mode) Re-Tuning Event: (only for SD3.0 SDR104 mode) Card Interrupt Card Removal Card Insertion Buffer Read Ready Buffer Write Ready DMA Interrupt Block Gap Event Transfer Complete Command Complete		
ab_uSDHC_INT_SIGNAL_EN	0x38	32	Description Interrupt Signal Enable DMA Error Tuning Error: (only for SD3.0 SDR104 mode) Auto CMD12 Error Data End Bit Error Data CRC Error Data Timeout Error Command Index Error Command End Bit Error Command CRC Error Command Timeout Error Tuning Pass:(only for SD3.0 SDR104 mode) Re-Tuning Event: (only for SD3.0 SDR104 mode) Card Interrupt Card Removal Card Insertion Buffer Read Ready Buffer Write Ready DMA Interrupt Block Gap Event Transfer Complete Command Complete		
ab_uSDHC_AUTOCMD12_ERR_STATUS	0x3c	32	Description Auto CMD12 Error Status Command Not Issued By Auto CMD12 Error Auto CMD12/23 Index Error Auto CMD12/23 CRC Error Auto CMD12/23 End Bit Error Auto CMD12/23 Timeout Error Auto CMD12 Not Executed		

ab_uSDHC_HOST_CTRL_CAP	0x40	32	Description Host Controller Capabilities Voltage Support 1.8 V Voltage Support 3.0 V Voltage Support 3.3V Suspend / Resume Support DMA Support High Speed Support ADMA Support (Advanced DMA Support) Max Block Length		
ab_uSDHC_WTMK_LVL	0x44	32	Description Watermark Level Write Burst Length 1 Write Watermark Level Read Burst Length 2 Read Watermark Level		
ab_uSDHC_MIX_CTRL	0x48	32	Description Mixer Control Feedback Clock Source Selection (Only used for SD3.0, SDR104 mode) Auto Tuning Enable (Only used for SD3.0, SDR104 mode) Tuned clock or Fixed clock is used to sample data / cmd (Only used for SD3.0, SDR104 mode) Execute Tuning: (Only used for SD3.0, SDR104 mode) Auto CMD23 Enable In DDR 4-bit mode nibble position indictation Multi / Single Block Select Data Transfer Direction Select Dual Data Rate mode selection Auto CMD12 Enable Block Count Enable DMA Enable		
ab_uSDHC_FORCE_EVENT	0x50	32	Description Force Event Force Event Card Interrupt Force Event DMA Error Force Tuning Error Force Event Auto Command 12 Error Force Event Data End Bit Error Force Event Data CRC Error Force Event Data Time Out Error Force Event Command Index Error Force Event Command End Bit Error Force Event Command CRC Error Force Event Command Time Out Error Force Event Command Not Executed By Auto Command 12 Error Force Event Auto Command 12 Index Error Force Event Auto Command 12 End Bit		

			Error Force Event Auto Command 12 CRC Error Force Event Auto Command 12 Time Out Error Force Event Auto Command 12 Not Executed		
ab_uSDHC_ADMA_ERR_STATUS	0x54	32	Description ADMA Error Status Register ADMA Descritor Error ADMA Length Mismatch Error ADMA Error State (when ADMA Error is occurred)		
ab_uSDHC_ADMA_SYS_ADDR	0x58	32	ADMA System Address		
ab_uSDHC_DLL_CTRL	0x60	32	Description DLL (Delay Line) Control DLL control loop update interval Slave delay line update interval Refer to DLL_CTRL_SLV_DLY_TARGET0 When SLV_OVERRIDE = 1 This field is used to select 1 of 128 physical taps manually. A value of 0 selects tap 1, and a value of 0x7f selects tap 128. Enable manual override for slave delay chain using SLV_OVERRIDE_VAL Prevent the DLL from updating The delay target for the uSDHC loopback read clock Force the slave delay line to update to the DLL calibrated value immediately Force a reset on DLL Enable the DLL and delay chain		
ab_uSDHC_DLL_STATUS	0x64	32	Description DLL Status Reference delay line select taps Slave delay line select status Reference DLL lock status Slave delay-line lock status		
ab_uSDHC_CLK_TUNE_CTRL_STATUS	0x68	32	Description CLK Tuning Control and Status PRE error Number of delay cells added on the feedback clock between the feedback clock and CLK_PRE Number of delay cells added on the feedback clock between CLK_PRE and CLK_OUT Number of delay cells added on the feedback clock between CLK_OUT and		

			CLK_POST NXT error Number of delay cells on the feedback clock between the feedback clock and CLK_PRE Number of delay cells on the feedback clock between CLK_PRE and CLK_OUT Number of delay cells on the feedback clock between CLK_OUT and CLK_POST		
ab_uSDHC_VEND_SPEC	0xc0	32	Description Vendor Specific Register Byte access Enable Internal State Value CRC Check Disable Card Clock Software Enable IPG_PERCLK Software Enable AHB Clock Software Enable IPG_CLK Software Enable Force CLK output active Only for debug. Force CLK output active when sending Abort command Only for debug. Polarity of the WP pin Only for debug.Polarity of the CD_B pin Only for debug.Polarity of DATA3 pin when it is used as card detection Check busy enable after auto CMD12 for write data packet Conflict check enable Voltage Selection External DMA Request Enable		
ab_uSDHC_MMC_BOOT	0xc4	32	Description MMC Boot Register Stop At Block Gap value of automatic mode Disable Time Out Enable auto stop at block gap function Boot mode enable Boot mode select Boot ACK mode select Boot ACK time out counter value		
ab_uSDHC_VEND_SPEC2	0xc8	32	Description Vendor Specific 2 Register Disable the feature to clear the Card interrupt status bit when Card Interrupt status enable bit is cleared Enable the auto tuning circuit to check the CMD line Enable the auto tuning circuit to check the DATA0 only. It is used with the TUNING_8bit_EN		

			together. Enable the auto tuning circuit to check the DATA[7:0]. It is used with the TUNING_1bit_EN together. Card Interrupt Detection Test Interrupt window after abort command is sent. CMD_OE / DATA_OE logic generation test. Timeout counter test.		

6.0 Peripheral components in the library

Table 6. Publicly available Imperas/OVP peripheral models (224 models)

Peripheral	Peripheral	Peripheral
nxp.ovpworld.org/iMX6_SRC	nxp.ovpworld.org/iMX6_UART	nxp.ovpworld.org/iMX6_WDOG
ovpworld.org/Alpha2x16Display	ovpworld.org/DynamicBridge	ovpworld.org/FlashDevice
ovpworld.org/ledRegister	ovpworld.org/SerInt	ovpworld.org/SimpleDma
ovpworld.org/switchRegister	ovpworld.org/temperatureSensor	ovpworld.org/trap
ovpworld.org/trap4K	ovpworld.org/vEthernet_Bridge	ovpworld.org/VirtioBlkMMIO
ovpworld.org/VirtioNetMMIO	philips.ovpworld.org/ISP1761	renesas.ovpworld.org/adc
renesas.ovpworld.org/bcu	renesas.ovpworld.org/brg	renesas.ovpworld.org/can
renesas.ovpworld.org/can	renesas.ovpworld.org/clkgen	renesas.ovpworld.org/crc
renesas.ovpworld.org/csib	renesas.ovpworld.org/csie	renesas.ovpworld.org/dma
renesas.ovpworld.org/intc	renesas.ovpworld.org/memc	renesas.ovpworld.org/rng
renesas.ovpworld.org/taa	renesas.ovpworld.org/tms	renesas.ovpworld.org/tmt
renesas.ovpworld.org/uartc	renesas.ovpworld.org/UPD70F3441Logic	riscv.ovpworld.org/CLINT
riscv.ovpworld.org/PLIC	riscv.ovpworld.org/SmartLoaderRV64Linux	safepower.ovpworld.org/node
safepower.ovpworld.org/NostrumNode	safepower.ovpworld.org/ring_oscillator	safepower.ovpworld.org/TTELNode
sifive.ovpworld.org/gpio	sifive.ovpworld.org/MSEL	sifive.ovpworld.org/PRCI
sifive.ovpworld.org/pwm	sifive.ovpworld.org/spi	sifive.ovpworld.org/teststatus
sifive.ovpworld.org/UART	smsc.ovpworld.org/LAN9118	smsc.ovpworld.org/LAN91C111
ti.ovpworld.org/tca6416a	ti.ovpworld.org/UartInterface	ti.ovpworld.org/ucd9012a
ti.ovpworld.org/ucd9248	vendor.com/fifo	xilinx.ovpworld.org/axi-gpio
xilinx.ovpworld.org/axi-intc	xilinx.ovpworld.org/axi-pcie	xilinx.ovpworld.org/axi-timer
xilinx.ovpworld.org/logicore-fit	xilinx.ovpworld.org/mdm	xilinx.ovpworld.org/mpmc
xilinx.ovpworld.org/xps-gpio	xilinx.ovpworld.org/xps-iic	xilinx.ovpworld.org/xps-intc
xilinx.ovpworld.org/xps-ll-temac	xilinx.ovpworld.org/xps-mch-emc	xilinx.ovpworld.org/xps-sysace
xilinx.ovpworld.org/xps-timer	xilinx.ovpworld.org/xps-uartlite	xilinx.ovpworld.org/zynq_7000-can
xilinx.ovpworld.org/zynq_7000-ddrc	xilinx.ovpworld.org/zynq_7000-devcfg	xilinx.ovpworld.org/zynq_7000-dmac
xilinx.ovpworld.org/zynq_7000-gpio	xilinx.ovpworld.org/zynq_7000-iic	xilinx.ovpworld.org/zynq_7000-ocm
xilinx.ovpworld.org/zynq_7000-qos301	xilinx.ovpworld.org/zynq_7000-qspi	xilinx.ovpworld.org/zynq_7000-sdio
xilinx.ovpworld.org/zynq_7000-slcr	xilinx.ovpworld.org/zynq_7000-spi	xilinx.ovpworld.org/zynq_7000-swdt
xilinx.ovpworld.org/zynq_7000-ttc	xilinx.ovpworld.org/zynq_7000-tz_GPVsecurity	xilinx.ovpworld.org/zynq_7000-tz_security
xilinx.ovpworld.org/zynq_7000-usb	altera.ovpworld.org/dw-apb-timer	altera.ovpworld.org/dw-apb-uart
altera.ovpworld.org/IntervalTimer32Core	altera.ovpworld.org/IntervalTimer64Core	altera.ovpworld.org/JtagUart
altera.ovpworld.org/PerformanceCounterCore	altera.ovpworld.org/RSTMGR	altera.ovpworld.org/SystemIDCore
altera.ovpworld.org/Uart	amd.ovpworld.org/79C970	andes.ovpworld.org/ATCUART100
andes.ovpworld.org/NCEPLIC100	andes.ovpworld.org/NCEPLMT100	arm.ovpworld.org/AaciPL041
arm.ovpworld.org/CompactFlashRegs	arm.ovpworld.org/CoreModule9x6	arm.ovpworld.org/DebugLedAndDipSwitch
arm.ovpworld.org/DMemCtrlPL341	arm.ovpworld.org/IcpControl	arm.ovpworld.org/IcpCounterTimer
arm.ovpworld.org/IntICP	arm.ovpworld.org/IntICP	arm.ovpworld.org/KbPL050
arm.ovpworld.org/L2CachePL310	arm.ovpworld.org/LcdPL110	arm.ovpworld.org/MmciPL181
arm.ovpworld.org/RtcPL031	arm.ovpworld.org/SerBusDviRegs	arm.ovpworld.org/SmartLoaderArm64Linux
arm.ovpworld.org/SmartLoaderArmLinux	arm.ovpworld.org/SMemCtrlPL354	arm.ovpworld.org/SysCtrlSP810
arm.ovpworld.org/TimerSP804	arm.ovpworld.org/TzpcBP147	arm.ovpworld.org/UartPL011
arm.ovpworld.org/VexpressSysRegs	arm.ovpworld.org/WdtSP805	atmel.ovpworld.org/AdvancedInterruptController
atmel.ovpworld.org/ParallelIOController	atmel.ovpworld.org/PowerSaving	atmel.ovpworld.org/SpecialFunction

atmel.ovpworld.org/TimerCounter	atmel.ovpworld.org/UsartInterface	atmel.ovpworld.org/WatchdogTimer
cadence.ovpworld.org/gem	cadence.ovpworld.org/uart	cirrus.ovpworld.org/GD5446
freescale.ovpworld.org/KinetisADC	freescale.ovpworld.org/KinetisAIPS	freescale.ovpworld.org/KinetisAXBS
freescale.ovpworld.org/KinetisCAN	freescale.ovpworld.org/KinetisCMP	freescale.ovpworld.org/KinetisCMT
freescale.ovpworld.org/KinetisCRC	freescale.ovpworld.org/KinetisDAC	freescale.ovpworld.org/KinetisDDR
freescale.ovpworld.org/KinetisDMA	freescale.ovpworld.org/KinetisDMAC	freescale.ovpworld.org/KinetisDMAMUX
freescale.ovpworld.org/KinetisENET	freescale.ovpworld.org/KinetisEWM	freescale.ovpworld.org/KinetisFB
freescale.ovpworld.org/KinetisFMC	freescale.ovpworld.org/KinetisFTFE	freescale.ovpworld.org/KinetisFTM
freescale.ovpworld.org/KinetisGPIO	freescale.ovpworld.org/KinetisI2C	freescale.ovpworld.org/KinetisI2S
freescale.ovpworld.org/KinetisLLWU	freescale.ovpworld.org/KinetisLPTMR	freescale.ovpworld.org/KinetisMCG
freescale.ovpworld.org/KinetisMPU	freescale.ovpworld.org/KinetisNFC	freescale.ovpworld.org/KinetisOSC
freescale.ovpworld.org/KinetisPDB	freescale.ovpworld.org/KinetisPIT	freescale.ovpworld.org/KinetisPMC
freescale.ovpworld.org/KinetisPORT	freescale.ovpworld.org/KinetisRCM	freescale.ovpworld.org/KinetisRFSYS
freescale.ovpworld.org/KinetisRFVBAT	freescale.ovpworld.org/KinetisRNG	freescale.ovpworld.org/KinetisRTC
freescale.ovpworld.org/KinetisSDHC	freescale.ovpworld.org/KinetisSIM	freescale.ovpworld.org/KinetisSMC
freescale.ovpworld.org/KinetisSPI	freescale.ovpworld.org/KinetisTSI	freescale.ovpworld.org/KinetisUART
freescale.ovpworld.org/KinetisUSB	freescale.ovpworld.org/KinetisUSBDCD	freescale.ovpworld.org/KinetisUSBHS
freescale.ovpworld.org/KinetisVREF	freescale.ovpworld.org/KinetisWDOG	freescale.ovpworld.org/Uart
freescale.ovpworld.org/VybridADC	freescale.ovpworld.org/VybridANADIG	freescale.ovpworld.org/VybridCCM
freescale.ovpworld.org/VybridDMA	freescale.ovpworld.org/VybridGPIO	freescale.ovpworld.org/VybridI2C
freescale.ovpworld.org/VybridLCD	freescale.ovpworld.org/VybridQUADSPI	freescale.ovpworld.org/VybridSDHC
freescale.ovpworld.org/VybridSPI	freescale.ovpworld.org/VybridUART	freescale.ovpworld.org/VybridUSB
imperas.ovpworld.org/frameBuffer	imperas.ovpworld.org/uart	imperas.ovpworld.org/usecCounter
intel.ovpworld.org/82077AA	intel.ovpworld.org/82371EB	intel.ovpworld.org/8253
intel.ovpworld.org/8259A	intel.ovpworld.org/NorFlash48F4400	intel.ovpworld.org/PciIDE
intel.ovpworld.org/PciPM	intel.ovpworld.org/PciUSB	intel.ovpworld.org/Ps2Control
marvell.ovpworld.org/GT6412x	maxim.ovpworld.org/max673x	microsemi.ovpworld.org/CoreUARTapb
mips.ovpworld.org/16450C	mips.ovpworld.org/MaltaFPGA	mips.ovpworld.org/SmartLoaderLinux
motorola.ovpworld.org/MC146818	national.ovpworld.org/16450	national.ovpworld.org/16550
national.ovpworld.org/16550_4bytes	nxp.ovpworld.org/iMX6_Analog	nxp.ovpworld.org/iMX6_CCM
nxp.ovpworld.org/iMX6_GPC	nxp.ovpworld.org/iMX6_GPIO	nxp.ovpworld.org/iMX6_GPT
nxp.ovpworld.org/iMX6_MMDC	nxp.ovpworld.org/iMX6_SDHC	

7.0 General Information on Peripheral Models

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers etc. and configuration options and general information for peripheral modeling with Imperas OVP.

7.1 Background

Imperas OVP simulation technology enables very high performance simulation, debug and analysis of platforms containing multiple processors and peripheral models. The technology is designed to be extensible: you can create new models of processors, peripherals and other platform components using interfaces and libraries defined by OVP.

The peripheral models created using the OVP APIs run on the Peripheral Simulation Engine (PSE).

The model is typically written in C and compiled into an executable for the PSE processor architecture. The model is compiled for speed of execution and to protect IP. It is dynamically loaded by the simulator at run time.

8.0 Building peripherals easily with Imperas iGen

To aid with model creation, Imperas products include iGen, a model generation tool. iGen takes the laborious and error-prone task of constructing the various hardware model and software element files required for a typical model, and automates this process. iGen creates the needed C files. iGen also creates the C++ SystemC TLM2 interface files needed to run peripheral models in SystemC simulations.

iGen takes as input a simple script specification that includes device internals such as registers and memories, port information, component descriptors, and other elements. iGen then builds the C code model files and user editable templates. These include model frameworks with registers, function calls, memory map, and other items. It ensures that all component parts of the model are well-structured using best practices, and are consistent throughout the files, thus eliminating a common source of errors.

More information on iGen can be found: imperas.com/products.

9.0 Peripheral model internals

Each instance of a peripheral model runs on its own virtual machine with an address space large enough for the model. This processor (the PSE) and its memory are separate from any processors, memories and buses in the platform being simulated; they exist only to execute the code of the peripheral model.

Interception of functions defined in the peripheral model allows the use of features of the host system in the

implementation of the behavior of a peripheral. As an example, a real platform might contain a video display device. When simulating this system, it is generally more convenient not to simulate the complete video display device but to use a video package available on the host machine, such as SDL, and to use this to render to the host display. Also models of uarts, ethernet devices and USB components can make use of the host PC resources during simulation, to allow, for example, a simulation to browse the real internet, or the simulation to connect to a real USB device.

10.0 Parts of peripheral models

10.1 Configuring the Peripheral Instance with Parameters

A peripheral can include the behaviour of several configurations. These are controlled when the peripheral is instanced in the platform by setting parameters defined on the peripheral.

10.2 Net Ports

Peripherals may be connected to other peripherals or processors with signal wires (nets). These can be used to act as interrupt signals or used to control behavior between peripherals.
The wires are created in the platform as nets and this net is connected into the peripheral using a net port.

10.3 Bus master ports

A bus master port initiates (and controls the address of) a bus cycle. Bus cycles are generated by behavioral code within the peripheral model.

10.4 Bus slave ports

A peripheral can be defined as having several bus slave ports. The bus slave ports can be split into several address blocks. Each address block be either local memory or memory mapped registers. Both of these can have associated callback functions. A memory mapped register can also be defined as specific read/write access, whether it is volatile, and also whether it is associated with a reset pin and mask. A memory mapped register can also have specific bit fields defined.

10.5 Packetnets

A peripheral can be defined as being connected to packetnet ports. A packetnet is used to model packet based communication such as Ethernet, CAN bus or GSM. A packetnet is created in a platform, then connected to packetnet ports on model instances. A packetnet can have many connections, each able to send or receive packets. A packetnet is used as an efficient method of communication within OVP models.

For more information on modeling with packetnets, please see the peripheral modeling documentation: OVP_Peripheral_Modeling_Guide.pdf, OVPsim_and_CpuManager_User_Guide.pdf and the example: $IMPERAS_HOME/Examples/Models/Peripherals/packetnet.

11.0 More information (documentation) on peripheral models and modeling

More information on modeling and APIs can be found at: OVPworld.org/technology_apis.

Specifics on modeling peripherals can be found: OVP_Peripheral_Modeling_Guide.pdf.

A full list of the currently available OVP documentation is available: OVPworld.org/documentation.
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