

OVP Guide to Using Processor Models

Model specific information for MIPS_MIPS64R6

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Contents

1	Overview	1
	1.1 Description	1
	1.2 Licensing	1
	1.3 Limitations	2
	1.4 Verification	2
	1.5 Features	2
	1.6 Description	2
	1.7 Licensing	2
	1.8 Limitations	2
	1.9 Verification	3
	1.10 Features	3
	1.11 Description	3
	1.12 Licensing	3
	1.13 Limitations	3
	1.14 Verification	3
	1.15 Features	4
2	Configuration	5
	2.1 Location	5
	2.2 GDB Path	5
	2.3 Semi-Host Library	5
	2.4 Processor Endian-ness	5
	2.5 QuantumLeap Support	5
	2.6 Processor ELF code	5
3	All Variants in this model	6
4	Bus Master Ports	7
5	Bus Slave Ports	8
6	Net Ports	9
7	FIFO Ports	20
8	Formal Parameters	2 1
9	Execution Modes	7 8

10 Exc	eptions	7 9
11 Hier	carchy of the model	82
	· · · · · · · · · · · · · · · · · · ·	82
11.2	Level 2: CPU	82
11.3	Level 3: VP	82
19 Mag	del Commands	84
		84
12.1		84
	·	84
19.9		84
12.2		84
	v	85
10.2		
12.3		85
	U	85
		85
	±	86
	1	86
	9	86
	1	86
	1	86
	1	86
	12.3.7.1 Argument description	86
	12.3.8 mipsCacheReset	86
	12.3.8.1 Argument description	86
	12.3.9 mipsCacheTrace	86
	12.3.10 mipsDebugFlags	87
	12.3.11 mipsReadRegister	87
	12.3.12 mipsReadTLBEntry	87
	· · · · · · · · · · · · · · · · · · ·	87
	± ±	87
	· · · · · · · · · · · · · · · · · · ·	88
	•	88
	•	88
	1	88
	•	88
		88
		88
	*	88
	1 9	
	12.3.20 mipsWriteTLBEntry	89
13 Reg		90
		90
13.2	Level 2: CPU	90
13.3	Level 3: VP	90
	13.3.1 Core	90
	13.3.2 FPU	91

Imperas OVP Fast Processor Model Documentation for MIPS_MIPS64R6

13.3.3	DSP		 	 	 	 	 						92
13.3.4	Shadow		 	 	 	 	 						92
13.3.5	COP0		 	 	 	 	 						94
13.3.6	$MSA \dots$.		 	 	 	 	 						97
13.3.7	$\operatorname{CMP_GCR}$.		 	 	 	 	 						98
13.3.8	$\operatorname{CMP_CPC}$.		 	 	 	 	 						99
13.3.9	$\mathrm{CMP_GIC}$		 	 	 	 	 						99
13 3 10	Integration su	innort											119

Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.

The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners. There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

MIPS64 Configurable Processor Model

If you need other variants, these models can be obtained from www.OVPworld.org/MIPSuser.

1.2 Licensing

Usage of binary model under license governing simulator usage. Source of model available under Imperas Software License Agreement.

1.3 Limitations

If this model is not part of your installation, then it is available for download from www.OVPworld.org/MIPSuser.

Cache model does not implement coherency

1.4 Verification

Models have been validated correct as part of the MIPS Verified program and run through the MIPS AVP test programs

1.5 Features

Only MIPS64 Instruction set implemented

MMU Type: Dual VTLB and FTLB

FPU implemented

L1 I and D cache model in either full or tag-only mode implemented (disabled by default)

External interrupt controller implemented

Vectored interrupts implemented

1.6 Description

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1.15 Features

Only MIPS64 Instruction set implemented

MMU Type: Dual VTLB and FTLB

FPU implemented

L1 I and D cache model in either full or tag-only mode implemented (disabled by default)

External interrupt controller implemented

Vectored interrupts implemented

Configuration

2.1 Location

This model's VLNV is mips.ovpworld.org/processor/mips64/1.0.

The model source is usually at:

\$IMPERAS_HOME/ImperasLib/source/mips.ovpworld.org/processor/mips64/1.0

The model binary is usually at:

\$IMPERAS_HOME/lib/\$IMPERAS_ARCH/ImperasLib/mips.ovpworld.org/processor/mips64/1.0

2.2 GDB Path

The default GDB for this model is: \$IMPERAS_HOME/lib/\$IMPERAS_ARCH/gdb/mips-sde-elf-gdb.

2.3 Semi-Host Library

The default semi-host library file is mips.ovpworld.org/semihosting/mips64Newlib/1.0

2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

2.6 Processor ELF code

The ELF code supported by this model is: 0x8.

All Variants in this model

This model has these variants

Variant	Description
P6600	
I6400	
MIPS64R6	(described in this document)
I6500	

Table 3.1: All Variants in this model

Bus Master Ports

This model has these bus master ports.

Name mir		max	Connect?	Description
INSTRUCTION	12	12 59 mandatory		
DATA	12	59	optional	

Table 4.1: Bus Master Ports

Bus Slave Ports

This model has no bus slave ports.

Net Ports

This model has these net ports.

Name	Type	Connect?	Description
reset	input	optional	CMP reset
dint	input	optional	Debug external interrupt
int0	input	optional	GIC external interrupt
int1	input	optional	GIC external interrupt
int2	input	optional	GIC external interrupt
int3	input	optional	GIC external interrupt
int4	input	optional	GIC external interrupt
int5	input	optional	GIC external interrupt
int6	input	optional	GIC external interrupt
int7	input	optional	GIC external interrupt
int8	input	optional	GIC external interrupt
int9	input	optional	GIC external interrupt
int10	input	optional	GIC external interrupt
int11	input	optional	GIC external interrupt
int12	input	optional	GIC external interrupt
int13	input	optional	GIC external interrupt
int14	input	optional	GIC external interrupt
int15	input	optional	GIC external interrupt
int16	input	optional	GIC external interrupt
int17	input	optional	GIC external interrupt
int18	input	optional	GIC external interrupt
int19	input	optional	GIC external interrupt
int20	input	optional	GIC external interrupt
int21	input	optional	GIC external interrupt
int22	input	optional	GIC external interrupt
int23	input	optional	GIC external interrupt
int24	input	optional	GIC external interrupt
int25	input	optional	GIC external interrupt
int26	input	optional	GIC external interrupt
int27	input	optional	GIC external interrupt
int28	input	optional	GIC external interrupt

int29	input	optional	GIC external interrupt
int30	input	optional	GIC external interrupt
int31	input	optional	GIC external interrupt
int32	input	optional	GIC external interrupt
int33	input	optional	GIC external interrupt
int34	input	optional	GIC external interrupt
int35	input	optional	GIC external interrupt
int36	input	optional	GIC external interrupt
int37	input	optional	GIC external interrupt
int38	input	optional	GIC external interrupt
int39	input	optional	GIC external interrupt
int40	input	optional	GIC external interrupt
int41	input	optional	GIC external interrupt
int42	input	optional	GIC external interrupt
int43	input	optional	GIC external interrupt
int44	input	optional	GIC external interrupt
int45	input	optional	GIC external interrupt
int46	input	optional	GIC external interrupt
int47	input	optional	GIC external interrupt
int48	input	optional	GIC external interrupt
int49	input	optional	GIC external interrupt
int50	input	optional	GIC external interrupt
int51	input	optional	GIC external interrupt
int52	input	optional	GIC external interrupt
int53	input	optional	GIC external interrupt
int54	input	optional	GIC external interrupt
int55	input	optional	GIC external interrupt
int56	input	optional	GIC external interrupt
int57	input	optional	GIC external interrupt
int58	input	optional	GIC external interrupt
int59	input	optional	GIC external interrupt
int60	input	optional	GIC external interrupt
int61	input	optional	GIC external interrupt
int62	input	optional	GIC external interrupt
int63	input	optional	GIC external interrupt
int64	input	optional	GIC external interrupt
int65	input	optional	GIC external interrupt
int66	input	optional	GIC external interrupt
int67	input	optional	GIC external interrupt
int68	input	optional	GIC external interrupt
int69	input	optional	GIC external interrupt
int70	input	optional	GIC external interrupt
int71	input	optional	GIC external interrupt
int72	input	optional	GIC external interrupt
int73	input	optional	GIC external interrupt
			-

int74	input	optional	GIC external interrupt
int75		optional	GIC external interrupt
int76	input	_	-
	input	optional	GIC external interrupt
int77	input	optional	GIC external interrupt
int78	input	optional	GIC external interrupt
int79	input	optional	GIC external interrupt
int80	input	optional	GIC external interrupt
int81	input	optional	GIC external interrupt
int82	input	optional	GIC external interrupt
int83	input	optional	GIC external interrupt
int84	input	optional	GIC external interrupt
int85	input	optional	GIC external interrupt
int86	input	optional	GIC external interrupt
int87	input	optional	GIC external interrupt
int88	input	optional	GIC external interrupt
int89	input	optional	GIC external interrupt
int90	input	optional	GIC external interrupt
int91	input	optional	GIC external interrupt
int92	input	optional	GIC external interrupt
int93	input	optional	GIC external interrupt
int94	input	optional	GIC external interrupt
int95	input	optional	GIC external interrupt
int96	input	optional	GIC external interrupt
int97	input	optional	GIC external interrupt
int98	input	optional	GIC external interrupt
int99	input	optional	GIC external interrupt
int100	input	optional	GIC external interrupt
int101	input	optional	GIC external interrupt
int102	input	optional	GIC external interrupt
int103	input	optional	GIC external interrupt
int104	input	optional	GIC external interrupt
int105	input	optional	GIC external interrupt
int106	input	optional	GIC external interrupt
int107	input	optional	GIC external interrupt
int108	input	optional	GIC external interrupt
int109	input	optional	GIC external interrupt
int110	input	optional	GIC external interrupt
int111	input	optional	GIC external interrupt
int112	input	optional	GIC external interrupt
int113	input	optional	GIC external interrupt
int114	input	optional	GIC external interrupt
int115	input	optional	GIC external interrupt
int116	input	optional	GIC external interrupt
int117	input	optional	GIC external interrupt
int118	input	optional	GIC external interrupt
1110110	լուբա	орионаг	OTO CAUGINAI IIIUGITUPU

	T		CTC
int119	input	optional	GIC external interrupt
int120	input	optional	GIC external interrupt
int121	input	optional	GIC external interrupt
int122	input	optional	GIC external interrupt
int123	input	optional	GIC external interrupt
int124	input	optional	GIC external interrupt
int125	input	optional	GIC external interrupt
int126	input	optional	GIC external interrupt
int127	input	optional	GIC external interrupt
ej_disable_probe_debug	input	optional	GIC ej_disable_probe_debug
ejtagbrk_override	input	optional	GIC ejtagbrk_override
ej_dint_in	input	optional	GIC ej_dint_in
GCR_CUSTOM_BASE	output	optional	Provides the least significant 32-bits of the value written to the GCR_CUSTOM_BASE register. Second half of GCR_CUSTOM_BASE_HI and GCR_CUSTOM_BASE output.
GCR_CUSTOM_BASE_UPPER	output	optional	Provides the most significant 32-bits of value written to the the GCR_CUSTOM_BASE register. First half of GCR_CUSTOM_BASE_HI and GCR_CUSTOM_BASE output.
dint_CPU0_VP0	input	optional	Debug external interrupt
hwint0_CPU0_VP0	input	optional	External interrupt
hwint1_CPU0_VP0	input	optional	External interrupt
hwint2_CPU0_VP0	input	optional	External interrupt
hwint3_CPU0_VP0	input	optional	External interrupt
hwint4_CPU0_VP0	input	optional	External interrupt
hwint5_CPU0_VP0	input	optional	External interrupt
nmi_CPU0_VP0	input	optional	Non-maskable external interrupt
EICPresent_CPU0_VP0	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU0_VP0	input	optional	External interrupt controller RIPL (alias
			of hwint0 - 5 or 7)
EIC_EICSS_CPU0_VP0	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU0_VP0	input	optional	External interrupt controller vector num-
			ber
EIC_VectorOffset_CPU0_VP0	input	optional	External interrupt controller vector offset
EIC_GID_CPU0_VP0	input	optional	External interrupt controller guest ID
intISS_CPU0_VP0	output	optional	True when interrupt request is serviced
causeTI_CPU0_VP0	output	optional	True when timer interrupt expires
causeIP0_CPU0_VP0	output	optional	Raised for software interrupt request IP0
causeIP1_CPU0_VP0	output	optional	Raised for software interrupt request IP1
si_sleep_CPU0_VP0	output	optional	True when the VPE is in WAIT state
hwint0	input	optional	External interrupt for compatibility
L			,

vc_run_CPU0_VP0	innut	ontional	Set to force stop of execution on processor
VC_run_CPUU_VPU	input	optional	
Cuest EIC DIDL CDIIO VDO	instant	on4: 1	VPE (simulation control only)
Guest.EIC_RIPL_CPU0_VP0	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU0_VP0	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU0_VP0	input	optional	Guest External interrupt controller vector
G + BIG H + Off + CDHO HBO			number
Guest.EIC_VectorOffset_CPU0_VP0	input	optional	Guest External interrupt controller vector
			offset
Guest.EIC_GID_CPU0_VP0	input	optional	Guest External interrupt controller guest
G IIGG CDIIO IVDO			ID
Guest.intISS_CPU0_VP0	output	optional	True when Guest interrupt request is ser-
			viced
Guest.causeTI_CPU0_VP0	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU0_VP0	output	optional	Raised for Guest software interrupt re-
			quest IP0
Guest.causeIP1_CPU0_VP0	output	optional	Raised for Guest software interrupt re-
			quest IP1
dint_CPU0_VP1	input	optional	Debug external interrupt
hwint0_CPU0_VP1	input	optional	External interrupt
hwint1_CPU0_VP1	input	optional	External interrupt
hwint2_CPU0_VP1	input	optional	External interrupt
hwint3_CPU0_VP1	input	optional	External interrupt
hwint4_CPU0_VP1	input	optional	External interrupt
hwint5_CPU0_VP1	input	optional	External interrupt
nmi_CPU0_VP1	input	optional	Non-maskable external interrupt
EICPresent_CPU0_VP1	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU0_VP1	input	optional	External interrupt controller RIPL (alias
			of hwint0 - 5 or 7)
EIC_EICSS_CPU0_VP1	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU0_VP1	input	optional	External interrupt controller vector num-
			ber
EIC_VectorOffset_CPU0_VP1	input	optional	External interrupt controller vector offset
EIC_GID_CPU0_VP1	input	optional	External interrupt controller guest ID
intISS_CPU0_VP1	output	optional	True when interrupt request is serviced
causeTI_CPU0_VP1	output	optional	True when timer interrupt expires
causeIP0_CPU0_VP1	output	optional	Raised for software interrupt request IP0
causeIP1_CPU0_VP1	output	optional	Raised for software interrupt request IP1
si_sleep_CPU0_VP1	output	optional	True when the VPE is in WAIT state
vc_run_CPU0_VP1	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)
Guest.EIC_RIPL_CPU0_VP1	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU0_VP1	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU0_VP1	input	optional	Guest External interrupt controller vector
	-	=	number
Guest.EIC_VectorOffset_CPU0_VP1	input	optional	Guest External interrupt controller vector
		-	offset

Guest.EIC_GID_CPU0_VP1	input	optional	Guest External interrupt controller guest ID
Guest.intISS_CPU0_VP1	output	ontional	True when Guest interrupt request is ser-
Guest.IIIt155_CF 00_VF1	output	optional	viced
Guest.causeTI_CPU0_VP1	output	optional	True when Guest timer interrupt expires
Guest.causeIPO_CPUO_VP1		optional	Raised for Guest software interrupt re-
	output	_	quest IP0
Guest.causeIP1_CPU0_VP1	output	optional	Raised for Guest software interrupt request IP1
dint_CPU0_VP2	input	optional	Debug external interrupt
hwint0_CPU0_VP2	input	optional	External interrupt
hwint1_CPU0_VP2	input	optional	External interrupt
hwint2_CPU0_VP2	input	optional	External interrupt
hwint3_CPU0_VP2	input	optional	External interrupt
hwint4_CPU0_VP2	input	optional	External interrupt
hwint5_CPU0_VP2	input	optional	External interrupt
nmi_CPU0_VP2	input	optional	Non-maskable external interrupt
EICPresent_CPU0_VP2	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU0_VP2	input	optional	External interrupt controller RIPL (alias
	_	_	of hwint0 - 5 or 7)
EIC_EICSS_CPU0_VP2	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU0_VP2	input	optional	External interrupt controller vector num-
			ber
EIC_VectorOffset_CPU0_VP2	input	optional	External interrupt controller vector offset
EIC_GID_CPU0_VP2	input	optional	External interrupt controller guest ID
intISS_CPU0_VP2	output	optional	True when interrupt request is serviced
causeTI_CPU0_VP2	output	optional	True when timer interrupt expires
causeIP0_CPU0_VP2	output	optional	Raised for software interrupt request IP0
causeIP1_CPU0_VP2	output	optional	Raised for software interrupt request IP1
si_sleep_CPU0_VP2	output	optional	True when the VPE is in WAIT state
vc_run_CPU0_VP2	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)
Guest.EIC_RIPL_CPU0_VP2	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU0_VP2	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU0_VP2	input	optional	Guest External interrupt controller vector
			number
Guest.EIC_VectorOffset_CPU0_VP2	input	optional	Guest External interrupt controller vector offset
Guest.EIC_GID_CPU0_VP2	input	optional	Guest External interrupt controller guest ID
Guest.intISS_CPU0_VP2	output	optional	True when Guest interrupt request is serviced
Guest.causeTI_CPU0_VP2	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU0_VP2	output	optional	Raised for Guest software interrupt re-
	•	•	quest IP0

G , ID1 GDIJO IJD0			
Guest.causeIP1_CPU0_VP2	output	optional	Raised for Guest software interrupt re-
II - ODII - IIDo			quest IP1
dint_CPU0_VP3	input	optional	Debug external interrupt
hwint0_CPU0_VP3	input	optional	External interrupt
hwint1_CPU0_VP3	input	optional	External interrupt
hwint2_CPU0_VP3	input	optional	External interrupt
hwint3_CPU0_VP3	input	optional	External interrupt
hwint4_CPU0_VP3	input	optional	External interrupt
hwint5_CPU0_VP3	input	optional	External interrupt
nmi_CPU0_VP3	input	optional	Non-maskable external interrupt
EICPresent_CPU0_VP3	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU0_VP3	input	optional	External interrupt controller RIPL (alias
			of hwint0 - 5 or 7)
EIC_EICSS_CPU0_VP3	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU0_VP3	input	optional	External interrupt controller vector num-
	_		ber
EIC_VectorOffset_CPU0_VP3	input	optional	External interrupt controller vector offset
EIC_GID_CPU0_VP3	input	optional	External interrupt controller guest ID
intISS_CPU0_VP3	output	optional	True when interrupt request is serviced
causeTI_CPU0_VP3	output	optional	True when timer interrupt expires
causeIP0_CPU0_VP3	output	optional	Raised for software interrupt request IP0
causeIP1_CPU0_VP3	output	optional	Raised for software interrupt request IP1
si_sleep_CPU0_VP3	output	optional	True when the VPE is in WAIT state
vc_run_CPU0_VP3	input	optional	Set to force stop of execution on processor
		* F *	VPE (simulation control only)
Guest.EIC_RIPL_CPU0_VP3	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU0_VP3	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU0_VP3	input	optional	Guest External interrupt controller vector
	inp ac	орогона	number
Guest.EIC_VectorOffset_CPU0_VP3	input	optional	Guest External interrupt controller vector
Guesti.Ele_vectoronset_er co_vr s	Impat	орионаг	offset
Guest.EIC_GID_CPU0_VP3	input	optional	Guest External interrupt controller guest
Guesti.Ele_Gib_el ee_vi e	input	optional	ID
Guest.intISS_CPU0_VP3	output	optional	True when Guest interrupt request is ser-
Guestinitiss_Cr CO_Vr 5	Output	орионаг	viced
Guest.causeTI_CPU0_VP3	output	optional	True when Guest timer interrupt expires
Guest.causeIPC_CPU0_VP3	output	optional	Raised for Guest software interrupt re-
Guest.causer U_OL UU_VI 3	Ծաւթա	орионаг	quest IP0
Guest.causeIP1_CPU0_VP3	output	optional	Raised for Guest software interrupt re-
Guest.causen 1_O1 UU_V1 5	Ծաւթաւ	opuonai	quest IP1
dint_CPU1_VP0	innut	ontional	Debug external interrupt
hwint0_CPU1_VP0	input	optional	External interrupt
hwint1_CPU1_VP0	input	optional	-
	input	optional	External interrupt
hwint2_CPU1_VP0	input	optional	External interrupt
hwint3_CPU1_VP0	input	optional	External interrupt

hwint4_CPU1_VP0	input	optional	External interrupt
hwint5_CPU1_VP0	input	optional	External interrupt
nmi_CPU1_VP0	input	optional	Non-maskable external interrupt
EICPresent_CPU1_VP0	input	optional	Input signal SLEICPresent per VPE
EIC_RIPL_CPU1_VP0	input	optional	External interrupt controller RIPL (alias
	1	•	of hwint0 - 5 or 7)
EIC_EICSS_CPU1_VP0	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU1_VP0	input	optional	External interrupt controller vector num-
	_		ber
EIC_VectorOffset_CPU1_VP0	input	optional	External interrupt controller vector offset
EIC_GID_CPU1_VP0	input	optional	External interrupt controller guest ID
intISS_CPU1_VP0	output	optional	True when interrupt request is serviced
causeTI_CPU1_VP0	output	optional	True when timer interrupt expires
causeIP0_CPU1_VP0	output	optional	Raised for software interrupt request IP0
causeIP1_CPU1_VP0	output	optional	Raised for software interrupt request IP1
si_sleep_CPU1_VP0	output	optional	True when the VPE is in WAIT state
vc_run_CPU1_VP0	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)
Guest.EIC_RIPL_CPU1_VP0	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU1_VP0	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU1_VP0	input	optional	Guest External interrupt controller vector
			number
Guest.EIC_VectorOffset_CPU1_VP0	input	optional	Guest External interrupt controller vector
			offset
Guest.EIC_GID_CPU1_VP0	input	optional	Guest External interrupt controller guest
			ID
Guest.intISS_CPU1_VP0	output	optional	True when Guest interrupt request is ser-
			viced
Guest.causeTI_CPU1_VP0	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU1_VP0	output	optional	Raised for Guest software interrupt re-
G IDI GDIH IVD			quest IP0
Guest.causeIP1_CPU1_VP0	output	optional	Raised for Guest software interrupt re-
l' - ODIII VD1	. ,	. 1	quest IP1
dint_CPU1_VP1	input	optional	Debug external interrupt
hwint0_CPU1_VP1	input	optional	External interrupt
hwint1_CPU1_VP1	input	optional	External interrupt
hwint2_CPU1_VP1	input	optional	External interrupt
hwint3_CPU1_VP1 hwint4_CPU1_VP1	input	optional	External interrupt
hwint4_CPU1_VP1 hwint5_CPU1_VP1	input	optional	External interrupt
	input	optional	External interrupt
nmi_CPU1_VP1	input	optional	Non-maskable external interrupt
EICPresent_CPU1_VP1	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU1_VP1	input	optional	External interrupt controller RIPL (alias
EIC_EICSS_CPU1_VP1	innut	ontional	of hwint0 - 5 or 7) External interrupt controller EICSS
EIO-EIOSS-OFUI-VFI	input	optional	External interrupt controller EIC55

EIC_VectorNum_CPU1_VP1	input	optional	External interrupt controller vector num-
			ber
EIC_VectorOffset_CPU1_VP1	input	optional	External interrupt controller vector offset
EIC_GID_CPU1_VP1	input	optional	External interrupt controller guest ID
intISS_CPU1_VP1	output	optional	True when interrupt request is serviced
causeTI_CPU1_VP1	output	optional	True when timer interrupt expires
causeIP0_CPU1_VP1	output	optional	Raised for software interrupt request IP0
causeIP1_CPU1_VP1	output	optional	Raised for software interrupt request IP1
si_sleep_CPU1_VP1	output	optional	True when the VPE is in WAIT state
vc_run_CPU1_VP1	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)
Guest.EIC_RIPL_CPU1_VP1	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU1_VP1	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU1_VP1	input	optional	Guest External interrupt controller vector
			number
Guest.EIC_VectorOffset_CPU1_VP1	input	optional	Guest External interrupt controller vector
			offset
Guest.EIC_GID_CPU1_VP1	input	optional	Guest External interrupt controller guest
			ID
Guest.intISS_CPU1_VP1	output	optional	True when Guest interrupt request is ser-
	_	-	viced
Guest.causeTI_CPU1_VP1	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU1_VP1	output	optional	Raised for Guest software interrupt re-
	_	-	quest IP0
Guest.causeIP1_CPU1_VP1	output	optional	Raised for Guest software interrupt re-
		_	quest IP1
dint_CPU1_VP2	input	optional	Debug external interrupt
hwint0_CPU1_VP2	input	optional	External interrupt
hwint1_CPU1_VP2	input	optional	External interrupt
hwint2_CPU1_VP2	input	optional	External interrupt
hwint3_CPU1_VP2	input	optional	External interrupt
hwint4_CPU1_VP2	input	optional	External interrupt
hwint5_CPU1_VP2	input	optional	External interrupt
nmi_CPU1_VP2	input	optional	Non-maskable external interrupt
EICPresent_CPU1_VP2	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU1_VP2	input	optional	External interrupt controller RIPL (alias
	_	•	of hwint0 - 5 or 7)
EIC_EICSS_CPU1_VP2	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU1_VP2	input	optional	External interrupt controller vector num-
	•	1	ber
EIC_VectorOffset_CPU1_VP2	input	optional	External interrupt controller vector offset
EIC_GID_CPU1_VP2	input	optional	External interrupt controller guest ID
intISS_CPU1_VP2	output	optional	True when interrupt request is serviced
causeTLCPU1_VP2	output	optional	True when timer interrupt expires
causeIP0_CPU1_VP2	output	optional	Raised for software interrupt request IP0
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causeIP1_CPU1_VP2	output	optional	Raised for software interrupt request IP1
si_sleep_CPU1_VP2			True when the VPE is in WAIT state
vc_run_CPU1_VP2	output	optional	
VC_FUII_CPUI_VP2	input	optional	Set to force stop of execution on processor VPE (simulation control only)
Guest.EIC_RIPL_CPU1_VP2	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU1_VP2	_		Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU1_VP2	input	optional	Guest External interrupt controller vector
Guest.ETC_vectorNum_CF01_vF2	input	optional	number
Guest.EIC_VectorOffset_CPU1_VP2	input	optional	Guest External interrupt controller vector
Guest.Ero_vectoronset_or or_vr2	Input	орионаг	offset
Guest.EIC_GID_CPU1_VP2	input	optional	Guest External interrupt controller guest
ducst. Die die die view 2	Impat	орионаг	ID
Guest.intISS_CPU1_VP2	output	optional	True when Guest interrupt request is ser-
	output	орионаг	viced
Guest.causeTI_CPU1_VP2	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU1_VP2	output	optional	Raised for Guest software interrupt re-
		1	quest IP0
Guest.causeIP1_CPU1_VP2	output	optional	Raised for Guest software interrupt re-
		•	quest IP1
dint_CPU1_VP3	input	optional	Debug external interrupt
hwint0_CPU1_VP3	input	optional	External interrupt
hwint1_CPU1_VP3	input	optional	External interrupt
hwint2_CPU1_VP3	input	optional	External interrupt
hwint3_CPU1_VP3	input	optional	External interrupt
hwint4_CPU1_VP3	input	optional	External interrupt
hwint5_CPU1_VP3	input	optional	External interrupt
nmi_CPU1_VP3	input	optional	Non-maskable external interrupt
EICPresent_CPU1_VP3	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU1_VP3	input	optional	External interrupt controller RIPL (alias
			of hwint0 - 5 or 7)
EIC_EICSS_CPU1_VP3	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU1_VP3	input	optional	External interrupt controller vector num-
			ber
EIC_VectorOffset_CPU1_VP3	input	optional	External interrupt controller vector offset
EIC_GID_CPU1_VP3	input	optional	External interrupt controller guest ID
intISS_CPU1_VP3	output	optional	True when interrupt request is serviced
causeTI_CPU1_VP3	output	optional	True when timer interrupt expires
causeIP0_CPU1_VP3	output	optional	Raised for software interrupt request IP0
causeIP1_CPU1_VP3	output	optional	Raised for software interrupt request IP1
si_sleep_CPU1_VP3	output	optional	True when the VPE is in WAIT state
vc_run_CPU1_VP3	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)
Guest.EIC_RIPL_CPU1_VP3	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU1_VP3	input	optional	Guest External interrupt controller EICSS

Guest.EIC_VectorNum_CPU1_VP3	input	optional	Guest External interrupt controller vector
			number
Guest.EIC_VectorOffset_CPU1_VP3	input	optional	Guest External interrupt controller vector
			offset
Guest.EIC_GID_CPU1_VP3	input	optional	Guest External interrupt controller guest
			ID
Guest.intISS_CPU1_VP3	output	optional	True when Guest interrupt request is ser-
			viced
Guest.causeTI_CPU1_VP3	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU1_VP3	output	optional	Raised for Guest software interrupt re-
			quest IP0
Guest.causeIP1_CPU1_VP3	output	optional	Raised for Guest software interrupt re-
			quest IP1

Table 6.1: Net Ports

FIFO Ports

This model has no FIFO ports.

Formal Parameters

Name	Type	Description
variant	Enumeration	Processor variant
endian	Endian	Model endian
cacheenable	Enumeration	Select cache model mode (default, tag or full)
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info structure
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for AVP test termination)
cache Index By pass TLB	Boolean	When set, cache index ops do not generate TLB exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
gprNames	Boolean	Disassemble the register names from the default ABI instead of register numbers for MIPS-format trace output
supervisorMode	Boolean	Override whether processor implements supervisor mode
busErrors	Boolean	Override bus error exception behavior. When true, accesses of memory not defined by platform will cause bus error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when true (sets Config.MT=3, Config.KU/K23=2 and Config1.MMUSizeM1=0)
${\it fixedDbgRegSize}$	Boolean	Enable applications to debug on P5600 with GDB version 2015.06-05 and prior
removeDSP	Boolean	Override the DSP-present configuration when true (sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true (sets Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true (sets Config1.FP to 0)
removeFTLB	Boolean	Override the FTLBEn configuration when true (disable FTLB)
isISA	Boolean	Enable to specify ISA model (reset address from ELF, all coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to maximum value to improve performance
perfCounters	Uns32	Performance Counters
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores only)

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ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC
IMODINOD	TT 00	implementation (MT cores only)
ITCFIFODepth	Uns32	Specify ITC FIFO cell depth. By default supports
		4.
ITCEmptyOnReset	Boolean	Specify ITC E/F cells reset to a known empty state.
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior,
		2:new mttc1 behavior)
supportDenormals	Boolean	Enable to specify that the FPU supports denormal
		operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0. Ig-
		nored if less than two VPEs configured.
VPE1MaxTC	Uns32	Specifies the maximum TCs initially on VPE1. Ig-
		nored if less than three VPEs configured.
segBits	Uns32	Override the number of address bits implemented
508210	011002	for 64 bit segments (MIPS64 Only)
mpuRegions	Uns32	Number of regions for memory protection unit
mpuType	Uns32	Type of MPU implementation
mpuEnable	Boolean	Enable MPU2 segment control at reset
mpuSegment0	Uns32	Attributes for segment 0 in MPU2 SegmentCon-
		trol_0 register
mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentCon-
		trol_0 register
mpuSegment2	Uns32	Attributes for segment 2 in MPU2 SegmentCon-
		trol_0 register
mpuSegment3	Uns32	Attributes for segment 3 in MPU2 SegmentCon-
		trol_0 register
mpuSegment4	Uns32	Attributes for segment 4 in MPU2 SegmentCon-
		trol_1 register
mpuSegment5	Uns32	Attributes for segment 5 in MPU2 SegmentCon-
		trol_1 register
mpuSegment6	Uns32	Attributes for segment 6 in MPU2 SegmentCon-
		trol_1 register
mpuSegment7	Uns32	Attributes for segment 7 in MPU2 SegmentCon-
•		trol_1 register
mpuSegment8	Uns32	Attributes for segment 8 in MPU2 SegmentCon-
		trol_2 register
mpuSegment9	Uns32	Attributes for segment 9 in MPU2 SegmentCon-
inp ac eginenee	011302	trol_2 register
mpuSegment10	Uns32	Attributes for segment 10 in MPU2 SegmentCon-
inpusegment to	0.11502	trol_2 register
mpuSegment11	Uns32	Attributes for segment 11 in MPU2 SegmentCon-
inpusegment11	011852	trol_2 register
mpuSegment12	IIma 20	Attributes for segment 12 in MPU2 SegmentCon-
mpusegment12	Uns32	
	TT 00	trol-3 register
mpuSegment13	Uns32	Attributes for segment 13 in MPU2 SegmentCon-
9 114	77 00	trol_3 register
mpuSegment14	Uns32	Attributes for segment 14 in MPU2 SegmentCon-
~		trol_3 register
mpuSegment15	Uns32	Attributes for segment 15 in MPU2 SegmentCon-
		trol_3 register
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
tcDisable	Uns32	Number of disabled TCs
vpeDisable	Uns32	Number of disabled VPEs
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
		<u> </u>

mvpconf1c1f	Boolean	Override MVPConf.C1F
mvpcontrolPolicyMode	Boolean	Override MVPControl.POLICY_MODE
hasFDC	Uns32	Specify the size of Fast Debug Channel register
hasi bo	011502	block
licenseWarningDays	Uns32	Specify the number of days before a license expires
		to start issuing a warning. 0 disables warnings.
MIPS_UHI	Boolean	Enable MIPS-Unified Hosting interface
mipsUhiArgs	String	Specifies UHI arguments string separated by spaces
mipsUhiJail	String	Specifies UHI jailroot
MIPS_DV_MODE	Boolean	Enable Design Verification mode
MIPS_MAGIC_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes
enableTrickbox	Boolean	Enable trickbox addresses (specific for AVP)
fpuexcdisable	Boolean	Disable FPU exceptions
TRU_PRESENT	Boolean	Disable or Enable based on TRU presence to con-
		trol certain fields (e.x.perfCtl.PCTD
ucLLwordsLocked	Uns32	Numbers of words (4 byte) an uncached LL is lock-
		ing. Maximum: 4K
FUSA	Boolean	Enable Functional Safety
CPC_FAULT_SUPPORTED	Uns32	Specify the value for Functional Safety Supported
		register
CPC_FAULT_ENABLE	Uns32	Specify the value for Functional Safety Enable reg-
		ister
cop2Bits	Uns32	Specifies width in bits of COP2 registers (32 or 64)
cop2FileName	String	Specifies COP2 dynamically-loaded object
		(.so/.dll) defining COP2 instructions
udiConfig	Int32	Specifies UDI configuration attribute
udiFileName	String	Specifies UDI dynamically-loaded object (.so/.dll)
		defining UDI instructions
vectoredinterrupt	Boolean	Enables vectored interrupts (sets Config3 VInt)
externalinterrupt	Boolean	Enables the use of an external interrupt controller
		(sets Config3 VEIC)
config3VEIC_VPE0	Boolean	Enables an external interrupt controller on VPE0
		(sets Config3 VEIC)
config3VEIC_VPE1	Boolean	Enables an external interrupt controller on VPE1
		(sets Config3 VEIC)
config3VEIC_VPE2	Boolean	Enables an external interrupt controller on VPE2
		(sets Config3 VEIC)
config3VEIC_VPE3	Boolean	Enables an external interrupt controller on VPE3
		(sets Config3 VEIC)
rootFixedMMU	Boolean	Override the root MMU type to fixed map-
		ping when true (sets Config.MT=3 and Con-
ADDITIO: DAI	11 00	fig.KU/K23=2)
${ m rootMMUSizeM1}$	Uns32	Override the root MMUSizeM1 field in Config1 reg-
	IT 90	ister (number of MMU entries-1)
srsctlHSS	Uns32	Override the HSS field in SRSCtl register (number
fDC	IT 90	of shadow register sets)
firPS	Uns32	Override the PS field in FIR register
firHas2008	Uns32	Override the Has2008 field in FIR register
usePreciseFpu	Uns32	Use the precise Floating Point emulation
simulateLite	Enumeration	Run Simulation with optimization. There are
		several optimizations which coule be combined
nridCompanyOptions	Uns32	(NONE, FS, MA or FSMA) Override the Company Options field in PRId reg-
pridCompanyOptions	Ulisaz	override the Company Options field in PRId register
pridRevision	Uns32	Override the Revision field in PRId register
pridrevision	UIIS52	Override the revision held in Prid register

globalClusterNum	Uns32	Override the ClusterNum field in GlobalNumber
		register
intctlIPTI	Uns32	Override the IPTI field in IntCtl register
intctlIPFDC	Uns32	Override the IPFDC field in IntCtl register
intetlIPPCI	Uns32	Override the IPPCI field in IntCtl register
numWatch	Uns32	Specify number of WatchLo/WatchHi register pairs
maxVP	Uns32	Specify maximum number of Virtual Processors present in a core
numVP	Uns32	Specify number of Virtual Processors to be present
numVPtoStart	Uns32	Specify number of Virtual Processors to be started
sharedTLBindex	Uns32	Specify first shared TLB Index between Virtual Cores
xconfigSpecified	Boolean	True if the configuration comes from a valid xconfig file
intctlIPTI_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
intctlIPTI_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
intctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
intctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
intctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
intctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
intctlIPTI_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
intctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
intctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
intctlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
intctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
intctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
intctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
intctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
intctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
intctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
intctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
intctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
intctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
intctlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
intctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0

intctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for
		CPU5/VP1
intctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
intctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
intctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
intctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
intctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
intctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
intctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
intctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
intctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
intctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
intetlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
intctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
intctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
intetlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
intctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
intetlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
intctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
intetlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
intctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0
intctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
intctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
intetlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
intctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
intetlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
intctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
intctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
intctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0

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intctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1
intctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
intctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
intctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
intctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
intctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
intctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
intctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
intctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
intctlIPFDC_CPU6_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2
intctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
intctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
intctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
intctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
intctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
intetlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
intetlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
intctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
intctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
intctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0
intctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP1
intctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
intctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
intctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
intctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
intctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
intctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
intctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0

intctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1
intctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP2
intctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
intctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
intctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
intctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
intctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
intctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0
intctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1
intctlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2
intctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
intctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
intctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP1
intctlIPPCI_CPU6_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP2
intctlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
intctlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
intctlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
intctlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
intctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
segcfg0PA	Uns32	Set CFG0.PA field of SegCtl0 register
segcfg1PA	Uns32	Set CFG1.PA field of SegCtl0 register
segcfg2PA	Uns32	Set CFG2.PA field of SegCtl1 register
segcfg3PA	Uns32	Set CFG3.PA field of SegCtl1 register
segcfg4PA	Uns32	Set CFG4.PA field of SegCtl2 register
segcfg5PA	Uns32	Set CFG5.PA field of SegCtl2 register
segcfg0AM	Uns32	Set CFG0.AM field of SegCtl0 register
segcfg1AM	Uns32	Set CFG1.AM field of SegCtl0 register
segcfg2AM	Uns32	Set CFG2.AM field of SegCtl1 register
segcfg3AM	Uns32	Set CFG3.AM field of SegCtl1 register
segcfg4AM	Uns32	Set CFG4.AM field of SegCtl2 register
segcfg5AM	Uns32	Set CFG5.AM field of SegCtl2 register
segcfg0EU	Uns32	Set CFG0.EU field of SegCtl0 register
segcfg1EU	Uns32	Set CFG1.EU field of SegCtl0 register
segcfg2EU	Uns32	Set CFG2.EU field of SegCtl1 register
segcfg3EU	Uns32	Set CFG3.EU field of SegCtl1 register
segcfg4EU	Uns32	Set CFG4.EU field of SegCtl2 register
segcfg5EU	Uns32	Set CFG5.EU field of SegCtl2 register
	0.11502	TO THE PARTY OF SUSPENSE TO SERVICE

	Set CFG0.C field of SegCtl0 register
	Set CFG1.C field of SegCtl0 register
	Set CFG2.C field of SegCtl1 register
Uns32	Set CFG3.C field of SegCtl1 register
Uns32	Set CFG4.C field of SegCtl2 register
Uns32	Set CFG5.C field of SegCtl2 register
Uns32	Override the cdmmsize reset value
Uns32	Enables R6 support
Uns32	Override the BM field in Config register (burst
	mode)
Boolean	Override Config.DSP (data scratchpad RAM
	present)
Boolean	Override Config.ISP (instruction scratchpad RAM
	present)
Uns32	Override power on value of Config.K0 (set Kseg0
	cacheability)
Uns32	Override power on value of Config.KU (set Useg
011502	cacheability)
Uns32	Override power on value of Config.K23 (set Kseg23
011502	cacheability)
Boolean	Override Config.MDU (iterative multiply/divide
Boolean	unit)
Boolean	Override Config.MM (merging mode for write)
	Override Config.MT
	Override Config.SB (simple bus transfers only)
	Override Config.BCP (Buffer Cache Present)
	Override Config. CA (enables the MIPS16e ASE)
	Override Config1.DA (Deache associativity)
	Override Config1.DL (Deache line size)
	Override Config1.DL (Deache line size) Override Config1.DS (Deache sets per way)
	Override Config1.EP (EJTag present)
	Override Config1.IA (Icache associativity)
	Override Config1.IL (Icache line size)
	Override Config1.IS (Icache sets per way)
Uns32	Override Config1.MMUSizeM1 (number of MMU
11 00	entries-1)
	Override Config1.MMUSizeM1 for VPE1
	Override Config1.MMUSizeM1 for VPE2
	Override Config1.MMUSizeM1 for VPE3
Boolean	Override Config1.WR (watchpoint registers
<u> </u>	present)
Boolean	Override Config1.PC (Performance Counters
	present)
	Override Config1.C2 (Coprocessor 2 present)
	Override the SU field in Config2 register
	Override the SS field in Config2 register
Uns32	
Uns32	Override the SL field in Config2 register
Uns32 Uns32	Override the SL field in Config2 register Override the SA field in Config2 register
Uns32 Uns32 Boolean	Override the SL field in Config2 register Override the SA field in Config2 register Override Config3.BI
Uns32 Uns32 Boolean Boolean	Override the SL field in Config2 register Override the SA field in Config2 register Override Config3.BI Override Config3.BP
Uns32 Uns32 Boolean Boolean Boolean	Override the SL field in Config2 register Override the SA field in Config2 register Override Config3.BI Override Config3.BP Override Config3.CDMM
Uns32 Uns32 Boolean Boolean Boolean Boolean	Override the SL field in Config2 register Override the SA field in Config2 register Override Config3.BI Override Config3.BP Override Config3.CDMM Override Config3.CTXTC
Uns32 Uns32 Boolean Boolean Boolean	Override the SL field in Config2 register Override the SA field in Config2 register Override Config3.BI Override Config3.BP Override Config3.CDMM
Uns32 Uns32 Boolean Boolean Boolean Boolean	Override the SL field in Config2 register Override the SA field in Config2 register Override Config3.BI Override Config3.BP Override Config3.CDMM Override Config3.CTXTC
Uns32 Uns32 Boolean Boolean Boolean Boolean Boolean	Override the SL field in Config2 register Override the SA field in Config2 register Override Config3.BI Override Config3.BP Override Config3.CDMM Override Config3.CTXTC Override Config3.DSPP
	Uns32

config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3ITL	Boolean	Override Config3.ITL
config3LPA	Boolean	Override Config3.LPA
config3MCU	Boolean	Override Config3.MCU
config3MMAR	Uns32	Override Config3.MMAR
config3RXI	Boolean	Override Config3.RXI
config3SC	Boolean	Override Config3.SC
config3ULRI	Boolean	Override Config3.ULRI
config3VZ	Boolean	Override Config3.VZ
config3MSAP	Boolean	Override Config3.MSAP
config3CMGCR	Boolean	Override the CMGCR field in Config3 register
config3SP	Boolean	Override the SP field in Config3 register
config3TL	Uns32	Override the TL field in Config3 register
config3PW	Boolean	Override the PW field in Config3 register
config4AE	Boolean	Override Config4.AE
config4IE	Uns32	Override Config4.IE
config4MMUConfig	Uns32	Override Config 4.MMUConfig field (interpretation
Comigativity Comig	011302	depends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.With ExtDer Override Config4.VTLBSizeExt
config4V1LBSizeExt config4KScrExist		Override Config4.V1LBSizeExt Override Config4.KScrExist
	Uns32	9
config5EVA	Boolean	Override Config5.EVA
config5LLB	Boolean	Override Config5.LLB (LLAddr supports LLbit)
config5MRP	Boolean	Override Config5.MRP (MaaR Present)
config5NFExists	Boolean	Override Config5.NFExists
mips32Macro	Boolean	Enables the MIPS32 SAVE and RESTORE macro
		instructions. Ignored if Config5.CA2 is not set)
config5MSAEn	Boolean	Override Config5.MSAEn
config5MVH	Boolean	Override Config5.MVH (enable MTHC0 and
		MFHC0 instructions)
config5DEC	Boolean	Override Config5.DEC (to test Dual Endian Capa-
		bility)
config5GI	Uns32	Override Config5.GI (enable GINV)
config5CRCP	Boolean	Override Config5.CRCP (CRCP Present)
config5VP	Boolean	Override Config5.VP
config6FTLBEn	Boolean	Override power on value of Config6.FTLBEn
config7AR	Boolean	Override Config7.AR (Alias removed Data cache)
config7DCIDX_MODE	Uns32	Override Config7.DCIDX_MODE
config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initializa-
		tion)
config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction
0011119	Boolean	cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)
config7ES	Uns32	Override the ES field in Config7 register (External-
Comigres	011302	ize sync)
config7WR	Boolean	Override Config7[31] bit (Alternative implementa-
comig/ wit	Doolean	tion of Watch registers)
config7FPR		Override Config7.FPR (one-half FPU clock ratio)
	Booloom	TO A CONTRACT OF A LANGE TO THE PROPERTY OF TH
aonfig7IICD	Boolean	
config7USP	Uns32	Override Config7.USP (USPRAM enable)
config7BTLM	Uns32 Boolean	Override Config7.USP (USPRAM enable) Override Config7.BTLM bit
config7BTLM config7BusSlp	Uns32 Boolean Boolean	Override Config7.USP (USPRAM enable) Override Config7.BTLM bit Override Config7.BusSlp bit
config7BTLM config7BusSlp config7IVAD	Uns32 Boolean Boolean Boolean	Override Config7.USP (USPRAM enable) Override Config7.BTLM bit Override Config7.BusSlp bit Override Config7.IVAD bit
config7BTLM config7BusSlp config7IVAD config7RPS	Uns32 Boolean Boolean Boolean Boolean	Override Config7.USP (USPRAM enable) Override Config7.BTLM bit Override Config7.BusSlp bit Override Config7.IVAD bit Override Config7.RPS bit
config7BTLM config7BusSlp config7IVAD config7RPS config7IAR_CPU0_VPE0	Uns32 Boolean Boolean Boolean Boolean Boolean Boolean	Override Config7.USP (USPRAM enable) Override Config7.BTLM bit Override Config7.BusSlp bit Override Config7.IVAD bit Override Config7.RPS bit Override Config7.IAR bit for CPU0/VPE0
config7BTLM config7BusSlp config7IVAD config7RPS	Uns32 Boolean Boolean Boolean Boolean	Override Config7.USP (USPRAM enable) Override Config7.BTLM bit Override Config7.BusSlp bit Override Config7.IVAD bit Override Config7.RPS bit

config7IAR_CPU0_VPE3	Boolean	Override Config7.IAR bit for CPU0/VPE3
config7IAR_CPU1_VPE0	Boolean	Override Config7.IAR bit for CPU1/VPE0
config7IAR_CPU1_VPE1	Boolean	Override Config7.IAR bit for CPU1/VPE1
config7IAR_CPU1_VPE2	Boolean	Override Config7.IAR bit for CPU1/VPE2
config7IAR_CPU1_VPE3	Boolean	Override Config7.IAR bit for CPU1/VPE3
config7IAR_CPU2_VPE0	Boolean	Override Config7.IAR bit for CPU2/VPE0
config7IAR_CPU2_VPE1	Boolean	Override Config7.IAR bit for CPU2/VPE1
config7IAR_CPU2_VPE2	Boolean	Override Config7.IAR bit for CPU2/VPE2
config7IAR_CPU2_VPE3	Boolean	Override Config7.IAR bit for CPU2/VPE3
config7IAR_CPU3_VPE0	Boolean	Override Config7.IAR bit for CPU3/VPE0
config7IAR_CPU3_VPE1	Boolean	Override Config7.IAR bit for CPU3/VPE1
config7IAR_CPU3_VPE2	Boolean	Override Config7.IAR bit for CPU3/VPE2
config7IAR_CPU3_VPE3	Boolean	Override Config7.IAR bit for CPU3/VPE3
config7IAR_CPU4_VPE0	Boolean	Override Config7.IAR bit for CPU4/VPE0
config7IAR_CPU4_VPE1	Boolean	Override Config7.IAR bit for CPU4/VPE1
config7IAR_CPU4_VPE2	Boolean	Override Config7.IAR bit for CPU4/VPE2
config7IAR_CPU4_VPE3	Boolean	Override Config7.IAR bit for CPU4/VPE3
config7IAR_CPU5_VPE0	Boolean	Override Config7.IAR bit for CPU5/VPE0
config7IAR_CPU5_VPE1	Boolean	Override Config7.IAR bit for CPU5/VPE1
config7IAR_CPU5_VPE2	Boolean	Override Config7.IAR bit for CPU5/VPE2
config7IAR_CPU5_VPE3	Boolean	Override Config7.IAR bit for CPU5/VPE3
config7IAR_CPU6_VPE0	Boolean	Override Config7.IAR bit for CPU6/VPE0
config7IAR_CPU6_VPE1	Boolean	Override Config7.IAR bit for CPU6/VPE1
config7IAR_CPU6_VPE2	Boolean	Override Config7.IAR bit for CPU6/VPE2
config7IAR_CPU6_VPE3	Boolean	Override Config7.IAR bit for CPU6/VPE3
config7IAR_CPU7_VPE0	Boolean	Override Config7.IAR bit for CPU7/VPE0
config7IAR_CPU7_VPE1	Boolean	Override Config7.IAR bit for CPU7/VPE1
config7IAR_CPU7_VPE2	Boolean	Override Config7.IAR bit for CPU7/VPE2
config7IAR_CPU7_VPE3	Boolean	Override Config7.IAR bit for CPU7/VPE3
config7IVAD_CPU0_VPE0	Boolean	Override Config7.IVAD bit for CPU0/VPE0
config7IVAD_CPU0_VPE1	Boolean	Override Config7.IVAD bit for CPU0/VPE1
config7IVAD_CPU0_VPE2	Boolean	Override Config7.IVAD bit for CPU0/VPE2
config7IVAD_CPU0_VPE3	Boolean	Override Config7.IVAD bit for CPU0/VPE3
config7IVAD_CPU1_VPE0		
config7IVAD_CPU1_VPE1	Boolean Boolean	Override Config7.IVAD bit for CPU1/VPE0 Override Config7.IVAD bit for CPU1/VPE1
		Override Config7.IVAD bit for CPU1/VPE1 Override Config7.IVAD bit for CPU1/VPE2
config7IVAD_CPU1_VPE2	Boolean	Override Config7.IVAD bit for CPU1/VPE2 Override Config7.IVAD bit for CPU1/VPE3
config7IVAD_CPU1_VPE3	Boolean	
config7IVAD_CPU2_VPE0	Boolean	Override Config7.IVAD bit for CPU2/VPE0
config7IVAD_CPU2_VPE1	Boolean	Override Config7.IVAD bit for CPU2/VPE1
config7IVAD_CPU2_VPE2	Boolean	Override Config7.IVAD bit for CPU2/VPE2
config7IVAD_CPU2_VPE3	Boolean	Override Config7.IVAD bit for CPU2/VPE3
config7IVAD_CPU3_VPE0	Boolean	Override Config7.IVAD bit for CPU3/VPE0
config7IVAD_CPU3_VPE1	Boolean	Override Config7.IVAD bit for CPU3/VPE1
config7IVAD_CPU3_VPE2	Boolean	Override Config7.IVAD bit for CPU3/VPE2
config7IVAD_CPU3_VPE3	Boolean	Override Config7.IVAD bit for CPU3/VPE3
config7IVAD_CPU4_VPE0	Boolean	Override Config7.IVAD bit for CPU4/VPE0
config7IVAD_CPU4_VPE1	Boolean	Override Config7.IVAD bit for CPU4/VPE1
config7IVAD_CPU4_VPE2	Boolean	Override Config7.IVAD bit for CPU4/VPE2
config7IVAD_CPU4_VPE3	Boolean	Override Config7.IVAD bit for CPU4/VPE3
config7IVAD_CPU5_VPE0	Boolean	Override Config7.IVAD bit for CPU5/VPE0
config7IVAD_CPU5_VPE1	Boolean	Override Config7.IVAD bit for CPU5/VPE1
config7IVAD_CPU5_VPE2	Boolean	Override Config7.IVAD bit for CPU5/VPE2
config7IVAD_CPU5_VPE3	Boolean	Override Config7.IVAD bit for CPU5/VPE3
config7IVAD_CPU6_VPE0	Boolean	Override Config7.IVAD bit for CPU6/VPE0
config7IVAD_CPU6_VPE1	Boolean	Override Config7.IVAD bit for CPU6/VPE1
config7IVAD_CPU6_VPE2	Boolean	Override Config7.IVAD bit for CPU6/VPE2

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config7IVAD_CPU6_VPE3	Boolean	Override Config7.IVAD bit for CPU6/VPE3
config7IVAD_CPU7_VPE0	Boolean	Override Config7.IVAD bit for CPU7/VPE0
config7IVAD_CPU7_VPE1	Boolean	Override Config7.IVAD bit for CPU7/VPE1
config7IVAD_CPU7_VPE2	Boolean	Override Config7.IVAD bit for CPU7/VPE2
config7IVAD_CPU7_VPE3	Boolean	Override Config7.IVAD bit for CPU7/VPE3
config7RPS_CPU0_VPE0	Boolean	Override Config7.RPS bit for CPU0/VPE0
config7RPS_CPU0_VPE1	Boolean	Override Config7.RPS bit for CPU0/VPE1
config7RPS_CPU0_VPE2	Boolean	Override Config7.RPS bit for CPU0/VPE2
config7RPS_CPU0_VPE3	Boolean	Override Config7.RPS bit for CPU0/VPE3
config7RPS_CPU1_VPE0	Boolean	Override Config7.RPS bit for CPU1/VPE0
config7RPS_CPU1_VPE1	Boolean	Override Config7.RPS bit for CPU1/VPE1
config7RPS_CPU1_VPE2	Boolean	Override Config7.RPS bit for CPU1/VPE2
config7RPS_CPU1_VPE3	Boolean	Override Config7.RPS bit for CPU1/VPE3
config7RPS_CPU2_VPE0	Boolean	Override Config7.RPS bit for CPU2/VPE0
config7RPS_CPU2_VPE1	Boolean	Override Config7.RPS bit for CPU2/VPE1
config7RPS_CPU2_VPE2	Boolean	Override Config7.RPS bit for CPU2/VPE2
config7RPS_CPU2_VPE3	Boolean	Override Config7.RPS bit for CPU2/VPE3
config7RPS_CPU3_VPE0	Boolean	Override Config7.RPS bit for CPU3/VPE0
config7RPS_CPU3_VPE1	Boolean	Override Config7.RPS bit for CPU3/VPE1
config7RPS_CPU3_VPE2	Boolean	Override Config7.RPS bit for CPU3/VPE2
config7RPS_CPU3_VPE3	Boolean	Override Config7.RPS bit for CPU3/VPE3
config7RPS_CPU4_VPE0	Boolean	Override Config7.RPS bit for CPU4/VPE0
config7RPS_CPU4_VPE1	Boolean	Override Config7.RPS bit for CPU4/VPE1
config7RPS_CPU4_VPE2	Boolean	Override Config7.RPS bit for CPU4/VPE2
config7RPS_CPU4_VPE3	Boolean	Override Config7.RPS bit for CPU4/VPE3
config7RPS_CPU5_VPE0	Boolean	Override Config7.RPS bit for CPU5/VPE0
config7RPS_CPU5_VPE1	Boolean	Override Config7.RPS bit for CPU5/VPE1
config7RPS_CPU5_VPE2	Boolean	Override Config7.RPS bit for CPU5/VPE2
config7RPS_CPU5_VPE3	Boolean	Override Config7.RPS bit for CPU5/VPE3
config7RPS_CPU6_VPE0	Boolean	1
		Override Config7.RPS bit for CPU6/VPE0
config7RPS_CPU6_VPE1	Boolean	Override Config7.RPS bit for CPU6/VPE1
config7RPS_CPU6_VPE2	Boolean	Override Config7.RPS bit for CPU6/VPE2
config7RPS_CPU6_VPE3	Boolean	Override Config7.RPS bit for CPU6/VPE3
config7RPS_CPU7_VPE0	Boolean	Override Config7.RPS bit for CPU7/VPE0
config7RPS_CPU7_VPE1	Boolean	Override Config7.RPS bit for CPU7/VPE1
config7RPS_CPU7_VPE2	Boolean	Override Config7.RPS bit for CPU7/VPE2
config7RPS_CPU7_VPE3	Boolean	Override Config7.RPS bit for CPU7/VPE3
statusFR	Boolean	Override power on value in Status.FR (Floating
		point register mode)
fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant
		with IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/SNaN encodings
		match IEEE 754-2008 recommendation)
numMaarRegs	Uns32	Override number of MAAR registers (must be even)
srsconf0SRS1	Uns32	Override the SRS1 field in SRSConf0 register
srsconf0SRS2	Uns32	Override the SRS2 field in SRSConf0 register
srsconf0SRS3	Uns32	Override the SRS3 field in SRSConf0 register
wiredLimit	Uns32	Override Limit field of the Wired register
wiredLimitBits	Uns32	Override width of Limit field of the Wired register
wiredWiredBits	Uns32	Override width of Wired field of the Wired register
cdmmBaseCI	Boolean	Override CDMMBase.CI
parityEnable	Uns32	Specify error detection support: 0 - none; 1 - parity;
•		2 - ECC
useMpTb	Boolean	Override Use of multi-processor test bench
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use
	0.11002	GCR_Cx_RESET_BASE on CMP processors)

UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the cor-
UseExceptionBase	Boolean	responding BEV address bits
11BufferCache	Boolean	L1 Buffer Cache
GCU_EX	Boolean	CMP system only: GCR custom block present
GIC.EX	Boolean	CMP system only: GCR custom block present CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: GPC unit present CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable
SWINTIROUTABLE	Boolean	within cluster
PERFCNT_ROUTABLE	Boolean	CMP system only: performance counter interrupt
1 ERFONT HOUTABLE	Doolean	routable within cluster
FDC_ROUTABLE	Boolean	CMP system only: fast debug channel interrupt
1 DOI(OO IMBEE	Boolean	routable within cluster
GCR_PCORES	Uns32	CMP system only: override
	011502	GCR_CONFIG.PCORES (number of cores-1)
GCR_ADDR_REGIONS	Uns32	CMP system only: override
001011111111111111111111111111111111111	011502	GCR_CONFIG.ADDR_REGIONS (number of
		MMIO address regions)
GCR_NUMAUX	Uns32	CMP system only: override
	0 0 -	GCR_CONFIG.NUMAUX (number of auxil-
		iary memory ports)
GCR_BASE	Uns64	CMP system only: override
0.010_5110_5	011001	GCR_BASE.GCR_BASE (default GCR regis-
		ter address)
GCR_MINOR_REV	Uns32	CMP system only: override
GOILLIII (OILLI)	011502	GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	CMP system only: override
GOIL-IVIII OIL-ILLI V	011302	GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override
GOIL-OIL-OIL-OIL-IVE V	011502	GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override
0 010=01101115=11110 010=10=1	011502	GCR_CACHE_REV.MAJOR_REV
GCR_L2_ASSOC	Uns32	CMP system only: override
		GCR_L2_CONFIG.ASSOC
GCR_L2_SET_SIZE	Uns32	CMP system only: override
		GCR_L2_CONFIG.SET_SIZE
GCR_SYS_CONFIG2_MAX_VP_WIDTH	Uns32	CMP system only: override
		GCR_SYS_CONFIG2.MAX_VP_WIDTH
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override
		GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override
		GCR_IOCU1_REV.MAJOR_REV
GCR_BEV_BASE	Uns32	CMP system only: override GCR_BEV_BASE
GCR_KX_BASE_MODE	Boolean	CMP system only: override BEV_BASE_MODE &
		RESET_BASE_MODE
GCR_MMIO_REQ_LIMIT	Uns32	CMP system only: override
•		GCR_MMIO_REQ_LIMIT.MMIO_REQ_LIMIT
		value
GCR_MMIO0_BOTTOM	Uns64	CMP system only: override
		GCR_MMIO0_BOTTOM register value
GCR_MMIO0_TOP_ADDR	Uns32	CMP system only: override
		GCR_MMIO0_TOP.TOP_ADDR value
		GOIL-WIWIOU-1 OI . 1 OI -ADDIT value
GCR_MMIO1_BOTTOM	Uns64	CMP system only: override
GCR_MMIO1_BOTTOM	Uns64	
GCR_MMIO1_BOTTOM GCR_MMIO1_TOP_ADDR	Uns64 Uns32	CMP system only: override

GCR_MMIO2_BOTTOM	Uns64	CMP system only: override
GCR_MMIO2_BOTTOM	Uns04	CMP system only: override GCR_MMIO2_BOTTOM register value
GCR_MMIO2_TOP_ADDR	Uns32	CMP system only: override
		GCR_MMIO2_TOP.TOP_ADDR value
GCR_MMIO3_BOTTOM	Uns64	CMP system only: override
		GCR_MMIO3_BOTTOM register value
GCR_MMIO3_TOP_ADDR	Uns32	CMP system only: override
		GCR_MMIO3_TOP.TOP_ADDR value
GIC_NUMINTERRUPTS	Uns32	CMP system only: override
		GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override
CIC MINOD DEV	11 20	GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override
GIC_MAJOR_REV	Ulis52	GIC_SH_REVISION.MAJOR_REV
GIC_NUM_TEAMS	Uns32	CMP system only: override
GICINOMITEAMS	Ulisaz	GIC_SH_DBG_CONFIG.NUM_TEAMS
GIC_TRIG_RESET	Uns32	CMP system only: Zero value of
	0 11502	GIC_SH_TRIG_[31_0, 63_32]
GIC_PVPES	Uns32	CMP system only: override
	3 3 -	GIC_SH_CONFIG.PVPE
CPC_MICROSTEP	Uns32	CMP system only: override
		CPC_SEQUEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override
		CPC_RAIL.RAILDELAY
CPC_RESETLEN	Uns32	CMP system only: override
		CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override
CDC 141 IOD DDV	***	CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override
CIC CII CID CONDICALO	11 20	CPC_REVISION.MAJOR_REV
GIC_SH_GID_CONFIG31_0	Uns32	CMP system only: override GIC_SH_GID_CONFIG[31_0]
GIC_SH_GID_CONFIG63_32	Uns32	CMP system only: override
G10_511_G1D_001v11G05_52	011852	GIC_SH_GID_CONFIG[63_32]
GIC_SH_GID_CONFIG95_64	Uns32	CMP system only: override
	0 11502	GIC_SH_GID_CONFIG[95_64]
GIC_SH_GID_CONFIG127_96	Uns32	CMP system only: override
		GIC_SH_GID_CONFIG[127_96]
GIC_SH_GID_CONFIG159_128	Uns32	CMP system only: override
		GIC_SH_GID_CONFIG[159_128]
GIC_SH_GID_CONFIG191_160	Uns32	CMP system only: override
		GIC_SH_GID_CONFIG[191_160]
GIC_SH_GID_CONFIG223_192	Uns32	CMP system only: override
CIC OIL CID COMPICATE AND	11 00	GIC_SH_GID_CONFIG[223_192]
GIC_SH_GID_CONFIG255_224	Uns32	CMP system only: override
gicVirtualVPNum_CPU0_VP0	Uns32	GIC_SH_GID_CONFIG[255_224] Override the IPTI field in IntCtl register for
gic v ii tuai v r ivuiii_Or ou_VPU	Ulis32	CPU0/VP0
gicVirtualVPNum_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for
910 , 11 0 d car , 1 1 d d d 1 0 0 1 1 1	011302	CPU0/VP1
gicVirtualVPNum_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for
5-0,	011002	CPU0/VP2
		CF UU/ VF 2
gicVirtualVPNum_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for

gicVirtualVPNum_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
gicVirtualVPNum_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
$gicVirtual VPNum_CPU1_VP2$	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
gicVirtualVPNum_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
gicVirtualVPNum_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
gicVirtualVPNum_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
gicVirtualVPNum_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
gicVirtualVPNum_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
gicVirtualVPNum_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
gicVirtualVPNum_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
gicVirtualVPNum_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
gicVirtualVPNum_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
gicVirtualVPNum_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
gicVirtualVPNum_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
$gicVirtual VPNum_CPU4_VP2$	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
gicVirtualVPNum_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
gicVirtualVPNum_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
gicVirtualVPNum_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
gicVirtualVPNum_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
gicVirtualVPNum_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
gicVirtualVPNum_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
gicVirtualVPNum_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
$gicVirtual VPNum_CPU6_VP2$	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
gicVirtualVPNum_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
gicVirtualVPNum_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
gicVirtualVPNum_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
gicVirtualVPNum_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
gicVirtualVPNum_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3

GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
		core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
GCR_C4_RESET_BASE	Uns32	core 3 CMP system only: GCR_CL_RESET_BASE for
GCR_C4_RESE1_BASE	Ulis52	core 4
GCR_C5_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
		core 5
GCR_C6_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
GCR_C7_RESET_BASE	Uns32	core 6 CMP system only: GCR_CL_RESET_BASE for
GCR_C/_RESET_DASE	011852	core 7
GCR_C8_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
		core 8
GCR_C9_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
GCR_C0_RESET_EXT_BASE	Uns32	core 9 CMP system only: GCR_CL_RESET_EXT_BASE
GCR_CU_RESET_EXT_BASE	Ulis52	for core 0
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 1
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
GCR_C3_RESET_EXT_BASE	Uns32	for core 2 CMP system only: GCR_CL_RESET_EXT_BASE
GCR_C3_RESET_EXT_BASE	Uns32	for core 3
GCR_C4_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 4
GCR_C5_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
GCR_C6_RESET_EXT_BASE	Uns32	for core 5 CMP system only: GCR_CL_RESET_EXT_BASE
GCR_CO_RESET_EXT_BASE	Ulis52	for core 6
GCR_C7_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 7
GCR_C8_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
GCR_C9_RESET_EXT_BASE	Uns32	for core 8 CMP system only: GCR_CL_RESET_EXT_BASE
GCR_C9_RESET_EXT_BASE	Uns32	for core 9
CPC_C0_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 0
CPC_C1_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 1
CPC_C2_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 2
CPC_C3_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 3
CPC_C4_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 4
CPC_C5_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 5
CPC_C6_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 6
CPC_C7_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 7
CPC_C8_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 8
CPC_C9_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 9
EIC_OPTION	Uns32	Override the external interrupt controller EIC_OPTION
guestCtl0RI	Uns32	Override the RI field in GuestCtl0 register
guestCtl0MC	Uns32	Override the MC field in GuestCtl0 register
guestCtl0CP0	Uns32	Override the CP0 field in GuestCtl0 register
guestCtl0AT	Uns32	Override the AT field in GuestCtl0 register

guestCtl0GT	Uns32	Override the GT field in GuestCtl0 register
guestCtl0CG	Uns32	Override the CG field in GuestCtl0 register
guestCtl0CF	Uns32	Override the CF field in GuestCtl0 register
guestCtl0G1	Uns32	Override the G1 field in GuestCtl0 register
guestCtl0RAD	Uns32	Override the RAD field in GuestCtl0 register
guestCtl0DRG	Uns32	Override the DRG field in GuestCtl0 register
hasImpl17	Boolean	Enable read/write of Impl17 bit in Status register
hasImpl16	Boolean	Enable read/write of Impl16 bit in Status register
guestintctlIPTI	Uns32	Override the Guest IPTI field in IntCtl register
guestintctlIPFDC	Uns32	Override the Guest II TI held in IntCtl register Override the Guest IPFDC field in IntCtl register
guestintetIIPPCI	Uns32	Override the Guest IPFDC field in IntCtl register Override the Guest IPPCI field in IntCtl register
guestintctIFFCI guestintctIPTI_CPU0_VP0	Uns32	
		Override the IPTI field in IntCtl register for CPU0/VP0
guestintctlIPTI_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
guestintctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
guestintctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
guestintctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
guestintctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
guestintctlIPTI_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
guestintctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
guestintctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
guestintctlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
guestintctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
guestintctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
guestintctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
guestintctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
guestintctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
guestintctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
guestintctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
guestintctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
guestintctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
guestintctlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
guestintctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
guestintctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1

guestintctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
guestintctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
guestintctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
guestintctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
guestintctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
guestintctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
guestintctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
guestintctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
guestintctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
guestintctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
guestintctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
guestintctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
guestintctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
guestintctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
guestintctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
guestintctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
guestintctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
guestintctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
guestintctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0
guestintctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
guestintctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
guestintctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
guestintctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
guestintctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
guestintctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
guestintctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
guestintctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0
guestintctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1

guestintctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
guestintctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
guestintctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
guestintctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
guestintctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
guestintctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
guestintctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
guestintctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
guestintctlIPFDC_CPU6_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2
guestintctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
guestintctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
guestintctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
guestintctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
guestintctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
guestintctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
guestintctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
guestintctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
guestintctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
guestintctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0
guestintctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP1
guestintctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
guestintctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
guestintctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
guestintctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
guestintctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
guestintctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
guestintctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0
guestintctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1

guestintctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for
		CPU3/VP2
guestintctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
guestintctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
guestintctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
guestintctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
guestintctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
guestintctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0
guestintctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1
guestintctlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2
guestintctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
guestintctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
guestintctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP1
guestintctlIPPCI_CPU6_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP2
guestintctlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
guestintctlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
guestintctlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
guestintctlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
guestintctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
ISPRAM_SIZE	Uns32	Encoded size of the ISPRAM region (log2(<ispram bytes="" in="" size="">) - 11)</ispram>
ISPRAM_BASE	Uns64	Starting physical address of the ISPRAM region
ISPRAM_ENABLE	Boolean	Set the enable bit of the ISPRAM region's tag (used to enable the ISPRAM region prior to reset)
ISPRAM_FILE	String	Load a MIPS hex file into the ISPRAM region prior to reset
DSPRAM_SIZE	Uns32	Encoded size of the DSPRAM region (log2(<dspram bytes="" in="" size="">) - 11)</dspram>
DSPRAM_BASE	Uns64	Starting physical address of the DSPRAM region
DSPRAM_ENABLE	Boolean	Set the enable bit of the DSPRAM region's tag
		(used to enable the DSPRAM region prior to reset)
DSPRAM_PRESENT	Boolean	DSPRAM is present with SAAR
USPRAM_SIZE	Uns32	Encoded size of the USPRAM region (log2(<uspram bytes="" in="" size="">) - 11)</uspram>
USPRAM_BASE	Uns64	Starting physical address of the USPRAM region
USPRAM_ENABLE	Boolean	Set the enable bit of the USPRAM region's tag
		(used to enable the USPRAM region prior to reset)

USPRAM_FILE	String	Load a MIPS hex file into the USPRAM region
		prior to reset
misaligned Data Exception	Enumeration	Select misaligned data access exception signaling: never, checkCCA or always (never, checkCCA or always)
commitTlbwErr	Boolean	Commit TLBWI/TLBRI on ECC; in MIPS_DV_MODE only

Table 8.1: Parameters that can be set in: CMP

Name	Type	Description
endian	Endian	Model endian
cacheenable	Enumeration	Select cache model mode (default, tag or full)
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info struc-
		ture
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for AVP test termination)
cacheIndexBypassTLB	Boolean	When set, cache index ops do not generate TLB exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
gprNames	Boolean	Disassemble the register names from the default
		ABI instead of register numbers for MIPS-format
		trace output
supervisorMode	Boolean	Override whether processor implements supervisor
		mode
busErrors	Boolean	Override bus error exception behavior. When true,
		accesses of memory not defined by platform will
		cause bus error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when
		true (sets Config.MT=3, Config.KU/K23=2 and
fixedDbgRegSize	Boolean	Config1.MMUSizeM1=0) Enable applications to debug on P5600 with GDB
		version 2015.06-05 and prior
removeDSP	Boolean	Override the DSP-present configuration when true (sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true
		(sets Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true
TOTAL D		(sets Config1.FP to 0)
removeFTLB	Boolean	Override the FTLBEn configuration when true (disable FTLB)
isISA	Boolean	Enable to specify ISA model (reset address from
	D 1	ELF, all coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to
m auf Caunt and	II _{r-} -20	maximum value to improve performance Performance Counters
perfCounters ITCNumEntries	Uns32 Uns32	Specify number of ITC cells present (MT cores
	Unsoz	only)
ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC
		implementation (MT cores only)
ITCFIFODepth	Uns32	Specify ITC FIFO cell depth. By default supports 4.
ITCEmptyOnReset	Boolean	Specify ITC E/F cells reset to a known empty state.
		-r j 2/1 come reset to a mis in simply state.

MTFPU supportDenormals	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior, 2:new mttc1 behavior)
	D '	2:new intici benavior)
	Llooloom	Enable to specify that the FPU supports denormal
LIDEON TO	Boolean	operands and results
	II20	Specifies the maximum TCs initially on VPE0. Ig-
VPE0MaxTC	Uns32	nored if less than two VPEs configured.
VPE1MaxTC	Uns32	
VPEIMAXIC	Uns32	Specifies the maximum TCs initially on VPE1. Ig-
D'4	TI 90	nored if less than three VPEs configured.
segBits	Uns32	Override the number of address bits implemented
ъ.	11 00	for 64 bit segments (MIPS64 Only)
mpuRegions	Uns32	Number of regions for memory protection unit
mpuType	Uns32	Type of MPU implementation
mpuEnable	Boolean	Enable MPU2 segment control at reset
mpuSegment0	Uns32	Attributes for segment 0 in MPU2 SegmentCon-
		trol_0 register
mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentCon-
		trol_0 register
mpuSegment2	Uns32	Attributes for segment 2 in MPU2 SegmentCon-
		trol_0 register
mpuSegment3	Uns32	Attributes for segment 3 in MPU2 SegmentCon-
		trol_0 register
mpuSegment4	Uns32	Attributes for segment 4 in MPU2 SegmentCon-
•		trol_1 register
mpuSegment5	Uns32	Attributes for segment 5 in MPU2 SegmentCon-
I and G		trol_1 register
mpuSegment6	Uns32	Attributes for segment 6 in MPU2 SegmentCon-
mp ac ognicia o	011002	trol_1 register
mpuSegment7	Uns32	Attributes for segment 7 in MPU2 SegmentCon-
inpusesment.	0 11302	trol_1 register
mpuSegment8	Uns32	Attributes for segment 8 in MPU2 SegmentCon-
mpusegmento	0 11302	trol_2 register
mpuSegment9	Uns32	Attributes for segment 9 in MPU2 SegmentCon-
mpusegments	011552	trol_2 register
mpuSegment10	Uns32	Attributes for segment 10 in MPU2 SegmentCon-
mpusegment to	011852	trol_2 register
mpuSegment11	Uns32	Attributes for segment 11 in MPU2 SegmentCon-
mpusegment11	Ulis52	trol_2 register
mpuSegment12	Uns32	Attributes for segment 12 in MPU2 SegmentCon-
mpuSegment12	Uns32	
0 110	11 00	trol_3 register
mpuSegment13	Uns32	Attributes for segment 13 in MPU2 SegmentCon-
0 111	11 00	trol-3 register
mpuSegment14	Uns32	Attributes for segment 14 in MPU2 SegmentCon-
-		trol_3 register
mpuSegment15	Uns32	Attributes for segment 15 in MPU2 SegmentCon-
		trol_3 register
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
tcDisable	Uns32	Number of disabled TCs
vpeDisable	Uns32	Number of disabled VPEs
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
mvpconf1c1f	Boolean	Override MVPConf.C1F
mvpcontrolPolicyMode	Boolean	Override MVPControl.POLICY_MODE
hasFDC	Uns32	Specify the size of Fast Debug Channel register
		block

licenseWarningDays	Uns32	Specify the number of days before a license expires
nceuse war inng Days	Ulisaz	to start issuing a warning. 0 disables warnings.
MIPS_UHI	Boolean	Enable MIPS-Unified Hosting interface
mipsUhiArgs	String	Specifies UHI arguments string separated by spaces
mipsUhiJail	String	Specifies UHI jailroot
MIPS_DV_MODE	Boolean	Enable Design Verification mode
MIPS_MAGIC_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes
enableTrickbox	Boolean	Enable trickbox addresses (specific for AVP)
fpuexcdisable	Boolean	Disable FPU exceptions
TRU_PRESENT	Boolean	Disable or Enable based on TRU presence to con-
		trol certain fields (e.x.perfCtl.PCTD
ucLLwordsLocked	Uns32	Numbers of words (4 byte) an uncached LL is lock-
		ing. Maximum: 4K
FUSA	Boolean	Enable Functional Safety
CPC_FAULT_SUPPORTED	Uns32	Specify the value for Functional Safety Supported
		register
CPC_FAULT_ENABLE	Uns32	Specify the value for Functional Safety Enable reg-
		ister
cop2Bits	Uns32	Specifies width in bits of COP2 registers (32 or 64)
cop2FileName	String	Specifies COP2 dynamically-loaded object
		(.so/.dll) defining COP2 instructions
udiConfig	Int32	Specifies UDI configuration attribute
udiFileName	String	Specifies UDI dynamically-loaded object (.so/.dll)
		defining UDI instructions
vectoredinterrupt	Boolean	Enables vectored interrupts (sets Config3 VInt)
externalinterrupt	Boolean	Enables the use of an external interrupt controller
		(sets Config3 VEIC)
config3VEIC_VPE0	Boolean	Enables an external interrupt controller on VPE0
		(sets Config3 VEIC)
config3VEIC_VPE1	Boolean	Enables an external interrupt controller on VPE1
		(sets Config3 VEIC)
config3VEIC_VPE2	Boolean	Enables an external interrupt controller on VPE2
6 AVEIG LIDEO	D 1	(sets Config3 VEIC)
config3VEIC_VPE3	Boolean	Enables an external interrupt controller on VPE3
T. 12.00.	D 1	(sets Config3 VEIC)
rootFixedMMU	Boolean	Override the root MMU type to fixed map-
		ping when true (sets Config.MT=3 and Con-
rootMMUSizeM1	Uns32	fig.KU/K23=2) Override the root MMUSizeM1 field in Config1 reg-
rootminosizemi	Ulis52	ister (number of MMU entries-1)
srsctlHSS	Uns32	Override the HSS field in SRSCtl register (number
SISCHIESS	Ulisaz	of shadow register sets)
firPS	Uns32	Override the PS field in FIR register
firHas2008	Uns32	Override the Has 2008 field in FIR register
usePreciseFpu	Uns32	Use the precise Floating Point emulation
simulateLite	Enumeration	Run Simulation with optimization. There are
		several optimizations which coule be combined
		(NONE, FS, MA or FSMA)
pridCompanyOptions	Uns32	Override the Company Options field in PRId reg-
r		ister
pridRevision	Uns32	Override the Revision field in PRId register
globalClusterNum	Uns32	Override the ClusterNum field in GlobalNumber
		, and the second
		register
intctlIPTI		register Override the IPTI field in IntCtl register
intctlIPTI intctlIPFDC	Uns32 Uns32	register Override the IPTI field in IntCtl register Override the IPFDC field in IntCtl register

numWatch	Uns32	Specify number of WatchLo/WatchHi register pairs
maxVP	Uns32	Specify maximum number of Virtual Processors
		present in a core
numVP	Uns32	Specify number of Virtual Processors to be present
numVPtoStart	Uns32	Specify number of Virtual Processors to be started
sharedTLBindex	Uns32	Specify first shared TLB Index between Virtual Cores
xconfigSpecified	Boolean	True if the configuration comes from a valid xconfig file
intctlIPTI_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
intctlIPTI_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
intctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
intctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
intctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
intctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
intctlIPTI_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
intctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
intctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
intctlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
intctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
intctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
intctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
intctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
intctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
intctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
intctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
intctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
intctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
intctlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
intctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
intctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
intctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
intctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3

intctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for
intctlIPTI_CPU6_VP1	11 00	CPU6/VP0
	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
intctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
intctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
intctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
intctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
intctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
intctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
intctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
intctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
intctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
intctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
intetlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
intctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
intctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
intctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
intctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0
intctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
intctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
intctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
intctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
intetlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
intctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
intctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
intctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0
intctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1
intctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
intctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3

intctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
intctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
intctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
intctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
intctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
intctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
intctlIPFDC_CPU6_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2
intctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
intctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
intctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
intctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
intctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
intctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
intctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
intctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
intctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
intctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0
intctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP1
intctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
intctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
intctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
intctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
intctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
intctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
intctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0
intctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1
intctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP2
intctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3

intctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for
		CPU4/VP0
intctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
intctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
intctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
intctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0
intctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1
intctlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2
intctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
intctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
intctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP1
intctlIPPCI_CPU6_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP2
intetlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
intetlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
intetlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
intetlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
intctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
segcfg0PA	Uns32	Set CFG0.PA field of SegCtl0 register
segcfg1PA	Uns32	Set CFG1.PA field of SegCtl0 register
segcfg2PA	Uns32	Set CFG2.PA field of SegCtl1 register
segcfg3PA	Uns32	Set CFG3.PA field of SegCtl1 register
segcfg4PA	Uns32	Set CFG4.PA field of SegCtl2 register
segcfg5PA	Uns32	Set CFG5.PA field of SegCtl2 register
segcfg0AM	Uns32	Set CFG0.AM field of SegCtl0 register
segcfg1AM	Uns32	Set CFG1.AM field of SegCtl0 register
segcfg2AM	Uns32	Set CFG2.AM field of SegCtl1 register
segcfg3AM	Uns32	Set CFG3.AM field of SegCtl1 register
segcfg4AM	Uns32	Set CFG4.AM field of SegCtl2 register
segcfg5AM	Uns32	Set CFG5.AM field of SegCtl2 register
segcfg0EU	Uns32	Set CFG0.EU field of SegCtl0 register
segcfg1EU	Uns32	Set CFG1.EU field of SegCtl0 register
segcfg2EU	Uns32	Set CFG2.EU field of SegCtl1 register
segcfg3EU	Uns32	Set CFG3.EU field of SegCtl1 register
segcfg4EU	Uns32	Set CFG4.EU field of SegCtl2 register
segcfg5EU	Uns32	Set CFG5.EU field of SegCtl2 register
segcfg0C	Uns32	Set CFG0.C field of SegCtl0 register
segcfg1C	Uns32	Set CFG1.C field of SegCtl0 register
segcfg2C	Uns32	Set CFG2.C field of SegCtl1 register
segcfg3C	Uns32	Set CFG3.C field of SegCtl1 register
segcfg4C	Uns32	Set CFG4.C field of SegCtl2 register
segcfg5C	Uns32	Set CFG5.C field of SegCtl2 register
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cdmmSize	Uns32	Override the cdmmsize reset value
configAR	Uns32	Enables R6 support
configBM	Uns32	Override the BM field in Config register (burst
ComigBivi	Ulis52	mode)
configDSP	Boolean	Override Config.DSP (data scratchpad RAM
ComigDoi	Boolean	present)
configISP	Boolean	Override Config.ISP (instruction scratchpad RAM
001119101	Boolean	present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0
	0 1.20 0	cacheability)
configKU	Uns32	Override power on value of Config.KU (set Useg
S		cacheability)
configK23	Uns32	Override power on value of Config.K23 (set Kseg23
S		cacheability)
configMDU	Boolean	Override Config.MDU (iterative multiply/divide
G		unit)
configMM	Boolean	Override Config.MM (merging mode for write)
configMT	Uns32	Override Config.MT
configSB	Boolean	Override Config.SB (simple bus transfers only)
configBCP	Boolean	Override Config.BCP (Buffer Cache Present)
MIPS16eASE	Boolean	Override Config1.CA (enables the MIPS16e ASE)
config1DA	Uns32	Override Config1.DA (Deache associativity)
config1DL	Uns32	Override Config1.DL (Deache line size)
config1DS	Uns32	Override Config1.DS (Deache sets per way)
config1EP	Boolean	Override Config1.EP (EJTag present)
config1IA	Uns32	Override Config1.IA (Icache associativity)
config1IL	Uns32	Override Config1.IL (Icache line size)
config1IS	Uns32	Override Config1.IS (Icache sets per way)
config1MMUSizeM1	Uns32	Override Config1.MMUSizeM1 (number of MMU
comgniviviopizewii	011392	entries-1)
config1MMUSizeM1_VPE1	Uns32	Override Config1.MMUSizeM1 for VPE1
config1MMUSizeM1_VPE2	Uns32	Override Config1.MMUSizeM1 for VPE2
config1MMUSizeM1_VPE3	Uns32	Override Config1.MMUSizeM1 for VPE3
config1WR	Boolean	Override Config1.WR (watchpoint registers
		present)
config1PC	Boolean	Override Config1.PC (Performance Counters
9		present)
config1C2	Boolean	Override Config1.C2 (Coprocessor 2 present)
config2SU	Uns32	Override the SU field in Config2 register
config2SS	Uns32	Override the SS field in Config2 register
config2SL	Uns32	Override the SL field in Config2 register
config2SA	Uns32	Override the SA field in Config2 register
config3BI	Boolean	Override Config3.BI
config3BP	Boolean	Override Config3.BP
config3CDMM	Boolean	Override Config3.CDMM
config3CTXTC	Boolean	Override Config3.CTXTC
config3DSPP	Boolean	Override Config3.DSPP
config3DSP2P	Boolean	Override Config3.DSP2P
config3IPLW	Uns32	Override Config3.IPLW
config3ISA	Uns32	Override Config3.ISA
config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3ITL	Boolean	Override Config3.ITL
config3LPA	Boolean	Override Config3.LPA
config3MCU	Boolean	Override Config3.MCU
config3MMAR	Uns32	Override Config3.MMAR
config3RXI	Boolean	Override Config3.RXI
		1 0

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config3SC	Boolean	Override Config3.SC
config3ULRI	Boolean	Override Config3.ULRI
config3VZ	Boolean	Override Config3.VZ
config3MSAP	Boolean	Override Config3.MSAP
config3CMGCR	Boolean	Override the CMGCR field in Config3 register
config3SP	Boolean	Override the SP field in Config3 register
config3TL	Uns32	Override the TL field in Config3 register
config3PW	Boolean	Override the PW field in Config3 register
config4AE	Boolean	Override Config4.AE
config4IE	Uns32	Override Config4.IE
config4MMUConfig	Uns32	Override Config4.MMUConfig field (interpretation
		depends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.VTLBSizeExt
config4KScrExist	Uns32	Override Config4.KScrExist
config5EVA	Boolean	Override Config5.EVA
config5LLB	Boolean	Override Config5.LLB (LLAddr supports LLbit)
config5MRP	Boolean	Override Config5.MRP (MaaR Present)
config5NFExists	Boolean	Override Config5.NFExists
mips32Macro	Boolean	Enables the MIPS32 SAVE and RESTORE macro
_		instructions. Ignored if Config5.CA2 is not set)
config5MSAEn	Boolean	Override Config5.MSAEn
config5MVH	Boolean	Override Config5.MVH (enable MTHC0 and
_		MFHC0 instructions)
config5DEC	Boolean	Override Config5.DEC (to test Dual Endian Capa-
_		bility)
config5GI	Uns32	Override Config5.GI (enable GINV)
config5CRCP	Boolean	Override Config5.CRCP (CRCP Present)
config5VP	Boolean	Override Config5.VP
config6FTLBEn	Boolean	Override power on value of Config6.FTLBEn
config7AR	Boolean	Override Config7.AR (Alias removed Data cache)
config7DCIDX_MODE	Uns32	Override Config7.DCIDX_MODE
config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initializa-
		tion)
config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction
		cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)
config7ES	Uns32	Override the ES field in Config7 register (External-
		ize sync)
config7WR	Boolean	Override Config7[31] bit (Alternative implementa-
		tion of Watch registers)
config7FPR	Boolean	Override Config7.FPR (one-half FPU clock ratio)
config7USP	Uns32	Override Config7.USP (USPRAM enable)
config7BTLM	Boolean	Override Config7.BTLM bit
config7BusSlp	Boolean	Override Config7.BusSlp bit
config7IVAD	Boolean	Override Config7.IVAD bit
config7RPS	Boolean	Override Config7.RPS bit
config7IAR_CPU0_VPE0	Boolean	Override Config7.IAR bit for CPU0/VPE0
config7IAR_CPU0_VPE1	Boolean	Override Config7.IAR bit for CPU0/VPE1
config7IAR_CPU0_VPE2	Boolean	Override Config7.IAR bit for CPU0/VPE2
config7IAR_CPU0_VPE3	Boolean	Override Config7.IAR bit for CPU0/VPE3
config7IAR_CPU1_VPE0	Boolean	Override Config7.IAR bit for CPU1/VPE0
config7IAR_CPU1_VPE1	Boolean	Override Config7.IAR bit for CPU1/VPE1
config7IAR_CPU1_VPE2	Boolean	Override Config7.IAR bit for CPU1/VPE2
config7IAR_CPU1_VPE3	Boolean	Override Config7.IAR bit for CPU1/VPE3
config7IAR_CPU2_VPE0	Boolean	Override Config7.IAR bit for CPU2/VPE0
COMISTANCE OF OZEVIED	Doolean	Override Comigr.IAIt bit for CFU2/VFE0

config7IAR_CPU2_VPE1	Boolean	Override Config7.IAR bit for CPU2/VPE1
config7IAR_CPU2_VPE2	Boolean	Override Config7.IAR bit for CPU2/VPE2
config7IAR_CPU2_VPE3	Boolean	Override Config7.IAR bit for CPU2/VPE3
config7IAR_CPU3_VPE0	Boolean	Override Config7.IAR bit for CPU3/VPE0
config7IAR_CPU3_VPE1	Boolean	Override Config7.IAR bit for CPU3/VPE1
config7IAR_CPU3_VPE2	Boolean	Override Config7.IAR bit for CPU3/VPE2
config7IAR_CPU3_VPE3	Boolean	Override Config7.IAR bit for CPU3/VPE3
config7IAR_CPU4_VPE0	Boolean	Override Config7.IAR bit for CPU4/VPE0
config7IAR_CPU4_VPE1	Boolean	Override Config7.IAR bit for CPU4/VPE1
config7IAR_CPU4_VPE2	Boolean	Override Config7.IAR bit for CPU4/VPE2
config7IAR_CPU4_VPE3	Boolean	Override Config7.IAR bit for CPU4/VPE3
config7IAR_CPU5_VPE0	Boolean	Override Config7.IAR bit for CPU5/VPE0
config7IAR_CPU5_VPE1	Boolean	Override Config7.IAR bit for CPU5/VPE1
config7IAR_CPU5_VPE2	Boolean	Override Config7.IAR bit for CPU5/VPE2
config7IAR_CPU5_VPE3	Boolean	Override Config7.IAR bit for CPU5/VPE3
config7IAR_CPU6_VPE0	Boolean	Override Config7.IAR bit for CPU6/VPE0
config7IAR_CPU6_VPE1	Boolean	Override Config7.IAR bit for CPU6/VPE1
config7IAR_CPU6_VPE2	Boolean	Override Config7.IAR bit for CPU6/VPE2
config7IAR_CPU6_VPE3	Boolean	Override Config7.IAR bit for CPU6/VPE3
config7IAR_CPU7_VPE0	Boolean	Override Config7.IAR bit for CPU7/VPE0
config7IAR_CPU7_VPE1	Boolean	Override Config7.IAR bit for CPU7/VPE1
config7IAR_CPU7_VPE2	Boolean	Override Config7.IAR bit for CPU7/VPE2
config7IAR_CPU7_VPE3	Boolean	Override Config7.IAR bit for CPU7/VPE3
config7IVAD_CPU0_VPE0	Boolean	Override Config7.IVAD bit for CPU0/VPE0
config7IVAD_CPU0_VPE1	Boolean	Override Config7.IVAD bit for CPU0/VPE1
config7IVAD_CPU0_VPE2	Boolean	Override Config7.IVAD bit for CPU0/VPE2
config7IVAD_CPU0_VPE3	Boolean	Override Config7.IVAD bit for CPU0/VPE3
config7IVAD_CPU1_VPE0	Boolean	Override Config7.IVAD bit for CPU1/VPE0
config7IVAD_CPU1_VPE1	Boolean	Override Config7.IVAD bit for CPU1/VPE1
config7IVAD_CPU1_VPE2	Boolean	Override Config7.IVAD bit for CPU1/VPE2 Override Config7.IVAD bit for CPU1/VPE2
config7IVAD_CPU1_VPE3		Override Config7.IVAD bit for CPU1/VPE3 Override Config7.IVAD bit for CPU1/VPE3
config7IVAD_CPU2_VPE0	Boolean	Override Config7.IVAD bit for CPU1/VPE3 Override Config7.IVAD bit for CPU2/VPE0
	Boolean	- ,
config7IVAD_CPU2_VPE1	Boolean	Override Config7.IVAD bit for CPU2/VPE1
config7IVAD_CPU2_VPE2	Boolean	Override Config7.IVAD bit for CPU2/VPE2
config7IVAD_CPU2_VPE3	Boolean	Override Config7.IVAD bit for CPU2/VPE3
config7IVAD_CPU3_VPE0	Boolean	Override Config7.IVAD bit for CPU3/VPE0
config7IVAD_CPU3_VPE1	Boolean	Override Config7.IVAD bit for CPU3/VPE1
config7IVAD_CPU3_VPE2	Boolean	Override Config7.IVAD bit for CPU3/VPE2
config7IVAD_CPU3_VPE3	Boolean	Override Config7.IVAD bit for CPU3/VPE3
config7IVAD_CPU4_VPE0	Boolean	Override Config7.IVAD bit for CPU4/VPE0
config7IVAD_CPU4_VPE1	Boolean	Override Config7.IVAD bit for CPU4/VPE1
config7IVAD_CPU4_VPE2	Boolean	Override Config7.IVAD bit for CPU4/VPE2
config7IVAD_CPU4_VPE3	Boolean	Override Config7.IVAD bit for CPU4/VPE3
config7IVAD_CPU5_VPE0	Boolean	Override Config7.IVAD bit for CPU5/VPE0
config7IVAD_CPU5_VPE1	Boolean	Override Config7.IVAD bit for CPU5/VPE1
config7IVAD_CPU5_VPE2	Boolean	Override Config7.IVAD bit for CPU5/VPE2
config7IVAD_CPU5_VPE3	Boolean	Override Config7.IVAD bit for CPU5/VPE3
config7IVAD_CPU6_VPE0	Boolean	Override Config7.IVAD bit for CPU6/VPE0
config7IVAD_CPU6_VPE1	Boolean	Override Config7.IVAD bit for CPU6/VPE1
config7IVAD_CPU6_VPE2	Boolean	Override Config7.IVAD bit for CPU6/VPE2
config7IVAD_CPU6_VPE3	Boolean	Override Config7.IVAD bit for CPU6/VPE3
config7IVAD_CPU7_VPE0	Boolean	Override Config7.IVAD bit for CPU7/VPE0
config7IVAD_CPU7_VPE1	Boolean	Override Config7.IVAD bit for CPU7/VPE1
config7IVAD_CPU7_VPE2	Boolean	Override Config7.IVAD bit for CPU7/VPE2
comig/TVAD_CF U/_VFE2	Doolean	Override Comignity and bit for C1 C1/ V1 L2
config7IVAD_CPU7_VPE3	Boolean	Override Config7.IVAD bit for CPU7/VPE3 Override Config7.RPS bit for CPU0/VPE0

6 MDDG CDHO LIDEA		O C C F DDC1:: C CDUO/VDC1
config7RPS_CPU0_VPE1	Boolean	Override Config7.RPS bit for CPU0/VPE1
config7RPS_CPU0_VPE2	Boolean	Override Config7.RPS bit for CPU0/VPE2
config7RPS_CPU0_VPE3	Boolean	Override Config7.RPS bit for CPU0/VPE3
config7RPS_CPU1_VPE0	Boolean	Override Config7.RPS bit for CPU1/VPE0
config7RPS_CPU1_VPE1	Boolean	Override Config7.RPS bit for CPU1/VPE1
config7RPS_CPU1_VPE2	Boolean	Override Config7.RPS bit for CPU1/VPE2
config7RPS_CPU1_VPE3	Boolean	Override Config7.RPS bit for CPU1/VPE3
config7RPS_CPU2_VPE0	Boolean	Override Config7.RPS bit for CPU2/VPE0
config7RPS_CPU2_VPE1	Boolean	Override Config7.RPS bit for CPU2/VPE1
config7RPS_CPU2_VPE2	Boolean	Override Config7.RPS bit for CPU2/VPE2
config7RPS_CPU2_VPE3	Boolean	Override Config7.RPS bit for CPU2/VPE3
config7RPS_CPU3_VPE0	Boolean	Override Config7.RPS bit for CPU3/VPE0
config7RPS_CPU3_VPE1	Boolean	Override Config7.RPS bit for CPU3/VPE1
config7RPS_CPU3_VPE2	Boolean	Override Config7.RPS bit for CPU3/VPE2
config7RPS_CPU3_VPE3	Boolean	Override Config7.RPS bit for CPU3/VPE3
config7RPS_CPU4_VPE0	Boolean	Override Config7.RPS bit for CPU4/VPE0
config7RPS_CPU4_VPE1	Boolean	Override Config7.RPS bit for CPU4/VPE1
config7RPS_CPU4_VPE2	Boolean	Override Config7.RPS bit for CPU4/VPE2
config7RPS_CPU4_VPE3	Boolean	Override Config7.RPS bit for CPU4/VPE3
config7RPS_CPU5_VPE0	Boolean	Override Config7.RPS bit for CPU5/VPE0
config7RPS_CPU5_VPE1	Boolean	Override Config7.RPS bit for CPU5/VPE1
config7RPS_CPU5_VPE2	Boolean	Override Config7.RPS bit for CPU5/VPE2
config7RPS_CPU5_VPE3	Boolean	Override Config7.RPS bit for CPU5/VPE3
config7RPS_CPU6_VPE0	Boolean	Override Config7.RPS bit for CPU6/VPE0
config7RPS_CPU6_VPE1	Boolean	Override Config7.RPS bit for CPU6/VPE1
config7RPS_CPU6_VPE2	Boolean	Override Config7.RPS bit for CPU6/VPE2
config7RPS_CPU6_VPE3	Boolean	Override Config7.RPS bit for CPU6/VPE3
config7RPS_CPU7_VPE0	Boolean	Override Config7.RPS bit for CPU7/VPE0
config7RPS_CPU7_VPE1	Boolean	Override Config7.RPS bit for CPU7/VPE1
config7RPS_CPU7_VPE2	Boolean	Override Config7.RPS bit for CPU7/VPE2
config7RPS_CPU7_VPE3	Boolean	Override Config7.RPS bit for CPU7/VPE3
statusFR	Boolean	Override power on value in Status.FR (Floating
		point register mode)
fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant
		with IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/SNaN encodings
1001111112000	Boolean	match IEEE 754-2008 recommendation)
numMaarRegs	Uns32	Override number of MAAR registers (must be even)
srsconf0SRS1	Uns32	Override the SRS1 field in SRSConf0 register
srsconf0SRS2	Uns32	Override the SRS2 field in SRSConf0 register
srsconf0SRS3	Uns32	Override the SRS3 field in SRSConf0 register
wiredLimit	Uns32	Override Limit field of the Wired register
wiredLimitBits	Uns32	Override width of Limit field of the Wired register
wiredWiredBits	Uns32	Override width of Wired field of the Wired register
cdmmBaseCI	Boolean	Override CDMMBase.CI
parityEnable	Uns32	Specify error detection support: 0 - none; 1 - parity;
M. (D)	D 1	2 - ECC
useMpTb	Boolean	Override Use of multi-processor test bench
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use GCR_Cx_RESET_BASE on CMP processors)
UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the cor-
		responding BEV address bits
l1BufferCache	Boolean	L1 Buffer Cache
GCU_EX	Boolean	CMP system only: GCR custom block present
GIC-EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present
OI OLEA	Doolean	OMI System omy. Of Chunt present

TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable
SWINT_ROUTABLE	Boolean	within cluster CMP system only: software interrupt routable
		within cluster
PERFCNT_ROUTABLE	Boolean	CMP system only: performance counter interrupt routable within cluster
FDC_ROUTABLE	Boolean	CMP system only: fast debug channel interrupt
I BOMOO INBEE	Boolean	routable within cluster
GCR_PCORES	Uns32	CMP system only: override
0.000	0 0 -	GCR_CONFIG.PCORES (number of cores-1)
GCR_ADDR_REGIONS	Uns32	CMP system only: override
		GCR_CONFIG.ADDR_REGIONS (number of
		MMIO address regions)
GCR_NUMAUX	Uns32	CMP system only: override
		GCR_CONFIG.NUMAUX (number of auxil-
		iary memory ports)
GCR_BASE	Uns64	CMP system only: override
GCR_DASE	011804	GCR_BASE.GCR_BASE (default GCR regis-
		ter address)
CCD MINOD DEV	TT 20	/
GCR_MINOR_REV	Uns32	
		GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	CMP system only: override
		GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override
		GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override
		GCR_CACHE_REV.MAJOR_REV
GCR_L2_ASSOC	Uns32	CMP system only: override
		GCR_L2_CONFIG.ASSOC
GCR_L2_SET_SIZE	Uns32	CMP system only: override
0.010=2=021=0122	011002	GCR_L2_CONFIG.SET_SIZE
GCR_SYS_CONFIG2_MAX_VP_WIDTH	Uns32	CMP system only: override
	011092	GCR_SYS_CONFIG2.MAX_VP_WIDTH
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override
derend der innverteur.	011002	GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override
GOILIOCOTIMAJOILILEV	011552	GCR_IOCU1_REV.MAJOR_REV
GCR_BEV_BASE	Uns32	CMP system only: override GCR_BEV_BASE
GCR_KX_BASE_MODE	Boolean	CMP system only: override BEV_BASE_MODE &
	** 00	RESET_BASE_MODE
GCR_MMIO_REQ_LIMIT	Uns32	CMP system only: override
		GCR_MMIO_REQ_LIMIT.MMIO_REQ_LIMIT
		value
GCR_MMIO0_BOTTOM	Uns64	CMP system only: override
		GCR_MMIO0_BOTTOM register value
GCR_MMIO0_TOP_ADDR	Uns32	CMP system only: override
		GCR_MMIO0_TOP.TOP_ADDR value
GCR_MMIO1_BOTTOM	Uns64	CMP system only: override
		GCR_MMIO1_BOTTOM register value
GCR_MMIO1_TOP_ADDR	Uns32	CMP system only: override
		GCR_MMIO1_TOP.TOP_ADDR value
GCR_MMIO2_BOTTOM	Uns64	CMP system only: override
S 010-1111110 2-100 1 1 0 1/1	OHOOT	GCR_MMIO2_BOTTOM register value
GCR_MMIO2_TOP_ADDR	Uns32	CMP system only: override
GOR_MIMIO2_TOF_ADDR	U1IS32	GCR_MMIO2_TOP_TOP_ADDR value
COD MMIOS DOTTOM	TT - C4	
GCR_MMIO3_BOTTOM	Uns64	CMP system only: override
		GCR_MMIO3_BOTTOM register value

GCR_MMIO3_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO3_TOP.TOP_ADDR value
GIC_NUMINTERRUPTS	Uns32	CMP system only: override
		GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MAJOR_REV
GIC_NUM_TEAMS	Uns32	CMP system only: override GIC_SH_DBG_CONFIG.NUM_TEAMS
GIC_TRIG_RESET	Uns32	CMP system only: Zero value of GIC_SH_TRIG_[31_0, 63_32]
GIC_PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPE
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY
CPC_RESETLEN	Uns32	CMP system only: override CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override CPC_REVISION.MAJOR_REV
GIC_SH_GID_CONFIG31_0	Uns32	CMP system only: override GIC_SH_GID_CONFIG[31_0]
GIC_SH_GID_CONFIG63_32	Uns32	CMP system only: override GIC_SH_GID_CONFIG[63_32]
GIC_SH_GID_CONFIG95_64	Uns32	CMP system only: override GIC_SH_GID_CONFIG[95_64]
GIC_SH_GID_CONFIG127_96	Uns32	CMP system only: override GIC_SH_GID_CONFIG[127_96]
GIC_SH_GID_CONFIG159_128	Uns32	CMP system only: override GIC_SH_GID_CONFIG[159_128]
GIC_SH_GID_CONFIG191_160	Uns32	CMP system only: override GIC_SH_GID_CONFIG[191_160]
GIC_SH_GID_CONFIG223_192	Uns32	CMP system only: override GIC_SH_GID_CONFIG[223_192]
GIC_SH_GID_CONFIG255_224	Uns32	CMP system only: override GIC_SH_GID_CONFIG[255_224]
gicVirtualVPNum_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
gicVirtualVPNum_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
gicVirtualVPNum_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
gicVirtualVPNum_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
gicVirtualVPNum_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
gicVirtualVPNum_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
gicVirtualVPNum_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2

gicVirtualVPNum_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
gicVirtualVPNum_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
gicVirtualVPNum_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
gicVirtualVPNum_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
gicVirtualVPNum_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
gicVirtualVPNum_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
gicVirtualVPNum_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
gicVirtualVPNum_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
gicVirtualVPNum_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
gicVirtualVPNum_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
gicVirtualVPNum_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
gicVirtualVPNum_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
gicVirtualVPNum_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
gicVirtualVPNum_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
gicVirtualVPNum_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
gicVirtualVPNum_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
gicVirtualVPNum_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
gicVirtualVPNum_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
gicVirtualVPNum_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
gicVirtualVPNum_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
gicVirtualVPNum_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
gicVirtualVPNum_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
gicVirtualVPNum_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
gicVirtualVPNum_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
gicVirtualVPNum_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2

GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
GGD GL DEGET DAGE	77. 22	core 3
GCR_C4_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
GGD GT DEGET DAGE	77. 00	core 4
GCR_C5_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
CCD CO DECET DACE	11 00	core 5
GCR_C6_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
CCD CT DECET DACE	11 00	core 6
GCR_C7_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
GCR_C8_RESET_BASE	11 20	core 7
GCR_C8_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
GCR_C9_RESET_BASE	Uns32	core 8 CMP system only: GCR_CL_RESET_BASE for
GCR_C9_RESET_BASE	Uns32	core 9
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
GCR_CU_RESET_EAT_DASE	Ulisaz	for core 0
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
GCR_C1_RESE1_EX1_DASE	Ulisaz	for core 1
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
GOIL-OZ-ILESET-EXT-DASE	Clisoz	for core 2
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
GOIL-OS-ILESET-EXT-DASE	Clisoz	for core 3
GCR_C4_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
	011352	for core 4
GCR_C5_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
	011352	for core 5
GCR_C6_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
	011502	for core 6
GCR_C7_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
	0 0	for core 7
GCR_C8_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 8
GCR_C9_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 9
CPC_C0_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 0
CPC_C1_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 1
CPC_C2_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 2
CPC_C3_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 3
CPC_C4_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 4
CPC_C5_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 5
CPC_C6_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 6
CPC_C7_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 7
CPC_C8_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 8
CPC_C9_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 9
EIC_OPTION	Uns32	Override the external interrupt controller
		EIC_OPTION
guestCtl0RI	Uns32	Override the RI field in GuestCtl0 register
guestCtl0MC	Uns32	Override the MC field in GuestCtl0 register
guestCtl0CP0	Uns32	Override the CP0 field in GuestCtl0 register
guestCtl0AT	Uns32	Override the AT field in GuestCtl0 register
guestCtl0GT	Uns32	Override the GT field in GuestCtl0 register
guestCtl0CG	Uns32	Override the CG field in GuestCtl0 register
guestCtl0CF	Uns32	Override the CF field in GuestCtl0 register
guestCtl0G1	Uns32	Override the G1 field in GuestCtl0 register
	Uns32	
guestCtl0RAD guestCtl0DRG		Override the RAD field in GuestCtl0 register Override the DRG field in GuestCtl0 register

hasImpl17	Boolean	Enable read/write of Impl17 bit in Status register
hasImpl16	Boolean	Enable read/write of Impl16 bit in Status register
guestintctlIPTI	Uns32	Override the Guest IPTI field in IntCtl register
guestintctlIPFDC	Uns32	Override the Guest IPFDC field in IntCtl register
guestintctlIPPCI	Uns32	Override the Guest IPPCI field in IntCtl register
guestintctlIPTI_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
$guest intctlIPTI_CPU0_VP1$	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
guestintctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
guestintctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
guestintctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
guestintctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
guestintctlIPTI_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
guestintctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
guestintctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
guestintctlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
guestintctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
guestintctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
guestintctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
guestintctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
guestintctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
guestintctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
guestintctIIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
guestintctIIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
guestintctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
guestintctIIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
guestintctIIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
guestintctIIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
guestintctIIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
guestintctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
guestintctIIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
guestintctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1

guestintctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
guestintctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
guestintctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
guestintctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
guestintctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
guestintctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
guestintctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
guestintctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
guestintctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
guestintctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
guestintctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
guestintctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
guestintctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
guestintctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
guestintctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0
guestintctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
guestintctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
guestintctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
guestintctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
guestintctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
guestintctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
guestintctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
guestintctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0
guestintctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1
guestintctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
guestintctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
guestintctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
guestintctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1

$guestintctlIPFDC_CPU5_VP2$	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
guestintctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
guestintctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
guestintctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
$guestintctlIPFDC_CPU6_VP2$	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2
guestintctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
guestintctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
guestintctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
guestintctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
guestintctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
guestintctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
guestintctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
guestintctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
guestintctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
guestintctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0
guestintctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP1
guestintctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
guestintctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
guestintctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
guestintctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
guestintctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
guestintctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
guestintctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0
guestintctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1
guestintctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP2
guestintctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
guestintctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
guestintctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1

guestintctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
guestintctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
guestintctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0
guestintctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1
guestintctlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2
guestintctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
guestintctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
guestintctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP1
guestintctlIPPCI_CPU6_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP2
guestintctlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
guestintctlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
guestintctlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
guestintctlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
guestintctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
ISPRAM_SIZE	Uns32	Encoded size of the ISPRAM region (log2(<ispram bytes="" in="" size="">) - 11)</ispram>
ISPRAM_BASE	Uns64	Starting physical address of the ISPRAM region
ISPRAM_ENABLE	Boolean	Set the enable bit of the ISPRAM region's tag (used to enable the ISPRAM region prior to reset)
ISPRAM_FILE	String	Load a MIPS hex file into the ISPRAM region prior to reset
DSPRAM_SIZE	Uns32	Encoded size of the DSPRAM region (log2(<dspram bytes="" in="" size="">) - 11)</dspram>
DSPRAM_BASE	Uns64	Starting physical address of the DSPRAM region
DSPRAM_ENABLE	Boolean	Set the enable bit of the DSPRAM region's tag
		(used to enable the DSPRAM region prior to reset)
DSPRAM_PRESENT	Boolean	DSPRAM is present with SAAR
USPRAM_SIZE	Uns32	Encoded size of the USPRAM region (log2(<uspram bytes="" in="" size="">) - 11)</uspram>
USPRAM_BASE	Uns64	Starting physical address of the USPRAM region
USPRAM_ENABLE	Boolean	Set the enable bit of the USPRAM region's tag
		(used to enable the USPRAM region prior to reset)
USPRAM_FILE	String	Load a MIPS hex file into the USPRAM region prior to reset
misaligned Data Exception	Enumeration	Select misaligned data access exception signaling: never, checkCCA or always (never, checkCCA or always)
commitTlbwErr	Boolean	Commit TLBWI/TLBRI on ECC; in MIPS_DV_MODE only

Table 8.2: Parameters that can be set in: CPU

Name	Type	Description
endian	Endian	Model endian
cacheenable	Enumeration	Select cache model mode (default, tag or full)
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info structure
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for AVP test termination)
${\it cache Index By pass TLB}$	Boolean	When set, cache index ops do not generate TLB exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
gprNames	Boolean	Disassemble the register names from the default ABI instead of register numbers for MIPS-format trace output
supervisorMode	Boolean	Override whether processor implements supervisor mode
busErrors	Boolean	Override bus error exception behavior. When true, accesses of memory not defined by platform will cause bus error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when true (sets Config.MT=3, Config.KU/K23=2 and Config1.MMUSizeM1=0)
${\it fixedDbgRegSize}$	Boolean	Enable applications to debug on P5600 with GDB version 2015.06-05 and prior
removeDSP	Boolean	Override the DSP-present configuration when true (sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true (sets Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true (sets Config1.FP to 0)
removeFTLB	Boolean	Override the FTLBEn configuration when true (disable FTLB)
isISA	Boolean	Enable to specify ISA model (reset address from ELF, all coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to maximum value to improve performance
perfCounters	Uns32	Performance Counters
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores only)
ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC implementation (MT cores only)
ITCFIFODepth	Uns32	Specify ITC FIFO cell depth. By default supports 4.
ITCEmptyOnReset	Boolean	Specify ITC E/F cells reset to a known empty state.
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior, 2:new mttc1 behavior)
support Denormals	Boolean	Enable to specify that the FPU supports denormal operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0. Ignored if less than two VPEs configured.
VPE1MaxTC	Uns32	Specifies the maximum TCs initially on VPE1. Ignored if less than three VPEs configured.
segBits	Uns32	Override the number of address bits implemented for 64 bit segments (MIPS64 Only)
mpuRegions	Uns32	Number of regions for memory protection unit

mpuType	Uns32	Type of MPU implementation
mpuEnable	Boolean	Enable MPU2 segment control at reset
mpuSegment0	Uns32	Attributes for segment 0 in MPU2 SegmentCon-
		trol_0 register
mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentCon-
		trol_0 register
mpuSegment2	Uns32	Attributes for segment 2 in MPU2 SegmentCon-
		trol_0 register
mpuSegment3	Uns32	Attributes for segment 3 in MPU2 SegmentCon-
		trol_0 register
mpuSegment4	Uns32	Attributes for segment 4 in MPU2 SegmentCon-
		trol_1 register
mpuSegment5	Uns32	Attributes for segment 5 in MPU2 SegmentCon-
		trol_1 register
mpuSegment6	Uns32	Attributes for segment 6 in MPU2 SegmentCon-
		trol_1 register
mpuSegment7	Uns32	Attributes for segment 7 in MPU2 SegmentCon-
		trol_1 register
mpuSegment8	Uns32	Attributes for segment 8 in MPU2 SegmentCon-
		trol_2 register
mpuSegment9	Uns32	Attributes for segment 9 in MPU2 SegmentCon-
9	***	trol_2 register
mpuSegment10	Uns32	Attributes for segment 10 in MPU2 SegmentCon-
0 111	11 00	trol_2 register
mpuSegment11	Uns32	Attributes for segment 11 in MPU2 SegmentCon-
G 442	11 00	trol_2 register
mpuSegment12	Uns32	Attributes for segment 12 in MPU2 SegmentCon-
0 110	11 00	trol_3 register
mpuSegment13	Uns32	Attributes for segment 13 in MPU2 SegmentCon-
mpuSegment14	Uns32	trol_3 register Attributes for segment 14 in MPU2 SegmentCon-
mpusegment14	Ulisaz	trol-3 register
mpuSegment15	Uns32	Attributes for segment 15 in MPU2 SegmentCon-
mpusegment 15	Ulisaz	trol.3 register
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
tcDisable	Uns32	Number of disabled TCs
vpeDisable	Uns32	Number of disabled VPEs
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
mvpconftc1f	Boolean	Override MVPConf.C1F
mvpcontrolPolicyMode	Boolean	Override MVPControl.POLICY_MODE
hasFDC	Uns32	Specify the size of Fast Debug Channel register
nasr DC	Ulisoz	block
licenseWarningDays	Uns32	Specify the number of days before a license expires
neense warmingDays	011392	to start issuing a warning. 0 disables warnings.
MIPS_UHI	Boolean	Enable MIPS-Unified Hosting interface
mipsUhiArgs	String	Specifies UHI arguments string separated by spaces
mipsUhiJail	String	Specifies UHI jailroot
MIPS_DV_MODE	Boolean	Enable Design Verification mode
MIPS_MAGIC_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes
enableTrickbox	Boolean	Enable trickbox addresses (specific for AVP)
	Doorcan	Eliable dickbox addresses (specific for 11v1)
	Roolean	Disable FPU exceptions
fpuexcdisable TRU_PRESENT	Boolean Boolean	Disable FPU exceptions Disable or Enable based on TRU presence to con-

ucLLwordsLocked	Uns32	Numbers of words (4 byte) an uncached LL is locking. Maximum: 4K
FUSA	Boolean	Enable Functional Safety
CPC_FAULT_SUPPORTED	Uns32	Specify the value for Functional Safety Supported register
CPC_FAULT_ENABLE	Uns32	Specify the value for Functional Safety Enable register
cop2Bits	Uns32	Specifies width in bits of COP2 registers (32 or 64)
cop2FileName	String	Specifies COP2 dynamically-loaded object (.so/.dll) defining COP2 instructions
udiConfig	Int32	Specifies UDI configuration attribute
udiFileName	String	Specifies UDI dynamically-loaded object (.so/.dll) defining UDI instructions
vectoredinterrupt	Boolean	Enables vectored interrupts (sets Config3 VInt)
externalinterrupt	Boolean	Enables the use of an external interrupt controller (sets Config3 VEIC)
config3VEIC_VPE0	Boolean	Enables an external interrupt controller on VPE0 (sets Config3 VEIC)
config3VEIC_VPE1	Boolean	Enables an external interrupt controller on VPE1 (sets Config3 VEIC)
config3VEIC_VPE2	Boolean	Enables an external interrupt controller on VPE2 (sets Config3 VEIC)
config3VEIC_VPE3	Boolean	Enables an external interrupt controller on VPE3 (sets Config3 VEIC)
${\bf rootFixedMMU}$	Boolean	Override the root MMU type to fixed mapping when true (sets Config.MT=3 and Config.KU/K23=2)
${\bf rootMMUSizeM1}$	Uns32	Override the root MMUSizeM1 field in Config1 register (number of MMU entries-1)
srsctlHSS	Uns32	Override the HSS field in SRSCtl register (number of shadow register sets)
firPS	Uns32	Override the PS field in FIR register
firHas2008	Uns32	Override the Has2008 field in FIR register
usePreciseFpu	Uns32	Use the precise Floating Point emulation
${\bf simulate Lite}$	Enumeration	Run Simulation with optimization. There are several optimizations which coule be combined (NONE, FS, MA or FSMA)
pridCompanyOptions	Uns32	Override the Company Options field in PRId register
pridRevision	Uns32	Override the Revision field in PRId register
globalClusterNum	Uns32	Override the ClusterNum field in GlobalNumber register
intctlIPTI	Uns32	Override the IPTI field in IntCtl register
intctlIPFDC	Uns32	Override the IPFDC field in IntCtl register
intctlIPPCI	Uns32	Override the IPPCI field in IntCtl register
numWatch	Uns32	Specify number of WatchLo/WatchHi register pairs
maxVP	Uns32	Specify maximum number of Virtual Processors present in a core
numVP	Uns32	Specify number of Virtual Processors to be present
numVPtoStart sharedTLBindex	Uns32 Uns32	Specify number of Virtual Processors to be started Specify first shared TLB Index between Virtual
xconfigSpecified	Boolean	Cores True if the configuration comes from a valid xconfig file
intctlIPTI_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0

intctlIPTI_CPU0_VP1	11 00	
	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
intctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
intctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
intctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
intctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
intctlIPTI_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
intctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
intctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
intetlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
intctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
intctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
intctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
intctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
intctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
intctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
intctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
intctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
intctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
intctlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
intctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
intctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
intctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
intctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
intctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
intctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
intctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
intctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
intctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0

intctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for
intctlIPTI_CPU7_VP2	Uns32	CPU7/VP1 Override the IPTI field in IntCtl register for CPU7/VP2
intctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
intctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
intctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
intctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
intctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
intctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
intctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
intctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
intctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
intctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0
intctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
intctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
intctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
intctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
intctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
intctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
intctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
intctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0
intctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1
intctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
intctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
intctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
intctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
intctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
intctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
intctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0

intctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
intctlIPFDC_CPU6_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2
intctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
intctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
intctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
intctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
intctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
intctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
intctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
intctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
intctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
intctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0
intctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP1
intctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
intctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
intctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
intctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
intctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
intctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
intctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0
intctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1
intctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP2
intctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
intctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
intctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
intctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
intctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
intctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0

intctlIPPCI_CPU5_VP1		
internal circle object i	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1
intetlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2
intctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
intctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
intctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for
intctlIPPCI_CPU6_VP2	Uns32	CPU6/VP1 Override the IPPCI field in IntCtl register for
intctlIPPCI_CPU6_VP3	Uns32	CPU6/VP2 Override the IPPCI field in IntCtl register for
intctlIPPCI_CPU7_VP0	Uns32	CPU6/VP3 Override the IPPCI field in IntCtl register for
intctlIPPCI_CPU7_VP1	Uns32	CPU7/VP0 Override the IPPCI field in IntCtl register for
intctlIPPCI_CPU7_VP2	Uns32	CPU7/VP1 Override the IPPCI field in IntCtl register for
intctlIPPCI_CPU7_VP3	Uns32	CPU7/VP2 Override the IPPCI field in IntCtl register for CPU7/VP3
segcfg0PA	Uns32	Set CFG0.PA field of SegCtl0 register
segcfg1PA	Uns32	Set CFG0.FA field of SegCtl0 register Set CFG1.PA field of SegCtl0 register
segcig1FA segcfg2PA	Uns32	Set CFG1.FA field of SegCt10 register Set CFG2.PA field of SegCt11 register
segcig2FA segcfg3PA	Uns32	Set CFG2.FA field of SegCtl1 register Set CFG3.PA field of SegCtl1 register
segcig3FA segcfg4PA	Uns32	Set CFG3.FA field of SegCtl1 register Set CFG4.PA field of SegCtl2 register
segcig41 A segcfg5PA	Uns32	Set CFG4.1 A field of SegCt12 register Set CFG5.PA field of SegCt12 register
segcfg0AM	Uns32	Set CFG0.AM field of SegCt12 register Set CFG0.AM field of SegCt10 register
	Uns32	Set CFG0.AM field of SegCt10 register Set CFG1.AM field of SegCt10 register
segcfg1AM	Uns32	Set CFG1.AM field of SegCt10 register Set CFG2.AM field of SegCt11 register
segcfg2AM		
segcfg3AM	Uns32 Uns32	Set CFG3.AM field of SegCtl1 register
segcfg4AM	Uns32	Set CFG4.AM field of SegCtl2 register Set CFG5.AM field of SegCtl2 register
segcfg5AM		Set CFG0.EU field of SegCtl2 register Set CFG0.EU field of SegCtl0 register
segcfg0EU segcfg1EU	Uns32	Set CFG0.EU field of SegCtl0 register Set CFG1.EU field of SegCtl0 register
	Uns32	Set CFG1.EU field of SegCtl1 register Set CFG2.EU field of SegCtl1 register
segcfg2EU	Uns32 Uns32	Set CFG2.EU field of SegCtl1 register Set CFG3.EU field of SegCtl1 register
segcfg3EU		
segcfg4EU segcfg5EU	Uns32 Uns32	Set CFG4.EU field of SegCtl2 register Set CFG5.EU field of SegCtl2 register
segcigoE0	Uns32	Set CFG0.C field of SegCtl2 register Set CFG0.C field of SegCtl0 register
segcigoC segcfg1C	Uns32	Set CFG1.C field of SegCt10 register Set CFG1.C field of SegCt10 register
segcig1C segcfg2C	Uns32	
	Uns32 Uns32	Set CFG2.C field of SegCt11 register
segcfg3C segcfg4C		Set CFG3.C field of SegCt11 register
segcig4C segcig5C	Uns32 Uns32	Set CFG4.C field of SegCtl2 register Set CFG5.C field of SegCtl2 register
cdmmSize	Uns32	Override the cdmmsize reset value
configAR	Uns32	Enables R6 support
configBM	Uns32	Override the BM field in Config register (burst
_		mode)
configDSP	Boolean	Override Config.DSP (data scratchpad RAM present)
configISP	Boolean	Override Config.ISP (instruction scratchpad RAM present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0 cacheability)

configMDU Boolean Override Config.MDU (iterative multiply/divide unit) ConfigMM Boolean Override Config.MDU (iterative multiply/divide unit) Override Config.MM (merging mode for write) Override Config.SB (simple bus transfers only) Override Config.SB (simple bus transfers only) Override Config.DA (config.CA) Override Config.DA (config.DA) Override Config.DA (con	configKU	Uns32	Override power on value of Config.KU (set Useg cacheability)
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config4AE Boolean Override Config4.AE	config3PW	Boolean	Override the PW field in Config3 register
		Boolean	
	config4IE	Uns32	Override Config4.IE

config4MMUConfig	Uns32	Override Config4.MMUConfig field (interpretation
	0 0	depends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.VTLBSizeExt
config4KScrExist	Uns32	Override Config4.KScrExist
config5EVA	Boolean	Override Config5.EVA
config5LLB	Boolean	Override Config5.LLB (LLAddr supports LLbit)
config5MRP	Boolean	Override Config5.MRP (MaaR Present)
config5NFExists	Boolean	Override Config5.NFExists
mips32Macro	Boolean	Enables the MIPS32 SAVE and RESTORE macro
		instructions. Ignored if Config5.CA2 is not set)
config5MSAEn	Boolean	Override Config5.MSAEn
config5MVH	Boolean	Override Config5.MVH (enable MTHC0 and
		MFHC0 instructions)
config5DEC	Boolean	Override Config5.DEC (to test Dual Endian Capa-
		bility)
config5GI	Uns32	Override Config5.GI (enable GINV)
config5CRCP	Boolean	Override Config5.CRCP (CRCP Present)
config5VP	Boolean	Override Config5.VP
config6FTLBEn	Boolean	Override power on value of Config6.FTLBEn
config7AR	Boolean	Override Config7.AR (Alias removed Data cache)
config7DCIDX_MODE	Uns32	Override Config7.DCIDX_MODE
config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initializa-
		tion)
config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction
0	ļ ,	cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)
config7ES	Uns32	Override the ES field in Config7 register (External-
config7WR	D1	ize sync)
conng t w K	Boolean	Override Config7[31] bit (Alternative implementation of Watch registers)
config7FPR	Boolean	Override Config7.FPR (one-half FPU clock ratio)
config7USP	Uns32	Override Config7.FFR (one-nan FF C clock ratio) Override Config7.USP (USPRAM enable)
config7BTLM	Boolean	Override Config7.BTLM bit
config7BusSlp	Boolean	Override Config7.BusSlp bit
config7IVAD	Boolean	Override Config7.IVAD bit
config7RPS	Boolean	Override Config7.RPS bit
config7IAR_CPU0_VPE0	Boolean	Override Config7.IAR bit for CPU0/VPE0
config7IAR_CPU0_VPE1	Boolean	Override Config7.IAR bit for CPU0/VPE1
config7IAR_CPU0_VPE2	Boolean	Override Config7.IAR bit for CPU0/VPE2
config7IAR_CPU0_VPE3	Boolean	Override Config7.IAR bit for CPU0/VPE3
config7IAR_CPU1_VPE0	Boolean	Override Config7.IAR bit for CPU1/VPE0
config7IAR_CPU1_VPE1	Boolean	Override Config7.IAR bit for CPU1/VPE1
config7IAR_CPU1_VPE2	Boolean	Override Config7.IAR bit for CPU1/VPE2
config7IAR_CPU1_VPE3	Boolean	Override Config7.IAR bit for CPU1/VPE3
config7IAR_CPU2_VPE0	Boolean	Override Config7.IAR bit for CPU2/VPE0
config7IAR_CPU2_VPE1	Boolean	Override Config7.IAR bit for CPU2/VPE1
config7IAR_CPU2_VPE2	Boolean	Override Config7.IAR bit for CPU2/VPE2
config7IAR_CPU2_VPE3	Boolean	Override Config7.IAR bit for CPU2/VPE3
9	Boolean	Override Config7.IAR bit for CPU3/VPE0
config7IAR_CPU3_VPE0		, O:
config7IAR_CPU3_VPE0 config7IAR_CPU3_VPE1		Override Config7.IAR bit for CPU3/VPE1
config7IAR_CPU3_VPE1	Boolean	Override Config7.IAR bit for CPU3/VPE1 Override Config7.IAR bit for CPU3/VPE2
config7IAR_CPU3_VPE1 config7IAR_CPU3_VPE2	Boolean Boolean	Override Config7.IAR bit for CPU3/VPE2
config7IAR_CPU3_VPE1 config7IAR_CPU3_VPE2 config7IAR_CPU3_VPE3	Boolean Boolean Boolean	Override Config7.IAR bit for CPU3/VPE2 Override Config7.IAR bit for CPU3/VPE3
config7IAR_CPU3_VPE1 config7IAR_CPU3_VPE2	Boolean Boolean	Override Config7.IAR bit for CPU3/VPE2

config7IAR_CPU4_VPE3	Boolean	Override Config7.IAR bit for CPU4/VPE3
config7IAR_CPU5_VPE0	Boolean	Override Config7.IAR bit for CPU5/VPE0
config7IAR_CPU5_VPE1	Boolean	Override Config7.IAR bit for CPU5/VPE1
config7IAR_CPU5_VPE2	Boolean	Override Config7.IAR bit for CPU5/VPE2
config7IAR_CPU5_VPE3	Boolean	Override Config7.IAR bit for CPU5/VPE3
config7IAR_CPU6_VPE0	Boolean	Override Config7.IAR bit for CPU6/VPE0
config7IAR_CPU6_VPE1	Boolean	Override Config7.IAR bit for CPU6/VPE1
config7IAR_CPU6_VPE2	Boolean	Override Config7.IAR bit for CPU6/VPE2
config7IAR_CPU6_VPE3	Boolean	Override Config7.IAR bit for CPU6/VPE3
config7IAR_CPU7_VPE0	Boolean	Override Config7.IAR bit for CPU7/VPE0
config7IAR_CPU7_VPE1	Boolean	Override Config7.IAR bit for CPU7/VPE1
config7IAR_CPU7_VPE2	Boolean	Override Config7.IAR bit for CPU7/VPE2
config7IAR_CPU7_VPE3	Boolean	Override Config7.IAR bit for CPU7/VPE3
config7IVAD_CPU0_VPE0	Boolean	Override Config7.IVAD bit for CPU0/VPE0
config7IVAD_CPU0_VPE1	Boolean	Override Config7.IVAD bit for CPU0/VPE1
config7IVAD_CPU0_VPE2	Boolean	Override Config7.IVAD bit for CPU0/VPE2
config7IVAD_CPU0_VPE3	Boolean	Override Config7.IVAD bit for CPU0/VPE3
config7IVAD_CPU1_VPE0	Boolean	Override Config7.IVAD bit for CPU1/VPE0
config7IVAD_CPU1_VPE1	Boolean	Override Config7.IVAD bit for CPU1/VPE1
config7IVAD_CPU1_VPE2	Boolean	Override Config7.IVAD bit for CPU1/VPE2
config7IVAD_CPU1_VPE3	Boolean	Override Config7.IVAD bit for CPU1/VPE3
config7IVAD_CPU2_VPE0	Boolean	Override Config7.IVAD bit for CPU2/VPE0
config7IVAD_CPU2_VPE1	Boolean	Override Config7.IVAD bit for CPU2/VPE1
config7IVAD_CPU2_VPE2	Boolean	Override Config7.IVAD bit for CPU2/VPE2
config7IVAD_CPU2_VPE3	Boolean	Override Config7.IVAD bit for CPU2/VPE3
config7IVAD_CPU3_VPE0	Boolean	Override Config7.IVAD bit for CPU3/VPE0
config7IVAD_CPU3_VPE1	Boolean	Override Config7.IVAD bit for CPU3/VPE1
config7IVAD_CPU3_VPE2	Boolean	Override Config7.IVAD bit for CPU3/VPE2
config7IVAD_CPU3_VPE3	Boolean	Override Config7.IVAD bit for CPU3/VPE3
config7IVAD_CPU4_VPE0	Boolean	Override Config7.IVAD bit for CPU4/VPE0
config7IVAD_CPU4_VPE1	Boolean	Override Config7.IVAD bit for CPU4/VPE1
config7IVAD_CPU4_VPE2	Boolean	Override Config7.IVAD bit for CPU4/VPE2
config7IVAD_CPU4_VPE3	Boolean	Override Config7.IVAD bit for CPU4/VPE3
config7IVAD_CPU5_VPE0	Boolean	Override Config7.IVAD bit for CPU5/VPE0
config7IVAD_CPU5_VPE1	Boolean	Override Config7.IVAD bit for CPU5/VPE1
config7IVAD_CPU5_VPE2	Boolean	Override Config7.IVAD bit for CPU5/VPE2
config7IVAD_CPU5_VPE3	Boolean	Override Config7.IVAD bit for CPU5/VPE3
config7IVAD_CPU6_VPE0	Boolean	Override Config7.IVAD bit for CPU6/VPE0
config7IVAD_CPU6_VPE1	Boolean	Override Config7.IVAD bit for CPU6/VPE1
config7IVAD_CPU6_VPE2	Boolean	Override Config7.IVAD bit for CPU6/VPE2
config7IVAD_CPU6_VPE3	Boolean	Override Config7.IVAD bit for CPU6/VPE3
config7IVAD_CPU7_VPE0	Boolean	Override Config7.IVAD bit for CPU7/VPE0
config7IVAD_CPU7_VPE1	Boolean	Override Config7.IVAD bit for CPU7/VPE1
config7IVAD_CPU7_VPE2	Boolean	Override Config7.IVAD bit for CPU7/VPE2
config7IVAD_CPU7_VPE3	Boolean	Override Config7.IVAD bit for CPU7/VPE3
config7RPS_CPU0_VPE0	Boolean	Override Config7.RPS bit for CPU0/VPE0
config7RPS_CPU0_VPE1	Boolean	Override Config7.RPS bit for CPU0/VPE1
config7RPS_CPU0_VPE2	Boolean	Override Config7.RPS bit for CPU0/VPE2
config7RPS_CPU0_VPE3	Boolean	Override Config7.RPS bit for CPU0/VPE3
config7RPS_CPU1_VPE0	Boolean	Override Config7.RPS bit for CPU1/VPE0
config7RPS_CPU1_VPE1	Boolean	Override Config7.RPS bit for CPU1/VPE1
config7RPS_CPU1_VPE2	Boolean	Override Config7.RPS bit for CPU1/VPE2
config7RPS_CPU1_VPE3	Boolean	Override Config7.RPS bit for CPU1/VPE3
config7RPS_CPU2_VPE0	Boolean	Override Config7.RPS bit for CPU2/VPE0
config7RPS_CPU2_VPE1	Boolean	Override Config7.RPS bit for CPU2/VPE1
config7RPS_CPU2_VPE2	Boolean	Override Config7.RPS bit for CPU2/VPE2
Comis, 101 0201 02_V1 E2	Poorean	Override Comistitut o oil for O1 O2/ V1 E2

	Dealess	Oi la Cambara DDC 1:4 fam CDH9/VDE9
config7RPS_CPU2_VPE3	Boolean	Override Config7.RPS bit for CPU2/VPE3
config7RPS_CPU3_VPE0 config7RPS_CPU3_VPE1	Boolean Boolean	Override Config7.RPS bit for CPU3/VPE0
9		Override Config7.RPS bit for CPU3/VPE1
config7RPS_CPU3_VPE2	Boolean	Override Config7.RPS bit for CPU3/VPE2
config7RPS_CPU3_VPE3	Boolean	Override Config7.RPS bit for CPU3/VPE3
config7RPS_CPU4_VPE0	Boolean	Override Config7.RPS bit for CPU4/VPE0
config7RPS_CPU4_VPE1	Boolean	Override Config7.RPS bit for CPU4/VPE1
config7RPS_CPU4_VPE2	Boolean	Override Config7.RPS bit for CPU4/VPE2
config7RPS_CPU4_VPE3	Boolean	Override Config7.RPS bit for CPU4/VPE3
config7RPS_CPU5_VPE0	Boolean	Override Config7.RPS bit for CPU5/VPE0
config7RPS_CPU5_VPE1	Boolean	Override Config7.RPS bit for CPU5/VPE1
config7RPS_CPU5_VPE2	Boolean	Override Config7.RPS bit for CPU5/VPE2
config7RPS_CPU5_VPE3	Boolean	Override Config7.RPS bit for CPU5/VPE3
config7RPS_CPU6_VPE0	Boolean	Override Config7.RPS bit for CPU6/VPE0
config7RPS_CPU6_VPE1	Boolean	Override Config7.RPS bit for CPU6/VPE1
config7RPS_CPU6_VPE2	Boolean	Override Config7.RPS bit for CPU6/VPE2
config7RPS_CPU6_VPE3	Boolean	Override Config7.RPS bit for CPU6/VPE3
config7RPS_CPU7_VPE0	Boolean	Override Config7.RPS bit for CPU7/VPE0
config7RPS_CPU7_VPE1	Boolean	Override Config7.RPS bit for CPU7/VPE1
config7RPS_CPU7_VPE2	Boolean	Override Config7.RPS bit for CPU7/VPE2
config7RPS_CPU7_VPE3	Boolean	Override Config7.RPS bit for CPU7/VPE3
statusFR	Boolean	Override power on value in Status.FR (Floating
		point register mode)
fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant
		with IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/SNaN encodings
		match IEEE 754-2008 recommendation)
numMaarRegs	Uns32	Override number of MAAR registers (must be even)
srsconf0SRS1	Uns32	Override the SRS1 field in SRSConf0 register
srsconf0SRS2	Uns32	Override the SRS2 field in SRSConf0 register
srsconf0SRS3	Uns32	Override the SRS3 field in SRSConf0 register
wiredLimit	Uns32	Override Limit field of the Wired register
wiredLimitBits	Uns32	Override width of Limit field of the Wired register
wiredWiredBits	Uns32	Override width of Wired field of the Wired register
cdmmBaseCI	Boolean	Override CDMMBase.CI
parityEnable	Uns32	Specify error detection support: 0 - none; 1 - parity;
		2 - ECC
useMpTb	Boolean	Override Use of multi-processor test bench
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use
1		GCR_Cx_RESET_BASE on CMP processors)
UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the cor-
r		responding BEV address bits
l1BufferCache	Boolean	L1 Buffer Cache
GCU_EX	Boolean	CMP system only: GCR custom block present
GIC-EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable
	Boolowii	within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable
~ ·	Boolean	within cluster
PERFCNT_ROUTABLE	Boolean	CMP system only: performance counter interrupt
	Doorcan	routable within cluster
FDC_ROUTABLE	Boolean	CMP system only: fast debug channel interrupt
I DOLLOO INDEE	Doolean	routable within cluster
GCR_PCORES	Uns32	CMP system only: override
	011502	GCR_CONFIG.PCORES (number of cores-1)
		GOTT-CONFIG.1 COTTES (Humber of cores-1)

GCR_ADDR_REGIONS	Uns32	CMP system only: override
GOIL-ADDIL-ILEGIONS	011852	GCR_CONFIG.ADDR_REGIONS (number of
		MMIO address regions)
GCR_NUMAUX	Uns32	CMP system only: override
GOICIVOMITOX	011302	GCR_CONFIG.NUMAUX (number of auxil-
		iary memory ports)
GCR_BASE	Uns64	CMP system only: override
GCILDASE	011804	GCR_BASE.GCR_BASE (default GCR regis-
		ter address)
GCR_MINOR_REV	Uns32	CMP system only: override
GCR_MINOR_REV	Ulis52	GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	
GCR_MAJOR_REV	Uns32	CMP system only: override
COD CLOUE MINOD DEN	TT 00	GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override
		GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override
		GCR_CACHE_REV.MAJOR_REV
GCR_L2_ASSOC	Uns32	CMP system only: override
		GCR_L2_CONFIG.ASSOC
GCR_L2_SET_SIZE	Uns32	CMP system only: override
		GCR_L2_CONFIG.SET_SIZE
GCR_SYS_CONFIG2_MAX_VP_WIDTH	Uns32	CMP system only: override
		GCR_SYS_CONFIG2.MAX_VP_WIDTH
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override
		GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override
		GCR_IOCU1_REV.MAJOR_REV
GCR_BEV_BASE	Uns32	CMP system only: override GCR_BEV_BASE
GCR_KX_BASE_MODE	Boolean	CMP system only: override BEV_BASE_MODE &
001021112111011110111	Boolom	RESET_BASE_MODE
GCR_MMIO_REQ_LIMIT	Uns32	CMP system only: override
	0 11502	GCR_MMIO_REQ_LIMIT.MMIO_REQ_LIMIT
		value
GCR_MMIO0_BOTTOM	Uns64	CMP system only: override
GCI(_WIMIOU_DOTION	011304	GCR_MMIO0_BOTTOM register value
GCR_MMIO0_TOP_ADDR	Uns32	CMP system only: override
GCIt_MMIOU_IOI_ADDIt	011852	GCR_MMIO0_TOP.TOP_ADDR value
GCR_MMIO1_BOTTOM	Uns64	
GCR_MMIOI_BOTTOM	Ulis04	
GCR_MMIO1_TOP_ADDR	Uns32	GCR_MMIO1_BOTTOM register value CMP system only: override
GCR_MMIO1_TOP_ADDR	Uns32	
CCD AD HOS DOTTOM	TT 04	GCR_MMIO1_TOP.TOP_ADDR value
GCR_MMIO2_BOTTOM	Uns64	CMP system only: override
		GCR_MMIO2_BOTTOM register value
GCR_MMIO2_TOP_ADDR	Uns32	CMP system only: override
	_	GCR_MMIO2_TOP.TOP_ADDR value
GCR_MMIO3_BOTTOM	Uns64	CMP system only: override
		GCR_MMIO3_BOTTOM register value
GCR_MMIO3_TOP_ADDR	Uns32	CMP system only: override
		GCR_MMIO3_TOP.TOP_ADDR value
GIC_NUMINTERRUPTS	Uns32	CMP system only: override
		GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override
GIC-COCITIBILE		GIC_SH_CONFIG.COUNTBITS
OTO-CO CITIBITE		
GIC_MINOR_REV	Uns32	CMP system only: override
	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV
	Uns32	

GIC_NUM_TEAMS	Uns32	CMP system only: override GIC_SH_DBG_CONFIG.NUM_TEAMS
GIC_TRIG_RESET	Uns32	CMP system only: Zero value of GIC_SH_TRIG_[31_0, 63_32]
GIC_PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPE
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY
CPC_RESETLEN	Uns32	CMP system only: override CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override CPC_REVISION.MAJOR_REV
GIC_SH_GID_CONFIG31_0	Uns32	CMP system only: override GIC_SH_GID_CONFIG[31.0]
GIC_SH_GID_CONFIG63_32	Uns32	CMP system only: override GIC_SH_GID_CONFIG[63_32]
GIC_SH_GID_CONFIG95_64	Uns32	CMP system only: override GIC_SH_GID_CONFIG[95_64]
GIC_SH_GID_CONFIG127_96	Uns32	CMP system only: override GIC_SH_GID_CONFIG[127_96]
GIC_SH_GID_CONFIG159_128	Uns32	CMP system only: override GIC_SH_GID_CONFIG[159_128]
GIC_SH_GID_CONFIG191_160	Uns32	CMP system only: override GIC_SH_GID_CONFIG[191_160]
GIC_SH_GID_CONFIG223_192	Uns32	CMP system only: override GIC_SH_GID_CONFIG[223_192]
GIC_SH_GID_CONFIG255_224	Uns32	CMP system only: override GIC_SH_GID_CONFIG[255_224]
gicVirtualVPNum_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
gicVirtualVPNum_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
gicVirtualVPNum_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
gicVirtualVPNum_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
gicVirtualVPNum_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
gicVirtualVPNum_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
$gicVirtual VPNum_CPU1_VP2$	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
gicVirtualVPNum_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
gicVirtualVPNum_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
gicVirtualVPNum_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
gicVirtualVPNum_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
gicVirtualVPNum_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3

gicVirtualVPNum_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
gicVirtualVPNum_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
gicVirtualVPNum_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
gicVirtualVPNum_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
gicVirtualVPNum_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
gicVirtualVPNum_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
gicVirtualVPNum_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
gicVirtualVPNum_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
gicVirtualVPNum_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
gicVirtualVPNum_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
gicVirtualVPNum_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
gicVirtualVPNum_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
gicVirtualVPNum_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
gicVirtualVPNum_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
gicVirtualVPNum_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
gicVirtualVPNum_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
gicVirtualVPNum_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
gicVirtualVPNum_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
gicVirtualVPNum_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
gicVirtualVPNum_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 3
GCR_C4_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 4
GCR_C5_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 5
GCR_C6_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 6
GCR_C7_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 7

GCR_C8_RESET_BASE	II20	CMP system only: GCR_CL_RESET_BASE for
GCR_C8_RESET_BASE	Uns32	core 8
GCR_C9_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
GOIL-O9-I(ESET-DASE	011852	core 9
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
GOIL-COLILESET-EXTEDASE	011852	for core 0
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
	011502	for core 1
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
	011502	for core 2
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 3
GCR_C4_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 4
GCR_C5_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 5
GCR_C6_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 6
GCR_C7_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 7
GCR_C8_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 8
GCR_C9_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 9
CPC_C0_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 0
CPC_C1_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 1
CPC_C2_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 2
CPC_C3_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 3
CPC_C4_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 4
CPC_C5_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 5
CPC_C6_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 6
CPC_C7_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 7
CPC_C8_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 8
CPC_C9_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 9
EIC_OPTION	Uns32	Override the external interrupt controller
		EIC_OPTION
guestCtl0RI	Uns32	Override the RI field in GuestCtl0 register
guestCtl0MC	Uns32	Override the MC field in GuestCtl0 register
guestCtl0CP0	Uns32	Override the CP0 field in GuestCtl0 register
guestCtl0AT	Uns32	Override the AT field in GuestCtl0 register
guestCtl0GT	Uns32	Override the GT field in GuestCtl0 register
guestCtl0CG	Uns32	Override the CG field in GuestCtl0 register
guestCtl0CF	Uns32	Override the CF field in GuestCtl0 register
guestCtl0G1	Uns32	Override the G1 field in GuestCtl0 register
guestCtl0RAD	Uns32	Override the RAD field in GuestCtl0 register
guestCtl0DRG	Uns32	Override the DRG field in GuestCtl0 register
hasImpl17	Boolean	Enable read/write of Impl17 bit in Status register
hasImpl16	Boolean	Enable read/write of Impl16 bit in Status register
guestintctlIPTI	Uns32	Override the Guest IPTI field in IntCtl register
guestintctlIPFDC	Uns32	Override the Guest IPFDC field in IntCtl register
guestintctlIPPCI	Uns32	Override the Guest IPPCI field in IntCtl register
guestintctlIPTI_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for
musetint et IIDTI CDI 10 VD1	II20	CPU0/VP0
guestintctlIPTI_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
		OF 00/ VF1

guestintctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
guestintctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
guestintctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
guestintctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
guestintctlIPTI_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
guestintctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
guestintctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
guestintctlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
guestintctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
guestintctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
guestintctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
guestintctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
guestintctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
guestintctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
guestintctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
guestintctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
guestintctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
guestintctlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
guestintctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
guestintctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
guestintctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
guestintctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
guestintctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
guestintctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
guestintctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
guestintctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
guestintctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
guestintctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1

guestintctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
guestintctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
$guest intctlIPFDC_CPU0_VP0$	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
guestintctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
guestintctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
guestintctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
guestintctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
guestintctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
$guest int ctlIPFDC_CPU1_VP2$	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
guestintctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
guestintctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0
guestintctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
guestintctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
guestintctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
guestintctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
guestintctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
guestintctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
guestintctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
guestintctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0
guestintctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1
guestintctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
guestintctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
guestintctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
guestintctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
$guest intctlIPFDC_CPU5_VP2$	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
guestintctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
guestintctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
guestintctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1

$guestintctlIPFDC_CPU6_VP2$	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2
guestintctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
guestintctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
guestintctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
guestintctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
guestintctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
guestintctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
guestintctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
guestintctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
guestintctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
guestintctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0
guestintctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP1
guestintctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
guestintctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
guestintctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
guestintctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
guestintctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
guestintctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
guestintctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0
guestintctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1
guestintctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP2
guestintctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
guestintctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
guestintctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
guestintctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
guestintctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
guestintctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0
guestintctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1

guestintctlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2
guestintctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
guestintctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
guestintctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP1
guestintctlIPPCI_CPU6_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP2
guestintctlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
guestintctlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
guestintctlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
guestintctlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
guestintctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
ISPRAM_SIZE	Uns32	Encoded size of the ISPRAM region (log2(<ispram bytes="" in="" size="">) - 11)</ispram>
ISPRAM_BASE	Uns64	Starting physical address of the ISPRAM region
ISPRAM_ENABLE	Boolean	Set the enable bit of the ISPRAM region's tag (used to enable the ISPRAM region prior to reset)
ISPRAM_FILE	String	Load a MIPS hex file into the ISPRAM region prior to reset
DSPRAM_SIZE	Uns32	Encoded size of the DSPRAM region (log2(<dspram bytes="" in="" size="">) - 11)</dspram>
DSPRAM_BASE	Uns64	Starting physical address of the DSPRAM region
DSPRAM_ENABLE	Boolean	Set the enable bit of the DSPRAM region's tag (used to enable the DSPRAM region prior to re- set)
DSPRAM_PRESENT	Boolean	DSPRAM is present with SAAR
USPRAM_SIZE	Uns32	Encoded size of the USPRAM region (log2(<uspram bytes="" in="" size="">) - 11)</uspram>
USPRAM_BASE	Uns64	Starting physical address of the USPRAM region
USPRAM_ENABLE	Boolean	Set the enable bit of the USPRAM region's tag (used to enable the USPRAM region prior to reset)
USPRAM_FILE	String	Load a MIPS hex file into the USPRAM region prior to reset
misaligned Data Exception	Enumeration	Select misaligned data access exception signaling: never, checkCCA or always (never, checkCCA or always)
commitTlbwErr	Boolean	Commit TLBWI/TLBRI on ECC; in MIPS_DV_MODE only

Table 8.3: Parameters that can be set in: VP

Execution Modes

Mode	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3

Table 9.1: Modes implemented in: CMP

Mode	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3
GUEST_KERNEL	4
GUEST_SUPERVISOR	5
GUEST_USER	6

Table 9.2: Modes implemented in: CPU

Mode	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3
GUEST_KERNEL	4
GUEST_SUPERVISOR	5
GUEST_USER	6

Table 9.3: Modes implemented in: VP

Exceptions

Exception	Code
Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Вр	9
RI	10
CpU	11
Ov	12
Tr	13
MSAFPE	14
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MSADis	21
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
GE	27
Prot	29
CacheErr	30

Table 10.1: Exceptions implemented in: CMP $\,$

Exception	Code
Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Вр	9
RI	10
CpU	11
Ov	12
Tr	13
MSAFPE	14
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MSADis	21
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
GE	27
Prot	29
CacheErr	30

Table 10.2: Exceptions implemented in: CPU

Exception	Code
Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Вр	9

RI	10
CpU	11
Ov	12
Tr	13
MSAFPE	14
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MSADis	21
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
GE	27
Prot	29
CacheErr	30

Table 10.3: Exceptions implemented in: VP

Hierarchy of the model

A CPU core may be configured to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.

OVP processor models can be written to include SMP blocks and to have many levels of hierarchy. Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

11.1 Level 1: CMP

This level in the model hierarchy has 2 commands. This level in the model hierarchy has no register groups. This level in the model hierarchy has 2 children: CPU0 and CPU1.

11.2 Level 2: CPU

This level in the model hierarchy has 2 commands. This level in the model hierarchy has no register groups. This level in the model hierarchy has 4 children: CPU0_VP0, CPU0_VP1, CPU0_VP2 and CPU0_VP3.

11.3 Level 3: VP

This level in the model hierarchy has 20 commands. This level in the model hierarchy has 10 register groups:

Group name	Registers
Core	65
FPU	34

DSP	9
Shadow	64
COP0	174
MSA	40
CMP_GCR	36
CMP_CPC	14
CMP_GIC	721
Integration_support	1

Table 11.1: Register groups

This level in the model hierarchy has no children.

Model Commands

A Processor model can implement one or more **Model Commands** available to be invoked from the simulator command line, from the OP API or from the Imperas Multiprocessor Debugger.

12.1 Level 1: CMP

12.1.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.1: isync command arguments

12.1.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.2: itrace command arguments

12.2 Level 2: CPU

12.2.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.3: isync command arguments

12.2.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.4: itrace command arguments

12.3 Level 3: VP

12.3.1 isync

specify instruction address range for synchronous execution

Argument		*
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.5: isync command arguments

12.3.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.6: itrace command arguments

12.3.3 mipsCOP0

query a COP0 register value using <register><select>

Argument	Type	Description
-register	Uns32	specify the COP0 register resource
-select	Uns32	specify the COP0 register select

Table 12.7: mipsCOP0 command arguments

12.3.4 mipsCacheDisable

12.3.4.1 Argument description

Disables tag or full cache model

12.3.5 mipsCacheEnable

enable tag or full cache model

Argument	Type	Description
-debug	Int32	set cache model debug flags
-full	Boolean	enable full cache model
-tag	Boolean	enable cache tag line only model

Table 12.8: mipsCacheEnable command arguments

12.3.6 mipsCacheRatio

Report current hit ratio for selected cache

Argument	Type	Description
-dcache	Boolean	report hit ratio for dcache
-icache	Boolean	report hit ratio for icache

Table 12.9: mipsCacheRatio command arguments

12.3.7 mipsCacheReport

12.3.7.1 Argument description

Report current cache statistics

12.3.8 mipsCacheReset

12.3.8.1 Argument description

reset the cache model

12.3.9 mipsCacheTrace

Control the tracing of cache accesses

Argument	Type	Description
-noartifact	Boolean	
-nocached	Boolean	
-nodcache	Boolean	
-noicache	Boolean	
-notrue	Boolean	
-nouncached	Boolean	
-off	Boolean	turn off the cache tracing
-on	Boolean	turn on the cache tracing

Table 12.10: mipsCacheTrace command arguments

12.3.10 mipsDebugFlags

Set the mips model debug value

Argument	Type	Description
-value	Uns32	specify mips model debug flags

Table 12.11: mipsDebugFlags command arguments

12.3.11 mipsReadRegister

Read processor register using <resource><offset>

Argument	Type	Description
-offset	Uns32	the register offset
-resource	Uns32	the register resource

Table 12.12: mipsReadRegister command arguments

12.3.12 mipsReadTLBEntry

read a TLB entry specified by the index

Argument	Type	Description
-index	Uns64	select the TLB entry

Table 12.13: mipsReadTLBEntry command arguments

12.3.13 mipsTLBDump

12.3.13.1 Argument description

Dumps the current contents of the TLB

12.3.14 mipsTLBDumpGuest

12.3.14.1 Argument description

Dumps the current contents of the Guest TLB

12.3.15 mipsTLBDumpRoot

12.3.15.1 Argument description

Dumps the current contents of the Root TLB

12.3.16 mipsTLBGetPhys

Reports the entry(s) in the TLB that match the given virtual address and ASID

Argument	Type	Description
-asid	Uns64	ASID
-va	Uns64	virtual address

Table 12.14: mipsTLBGetPhys command arguments

12.3.17 mipsTraceGuest

control tracing of guest

Argument	Type	Description
-off	Boolean	stop tracing
-on	Boolean	start tracing

Table 12.15: mipsTraceGuest command arguments

12.3.18 mipsTraceRoot

control tracing on root processor

Argument	Type	Description
-off	Boolean	stop tracing
-on	Boolean	start tracing

Table 12.16: mipsTraceRoot command arguments

12.3.19 mipsWriteRegister

Write processor register using <resource><offset><value>

Argument	Type	Description
-offset	Uns32	the register offset
-resource	Uns32	the register resource
-value	Uns64	the value to write to register

Table 12.17: mipsWriteRegister command arguments

12.3.20 mipsWriteTLBEntry

Writes values to a TLB entry using the index, lo0, lo1, hi0 and mask fields

Argument	Type	Description
-hi0	Uns64	the TLB entry high address
-index	Uns64	the TLB entry index
-lo0	Uns64	the TLB entry low address 0
-lo1	Uns64	the TLB entry low address 1
-mask	Uns64	the TLB entry mask

Table 12.18: mipsWriteTLBEntry command arguments

Registers

13.1 Level 1: CMP

No registers.

13.2 Level 2: CPU

No registers.

13.3 Level 3: VP

13.3.1 Core

Registers at level:3, type:VP group:Core

Name	Bits	Initial-Hex	RW	Description
zero	64	0	r-	constant zero
at	64	0	rw	
v0	64	0	rw	
v1	64	0	rw	
a0	64	0	rw	
a1	64	0	rw	
a2	64	0	rw	
a3	64	0	rw	
t0	64	0	rw	
t1	64	0	rw	
t2	64	0	rw	
t3	64	0	rw	
t4	64	0	rw	
t5	64	0	rw	
t6	64	0	rw	
t7	64	0	rw	
s0	64	0	rw	
s1	64	0	rw	
s2	64	0	rw	
s3	64	0	rw	
s4	64	0	rw	
s5	64	0	rw	
s6	64	0	rw	

18	s7	64	0	rw	
t9 64 0 rw k0 64 0 rw k1 64 0 rw gp 64 0 rw sp 64 0 rw sp 64 0 rw ra 64 0 rw pc 64 ffffffffffffff rw r0 64 0 rw r1 64 0 rw r2 64 0 rw r3 64 0 rw r4 64 0 rw r5 64 0 rw r6 64 0 rw r8 64 0 rw r8 64 0 rw r9 64 0 rw r10 64 0 rw r11 64 0 rw r12 64 0					
k0 64 0 rw gp 64 0 rw sp 64 0 rw sp 64 0 rw s8 64 0 rw ra 64 0 rw pc 64 ffffffff rw pc 64 0 rw r0 64 0 rw r1 64 0 rw r2 64 0 rw r3 64 0 rw r4 64 0 rw r6 64 0 rw r6 64 0 rw r9 64 0 rw r10 64 0 rw r12 64 0 rw r13 64 0 rw r12 64 0 rw r12 64 0					
K1					
gp 64 0 rw stack pointer s8 64 0 rw stack pointer ra 64 0 rw frame pointer ra 64 0 rw program counter ra 64 0 rw rconstant zero ra 64 0 rw rw ra 64 0 rw ra ra rw ra <t< td=""><td></td><td></td><td></td><td></td><td></td></t<>					
sp 64 0 rw stack pointer ra 64 0 rw frame pointer ra 64 0 rw frame pointer ra 64 0 rw program counter r0 64 0 rw rw r1 64 0 rw r2 64 0 rw r3 64 0 rw r4 64 0 rw r5 64 0 rw r6 64 0 rw r8 64 0 rw r10 64 0 rw r11 64 0 rw r12 64 0 rw r13 64 0 rw r14 64 0 rw r15 64 0 rw r16 64 0 rw r17					
s8 64 0 rw frame pointer pc 64 0 rw program counter pc 64 0 rw program counter n0 64 0 rw respectively r1 64 0 rw respectively r2 64 0 rw respectively r3 64 0 rw respectively r4 64 0 rw respectively r5 64 0 rw respectively respectively r8 64 0 rw respectively respectively respectively r10 64 0 rw respectively respectively respectively r12 64 0 rw respectively respectively respectively respectively r17 64 0 rw respectively respectively respectively respectively respectively respecti					stack pointer
Ta	sp s8	1			
DC					name pointer
r0 64 0 r- constant zero r1 64 0 rw r2 64 0 rw r3 64 0 rw r4 64 0 rw r5 64 0 rw r6 64 0 rw r7 64 0 rw r9 64 0 rw r10 64 0 rw r11 64 0 rw r13 64 0 rw r13 64 0 rw r14 64 0 rw r15 64 0 rw r16 64 0 rw r17 64 0 rw r19 64 0 rw r19 64 0 rw r19 64 0 rw r20					program counter
r1 64 0 rw r2 64 0 rw r3 64 0 rw r4 64 0 rw r5 64 0 rw r6 64 0 rw r7 64 0 rw r8 64 0 rw r9 64 0 rw r10 64 0 rw r12 64 0 rw r13 64 0 rw r14 64 0 rw r16 64 0 rw r17 64 0 rw r18 64 0 rw r19 64 0 rw r12 64 0 rw r19 64 0 rw r20 64 0 rw r22 64 0	рс		bfc00000	1 00	program counter
r2 64 0 rw r3 64 0 rw r4 64 0 rw r5 64 0 rw r6 64 0 rw r7 64 0 rw r8 64 0 rw r10 64 0 rw r11 64 0 rw r11 64 0 rw r13 64 0 rw r14 64 0 rw r15 64 0 rw r16 64 0 rw r17 64 0 rw r18 64 0 rw r19 64 0 rw r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0				r-	constant zero
r3 64 0 rw r5 64 0 rw r6 64 0 rw r6 64 0 rw r7 64 0 rw r8 64 0 rw r9 64 0 rw r10 64 0 rw r11 64 0 rw r12 64 0 rw r13 64 0 rw r15 64 0 rw r16 64 0 rw r17 64 0 rw r19 64 0 rw r20 64 0 rw r21 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r24 64 0				rw	
r4 64 0 rw r5 64 0 rw r6 64 0 rw r7 64 0 rw r8 64 0 rw r9 64 0 rw r10 64 0 rw r11 64 0 rw r13 64 0 rw r14 64 0 rw r15 64 0 rw r16 64 0 rw r18 64 0 rw r19 64 0 rw r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r24 64 0 rw r25 64 0 rw r26 64 0				rw	
r5 64 0 rw r6 64 0 rw r7 64 0 rw r8 64 0 rw r10 64 0 rw r11 64 0 rw r11 64 0 rw r13 64 0 rw r14 64 0 rw r15 64 0 rw r16 64 0 rw r18 64 0 rw r19 64 0 rw r20 64 0 rw r21 64 0 rw r23 64 0 rw r24 64 0 rw r25 64 0 rw r26 64 0 rw r28 64 0 rw r29 64 0				rw	
r6 64 0 rw r7 64 0 rw r8 64 0 rw r9 64 0 rw r10 64 0 rw r11 64 0 rw r13 64 0 rw r14 64 0 rw r15 64 0 rw r16 64 0 rw r17 64 0 rw r18 64 0 rw r19 64 0 rw r20 64 0 rw r22 64 0 rw r23 64 0 rw r25 64 0 rw r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0				rw	
r7 64 0 rw r8 64 0 rw r9 64 0 rw r10 64 0 rw r11 64 0 rw r12 64 0 rw r13 64 0 rw r14 64 0 rw r15 64 0 rw r16 64 0 rw r17 64 0 rw r18 64 0 rw r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw r29 64 0 <td></td> <td></td> <td></td> <td>rw</td> <td></td>				rw	
r8 64 0 rw r9 64 0 rw r10 64 0 rw r11 64 0 rw r12 64 0 rw r13 64 0 rw r14 64 0 rw r15 64 0 rw r16 64 0 rw r17 64 0 rw r18 64 0 rw r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r25 64 0 rw r25 64 0 rw r27 64 0 rw r28 64 0 rw r29 64 0 rw frame pointer				rw	
r9 64 0 rw r10 64 0 rw r11 64 0 rw r12 64 0 rw r13 64 0 rw r14 64 0 rw r15 64 0 rw r16 64 0 rw r17 64 0 rw r18 64 0 rw r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw r29 64 0 rw frame pointer				rw	
r10 64 0 rw r11 64 0 rw r12 64 0 rw r13 64 0 rw r14 64 0 rw r15 64 0 rw r16 64 0 rw r17 64 0 rw r18 64 0 rw r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r24 64 0 rw r25 64 0 rw r27 64 0 rw r28 64 0 rw r29 64 0 rw frame pointer				rw	
r11 64 0 rw r12 64 0 rw r13 64 0 rw r14 64 0 rw r15 64 0 rw r16 64 0 rw r17 64 0 rw r19 64 0 rw r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r24 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw r29 64 0 rw frame pointer				rw	
r12 64 0 rw r13 64 0 rw r14 64 0 rw r15 64 0 rw r16 64 0 rw r17 64 0 rw r19 64 0 rw r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r24 64 0 rw r25 64 0 rw r26 64 0 rw r28 64 0 rw r29 64 0 rw frame pointer				rw	
r13 64 0 rw r14 64 0 rw r15 64 0 rw r16 64 0 rw r17 64 0 rw r18 64 0 rw r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r24 64 0 rw r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw stack pointer r30 64 0 rw frame pointer				rw	
r14 64 0 rw r15 64 0 rw r16 64 0 rw r17 64 0 rw r18 64 0 rw r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r24 64 0 rw r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw r29 64 0 rw frame pointer				rw	
r15 64 0 rw r16 64 0 rw r17 64 0 rw r18 64 0 rw r19 64 0 rw r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r24 64 0 rw r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw stack pointer r30 64 0 rw frame pointer				rw	
r16 64 0 rw r17 64 0 rw r18 64 0 rw r19 64 0 rw r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r24 64 0 rw r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw stack pointer r30 64 0 rw frame pointer				rw	
r17 64 0 rw r18 64 0 rw r19 64 0 rw r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r24 64 0 rw r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw stack pointer r30 64 0 rw frame pointer			0	rw	
r18 64 0 rw r19 64 0 rw r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r24 64 0 rw r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw r29 64 0 rw frame pointer			0	rw	
r19 64 0 rw r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r24 64 0 rw r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw r29 64 0 rw frame pointer				rw	
r20 64 0 rw r21 64 0 rw r22 64 0 rw r23 64 0 rw r24 64 0 rw r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw r29 64 0 rw frame pointer				rw	
r21 64 0 rw r22 64 0 rw r23 64 0 rw r24 64 0 rw r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw r29 64 0 rw stack pointer r30 64 0 rw frame pointer			0	rw	
r22 64 0 rw r23 64 0 rw r24 64 0 rw r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw r29 64 0 rw stack pointer r30 64 0 rw frame pointer				rw	
r23 64 0 rw r24 64 0 rw r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw r29 64 0 rw stack pointer r30 64 0 rw frame pointer				rw	
r24 64 0 rw r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw r29 64 0 rw stack pointer r30 64 0 rw frame pointer				rw	
r25 64 0 rw r26 64 0 rw r27 64 0 rw r28 64 0 rw r29 64 0 rw stack pointer r30 64 0 rw frame pointer			0	rw	
r26 64 0 rw r27 64 0 rw r28 64 0 rw r29 64 0 rw stack pointer r30 64 0 rw frame pointer			0	rw	
r27 64 0 rw r28 64 0 rw r29 64 0 rw stack pointer r30 64 0 rw frame pointer				rw	
r28 64 0 rw r29 64 0 rw stack pointer r30 64 0 rw frame pointer				rw	
r29 64 0 rw stack pointer r30 64 0 rw frame pointer				rw	
r30 64 0 rw frame pointer	r28	64	0	rw	
			0	rw	stack pointer
	r30	64	0	rw	
r31 64 0 rw	r31	64	0	rw	

Table 13.1: Registers at level 3, type:VP group:Core

13.3.2 FPU

Registers at level:3, type:VP group:FPU

Name	Bits	Initial-Hex	RW	Description
f0	64	0	rw	
f1	64	0	rw	
f2	64	0	rw	
f3	64	0	rw	
f4	64	0	rw	

f5 64 f6 64 f7 64 f8 64 f9 64 f10 64 f11 64 f12 64 f13 64 f14 64 f15 64 f16 64	64 0 64 0 64 0 64 0 64 0 64 0 64 0 64 0 64 0 64 0 64 0 64 0 64 0 64 0	rw rw rw rw rw rw rw rw rw	
f7 64 f8 64 f9 64 f10 64 f11 64 f12 64 f13 64 f14 64 f15 64	34 0 34 0 34 0 34 0 34 0 34 0 34 0 34 0 34 0 34 0	rw rw rw rw rw rw rw rw	
f8 64 f9 64 f10 64 f11 64 f12 64 f13 64 f14 64 f15 64	34 0 34 0 34 0 34 0 34 0 34 0 34 0 34 0 34 0 34 0	rw rw rw rw rw rw rw	
f9 64 f10 64 f11 64 f12 64 f13 64 f14 64 f15 64	64 0 64 0 64 0 64 0 64 0 64 0 64 0 64 0	rw rw rw rw rw rw	
f10 64 f11 64 f12 64 f13 64 f14 64 f15 64	34 0 34 0 34 0 34 0 34 0 34 0 34 0	rw rw rw rw	
f11 64 f12 64 f13 64 f14 64 f15 64	64 0 64 0 64 0 64 0 64 0 64 0	rw rw rw	
f12 64 f13 64 f14 64 f15 64	64 0 64 0 64 0 64 0	rw rw rw	
f13 64 f14 64 f15 64	64 0 64 0 64 0	rw rw	
f14 64 f15 64	64 0 64 0	rw	
f15 64	64 0		
		2717	
f16 64	64 0	rw	
	- 0	rw	
f17 64	64 0	rw	
f18 64	64 0	rw	
f19 64	64 0	rw	
f20 64	64 0	rw	
f21 64	64 0	rw	
f22 64	64 0	rw	
f23 64	64 0	rw	
f24 64	64 0	rw	
f25 64	64 0	rw	
f26 64	64 0	rw	
f27 64		rw	
f28 64		rw	
f29 64	64 0	rw	
f30 64	64 0	rw	
f31 64	64 0	rw	
fsr 64	64 c0000	rw	floating point status
fir 64	34 20f30320	r-	floating point information

Table 13.2: Registers at level 3, type:VP group:FPU

13.3.3 DSP

Registers at level:3, type:VP group:DSP

Name	Bits	Initial-Hex	RW	Description
lo	64	0	rw	
hi	64	0	rw	
lo1	64	0	rw	
hi1	64	0	rw	
lo2	64	0	rw	
hi2	64	0	rw	
lo3	64	0	rw	
hi3	64	0	rw	
dspctl	64	0	rw	DSP control

Table 13.3: Registers at level 3, type:VP group:DSP

13.3.4 Shadow

Registers at level:3, type:VP group:Shadow

Name	Bits	Initial-Hex	RW	Description	
zero[0]	64	0	r-	constant zero	

at[0]	64	0	rw	
v0[0]	64	0	rw	
v1[0]	64	0	rw	
a0[0]	64	0	rw	
a1[0]	64	0	rw	
a2[0]	64	0	rw	
a3[0]	64	0	rw	
t0[0]	64	0	rw	
t1[0]	64	0	rw	
t2[0]	64	0	rw	
t3[0]	64	0	rw	
t4[0]	64	0	rw	
t5[0]	64	0	rw	
t6[0]	64	0	rw	
t7[0]	64	0	_	
s0[0]	64	0	rw	
	64	0	rw	
s1[0] s2[0]	64	0	rw	
	64		rw	
s3[0]		0	rw	
s4[0]	64	0	rw	
s5[0]	64	0	rw	
s6[0]	64	0	rw	
s7[0]	64	0	rw	
t8[0]	64	0	rw	
t9[0]	64	0	rw	
k0[0]	64	0	rw	
k1[0]	64	0	rw	
[[]				
gp[0]	64	0	rw	
sp[0]	64	0	rw rw	stack pointer
$\frac{\operatorname{sp}[0]}{\operatorname{s8}[0]}$	64 64	0	_	stack pointer frame pointer
sp[0] s8[0] ra[0]	64 64 64	0 0 0	rw	frame pointer
sp[0] s8[0] ra[0] r0[0]	64 64 64 64	0 0 0 0	rw rw	
sp[0] s8[0] ra[0] r0[0] r1[0]	64 64 64 64	0 0 0 0	rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0]	64 64 64 64 64	0 0 0 0 0	rw rw rw r-	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0]	64 64 64 64 64 64	0 0 0 0	rw rw rw r- rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0]	64 64 64 64 64	0 0 0 0 0	rw rw rw r- rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0]	64 64 64 64 64 64 64 64	0 0 0 0 0 0	rw rw rw r- rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0]	64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0	rw rw rw r- rw rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0]	64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0	rw rw rw r- rw rw rw rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0]	64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0	rw rw rw r- rw rw rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0]	64 64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0 0	rw rw rw r- rw rw rw rw rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0]	64 64 64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0 0 0	rw rw rw r- rw rw rw rw rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0]	64 64 64 64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0 0 0 0	rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r9[0] r10[0]	64 64 64 64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0 0 0 0 0	rw	frame pointer
sp[0] s8[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r9[0] r10[0] r11[0] r12[0]	64 64 64 64 64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r13[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r13[0] r14[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] ra[0] ra[0] ra[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r13[0] r14[0] r15[0] r3[0] r15[0] r15[0] r3[0] r15[0] r15[0] r3[0] r3[0] r15[0] r3[0] r3[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] ra[0] ra[0] ra[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r13[0] r14[0] r15[0] r16[0] rage rag	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] ra[0	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] ss[0] ra[0] ra[0	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r14[0] r15[0] r15[0] r16[0] r17[0] r18[0] r19[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r14[0] r15[0] r15[0] r16[0] r17[0] r18[0] r19[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r14[0] r15[0] r15[0] r15[0] r16[0] r17[0] r18[0] r19[0] r20[0] r21[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r14[0] r15[0] r14[0] r15[0] r16[0] r17[0] r18[0] r19[0] r20[0] r22[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] ra[0	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer

r25[0]	64	0	rw	
r26[0]	64	0	rw	
r27[0]	64	0	rw	
r28[0]	64	0	rw	
r29[0]	64	0	rw	stack pointer
r30[0]	64	0	rw	frame pointer
r31[0]	64	0	rw	

Table 13.4: Registers at level 3, type:VP group:Shadow

13.3.5 COP0

Registers at level:3, type:VP group:COP0

Name	Bits	Initial-Hex	RW	Description
sr	64	4400004	rw	CP0 register 12/0 (status)
bad	64	0	rw	CP0 register 8/0 (badvaddr)
cause	64	0	rw	CP0 register 13/0 (cause)
index	64	0	rw	CP0 register 0/0
vpcontrol	64	0	rw	CP0 register 0/4
entrylo0	64	0	rw	CP0 register 2/0
entrylo1	64	0	rw	CP0 register 3/0
globalnumber	64	0	rw	CP0 register 3/1
context	64	0	rw	CP0 register 4/0
userlocal	64	0	rw	CP0 register 4/2
pagemask	64	0	rw	CP0 register 5/0
pagegrain	64	c8000000	rw	CP0 register 5/1
wired	64	0	rw	CP0 register 6/0
hwrena	64	0	rw	CP0 register 7/0
badvaddr	64	0	rw	CP0 register 8/0
badinstr	64	0	rw	CP0 register 8/1
badinstrp	64	0	rw	CP0 register 8/2
count	64	0	rw	CP0 register 9/0
entryhi	64	0	rw	CP0 register 10/0
guestctl1	64	0	rw	CP0 register 10/4
guestctl2	64	0	rw	CP0 register 10/5
guestctl3	64	0	rw	CP0 register 10/6
compare	64	0	rw	CP0 register 11/0
guestctl0ext	64	80	rw	CP0 register 11/4
status	64	4400004	rw	CP0 register 12/0
intctl	64	e0000000	rw	CP0 register 12/1
srsctl	64	0	rw	CP0 register 12/2
srsmap	64	0	rw	CP0 register 12/3
guestctl0	64	c4c0080	rw	CP0 register 12/6
gtoffset	64	0	rw	CP0 register 12/7
epc	64	0	rw	CP0 register 14/0
prid	64	1ac00	rw	CP0 register 15/0
ebase	64	ffffffff	rw	CP0 register 15/1
		80000000		
cmgcrbase	64	1fbf800	rw	CP0 register 15/3
config	64	8000ca02	rw	CP0 register 16/0
config1	64	9eab5593	rw	CP0 register 16/1
config2	64	80000000	rw	CP0 register 16/2
config3	64	fc8031e1	rw	CP0 register 16/3
config4	64	d0fc0227	rw	CP0 register 16/4
config5	64	498	rw	CP0 register 16/5

	T 0.4	La		GD0 1 1 10/0
config6	64	0	rw	CP0 register 16/6
config7	64	80000000	rw	CP0 register 16/7
lladdr	64	0	rw	CP0 register 17/0
maar	64	0	rw	CP0 register 17/1
maari	64	0	rw	CP0 register 17/2
xcontext	64	0	rw	CP0 register 20/0
debug	64	2008000	rw	CP0 register 23/0
tracecontrol	64	0	rw	CP0 register 23/1
tracecontrol2	64	0	rw	CP0 register 23/2
usertracedata	64	0	rw	CP0 register 23/3
traceibpc	64	0	rw	CP0 register 23/4
tracedbpc	64	0	rw	CP0 register 23/5
ibp2_3_action	64	0	rw	CP0 register 23/7
depc	64	0	rw	CP0 register 24/0
dbp2_3_action	64	0	rw	CP0 register 24/1
tracecontrol3	64	0	rw	CP0 register 24/2
usertracedata2	64	0	rw	CP0 register 24/3
tcbconfig	64	0	rw	CP0 register 24/4
tcbcontrole	64	0	rw	CP0 register 24/5
ibp4_5_action	64	0	rw	CP0 register 24/6
ibp6_7_action	64	0	rw	CP0 register 24/7
perfctl0	64	80000000	rw	CP0 register 25/0
perfcnt0	64	0	rw	CP0 register 25/1
perfctl1	64	80000000	rw	CP0 register 25/2
perfent1	64	0	rw	CP0 register 25/3
perfettl2	64	80000000	rw	CP0 register 25/4
perfent2	64	0	rw	CP0 register 25/5
perfett3	64	0	rw	CP0 register 25/6
perfent3	64	0	rw	CP0 register 25/7
errctl	64	0	rw	CP0 register 26/0
tcbcontrold	64	0	rw	CP0 register 26/4
cacheerr	64	0	rw	CP0 register 27/0
	64	0		CP0 register 28/0
itaglo idatalo	64	0	rw	CP0 register 28/1
	64	0	rw	CP0 register 28/1 CP0 register 28/2
dtaglo		_	rw	
ddatalo	64	0	rw	CP0 register 28/3
itaghi	64	0	rw	CP0 register 29/0
idatahi	64	0	rw	CP0 register 29/1
dtaghi	64	0	rw	CP0 register 29/2
ddatahi	64	0	rw	CP0 register 29/3
errorepc	64	0	rw	CP0 register 30/0
desave	64	0	rw	CP0 register 31/0
kscratch1	64	0	rw	CP0 register 31/2
kscratch2	64	0	rw	CP0 register 31/3
kscratch3	64	0	rw	CP0 register 31/4
kscratch4	64	0	rw	CP0 register 31/5
kscratch5	64	0	rw	CP0 register 31/6
kscratch6	64	0	rw	CP0 register 31/7
guestindex	64	0	rw	CP0 guest register 0/0
guestvpcontrol	64	0	rw	CP0 guest register 0/4
guestentrylo0	64	0	rw	CP0 guest register 2/0
guestentrylo1	64	0	rw	CP0 guest register 3/0
guestglobalnumber	64	0	rw	CP0 guest register 3/1
guestcontext	64	0	rw	CP0 guest register 4/0
guestuserlocal	64	0	rw	CP0 guest register 4/2
guestpagemask	64	0	rw	CP0 guest register 5/0
OIO	1	L -		

guestymen 64 0 rv CPG guest register 5/1 guesthwenn 64 0 rv CPG guest register 6/0 guesthaddr 64 0 rv CPG guest register 8/0 guesthadinstr 64 0 rv CPG guest register 8/2 guestcount 64 0 rv CPG guest register 10/0 guesthadinstr 64 0 rv CPG guest register 10/0 guesthadinstr 64 0 rv CPG guest register 10/0 guestguester 11 64 0 rv CPG guest register 10/0 guestguester 13 64 0 rv CPG guest register 10/0 guestguester 13 64 0 rv CPG guest register 10/6 guestguester 13 64 0 rv CPG guest register 10/6 guestguester 13 64 0 rv CPG guest register 10/6 guestguester 13 64 0 rv CPG guest register 10/6 guestguester 13 64 0 rv CPG guest register 10/6 guestguester 13 64 0 rv CPG guest register 11/4 gueststatus 64 4000000 rv CPG guest register 11/4 gueststatus 64 0 rv CPG guest register 12/1 guestspand 64 0 rv CPG guest register 12/1 guestguester 64 0 rv CPG guest register 12/2 guestguester 64 0 rv CPG guest register 12/3 guestguester 64 0 rv CPG guest register 12/7 guestprid 64 0 rv CPG guest register 13/0 guestprid 64 0 rv CPG guest register 13/0 guester guester 64 0 rv CPG guest register 13/0 guester 64 0 rv CPG guest register 13/0 guester 64 0 rv CPG guest register 14/0 guester 64 0 rv CPG guest register 16/0 guester 64 0 rv CPG guest register 24/0 guester 64 0 rv CPG guest register 24/0 gue		T 0.4		1	CODO
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guestusertracedata2 64 0 rw CP0 guest register 24/3 guesttcbconfig 64 0 rw CP0 guest register 24/4 guesttcbcontrole 64 0 rw CP0 guest register 24/5 guestibp4_5_action 64 0 rw CP0 guest register 24/6 guestibp6_7_action 64 0 rw CP0 guest register 24/7 guestperfctl0 64 80000000 rw CP0 guest register 25/0 guestperfctl1 64 80000000 rw CP0 guest register 25/1 guestperfctl1 64 80000000 rw CP0 guest register 25/2				-	
guesttcbconfig 64 0 rw CP0 guest register 24/4 guesttcbcontrole 64 0 rw CP0 guest register 24/5 guestibp4_5_action 64 0 rw CP0 guest register 24/6 guestibp6_7_action 64 0 rw CP0 guest register 24/7 guestperfctl0 64 80000000 rw CP0 guest register 25/0 guestperfctl0 64 0 rw CP0 guest register 25/1 guestperfctl1 64 80000000 rw CP0 guest register 25/2	_				
guesttcbcontrole 64 0 rw CP0 guest register 24/5 guestibp4_5_action 64 0 rw CP0 guest register 24/6 guestibp6_7_action 64 0 rw CP0 guest register 24/7 guestperfctl0 64 80000000 rw CP0 guest register 25/0 guestperfcnt0 64 0 rw CP0 guest register 25/1 guestperfctl1 64 80000000 rw CP0 guest register 25/2	_				
guestibp4_5_action 64 0 rw CP0 guest register 24/6 guestibp6_7_action 64 0 rw CP0 guest register 24/7 guestperfctl0 64 80000000 rw CP0 guest register 25/0 guestperfcnt0 64 0 rw CP0 guest register 25/1 guestperfctl1 64 80000000 rw CP0 guest register 25/2	_			rw	
guestibp6-7_action 64 0 rw CP0 guest register 24/7 guestperfctl0 64 80000000 rw CP0 guest register 25/0 guestperfcnt0 64 0 rw CP0 guest register 25/1 guestperfctl1 64 80000000 rw CP0 guest register 25/2				rw	
guestperfctl0 64 80000000 rw CP0 guest register 25/0 guestperfcnt0 64 0 rw CP0 guest register 25/1 guestperfctl1 64 80000000 rw CP0 guest register 25/2				rw	
guestperfcnt0 64 0 rw CP0 guest register 25/1 guestperfctl1 64 80000000 rw CP0 guest register 25/2			_	rw	
guestperfctl1 64 80000000 rw CP0 guest register 25/2			80000000	rw	
			_	rw	
guestperfcnt1 64 0 rw CP0 guest register 25/3			80000000	rw	
	guestperfcnt1	64	0	rw	CP0 guest register 25/3

guestperfctl2	64	80000000	rw	CP0 guest register 25/4
guestperfcnt2	64	0	rw	CP0 guest register 25/5
guestperfctl3	64	0	rw	CP0 guest register 25/6
guestperfcnt3	64	0	rw	CP0 guest register 25/7
guesterrctl	64	0	rw	CP0 guest register 26/0
guesttcbcontrold	64	0	rw	CP0 guest register 26/4
guestcacheerr	64	0	rw	CP0 guest register 27/0
guestitaglo	64	0	rw	CP0 guest register 28/0
guestidatalo	64	0	rw	CP0 guest register 28/1
guestdtaglo	64	0	rw	CP0 guest register 28/2
guestddatalo	64	0	rw	CP0 guest register 28/3
guestitaghi	64	0	rw	CP0 guest register 29/0
guestidatahi	64	0	rw	CP0 guest register 29/1
guestdtaghi	64	0	rw	CP0 guest register 29/2
guestddatahi	64	0	rw	CP0 guest register 29/3
guesterrorepc	64	0	rw	CP0 guest register 30/0
guestdesave	64	0	rw	CP0 guest register 31/0
guestkscratch1	64	0	rw	CP0 guest register 31/2
guestkscratch2	64	0	rw	CP0 guest register 31/3
guestkscratch3	64	0	rw	CP0 guest register 31/4
guestkscratch4	64	0	rw	CP0 guest register 31/5
guestkscratch5	64	0	rw	CP0 guest register 31/6
guestkscratch6	64	0	rw	CP0 guest register 31/7

Table 13.5: Registers at level 3, type:VP group:COP0

13.3.6 MSA

Registers at level:3, type:VP group:MSA

Name	Bits	Initial-Hex	RW	Description
w0	128	-	rw	
w1	128	-	rw	
w2	128	-	rw	
w3	128	-	rw	
w4	128	-	rw	
w5	128	-	rw	
w6	128	-	rw	
w7	128	-	rw	
w8	128	-	rw	
w9	128	-	rw	
w10	128	-	rw	
w11	128	-	rw	
w12	128	-	rw	
w13	128	-	rw	
w14	128	-	rw	
w15	128	-	rw	
w16	128	-	rw	
w17	128	-	rw	
w18	128	-	rw	
w19	128	-	rw	
w20	128	-	rw	
w21	128	-	rw	
w22	128	-	rw	
w23	128	-	rw	
w24	128	-	rw	

w25	128	_	rw	
w26	128	-	rw	
w27	128	-	rw	
w28	128	-	rw	
w29	128	-	rw	
w30	128	-	rw	
w31	128	-	rw	
msair	64	320	r-	MSA implementation
msacsr	64	0	rw	MSA control and status
msaaccess	64	-	r-	MSA access
msasave	64	-	r-	MSA save
msamodify	64	-	r-	MSA modify
msarequest	64	-	r-	MSA request
msamap	64	-	r-	MSA map
msaunmap	64	-	r-	MSA unmap

Table 13.6: Registers at level 3, type:VP group:MSA

13.3.7 CMP_GCR

Registers at level:3, type: VP group: CMP_GCR

Name	Bits	Initial-Hex	RW	Description
GCR_CONFIG	64	1	r-	-
GCR_BASE	64	1fbf8000	r-	
GCR_BASE_UPPER	64	0	rw	
GCR_CONTROL	64	40200000	rw	
GCR_REV	64	800	r-	
GCR_ERROR_CONTROL	64	13	rw	
GCR_ERROR_MASK	64	0	rw	
GCR_ERROR_CAUSE	64	0	r-	
GCR_ERROR_ADDR	64	0	r-	
GCR_ERROR_ADDR_UPPER	64	0	-	
GCR_ERROR_MULT	64	0	r-	
GCR_CUSTOM_BASE	64	0	rw	
GCR_CUSTOM_STATUS	64	0	r-	
GCR_GIC_BASE	64	0	rw	
GCR_GIC_BASE_UPPER	64	0	rw	
GCR_CPC_BASE	64	0	rw	
GCR_CPC_BASE_UPPER	64	0	rw	
GCR_GIC_STATUS	64	1	r-	
GCR_CACHE_REV	64	0	r-	
GCR_CPC_STATUS	64	1	r-	
GCR_ACCESS	64	3f	rw	
GCR_L2_CONFIG	64	0	rw	
GCR_SYS_CONFIG2	64	0	r-	
GCR_IOCU1_REV	64	400	r-	
GCR_BEV_BASE	64	bfc00000	rw	
GCR_MMIO_REQ_LIMIT	64	0	rw	
GCR_CL_COHERENCE	64	0	rw	
GCR_CL_CONFIG	64	3	r-	
GCR_CL_OTHER	64	0	rw	
GCR_CL_RESET_BASE	64	bfc00001	rw	
GCR_CL_ID	64	0	r-	
GCR_CO_COHERENCE	64	0	rw	
GCR_CO_CONFIG	64	3	r-	

GCR_CO_OTHER	64	0	rw	
GCR_CO_RESET_BASE	64	bfc00001	rw	
GCR_CO_ID	64	0	r-	

Table 13.7: Registers at level 3, type:VP group:CMP_GCR

13.3.8 CMP_CPC

Registers at level:3, type:VP group:CMP_CPC

Name	Bits	Initial-Hex	RW	Description
CPC_SEQDEL	64	0	rw	
CPC_RAIL	64	0	rw	
CPC_RESETLEN	64	0	rw	
CPC_REVISION	64	0	r-	
CPC_CMD	64	3	rw	
CPC_STAT_CONF	64	b37203	rw	
CPC_CL_VP_STOP	64	0	rw	
CPC_CL_VP_RUN	64	1	rw	
CPC_CL_VP_RUNNING	64	1	r-	
CPC_CMD	64	3	rw	
CPC_STAT_CONF	64	b37203	rw	
CPC_CO_VP_STOP	64	0	rw	
CPC_CO_VP_RUN	64	1	rw	
CPC_CO_VP_RUNNING	64	1	r-	

Table 13.8: Registers at level 3, type:VP group:CMP_CPC

13.3.9 CMP_GIC

Registers at level:3, type:VP group:CMP_GIC

Name	Bits	Initial-Hex	RW	Description
GIC_SH_CONFIG	64	980f0007	rw	
GIC_Counter	64	0	rw	
GIC_SH_REVISION	64	500	r-	
GIC_SH_POL63_0	64	0	rw	
GIC_SH_POL127_64	64	0	rw	
GIC_SH_POL191_128	64	0	rw	
GIC_SH_POL255_192	64	0	rw	
GIC_SH_TRIG63_0	64	0	rw	
GIC_SH_TRIG127_64	64	0	rw	
GIC_SH_TRIG191_128	64	0	rw	
GIC_SH_TRIG255_192	64	0	rw	
GIC_SH_DUAL63_0	64	0	rw	
GIC_SH_DUAL127_64	64	0	rw	
GIC_SH_DUAL191_128	64	0	rw	
GIC_SH_DUAL255_192	64	0	rw	
GIC_SH_WEDGE	64	0	-w	
GIC_SH_RMASK63_0	64	0	-w	
GIC_SH_RMASK127_64	64	0	-w	
GIC_SH_RMASK191_128	64	0	-w	
GIC_SH_RMASK255_192	64	0	-w	
GIC_SH_SMASK63_0	64	0	-w	
GIC_SH_SMASK127_64	64	0	-W	

GIC_SH_SMASK191_128	64	0	-w	
GIC_SH_SMASK255_192	64	0	-w	
GIC_SH_MASK63_0	64	0	r-	
GIC_SH_MASK127_64	64	0	r-	
GIC_SH_MASK191_128	64	0	r-	
GIC_SH_MASK255_192	64	0	r-	
GIC_SH_PEND63_0	64	0	r-	
GIC_SH_PEND127_64	64	0	r-	
GIC_SH_PEND191_128	64	0	r-	
GIC_SH_PEND255_192	64	0	r-	
GIC_SH_MAP000_PIN	64	80000000	rw	
GIC_SH_MAP001_PIN	64	80000000	rw	
GIC_SH_MAP002_PIN	64	80000000	rw	
GIC_SH_MAP003_PIN	64	80000000	rw	
GIC_SH_MAP004_PIN	64	80000000	rw	
GIC_SH_MAP005_PIN	64	80000000	rw	
GIC_SH_MAP006_PIN	64	80000000	rw	
GIC_SH_MAP007_PIN	64	80000000	rw	
GIC_SH_MAP008_PIN	64	80000000	rw	
GIC_SH_MAP009_PIN	64	80000000	rw	
GIC_SH_MAP010_PIN	64	80000000	rw	
GIC_SH_MAP011_PIN	64	80000000	rw	
GIC_SH_MAP012_PIN	64	80000000	rw	
GIC_SH_MAP013_PIN	64	80000000	rw	
GIC_SH_MAP014_PIN	64	80000000	rw	
GIC_SH_MAP015_PIN	64	80000000	rw	
GIC_SH_MAP016_PIN	64	80000000	rw	
GIC_SH_MAP017_PIN	64	80000000	rw	
GIC_SH_MAP018_PIN	64	80000000	rw	
GIC_SH_MAP019_PIN	64	80000000	rw	
GIC_SH_MAP020_PIN	64	80000000	rw	
GIC_SH_MAP021_PIN	64	80000000	rw	
GIC_SH_MAP022_PIN	64	80000000	rw	
GIC_SH_MAP023_PIN	64	80000000	rw	
GIC_SH_MAP024_PIN	64	80000000	rw	
GIC_SH_MAP025_PIN	64	80000000	rw	
GIC_SH_MAP026_PIN	64	80000000	rw	
GIC_SH_MAP027_PIN	64	80000000	rw	
GIC_SH_MAP028_PIN	64	80000000	rw	
GIC_SH_MAP029_PIN	64	80000000	rw	
GIC_SH_MAP030_PIN	64	80000000	rw	
GIC_SH_MAP031_PIN	64	80000000		
GIC_SH_MAP031_PIN	64	80000000	rw	
GIC_SH_MAP032_PIN GIC_SH_MAP033_PIN	64	80000000	rw	
GIC_SH_MAP033_PIN GIC_SH_MAP034_PIN	64	80000000	rw	
GIC_SH_MAP034_PIN GIC_SH_MAP035_PIN	64		rw	
		80000000	rw	
GIC_SH_MAP036_PIN	64	80000000	rw	
GIC_SH_MAP037_PIN	64	80000000	rw	
GIC_SH_MAP038_PIN	64	80000000	rw	
GIC_SH_MAP039_PIN	64	80000000	rw	
GIC_SH_MAP040_PIN	64	80000000	rw	
GIC_SH_MAP041_PIN	64	80000000	rw	
GIC_SH_MAP042_PIN	64	80000000	rw	
GIC_SH_MAP043_PIN	64	80000000	rw	
GIC_SH_MAP044_PIN	64	80000000	rw	
GIC_SH_MAP045_PIN	64	80000000	rw	

GIC_SH_MAP046_PIN	64	80000000	rw	
GIC_SH_MAP047_PIN	64	80000000	rw	
GIC_SH_MAP048_PIN	64	80000000	rw	
GIC_SH_MAP049_PIN	64	80000000	rw	
GIC_SH_MAP050_PIN	64	80000000	rw	
GIC_SH_MAP051_PIN	64	80000000	rw	
GIC_SH_MAP052_PIN	64	80000000	rw	
GIC_SH_MAP053_PIN	64	80000000	rw	
GIC_SH_MAP054_PIN	64	80000000	rw	
GIC_SH_MAP055_PIN	64	80000000	rw	
GIC_SH_MAP056_PIN	64	80000000	rw	
GIC_SH_MAP057_PIN	64	80000000	rw	
GIC_SH_MAP058_PIN	64	80000000	rw	
GIC_SH_MAP059_PIN	64	80000000	rw	
GIC_SH_MAP060_PIN	64	80000000	rw	
GIC_SH_MAP061_PIN	64	80000000	rw	
GIC_SH_MAP062_PIN	64	80000000	rw	
GIC_SH_MAP063_PIN	64	80000000	rw	
GIC_SH_MAP064_PIN	64	80000000	rw	
GIC_SH_MAP065_PIN	64	80000000	rw	
GIC_SH_MAP066_PIN	64	80000000	rw	
GIC_SH_MAP067_PIN	64	80000000	rw	
GIC_SH_MAP068_PIN	64	80000000	rw	
GIC_SH_MAP069_PIN	64	80000000	rw	
GIC_SH_MAP070_PIN	64	80000000	rw	
GIC_SH_MAP071_PIN	64	80000000	rw	
GIC_SH_MAP072_PIN	64	8000000	rw	
GIC_SH_MAP073_PIN	64	8000000	rw	
GIC_SH_MAP074_PIN	64	8000000	rw	
GIC_SH_MAP075_PIN	64	8000000	rw	
GIC_SH_MAP076_PIN	64	8000000	rw	
GIC_SH_MAP077_PIN	64	8000000	rw	
GIC_SH_MAP078_PIN	64	8000000		
GIC_SH_MAP079_PIN	64	80000000	rw	
GIC_SH_MAP080_PIN	64	8000000	rw	
GIC_SH_MAP081_PIN	64	80000000	rw	
GIC_SH_MAP081_PIN			rw	
GIC_SH_MAP082_PIN GIC_SH_MAP083_PIN	64	80000000	rw	
GIC_SH_MAP083_PIN GIC_SH_MAP084_PIN	-	80000000	rw	
	64	80000000	rw	
GIC_SH_MAP085_PIN	64	80000000	rw	
GIC_SH_MAP086_PIN	64	80000000	rw	
GIC_SH_MAP087_PIN	64	80000000	rw	
GIC_SH_MAP088_PIN	64	80000000	rw	
GIC_SH_MAP089_PIN	64	80000000	rw	
GIC_SH_MAP090_PIN	64	80000000	rw	
GIC_SH_MAP091_PIN	64	80000000	rw	
GIC_SH_MAP092_PIN	64	80000000	rw	
GIC_SH_MAP093_PIN	64	80000000	rw	
GIC_SH_MAP094_PIN	64	80000000	rw	
GIC_SH_MAP095_PIN	64	80000000	rw	
GIC_SH_MAP096_PIN	64	80000000	rw	
GIC_SH_MAP097_PIN	64	80000000	rw	
GIC_SH_MAP098_PIN	64	80000000	rw	
GIC_SH_MAP099_PIN	64	80000000	rw	
GIC_SH_MAP100_PIN	64	80000000	rw	
GIC_SH_MAP101_PIN	64	80000000	rw	

GIC_SH_MAP102_PIN	64	80000000	rw	
GIC_SH_MAP103_PIN	64	80000000	rw	
GIC_SH_MAP104_PIN	64	80000000	rw	
GIC_SH_MAP105_PIN	64	80000000	rw	
GIC_SH_MAP106_PIN	64	80000000	rw	
GIC_SH_MAP107_PIN	64	80000000	rw	
GIC_SH_MAP108_PIN	64	80000000	rw	
GIC_SH_MAP109_PIN	64	80000000	rw	
GIC_SH_MAP110_PIN	64	80000000	rw	
GIC_SH_MAP111_PIN	64	80000000	rw	
GIC_SH_MAP112_PIN	64	80000000	rw	
GIC_SH_MAP113_PIN	64	80000000	rw	
GIC_SH_MAP114_PIN	64	80000000	rw	
GIC_SH_MAP115_PIN	64	80000000	rw	
GIC_SH_MAP116_PIN	64	80000000	rw	
GIC_SH_MAP117_PIN	64	80000000	rw	
GIC_SH_MAP118_PIN	64	80000000	rw	
GIC_SH_MAP119_PIN	64	80000000	rw	
GIC_SH_MAP120_PIN	64	8000000	rw	
GIC_SH_MAP121_PIN	64	8000000	rw	
GIC_SH_MAP122_PIN	64	80000000	rw	
GIC_SH_MAP123_PIN	64	8000000		
GIC_SH_MAP124_PIN	64	8000000	rw	
GIC_SH_MAP125_PIN	64	8000000	rw	
GIC_SH_MAP126_PIN	64	8000000	rw	
GIC_SH_MAP120_FIN	64	80000000	rw	
	-		rw	
GIC_SH_MAP128_PIN	64	0	rw	
GIC_SH_MAP129_PIN	64	_	rw	
GIC_SH_MAP130_PIN	64	0	rw	
GIC_SH_MAP131_PIN	64	0	rw	
GIC_SH_MAP132_PIN	64	0	rw	
GIC_SH_MAP133_PIN	64	0	rw	
GIC_SH_MAP134_PIN	64	0	rw	
GIC_SH_MAP135_PIN	64	0	rw	
GIC_SH_MAP136_PIN	64	0	rw	
GIC_SH_MAP137_PIN	64	0	rw	
GIC_SH_MAP138_PIN	64	0	rw	
GIC_SH_MAP139_PIN	64	0	rw	
GIC_SH_MAP140_PIN	64	0	rw	
GIC_SH_MAP141_PIN	64	0	rw	
GIC_SH_MAP142_PIN	64	0	rw	
GIC_SH_MAP143_PIN	64	0	rw	
GIC_SH_MAP144_PIN	64	0	rw	
GIC_SH_MAP145_PIN	64	0	rw	
GIC_SH_MAP146_PIN	64	0	rw	
GIC_SH_MAP147_PIN	64	0	rw	
GIC_SH_MAP148_PIN	64	0	rw	
GIC_SH_MAP149_PIN	64	0	rw	
GIC_SH_MAP150_PIN	64	0	rw	
GIC_SH_MAP151_PIN	64	0	rw	
GIC_SH_MAP152_PIN	64	0	rw	
GIC_SH_MAP153_PIN	64	0	rw	
GIC_SH_MAP154_PIN	64	0	rw	
GIC_SH_MAP155_PIN	64	0	rw	
GIC_SH_MAP156_PIN	64	0	rw	
GIC_SH_MAP157_PIN	64	0	rw	
	-	1		1

		_		
GIC_SH_MAP158_PIN	64	0	rw	
GIC_SH_MAP159_PIN	64	0	rw	
GIC_SH_MAP160_PIN	64	0	rw	
GIC_SH_MAP161_PIN	64	0	rw	
GIC_SH_MAP162_PIN	64	0	rw	
GIC_SH_MAP163_PIN	64	0	rw	
GIC_SH_MAP164_PIN	64	0	rw	
GIC_SH_MAP165_PIN	64	0	rw	
GIC_SH_MAP166_PIN	64	0	rw	
GIC_SH_MAP167_PIN	64	0	rw	
GIC_SH_MAP168_PIN	64	0	rw	
GIC_SH_MAP169_PIN	64	0	rw	
GIC_SH_MAP170_PIN	64	0	rw	
GIC_SH_MAP171_PIN	64	0	rw	
GIC_SH_MAP172_PIN	64	0	rw	
GIC_SH_MAP173_PIN	64	0		
GIC_SH_MAP174_PIN	64	0	rw	
		-	rw	
GIC_SH_MAP175_PIN	64	0	rw	
GIC_SH_MAP176_PIN	64	0	rw	
GIC_SH_MAP177_PIN	64	0	rw	
GIC_SH_MAP178_PIN	64	0	rw	
GIC_SH_MAP179_PIN	64	0	rw	
GIC_SH_MAP180_PIN	64	0	rw	
GIC_SH_MAP181_PIN	64	0	rw	
GIC_SH_MAP182_PIN	64	0	rw	
GIC_SH_MAP183_PIN	64	0	rw	
GIC_SH_MAP184_PIN	64	0	rw	
GIC_SH_MAP185_PIN	64	0	rw	
GIC_SH_MAP186_PIN	64	0	rw	
GIC_SH_MAP187_PIN	64	0	rw	
GIC_SH_MAP188_PIN	64	0	rw	
GIC_SH_MAP189_PIN	64	0	rw	
GIC_SH_MAP190_PIN	64	0	rw	
GIC_SH_MAP191_PIN	64	0	rw	
GIC_SH_MAP192_PIN	64	0	rw	
GIC_SH_MAP193_PIN	64	0	rw	
GIC_SH_MAP194_PIN	64	0	rw	
GIC_SH_MAP195_PIN	64	0	rw	
GIC_SH_MAP196_PIN	64	0	rw	
GIC_SH_MAP197_PIN	64	0	rw	
GIC_SH_MAP198_PIN	64	0	rw	
GIC_SH_MAP199_PIN	64	0		
GIC_SH_MAP199_PIN GIC_SH_MAP200_PIN	64	0	rw	
		-	rw	
GIC_SH_MAP201_PIN	64	0	rw	
GIC_SH_MAP202_PIN	64	0	rw	
GIC_SH_MAP203_PIN	64	0	rw	
GIC_SH_MAP204_PIN	64	0	rw	
GIC_SH_MAP205_PIN	64	0	rw	
GIC_SH_MAP206_PIN	64	0	rw	
GIC_SH_MAP207_PIN	64	0	rw	
GIC_SH_MAP208_PIN	64	0	rw	
GIC_SH_MAP209_PIN	64	0	rw	
GIC_SH_MAP210_PIN	64	0	rw	
GIC_SH_MAP211_PIN	64	0	rw	
GIC_SH_MAP212_PIN	64	0	rw	
GIC_SH_MAP213_PIN	64	0	rw	
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GIC_SH_MAP214_PIN	64	0	rw	
GIC_SH_MAP215_PIN	64	0	rw	
GIC_SH_MAP216_PIN	64	0	rw	
GIC_SH_MAP217_PIN	64	0	rw	
GIC_SH_MAP218_PIN	64	0	rw	
GIC_SH_MAP219_PIN	64	0	rw	
GIC_SH_MAP220_PIN	64	0	rw	
GIC_SH_MAP221_PIN	64	0	rw	
GIC SH_MAP222_PIN	64	0	rw	
GIC SH MAP223 PIN	64	0	rw	
GIC_SH_MAP224_PIN	64	0	rw	
GIC_SH_MAP225_PIN	64	0	rw	
GIC_SH_MAP226_PIN	64	0	rw	
GIC_SH_MAP227_PIN	64	0	rw	
GIC_SH_MAP228_PIN	64	0		
GIC_SH_MAP229_PIN	64	0	rw	
GIC_SH_MAP230_PIN	64	0	rw	
GIC_SH_MAP231_PIN	64		rw	
		0	rw	
GIC_SH_MAP232_PIN	64	0	rw	
GIC_SH_MAP233_PIN	64	0	rw	
GIC_SH_MAP234_PIN	64	0	rw	
GIC_SH_MAP235_PIN	64	0	rw	
GIC_SH_MAP236_PIN	64	0	rw	
GIC_SH_MAP237_PIN	64	0	rw	
GIC_SH_MAP238_PIN	64	0	rw	
GIC_SH_MAP239_PIN	64	0	rw	
GIC_SH_MAP240_PIN	64	0	rw	
GIC_SH_MAP241_PIN	64	0	rw	
GIC_SH_MAP242_PIN	64	0	rw	
GIC_SH_MAP243_PIN	64	0	rw	
GIC_SH_MAP244_PIN	64	0	rw	
GIC_SH_MAP245_PIN	64	0	rw	
GIC_SH_MAP246_PIN	64	0	rw	
GIC_SH_MAP247_PIN	64	0	rw	
GIC_SH_MAP248_PIN	64	0	rw	
GIC_SH_MAP249_PIN	64	0	rw	
GIC_SH_MAP250_PIN	64	0	rw	
GIC_SH_MAP251_PIN	64	0	rw	
GIC_SH_MAP252_PIN	64	0	rw	
GIC_SH_MAP253_PIN	64	0	rw	
GIC_SH_MAP254_PIN	64	0	rw	
GIC_SH_MAP255_PIN	64	0	rw	
GIC_SH_MAP000_VPE31_0	64	0	rw	
GIC_SH_MAP001_VPE31_0	64	0	rw	
GIC_SH_MAP002_VPE31_0	64	0	rw	
GIC_SH_MAP003_VPE31_0	64	0	rw	
GIC_SH_MAP004_VPE31_0	64	0		
GIC_SH_MAP004_VPE31_0	64	0	rw	
GIC_SH_MAP005_VPE31_0		_	rw	
	64	0	rw	
GIC_SH_MAP007_VPE31_0	64	0	rw	
GIC_SH_MAP008_VPE31_0	64	0	rw	
GIC_SH_MAP009_VPE31_0	64	0	rw	
GIC_SH_MAP010_VPE31_0	64	0	rw	
GIC_SH_MAP011_VPE31_0	64	0	rw	
GIC_SH_MAP012_VPE31_0	64	0	rw	
GIC_SH_MAP013_VPE31_0	64	0	rw	

GIC_SH_MAP014_VPE31_0	64	0	rw	
GIC_SH_MAP015_VPE31_0	64	0	rw	
GIC_SH_MAP016_VPE31_0	64	0	rw	
GIC_SH_MAP017_VPE31_0	64	0	rw	
GIC_SH_MAP018_VPE31_0	64	0	rw	
GIC_SH_MAP019_VPE31_0	64	0	rw	
GIC_SH_MAP020_VPE31_0	64	0	rw	
GIC_SH_MAP021_VPE31_0	64	0	rw	
GIC_SH_MAP022_VPE31_0	64	0	rw	
GIC_SH_MAP023_VPE31_0	64	0	rw	
GIC_SH_MAP024_VPE31_0	64	0	rw	
GIC_SH_MAP025_VPE31_0	64	0	rw	
GIC_SH_MAP026_VPE31_0	64	0	rw	
GIC_SH_MAP027_VPE31_0	64	0	rw	
GIC_SH_MAP028_VPE31_0	64	0	rw	
GIC_SH_MAP029_VPE31_0	64	0	rw	
GIC_SH_MAP030_VPE31_0	64	0	rw	
GIC_SH_MAP031_VPE31_0	64	0	rw	
GIC_SH_MAP032_VPE31_0	64	0	rw	
GIC_SH_MAP033_VPE31_0	64	0	rw	
GIC_SH_MAP034_VPE31_0	64	0		
GIC_SH_MAP035_VPE31_0	64	0	rw	
GIC_SH_MAP036_VPE31_0	64	0	rw	
GIC SH MAP036 VPE31 0	_	-	rw	
0.0000000000000000000000000000000000000	64	0	rw	
GIC_SH_MAP038_VPE31_0	64	0	rw	
GIC_SH_MAP039_VPE31_0	64	0	rw	
GIC_SH_MAP040_VPE31_0	64	0	rw	
GIC_SH_MAP041_VPE31_0	64	0	rw	
GIC_SH_MAP042_VPE31_0	64	0	rw	
GIC_SH_MAP043_VPE31_0	64	0	rw	
GIC_SH_MAP044_VPE31_0	64	0	rw	
GIC_SH_MAP045_VPE31_0	64	0	rw	
GIC_SH_MAP046_VPE31_0	64	0	rw	
GIC_SH_MAP047_VPE31_0	64	0	rw	
GIC_SH_MAP048_VPE31_0	64	0	rw	
GIC_SH_MAP049_VPE31_0	64	0	rw	
GIC_SH_MAP050_VPE31_0	64	0	rw	
GIC_SH_MAP051_VPE31_0	64	0	rw	
GIC_SH_MAP052_VPE31_0	64	0	rw	
GIC_SH_MAP053_VPE31_0	64	0	rw	
GIC_SH_MAP054_VPE31_0	64	0	rw	
GIC_SH_MAP055_VPE31_0	64	0	rw	
GIC_SH_MAP056_VPE31_0	64	0	rw	
GIC_SH_MAP057_VPE31_0	64	0	rw	
GIC_SH_MAP058_VPE31_0	64	0	rw	
GIC_SH_MAP059_VPE31_0	64	0	rw	
GIC_SH_MAP060_VPE31_0	64	0	rw	
GIC_SH_MAP061_VPE31_0	64	0	rw	
GIC_SH_MAP062_VPE31_0	64	0	rw	
GIC_SH_MAP063_VPE31_0	64	0	rw	
GIC_SH_MAP064_VPE31_0	64	0	rw	
GIC_SH_MAP065_VPE31_0	64	0	rw	
GIC_SH_MAP066_VPE31_0	64	0	rw	
GIC_SH_MAP067_VPE31_0	64	0	rw	
GIC_SH_MAP068_VPE31_0	64	0		
GIC_SH_MAP069_VPE31_0	64	0	rw rw	
G10_D11_W171 003_V1 1201_0	04	9	ı vv	

GIC_SH_MAP070_VPE31_0	64	0	rw	
GIC_SH_MAP071_VPE31_0	64	0	rw	
GIC_SH_MAP072_VPE31_0	64	0	rw	
GIC_SH_MAP073_VPE31_0	64	0	rw	
GIC_SH_MAP074_VPE31_0	64	0	rw	
GIC_SH_MAP075_VPE31_0	64	0	rw	
GIC_SH_MAP076_VPE31_0	64	0	rw	
GIC_SH_MAP077_VPE31_0	64	0	rw	
GIC_SH_MAP078_VPE31_0	64	0	rw	
GIC SH MAP079 VPE31 0	64	0	rw	
GIC_SH_MAP080_VPE31_0	64	0	rw	
GIC_SH_MAP081_VPE31_0	64	0	rw	
GIC_SH_MAP082_VPE31_0	64	0	rw	
GIC_SH_MAP083_VPE31_0	64	0	rw	
GIC_SH_MAP084_VPE31_0	64	0	rw	
GIC_SH_MAP085_VPE31_0	64	0	rw	
GIC_SH_MAP086_VPE31_0	64	0	rw	
GIC_SH_MAP087_VPE31_0	64	0	rw	
GIC_SH_MAP088_VPE31_0	64	0		
GIC_SH_MAP088_VPE31_0	64	0	rw	
GIC_SH_MAP089_VPE31_0	64	0	rw	
GIC_SH_MAP090_VPE31_0	64	0	rw	
GIC_SH_MAP091_VPE31_0		-	rw	
	64	0	rw	
GIC_SH_MAP093_VPE31_0	64	0	rw	
GIC_SH_MAP094_VPE31_0	64	0	rw	
GIC_SH_MAP095_VPE31_0	64	0	rw	
GIC_SH_MAP096_VPE31_0	64	0	rw	
GIC_SH_MAP097_VPE31_0	64	0	rw	
GIC_SH_MAP098_VPE31_0	64	0	rw	
GIC_SH_MAP099_VPE31_0	64	0	rw	
GIC_SH_MAP100_VPE31_0	64	0	rw	
GIC_SH_MAP101_VPE31_0	64	0	rw	
GIC_SH_MAP102_VPE31_0	64	0	rw	
GIC_SH_MAP103_VPE31_0	64	0	rw	
GIC_SH_MAP104_VPE31_0	64	0	rw	
GIC_SH_MAP105_VPE31_0	64	0	rw	
GIC_SH_MAP106_VPE31_0	64	0	rw	
GIC_SH_MAP107_VPE31_0	64	0	rw	
GIC_SH_MAP108_VPE31_0	64	0	rw	
GIC_SH_MAP109_VPE31_0	64	0	rw	
GIC_SH_MAP110_VPE31_0	64	0	rw	
GIC_SH_MAP111_VPE31_0	64	0	rw	
GIC_SH_MAP112_VPE31_0	64	0	rw	
GIC_SH_MAP113_VPE31_0	64	0	rw	
GIC_SH_MAP114_VPE31_0	64	0	rw	
GIC_SH_MAP115_VPE31_0	64	0	rw	
GIC_SH_MAP116_VPE31_0	64	0	rw	
GIC_SH_MAP117_VPE31_0	64	0	rw	
GIC_SH_MAP118_VPE31_0	64	0	rw	
GIC_SH_MAP119_VPE31_0	64	0	rw	
GIC_SH_MAP120_VPE31_0	64	0	rw	
GIC_SH_MAP121_VPE31_0	64	0	rw	
GIC_SH_MAP122_VPE31_0	64	0	rw	
GIC_SH_MAP123_VPE31_0	64	0	rw	
GIC_SH_MAP124_VPE31_0	64	0	rw	
GIC_SH_MAP125_VPE31_0	64	0	rw	
010_011_WIII 120_V1 E01_0	1 04	U	1 44	

GICS.BH.MAP126.VPB31.0 64 0 rw GICS.BH.MAP128.VPB31.0 64 0 rw GICS.BH.MAP129.VPB31.0 64 0 rw GICS.BH.MAP130.VPB31.0 64 0 rw GICS.BH.MAP131.VPB31.0 64 0 rw GICS.BH.MAP131.VPB31.0 64 0 rw GICS.BH.MAP131.VPB31.0 64 0 rw GICS.BH.MAP132.VPB31.0 64 0 rw GICS.BH.MAP132.VPB31.0 64 0 rw GICS.BH.MAP134.VPB31.0 64 0 rw GICS.BH.MAP134.VPB31.0 64 0 rw GICS.BH.MAP134.VPB31.0 64 0 rw GICS.BH.MAP136.VPB31.0 64 0 rw GICS.BH.MAP149.VPB31.0 64 0 rw GICS.BH.MAP140.VPB31.0 64 0 rw GICS.BH.MAP140.VPB31.0 64 0 rw GICS.BH.MAP140.VPB31.0 64 0 rw GICS.BH.MAP144.VPB31.0 64 0 rw GICS.BH.MAP145.VPB31.0 64 0 rw GICS.BH.MAP145.VPB31.0 64 0 rw GICS.BH.MAP146.VPB31.0 64 0 rw GICS.BH.MAP147.VPB31.0 64 0 rw GICS.BH.MAP148.VPB31.0 64 0 rw GICS.BH.MAP147.VPB31.0 64 0 rw GICS.BH.MAP149.VPB31.0 64 0 rw GICS.BH.MAP159.VPB31.0 64 0 rw GICS.BH.MAP159.VPB31.0 64 0 rw GICS.BH.MAP159.VPB31.0 64 0 rw GICS.BH.MAP159.VPB31.0 64 0 rw GICS.BH.MAP169.VPB31.0 64 0 rw					
GIC SILMAP128-VPF31.0 64 0 rw GIC SILMAP130-VF831.0 64 0 rw GIC SILMAP130-VF831.0 64 0 rw GIC SILMAP131-VF831.0 64 0 rw GIC SILMAP131-VF831.0 64 0 rw GIC SILMAP132-VF831.0 64 0 rw GIC SILMAP132-VF831.0 64 0 rw GIC SILMAP133-VF831.0 64 0 rw GIC SILMAP134-VF831.0 64 0 rw GIC SILMAP135-VF831.0 64 0 rw GIC SILMAP136-VF831.0 64 0 rw GIC SILMAP136-VF831.0 64 0 rw GIC SILMAP136-VF831.0 64 0 rw GIC SILMAP138-VF831.0 64 0 rw GIC SILMAP138-VF831.0 64 0 rw GIC SILMAP139-VF831.0 64 0 rw GIC SILMAP139-VF831.0 64 0 rw GIC SILMAP140-VF831.0 64 0 rw GIC SILMAP141-VF831.0 64 0 rw GIC SILMAP141-VF831.0 64 0 rw GIC SILMAP141-VF831.0 64 0 rw GIC SILMAP145-VF831.0 64 0 rw GIC SILMAP155-VF831.0 64 0 rw GIC SILMAP165-VF831.0 64 0 rw GIC SILMAP165-VF831.0 64 0 rw GIC SILMAP165-VF831.0 64 0 rw GIC SILMAP160-VF831.0 64 0 rw GIC SILMAP170-VF831.0 64 0 rw GIC SI	GIC_SH_MAP126_VPE31_0	64	0	rw	
GIC.SILMAP130.VPE31.0 64 0 rw GIC.SILMAP131.VPE31.0 64 0 rw GIC.SILMAP131.VPE31.0 64 0 rw GIC.SILMAP133.VPE31.0 64 0 rw GIC.SILMAP133.VPE31.0 64 0 rw GIC.SILMAP133.VPE31.0 64 0 rw GIC.SILMAP133.VPE31.0 64 0 rw GIC.SILMAP134.VPE31.0 64 0 rw GIC.SILMAP135.VPE31.0 64 0 rw GIC.SILMAP135.VPE31.0 64 0 rw GIC.SILMAP135.VPE31.0 64 0 rw GIC.SILMAP136.VPE31.0 64 0 rw GIC.SILMAP140.VPE31.0 64 0 rw GIC.SILMAP140.VPE31.0 64 0 rw GIC.SILMAP141.VPE31.0 64 0 rw GIC.SILMAP147.VPE31.0 64 0 rw GIC.SILMAP147.VPE31.0 64 0 rw GIC.SILMAP147.VPE31.0 64 0 rw GIC.SILMAP145.VPE31.0 64 0 rw GIC.SILMAP155.VPE31.0 64 0 rw GIC.SILMAP156.VPE31.0 64 0 rw GIC.SILMAP157.VPE31.0 64 0 rw GIC.SILMAP157.VPE31.0 64 0 rw GIC.SILMAP159.VPE31.0 64 0 rw GIC.SILMAP159.VPE31.0 64 0 rw GIC.SILMAP164.VPE31.0 64 0 rw GIC.SILMAP157.VPE31.0 64 0 rw GIC.SI	GIC_SH_MAP127_VPE31_0	64	0	rw	
GIC SH MAP130 VPE31.0 64 0 rw GIC SH MAP131 VPE31.0 64 0 rw GIC SH MAP132 VPE31.0 64 0 rw GIC SH MAP132 VPE31.0 64 0 rw GIC SH MAP134 VPE31.0 64 0 rw GIC SH MAP136 VPE31.0 64 0 rw GIC SH MAP137 VPE31.0 64 0 rw GIC SH MAP138 VPE31.0 64 0 rw GIC SH MAP136 VPE31.0 64 0 rw GIC SH MAP140 VPE31.0 64 0 rw GIC SH MAP141 VPE31.0 64 0 rw GIC SH MAP141 VPE31.0 64 0 rw GIC SH MAP143 VPE31.0 64 0 rw GIC SH MAP145 VPE31.0 64 0 rw GIC SH MAP150 VPE31.0 64 0 rw GIC SH MAP170 VPE31.0 64 0 rw GIC SH MAP170 VPE31.0 64 0 rw GIC SH	GIC_SH_MAP128_VPE31_0	64	0	rw	
GIC SH MAP131 VPE31.0 64 0 rw GIC SH MAP132 VPE31.0 64 0 rw GIC SH MAP133 VPE31.0 64 0 rw GIC SH MAP133 VPE31.0 64 0 rw GIC SH MAP135 VPE31.0 64 0 rw GIC SH MAP135 VPE31.0 64 0 rw GIC SH MAP135 VPE31.0 64 0 rw GIC SH MAP137 VPE31.0 64 0 rw GIC SH MAP138 VPE31.0 64 0 rw GIC SH MAP138 VPE31.0 64 0 rw GIC SH MAP138 VPE31.0 64 0 rw GIC SH MAP139 VPE31.0 64 0 rw GIC SH MAP140 VPE31.0 64 0 rw GIC SH MAP140 VPE31.0 64 0 rw GIC SH MAP140 VPE31.0 64 0 rw GIC SH MAP141 VPE31.0 64 0 rw GIC SH MAP141 VPE31.0 64 0 rw GIC SH MAP142 VPE31.0 64 0 rw GIC SH MAP144 VPE31.0 64 0 rw GIC SH MAP145 VPE31.0 64 0 rw GIC SH MAP15 VPE31.0 64 0 rw GIC SH MAP16 VPE31.0 64 0 rw GIC SH MAP17 VPE31.0 64 0 rw GIC SH MAP16 VPE31.0 64 0 rw GIC SH MAP17 VPE31.0 64 0 rw GIC SH MAP17	GIC_SH_MAP129_VPE31_0	64	0	rw	
GIC SH MAP131 VPE31.0 64 0 rw GIC SH MAP132 VPE31.0 64 0 rw GIC SH MAP133 VPE31.0 64 0 rw GIC SH MAP133 VPE31.0 64 0 rw GIC SH MAP135 VPE31.0 64 0 rw GIC SH MAP135 VPE31.0 64 0 rw GIC SH MAP135 VPE31.0 64 0 rw GIC SH MAP137 VPE31.0 64 0 rw GIC SH MAP138 VPE31.0 64 0 rw GIC SH MAP138 VPE31.0 64 0 rw GIC SH MAP138 VPE31.0 64 0 rw GIC SH MAP139 VPE31.0 64 0 rw GIC SH MAP140 VPE31.0 64 0 rw GIC SH MAP140 VPE31.0 64 0 rw GIC SH MAP140 VPE31.0 64 0 rw GIC SH MAP141 VPE31.0 64 0 rw GIC SH MAP141 VPE31.0 64 0 rw GIC SH MAP142 VPE31.0 64 0 rw GIC SH MAP144 VPE31.0 64 0 rw GIC SH MAP145 VPE31.0 64 0 rw GIC SH MAP15 VPE31.0 64 0 rw GIC SH MAP16 VPE31.0 64 0 rw GIC SH MAP17 VPE31.0 64 0 rw GIC SH MAP16 VPE31.0 64 0 rw GIC SH MAP17 VPE31.0 64 0 rw GIC SH MAP17	GIC_SH_MAP130_VPE31_0	64	0	rw	
GIC SIL MAP133 VPE31.0 64 0 rw GIC SIL MAP134 VPE31.0 64 0 rw GIC SIL MAP134 VPE31.0 64 0 rw GIC SIL MAP136 VPE31.0 64 0 rw GIC SIL MAP138 VPE31.0 64 0 rw GIC SIL MAP140 VPE31.0 64 0 rw GIC SIL MAP150 VPE31.0 64 0 rw GIC SIL MAP160 VPE31.0 64 0 rw GIC SIL MAP170 VPE31.0 64 0 rw		64	0	rw	
GIC SH MAP134 VPE31.0 64 0 rw GIC SH MAP135 VPE31.0 64 0 rw GIC SH MAP137 VPE31.0 64 0 rw GIC SH MAP138 VPE31.0 64 0 rw GIC SH MAP139 VPE31.0 64 0 rw GIC SH MAP139 VPE31.0 64 0 rw GIC SH MAP140 VPE31.0 64 0 rw GIC SH MAP141 VPE31.0 64 0 rw GIC SH MAP142 VPE31.0 64 0 rw GIC SH MAP145 VPE31.0 64 0 rw GIC SH MAP150 VPE31.0 64 0 rw GIC SH MAP160 VPE31.0 64 0 rw GIC SH MAP170 VPE31.0 64 0 rw GIC SH					
GIC SH MAP135 VPE31.0 64 0 rw GIC SH MAP136 VPE31.0 64 0 rw GIC SH MAP136 VPE31.0 64 0 rw GIC SH MAP136 VPE31.0 64 0 rw GIC SH MAP138 VPE31.0 64 0 rw GIC SH MAP139 VPE31.0 64 0 rw GIC SH MAP139 VPE31.0 64 0 rw GIC SH MAP140 VPE31.0 64 0 rw GIC SH MAP141 VPE31.0 64 0 rw GIC SH MAP145 VPE31.0 64 0 rw GIC SH MAP145 VPE31.0 64 0 rw GIC SH MAP145 VPE31.0 64 0 rw GIC SH MAP146 VPE31.0 64 0 rw GIC SH MAP146 VPE31.0 64 0 rw GIC SH MAP147 VPE31.0 64 0 rw GIC SH MAP148 VPE31.0 64 0 rw GIC SH MAP149 VPE31.0 64 0 rw GIC SH MAP150 VPE31.0 64 0 rw GIC SH MAP160 VPE31.0 64 0 rw GIC SH MAP170 VPE31.0 64 0 rw			_		
GIC.SH.MAP136.VPE31.0 64 0 rw GIC.SH.MAP137.VPE31.0 64 0 rw GIC.SH.MAP137.VPE31.0 64 0 rw GIC.SH.MAP137.VPE31.0 64 0 rw GIC.SH.MAP139.VPE31.0 64 0 rw GIC.SH.MAP130.VPE31.0 64 0 rw GIC.SH.MAP130.VPE31.0 64 0 rw GIC.SH.MAP140.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH			-		
GIC SH MAP136 VPE31.0 64 0 rw GIC SH MAP137 VPE31.0 64 0 rw GIC SH MAP138 VPE31.0 64 0 rw GIC SH MAP140 VPE31.0 64 0 rw GIC SH MAP140 VPE31.0 64 0 rw GIC SH MAP141 VPE31.0 64 0 rw GIC SH MAP141 VPE31.0 64 0 rw GIC SH MAP141 VPE31.0 64 0 rw GIC SH MAP142 VPE31.0 64 0 rw GIC SH MAP143 VPE31.0 64 0 rw GIC SH MAP144 VPE31.0 64 0 rw GIC SH MAP145 VPE31.0 64 0 rw GIC SH MAP146 VPE31.0 64 0 rw GIC SH MAP146 VPE31.0 64 0 rw GIC SH MAP146 VPE31.0 64 0 rw GIC SH MAP147 VPE31.0 64 0 rw GIC SH MAP149 VPE31.0 64 0 rw GIC SH MAP151 VPE31.0 64 0 rw GIC SH MAP153 VPE31.0 64 0 rw GIC SH MAP153 VPE31.0 64 0 rw GIC SH MAP150 VPE31.0 64 0 rw GIC SH MAP160 VPE31.0 64 0 rw GIC SH MAP170 VPE31.0 64 0 rw		-	-		
GIC.SH.MAP138.VPE31.0 64 0 rw GIC.SH.MAP139.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP141.VPE31.0 64 0 rw GIC.SH.MAP141.VPE31.0 64 0 rw GIC.SH.MAP142.VPE31.0 64 0 rw GIC.SH.MAP142.VPE31.0 64 0 rw GIC.SH.MAP142.VPE31.0 64 0 rw GIC.SH.MAP143.VPE31.0 64 0 rw GIC.SH.MAP143.VPE31.0 64 0 rw GIC.SH.MAP144.VPE31.0 64 0 rw GIC.SH.MAP145.VPE31.0 64 0 rw GIC.SH.MAP147.VPE31.0 64 0 rw GIC.SH.MAP147.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP152.VPE31.0 64 0 rw GIC.SH.MAP152.VPE31.0 64 0 rw GIC.SH.MAP153.VPE31.0 64 0 rw GIC.SH.MAP154.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP156.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH		-	-		
GIC.SH.MAP139.VPE31.0					
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GIC.SH_MAP156.VPE31.0 64 0 rw GIC.SH_MAP157.VPE31.0 64 0 rw GIC.SH_MAP158.VPE31.0 64 0 rw GIC.SH_MAP159.VPE31.0 64 0 rw GIC.SH_MAP160.VPE31.0 64 0 rw GIC.SH_MAP161.VPE31.0 64 0 rw GIC.SH_MAP161.VPE31.0 64 0 rw GIC.SH_MAP163.VPE31.0 64 0 rw GIC.SH_MAP163.VPE31.0 64 0 rw GIC.SH_MAP165.VPE31.0 64 0 rw GIC.SH_MAP166.VPE31.0 64 0 rw GIC.SH_MAP166.VPE31.0 64 0 rw GIC.SH_MAP166.VPE31.0 64 0 rw GIC.SH_MAP167.VPE31.0 64 0 rw GIC.SH_MAP167.VPE31.0 64 0 rw GIC.SH_MAP167.VPE31.0 64 0 rw GIC.SH_MAP169.VPE31.0 64 0 rw GIC.SH_MAP169.VPE31.0 64 0 rw GIC.SH_MAP171.VPE31.0 64 0 rw GIC.SH_MAP171.VPE31.0 64 0 rw GIC.SH_MAP172.VPE31.0 64 0 rw GIC.SH_MAP172.VPE31.0 64 0 rw GIC.SH_MAP173.VPE31.0 64 0 rw GIC.SH_MAP173.VPE31.0 64 0 rw GIC.SH_MAP173.VPE31.0 64 0 rw GIC.SH_MAP174.VPE31.0 64 0 rw GIC.SH_MAP175.VPE31.0 64 0 rw GIC.SH_MAP175.VPE31.0 64 0 rw GIC.SH_MAP177.VPE31.0 64 0 rw GIC.SH_MAP178.VPE31.0 64 0 rw GIC.SH_MAP179.VPE31.0 64 0 rw	GIC_SH_MAP154_VPE31_0	64	0	rw	
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GIC.SH.MAP158.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP166.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP169.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP171.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw GIC.SH.MAP174.VPE31.0 64 0 rw GIC.SH.MAP174.VPE31.0 64 0 rw GIC.SH.MAP175.VPE31.0 64 0 rw GIC.SH.MAP175.VPE31.0 64 0 rw GIC.SH.MAP177.VPE31.0 64 0 rw GIC.SH.MAP178.VPE31.0 64 0 rw GIC.SH.MAP179.VPE31.0 64 0 rw	GIC_SH_MAP156_VPE31_0	64	0	rw	
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GIC_SH_MAP171_VPE31_0 64 0 rw GIC_SH_MAP172_VPE31_0 64 0 rw GIC_SH_MAP173_VPE31_0 64 0 rw GIC_SH_MAP174_VPE31_0 64 0 rw GIC_SH_MAP175_VPE31_0 64 0 rw GIC_SH_MAP176_VPE31_0 64 0 rw GIC_SH_MAP177_VPE31_0 64 0 rw GIC_SH_MAP177_VPE31_0 64 0 rw GIC_SH_MAP177_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw			-		
GIC_SH_MAP172_VPE31_0 64 0 rw GIC_SH_MAP173_VPE31_0 64 0 rw GIC_SH_MAP174_VPE31_0 64 0 rw GIC_SH_MAP175_VPE31_0 64 0 rw GIC_SH_MAP176_VPE31_0 64 0 rw GIC_SH_MAP177_VPE31_0 64 0 rw GIC_SH_MAP177_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw			-		
GIC_SH_MAP173_VPE31_0 64 0 rw GIC_SH_MAP174_VPE31_0 64 0 rw GIC_SH_MAP175_VPE31_0 64 0 rw GIC_SH_MAP176_VPE31_0 64 0 rw GIC_SH_MAP177_VPE31_0 64 0 rw GIC_SH_MAP177_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw					
GIC_SH_MAP174_VPE31_0 64 0 rw GIC_SH_MAP175_VPE31_0 64 0 rw GIC_SH_MAP176_VPE31_0 64 0 rw GIC_SH_MAP177_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw		-			
GIC_SH_MAP175_VPE31_0 64 0 rw GIC_SH_MAP176_VPE31_0 64 0 rw GIC_SH_MAP177_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP180_VPE31_0 64 0 rw					
GIC_SH_MAP176_VPE31_0 64 0 rw GIC_SH_MAP177_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP180_VPE31_0 64 0 rw			-		
GIC_SH_MAP177_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP180_VPE31_0 64 0 rw		-	-		
GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP180_VPE31_0 64 0 rw			-		
GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP180_VPE31_0 64 0 rw			-		
GIC_SH_MAP180_VPE31_0 64 0 rw				rw	
				rw	
GIC_SH_MAP181_VPE31_0				rw	
	GIC_SH_MAP181_VPE31_0	64	0	rw	

GIC_SH_MAP182_VPE31_0	64	0	rw	
GIC_SH_MAP183_VPE31_0	64	0	rw	
GIC_SH_MAP184_VPE31_0	64	0	rw	
GIC_SH_MAP185_VPE31_0	64	0	rw	
GIC_SH_MAP186_VPE31_0	64	0	rw	
GIC_SH_MAP187_VPE31_0	64	0	rw	
GIC_SH_MAP188_VPE31_0	64	0	rw	
GIC_SH_MAP189_VPE31_0	64	0	rw	
GIC_SH_MAP190_VPE31_0	64	0	rw	
GIC_SH_MAP191_VPE31_0	64	0	rw	
GIC_SH_MAP192_VPE31_0	64	0	rw	
GIC_SH_MAP193_VPE31_0	64	0	rw	
GIC_SH_MAP194_VPE31_0	64	0	rw	
GIC_SH_MAP195_VPE31_0	64	0	rw	
GIC_SH_MAP196_VPE31_0	64	0	rw	
GIC_SH_MAP197_VPE31_0	64	0	rw	
GIC_SH_MAP198_VPE31_0	64	0	rw	
GIC_SH_MAP199_VPE31_0	64	0		
GIC_SH_MAP200_VPE31_0	64	0	rw	
GIC_SH_MAP200_VPE31_0	64	0	rw	
GIC SH MAP202 VPE31 0	64	0	rw	
GIC_SH_MAP203_VPE31_0		_	rw	
	64	0	rw	
GIC_SH_MAP204_VPE31_0	64	0	rw	
GIC_SH_MAP205_VPE31_0	64	0	rw	
GIC_SH_MAP206_VPE31_0	64	0	rw	
GIC_SH_MAP207_VPE31_0	64	0	rw	
GIC_SH_MAP208_VPE31_0	64	0	rw	
GIC_SH_MAP209_VPE31_0	64	0	rw	
GIC_SH_MAP210_VPE31_0	64	0	rw	
GIC_SH_MAP211_VPE31_0	64	0	rw	
GIC_SH_MAP212_VPE31_0	64	0	rw	
GIC_SH_MAP213_VPE31_0	64	0	rw	
GIC_SH_MAP214_VPE31_0	64	0	rw	
GIC_SH_MAP215_VPE31_0	64	0	rw	
GIC_SH_MAP216_VPE31_0	64	0	rw	
GIC_SH_MAP217_VPE31_0	64	0	rw	
GIC_SH_MAP218_VPE31_0	64	0	rw	
GIC_SH_MAP219_VPE31_0	64	0	rw	
GIC_SH_MAP220_VPE31_0	64	0	rw	
GIC_SH_MAP221_VPE31_0	64	0	rw	
GIC_SH_MAP222_VPE31_0	64	0	rw	
GIC_SH_MAP223_VPE31_0	64	0	rw	
GIC_SH_MAP224_VPE31_0	64	0	rw	
GIC_SH_MAP225_VPE31_0	64	0	rw	
GIC_SH_MAP226_VPE31_0	64	0	rw	
GIC_SH_MAP227_VPE31_0	64	0	rw	
GIC_SH_MAP228_VPE31_0	64	0	rw	
GIC_SH_MAP229_VPE31_0	64	0	rw	
GIC_SH_MAP230_VPE31_0	64	0	rw	
GIC_SH_MAP231_VPE31_0	64	0	rw	
GIC_SH_MAP232_VPE31_0	64	0	rw	
GIC_SH_MAP233_VPE31_0	64	0	rw	
GIC_SH_MAP234_VPE31_0	64	0	rw	
GIC_SH_MAP235_VPE31_0	64	0	rw	
GIC_SH_MAP236_VPE31_0	64	0	rw	
GIC_SH_MAP237_VPE31_0	64	0	rw	
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		T		
GIC_SH_MAP238_VPE31_0	64	0	rw	
GIC_SH_MAP239_VPE31_0	64	0	rw	
GIC_SH_MAP240_VPE31_0	64	0	rw	
GIC_SH_MAP241_VPE31_0	64	0	rw	
GIC_SH_MAP242_VPE31_0	64	0	rw	
GIC_SH_MAP243_VPE31_0	64	0	rw	
GIC_SH_MAP244_VPE31_0	64	0	rw	
GIC_SH_MAP245_VPE31_0	64	0	rw	
GIC_SH_MAP246_VPE31_0	64	0	rw	
GIC_SH_MAP247_VPE31_0	64	0	rw	
GIC_SH_MAP248_VPE31_0	64	0	rw	
GIC_SH_MAP249_VPE31_0	64	0	rw	
GIC_SH_MAP250_VPE31_0	64	0	rw	
GIC_SH_MAP251_VPE31_0	64	0	rw	
GIC_SH_MAP252_VPE31_0	64	0		
GIC_SH_MAP253_VPE31_0	64	0	rw	
	-	_	rw	
GIC_SH_MAP254_VPE31_0	64	0	rw	
GIC_SH_MAP255_VPE31_0	64	0	rw	
GIC_SH_EJTAG_BRK	64	0	rw	
GIC_SH_TEAMID_LO	64	0	rw	
GIC_SH_TEAMID_HI	64	0	rw	
GIC_SH_TEAMID_EXT	64	0	rw	
GIC_SH_DBG_CONFIG	64	70	rw	
GIC_SH_DINT_PART	64	0	rw	
GIC_SH_DEBUGM_STATUS	64	0	r-	
GIC_VPE_CTL	64	0	rw	
GIC_VPE_PEND	64	0	r-	
GIC_VPE_MASK	64	7f	r-	
GIC_VPE_RMASK	64	0	-w	
GIC_VPE_SMASK	64	0	-w	
GIC_VPE_WD_MAP	64	40000000	rw	
GIC_VPE_COMPARE_MAP	64	80000000	rw	
GIC_VPE_TIMER_MAP	64	80000005	rw	
GIC_VPE_FDC_MAP	64	80000005	rw	
GIC_VPE_PERFCTR_MAP	64	80000005	rw	
GIC_VPE_SWInt0_MAP	64	80000000		
GIC_VPE_SWInt1_MAP	64	8000000	rw	
GIC_VPE_SWINTI_MAP GIC_VPE_OTHER_ADDRESS	64	0	rw	
GIC_VPE_OTHER_ADDRESS GIC_VPE_IDENT	_	-	rw	
	64	0	r-	
GIC_VPE_WD_CONFIG	64	0	rw	
GIC_VPE_WD_COUNT	64	0	r-	
GIC_VPE_WD_INITIAL	64	0	rw	
GIC_VPE_Compare	64	mann mann	rw	
GIC_VPE_EICSS00	64	0	rw	
GIC_VPE_EICSS01	64	0	rw	
GIC_VPE_EICSS02	64	0	rw	
GIC_VPE_EICSS03	64	0	rw	
GIC_VPE_EICSS04	64	0	rw	
GIC_VPE_EICSS05	64	0	rw	
GIC_VPE_EICSS06	64	0	rw	
GIC_VPE_EICSS07	64	0	rw	
GIC_VPE_EICSS08	64	0	rw	
GIC_VPE_EICSS09	64	0	rw	
GIC-VPE-EICSS10	64	0	rw	
GIC-VPE-EICSS11	64	0	rw	
GIC_VPE_EICSS11	64	0	rw	
				1

GIC_VPE_EICSS13	64	0	rw	
GIC_VPE_EICSS14	64	0	rw	
GIC_VPE_EICSS15	64	0	rw	
GIC_VPE_EICSS16	64	0	rw	
GIC_VPE_EICSS17	64	0	rw	
GIC_VPE_EICSS18	64	0	rw	
GIC_VPE_EICSS19	64	0	rw	
GIC_VPE_EICSS20	64	0	rw	
GIC_VPE_EICSS21	64	0	rw	
GIC_VPE_EICSS22	64	0	rw	
GIC_VPE_EICSS23	64	0	rw	
GIC_VPE_EICSS24	64	0	rw	
GIC_VPE_EICSS25	64	0	rw	
GIC_VPE_EICSS26	64	0	rw	
GIC_VPE_EICSS27	64			
		0	rw	
GIC_VPE_EICSS28	64	0	rw	
GIC_VPE_EICSS29	64	0	rw	
GIC_VPE_EICSS30	64	0	rw	
GIC_VPE_EICSS31	64	0	rw	
GIC_VPE_EICSS32	64	0	rw	
GIC_VPE_EICSS33	64	0	rw	
GIC_VPE_EICSS34	64	1	rw	
GIC_VPE_EICSS35	64	0	rw	
GIC_VPE_EICSS36	64	0	rw	
GIC_VPE_EICSS37	64	0	rw	
GIC_VPE_EICSS38	64	0	rw	
GIC_VPE_EICSS39	64	0	rw	
GIC_VPE_EICSS40	64	0	rw	
GIC_VPE_EICSS41	64	0	rw	
GIC_VPE_EICSS42	64	0	rw	
GIC_VPE_EICSS43	64	0	rw	
GIC_VPE_EICSS44	64	0	rw	
GIC_VPE_EICSS45	64	0	rw	
GIC_VPE_EICSS46	64	0	rw	
GIC_VPE_EICSS47	64	0	rw	
GIC_VPE_EICSS48	64	0	rw	
GIC_VPE_EICSS49	64	0	rw	
GIC_VPE_EICSS49	64	0	rw	
GIC_VPE_EICSS50	64	0		
GIC_VFE_EICSS51	64	0	rw	
GIC_VPE_EICSS52 GIC_VPE_EICSS53	64	0	rw	
			rw	
GIC_VPE_EICSS54	64	0	rw	
GIC_VPE_EICSS55	64	0	rw	
GIC_VPE_EICSS56	64	0	rw	
GIC_VPE_EICSS57	64	0	rw	
GIC_VPE_EICSS58	64	0	rw	
GIC_VPE_EICSS59	64	0	rw	
GIC_VPE_EICSS60	64	0	rw	
GIC_VPE_EICSS61	64	0	rw	
GIC_VPE_EICSS62	64	0	rw	
GIC_VPE_EICSS63	64	0	rw	
GIC_VL_COFFSET	64	0	rw	
GIC_VL_VIRTUAL_VP_NUM	64	0	rw	
GIC_VPE_CTL	64	0	rw	
GIC_VPE_PEND	64	0	r-	
GIC_VI E_I END				1
GIC_VPE_MASK	64	7f	r-	

GIC_VPE_RMASK	64	0	-w	
GIC_VPE_SMASK	64	0	-w	
GIC_VPE_WD_MAP	64	40000000	rw	
GIC_VPE_COMPARE_MAP	64	80000000	rw	
GIC_VPE_TIMER_MAP	64	80000005	rw	
GIC_VPE_FDC_MAP	64	80000005	rw	
GIC_VPE_PERFCTR_MAP	64	80000005	rw	
GIC_VPE_SWInt0_MAP	64	80000000	rw	
GIC_VPE_SWInt1_MAP	64	80000000	rw	
GIC_VPE_OTHER_ADDRESS	64	0	rw	
GIC_VPE_IDENT	64	0	r-	
GIC_VPE_WD_CONFIG	64	0	rw	
GIC_VPE_WD_COUNT	64	0	r-	
GIC_VPE_WD_INITIAL	64	0	rw	
GIC_VPE_Compare	64	ALLER	rw	
GIC_VPE_EICSS00	64	0	rw	
GIC_VPE_EICSS01	64	0	rw	
GIC_VPE_EICSS02	64	0	rw	
GIC_VPE_EICSS03	64	0	rw	
GIC_VPE_EICSS04	64	0	rw	
GIC_VPE_EICSS05	64	0	rw	
GIC_VPE_EICSS06	64	0	rw	
GIC_VPE_EICSS07	64	0	rw	
GIC_VPE_EICSS07	64	0		
GIC_VPE_EICSS09	64	0	rw	
GIC_VPE_EICSS09	64	0	rw	
GIC_VPE_EICSS10 GIC_VPE_EICSS11	64	0	rw	
GIC_VPE_EICSS11	64	0	rw	
	_		rw	
GIC_VPE_EICSS13 GIC_VPE_EICSS14	64	0	rw	
	64	0	rw	
GIC_VPE_EICSS15	64	0	rw	
GIC_VPE_EICSS16	64	0	rw	
GIC_VPE_EICSS17	64	0	rw	
GIC_VPE_EICSS18	64	0	rw	
GIC_VPE_EICSS19	64	0	rw	
GIC_VPE_EICSS20	64	0	rw	
GIC_VPE_EICSS21	64	0	rw	
GIC_VPE_EICSS22	64	0	rw	
GIC_VPE_EICSS23	64	0	rw	
GIC_VPE_EICSS24	64	0	rw	
GIC_VPE_EICSS25	64	0	rw	
GIC_VPE_EICSS26	64	0	rw	
GIC_VPE_EICSS27	64	0	rw	
GIC_VPE_EICSS28	64	0	rw	
GIC_VPE_EICSS29	64	0	rw	
GIC_VPE_EICSS30	64	0	rw	
GIC_VPE_EICSS31	64	0	rw	
GIC_VPE_EICSS32	64	0	rw	
GIC_VPE_EICSS33	64	0	rw	
GIC_VPE_EICSS34	64	1	rw	
GIC_VPE_EICSS35	64	0	rw	
GIC_VPE_EICSS36	64	0	rw	
GIC_VPE_EICSS37	64	0	rw	
GIC_VPE_EICSS38	64	0	rw	
GIC_VPE_EICSS39	64	0	rw	
GIC_VPE_EICSS40	64	0	rw	
	l	I .		

GIC-VPE_EICSS41 64 0 rw GIC-VPE_EICSS43 64 0 rw GIC-VPE_EICSS44 64 0 rw GIC-VPE_EICSS44 64 0 rw GIC-VPE_EICSS45 64 0 rw GIC-VPE_EICSS46 64 0 rw GIC-VPE_EICSS47 64 0 rw GIC-VPE_EICSS48 64 0 rw GIC-VPE_EICSS49 64 0 rw GIC-VPE_EICSS49 64 0 rw GIC-VPE_EICSS50 64 0 rw GIC-VPE_EICSS51 64 0 rw GIC-VPE_EICSS51 64 0 rw GIC-VPE_EICSS53 64 0 rw GIC-VPE_EICSS55 64 0 rw GIC-VPE_EICSS56 64 0 rw GIC-VPE_EICSS56 64 0 rw GIC-VPE_EICSS57 64 0 rw GIC-VPE_EICSS58 64 0 rw GIC-VPE_EICSS58 64 0 rw GIC-VPE_EICSS59 64 0 rw GIC-VPE_EICSS59 64 0 rw GIC-VPE_EICSS59 64 0 rw GIC-VPE_EICSS60 64 0 rw GIC-VPE_EICSS60 64 0 rw GIC-VPE_EICSS61 64 0 rw GIC-VPE_EICSS61 64 0 rw GIC-VPE_EICSS63 64 0 rw GIC-VPL_COFFSET 64 0 rw GIC-VL_COFFSET 64 0 rw					
GIC.VPE.EICSS43 64 0 rw GIC.VPE.EICSS45 64 0 rw GIC.VPE.EICSS46 64 0 rw GIC.VPE.EICSS47 64 0 rw GIC.VPE.EICSS48 64 0 rw GIC.VPE.EICSS48 64 0 rw GIC.VPE.EICSS48 64 0 rw GIC.VPE.EICSS49 64 0 rw GIC.VPE.EICSS50 64 0 rw GIC.VPE.EICSS51 64 0 rw GIC.VPE.EICSS52 64 0 rw GIC.VPE.EICSS53 64 0 rw GIC.VPE.EICSS55 64 0 rw GIC.VPE.EICSS55 64 0 rw GIC.VPE.EICSS57 64 0 rw GIC.VPE.EICSS58 64 0 rw GIC.VPE.EICSS58 64 0 rw GIC.VPE.EICSS58 64 0 rw GIC.VPE.EICSS55 64 0 rw GIC.VPE.EICSS56 64 0 rw GIC.VPE.EICSS56 64 0 rw GIC.VPE.EICSS56 64 0 rw GIC.VPE.EICSS58 64 0 rw GIC.VPE.EICSS58 64 0 rw GIC.VPE.EICSS58 64 0 rw GIC.VPE.EICSS58 64 0 rw GIC.VPE.EICSS59 64 0 rw GIC.VPE.EICSS59 64 0 rw GIC.VPE.EICSS59 64 0 rw GIC.VPE.EICSS60 64 0 rw GIC.VPE.EICSS61 64 0 rw GIC.VPE.EICSS61 64 0 rw GIC.VPE.EICSS61 64 0 rw GIC.VPE.EICSS63 64 0 rw GIC.VL.COFFSET 64 0 rw GIC.VL.VIRTUAL.VP.NUM 64 0 rw GIC.VL.VIRTUAL.VP.NUM 64 0 rw	GIC_VPE_EICSS41	64	0	rw	
GIC_VPE_EICSS44 64 0 rw GIC_VPE_EICSS45 64 0 rw GIC_VPE_EICSS46 64 0 rw GIC_VPE_EICSS47 64 0 rw GIC_VPE_EICSS48 64 0 rw GIC_VPE_EICSS49 64 0 rw GIC_VPE_EICSS50 64 0 rw GIC_VPE_EICSS51 64 0 rw GIC_VPE_EICSS52 64 0 rw GIC_VPE_EICSS53 64 0 rw GIC_VPE_EICSS55 64 0 rw GIC_VPE_EICSS56 64 0 rw GIC_VPE_EICSS56 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS59 64 0 rw GIC_VPE_EICSS59 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VPL_VIRTUAL_VP_NUM 64 0 rw GIC_VU_VIRTUAL_VP_NUM 64 0 rw GIC_COunterLoUser 64 0 rw	GIC_VPE_EICSS42	64	0	rw	
GIC_VPE_EICSS45 64 0 rw GIC_VPE_EICSS47 64 0 rw GIC_VPE_EICSS48 64 0 rw GIC_VPE_EICSS48 64 0 rw GIC_VPE_EICSS49 64 0 rw GIC_VPE_EICSS50 64 0 rw GIC_VPE_EICSS51 64 0 rw GIC_VPE_EICSS52 64 0 rw GIC_VPE_EICSS53 64 0 rw GIC_VPE_EICSS54 64 0 rw GIC_VPE_EICSS55 64 0 rw GIC_VPE_EICSS55 64 0 rw GIC_VPE_EICSS55 64 0 rw GIC_VPE_EICSS55 64 0 rw GIC_VPE_EICSS56 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS59 64 0 rw GIC_VPE_EICSS59 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VPE_FICSS64 64 0 rw GIC_VPE_FICSS65 64 0 rw GIC_VPE_FICSS65 64 0 rw GIC_VPE_FICSS63 64 0 rw GIC_VPE_FICSS64 64 0 rw GIC_VPE_FICSS65 64 0 rw GIC_VPE_FICSS65 64 0 rw GIC_VPE_FICSS64 64 0 rw GIC_VPE_FICSS65 64 0 rw GIC_VPE_FICSS65 64 0 rw GIC_VPE_FICSS64 64 0 rw GIC_VPE_FICSS65 64 0 rw	GIC_VPE_EICSS43	64	0	rw	
GIC_VPE_EICSS46 64 0 rw GIC_VPE_EICSS48 64 0 rw GIC_VPE_EICSS49 64 0 rw GIC_VPE_EICSS50 64 0 rw GIC_VPE_EICSS51 64 0 rw GIC_VPE_EICSS52 64 0 rw GIC_VPE_EICSS53 64 0 rw GIC_VPE_EICSS53 64 0 rw GIC_VPE_EICSS54 64 0 rw GIC_VPE_EICSS55 64 0 rw GIC_VPE_EICSS56 64 0 rw GIC_VPE_EICSS56 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS59 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw	GIC_VPE_EICSS44	64	0	rw	
GIC_VPE_EICSS47 64 0 rw GIC_VPE_EICSS48 64 0 rw GIC_VPE_EICSS49 64 0 rw GIC_VPE_EICSS50 64 0 rw GIC_VPE_EICSS51 64 0 rw GIC_VPE_EICSS52 64 0 rw GIC_VPE_EICSS53 64 0 rw GIC_VPE_EICSS54 64 0 rw GIC_VPE_EICSS55 64 0 rw GIC_VPE_EICSS56 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS59 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_CounterLoUser	GIC_VPE_EICSS45	64	0	rw	
GIC_VPE_EICSS48 64 0 rw GIC_VPE_EICSS49 64 0 rw GIC_VPE_EICSS50 64 0 rw GIC_VPE_EICSS51 64 0 rw GIC_VPE_EICSS52 64 0 rw GIC_VPE_EICSS53 64 0 rw GIC_VPE_EICSS54 64 0 rw GIC_VPE_EICSS55 64 0 rw GIC_VPE_EICSS56 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS59 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_VIRTUAL_VP_NUM 64 0 rw GIC_CounterLoUser 64 0 r-	GIC_VPE_EICSS46	64	0	rw	
GIC_VPE_EICSS49 64 0 rw GIC_VPE_EICSS50 64 0 rw GIC_VPE_EICSS51 64 0 rw GIC_VPE_EICSS52 64 0 rw GIC_VPE_EICSS53 64 0 rw GIC_VPE_EICSS54 64 0 rw GIC_VPE_EICSS55 64 0 rw GIC_VPE_EICSS56 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS69 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_VIRTUAL_VP_NUM 64 0 rw GIC_CounterLoUser 64 0 r-	GIC_VPE_EICSS47	64	0	rw	
GIC.VPE.EICSS50 64 0 rw GIC.VPE.EICSS51 64 0 rw GIC.VPE.EICSS52 64 0 rw GIC.VPE.EICSS53 64 0 rw GIC.VPE.EICSS54 64 0 rw GIC.VPE.EICSS55 64 0 rw GIC.VPE.EICSS56 64 0 rw GIC.VPE.EICSS57 64 0 rw GIC.VPE.EICSS58 64 0 rw GIC.VPE.EICSS60 64 0 rw GIC.VPE.EICSS61 64 0 rw GIC.VPE.EICSS62 64 0 rw GIC.VPE.EICSS63 64 0 rw GIC.VL.COFFSET 64 0 rw GIC.VL.VIRTUAL_VP.NUM 64 0 rw GIC.CounterLoUser 64 0 r-	GIC_VPE_EICSS48	64	0	rw	
GIC_VPE_EICSS51 64 0 rw GIC_VPE_EICSS52 64 0 rw GIC_VPE_EICSS53 64 0 rw GIC_VPE_EICSS54 64 0 rw GIC_VPE_EICSS55 64 0 rw GIC_VPE_EICSS56 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_VIRTUAL_VP_NUM 64 0 rw GIC_CounterLouser 64 0 r-	GIC_VPE_EICSS49	64	0	rw	
GIC_VPE_EICSS52 64 0 rw GIC_VPE_EICSS53 64 0 rw GIC_VPE_EICSS54 64 0 rw GIC_VPE_EICSS55 64 0 rw GIC_VPE_EICSS55 64 0 rw GIC_VPE_EICSS56 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS59 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_VIRTUAL_VP_NUM 64 0 rw GIC_CounterLoUser 64 0 rw	GIC_VPE_EICSS50	64	0	rw	
GIC_VPE_EICSS53 64 0 rw GIC_VPE_EICSS54 64 0 rw GIC_VPE_EICSS55 64 0 rw GIC_VPE_EICSS56 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS59 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_COUNTERUAL_VP_NUM 64 0 rw GIC_COUNTERUAL_VP_NUM 64 0 rw	GIC_VPE_EICSS51	64	0	rw	
GIC_VPE_EICSS54 64 0 rw GIC_VPE_EICSS55 64 0 rw GIC_VPE_EICSS56 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS59 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_COTFSET 64 0 rw GIC_COUNTERUAL_VP_NUM 64 0 rw GIC_COUNTERUAL_VP_NUM 64 0 rw	GIC_VPE_EICSS52	64	0	rw	
GIC_VPE_EICSS55 64 0 rw GIC_VPE_EICSS56 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS59 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_VIRTUAL_VP_NUM 64 0 rw GIC_CounterLoUser 64 0 r-	GIC_VPE_EICSS53	64	0	rw	
GIC_VPE_EICSS56 64 0 rw GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS59 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_COUNTETUAL_VP_NUM 64 0 rw GIC_COUNTETUAL_VP_NUM 64 0 rw	GIC_VPE_EICSS54	64	0	rw	
GIC_VPE_EICSS57 64 0 rw GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS59 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_COTENTUAL_VP_NUM 64 0 rw GIC_COUNTERUAL_VP_NUM 64 0 rw	GIC_VPE_EICSS55	64	0	rw	
GIC_VPE_EICSS58 64 0 rw GIC_VPE_EICSS59 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_VIRTUAL_VP_NUM 64 0 rw GIC_CounterLoUser 64 0 r-	GIC_VPE_EICSS56	64	0	rw	
GIC_VPE_EICSS59 64 0 rw GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_VIRTUAL_VP_NUM 64 0 rw GIC_CounterLoUser 64 0 r-	GIC_VPE_EICSS57	64	0	rw	
GIC_VPE_EICSS60 64 0 rw GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_VIRTUAL_VP_NUM 64 0 rw GIC_CounterLoUser 64 0 r-	GIC_VPE_EICSS58	64	0	rw	
GIC_VPE_EICSS61 64 0 rw GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_VIRTUAL_VP_NUM 64 0 rw GIC_CounterLoUser 64 0 r-	GIC_VPE_EICSS59	64	0	rw	
GIC_VPE_EICSS62 64 0 rw GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_VIRTUAL_VP_NUM 64 0 rw GIC_CounterLoUser 64 0 r-	GIC_VPE_EICSS60	64	0	rw	
GIC_VPE_EICSS63 64 0 rw GIC_VL_COFFSET 64 0 rw GIC_VL_VIRTUAL_VP_NUM 64 0 rw GIC_CounterLoUser 64 0 r-	GIC_VPE_EICSS61	64	0	rw	
GIC_VL_COFFSET 64 0 rw GIC_VL_VIRTUAL_VP_NUM 64 0 rw GIC_CounterLoUser 64 0 r-	GIC_VPE_EICSS62	64	0	rw	
GIC_VL_VIRTUAL_VP_NUM 64 0 rw GIC_CounterLoUser 64 0 r-	GIC_VPE_EICSS63	64	0	rw	
GIC_CounterLoUser 64 0 r-		64	0	rw	
	GIC_VL_VIRTUAL_VP_NUM	64	0	rw	
	GIC_CounterLoUser	64	0	r-	
GIC_CounterHiUser 64 0 r-	GIC_CounterHiUser	64	0	r-	

Table 13.9: Registers at level 3, type:VP group:CMP_GIC

13.3.10 Integration_support

Registers at level:3, type:VP group:Integration_support

Name	Bits	Initial-Hex	RW	Description
stop	32	0	rw	write with non-zero to stop processor

Table 13.10: Registers at level 3, type:VP group:Integration_support