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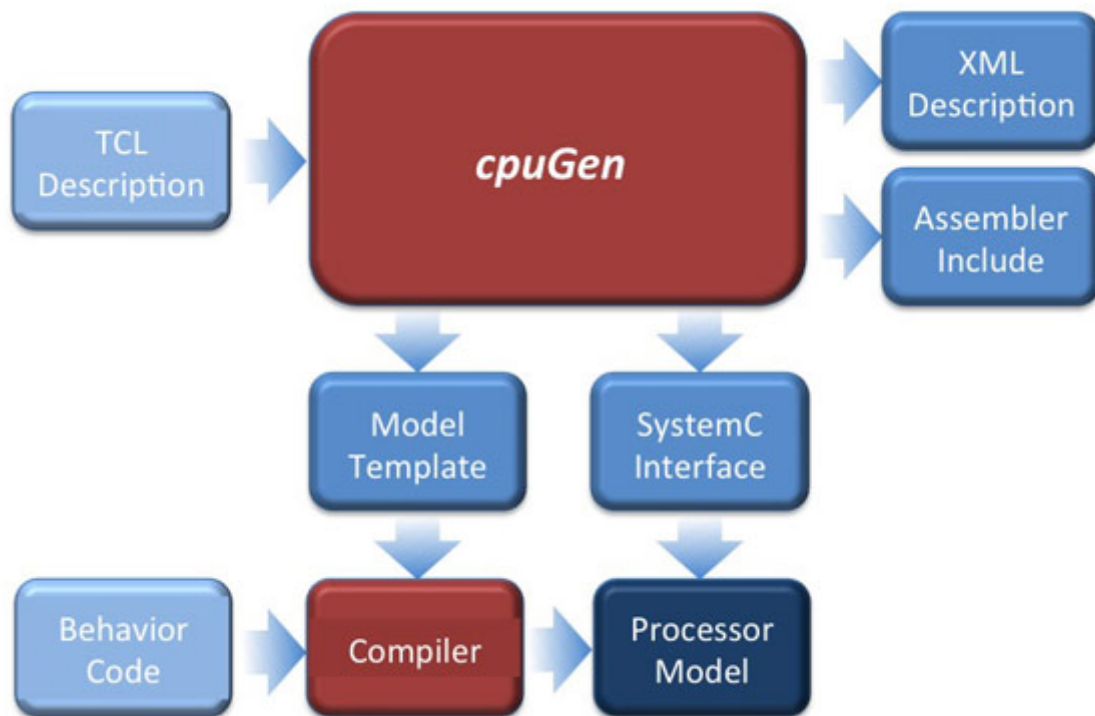
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## cpuGen - CPU Model Generation

### cpuGen™ - Processor Model Framework Generation

The Open Virtual Platform (OVP) modeling methodology may be leveraged to produce extremely high performance, instruction accurate processor models. These models can operate within OVP C, within C++ and SystemC TLM2 virtual platform formats. OVP's modeling infrastructure simplifies the model development process and, when combined with cpuGen, a processor model framework generator, reduces months long model development programs to just a few weeks or less.

The cpuGen product accelerates the creation of complete frameworks for OVP processor models, automating many of the laborious and error prone tasks associated with establishing model structures. The product takes a relatively simple TCL description of the processor characteristics and generates important model files, such as a C template for the model itself, Assembler and Dissassembler instruction components, a SystemC TLM2 interface and even an XML description of the model.



To use *cpuGen*, the model developer describes information such as the model definition, registers, instruction formats, the memory map, flags, instruction variants and other items in a TCL script. *cpuGen* uses this information to create a `model.c` file which contains the code necessary to compile the model to target the Imperas simulation technology, including register definitions, the instruction decoder, ports and other features, less the actual instruction behaviors. It also generates a SystemC TLM 2 interface that allows the SystemC simulator to call the model directly. It can provide instruction include files for an assembler and disassembler if these are not already available. It can also provide descriptions of the instructions and other processor items in the XML format.

A model initiated with *cpuGen* will be guaranteed to be well structured, saving both time up front and eliminating a source of issues later in the development.

