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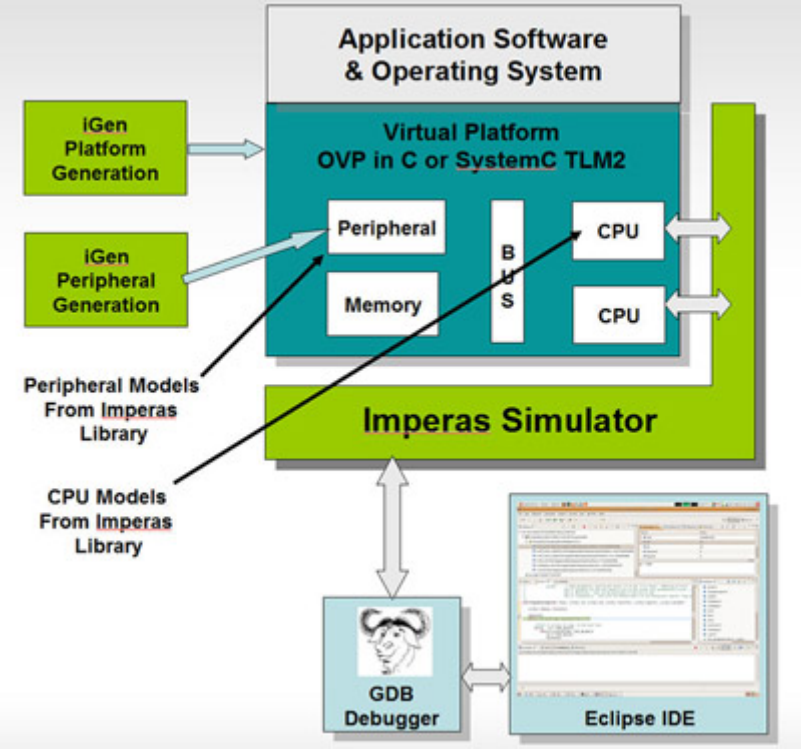
DEV - Virtual Platform Development and Simulation

C*DEV, S*DEV, M*DEV

Controller, Standard and Multicore Virtual Platform Developer Products

Overview

The Imperas Developer products consist of tools, models and infrastructure components critical for the high quality, rapid development and verification of embedded software, utilizing virtual platforms. The Developer products provide the necessary capabilities to develop platforms, including software simulation capability to execute embedded code on the platforms.



To enable the rapid creation of accurate and efficient virtual platforms, the Developer products contain:

- Imperas Model Library, a comprehensive range of processor, platform and peripheral

models
- iGen Model Generator, which automates the creation of a code framework for new models, simplifying the laborious and error prone initial phase of model generation. These models are built around the platform development infrastructure of Open Virtual (OVP), an open industry standard noted for enabling the efficient modeling of virtual platforms that leverages industry standards
- Targeted simulation solution for the execution of embedded code, dependent on the processor capability required. The simulator can operate with GDB and the Eclipse IDE, as well as the Imperas Multicore Software Design Kit.

Developer Products

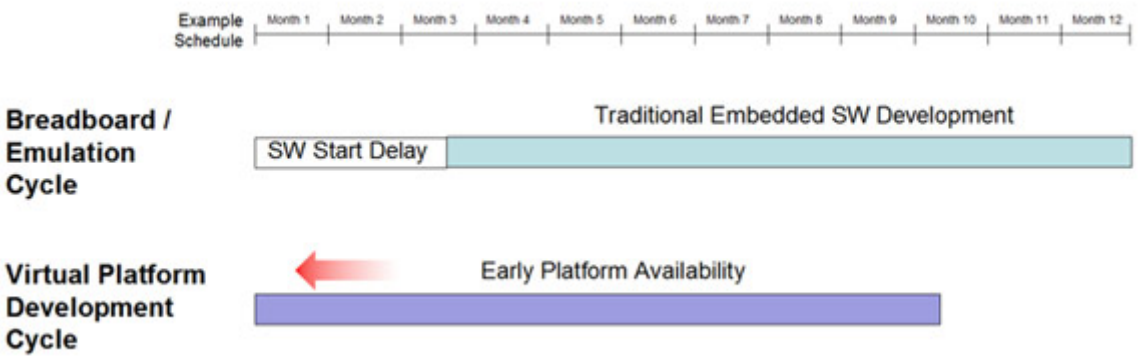
The products are divided into three product groups based on processor type and capabilities, as follows:

- The Controller Developer (C*DEV) contains capability for the development of code for single processor or single core multi-processor systems, primarily controllers.
- The Standard Developer (S*DEV) targets homogeneous systems, which may include several single or multi-processor cores of the same type.
- The Multicore Developer (M*DEV) includes a complete range of functionality for systems using single or multi-processor cores in homogeneous or heterogeneous configurations.

Technology

Imperas has pioneered three technological advancements, which revolve around the simulation engine and its interaction with models and environment components to significantly improve the user experience, as follows:

- Unique, powerful capabilities targeting improved engineering efficiency, allowing hard to identify problems to be rapidly identified and rectified.
- High software execution performance enabling the largest code base to be run far faster than previously possible in a simulation based software development environment.
- Significant ease-of-use characteristics, driving an intuitive, recognizable user interface and reducing the environment learning curve.



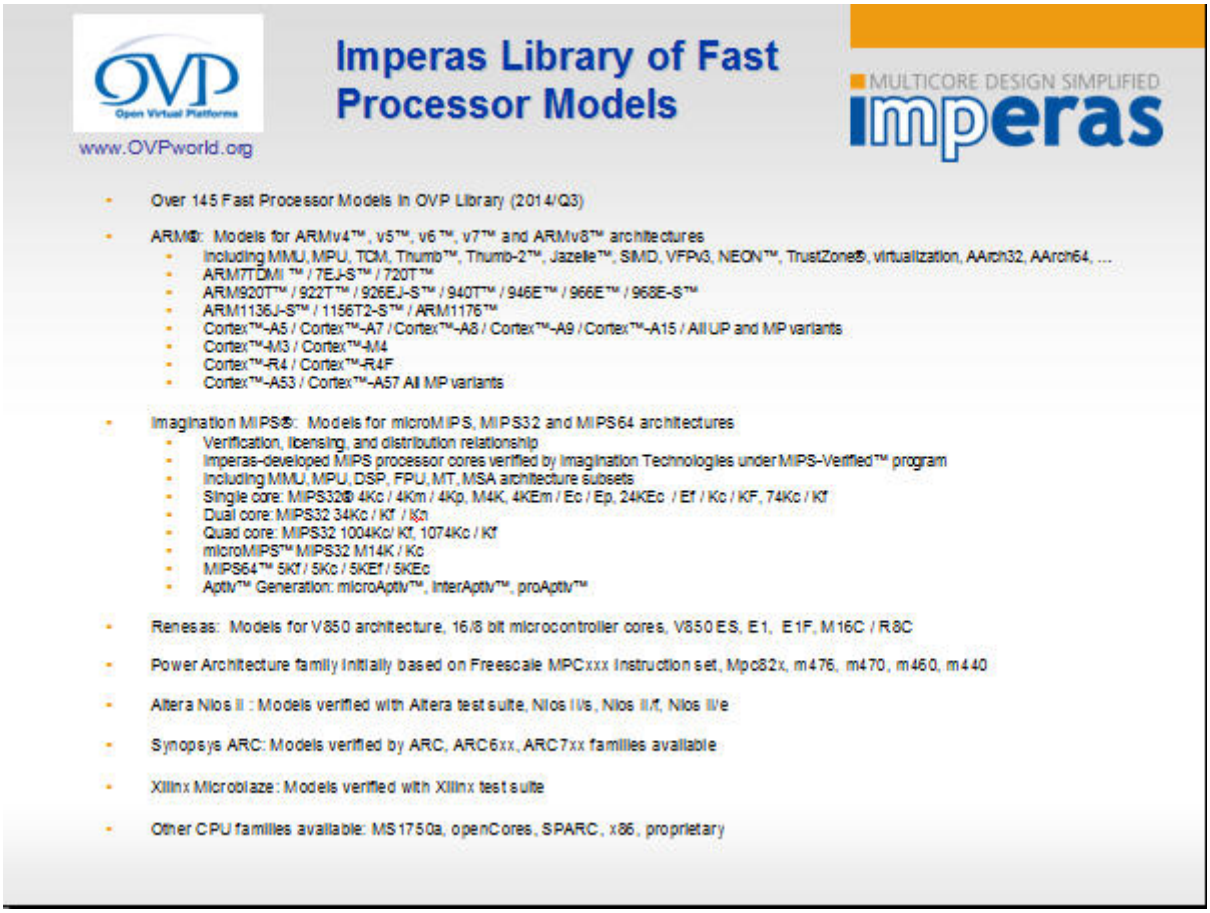
The Imperas Model Library

Imperas has developed an extensive model library of processors, peripherals and reference platforms for use in Virtual Platforms.

The model library contains more than 130 models of CPU devices from most of the major embedded processor vendors. Included in this extensive range are the complete families of the ARMv4, ARMv5, ARMv6 and ARMv7 architecture-based processors, including models of the ARM Cortex-M, Cortex-R and Cortex-A series of devices. The entire collection of the Imagination MIPS 32 and 64 bit processor models is also contained in the library. Processors such as the PowerPC, OpenCores OR1K, the Renesas v850 processor range, Altera Nios II, Xilinx Microblaze, and the Synopsys ARC range are all modeled at the Instruction Accurate (IA) level. All processor functionality is faithfully reproduced, including noted hard-to-model capabilities, such as ARM's TrustZone and virtualization features.

Almost one hundred common peripheral models may also be downloaded from the library.

In addition to the processor and peripheral models, many reference platforms are also included. These represent well-known industry examples, such as the MIPS Malta, ARM Integrator and Versatile Express, Renesas V850/PHO3, Xilinx ML505, Atmel AT91SAM7, Altera CycloneV platforms.



The models are written in C and use the OVP APIs, enabling execution on OVP compliant simulators such as the Imperas simulator. Additionally, all the models have the Imperas development environment tightly integrated within. Many of the models are available as open source and all may be downloaded directly from the OVPworld.org website.

One reason for the extensive range of processors and other models included in the library is

ease of modeling provided by the OVP APIs. APIs are available for modeling platforms, processors, behavioral models and peripherals, each optimized for the particular modeling style required. The modeling standards allow for functionality to be included quickly while maintaining model performance and ease of use, reducing a typical multi-month development project down to just a few weeks.

All models may be incorporated within a SystemC environment. The models are delivered with a bus transactional interface and this has been leveraged to provide a high speed TLM 2.0 interface layer that allows their use in a SystemC TLM 2.0 environment, enabling the fastest possible simulation performance.

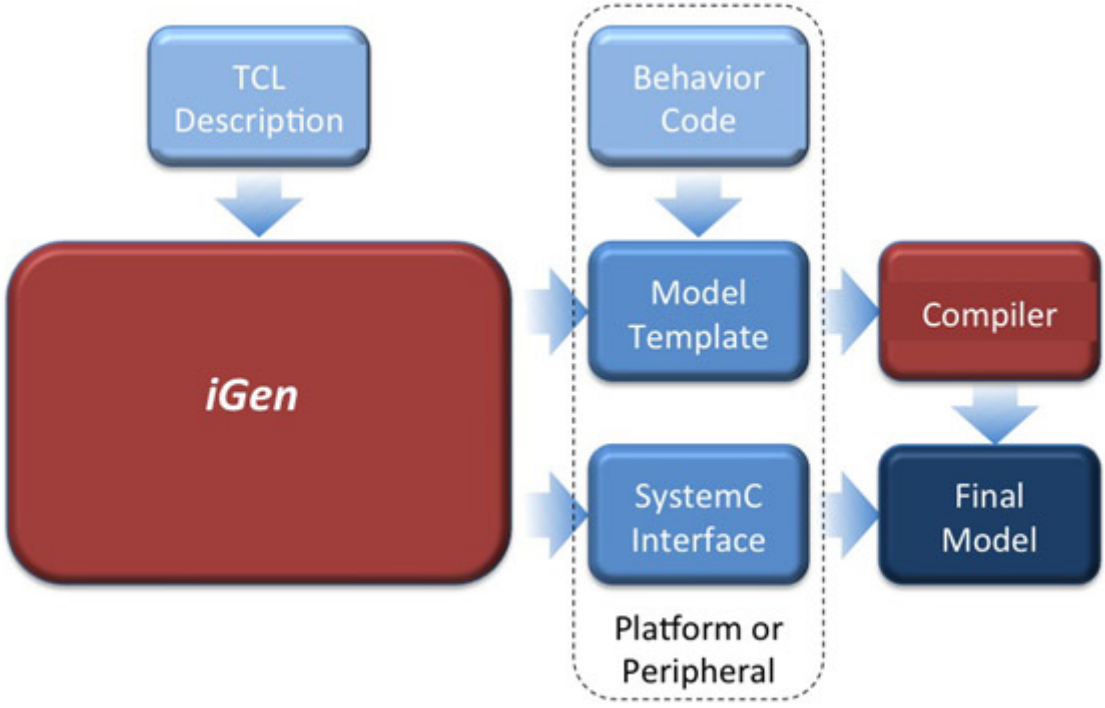
All models are available directly from the www.OVPworld.org/library link.

iGen Model Framework Generator

To aid with model creation, all the Imperas Developer products include iGen, a model framework generation system. iGen takes the laborious and error-prone task of constructing the various hardware model and software element files required for a typical model, and automates this process.

iGen takes as input a simple TCL specification that includes device internals such as registers and memories, port information, component descriptors, and other elements.

iGen builds three sets of model items, C code model files, user editable templates, and XML descriptions. These include model frameworks with registers, function calls, memory map, and other items, including matching XML information. It ensures that all component parts of the model are well-structured using best practices, and are consistent throughout the files, thus eliminating a common source of errors.



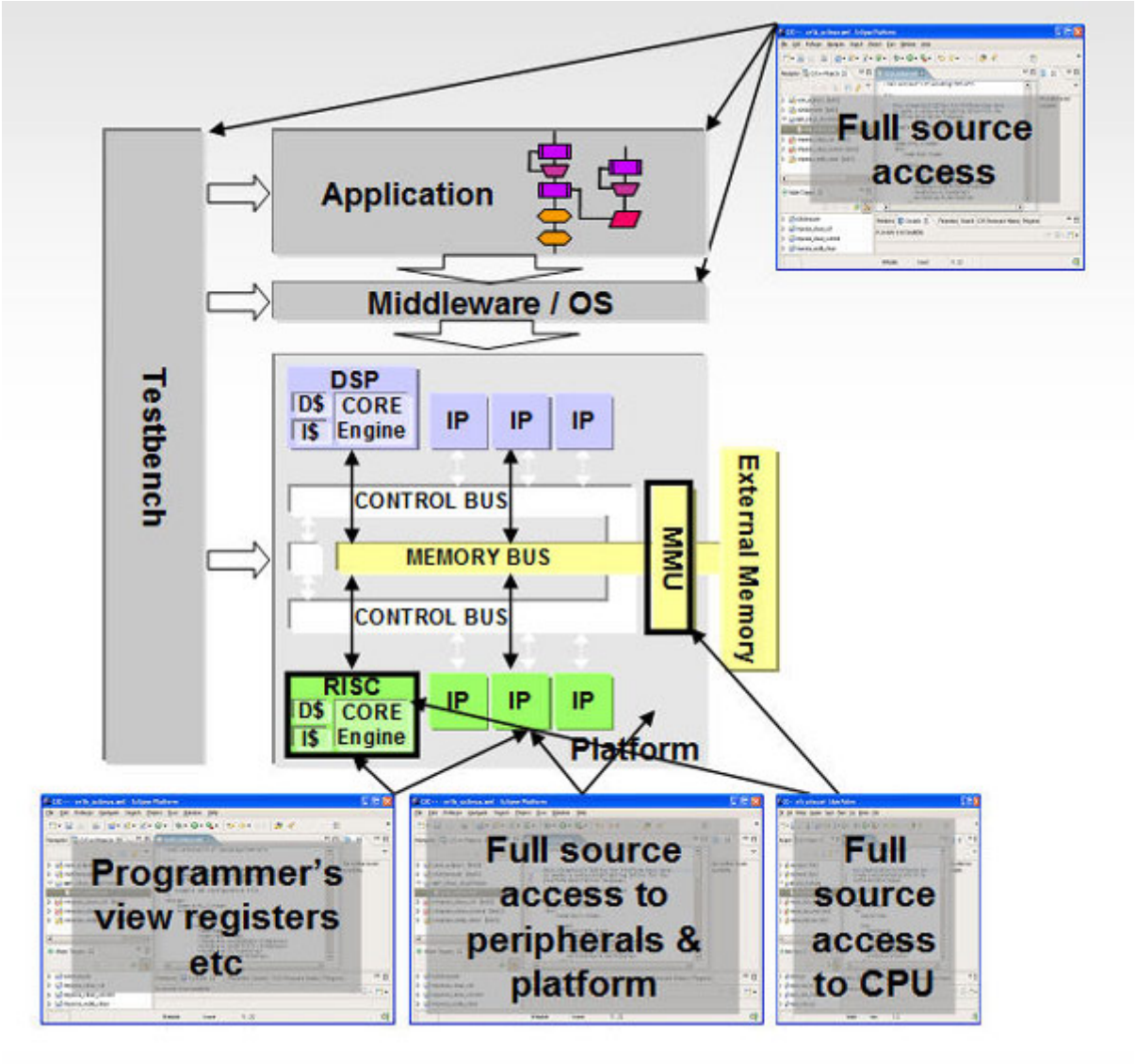
iGen presents to the developer a set of function calls and model elements that simply need to

be filled in with required behavior, thereby reducing the set up overhead of a new model significantly. iGen also creates code in the model to provide very efficient run time tracing and diagnostics.

The OVP Open Source Modeling Infrastructure

Open Virtual Platforms (OVP) is an open industry initiative designed to provide a common infrastructure, models and interfaces for the development of highly efficient virtual platforms. Imperas donated to the initiative a set of APIs, open source models, and a reference simulation engine with the intent of enabling an easily to utilize, complete solution for companies wishing to create platforms for their internal or external embedded software teams. The OVP initiative is very successful with many users of the technology from hobbyists, universities, commercial companies, and advanced research facilities.

One reason for the extensive range of processors and other models included in the Imperas library is ease of modeling provided by the OVP APIs. APIs are available for modeling platforms, processors, behavioral models / peripherals respectively, each optimized for the particular modeling style required. The modeling standards allow for functionality to be included quickly while maintaining model performance and ease of use, reducing a typical multi-month model development project down to just a few weeks.



OVP models can be used in platforms written in C or in platforms written in SystemC TLM2.0.

The processor and peripheral models are delivered with a C bus transactional interface that is used in C based OVP platforms, and this interface is used to provide a high speed TLM 2.0 interface layer that allows the model to be used in a SystemC TLM 2.0 environment with the fastest possible simulation performance.

The Imperas Simulation System

At the core of all Imperas solutions is a fully functional simulation system that operates at the highest performance of any virtual platform simulator available today. The simulator is designed to allow embedded software to be executed on a modeled (virtual) platform for the purposes of verification, analysis, debug, profiling, fault injection, and regression testing. Its purpose within the Developer products is to execute the various models, to interface the models to the appropriate selected tools, to run software on the processor models, and to enable the tasks of OS and driver bring-up, or initial embedded software development.

The Imperas models and simulator enable high performance simulation of systems running embedded software using the production un-modified binaries of the embedded software. The embedded software running cannot tell that it is not running on physical hardware but is

running on a simulated, virtual platform model, of the physical hardware.

Models of the processor and other components are created in C using the OVP APIs, as described in the OVP Infrastructure section. A full range of single, and homogeneous and heterogeneous multicore processors are supported through the simulation engine, based on the respective Developer product utilized. The simulator also supports any style of bus topology and can be used in C or C++/SystemC environments. All models in the Imperas model library can be in used in C or SystemC platforms, and the models are provided with native SystemC TLM2 interfaces.

The simulator utilizes Just-In-Time code morphing to enable particularly high-performance execution speed on standard x86 desktop computers, see the table below. By generating execution code on the fly, and combining this with other Imperas proprietary optimization schemes, the simulation performance that is achieved allows embedded code to be executed, often, faster than real time. Very large numbers of tests may be executed on embedded code within reasonable timescales, allowing product quality to be increased.

In addition, an extension of this mechanism, the Imperas ToolMorphing™ technology, allows for a highly streamlined integration of the Imperas software development kit, minimizing the traditional performance overhead and enabling tool usage without impact on software execution accuracy.

	Altera Nios II			ARM32			Imagination MIPS32		
Benchmark	Simulated Instructions	Run time	Simulated MIPS	Simulated Instructions	Run time	Simulated MIPS	Simulated Instructions	Run time	Simulated MIPS
linpack	3,075,857,171	1.8s	1718	6,105,766,856	4.32s	1413	9,814,621,392	4.83s	2032
Dhrystone	1,810,082,387	1.08s	1676	2,250,079,359	2.08s	1083	1,795,088,667	1.05s	1710
Whetstone	5,850,887,389	2.67s	2200	1,185,959,501	0.96s	1238	1,890,420,892	0.8s	2368
peakSpeed2	22,000,013,458	3s	7335	22,400,008,766	4.6s	4872	22,800,009,853	3.07s	7427
	Xilinx MicroBlaze			ARM AARCH64			Imagination MIPS64		
Benchmark	Simulated Instructions	Run time	Simulated MIPS	Simulated Instructions	Run time	Simulated MIPS	Simulated Instructions	Run time	Simulated MIPS
linpack	6,386,275,159	3.2s	2002	2,403,904,724	3.7s	650 *	1,558,856,686	0.75s	2079
Dhrystone	3,770,115,740	2.42s	1564	11,510,061,362	11.36s	1013	1,590,094,345	1.05s	1516
Whetstone	27,108,532,655	11.49s	2359	2,623,931,374	3.01s	872 *	2,133,926,552	0.88s	2453
peakSpeed2	22,000,023,433	4.38s	5034	44,800,003,885	6.7s	6687	17,100,018,075	3.26s	5249
	PowerPC			Renesas v850			Synopsys ARC		
Benchmark	Simulated Instructions	Run time	Simulated MIPS	Simulated Instructions	Run time	Simulated MIPS	Simulated Instructions	Run time	Simulated MIPS
linpack	3,163,966,113	2.24s	1419	4,991,344,159	3.66s	1368	4,184,162,664	3.15s	1328
Dhrystone	2,205,068,239	1.53s	1441	6,410,133,101	3.63s	1766	3,155,082,476	2.23s	1412
Whetstone	6,424,865,755	3.34s	1929	10,296,940,591	6.16s	1674	7,883,567,047	3.77s	2091
peakSpeed2	22,400,002,937	4.37s	5126	22,400,007,569	3.29s	6809	22,000,002,100	3.83s	5744

All measurements on 3.50GHz Intel i7-4770K, Linux FC20, OVPsim 20140731.0 * Hardware Floating Point Instructions

Embedded Software Debugging

The simulator can operate with GNU's GDB debugger, with or without the Eclipse IDE. The Imperas Multicore Software Development Kit (M*SDK) may be used which allows an extensive range of options for the verification, analysis and profiling of designs. The M*SDK also contains a powerful, three-dimensional debugger (temporal, spatial and abstract) that is CPU- and OS-aware and which adds to GDB-like functionality a series of options to target complex homogeneous/heterogeneous multicore platform debug.

C*DEV/S*DEV/M*DEV Feature Table

The three Developer packages are designed to target different processor configurations and

use models. The table below illustrates the differences:

Imperas Developer Family	Controller	Standard	Multicore
	C*DEV	S*DEV	M*DEV
Model Library	✔	✔	✔
iGen™	✔	✔	✔
Simulation			
Base capability, single core	✔	✔	✔
Standard capability, homogeneous		✔	✔
Advanced capability, heterogeneous			✔

See the model families available from OVPworld
