Imperas Peripheral Model Guide

Model Specific Information for freescale.ovpworld.org / VybridQUADSPI

Imperas Software Limited

Imperas Buildings, North Weston
Thame, Oxfordshire, OX9 2HA, U.K.
docs@imperas.com.

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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

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1.0 Model Specific Information

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers, other component parts, and configuration options and general information for peripheral modeling with Imperas OVP.

1.1 Description

Model of the QUADSPI peripheral used on the Freescale Vybrid platform

1.2 Limitations

Provides the base behaviour for the OVP Freescale Vybrid platforms

1.3 Reference

Development based on document number: VYBRIDRM Rev. 5, 07/2013

1.4 Licensing

Open Source Apache 2.0

1.5 Location

The VybridQUADSPI peripheral model is located in an Imperas/OVP installation at the VLNV: freescale.ovpworld.org / peripheral / VybridQUADSPI / 1.0.

2.0 Net Ports

This model has the following net ports:

Table 1. Net Ports

Name	Type	Must Be Connected	Description
Reset	input	F (False)	

3.0 Bus Slave Ports

This model has the following bus slave ports:

3.1 Bus Slave Port: bport1

Table 2. Bus Slave Port: bport1

Name	Size (bytes)	Must Be Connected	Description
bport1	0x1000	F (False)	

Table 3. Bus Slave Port: bport1 Registers:

Name	Offset	Width (bits)	Description	R/W	is Volatile
ab_MCR	0x0	32	Module Configuration Register, offset: 0x0		

ab_IPCR	0x8	32	IP Configuration Register, offset: 0x8		
ab_FLSHCR	0xc	32	Flash Configuration Register, offset: 0xC		
ab_BUF0CR	0x10	32	Buffer0 Configuration Register, offset: 0x10		
ab_BUF1CR	0x14	32	Buffer1 Configuration Register, offset: 0x14		
ab_BUF2CR	0x18	32	Buffer2 Configuration Register, offset: 0x18		
ab_BUF3CR	0x1c	32	Buffer3 Configuration Register, offset: 0x1C		
ab_BFGENCR	0x20	32	Buffer Generic Configuration Register, offset: 0x20		
ab_BUF0IND	0x30	32	Buffer0 Top Index Register, offset: 0x30		
ab_BUF1IND	0x34	32	Buffer1 Top Index Register, offset: 0x34		
ab_BUF2IND	0x38	32	Buffer2 Top Index Register, offset: 0x38		
ab_SFAR	0x100	32	Serial Flash Address Register, offset: 0x100		
ab_SMPR	0x108	32	Sampling Register, offset: 0x108		
ab_RBSR	0x10c	32	RX Buffer Status Register, offset: 0x10C		
ab_RBCT	0x110	32	RX Buffer Control Register, offset: 0x110		
ab_TBSR	0x150	32	TX Buffer Status Register, offset: 0x150		
ab_TBDR	0x154	32	TX Buffer Data Register, offset: 0x154		
ab_SR	0x15c	32	Status Register, offset: 0x15C		
ab_FR	0x160	32	Flag Register, offset: 0x160		
ab_RSER	0x164	32	Interrupt and DMA Request Select and Enable Register, offset: 0x164		
ab_SPNDST	0x168	32	Sequence Suspend Status Register, offset: 0x168		
ab_SPTRCLR	0x16c	32	Sequence Pointer Clear Register, offset: 0x16C		
ab_SFA1AD	0x180	32	Serial Flash A1 Top Address, offset: 0x180		
ab_SFA2AD	0x184	32	Serial Flash A2 Top Address, offset: 0x184		
ab_SFB1AD	0x188	32	Serial Flash B1Top Address, offset: 0x188		
ab_SFB2AD	0x18c	32	Serial Flash B2Top Address, offset: 0x18C		
ab_LUTKEY	0x300	32	LUT Key Register, offset: 0x300		

ab_LCKCR	0x304	32	LUT Lock Configuration Register, offset: 0x304		
ab_RBDR0	0x200	32	RX Buffer DataRegister 0 offset base 0x200: array step: 0x4		
ab_RBDR1	0x204	32	RX Buffer DataRegister 1 offset base 0x200: array step: 0x4		
ab_RBDR2	0x208	32	RX Buffer DataRegister 2 offset base 0x200: array step: 0x4		
ab_RBDR3	0x20c	32	RX Buffer DataRegister 3 offset base 0x200: array step: 0x4		
ab_RBDR4	0x210	32	RX Buffer DataRegister 4 offset base 0x200: array step: 0x4		
ab_RBDR5	0x214	32	RX Buffer DataRegister 5 offset base 0x200: array step: 0x4		
ab_RBDR6	0x218	32	RX Buffer DataRegister 6 offset base 0x200: array step: 0x4		
ab_RBDR7	0x21c	32	RX Buffer DataRegister 7 offset base 0x200: array step: 0x4		
ab_RBDR8	0x220	32	RX Buffer DataRegister 8 offset base 0x200: array step: 0x4		
ab_RBDR9	0x224	32	RX Buffer DataRegister 9 offset base 0x200: array step: 0x4		
ab_RBDR10	0x228	32	RX Buffer DataRegister 10 offset base 0x200: array step: 0x4		
ab_RBDR11	0x22c	32	RX Buffer DataRegister 11 offset base 0x200: array step: 0x4		
ab_RBDR12	0x230	32	RX Buffer DataRegister 12 offset base 0x200: array step: 0x4		
ab_RBDR13	0x234	32	RX Buffer DataRegister 13 offset base 0x200: array step: 0x4		
ab_RBDR14	0x238	32	RX Buffer DataRegister 14 offset base 0x200: array step: 0x4		
ab_RBDR15	0x23c	32	RX Buffer DataRegister 15 offset base 0x200: array step: 0x4		
ab_RBDR16	0x240	32	RX Buffer DataRegister 16 offset base 0x200: array step: 0x4		
ab_RBDR17	0x244	32	RX Buffer DataRegister 17 offset base 0x200: array step: 0x4		
ab_RBDR18	0x248	32	RX Buffer DataRegister 18 offset base 0x200:		

			array step: 0x4		
ab_RBDR19	0x24c	32	RX Buffer DataRegister 19 offset base 0x200: array step: 0x4		
ab_RBDR20	0x250	32	RX Buffer DataRegister 20 offset base 0x200: array step: 0x4		
ab_RBDR21	0x254	32	RX Buffer DataRegister 21 offset base 0x200: array step: 0x4		
ab_RBDR22	0x258	32	RX Buffer DataRegister 22 offset base 0x200: array step: 0x4		
ab_RBDR23	0x25c	32	RX Buffer DataRegister 23 offset base 0x200: array step: 0x4		
ab_RBDR24	0x260	32	RX Buffer DataRegister 24 offset base 0x200: array step: 0x4		
ab_RBDR25	0x264	32	RX Buffer DataRegister 25 offset base 0x200: array step: 0x4		
ab_RBDR26	0x268	32	RX Buffer DataRegister 26 offset base 0x200: array step: 0x4		
ab_RBDR27	0x26c	32	RX Buffer DataRegister 27 offset base 0x200: array step: 0x4		
ab_RBDR28	0x270	32	RX Buffer DataRegister 28 offset base 0x200: array step: 0x4		
ab_RBDR29	0x274	32	RX Buffer DataRegister 29 offset base 0x200: array step: 0x4		
ab_RBDR30	0x278	32	RX Buffer DataRegister 30 offset base 0x200: array step: 0x4		
ab_RBDR31	0x27c	32	RX Buffer DataRegister 31 offset base 0x200: array step: 0x4		
ab_RBDR32	0x280	32	RX Buffer DataRegister 32 offset base 0x200: array step: 0x4		
ab_RBDR33	0x284	32	RX Buffer DataRegister 33 offset base 0x200: array step: 0x4		
ab_RBDR34	0x288	32	RX Buffer DataRegister 34 offset base 0x200: array step: 0x4		
ab_RBDR35	0x28c	32	RX Buffer DataRegister 35 offset base 0x200: array step: 0x4		
ab_RBDR36	0x290	32	RX Buffer DataRegister 36 offset base 0x200: array step: 0x4		
ab_RBDR37	0x294	32	RX Buffer DataRegister 37 offset base 0x200: array step: 0x4		

ab_RBDR38	0x298	32	RX Buffer DataRegister 38 offset base 0x200: array step: 0x4		
ab_RBDR39	0x29c	32	RX Buffer DataRegister 39 offset base 0x200: array step: 0x4		
ab_RBDR40	0x2a0	32	RX Buffer DataRegister 40 offset base 0x200: array step: 0x4		
ab_RBDR41	0x2a4	32	RX Buffer DataRegister 41 offset base 0x200: array step: 0x4		
ab_RBDR42	0x2a8	32	RX Buffer DataRegister 42 offset base 0x200: array step: 0x4		
ab_RBDR43	0x2ac	32	RX Buffer DataRegister 43 offset base 0x200: array step: 0x4		
ab_RBDR44	0x2b0	32	RX Buffer DataRegister 44 offset base 0x200: array step: 0x4		
ab_RBDR45	0x2b4	32	RX Buffer DataRegister 45 offset base 0x200: array step: 0x4		
ab_RBDR46	0x2b8	32	RX Buffer DataRegister 46 offset base 0x200: array step: 0x4		
ab_RBDR47	0x2bc	32	RX Buffer DataRegister 47 offset base 0x200: array step: 0x4		
ab_RBDR48	0x2c0	32	RX Buffer DataRegister 48 offset base 0x200: array step: 0x4		
ab_RBDR49	0x2c4	32	RX Buffer DataRegister 49 offset base 0x200: array step: 0x4		
ab_RBDR50	0x2c8	32	RX Buffer DataRegister 50 offset base 0x200: array step: 0x4		
ab_RBDR51	0x2cc	32	RX Buffer DataRegister 51 offset base 0x200: array step: 0x4		
ab_RBDR52	0x2d0	32	RX Buffer DataRegister 52 offset base 0x200: array step: 0x4		
ab_RBDR53	0x2d4	32	RX Buffer DataRegister 53 offset base 0x200: array step: 0x4		
ab_RBDR54	0x2d8	32	RX Buffer DataRegister 54 offset base 0x200: array step: 0x4		
ab_RBDR55	0x2dc	32	RX Buffer DataRegister 55 offset base 0x200: array step: 0x4		
ab_RBDR56	0x2e0	32	RX Buffer DataRegister 56 offset base 0x200: array step: 0x4		

ab_RBDR57	0x2e4	32	RX Buffer DataRegister 57 offset base 0x200: array step: 0x4		
ab_RBDR58	0x2e8	32	RX Buffer DataRegister 58 offset base 0x200: array step: 0x4		
ab_RBDR59	0x2ec	32	RX Buffer DataRegister 59 offset base 0x200: array step: 0x4		
ab_RBDR60	0x2f0	32	RX Buffer DataRegister 60 offset base 0x200: array step: 0x4		
ab_RBDR61	0x2f4	32	RX Buffer DataRegister 61 offset base 0x200: array step: 0x4		
ab_RBDR62	0x2f8	32	RX Buffer DataRegister 62 offset base 0x200: array step: 0x4		
ab_RBDR63	0x2fc	32	RX Buffer DataRegister 63 offset base 0x200: array step: 0x4		
ab_LUT0	0x310	32	Look-up Table register 0, array offset base 0x310: , array step: 0x4		
ab_LUT1	0x314	32	Look-up Table register 1, array offset base 0x310: , array step: 0x4		
ab_LUT2	0x318	32	Look-up Table register 2, array offset base 0x310: , array step: 0x4		
ab_LUT3	0x31c	32	Look-up Table register 3, array offset base 0x310: , array step: 0x4		
ab_LUT4	0x320	32	Look-up Table register 4, array offset base 0x310: , array step: 0x4		
ab_LUT5	0x324	32	Look-up Table register 5, array offset base 0x310: , array step: 0x4		
ab_LUT6	0x328	32	Look-up Table register 6, array offset base 0x310: , array step: 0x4		
ab_LUT7	0x32c	32	Look-up Table register 7, array offset base 0x310: , array step: 0x4		
ab_LUT8	0x330	32	Look-up Table register 8, array offset base 0x310: , array step: 0x4		
ab_LUT9	0x334	32	Look-up Table register 9, array offset base 0x310: , array step: 0x4		
ab_LUT10	0x338	32	Look-up Table register 10, array offset base 0x310: , array step: 0x4		
ab_LUT11	0x33c	32	Look-up Table register 11, array offset base 0x310: , array step: 0x4		

ab_LUT12	0x340	32	Look-up Table register 12, array offset base 0x310: , array step: 0x4		
ab_LUT13	0x344	32	Look-up Table register 13, array offset base 0x310: , array step: 0x4		
ab_LUT14	0x348	32	Look-up Table register 14, array offset base 0x310: , array step: 0x4		
ab_LUT15	0x34c	32	Look-up Table register 15, array offset base 0x310: , array step: 0x4		
ab_LUT16	0x350	32	Look-up Table register 16, array offset base 0x310: , array step: 0x4		
ab_LUT17	0x354	32	Look-up Table register 17, array offset base 0x310: , array step: 0x4		
ab_LUT18	0x358	32	Look-up Table register 18, array offset base 0x310: , array step: 0x4		
ab_LUT19	0x35c	32	Look-up Table register 19, array offset base 0x310: , array step: 0x4		
ab_LUT20	0x360	32	Look-up Table register 20, array offset base 0x310: , array step: 0x4		
ab_LUT21	0x364	32	Look-up Table register 21, array offset base 0x310: , array step: 0x4		
ab_LUT22	0x368	32	Look-up Table register 22, array offset base 0x310: , array step: 0x4		
ab_LUT23	0x36c	32	Look-up Table register 23, array offset base 0x310: , array step: 0x4		
ab_LUT24	0x370	32	Look-up Table register 24, array offset base 0x310: , array step: 0x4		
ab_LUT25	0x374	32	Look-up Table register 25, array offset base 0x310: , array step: 0x4		
ab_LUT26	0x378	32	Look-up Table register 26, array offset base 0x310: , array step: 0x4		
ab_LUT27	0x37c	32	Look-up Table register 27, array offset base 0x310: , array step: 0x4		
ab_LUT28	0x380	32	Look-up Table register 28, array offset base 0x310: , array step: 0x4		
ab_LUT29	0x384	32	Look-up Table register 29, array offset base 0x310: , array step: 0x4		
ab_LUT30	0x388	32	Look-up Table register 30, array offset base 0x310: , array step: 0x4		

ab_LUT31	0x38c	32	Look-up Table register 31, array offset base 0x310: , array step: 0x4		
ab_LUT32	0x390	32	Look-up Table register 32, array offset base 0x310: , array step: 0x4		
ab_LUT33	0x394	32	Look-up Table register 33, array offset base 0x310: , array step: 0x4		
ab_LUT34	0x398	32	Look-up Table register 34, array offset base 0x310: , array step: 0x4		
ab_LUT35	0x39c	32	Look-up Table register 35, array offset base 0x310: , array step: 0x4		
ab_LUT36	0x3a0	32	Look-up Table register 36, array offset base 0x310: , array step: 0x4		
ab_LUT37	0x3a4	32	Look-up Table register 37, array offset base 0x310: , array step: 0x4		
ab_LUT38	0x3a8	32	Look-up Table register 38, array offset base 0x310: , array step: 0x4		
ab_LUT39	0x3ac	32	Look-up Table register 39, array offset base 0x310: , array step: 0x4		
ab_LUT40	0x3b0	32	Look-up Table register 40, array offset base 0x310: , array step: 0x4		
ab_LUT41	0x3b4	32	Look-up Table register 41, array offset base 0x310: , array step: 0x4		
ab_LUT42	0x3b8	32	Look-up Table register 42, array offset base 0x310: , array step: 0x4		
ab_LUT43	0x3bc	32	Look-up Table register 43, array offset base 0x310: , array step: 0x4		
ab_LUT44	0x3c0	32	Look-up Table register 44, array offset base 0x310: , array step: 0x4		
ab_LUT45	0x3c4	32	Look-up Table register 45, array offset base 0x310: , array step: 0x4		
ab_LUT46	0x3c8	32	Look-up Table register 46, array offset base 0x310: , array step: 0x4		
ab_LUT47	0x3cc	32	Look-up Table register 47, array offset base 0x310: , array step: 0x4		
ab_LUT48	0x3d0	32	Look-up Table register 48, array offset base 0x310: , array step: 0x4		
ab_LUT49	0x3d4	32	Look-up Table register 49, array offset base 0x310: , array step: 0x4		

ab_LUT50	0x3d8	32	Look-up Table register 50, array offset base 0x310: , array step: 0x4		
ab_LUT51	0x3dc	32	Look-up Table register 51, array offset base 0x310: , array step: 0x4		
ab_LUT52	0x3e0	32	Look-up Table register 52, array offset base 0x310: , array step: 0x4		
ab_LUT53	0x3e4	32	Look-up Table register 53, array offset base 0x310: , array step: 0x4		
ab_LUT54	0x3e8	32	Look-up Table register 54, array offset base 0x310: , array step: 0x4		
ab_LUT55	0x3ec	32	Look-up Table register 55, array offset base 0x310: , array step: 0x4		
ab_LUT56	0x3f0	32	Look-up Table register 56, array offset base 0x310: , array step: 0x4		
ab_LUT57	0x3f4	32	Look-up Table register 57, array offset base 0x310: , array step: 0x4		
ab_LUT58	0x3f8	32	Look-up Table register 58, array offset base 0x310: , array step: 0x4		
ab_LUT59	0x3fc	32	Look-up Table register 59, array offset base 0x310: , array step: 0x4		
ab_LUT60	0x400	32	Look-up Table register 60, array offset base 0x310: , array step: 0x4		
ab_LUT61	0x404	32	Look-up Table register 61, array offset base 0x310: , array step: 0x4		
ab_LUT62	0x408	32	Look-up Table register 62, array offset base 0x310: , array step: 0x4		
ab_LUT63	0x40c	32	Look-up Table register 63, array offset base 0x310: , array step: 0x4		

4.0 Platforms that use this peripheral component

Peripheral components can be used in many different platforms, including those developed by Imperas or by other users of OVP. You can use this peripheral in your own platforms.

Table 4. Publicly available platforms using peripheral 'VybridQUADSPI'

Platform Name	Vendor
FreescaleVybridVFxx	freescale.ovpworld.org

5.0 Peripheral components in the library

Table 5. Publicly available Imperas/OVP peripheral models (224 models)

Peripheral	Peripheral	Peripheral
freescale.ovpworld.org/VybridSDHC	freescale.ovpworld.org/VybridSPI	freescale.ovpworld.org/VybridUART
freescale.ovpworld.org/VybridUSB	imperas.ovpworld.org/frameBuffer	imperas.ovpworld.org/uart
imperas.ovpworld.org/usecCounter	intel.ovpworld.org/82077AA	intel.ovpworld.org/82371EB
intel.ovpworld.org/8253	intel.ovpworld.org/8259A	intel.ovpworld.org/NorFlash48F4400
intel.ovpworld.org/PciIDE	intel.ovpworld.org/PciPM	intel.ovpworld.org/PciUSB
intel.ovpworld.org/Ps2Control	marvell.ovpworld.org/GT6412x	maxim.ovpworld.org/max673x
microsemi.ovpworld.org/CoreUARTapb	mips.ovpworld.org/16450C	mips.ovpworld.org/MaltaFPGA
mips.ovpworld.org/SmartLoaderLinux	motorola.ovpworld.org/MC146818	national.ovpworld.org/16450
national.ovpworld.org/16550	national.ovpworld.org/16550_4bytes	nxp.ovpworld.org/iMX6_Analog
nxp.ovpworld.org/iMX6_CCM	nxp.ovpworld.org/iMX6_GPC	nxp.ovpworld.org/iMX6_GPIO
nxp.ovpworld.org/iMX6_GPT	nxp.ovpworld.org/iMX6_MMDC	nxp.ovpworld.org/iMX6_SDHC
nxp.ovpworld.org/iMX6_SRC	nxp.ovpworld.org/iMX6_UART	nxp.ovpworld.org/iMX6_WDOG
ovpworld.org/Alpha2x16Display	ovpworld.org/DynamicBridge	ovpworld.org/FlashDevice
ovpworld.org/ledRegister	ovpworld.org/SerInt	ovpworld.org/SimpleDma
ovpworld.org/switchRegister	ovpworld.org/temperatureSensor	ovpworld.org/trap
ovpworld.org/trap4K	ovpworld.org/vEthernet_Bridge	ovpworld.org/VirtioBlkMMIO
ovpworld.org/VirtioNetMMIO	philips.ovpworld.org/ISP1761	renesas.ovpworld.org/adc
renesas.ovpworld.org/bcu	renesas.ovpworld.org/brg	renesas.ovpworld.org/can
renesas.ovpworld.org/can	renesas.ovpworld.org/clkgen	renesas.ovpworld.org/crc
renesas.ovpworld.org/csib	renesas.ovpworld.org/csie	renesas.ovpworld.org/dma
renesas.ovpworld.org/intc	renesas.ovpworld.org/memc	renesas.ovpworld.org/rng
renesas.ovpworld.org/taa	renesas.ovpworld.org/tms	renesas.ovpworld.org/tmt
renesas.ovpworld.org/uartc	renesas.ovpworld.org/UPD70F3441Logic	riscv.ovpworld.org/CLINT
riscv.ovpworld.org/PLIC	riscv.ovpworld.org/SmartLoaderRV64Linux	safepower.ovpworld.org/node
safepower.ovpworld.org/NostrumNode	safepower.ovpworld.org/ring_oscillator	safepower.ovpworld.org/TTELNode
sifive.ovpworld.org/gpio	sifive.ovpworld.org/MSEL	sifive.ovpworld.org/PRCI
sifive.ovpworld.org/pwm	sifive.ovpworld.org/spi	sifive.ovpworld.org/teststatus
sifive.ovpworld.org/UART	smsc.ovpworld.org/LAN9118	smsc.ovpworld.org/LAN91C111
ti.ovpworld.org/tca6416a	ti.ovpworld.org/UartInterface	ti.ovpworld.org/ucd9012a
ti.ovpworld.org/ucd9248	vendor.com/fifo	xilinx.ovpworld.org/axi-gpio
xilinx.ovpworld.org/axi-intc	xilinx.ovpworld.org/axi-pcie	xilinx.ovpworld.org/axi-timer
xilinx.ovpworld.org/logicore-fit	xilinx.ovpworld.org/mdm	xilinx.ovpworld.org/mpmc
xilinx.ovpworld.org/xps-gpio	xilinx.ovpworld.org/xps-iic	xilinx.ovpworld.org/xps-intc
xilinx.ovpworld.org/xps-ll-temac	xilinx.ovpworld.org/xps-mch-emc	xilinx.ovpworld.org/xps-sysace
xilinx.ovpworld.org/xps-timer	xilinx.ovpworld.org/xps-uartlite	xilinx.ovpworld.org/zynq_7000-can
xilinx.ovpworld.org/zynq_7000-ddrc	xilinx.ovpworld.org/zynq_7000-devcfg	xilinx.ovpworld.org/zynq_7000-dmac
xilinx.ovpworld.org/zynq_7000-gpio	xilinx.ovpworld.org/zynq_7000-iic	xilinx.ovpworld.org/zynq_7000-ocm
xilinx.ovpworld.org/zynq_7000-qos301	xilinx.ovpworld.org/zynq_7000-qspi	xilinx.ovpworld.org/zynq_7000-sdio
xilinx.ovpworld.org/zynq_7000-slcr	xilinx.ovpworld.org/zynq_7000-spi	xilinx.ovpworld.org/zynq_7000-swdt
xilinx.ovpworld.org/zynq_7000-ttc	xilinx.ovpworld.org/zynq_7000-tz_GPVsecurity	xilinx.ovpworld.org/zynq_7000-tz_security
xilinx.ovpworld.org/zynq_7000-usb	altera.ovpworld.org/dw-apb-timer	altera.ovpworld.org/dw-apb-uart
altera.ovpworld.org/IntervalTimer32Core	altera.ovpworld.org/IntervalTimer64Core	altera.ovpworld.org/JtagUart
altera.ovpworld.org/PerformanceCounterCore	altera.ovpworld.org/RSTMGR	altera.ovpworld.org/SystemIDCore

altera.ovpworld.org/Uart	amd.ovpworld.org/79C970	andes.ovpworld.org/ATCUART100
andes.ovpworld.org/NCEPLIC100	andes.ovpworld.org/NCEPLMT100	arm.ovpworld.org/AaciPL041
arm.ovpworld.org/CompactFlashRegs	arm.ovpworld.org/CoreModule9x6	arm.ovpworld.org/DebugLedAndDipSwitch
arm.ovpworld.org/DMemCtrlPL341	arm.ovpworld.org/IcpControl	arm.ovpworld.org/IcpCounterTimer
arm.ovpworld.org/IntICP	arm.ovpworld.org/IntICP	arm.ovpworld.org/KbPL050
arm.ovpworld.org/L2CachePL310	arm.ovpworld.org/LcdPL110	arm.ovpworld.org/MmciPL181
arm.ovpworld.org/RtcPL031	arm.ovpworld.org/SerBusDviRegs	arm.ovpworld.org/SmartLoaderArm64Linux
arm.ovpworld.org/SmartLoaderArmLinux	arm.ovpworld.org/SMemCtrlPL354	arm.ovpworld.org/SysCtrlSP810
arm.ovpworld.org/TimerSP804	arm.ovpworld.org/TzpcBP147	arm.ovpworld.org/UartPL011
arm.ovpworld.org/VexpressSysRegs	arm.ovpworld.org/WdtSP805	atmel.ovpworld.org/AdvancedInterruptController
atmel.ovpworld.org/ParallelIOController	atmel.ovpworld.org/PowerSaving	atmel.ovpworld.org/SpecialFunction
atmel.ovpworld.org/TimerCounter	atmel.ovpworld.org/UsartInterface	atmel.ovpworld.org/WatchdogTimer
cadence.ovpworld.org/gem	cadence.ovpworld.org/uart	cirrus.ovpworld.org/GD5446
freescale.ovpworld.org/KinetisADC	freescale.ovpworld.org/KinetisAIPS	freescale.ovpworld.org/KinetisAXBS
freescale.ovpworld.org/KinetisCAN	freescale.ovpworld.org/KinetisCMP	freescale.ovpworld.org/KinetisCMT
freescale.ovpworld.org/KinetisCRC	freescale.ovpworld.org/KinetisDAC	freescale.ovpworld.org/KinetisDDR
freescale.ovpworld.org/KinetisDMA	freescale.ovpworld.org/KinetisDMAC	freescale.ovpworld.org/KinetisDMAMUX
freescale.ovpworld.org/KinetisENET	freescale.ovpworld.org/KinetisEWM	freescale.ovpworld.org/KinetisFB
freescale.ovpworld.org/KinetisFMC	freescale.ovpworld.org/KinetisFTFE	freescale.ovpworld.org/KinetisFTM
freescale.ovpworld.org/KinetisGPIO	freescale.ovpworld.org/KinetisI2C	freescale.ovpworld.org/KinetisI2S
freescale.ovpworld.org/KinetisLLWU	freescale.ovpworld.org/KinetisLPTMR	freescale.ovpworld.org/KinetisMCG
freescale.ovpworld.org/KinetisMPU	freescale.ovpworld.org/KinetisNFC	freescale.ovpworld.org/KinetisOSC
freescale.ovpworld.org/KinetisPDB	freescale.ovpworld.org/KinetisPIT	freescale.ovpworld.org/KinetisPMC
freescale.ovpworld.org/KinetisPORT	freescale.ovpworld.org/KinetisRCM	freescale.ovpworld.org/KinetisRFSYS
freescale.ovpworld.org/KinetisRFVBAT	freescale.ovpworld.org/KinetisRNG	freescale.ovpworld.org/KinetisRTC
freescale.ovpworld.org/KinetisSDHC	freescale.ovpworld.org/KinetisSIM	freescale.ovpworld.org/KinetisSMC
freescale.ovpworld.org/KinetisSPI	freescale.ovpworld.org/KinetisTSI	freescale.ovpworld.org/KinetisUART
freescale.ovpworld.org/KinetisUSB	freescale.ovpworld.org/KinetisUSBDCD	freescale.ovpworld.org/KinetisUSBHS
freescale.ovpworld.org/KinetisVREF	freescale.ovpworld.org/KinetisWDOG	freescale.ovpworld.org/Uart
freescale.ovpworld.org/VybridADC	freescale.ovpworld.org/VybridANADIG	freescale.ovpworld.org/VybridCCM
freescale.ovpworld.org/VybridDMA	freescale.ovpworld.org/VybridGPIO	freescale.ovpworld.org/VybridI2C
freescale.ovpworld.org/VybridLCD	freescale.ovpworld.org/VybridQUADSPI	

6.0 General Information on Peripheral Models

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers etc. and configuration options and general information for peripheral modeling with Imperas OVP.

6.1 Background

Imperas OVP simulation technology enables very high performance simulation, debug and analysis of platforms containing multiple processors and peripheral models. The technology is designed to be extensible: you can create new models of processors, peripherals and other platform components using interfaces and libraries defined by OVP.

The peripheral models created using the OVP APIs run on the Peripheral Simulation Engine (PSE).

The model is typically written in C and compiled into an executable for the PSE processor architecture. The model is compiled for speed of execution and to protect IP. It is dynamically loaded by the simulator at run time.

7.0 Building peripherals easily with Imperas iGen

To aid with model creation, Imperas products include iGen, a model generation tool. iGen takes the laborious and error-prone task of constructing the various hardware model and software element files required for a typical model, and automates this process. iGen creates the needed C files. iGen also creates the C++ SystemC TLM2 interface files needed to run peripheral models in SystemC simulations.

iGen takes as input a simple script specification that includes device internals such as registers and memories, port information, component descriptors, and other elements. iGen then builds the C code model files and user editable templates. These include model frameworks with registers, function calls, memory map, and other items. It ensures that all component parts of the model are well-structured using best practices, and are consistent throughout the files, thus eliminating a common source of errors.

More information on iGen can be found: imperas.com/products.

8.0 Peripheral model internals

Each instance of a peripheral model runs on its own virtual machine with an address space large enough for the model. This processor (the PSE) and its memory are separate from any processors, memories and buses in the platform being simulated; they exist only to execute the code of the peripheral model.

Interception of functions defined in the peripheral model allows the use of features of the host system in the

implementation of the behavior of a peripheral. As an example, a real platform might contain a video display device. When simulating this system, it is generally more convenient not to simulate the complete video display device but to use a video package available on the host machine, such as SDL, and to use this to render to the host display. Also models of uarts, ethernet devices and USB components can make use of the host PC resources during simulation, to allow, for example, a simulation to browse the real internet, or the simulation to connect to a real USB device.

9.0 Parts of peripheral models

9.1 Configuring the Peripheral Instance with Parameters

A peripheral can include the behaviour of several configurations. These are controlled when the peripheral is instanced in the platform by setting parameters defined on the peripheral.

9.2 Net Ports

Peripherals may be connected to other peripherals or processors with signal wires (nets). These can be used to act as interrupt signals or used to control behavior between peripherals.
The wires are created in the platform as nets and this net is connected into the peripheral using a net port.

9.3 Bus master ports

A bus master port initiates (and controls the address of) a bus cycle. Bus cycles are generated by behavioral code within the peripheral model.

9.4 Bus slave ports

A peripheral can be defined as having several bus slave ports. The bus slave ports can be split into several address blocks. Each address block be either local memory or memory mapped registers. Both of these can have associated callback functions. A memory mapped register can also be defined as specific read/write access, whether it is volatile, and also whether it is associated with a reset pin and mask. A memory mapped register can also have specific bit fields defined.

9.5 Packetnets

A peripheral can be defined as being connected to packetnet ports. A packetnet is used to model packet based communication such as Ethernet, CAN bus or GSM. A packetnet is created in a platform, then connected to packetnet ports on model instances. A packetnet can have many connections, each able to send or receive packets. A packetnet is used as an efficient method of communication within OVP models.

For more information on modeling with packetnets, please see the peripheral modeling documentation: OVP_Peripheral_Modeling_Guide.pdf, OVPsim_and_CpuManager_User_Guide.pdf and the example: $IMPERAS_HOME/Examples/Models/Peripherals/packetnet.

10.0 More information (documentation) on peripheral models and modeling

More information on modeling and APIs can be found at: OVPworld.org/technology_apis.

Specifics on modeling peripherals can be found: OVP_Peripheral_Modeling_Guide.pdf.

A full list of the currently available OVP documentation is available: OVPworld.org/documentation.
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