

Source URL (retrieved on November 7, 2014 - 17:29): <http://www.imperas.com/iss-the-imperas-instruction-set-simulator>



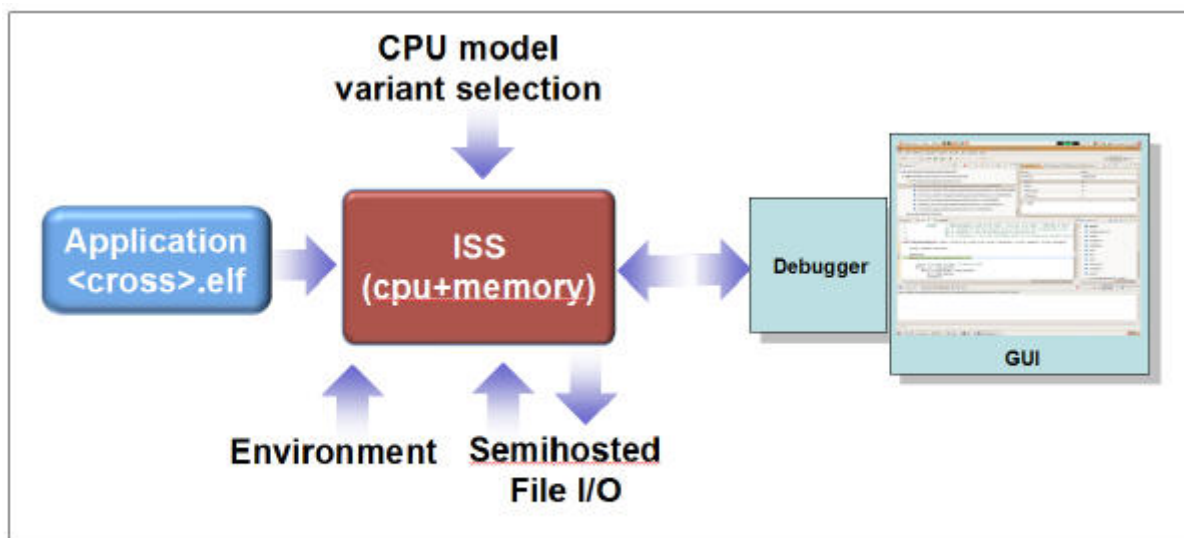
Published on Imperas (<http://www.imperas.com>)

[Home](#) > [Products](#) > ISS - The Imperas Instruction Set Simulator

ISS - The Imperas Instruction Set Simulator

Instruction Set Simulator (ISS) - fast, simple, easy to use, cross software development for embedded systems

The Imperas ISS is often the first simulation product used in an embedded software development project. The Imperas ISS allows the development and debug of code for the target architecture on an x86/x64 host PC with the minimum of setup and effort. It simply requires the cross compilation of your application and running the ISS with an argument to specify the name of the application object.



Imperas Instruction Set Simulator (ISS)

Used by application software engineers who need to create software binaries on the latest architectures but who do not need platform components - the Imperas ISS works with a standard GDB debugger and GUI which makes it very easy to get started with full source code interactive debugging.

Middleware library developers can also use the Imperas ISS when building software libraries for common functions, for example multimedia standards where they code at the assembly level and make extensive use of the processor data path - the debugger/GUI shows detailed assembly and all processor registers.

Test engineers can use the Imperas ISS in a regression test environment as it can be used in batch/scripted environments as well as being used interactively.

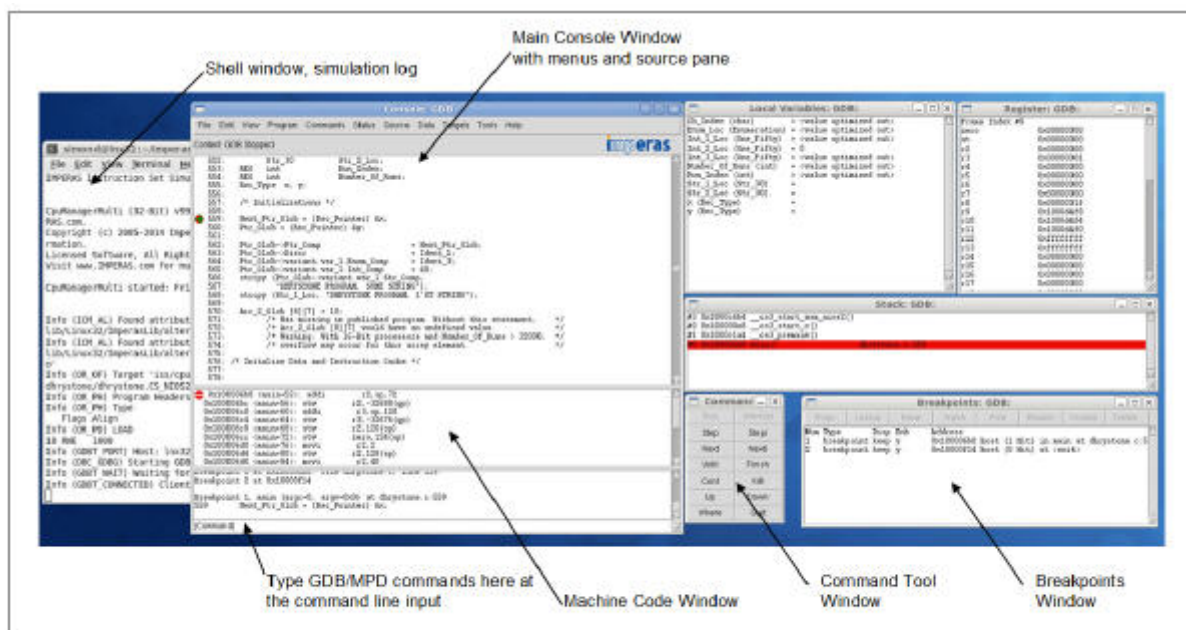
The Imperas ISS makes use of the Imperas OVP Fast Processor Model library providing access to over 130 different instruction accurate embedded CPU model variants from the Imagination/MIPS 24Kc to the ARM Cortex-A57MPx4 quad core 64 bit processor. The ISS product package comes with all these CPU models and example usage of them.

Speeds of up to 1,000 MIPS can be expected on modern desktop PCs.

Imperas ISS - detailed features

Released to run in x86 32 bit Windows/Linux and x64 64 bit Windows/Linux environments.

- includes the full library of all publicly released Imperas OVP Fast Processor Models
- includes a GDB debugger for each CPU family
- includes the Imperas Graphical User Interface (iGui) to provide full source code debug
- configurable trace subsystem to provide instruction and register tracing
- loads .elf file binaries directly
- allows one instance of a single or multi-core CPU with full memory construction
- uses built in semi-hosting to support library functions such as printf and fopen, and can access host native resources
- can be run interactively or in script/batch mode for regression testing
- includes Imperas Just-In-Time (JIT) Code Morphing high performance CPU simulator technology
- works with Eclipse/CDT GUI



Imperas Graphical User Interface (iGui)

Optional Upgrades

Imperas produces a range of products that can be layered on the ISS:

QuantumLeap MPonMP (MultiProcessor target on MultiProcessor host) acceleration software which adds to the already industry leading performance of the ISS. QuantumLeap accelerates simulation by taking advantage of the multiple x86/x64 cores on the host PC, which is especially advantageous for multi-core processors such as the ARM Cortex-

A53MPx4 or the Imagination/MIPS proAptiv. QuantumLeap simulates in parallel what other tools can only do serially and in doing so is typically 6-15x faster than other commercial simulators. Used with the ISS, QuantumLeap provides parallel simulation of the single instance of the CPU cluster.

Virtual Platform Development and Simulation solution (DEV) provides an extension to the ISS allowing the building of peripheral components and platforms to enable fast simulation of complete systems running Operating Systems (OS) and RTOS.

Multi-core Software Development Kit (M*SDK) provides the development of peripheral device models and virtual platforms using many heterogeneous or homogenous processors. M*SDK includes the Imperas Multi-Processor Debugger (MPD), and the very flexible Imperas Verification, Analysis, and Profiling (VAP) tools for embedded software development, debug and test.

Extendable Platform Kits (EPKs) are platforms built by Imperas that can be used out-of-the-box for software development. They include the CPU and main peripherals to enable full Operating Systems (OS) and RTOS to run. EPKs range from simple ones like the Atmel AT91SAM7 using an ARM7DTMI core and UART that boots ucLinux all the way to the ARMv8 Cortex-A57MPx4 Versatile Express that boots Linaro Linux. Many of the platforms include the Imperas virtualized UART, Ethernet, and USB models which not only run in simulation, but also connect to the real world allowing, for example a simulated browser to access the real internet, or the simulator to communicate with a real USB memory stick plugged into the host PC.

Evaluation

The Imperas ISS is available for free evaluation - please contact Imperas Software.

#

Source URL (retrieved on November 7, 2014 - 17:29): <http://www.imperas.com/iss-the-imperas-instruction-set-simulator>