Imperas Peripheral Model Guide

Model Specific Information for xilinx.ovpworld.org / zynq_7000-slcr

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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

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1.0 Model Specific Information

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers, other component parts, and configuration options and general information for peripheral modeling with Imperas OVP.

1.1 Description

Zynq 7000 Platform System Level Control Registers (SLCR)

1.2 Licensing

Open Source Apache 2.0

1.3 Limitations

This model implements the full set of registers. Only behavior required for processor reset control is included.

1.4 Reference

Zynq-7000 TRM
(https://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf)

1.5 Location

The zynq_7000-slcr peripheral model is located in an Imperas/OVP installation at the VLNV:
xilinx.ovpworld.org / peripheral / zynq_7000-slcr / 1.0.

2.0 Peripheral Instance Parameters

This model accepts the following parameters:

Table 1. Peripheral Parameters

Name	Type	Description
lockcode	uns32	
unlockcode	uns32	
deviceid	uns32	
devicerev	uns32	
psclock	uns32	Define the master clock (PS_CLK) frequency in MHz (default 33)
armmips	uns32	Define ARM CPU MIPS Rate in MIPS (default 500)
bootmode	uns32	Define BOOT_MODE value (default 0x04)
clockcontroldisable	bool	Disable change to ARM processor operating frequency when ARM PLL or clock control registers are modified.

3.0 Net Ports

This model has the following net ports:

Table 2. Net Ports

Name	Type	Must Be Connected	Description
A9_RST0	output	F (False)	
A9_RST1	output	F (False)	
ARM1Deration	output	F (False)	
ARM0Deration	output	F (False)	

4.0 Bus Master Ports

This model has the following bus master ports:

4.1 Bus Master Port: mpOCM

Table 3. mpOCM

Name	Address Width (bits)	Description
mpOCM	32	

4.2 Bus Master Port: mpDDR

Table 4. mpDDR

Name	Address Width (bits)	Description
mpDDR	32	

5.0 Bus Slave Ports

This model has the following bus slave ports:

5.1 Bus Slave Port: bport1

Table 5. Bus Slave Port: bport1

Name	Size (bytes)	Must Be Connected	Description
bport1	0xc00	T (True)	

Table 6. Bus Slave Port: bport1 Registers:

Name	Offset	Width (bits)	Description	R/W	is Volatile
ab_SCL	0x0	32	Secure Configuration Lock		
ab_SLCR_LOCK	0x4	32	SLCR Write Protection Lock		
ab_SLCR_UNLOCK	0x8	32	SLCR Write Protection Unlock		
ab_SLCR_LOCKSTA	0xc	32	SLCR Write Protection Status		
ab_ARM_PLL_CTRL	0x100	32	ARM PLL Control		
ab_DDR_PLL_CTRL	0x104	32	DDR PLL Control		
ab_IO_PLL_CTRL	0x108	32	IO PLL Control		
ab_PLL_STATUS	0x10c	32	PLL Status		

ab_ARM_PLL_CFG	0x110	32	ARM PLL Configuration		
ab_DDR_PLL_CFG	0x114	32	DDR PLL Configuration		
ab_IO_PLL_CFG	0x118	32	IO PLL Configuration		
ab_ARM_CLK_CTRL	0x120	32	CPU Clock Control		
ab_DDR_CLK_CTRL	0x124	32	DDR Clock Control		
ab_DCI_CLK_CTRL	0x128	32	DCI clock control		
ab_APER_CLK_CTRL	0x12c	32	AMBA Peripheral Clock Control		
ab_USB0_CLK_CTRL	0x130	32	USB 0 ULPI Clock Control		
ab_USB1_CLK_CTRL	0x134	32	USB 1 ULPI Clock Control		
ab_GEM0_RCLK_CTRL	0x138	32	GigE 0 Rx Clock and Rx Signals Select		
ab_GEM1_RCLK_CTRL	0x13c	32	GigE 1 Rx Clock and Rx Signals Select		
ab_GEM0_CLK_CTRL	0x140	32	GigE 0 Ref Clock Control		
ab_GEM1_CLK_CTRL	0x144	32	GigE 1 Ref Clock Control		
ab_SMC_CLK_CTRL	0x148	32	SMC Ref Clock Control		
ab_LQSPI_CLK_CTRL	0x14c	32	Quad SPI Ref Clock Control		
ab_SDIO_CLK_CTRL	0x150	32	SDIO Ref Clock Control		
ab_UART_CLK_CTRL	0x154	32	UART Ref Clock Control		
ab_SPI_CLK_CTRL	0x158	32	SPI Ref Clock Control		
ab_CAN_CLK_CTRL	0x15c	32	CAN Ref Clock Control		
ab_CAN_MIOCLK_CTRL	0x160	32	CAN MIO Clock Control		
ab_DBG_CLK_CTRL	0x164	32	SoC Debug Clock Control		
ab_PCAP_CLK_CTRL	0x168	32	PCAP Clock Control		
ab_TOPSW_CLK_CTRL	0x16c	32	Central Interconnect Clock Control		
ab_FPGA0_CLK_CTRL	0x170	32	PL Clock 0 Output control		
ab_FPGA0_THR_CTRL	0x174	32	PL Clock 0 Throttle control		
ab_FPGA0_THR_CNT	0x178	32	PL Clock 0 Throttle Count control		
ab_FPGA0_THR_STA	0x17c	32	PL Clock 0 Throttle Status read		
ab_FPGA1_CLK_CTRL	0x180	32	PL Clock 1 Output control		
ab_FPGA1_THR_CTRL	0x184	32	PL Clock 1 Throttle control		
ab_FPGA1_THR_CNT	0x188	32	PL Clock 1 Throttle Count		
ab_FPGA1_THR_STA	0x18c	32	PL Clock 1 Throttle Status control		
ab_FPGA2_CLK_CTRL	0x190	32	PL Clock 2 output control		
ab_FPGA2_THR_CTRL	0x194	32	PL Clock 2 Throttle Control		
ab_FPGA2_THR_CNT	0x198	32	PL Clock 2 Throttle Count		

ab_FPGA2_THR_STA	0x19c	32	PL Clock 2 Throttle Status		
ab_FPGA3_CLK_CTRL	0x1a0	32	PL Clock 3 output control		
ab_FPGA3_THR_CTRL	0x1a4	32	PL Clock 3 Throttle Control		
ab_FPGA3_THR_CNT	0x1a8	32	PL Clock 3 Throttle Count		
ab_FPGA3_THR_STA	0x1ac	32	PL Clock 3 Throttle Status		
ab_CLK_621_TRUE	0x1c4	32	CPU Clock Ratio Mode select		
ab_PSS_RST_CTRL	0x200	32	PS Software Reset Control		
ab_DDR_RST_CTRL	0x204	32	DDR Software Reset Control		
ab_TOPSW_RST_CTRL	0x208	32	Central Interconnect Reset Control		
ab_DMAC_RST_CTRL	0x20c	32	DMAC Software Reset Control		
ab_USB_RST_CTRL	0x210	32	USB Software Reset Control		
ab_GEM_RST_CTRL	0x214	32	Gigabit Ethernet SW Reset Control		
ab_SDIO_RST_CTRL	0x218	32	SDIO Software Reset Control		
ab_SPI_RST_CTRL	0x21c	32	SPI Software Reset Control		
ab_CAN_RST_CTRL	0x220	32	CAN Software Reset Control		
ab_I2C_RST_CTRL	0x224	32	I2C Software Reset Control		
ab_UART_RST_CTRL	0x228	32	UART Software Reset Control		
ab_GPIO_RST_CTRL	0x22c	32	GPIO Software Reset Control		
ab_LQSPI_RST_CTRL	0x230	32	Quad SPI Software Reset Control		
ab_SMC_RST_CTRL	0x234	32	SMC Software Reset Control		
ab_OCM_RST_CTRL	0x238	32	OCM Software Reset Control		
ab_FPGA_RST_CTRL	0x240	32	FPGA Software Reset Control		
ab_A9_CPU_RST_CTRL	0x244	32	CPU Reset and Clock control		
ab_RS_AWDT_CTRL	0x24c	32	Watchdog Timer Reset Control		
ab_REBOOT_STATUS	0x258	32	Reboot Status, persistent		
ab_BOOT_MODE	0x25c	32	Boot Mode Strapping Pins		
ab_APU_CTRL	0x300	32	APU Control		
ab_WDT_CLK_SEL	0x304	32	SWDT clock source select		
ab_TZ_OCM_RAM0	0x400	32	OCM RAM TrustZone Config 0		

ab_TZ_OCM_RAM1	0x404	32	OCM RAM TrustZone Config 1		
ab_TZ_OCM	0x408	32	OCM ROM TrustZone Config		
ab_TZ_DDR_RAM	0x430	32	DDR RAM TrustZone Config		
ab_TZ_DMA_NS	0x440	32	DMAC TrustZone Config		
ab_TZ_DMA_IRQ_NS	0x444	32	DMAC TrustZone Config for Interrupts		
ab_TZ_DMA_PERIPH_NS	0x448	32	DMAC TrustZone Config for Peripherals		
ab_TZ_GEM	0x450	32	Ethernet TrustZone Config		
ab_TZ_SDIO	0x454	32	SDIO TrustZone Config		
ab_TZ_USB	0x458	32	USB TrustZone Config		
ab_TZ_FPGA_M	0x484	32	FPGA master ports TrustZone Disable		
ab_TZ_FPGA_AFI	0x488	32	FPGA AFI AXI ports TrustZone Disable		
ab_PSS_IDCODE	0x530	32	PS IDCODE (REVISION=1 FAMILY=0x1b SUBFAMILY=0x9 DEVICE=0x11 (7z045) MANUFACTURE_ID=0x49		
ab_DDR_URGENT	0x600	32	DDR Urgent Control		
ab_DDR_CAL_START	0x60c	32	DDR Calibration Start Triggers		
ab_DDR_REF_START	0x614	32	DDR Refresh Start Triggers		
ab_DDR_CMD_STA	0x618	32	DDR Command Store Status		
ab_DDR_URGENT_SEL	0x61c	32	DDR Urgent Select		
ab_DDR_DFI_STATUS	0x620	32	DDR DFI status		
ab_MIO_PIN_00	0x700	32	MIO Pin 0 Control		
ab_MIO_PIN_01	0x704	32	MIO Pin 1 Control		
ab_MIO_PIN_02	0x708	32	MIO Pin 2 Control		
ab_MIO_PIN_03	0x70c	32	MIO Pin 3 Control		
ab_MIO_PIN_04	0x710	32	MIO Pin 4 Control		
ab_MIO_PIN_05	0x714	32	MIO Pin 5 Control		
ab_MIO_PIN_06	0x718	32	MIO Pin 6 Control		
ab_MIO_PIN_07	0x71c	32	MIO Pin 7 Control		
ab_MIO_PIN_08	0x720	32	MIO Pin 8 Control		
ab_MIO_PIN_09	0x724	32	MIO Pin 9 Control		
ab_MIO_PIN_10	0x728	32	MIO Pin 10 Control		
ab_MIO_PIN_11	0x72c	32	MIO Pin 11 Control		
ab_MIO_PIN_12	0x730	32	MIO Pin 12 Control		
ab_MIO_PIN_13	0x734	32	MIO Pin 13 Control		
ab_MIO_PIN_14	0x738	32	MIO Pin 14 Control		
ab_MIO_PIN_15	0x73c	32	MIO Pin 15 Control		
ab_MIO_PIN_16	0x740	32	MIO Pin 16 Control		

ab_MIO_PIN_17	0x744	32	MIO Pin 17 Control		
ab_MIO_PIN_18	0x748	32	MIO Pin 18 Control		
ab_MIO_PIN_19	0x74c	32	MIO Pin 19 Control		
ab_MIO_PIN_20	0x750	32	MIO Pin 20 Control		
ab_MIO_PIN_21	0x754	32	MIO Pin 21 Control		
ab_MIO_PIN_22	0x758	32	MIO Pin 22 Control		
ab_MIO_PIN_23	0x75c	32	MIO Pin 23 Control		
ab_MIO_PIN_24	0x760	32	MIO Pin 24 Control		
ab_MIO_PIN_25	0x764	32	MIO Pin 25 Control		
ab_MIO_PIN_26	0x768	32	MIO Pin 26 Control		
ab_MIO_PIN_27	0x76c	32	MIO Pin 27 Control		
ab_MIO_PIN_28	0x770	32	MIO Pin 28 Control		
ab_MIO_PIN_29	0x774	32	MIO Pin 29 Control		
ab_MIO_PIN_30	0x778	32	MIO Pin 30 Control		
ab_MIO_PIN_31	0x77c	32	MIO Pin 31 Control		
ab_MIO_PIN_32	0x780	32	MIO Pin 32 Control		
ab_MIO_PIN_33	0x784	32	MIO Pin 33 Control		
ab_MIO_PIN_34	0x788	32	MIO Pin 34 Control		
ab_MIO_PIN_35	0x78c	32	MIO Pin 35 Control		
ab_MIO_PIN_36	0x790	32	MIO Pin 36 Control		
ab_MIO_PIN_37	0x794	32	MIO Pin 37 Control		
ab_MIO_PIN_38	0x798	32	MIO Pin 38 Control		
ab_MIO_PIN_39	0x79c	32	MIO Pin 39 Control		
ab_MIO_PIN_40	0x7a0	32	MIO Pin 40 Control		
ab_MIO_PIN_41	0x7a4	32	MIO Pin 41 Control		
ab_MIO_PIN_42	0x7a8	32	MIO Pin 42 Control		
ab_MIO_PIN_43	0x7ac	32	MIO Pin 43 Control		
ab_MIO_PIN_44	0x7b0	32	MIO Pin 44 Control		
ab_MIO_PIN_45	0x7b4	32	MIO Pin 45 Control		
ab_MIO_PIN_46	0x7b8	32	MIO Pin 46 Control		
ab_MIO_PIN_47	0x7bc	32	MIO Pin 47 Control		
ab_MIO_PIN_48	0x7c0	32	MIO Pin 48 Control		
ab_MIO_PIN_49	0x7c4	32	MIO Pin 49 Control		
ab_MIO_PIN_50	0x7c8	32	MIO Pin 50 Control		
ab_MIO_PIN_51	0x7cc	32	MIO Pin 51 Control		
ab_MIO_PIN_52	0x7d0	32	MIO Pin 52 Control		
ab_MIO_PIN_53	0x7d4	32	MIO Pin 53 Control		
ab_MIO_LOOPBACK	0x804	32	Loopback function within MIO		
ab_MIO_MST_TRI0	0x80c	32	MIO pin Tri-state Enables, 31:0		
ab_MIO_MST_TRI1	0x810	32	MIO pin Tri-state Enables, 53:32		
ab_SD0_WP_CD_SEL	0x830	32	SDIO 0 WP CD select		
ab_SD1_WP_CD_SEL	0x834	32	SDIO 1 WP CD select		
ab_LVL_SHFTR_EN	0x900	32	Level Shifters Enable		
ab_OCM_CFG	0x910	32	OCM Address Mapping (user mode reset config)		
ab_Reserved	0xa1c	32	Reserved		

ab_GPIOB_CTRL	0xb00	32	PS IO Buffer Control		
ab_GPIOB_CFG_CMOS18	0xb04	32	MIO GPIOB CMOS 1.8V config		
ab_GPIOB_CFG_CMOS25	0xb08	32	MIO GPIOB CMOS 2.5V config		
ab_GPIOB_CFG_CMOS33	0xb0c	32	MIO GPIOB CMOS 3.3V config		
ab_GPIOB_CFG_HSTL	0xb14	32	MIO GPIOB HSTL config		
ab_GPIOB_DRVR_BIAS_CTRL	0xb18	32	MIO GPIOB Driver Bias Control		
ab_DDRIOB_ADDR0	0xb40	32	DDR IOB Config for A[14:0], CKE and DRST_B		
ab_DDRIOB_ADDR1	0xb44	32	DDR IOB Config for BA[2:0], ODT, CS_B, WE_B, RAS_B and CAS_B		
ab_DDRIOB_DATA0	0xb48	32	DDR IOB Config for Data 15:0		
ab_DDRIOB_DATA1	0xb4c	32	DDR IOB Config for Data 31:16		
ab_DDRIOB_DIFF0	0xb50	32	DDR IOB Config for DQS 1:0		
ab_DDRIOB_DIFF1	0xb54	32	DDR IOB Config for DQS 3:2		
ab_DDRIOB_CLOCK	0xb58	32	DDR IOB Config for Clock Output		
ab_DDRIOB_DRIVE_SLEW_ADDR	0xb5c	32	Drive and Slew controls for Address and Command pins of the DDR Interface		
ab_DDRIOB_DRIVE_SLEW_DATA	0xb60	32	Drive and Slew controls for DQ pins of the DDR Interface		
ab_DDRIOB_DRIVE_SLEW_DIFF	0xb64	32	Drive and Slew controls for DQS pins of the DDR Interface		
ab_DDRIOB_DRIVE_SLEW_CLOCK	0xb68	32	Drive and Slew controls for Clock pins of the DDR Interface		
ab_DDRIOB_DDR_CTRL	0xb6c	32	DDR IOB Buffer Control		
ab_DDRIOB_DCI_CTRL	0xb70	32	DDR IOB DCI Config		
ab_DDRIOB_DCI_STATUS	0xb74	32	DDR IO Buffer DCI Status		

5.2 Bus Slave Port: spOCMDDR

Table 7. Bus Slave Port: spOCMDDR

Name	Size (bytes)	Must Be Connected	Description
spOCMDDR	0x1	T (True)	

No address blocks have been defined for this slave port.

6.0 Platforms that use this peripheral component

Peripheral components can be used in many different platforms, including those developed by Imperas or by other users of OVP. You can use this peripheral in your own platforms.

Table 8. Publicly available platforms using peripheral 'zynq_7000-slcr'

Platform Name	Vendor
Zynq_PS	xilinx.ovpworld.org

7.0 Peripheral components in the library

Table 9. Publicly available Imperas/OVP peripheral models (224 models)

Peripheral	Peripheral	Peripheral
xilinx.ovpworld.org/zynq_7000-spi	xilinx.ovpworld.org/zynq_7000-swdt	xilinx.ovpworld.org/zynq_7000-ttc
xilinx.ovpworld.org/zynq_7000-tz_GPVsecurity	xilinx.ovpworld.org/zynq_7000-tz_security	xilinx.ovpworld.org/zynq_7000-usb
altera.ovpworld.org/dw-apb-timer	altera.ovpworld.org/dw-apb-uart	altera.ovpworld.org/IntervalTimer32Core
altera.ovpworld.org/IntervalTimer64Core	altera.ovpworld.org/JtagUart	altera.ovpworld.org/PerformanceCounterCore
altera.ovpworld.org/RSTMGR	altera.ovpworld.org/SystemIDCore	altera.ovpworld.org/Uart
amd.ovpworld.org/79C970	andes.ovpworld.org/ATCUART100	andes.ovpworld.org/NCEPLIC100
andes.ovpworld.org/NCEPLMT100	arm.ovpworld.org/AaciPL041	arm.ovpworld.org/CompactFlashRegs
arm.ovpworld.org/CoreModule9x6	arm.ovpworld.org/DebugLedAndDipSwitch	arm.ovpworld.org/DMemCtrlPL341
arm.ovpworld.org/IcpControl	arm.ovpworld.org/IcpCounterTimer	arm.ovpworld.org/IntICP
arm.ovpworld.org/IntICP	arm.ovpworld.org/KbPL050	arm.ovpworld.org/L2CachePL310
arm.ovpworld.org/LcdPL110	arm.ovpworld.org/MmciPL181	arm.ovpworld.org/RtcPL031
arm.ovpworld.org/SerBusDviRegs	arm.ovpworld.org/SmartLoaderArm64Linux	arm.ovpworld.org/SmartLoaderArmLinux
arm.ovpworld.org/SMemCtrlPL354	arm.ovpworld.org/SysCtrlSP810	arm.ovpworld.org/TimerSP804
arm.ovpworld.org/TzpcBP147	arm.ovpworld.org/UartPL011	arm.ovpworld.org/VexpressSysRegs
arm.ovpworld.org/WdtSP805	atmel.ovpworld.org/AdvancedInterruptController	atmel.ovpworld.org/ParallelIOController
atmel.ovpworld.org/PowerSaving	atmel.ovpworld.org/SpecialFunction	atmel.ovpworld.org/TimerCounter
atmel.ovpworld.org/UsartInterface	atmel.ovpworld.org/WatchdogTimer	cadence.ovpworld.org/gem
cadence.ovpworld.org/uart	cirrus.ovpworld.org/GD5446	freescale.ovpworld.org/KinetisADC
freescale.ovpworld.org/KinetisAIPS	freescale.ovpworld.org/KinetisAXBS	freescale.ovpworld.org/KinetisCAN
freescale.ovpworld.org/KinetisCMP	freescale.ovpworld.org/KinetisCMT	freescale.ovpworld.org/KinetisCRC
freescale.ovpworld.org/KinetisDAC	freescale.ovpworld.org/KinetisDDR	freescale.ovpworld.org/KinetisDMA
freescale.ovpworld.org/KinetisDMAC	freescale.ovpworld.org/KinetisDMAMUX	freescale.ovpworld.org/KinetisENET
freescale.ovpworld.org/KinetisEWM	freescale.ovpworld.org/KinetisFB	freescale.ovpworld.org/KinetisFMC
freescale.ovpworld.org/KinetisFTFE	freescale.ovpworld.org/KinetisFTM	freescale.ovpworld.org/KinetisGPIO
freescale.ovpworld.org/KinetisI2C	freescale.ovpworld.org/KinetisI2S	freescale.ovpworld.org/KinetisLLWU
freescale.ovpworld.org/KinetisLPTMR	freescale.ovpworld.org/KinetisMCG	freescale.ovpworld.org/KinetisMPU
freescale.ovpworld.org/KinetisNFC	freescale.ovpworld.org/KinetisOSC	freescale.ovpworld.org/KinetisPDB
freescale.ovpworld.org/KinetisPIT	freescale.ovpworld.org/KinetisPMC	freescale.ovpworld.org/KinetisPORT
freescale.ovpworld.org/KinetisRCM	freescale.ovpworld.org/KinetisRFSYS	freescale.ovpworld.org/KinetisRFVBAT
freescale.ovpworld.org/KinetisRNG	freescale.ovpworld.org/KinetisRTC	freescale.ovpworld.org/KinetisSDHC
freescale.ovpworld.org/KinetisSIM	freescale.ovpworld.org/KinetisSMC	freescale.ovpworld.org/KinetisSPI
freescale.ovpworld.org/KinetisTSI	freescale.ovpworld.org/KinetisUART	freescale.ovpworld.org/KinetisUSB
freescale.ovpworld.org/KinetisUSBDCD	freescale.ovpworld.org/KinetisUSBHS	freescale.ovpworld.org/KinetisVREF
freescale.ovpworld.org/KinetisWDOG	freescale.ovpworld.org/Uart	freescale.ovpworld.org/VybridADC
freescale.ovpworld.org/VybridANADIG	freescale.ovpworld.org/VybridCCM	freescale.ovpworld.org/VybridDMA
freescale.ovpworld.org/VybridGPIO	freescale.ovpworld.org/VybridI2C	freescale.ovpworld.org/VybridLCD
freescale.ovpworld.org/VybridQUADSPI	freescale.ovpworld.org/VybridSDHC	freescale.ovpworld.org/VybridSPI
freescale.ovpworld.org/VybridUART	freescale.ovpworld.org/VybridUSB	imperas.ovpworld.org/frameBuffer
imperas.ovpworld.org/uart	imperas.ovpworld.org/usecCounter	intel.ovpworld.org/82077AA
intel.ovpworld.org/82371EB	intel.ovpworld.org/8253	intel.ovpworld.org/8259A
intel.ovpworld.org/NorFlash48F4400	intel.ovpworld.org/PciIDE	intel.ovpworld.org/PciPM
intel.ovpworld.org/PciUSB	intel.ovpworld.org/Ps2Control	marvell.ovpworld.org/GT6412x
maxim.ovpworld.org/max673x	microsemi.ovpworld.org/CoreUARTapb	mips.ovpworld.org/16450C

mips.ovpworld.org/MaltaFPGA	mips.ovpworld.org/SmartLoaderLinux	motorola.ovpworld.org/MC146818
national.ovpworld.org/16450	national.ovpworld.org/16550	national.ovpworld.org/16550_4bytes
nxp.ovpworld.org/iMX6_Analog	nxp.ovpworld.org/iMX6_CCM	nxp.ovpworld.org/iMX6_GPC
nxp.ovpworld.org/iMX6_GPIO	nxp.ovpworld.org/iMX6_GPT	nxp.ovpworld.org/iMX6_MMDC
nxp.ovpworld.org/iMX6_SDHC	nxp.ovpworld.org/iMX6_SRC	nxp.ovpworld.org/iMX6_UART
nxp.ovpworld.org/iMX6_WDOG	ovpworld.org/Alpha2x16Display	ovpworld.org/DynamicBridge
ovpworld.org/FlashDevice	ovpworld.org/ledRegister	ovpworld.org/SerInt
ovpworld.org/SimpleDma	ovpworld.org/switchRegister	ovpworld.org/temperatureSensor
ovpworld.org/trap	ovpworld.org/trap4K	ovpworld.org/vEthernet_Bridge
ovpworld.org/VirtioBlkMMIO	ovpworld.org/VirtioNetMMIO	philips.ovpworld.org/ISP1761
renesas.ovpworld.org/adc	renesas.ovpworld.org/bcu	renesas.ovpworld.org/brg
renesas.ovpworld.org/can	renesas.ovpworld.org/can	renesas.ovpworld.org/clkgen
renesas.ovpworld.org/crc	renesas.ovpworld.org/csib	renesas.ovpworld.org/csie
renesas.ovpworld.org/dma	renesas.ovpworld.org/intc	renesas.ovpworld.org/memc
renesas.ovpworld.org/rng	renesas.ovpworld.org/taa	renesas.ovpworld.org/tms
renesas.ovpworld.org/tmt	renesas.ovpworld.org/uartc	renesas.ovpworld.org/UPD70F3441Logic
riscv.ovpworld.org/CLINT	riscv.ovpworld.org/PLIC	riscv.ovpworld.org/SmartLoaderRV64Linux
safepower.ovpworld.org/node	safepower.ovpworld.org/NostrumNode	safepower.ovpworld.org/ring_oscillator
safepower.ovpworld.org/TTELNode	sifive.ovpworld.org/gpio	sifive.ovpworld.org/MSEL
sifive.ovpworld.org/PRCI	sifive.ovpworld.org/pwm	sifive.ovpworld.org/spi
sifive.ovpworld.org/teststatus	sifive.ovpworld.org/UART	smsc.ovpworld.org/LAN9118
smsc.ovpworld.org/LAN91C111	ti.ovpworld.org/tca6416a	ti.ovpworld.org/UartInterface
ti.ovpworld.org/ucd9012a	ti.ovpworld.org/ucd9248	vendor.com/fifo
xilinx.ovpworld.org/axi-gpio	xilinx.ovpworld.org/axi-intc	xilinx.ovpworld.org/axi-pcie
xilinx.ovpworld.org/axi-timer	xilinx.ovpworld.org/logicore-fit	xilinx.ovpworld.org/mdm
xilinx.ovpworld.org/mpmc	xilinx.ovpworld.org/xps-gpio	xilinx.ovpworld.org/xps-iic
xilinx.ovpworld.org/xps-intc	xilinx.ovpworld.org/xps-ll-temac	xilinx.ovpworld.org/xps-mch-emc
xilinx.ovpworld.org/xps-sysace	xilinx.ovpworld.org/xps-timer	xilinx.ovpworld.org/xps-uartlite
xilinx.ovpworld.org/zynq_7000-can	xilinx.ovpworld.org/zynq_7000-ddrc	xilinx.ovpworld.org/zynq_7000-devcfg
xilinx.ovpworld.org/zynq_7000-dmac	xilinx.ovpworld.org/zynq_7000-gpio	xilinx.ovpworld.org/zynq_7000-iic
xilinx.ovpworld.org/zynq_7000-ocm	xilinx.ovpworld.org/zynq_7000-qos301	xilinx.ovpworld.org/zynq_7000-qspi
xilinx.ovpworld.org/zynq_7000-sdio	xilinx.ovpworld.org/zynq_7000-slcr	

8.0 General Information on Peripheral Models

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers etc. and configuration options and general information for peripheral modeling with Imperas OVP.

8.1 Background

Imperas OVP simulation technology enables very high performance simulation, debug and analysis of platforms containing multiple processors and peripheral models. The technology is designed to be extensible: you can create new models of processors, peripherals and other platform components using interfaces and libraries defined by OVP.

The peripheral models created using the OVP APIs run on the Peripheral Simulation Engine (PSE).

The model is typically written in C and compiled into an executable for the PSE processor architecture. The model is compiled for speed of execution and to protect IP. It is dynamically loaded by the simulator at run time.

9.0 Building peripherals easily with Imperas iGen

To aid with model creation, Imperas products include iGen, a model generation tool. iGen takes the laborious and error-prone task of constructing the various hardware model and software element files required for a typical model, and automates this process. iGen creates the needed C files. iGen also creates the C++ SystemC TLM2 interface files needed to run peripheral models in SystemC simulations.

iGen takes as input a simple script specification that includes device internals such as registers and memories, port information, component descriptors, and other elements. iGen then builds the C code model files and user editable templates. These include model frameworks with registers, function calls, memory map, and other items. It ensures that all component parts of the model are well-structured using best practices, and are consistent throughout the files, thus eliminating a common source of errors.

More information on iGen can be found: imperas.com/products.

10.0 Peripheral model internals

Each instance of a peripheral model runs on its own virtual machine with an address space large enough for the model. This processor (the PSE) and its memory are separate from any processors, memories and buses in the platform being simulated; they exist only to execute the code of the peripheral model.

Interception of functions defined in the peripheral model allows the use of features of the host system in the

implementation of the behavior of a peripheral. As an example, a real platform might contain a video display device. When simulating this system, it is generally more convenient not to simulate the complete video display device but to use a video package available on the host machine, such as SDL, and to use this to render to the host display. Also models of uarts, ethernet devices and USB components can make use of the host PC resources during simulation, to allow, for example, a simulation to browse the real internet, or the simulation to connect to a real USB device.

11.0 Parts of peripheral models

11.1 Configuring the Peripheral Instance with Parameters

A peripheral can include the behaviour of several configurations. These are controlled when the peripheral is instanced in the platform by setting parameters defined on the peripheral.

11.2 Net Ports

Peripherals may be connected to other peripherals or processors with signal wires (nets). These can be used to act as interrupt signals or used to control behavior between peripherals.
The wires are created in the platform as nets and this net is connected into the peripheral using a net port.

11.3 Bus master ports

A bus master port initiates (and controls the address of) a bus cycle. Bus cycles are generated by behavioral code within the peripheral model.

11.4 Bus slave ports

A peripheral can be defined as having several bus slave ports. The bus slave ports can be split into several address blocks. Each address block be either local memory or memory mapped registers. Both of these can have associated callback functions. A memory mapped register can also be defined as specific read/write access, whether it is volatile, and also whether it is associated with a reset pin and mask. A memory mapped register can also have specific bit fields defined.

11.5 Packetnets

A peripheral can be defined as being connected to packetnet ports. A packetnet is used to model packet based communication such as Ethernet, CAN bus or GSM. A packetnet is created in a platform, then connected to packetnet ports on model instances. A packetnet can have many connections, each able to send or receive packets. A packetnet is used as an efficient method of communication within OVP models.

For more information on modeling with packetnets, please see the peripheral modeling documentation: OVP_Peripheral_Modeling_Guide.pdf, OVPsim_and_CpuManager_User_Guide.pdf and the example: $IMPERAS_HOME/Examples/Models/Peripherals/packetnet.

12.0 More information (documentation) on peripheral models and modeling

More information on modeling and APIs can be found at: OVPworld.org/technology_apis.

Specifics on modeling peripherals can be found: OVP_Peripheral_Modeling_Guide.pdf.

A full list of the currently available OVP documentation is available: OVPworld.org/documentation.
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