Imperas Guide to using Virtual Platforms

Platform / Module Specific Information for imperas.ovpworld.org / HeteroAlteraCycloneV_HPS_CycloneIII_3c120

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MULTICORE DESIGN SIMPLIFIED
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Model Release Status

This model is released as part of standard Imperas releases and is included in Imperas packages. Please visit the Imperas User site to download.

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1.0 Platform / Module: HeteroAlteraCycloneV_HPS_CycloneIII_3c120

This document provides the details of the usage of an Imperas OVP Virtual Platform / Module. The first half of the document covers specifics of this particular component. For more information about Imperas OVP virtual platforms, how they are built and used, please see the later sections in this document.

1.1 Virtual Platform / Module Type

Hardware described using OVP can either be a platform, module, processor, or peripheral.
This is a fixed virtual platform.

1.2 Licensing

Open Source Apache 2.0

1.3 Description

This platform merges the Altera Cyclone V (ARM) and Cyclone III (Nios_II) processor systems

1.4 Limitations

Peripherals are modeled only to the extent required to boot and run Operating Systems such as Linux.

1.5 Reference

Altera Cyclone III 3c120 Reference Guide and Cyclone V Handbook Volume 3: Hard Processor System Technical Reference Manual cv_5v4 2013.12.30

1.6 Location

The HeteroAlteraCycloneV_HPS_CycloneIII_3c120 virtual platform / module is located in an Imperas/OVP installation at the VLNV: imperas.ovpworld.org / platform / HeteroAlteraCycloneV_HPS_CycloneIII_3c120 / 1.0.

1.7 Platform Simulation Attributes

Table 1. Platform Simulation Attributes

Attribute	Value	Description
stoponctrlc	stoponctrlc	Stop on control-C

2.0 Command Line Control of the Platform

2.1 Built-in Arguments

Table 2. Platform Built-in Arguments

Attribute	Value	Description
allargs	allargs	The Command line parser will accept the complete imperas argument set. Note that this option is ignored in some Imperas products

When running a platform in a Windows or Linux shell several command arguments can be specified.
Typically there is a '-help' command which lists the commands available in the platforms. For example:
myplatform.exe -help

Some command line arguments require a value to be provided. For example:
myplatform.exe -program myimagefile.elf

2.2 Platform Specific Command Line Arguments

Table 3. Platform Command Line Arguments

Name	Type	Description
ZIMAGE	stringvar	Linux zImage file to load using smartLoader
ZIMAGEADDR	uns64var	Physical address to load zImage file (default 0x04000000)
INITRD	stringvar	Linux initrd file to load using smartLoader
INITRDADDR	uns64var	Physical address to load initrd file (default 0x06000000)
LINUXSYM	stringvar	Linux ELF file with symbolic debug info (CpuManger only)
BOARDID	int32var	Value to pass to Linux as the boardid (default (0xffffffff)
LINUXMEM	uns64var	Amount of memory allocated to Linux (required in AMP mode)
LINUXCMD	stringvar	Linux command line (default: 'mem=1024M console=ttyS0', with mem value adjusted if LINUXMEM or MEMSIZE specified)
APP0	stringvar	ELF file to load on CPU0 instead of Linux (Precludes use of Linux options)
APP1	stringvar	ELF file to load on CPU1 for AMP
BOOT	stringvar	ELF file with boot code (both processors will start at its entry)
IMAGE0	stringvar	Image file to load on cpu0
IMAGE0ADDR	uns64var	load address for image on cpu0 (IMAGE0 must be specified)
IMAGE0SYM	stringvar	Elf file with symbolic debug info for image on cpu0 (IMAGE0 must be specified, CpuManger only)
IMAGE1	stringvar	Image file to load on cpu1
IMAGE1ADDR	uns64var	Load address for image on cpu1 (IMAGE1 must be specified)
IMAGE1SYM	stringvar	Elf file with symbolic debug info for image on cpu1 (IMAGE1 must be specified, CpuManger only)
UART0PORT	stringvar	Uart0 port: 'auto' for automatic console, 0 for simulator-chosen port, or number for specific port
UART1PORT	stringvar	Uart1 port: 'auto' for automatic console, 0 for simulator-chosen port, or number for specific port
NIOSBOOT	stringvar	vmlinux to load onto

3.0 Processor [arm.ovpworld.org/processor/arm/1.0] instance: cpu_A9MPx2

3.1 Processor model type: 'arm' variant 'Cortex-A9MPx2' definition

Imperas OVP processor models support multiple variants and details of the variants implemented in this model can be found in:
- the Imperas installation located at ImperasLib/source/arm.ovpworld.org/processor/arm/1.0/doc
- the OVP website: OVP_Model_Specific_Information_arm_Cortex-A9MPx2.pdf

3.1.1 Description

ARM Processor Model

3.1.2 Licensing

Usage of binary model under license governing simulator usage.
Note that for models of ARM CPUs the license includes the following terms:
Licensee is granted a non-exclusive, worldwide, non-transferable, revocable licence to:
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Source of model available under separate Imperas Software License Agreement.

3.1.3 Limitations

Instruction pipelines are not modeled in any way. All instructions are assumed to complete immediately. This means that instruction barrier instructions (e.g. ISB, CP15ISB) are treated as NOPs, with the exception of any undefined instruction behavior, which is modeled. The model does not implement speculative fetch behavior. The branch cache is not modeled.
Caches and write buffers are not modeled in any way. All loads, fetches and stores complete immediately and in order, and are fully synchronous (as if the memory was of Strongly Ordered or Device-nGnRnE type). Data barrier instructions (e.g. DSB, CP15DSB) are treated as NOPs, with the exception of any undefined instruction behavior, which is modeled. Cache manipulation instructions are implemented as NOPs, with the exception of any undefined instruction behavior, which is modeled.
Real-world timing effects are not modeled: all instructions are assumed to complete in a single cycle.

Performance Monitors are implemented as a register interface only except for the cycle counter, which is implemented assuming one instruction per cycle.
TLBs are architecturally-accurate but not device accurate. This means that all TLB maintenance and address translation operations are fully implemented but the cache is larger than in the real device.

3.1.4 Verification

Models have been extensively tested by Imperas. ARM Cortex-A models have been successfully used by customers to simulate SMP Linux, Ubuntu Desktop, VxWorks and ThreadX on Xilinx Zynq virtual platforms.

3.1.5 Core Features

Thumb-2 instructions are supported.
Trivial Jazelle extension is implemented.

3.1.6 Memory System

Security extensions are implemented (also known as TrustZone). Non-secure accesses can be made visible externally by connecting the processor to a 41-bit physical bus, in which case bits 39..0 give the true physical address and bit 40 is the NS bit.
VMSA secure and non-secure address translation is implemented.
TLB behavior is controlled by parameter ASIDCacheSize. If this parameter is 0, then an unlimited number of TLB entries will be maintained concurrently. If this parameter is non-zero, then only TLB entries for up to ASIDCacheSize different ASIDs will be maintained concurrently initially; as new ASIDs are used, TLB entries for less-recently used ASIDs are deleted, which improves model performance in some cases (especially when 16-bit ASIDs are in use). If the model detects that the TLB entry cache is too small (entry ejections are very frequent), it will increase the cache size automatically. In this variant, ASIDCacheSize is 8

3.1.7 Advanced SIMD and Floating-Point Features

SIMD and VFP instructions are implemented.
The model implements trapped exceptions if FPTrap is set to 1 in MVFR0 (for AArch32) or MVFR0_EL1 (for AArch64). When floating point exception traps are taken, cumulative exception flags are not updated (in other words, cumulative flag state is always the same as prior to instruction execution, even for SIMD instructions). When multiple enabled exceptions are raised by a single floating point operation, the exception reported is the one in least-significant bit position in FPSCR (for AArch32) or FPCR (for AArch64). When multiple enabled exceptions are raised by different SIMD element computations, the exception reported is selected from the lowest-index-number SIMD operation. Contact Imperas if requirements for exception reporting differ from these.
Trapped exceptions not are implemented in this variant (FPTrap=0)

3.1.8 Generic Interrupt Controller

GIC block is implemented (GICv1, including security extensions). Accesses to GIC registers can be viewed externally by connecting to the 32-bit GICRegisters bus port. Secure register accesses are at offset 0x0 on this bus; for example, a secure access to GIC register ICDDCR can be observed by monitoring address

0x00001000. Non-secure accesses are at offset 0x80000000 on this bus; for example, a non-secure access to GIC register ICDDCR can be observed by monitoring address 0x80001000

3.1.9 Debug Mask

It is possible to enable model debug features in various categories. This can be done statically using the "override_debugMask" parameter, or dynamically using the "debugflags" command. Enabled debug features are specified using a bitmask value, as follows:
Value 0x004: enable debugging of MMU/MPU mappings.
Value 0x020: enable debugging of reads and writes of GIC block registers.
Value 0x040: enable debugging of exception routing via the GIC model component.
Value 0x080: enable debugging of all system register accesses.
Value 0x100: enable debugging of all traps of system register accesses.
Value 0x200: enable verbose debugging of other miscellaneous behavior (for example, the reason why a particular instruction is undefined).
Value 0x400: enable debugging of Performance Monitor timers
Value 0x800: enable dynamic validation of TLB entries against in-memory page table contents (finds some classes of error where page table entries are updated without a subsequent flush of affected TLB entries).
All other bits in the debug bitmask are reserved and must not be set to non-zero values.

3.1.10 AArch32 Unpredictable Behavior

Many AArch32 instruction behaviors are described in the ARM ARM as CONSTRAINED UNPREDICTABLE. This section describes how such situations are handled by this model.

3.1.11 Equal Target Registers

Some instructions allow the specification of two target registers (for example, double-width SMULL, or some VMOV variants), and such instructions are CONSTRAINED UNPREDICTABLE if the same target register is specified in both positions. In this model, such instructions are treated as UNDEFINED.

3.1.12 Floating Point Load/Store Multiple Lists

Instructions that load or store a list of floating point registers (e.g. VSTM, VLDM, VPUSH, VPOP) are CONSTRAINED UNPREDICTABLE if either the uppermost register in the specified range is greater than 32 or (for 64-bit registers) if more than 16 registers are specified. In this model, such instructions are treated as UNDEFINED.

3.1.13 Floating Point VLD[2-4]/VST[2-4] Range Overflow

Instructions that load or store a fixed number of floating point registers (e.g. VST2, VLD2) are CONSTRAINED UNPREDICTABLE if the upper register bound exceeds the number of implemented floating point registers. In this model, these instructions load and store using modulo 32 indexing (consistent with AArch64 instructions with similar behavior).

3.1.14 If-Then (IT) Block Constraints

Where the behavior of an instruction in an if-then (IT) block is described as CONSTRAINED UNPREDICTABLE, this model treats that instruction as UNDEFINED.

3.1.15 Use of R13

In architecture variants before ARMv8, use of R13 was described as CONSTRAINED UNPREDICTABLE in many circumstances. From ARMv8, most of these situations are no longer considered unpredictable. This model allows R13 to be used like any other GPR, consistent with the ARMv8 specification.

3.1.16 Use of R15

Use of R15 is described as CONSTRAINED UNPREDICTABLE in many circumstances. This model allows such use to be configured using the parameter "unpredictableR15" as follows:
Value "undefined": any reference to R15 in such a situation is treated as UNDEFINED;
Value "nop": any reference to R15 in such a situation causes the instruction to be treated as a NOP;
Value "raz_wi": any reference to R15 in such a situation causes the instruction to be treated as a RAZ/WI (that is, R15 is read as zero and write-ignored);
Value "execute": any reference to R15 in such a situation is executed using the current value of R15 on read, and writes to R15 are allowed (but are not interworking).
Value "assert": any reference to R15 in such a situation causes the simulation to halt with an assertion message (allowing any such unpredictable uses to be easily identified).
In this variant, the default value of "unpredictableR15" is "undefined".

3.1.17 Unpredictable Instructions in Some Modes

Some instructions are described as CONSTRAINED UNPREDICTABLE in some modes only (for example, MSR accessing SPSR is CONSTRAINED UNPREDICTABLE in User and System modes). This model allows such use to be configured using the parameter "unpredictableModal", which can have values "undefined" or "nop". See the previous section for more information about the meaning of these values.
In this variant, the default value of "unpredictableModal" is "nop".

3.1.18 Integration Support

This model implements a number of non-architectural pseudo-registers and other features to facilitate integration.

3.1.19 Memory Transaction Query

Two registers are intended for use within memory callback functions to provide additional information about the current memory access. Register transactPL indicates the processor execution level of the current access (0-3). Note that for load/store translate instructions (e.g. LDRT, STRT) the reported execution level will be 0, indicating an EL0 access. Register transactAT indicates the type of memory access: 0 for a normal read or write; and 1 for a physical access resulting from a page table walk.

3.1.20 Page Table Walk Query

A banked set of registers provides information about the most recently completed page table walk. There are up to six banks of registers: bank 0 is for stage 1 walks, bank 1 is for stage 2 walks, and banks 2-5 are for stage 2 walks initiated by stage 1 level 0-3 entry lookups, respectively. Banks 1-5 are present only for processors with virtualization extensions. The currently active bank can be set using register PTWBankSelect. Register PTWBankValid is a bitmask indicating which banks contain valid data: for example, the value 0xb indicates that banks 0, 1 and 3 contain valid data.

Within each bank, there are registers that record addresses and values read during that page table walk. Register PTWBase records the table base address, register PTWInput contains the input address that starts a walk, register PTWOutput contains the result address and register PTWPgSize contains the page size (PTWOutput and PTWPgSize are valid only if the page table walk completes). Registers PTWAddressL0-PTWAddressL3 record the addresses of level 0 to level 3 entries read, respectively. Register PTWAddressValid is a bitmask indicating which address registers contain valid data: bits 0-3 indicate PTWAddressL0-PTWAddressL3, respectively, bit 4 indicates PTWBase, bit 5 indicates PTWInput, bit 6 indicates both PTWOutput and PTWPgSize. For example, the value 0x73 indicates that PTWBase, PTWInput, PTWOutput, PTWPgSize and PTWAddressL0-L1 are valid but PTWAddressL2-L3 are not. Register PTWAddressNS is a bitmask indicating whether an address is in non-secure memory: bits 0-3 indicate PTWAddressL0-PTWAddressL3, respectively, bit 4 indicates PTWBase, bit 6 indicates PTWOutput (PTWInput is a VA and thus has no secure/non-secure info). Registers PTWValueL0-PTWValueL3 contain page table entry values read at level 0 to level 3. Register PTWValueValid is a bitmask indicating which value registers contain valid data: bits 0-3 indicate PTWValueL0-PTWValueL3, respectively.

3.1.21 Artifact Page Table Walks

Registers are also available to enable a simulation environment to initiate an artifact page table walk (for example, to determine the ultimate PA corresponding to a given VA). Register PTWI_EL1S initiates a secure EL1 table walk for a fetch. Register PTWD_EL1S initiates a secure EL1 table walk for a load or store (note that current ARM processors have unified TLBs, so these registers are synonymous). Registers PTW[ID]_EL1NS initiate walks for non-secure EL1 accesses. Registers PTW[ID]_EL2 initiate EL2 walks. Registers PTW[ID]_S2 initiate stage 2 walks. Registers PTW[ID]_EL3 initiate AArch64 EL3 walks. Finally, registers PTW[ID]_current initiate current-mode walks (useful in a memory callback context). Each walk fills the query registers described above.

3.1.22 MMU and Page Table Walk Events

Two events are available that allow a simulation environment to be notified on MMU and page table walk actions. Event mmuEnable triggers when any MMU is enabled or disabled. Event pageTableWalk triggers on completion of any page table walk (including artifact walks).

3.1.23 Artifact Address Translations

A simulation environment can trigger an artifact address translation operation by writing to the architectural address translation registers (e.g. ATS1CPR). The results of such translations are written to an integration support register artifactPAR, instead of the architectural PAR register. This means that such artifact writes will not perturb architectural state.

3.1.24 TLB Invalidation

A simulation environment can cause TLB state for one or more address translation regimes in the processor to be flushed by writing to the artifact register ResetTLBs. The argument is a bitmask value, in which non-zero bits select the TLBs to be flushed, as follows:
Bit 0: EL0/EL1 stage 1 secure TLB
Bit 1: EL0/EL1 stage 1 non-secure TLB

3.1.25 Halt Reason Introspection

An artifact register HaltReason can be read to determine the reason or reasons that a processor is halted. This register is a bitfield, with the following encoding: bit 0 indicates the processor has executed a wait-for-event (WFE) instruction; bit 1 indicates the processor has executed a wait-for-interrupt (WFI) instruction; and bit 2 indicates the processor is held in reset.

3.1.26 System Register Access Monitor

If parameter "enableSystemMonitorBus" is True, an artifact 32-bit bus "SystemMonitor" is enabled for each PE. Every system register read or write by that PE is then visible as a read or write on this artifact bus, and can therefore be monitored using callbacks installed in the client environment (use opBusReadMonitorAdd/opBusWriteMonitorAdd or icmAddBusReadCallback/icmAddBusWriteCallback, depending on the client API). The format of the address on the bus is as follows:
bits 31:26 - zero
bit 25 - 1 if AArch64 access, 0 if AArch32 access
bit 24 - 1 if non-secure access, 0 if secure access
bits 23:20 - CRm value
bits 19:16 - CRn value
bits 15:12 - op2 value
bits 11:8 - op1 value
bits 7:4 - op0 value (AArch64) or coprocessor number (AArch32)
bits 3:0 - zero
As an example, to view non-secure writes to writes to CNTFRQ_EL0 in AArch64 state, install a write monitor on address range 0x020e0330:0x020e0333.

3.1.27 System Register Implementation

If parameter "enableSystemBus" is True, an artifact 32-bit bus "System" is enabled for each PE. Slave callbacks installed on this bus can be used to implement modified system register behavior (use opBusSlaveNew or icmMapExternalMemory, depending on the client API). The format of the address on the bus is the same as for the system monitor bus, described above.

3.2 Instance Parameters

Several parameters can be specified when a processor is instanced in a platform. For this processor instance 'cpu_A9MPx2' it has been instanced with the following parameters:

Table 4. Processor Instance 'cpu_A9MPx2' Parameters (Configurations)

Parameter	Value	Description
endian	little	Select processor endian (big or little)
simulateexceptions	simulateexceptions	Causes the processor simulate exceptions instead of halting
mips	100.0	The nominal MIPS for the processor

Table 5. Processor Instance 'cpu_A9MPx2' Parameters (Attributes)

Parameter Name	Value	Type
variant	Cortex-A9MPx2	enum

compatibility	ISA	enum
UAL	1	bool
showHiddenRegs	0	bool
override_CBAR	0xfffec000	uns32
override_GICD_TYPER_ITLines	6	uns32

3.3 Memory Map for processor 'cpu_A9MPx2' bus: 'smbus_HPS'

Processor instance 'cpu_A9MPx2' is connected to bus 'smbus_HPS' using master port 'INSTRUCTION'.
Processor instance 'cpu_A9MPx2' is connected to bus 'smbus_HPS' using master port 'DATA'.

Table 6. Memory Map ('cpu_A9MPx2' / 'smbus_HPS' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x3FFFFFFF	sram1	ram
remappable	remappable	CLKMGR0	trap
remappable	remappable	SYSMGR0	trap
remappable	remappable	emac0_dma	trap
remappable	remappable	emac1_dma	trap
remappable	remappable	gmac0	trap
remappable	remappable	gmac1	trap
remappable	remappable	pdma0	trap
0xFFC02000	0xFFC02FFF	uart0	dw-apb-uart
0xFFC03000	0xFFC03FFF	uart1	dw-apb-uart
0xFFC08000	0xFFC08FFF	timer0	dw-apb-timer
0xFFC09000	0xFFC09FFF	timer1	dw-apb-timer
0xFFD00000	0xFFD00FFF	timer2	dw-apb-timer
0xFFD01000	0xFFD01FFF	timer3	dw-apb-timer
0xFFD05000	0xFFD05FFF	RSTMGR0	RSTMGR
0xFFFEF000	0xFFFEFFFF	L2	L2CachePL310

3.4 Net Connections to processor: 'cpu_A9MPx2'

Table 7. Processor Net Connections ('cpu_A9MPx2')

Net Port	Net	Instance	Component
SPI199	ir199	timer0	dw-apb-timer
SPI200	ir200	timer1	dw-apb-timer
SPI201	ir201	timer2	dw-apb-timer
SPI202	ir202	timer3	dw-apb-timer
SPI194	ir194	uart0	dw-apb-uart
SPI195	ir195	uart1	dw-apb-uart
reset_CPU0	cpu0Reset	RSTMGR0	RSTMGR
reset_CPU1	cpu1Reset	RSTMGR0	RSTMGR

4.0 Processor [altera.ovpworld.org/processor/nios_ii/1.0] instance: cpu_Nios_II

4.1 Processor model type: 'nios_ii' variant 'Nios_II_F' definition

Imperas OVP processor models support multiple variants and details of the variants implemented in this

model can be found in:
- the Imperas installation located at ImperasLib/source/altera.ovpworld.org/processor/nios_ii/1.0/doc
- the OVP website: OVP_Model_Specific_Information_nios_ii_Nios_II_F.pdf

4.1.1 Description
Nios_II Family Processor Model.

4.1.2 Licensing
Open Source Apache 2.0

4.1.3 Limitations
No Custom instructions.
No Cache model.
No JTAG.

4.1.4 Verification
Models have been extensively tested by Imperas, and validated against tests from Altera.

4.1.5 Features
Barrel Shifter.
Configurable MPU.
Configurable MMU.
Shadow Register Sets.
Hardware Multiply.
Hardware Divide.
Hardware Extended Multiply.

4.2 Instance Parameters
Several parameters can be specified when a processor is instanced in a platform. For this processor instance 'cpu_Nios_II' it has been instanced with the following parameters:

Table 8. Processor Instance 'cpu_Nios_II' Parameters (Configurations)

Parameter	Value	Description
endian	little	Select processor endian (big or little)
simulateexceptions	simulateexceptions	Causes the processor simulate exceptions instead of halting
mips	125.0	The nominal MIPS for the processor

Table 9. Processor Instance 'cpu_Nios_II' Parameters (Attributes)

Parameter Name	Value	Type
variant	Nios_II_F	enum
BREAK_VECTOR	0xc7fff820	uns32
EXCEPTION_VECTOR	0xd0000020	uns32
RESET_VECTOR	0xc2800000	uns32

FAST_TLB_MISS_EXCEPTION_VECTOR	0xc7fff400	uns32
HW_DIVIDE	1	bool
HW_MULTIPLY	1	bool
HW_MULX	0	bool
INCLUDE_MMU	1	bool
MMU_TLB_SET_ASSOCIATIVITY	16	string
MMU_TLB_ENTRIES	128	string
MMU_PID_BITS	8	uns32
DATA_ADDR_WIDTH	29	uns32
INST_ADDR_WIDTH	29	uns32
TEST_HALT_EXIT	1	bool
EXCEPTION_EXTRA_INFORMATION	1	bool

4.3 Memory Map for processor 'cpu_Nios_II' bus: 'ibus_3c120'

Processor instance 'cpu_Nios_II' is connected to bus 'ibus_3c120' using master port 'INSTRUCTION'.

Table 10. Memory Map ('cpu_Nios_II' / 'ibus_3c120' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0xFFFFFFFF	pb_ibus_to_smbus_3c120	bridge

Table 11. Bridged Memory Map ('cpu_Nios_II' / 'pb_ibus_to_smbus_3c120' / 'smbus_3c120' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x3FFFFF	flash_mem_64m	ram
0x7FFF400	0x7FFF7FF	tlb_miss_ram_1k	ram
0x10000000	0x17FFFFFF	pb_cpu_to_ddr2_bot	ram

4.4 Memory Map for processor 'cpu_Nios_II' bus: 'dbus_3c120'

Processor instance 'cpu_Nios_II' is connected to bus 'dbus_3c120' using master port 'DATA'.

Table 12. Memory Map ('cpu_Nios_II' / 'dbus_3c120' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFF	pb_dbus_to_smbus_3c120_1	bridge
0x8000000	0x87FFFFF	pb_cpu_to_io	bridge
0x8800000	0xFFFFFFFF	pb_dbus_to_smbus_3c120_2	bridge

Table 13. Bridged Memory Map ('cpu_Nios_II' / 'pb_dbus_to_smbus_3c120_1' / 'smbus_3c120' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x3FFFFF	flash_mem_64m	ram
0x7FFF400	0x7FFF7FF	tlb_miss_ram_1k	ram

Table 14. Bridged Memory Map ('cpu_Nios_II' / 'pb_cpu_to_io' / 'iobus_3c120' [width: 32])

Lo Address	Hi Address	Instance	Component
0x4C80	0x4C9F	uart_s1	Uart

0x4D40	0x4D47	sysid	SystemIDCore
0x4D50	0x4D57	jtag_uart	JtagUart
0x400000	0x400017	timer_1ms	IntervalTimer32Core

Table 15. Bridged Memory Map ('cpu_Nios_II' / 'pb_dbus_to_smbus_3c120_2' / 'smbus_3c120' [width: 32])

Lo Address	Hi Address	Instance	Component
0x10000000	0x17FFFFF	pb_cpu_to_ddr2_bot	ram

4.5 Net Connections to processor: 'cpu_Nios_II'

Table 16. Processor Net Connections ('cpu_Nios_II')

Net Port	Net	Instance	Component
d_irq10	irq10	uart_s1	Uart
d_irq1	irq1	jtag_uart	JtagUart
d_irq11	irq11	timer_1ms	IntervalTimer32Core

5.0 Peripheral Instances

5.1 Peripheral [arm.ovpworld.org/peripheral/L2CachePL310/1.0] instance: L2

5.1.1 Description
ARM PL310 L2 Cache Control Registers

5.1.2 Licensing
Open Source Apache 2.0

5.1.3 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

5.1.4 Reference
ARM PrimeCell Level 2 Cache Controller (PL310) Technical Reference Manual (ARM DDI 0246)

There are no configuration options set for this peripheral instance.

5.2 Peripheral [altera.ovpworld.org/peripheral/dw-apb-timer/1.0] instance: timer0

5.2.1 Description
Model of dw-apb-timer for CycloneV platform.

5.2.2 Limitations
Only functionality required for Altera Cyclone-V is implemented: single timer, 32 bits, little endian only

Resolution of this timer is limited to the simulation time slice (aka quantum) size

5.2.3 Reference
Cyclone V Device Handbook Volume 3: Hard Processor System Technical Reference Manual cv_5v4 2013.12.30

5.2.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

5.3 Peripheral [altera.ovpworld.org/peripheral/dw-apb-timer/1.0] instance: timer1

5.3.1 Description
Model of dw-apb-timer for CycloneV platform.

5.3.2 Limitations
Only functionality required for Altera Cyclone-V is implemented: single timer, 32 bits, little endian only
Resolution of this timer is limited to the simulation time slice (aka quantum) size

5.3.3 Reference
Cyclone V Device Handbook Volume 3: Hard Processor System Technical Reference Manual cv_5v4 2013.12.30

5.3.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

5.4 Peripheral [altera.ovpworld.org/peripheral/dw-apb-timer/1.0] instance: timer2

5.4.1 Description
Model of dw-apb-timer for CycloneV platform.

5.4.2 Limitations
Only functionality required for Altera Cyclone-V is implemented: single timer, 32 bits, little endian only
Resolution of this timer is limited to the simulation time slice (aka quantum) size

5.4.3 Reference
Cyclone V Device Handbook Volume 3: Hard Processor System Technical Reference Manual cv_5v4 2013.12.30

5.4.4 Licensing

Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

5.5 Peripheral [altera.ovpworld.org/peripheral/dw-apb-timer/1.0] instance: timer3

5.5.1 Description
Model of dw-apb-timer for CycloneV platform.

5.5.2 Limitations
Only functionality required for Altera Cyclone-V is implemented: single timer, 32 bits, little endian only
Resolution of this timer is limited to the simulation time slice (aka quantum) size

5.5.3 Reference
Cyclone V Device Handbook Volume 3: Hard Processor System Technical Reference Manual cv_5v4 2013.12.30

5.5.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

5.6 Peripheral [altera.ovpworld.org/peripheral/dw-apb-uart/1.0] instance: uart0

5.6.1 Licensing
Open Source Apache 2.0

5.6.2 Description
Model of dw-apb-uart UART for CycloneV platform.

5.6.3 Limitations
No modeling of baudrate.
No modem support (DTR etc).
No support for parity.
No means to simulate errors.
Derived from national.ovpworld.org 16450 model. Just enough to do basic tty capabilities.
Only first 8 registers implemented.

5.6.4 Reference
Cyclone V Device Handbook Volume 3: Hard Processor System Technical Reference Manual cv_5v4 2013.12.30

Table 17. Configuration options (attributes) set for instance 'uart0'

Attribute	Value	Type	Expression
outfile	uart0.log	string	
console	1	bool	
finishOnDisconnect	1	bool	

5.7 Peripheral [altera.ovpworld.org/peripheral/dw-apb-uart/1.0] instance: uart1

5.7.1 Licensing
Open Source Apache 2.0

5.7.2 Description
Model of dw-apb-uart UART for CycloneV platform.

5.7.3 Limitations
No modeling of baudrate.
No modem support (DTR etc).
No support for parity.
No means to simulate errors.
Derived from national.ovpworld.org 16450 model. Just enough to do basic tty capabilities.
Only first 8 registers implemented.

5.7.4 Reference
Cyclone V Device Handbook Volume 3: Hard Processor System Technical Reference Manual cv_5v4 2013.12.30

Table 18. Configuration options (attributes) set for instance 'uart1'

Attribute	Value	Type	Expression
outfile	uart1.log	string	
console	1	bool	

5.8 Peripheral [altera.ovpworld.org/peripheral/RSTMGR/1.0] instance: RSTMGR0

5.8.1 Description
Altera Cyclone V Reset Manager

5.8.2 Limitations
Only register mpumodrst cpu0 and cpu1 reset functionality is implemented

5.8.3 Licensing
Open Source Apache 2.0

5.8.4 Reference
Cyclone V Device Handbook Volume 3: Hard Processor System Technical Reference Manual cv_5v4

2013.12.30

There are no configuration options set for this peripheral instance.

5.9 Peripheral [ovpworld.org/peripheral/trap/1.0] instance: SYSMGR0

5.9.1 Description

Open a port and allocate a region that is defined by parameters.
The region can be configured to act as standard memory or can report read/write accesses.

5.9.2 Licensing

Open Source Apache 2.0

5.9.3 Limitations

This peripheral cannot be used in a hardware description used to generate a TLM platform.

5.9.4 Reference

This is not based upon the operation of a real device but is intended to be used for bring up and development of new virtual platforms.

Table 19. Configuration options (attributes) set for instance 'SYSMGR0'

Attribute	Value	Type	Expression
portAddress	0xffd08000	uns32	

5.10 Peripheral [ovpworld.org/peripheral/trap/1.0] instance: CLKMGR0

5.10.1 Description

Open a port and allocate a region that is defined by parameters.
The region can be configured to act as standard memory or can report read/write accesses.

5.10.2 Licensing

Open Source Apache 2.0

5.10.3 Limitations

This peripheral cannot be used in a hardware description used to generate a TLM platform.

5.10.4 Reference

This is not based upon the operation of a real device but is intended to be used for bring up and development of new virtual platforms.

Table 20. Configuration options (attributes) set for instance 'CLKMGR0'

Attribute	Value	Type	Expression
portAddress	0xffd04000	uns32	

5.11 Peripheral [ovpworld.org/peripheral/trap/1.0] instance: pdma0

5.11.1 Description

Open a port and allocate a region that is defined by parameters.
The region can be configured to act as standard memory or can report read/write accesses.

5.11.2 Licensing

Open Source Apache 2.0

5.11.3 Limitations

This peripheral cannot be used in a hardware description used to generate a TLM platform.

5.11.4 Reference

This is not based upon the operation of a real device but is intended to be used for bring up and development of new virtual platforms.

Table 21. Configuration options (attributes) set for instance 'pdma0'

Attribute	Value	Type	Expression
portAddress	0xffe01000	uns32	

5.12 Peripheral [ovpworld.org/peripheral/trap/1.0] instance: gmac0

5.12.1 Description

Open a port and allocate a region that is defined by parameters.
The region can be configured to act as standard memory or can report read/write accesses.

5.12.2 Licensing

Open Source Apache 2.0

5.12.3 Limitations

This peripheral cannot be used in a hardware description used to generate a TLM platform.

5.12.4 Reference

This is not based upon the operation of a real device but is intended to be used for bring up and development of new virtual platforms.

Table 22. Configuration options (attributes) set for instance 'gmac0'

Attribute	Value	Type	Expression
portAddress	0xff700000	uns32	

5.13 Peripheral [ovpworld.org/peripheral/trap/1.0] instance: emac0_dma

5.13.1 Description

Open a port and allocate a region that is defined by parameters.
The region can be configured to act as standard memory or can report read/write accesses.

5.13.2 Licensing

Open Source Apache 2.0

5.13.3 Limitations

This peripheral cannot be used in a hardware description used to generate a TLM platform.

5.13.4 Reference

This is not based upon the operation of a real device but is intended to be used for bring up and development of new virtual platforms.

Table 23. Configuration options (attributes) set for instance 'emac0_dma'

Attribute	Value	Type	Expression
portAddress	0xff701000	uns32	

5.14 Peripheral [ovpworld.org/peripheral/trap/1.0] instance: gmac1

5.14.1 Description

Open a port and allocate a region that is defined by parameters.
The region can be configured to act as standard memory or can report read/write accesses.

5.14.2 Licensing

Open Source Apache 2.0

5.14.3 Limitations

This peripheral cannot be used in a hardware description used to generate a TLM platform.

5.14.4 Reference

This is not based upon the operation of a real device but is intended to be used for bring up and development of new virtual platforms.

Table 24. Configuration options (attributes) set for instance 'gmac1'

Attribute	Value	Type	Expression
portAddress	0xff702000	uns32	

5.15 Peripheral [ovpworld.org/peripheral/trap/1.0] instance: emac1_dma

5.15.1 Description

Open a port and allocate a region that is defined by parameters.
The region can be configured to act as standard memory or can report read/write accesses.

5.15.2 Licensing

Open Source Apache 2.0

5.15.3 Limitations

This peripheral cannot be used in a hardware description used to generate a TLM platform.

5.15.4 Reference

This is not based upon the operation of a real device but is intended to be used for bring up and development of new virtual platforms.

Table 25. Configuration options (attributes) set for instance 'emac1_dma'

Attribute	Value	Type	Expression
portAddress	0xff703000	uns32	

5.16 Peripheral [arm.ovpworld.org/peripheral/SmartLoaderArmLinux/1.0] instance: smartLoader

5.16.1 Licensing

Open Source Apache 2.0

5.16.2 Description

Psuedo-peripheral to perform memory initialisation for an ARM based Linux kernel boot: Loads Linux kernel image file and (optional) initial ram disk image into memory. Writes ATAG data into memory. Writes tiny boot code at physical memory base that configures the registers as expected by Linux Kernel and then jumps to boot address (image load address by default).

5.16.3 Limitations

Only supports little endian

5.16.4 Reference

See ARM Linux boot requirements in Linux source tree at documentation/arm/Booting

Table 26. Configuration options (attributes) set for instance 'smartLoader'

Attribute	Value	Type	Expression
boardid	0xffffffff	uns32	
kernel	zImage	string	
initrd	fs.img	string	
command	mem=1024M console=ttyS0	string	
physicalbase	0x0	uns32	

memsize	0x40000000	uns32	
disable	0	bool	

5.17 Peripheral [altera.ovpworld.org/peripheral/Uart/1.0] instance: uart_s1

5.17.1 Licensing
Open Source Apache 2.0

5.17.2 Description
Altera Avalon UART

5.17.3 Limitations
No Support for pin level transitions

5.17.4 Reference
Embedded Peripherals IP User Guide, UG-01085-11.0 11.0 June 2011

There are no configuration options set for this peripheral instance.

5.18 Peripheral [altera.ovpworld.org/peripheral/SystemIDCore/1.0] instance: sysid

5.18.1 Licensing
Open Source Apache 2.0

5.18.2 Description
Altera Avalon System ID Core

5.18.3 Limitations
No Support for pin level transitions

5.18.4 Reference
Embedded Peripherals IP User Guide, UG-01085-11.0 11.0 June 2011

There are no configuration options set for this peripheral instance.

5.19 Peripheral [altera.ovpworld.org/peripheral/JtagUart/1.0] instance: jtag_uart

5.19.1 Licensing
Open Source Apache 2.0

5.19.2 Description
Altera Avalon JTAG UART

5.19.3 Limitations

No Support for pin level transitions

5.19.4 Reference

Embedded Peripherals IP User Guide, UG-01085-11.0 11.0 June 2011

Table 27. Configuration options (attributes) set for instance 'jtag_uart'

Attribute	Value	Type	Expression
writeIRQThreshold	8	uns32	
readIRQThreshold	8	uns32	
writeBufferDepth	64	uns32	
readBufferDepth	64	uns32	
console	1	bool	
outfile	jtag_uart.log	string	
finishOnDisconnect	1	bool	

5.20 Peripheral [altera.ovpworld.org/peripheral/IntervalTimer32Core/1.0] instance: timer_1ms

5.20.1 Licensing

Open Source Apache 2.0

5.20.2 Description

Altera Avalon Interval Timer32 Core

5.20.3 Limitations

No Support for pin level transitions

5.20.4 Reference

Altera Interval Timer Core

There are no configuration options set for this peripheral instance.

6.0 Overview of Imperas OVP Virtual Platforms

This document provides the details of the usage of an Imperas OVP Virtual Platform / Module. The first half of the document covers specifics of this particular virtual platform / module.

This second part of the document, includes information about Imperas OVP virtual platforms and modules, how they are built and used.

The Imperas virtual platforms are designed to provide a base for you to run high-speed software simulations of CPU-based SoCs and platforms on any suitable PC. They are typically based on the functionality of vendors fixed or evaluation platforms, enabling you to simulate software on these reference platforms. Typically virtual platforms are fixed and require the vendor to modify or extend them. Imperas virtual platforms are different in that they enable you to extend the functionality of the virtual platform, to closer reflect your own platform, by adding more component models, running different operating systems or adding additional applications.

Imperas virtual platforms are created using the Imperas iGen technology, allowing them to be used with Imperas OVP based simulators and also with Accellera/OSCI compliant SystemC simulators and commercial EDA System Design environments that use SystemC.

Virtual platforms include simulation models of the target devices, including the processor model(s) for the target device plus enough peripheral models to boot an operating system or run bare metal applications. The platform and the peripheral models used in most of the virtual platforms are open source, so that you can easily add new models to the platform as well as modify the existing models. Some models are only provided as binary, normally because the IP owner has restricted the release of the model source. In this case, please contact Imperas for more information.

There are typically several generic flavors of the virtual platforms for specific processor families, some targeting full operating systems, such as Linux, and some which focus on Real Time Operating Systems (RTOS) such as Mentor Nucleus or freeRTOS. OVP models of the processor cores are included in the virtual platforms, and for those processors which support mulitple cores SMP Linux is often supported for that virtual platform. For all of these virtual platforms, many of the peripheral components of the platform are modeled, often including the Ethernet and USB components. The semi-hosting capability of the Imperas virtual platform simulator products enables connection via the Ethernet and USB components from the virtual platform to the real world via the x86 host machine.

The Imperas OVP CPU models are written using the OVP Virtual Machine Interface (VMI) API that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. The processor models are Instruction Accurate and do not model the detailed cycle timing of the processor and they implement functionality at the level of a Programmers View of the processor and peripherals and the software running on them does not know it is not running on hardware. Many models are provided as a binary shared object

and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model. The models are run through an extensive QA and regression testing process and most processor model families are validated using technology provided by the processor IP owners. All the models in this platform are developed with the Open Virtual Platforms APIs and are implemented in C. A platform can be modeled as different levels of hierarchy using separately describable and compilable modules.

More information on modeling and APIs can be found on the www.OVPworld.org site.

7.0 Getting Started with Imperas OVP Virtual Platforms

Virtual platforms are downloadable from the OVPworld website OVPworld.org/downloads. You need to browse and look for '<platform processor name> Examples'. You do need to be registered and logged in on the OVP site to download. OVPworld currently provides 32 bit host versions of packages containing virtual platforms.

When downloading, choose, Linux or Windows host. 32 bit packages can be installed and executed on 32 bit or 64 bit hosts. If you require a 64 bit host version please contact Imperas.

For example, for the ARM Versatile Express platform booting Linux on Cortex-A15MP Single, Dual, and Quad core procesors, you would want the download package: 'OVPsim_demo_Linux_ArmVersatileExpress_arm_Cortex-A15MP'.

Most virtual platform packages contain the platform and all the processor and peripheral models needed. You will need to download a simulator to run the platform. You can use OVPsim, downloadable from OVPworld.org/downloads, or you can use one of the Imperas simulators (imperas.com/products) available commercially from Imperas.

8.0 Simulating Software

8.1 Getting a license key to run

After you have downloaded you will need a runtime license key before the simulators will run. For OVPsim please visit OVPworld.org/likey and provide the required information and an evaluation/demo license key will be automatically sent to you. If you are using Imperas, then please contact Imperas for a license key.

8.2 Normal runs

To run a platform, read the section below on command line control of the platform and the section on setting command line arguments.

8.3 Loading Software

For most virtual platforms the platform is already configured to run the default software application/program and there is normally a script to run that sets some arguments. You can then copy/edit this script to select your own applications etc.

The example application programs are typically .elf format files and are provided pre-compiled. There are normally makefiles and associated scripts to recompile the example applications.

To find more information about compiling and loading software, the following document should be looked at: Imperas_Installation_and_Getting_Started.pdf.

8.4 Semihosting

In a virtual platform, semihosting is not normally used as there is normally hardware that implements the appropriate functionality - for example I/O will be handled by UARTs etc.

8.5 Using a terminal (UART)

If the platform includes one or more UARTs you will need to connect a terminal program to it so that you can see output and type into the simulated program. Review the list of peripherals below and see what configuration options it has been set with. In most cases there is an option to set to instruct the simulator to 'pop up' a terminal window connected to the simulated UART.

8.6 Interacting with the simulation (keyboard and mouse)

If the platform has a simulated UART you can normally set a command to get the simulator to pop up a terminal window allowing you to see output from the simulated UART and also allowing you to type characters into the UART that can be processed by the simulated software.

If your simulated platform has an LCD device then you can often configure it to recognize mouse movements and mouse clicks - allowing full interaction.

To see these interactions in action, have a look at some of the available videos available at OVPworld.org/demosandvideos.

8.7 More Information (Documentation) on Simulation

To find more information about running simulations and more of the options the simulators provide, the following documents should be looked at:
Imperas_Installation_and_Getting_Started.pdf
Simulation_Control_of_Platforms_and_Modules_User_Guide.pdf
Advanced_Simulation_Control_of_Platforms_and_Modules_User_Guide.pdf
OVP_Control_File_User_Guide.pdf

A full list of the currently available OVP documentation is available: OVPworld.org/documentation.

9.0 Debugging Software running on an Imperas OVP Virtual Platform

The Imperas and OVP simulators have several different interfaces to debuggers. These include several proprietary formats and also the standard GNU RSP format is supported allowing many compatible debuggers to be used. Below are some examples that Imperas directly support.

9.1 Debugging with GDB

A GNU debugger (GDB) can be connected to a processor in a platform using the RSP protocol. This allows the application program running on a processor to be debugged using a specific GDB for the processor selected. When using the Imperas Professional products many connections can be made allowing a GDB to be connected to all the processors in the platform.

The use of GDB is documented: OVPsim_Debugging_Applications_with_GDB_User_Guide.pdf.

*9.2 Debugging with Imperas M*DBG*

The Imperas multi-processor debugger can be connected to a platform and through this connection you can debug application programs running on all of the processors instanced within the platform. It is also capable, within this single unified environment, to debug peripheral model behavioral code in conjunction with the processor application programs.

For more information please see the Imperas M*DBG user guide.

The Imperas multi-processor debugger is also capable of controlling the Imperas Verification Analysis aand Profiling (VAP) tools in real time, making them invaluable to application program development, debugging and analysis.

For more information please see the Imperas VAP tools user guide.

9.3 Debugging with the Imperas eGui and GDB

Imperas eGui gives a GUI front end to the use of the GDB debugger. It allows use of all the features of GDB including source level application program debugging on processors.

*9.4 Debugging with the Imperas eGui and M*DBG*

Imperas eGui gives a GUI front end to the Imperas multi-processor debugger. It provides all the features of this debugger but does so with source level application program debugging on processors and source level debugging of the behavioral code on peripheral components in the platform. A context view shows all the processor and peripheral components within the platform and allows switching between them to examine the state of each at the event at which the simulation was stopped

Imperas eGui provides a menu from which the Imperas VAP tools can be controlled.

9.5 Debugging with Imperas eGui and Eclipse

Imperas provide a GUI based on Eclipse called eGui. This provides a GUI front end to use with a standard GDB or the Imperas MPD (Multi-Processor Debugger).

The use of eGui is documented: eGui_Eclipse_User_Guide.pdf.

A standard Eclipse CDT development environment can be connected to one or more processors in a

platform (multiple processors require an Imperas professional product). The simulation platform is started remotely or using the external tool feature in Eclipse, opens a debug port and awaits the connection with Eclipse. All features provided by the Eclipse CDT development environment are available to be used to debug software applications executing on the processors in the platform.

The use of Eclipse is documented: OVPsim_Debugging_Applications_with_Eclipse_User_Guide.pdf.

9.6 Debugging applications running under a simulated operating system

If the simulated platform is running an Operating System and the platform has a UART or Ethernet etc connection then it is often possible to connect an external debugger and debug the applications running under the simulated operating system.

An example would be a simulated platform running the Linux operating system, such as the MIPS Malta, or ARM Versatile Express. Within the simulated Linux you can start a gdbserver that connects from within the simulation through a UART out to the host PC via a port. Within the host PC you start a terminal program and connect to the port with a debugger such as GDB and can then debug the simulated user application.

10.0 Modifying the Platform / Module

10.1 Platforms / Modules use C/C++ and OVP APIs

The Imperas and OVP simulators execute a platform / module that is written in C/C++ and that makes function calls into the simulator's APIs. Thus the virtual platform / module is compiled from C/C++ into a binary shared object that the simulator loads and runs. OVP provides the definition and documentation that defines the C APIs for modeling the platforms, modules, the peripherals, and the processors. You can find more information about these APIs on the OVP website and in the OVP API documentation.

10.2 Platforms/Modules/Peripherals can be easily built with iGen from Imperas

Imperas provides a product 'iGen' that takes an input script file and creates the C/C++ files needed for platforms, modules, and peripherals - it creates the C/C++ file that is compiled into the platform, module or peripheral that is needed as an object file by the simulator. iGen creates the C/C++ files, you then need to add any necessary behaviors or further details etc. For platforms iGen creates either a C platform or a C++ SystemC TLM2 platform. For peripherals or modules iGen creates the C files and also provides a native C++ SystemC TLM2 interface to allow the peripheral/module to be instantiated in SystemC TLM2 platforms.

Information on iGen is available from: imperas.com/products.

10.3 Re-configuring the platform

There will nornmally be several configuration options that you can set when running the platform without the neeed to change any source. Refer to the section above on command line arguments. If these do not allow you to make the changes you need, then you may need to edit and recompile the source of the platform.

The source of the platform, modules, and the source of the peripherals will be installed as part of the packages you are using. The sources are located in the Imperas/OVP installation VLNV source tree. The VLNV term refers to: Vendor (eg arm.ovpworld.org), Library (eg platform), Name, (eg ArmVersatileExpress-CA15), and Version (eg 1.0). To modify the platform, locate the platform source files.

If you are an Imperas user and have access to iGen, we recommend you modify the source script files and regenerate and recompile the C that makes up the platform. Refer to the Imperas iGen model generator guide and the Imperas platform generator guide.

If you are using the C or SystemC TLM2 platforms with OVPsim, then you can edit the C/C++ files, recompile the source directly using the supplied makefiles, and the run the simulator directly with the resultant shared object.

10.4 Replacing peripherals components

If you need to replace peripherals, find the appropriate place in the source of the platform, make the change you need, and recompile etc. Look in the library for documentation on available peripherals and their configuration options.

10.5 Adding new peripherals components

If you need to add peripherals, find the appropriate place in the source, make the additions you need, and recompile etc. Look in the library for documentation on available peripherals and their configuration options.

If you need to create new peripheral components then use iGen to very quickly create the necessary C/C++ files that get you started. With iGen you can create peripherals with register/memory state in a few lines of iGen source. When adding behavior to the peripherals refer to the OVP API documentation.

11.0 Available Virtual Platforms

Table 28. Imperas / OVP Extendable Platform Kits (13 available)

Name	Vendor
AlteraCycloneIII_3c120	altera.ovpworld.org
AlteraCycloneV_HPS	altera.ovpworld.org
ArmIntegratorCP	arm.ovpworld.org
ArmVersatileExpress	arm.ovpworld.org
ArmVersatileExpress-CA15	arm.ovpworld.org
ArmVersatileExpress-CA9	arm.ovpworld.org
AtmelAT91SAM7	atmel.ovpworld.org
FreescaleKinetis60	freescale.ovpworld.org
FreescaleKinetis64	freescale.ovpworld.org
FreescaleVybridVFxx	freescale.ovpworld.org
MipsMalta	mips.ovpworld.org
RenesasUPD70F3441	renesas.ovpworld.org
XilinxML505	xilinx.ovpworld.org

Table 29. Imperas General Virtual Platforms (6 available)

Name	Vendor
arm-ti-eabi	arm.imperas.com
armm-ti-coff	arm.imperas.com
armm-ti-eabi	arm.imperas.com
HeteroAlteraCycloneV_HPS_CycloneIII_3c120	imperas.ovpworld.org
HeteroArmNucleusMIPSLinux	imperas.ovpworld.org
SiFiveFU540	imperas.ovpworld.org

Table 30. Imperas Modules (component of other platforms) (55 available)

Name	Vendor
AlteraCycloneIII_3c120	altera.ovpworld.org
AlteraCycloneV_HPS	altera.ovpworld.org
AE350	andes.ovpworld.org
ARMv8-A-FMv1	arm.ovpworld.org
ArmIntegratorCP	arm.ovpworld.org
ArmVersatileExpress	arm.ovpworld.org
ArmVersatileExpress-CA15	arm.ovpworld.org
ArmVersatileExpress-CA9	arm.ovpworld.org
AtmelAT91SAM7	atmel.ovpworld.org
ArmCortexMFreeRTOS	imperas.ovpworld.org
ArmCortexMuCOS-II	imperas.ovpworld.org
ArmuKernel	imperas.ovpworld.org
ArmuKernelDual	imperas.ovpworld.org
BareMetalMIPS	imperas.ovpworld.org
Dual_ARMv8-A-FMv1_VLAN	imperas.ovpworld.org
Hetero_1xArm_3xMips32	imperas.ovpworld.org
Hetero_ARM_RISCV_NeuralNetwork	imperas.ovpworld.org

Hetero_ARMv8-A-FMv1_Cortex-M3	imperas.ovpworld.org
Hetero_ARMv8-A-FMv1_MIPS_microAptiv	imperas.ovpworld.org
Hetero_AlteraCycloneV_HPS_AlteraCycloneIII_3c120	imperas.ovpworld.org
Hetero_ArmIntegratorCP_XilinxMicroBlaze	imperas.ovpworld.org
Hetero_ArmVersatileExpress_MipsMalta	imperas.ovpworld.org
Hetero_ArmVersatileExpress_XilinxMicroBlaze	imperas.ovpworld.org
Quad_ArmVersatileExpress-CA15	imperas.ovpworld.org
RiscvRV32FreeRTOS	imperas.ovpworld.org
MipsMalta	mips.ovpworld.org
iMX6S	nxp.ovpworld.org
RenesasUPD70F3441	renesas.ovpworld.org
ghs-multi	renesas.ovpworld.org
virtio	riscv.ovpworld.org
FaultInjection	safepower.ovpworld.org
PublicDemonstrator	safepower.ovpworld.org
Zynq_PL_DualMicroblaze	safepower.ovpworld.org
Zynq_PL_NoC	safepower.ovpworld.org
Zynq_PL_NoC_node	safepower.ovpworld.org
Zynq_PL_NostrumNoC	safepower.ovpworld.org
Zynq_PL_NostrumNoC_node	safepower.ovpworld.org
Zynq_PL_RO	safepower.ovpworld.org
Zynq_PL_SingleMicroblaze	safepower.ovpworld.org
Zynq_PL_TTELNoC	safepower.ovpworld.org
Zynq_PL_TTELNoC_node	safepower.ovpworld.org
Zynq_PL_TTELNoC_processing_node_public_demonstrator	safepower.ovpworld.org
Zynq_PL_TTELNoC_public_demonstrator	safepower.ovpworld.org
Zynq_PL_TTELNoC_sensor_actor_node_public_demonstrator	safepower.ovpworld.org
FU540	sifive.ovpworld.org
S51CC	sifive.ovpworld.org
coreip-s51-arty	sifive.ovpworld.org
coreip-s51-rtl	sifive.ovpworld.org
dualFifo	vendor.com
XilinxML505	xilinx.ovpworld.org
Zynq	xilinx.ovpworld.org
Zynq_PL_Default	xilinx.ovpworld.org
Zynq_PS	xilinx.ovpworld.org
zc702	xilinx.ovpworld.org
zc706	xilinx.ovpworld.org

Table 31. Imperas / OVP Bare Metal Virtual Platforms (22 available)

Name	Vendor
BareMetalNios_IISingle	altera.ovpworld.org
BareMetalArcSingle	arc.ovpworld.org
BareMetalArm7Single	arm.ovpworld.org
BareMetalArmCortexADual	arm.ovpworld.org
BareMetalArmCortexASingle	arm.ovpworld.org
BareMetalArmCortexASingleAngelTrap	arm.ovpworld.org
BareMetalArmCortexMSingle	arm.ovpworld.org

ArmCortexMFreeRTOS	imperas.ovpworld.org
ArmCortexMuCOS-II	imperas.ovpworld.org
BareMetalArmx1Mips32x3	imperas.ovpworld.org
Or1kUclinux	imperas.ovpworld.org
BareMetalM14KSingle	mips.ovpworld.org
BareMetalMips32Dual	mips.ovpworld.org
BareMetalMips32Single	mips.ovpworld.org
BareMetalMips64Single	mips.ovpworld.org
BareMetalMipsDual	mips.ovpworld.org
BareMetalMipsSingle	mips.ovpworld.org
BareMetalOr1kSingle	ovpworld.org
BareMetalM16cSingle	posedgesoft.ovpworld.org
BareMetalPowerPc32Single	power.ovpworld.org
BareMetalV850Single	renesas.ovpworld.org
ghs-multi	renesas.ovpworld.org

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