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A novel AlGaN/GaN multiple aperture vertical high electron mobility transistor with silicon oxide current blocking layer

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ABSTRACT

In this work, a new AlGaN/GaN vertical high electron mobility transistor (HEMT) with silicon oxide (SiO_2) current blocking layer (CBL) is designed and studied numerically for high-power devices. To overcome the excessive vertical leakage through CBL layer in conventional p-GaN CBL vertical HEMT, large band-gap material, SiO_2 is, for the first time, introduced as a CBL material. The band-gap of SiO_2 leads to a large barrier which can effectively suppress the vertical leakage even at high drain bias and enhance the breakdown voltage to 1270 V (154% enhancement compared with the conventional p-GaN CBL vertical HEMT). In addition, a device with four parallel apertures is proposed to reduce the aperture resistance, where the total aperture thickness is equal to the aperture thickness of the conventional one. Therefore, the drain current is increased. We not only focus on the vertical leakage control, but also, on the drain current boost (7% improvement).

1. Introduction

Gallium nitride (GaN) is a suitable material for high-voltage power-switching devices due to its critical electric field [1]. Therefore, the breakdown voltage (BV) of a GaN device can be significantly higher than the currently existing silicon device with the same on-state resistance (R_{on}). GaN lateral high electron mobility transistors (HEMTs) in which current flows near the surface are commonly used because of their crucial properties, such as low conduction losses (i.e., low on-state resistance), low switching losses, and ease of fabrication [2]. However, there are still many open questions related to the performance of these GaN based lateral devices [3]. Because of a linear dependence of breakdown voltage with a specific R_{on} [4], a device with large gate drain distance is required to increase the breakdown voltage in lateral HEMTs. To get rid of this problem, a vertical structure could be put into practice [5]. The vertical device is area-cost-effective for both high BV and low R_{on} [6]. Easier package is also one of the additional advantages of the vertical device. Furthermore, in vertical devices, DC-RF dispersion induced by surface states may be mitigated because high-field regions can be buried below the gate electrode [7]. Recent studies on vertical HEMT are with an Mg-doped GaN current blocking layer (CBL) [8,9]. However, CBL is very critical in the vertical HEMT. Because of technological difficulties, channel and barrier layers above the CBL must be regrown. Nevertheless, regrowth was performed under high-temperature conditions leading to pits and exhibited large leakage currents through the insulating layer [7]. The leakage via the Mg-doped CBL layer is excessive at high bias condition due to barrier lowering. Such leakage through CBL at high drain bias prevents the vertical HEMT being used in real-world device applications. Therefore, it will be an interesting study for us to make the vertical structure more reliable and practically applicable by integrating a new material for the CBL layer. Moreover, structural engineering of the vertical HEMT makes the current flow in the vertical direction (from source to drain) through the GaN bulk. Therefore, the resistance of the aperture plays a crucial role in the vertical device. The resistance of the

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aperture lowers the current in the vertical HEMT and, ultimately, degrades the device performance.

In this work, we introduce SiO_2 as current blocking layer for AlGaN/GaN vertical HEMT and explore the effect of SiO_2 CBL on electrical characteristic of the device. The comparatively larger band-gap of SiO_2 helps to reduce the vertical leakage current and make the device more robust even at high bias condition. Besides, the single aperture is replaced by multiple parallel apertures, under the same total width, to reduce the resistance of the aperture and, as a result, device current is increased.

2. The novel device structure, fabrication and simulation

Fig. 1 represents the detail of the epilayer grown and fabrication process of the proposed AlGaN/GaN SiO_2 CBL vertical HEMT structure. The entire structure, except SiO_2 CBL, is grown by metal oxide chemical vapour deposition (MOCVD) on a GaN substrate. Ammonia (NH_3), trimethylgallium (TMGa), and trimethylaluminum (TMAl) are used as precursors and hydrogen as carrier gas. Prior to growth, the substrates were treated in H_2 ambient at high temperature for about 10 min. After that, n-type doped GaN is grown on the GaN substrate at high temperature. Silane (SiH_4) is used as a source material for n-type doping. These steps are shown in Fig. 1(a) and (b). Then, the sample is moved out from MOCVD and 500 nm SiO_2 is deposited on GaN by plasma enhanced chemical vapour deposition (PECVD) under high temperature for 10 min in N_2 or O_2 ambient as shown in Fig. 1(c). A 0.8-μm-long SiO_2 corresponding area for the aperture is dry etched, as shown in Fig. 1(d). For multiple apertures the VHEMT, mask is patterned with four apertures of 0.2 μm by using electron-beam lithography [10]. Next, GaN is regrown from the GaN layer in the etched region by using a pendeo epitaxial method [11–13] and 50 nm n-type (3×10^{16}) GaN and 15 nm thick $Al_{0.25}Ga_{0.75}N$ is grown by using MOCVD. Regrown steps are shown in Fig. 1(e) and (f). The entire layer is grown at high temperature. The Ti/Al/Ni/Au multilayer metal is deposited as ohmic metal and is annealed in a rapid thermal annealing (RTA) system at 800 °C for 60 s in N_2 ambient. The drain electrode is deposited on the opposite plane of the source. Then, the TiN/Au gate metal is deposited as the gate electrode by a reactive sputtering method as shown in Fig. 1(g). Fig. 2(a), (b) and (c) are the schematic plots of the conventional p-GaN CBL vertical HEMT (denoted as Sample I), the proposed SiO_2 CBL single aperture vertical HEMT (Sample II), and SiO_2 CBL low resistance multiple aperture vertical HEMT (Sample III), respectively. For sample III, ICP etching is used.

The transport properties of conventional and proposed devices are numerically studied by performing two-dimensional (2D) device simulation. The simulation details could be found in our recent work [1,14,15]. Notably, performance of device mainly depends on the carriers' mobility which is affected by various types of scattering mechanism; such as, the phonon scattering, the alloy disorder scattering, the ionized impurities scattering, the dislocation scattering, and the dipole scattering. In our device simulation, the mobility model considers two parts; one is the low field mobility model and the other is the nitride specific high field dependent mobility model. For entire simulation, the studied gate length is 3 μm and gate width is 100 μm. The source-to-gate distance and the gate-to-drain distance are fixed at 1 μm. Overlapping of gate on CBL is 1.1 μm in both the sample I and sample II. For the sample III, the device is designed with four identical apertures with the total aperture lengths equal to the aperture length of the samples I and II. Therefore, the gate overlapping with CBL in Sample III is smaller than that in Sample I and Sample II.

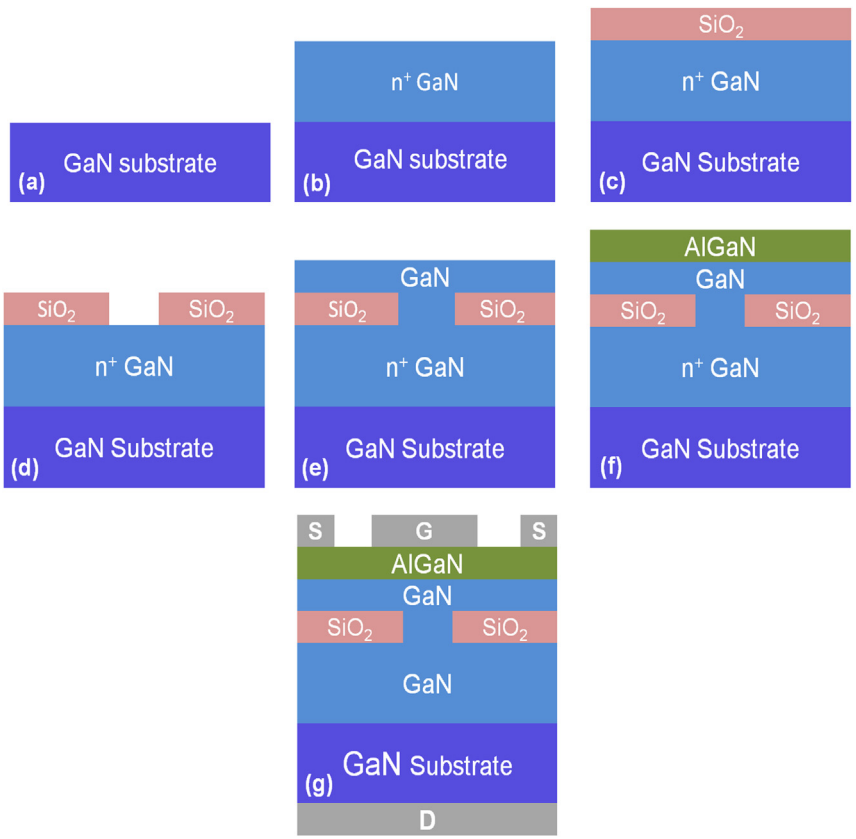

Fig. 1. Fabrication process for the proposed AlGaN/GaN vertical HEMTs with SiO_2 CBL.

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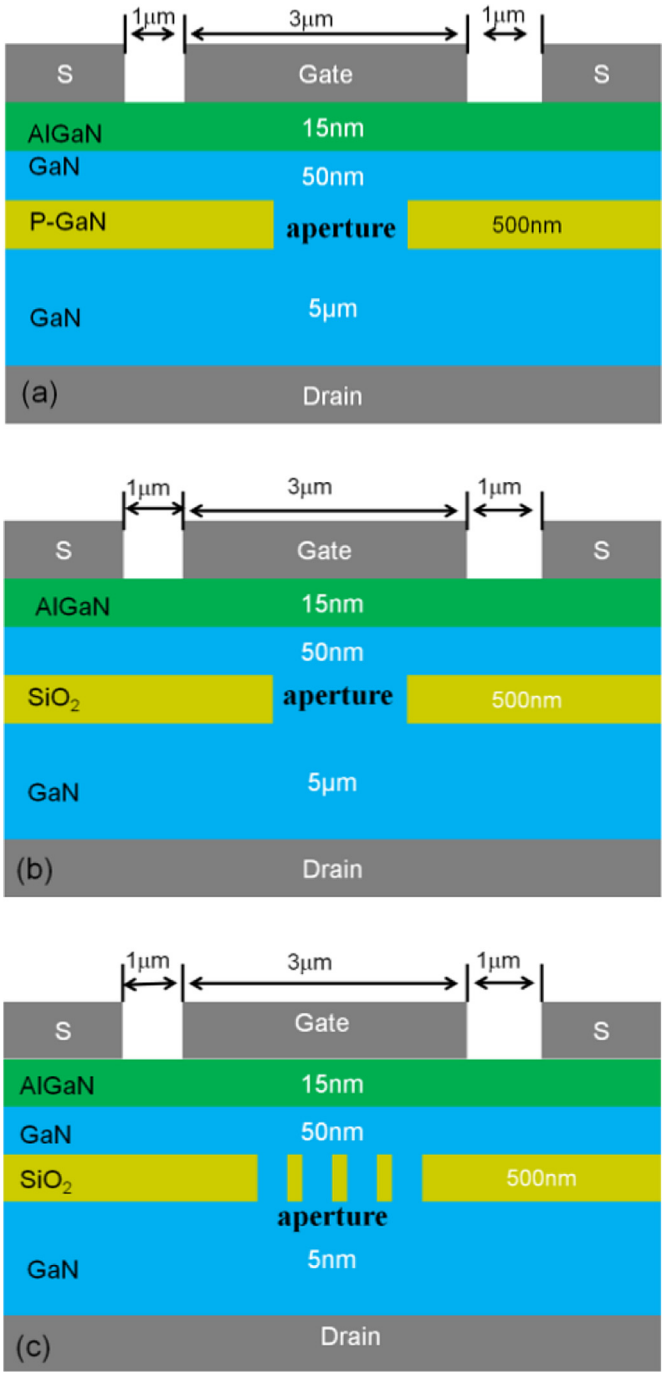

Fig. 2. Schematic plots of the explored vertical HEMT devices. (a) Conventional p-GaN CBL (Sample I). (b) Single aperture SiO_2 CBL (Sample II). (c) Multiple aperture SiO_2 CBL (Sample III).

3. Results and discussions

The I_D–V_G transfer characteristics of three types of AlGaN/GaN vertical HEMTs (Sample I, Sample II and Sample III) at drain bias of 1 V are plotted in Fig. 3. The simulation results demonstrate that drain current of the proposed SiO_2 CBL vertical HEMT is larger than that of the conventional p-GaN CBL vertical HEMT. In the conventional p-GaN CBL vertical HEMT, the p–n junction is formed between the p-GaN CBL layer and n-GaN channel. The effective channel of sample I is comparatively thinner than that of sample II even for equally thick channel layers due to formation of a

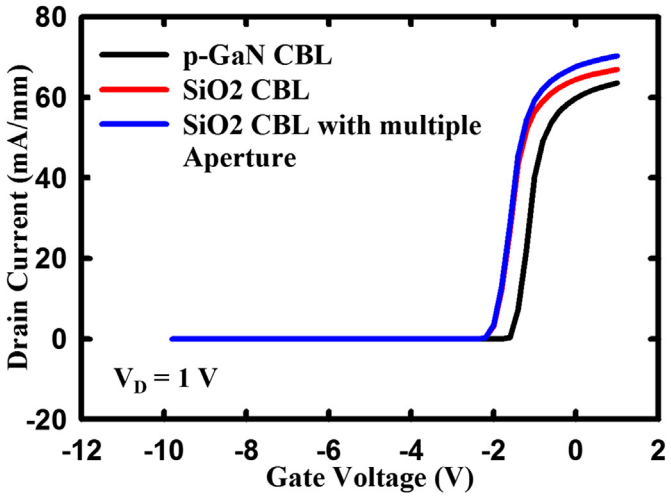

Fig. 3. Plot of I_D–V_G transfer curves of the explored three different vertical HEMTs, respectively.

depletion layer. The device with a thick channel layer has higher channel mobility, larger electron velocity and smaller R_{on} than the device with a thin channel layer [16]. Therefore, the sample II device has higher drain current than that of the sample I. The result of this study shows that drain current is increased by 7% in the sample II device, in comparison with sample I device. In contrast, there is a wider current path and a higher 2DEG density in the device sample II, resulting in a more negative threshold voltage [17]. It is observed in the 2D device simulation that the threshold voltage is shifted toward negative magnitude by 0.3 V.

The device sample III has four apertures with each aperture thickness equal to 0.2 μm and each aperture is separated by a 0.1-μm-thick SiO_2 layer. The total thickness of aperture in Sample III is the same as the aperture thickness of Sample II. We note that the effective CBL resistances are decreased when they are in parallel: $1/R_{eff} = \sum_{i=1}^{n} 1/R_i$. The calculated on-state resistance of the device sample III is 0.726 mΩ–cm^2, which is about 34% less than that of sample II, as shown in Table 1. The drain current of the parallel aperture SiO_2 CBL vertical HEMT (Sample III) is 8% larger than for the single aperture SiO_2 CBL vertical HEMT (Sample II), as shown in Fig. 3.

Energy band profile of the vertical HEMT with p-GaN and SiO_2 CBL layer at zero bias condition are plotted in Fig. 4(a) and (b). They show the barrier in SiO_2 CBL layer is higher than that of p-GaN CBL layer. The band-gap energy of the SiO_2 (8.9 eV) [18] is significantly larger than the band-gap energy of GaN. Fig. 4 shows that the barrier of the device sample II is two times larger than that of the device sample I at zero bias condition. Therefore, the confinement of carriers in the channel layer is more pronounced, the probability of vertical leakage through the CBL is significantly minimized and the drain current is comparatively higher. Our simulation result reveals that performance of the vertical HEMT at high drain bias is much more severe. The contour plots of the current flow are plotted in Fig. 5(a). There is excessive vertical leakage of current in the

Table 1
List of the estimated values of the breakdown voltage and drain current among the explored devices.

HEMT devices	Sample I	Sample II	Sample III
Drain current (mA/mm) at $V_D = 1$ V	63	67	71
Breakdown voltage	500 V	1260 V	1270 V
On resistance (mΩcm^2)	1.137	1.08	0.726

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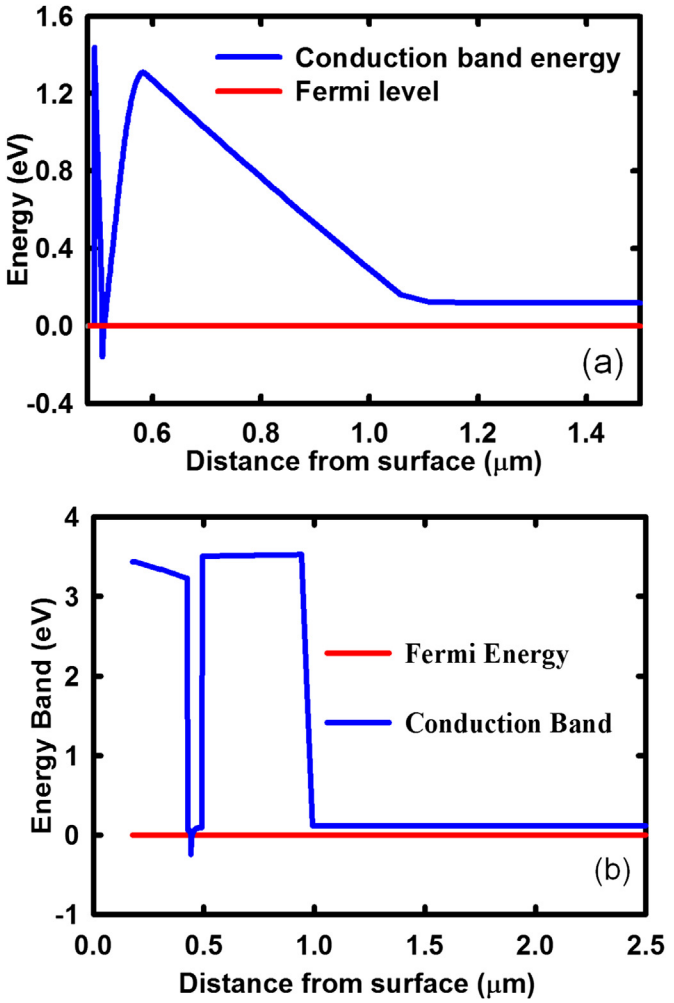

Fig. 4. Plot of the energy band profile of the vertical HEMT with (a) p-GaN CBL (b) SiO_2 CBL under unbiased condition.

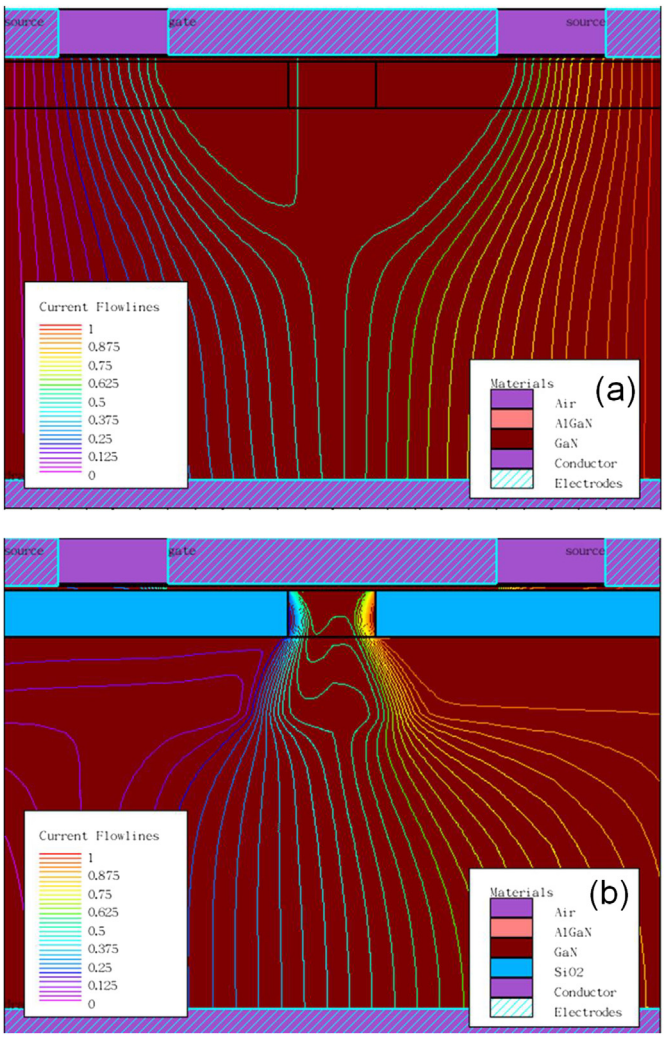

Fig. 5. Distributions of the simulated current flow of the vertical HEMTs with (a) p-GaN CBL (b) SiO_2 CBL at $V_G = -4$ V and $V_D = 50$ V.

device Sample I at high drain bias of 50 V. For the device sample II, the vertical leakage via CBL at high drain bias is effectively reduced, as shown in Fig. 5(b). This reveals that the vertical leakage could be comparatively controlled by using the SiO_2 CBL layer in the vertical HEMT at higher gate bias.

At high drain bias, the entire device temperature is increased; therefore, the barrier of p-GaN layer will be significantly diminished owing the inverse dependence of band-gap energy on the temperature, and the vertical leakage through CBL is pronounced. Fig. 5(b) shows that vertical leakage at higher drain bias is comparatively small in the vertical device with SiO_2 CBL. This is because the effective barrier of SiO_2 is higher than that of Sample I, at high bias condition. It can be effectively explained by the argument of conduction-band energy profile of the device at $V_G = -4$ V and $V_D = 50$ V, as shown in Fig. 6(a) and (b). The findings of this study strongly confirm that SiO_2 CBL can be a more effective technique for controlling vertical leakage at high drain bias.

The off-state output characteristic of the devices, as shown in Fig. 7, also explains the leakage suppression by using the SiO_2 CBL. Notably, the breakdown voltage has a physically inverse relation with respect to the off-state current [19] and, as a result, the off-state breakdown voltage is also effectively increased. The simulation results enable us to estimate the breakdown voltages for the sample I and sample II devices; they are 500 V and 1270 V, respectively. The magnitude of BV is increased by 154% on using the SiO_2 CBL in the studied AlGaN/GaN vertical HEMT. As shown in Fig. 7, the device sample III's BV is 1260 V. The difference of the off-state current and the breakdown voltage between Sample II and Sample III is very small. Listed in Table 1, we provide the estimated values of the breakdown voltage and drain current among the devices studied. Therefore, the design of multi-aperture vertical HEMT is promising for high power device technologies.

4. Conclusions

We have successfully designed and studied a novel GaN vertical HEMT with SiO_2 current blocking layer. Device fabrication steps were presented and the simulation results revealed that proposed device has superior performance than that with a p-GaN CB layer. The large band-gap energy of SiO_2 can help to create a high barrier layer and hence reduce the vertical leakage through CBL. The maximum drain current of Sample II is increased by almost 7%. Suppression of vertical leakage through the SiO_2 CBL at high drain bias can effectively reduce the off-state current and significantly enhance the breakdown voltage. The breakdown voltage of the proposed multiple aperture SiO_2 CBL vertical HEMT is 1260 V which is 152% higher than that of the conventional vertical HEMT (Sample I). In addition, the parallel multiple

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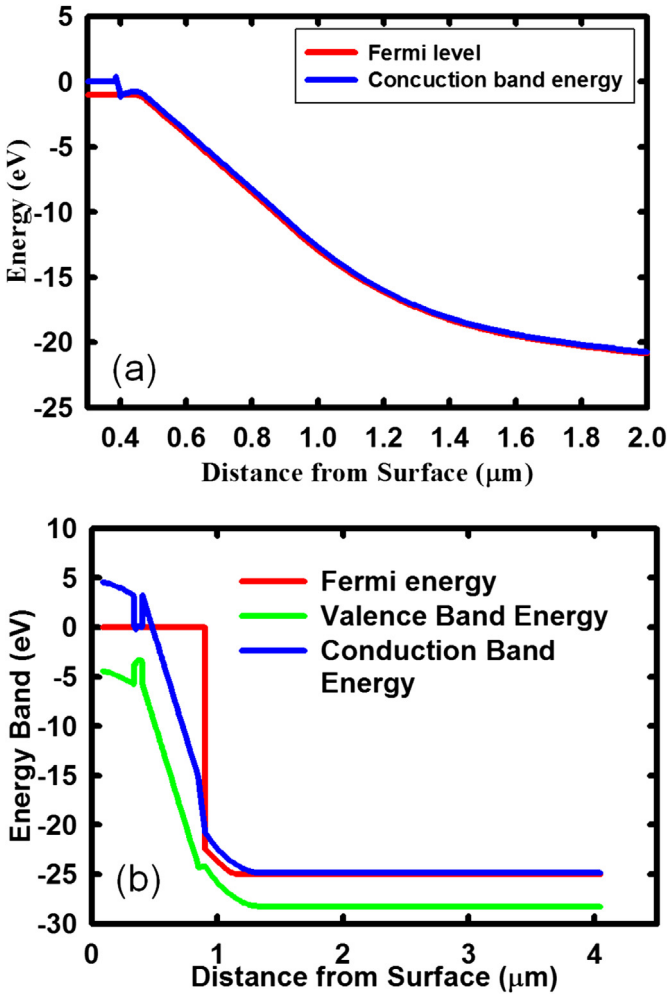

Fig. 6. Plot of the energy band profile of vertical HEMTs with (a) P-GaN CBL (b) SiO_2 CBL at $V_G = -4$ V and $V_D = 50$ V.

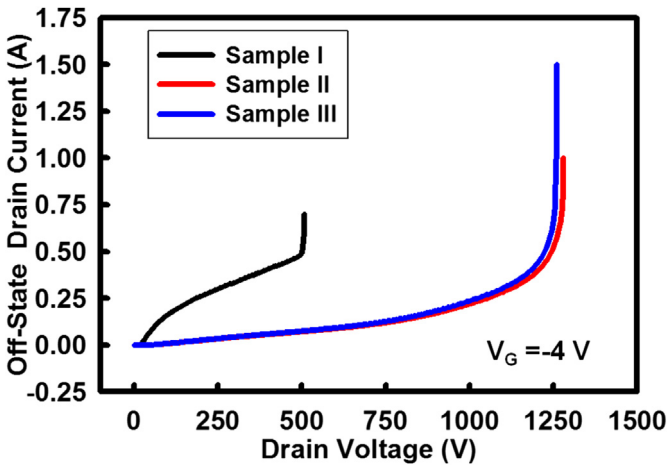

Fig. 7. The off-state drain current versus the drain voltage for the three different vertical HEMTs with p-GaN CBL and SiO_2 CBL with single and multi apertures, respectively.

apertures reduce the on-state resistance and increase the drain current. Comparatively low vertical leakage and high breakdown voltage with high drain current lead to the multiple aperture AlGaN/GaN vertical HEMT with SiO_2 current blocking layer a bona fide candidate for future high power application. Notably, the SiO_2 layer thickness helps to increase the breakdown voltage. Moreover, for the VHEMT with multiple apertures, the current density shows non-uniform distribution. For the apertures near electrodes, the device exhibits high current density. However, for the middle apertures the device's current density is low. We are currently studying the effect of SiO_2 layer thickness together with the sample fabrication.

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