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GAN –STRUCTURE AND FABRICATION TECHNIQUES- A COMPREHENSIVE REVIEW

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Abstract
HEMT (High Electron Mobility Transistor) Gallium Nitride (GaN), a heterostructure semiconductor with huge potential for fostering economic development in a silicon-based electronics industry, is currently facing growing production versus investment costs. The high intensity of the electric field and the mobility of electrons have previously demonstrated enormous potential for multi-gigahertz frequency communications and photonic applications at material level. Productivity developments on commercially viable wide area substrates are now at the marketing stage where GaN power conversion technologies are on the verge of available for market. The prospect to build on the research outlined here is very interesting in ways informed by unique problems emerging out of entirely advanced markets and applications. Hence, this series of innovation in GaN technology is not itself a road map, but a valuable set of state-of-the-art international GaN research that guides the next development process as market-driven needs evolve. Industrial companies make significant investments in a wide range of sector identifying the use of innovation in new circuit designs, packaging technologies and system level interfacing required to achieve and maximize the product benefits provided by GaN transistors. AlN / GaN MOS-HEMTs process layout is dealt with problems and challenges in the manufacturing process. The advanced technology is using Al_2O_3 thermally grown as a dielectric gate and system surface passivation. Significant improvement in system efficiency seen using Ohmic contact optimization and mesa sidewall passivation are elaborated. This paper describes and analyzes the DC and RF efficiency of the semiconductor switch and it is concluded that a GaN device with enhancement mode with a vertical structure is preferred as it has numerous advantages. These GaN devices are now employed in the field operating within power supplies and motor controls for industrial, commercial, and automotive applications, in addition to their recognition and reputation.

Keywords: Vertical and Lateral Structures of GaN, AlN/GaN MOS-HEMT, Ohmic Contact Resistance, Quadruple Gate GaN MOS-HEMT

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INTRODUCTION

Gallium nitride (GaN) is a substance that can be used in the manufacture of semiconductor power devices, as well as radio frequency (RF) modules and light emitting diodes (LEDs). GaN has demonstrated the ability to be the silicone semiconductor displacement technology in power conversion, RF, and analog applications. Power design engineers have been on a hunt for the perfect switch since the dawn of the electronics age over a hundred years ago, one that will quickly and efficiently turn raw electrical energy into a regulated, usable flow of electrons. The vacuum tube came first, but inefficiency, as shown by the heat they produce, and their large size and high cost, created limits to their maximum use. Then, the transistor gained widespread use in the late ' 50s with its small size and better efficiency, which quickly replaced tubes and thus generating vast new unattainable markets through vacuum tube technology.

The cost of manufacturing a GaN device is significantly lower than the cost of manufacturing a MOSFET device, because GaN devices are produced using normal silicone manufacturing methods in the same factories that currently produce conventional silicon semiconductors, and the resulting devices are much lower for the same functionality. Since the individual devices are much smaller than silicon devices, it is possible to produce many more GaN devices per wafer, creating a situation where GaN devices will always cost less to manufacture than their equivalents in silicone. The cost gap gets even wider as GaN technology improves.

GaN power devices originally developed based on a lateral configuration. Recent interest in vertical architectures has however grown. The advantages of this design include the capacity to attain high breakdown voltage and current rates without increasing the package size. This also ensures better efficiency in the peak electrical field resulting from the surface change to the majority of the network, and simplification of thermal control opposed to lateral systems. In acknowledgement of these characteristics, vertical GaN systems are the most probable rivals to combine currents exceeding 100 A with voltages exceeding 600 V, the standard specifications for several medium to high-power applications, such as electric cars and renewable energies. One of the problems facing vertical GaN power switches, like their lateral counterparts, is the realization of normal-off operations. Nonetheless many vertical devices need either p-type GaN or epitaxial regrowth. This isn't easy compared to n-type GaN, the p-type version has a higher acceptor activation ratio and much lower carrier mobility. And if epitaxial regrowth is needed this will escalate the complexity of manufacturing devices considerably[4].

High-electron mobility transistors (HEMTs) based on Gallium Nitride are appealing for high-temperature and high-power microwave applications owing to their attractive material properties, such as broad energy bandgap, high electron saturation speed and high AlGaN / GaN hetero-interface 2-D electron gas (2-DEG) density [1], [2]. Nonetheless, the RF output power supplied by AlGaN / GaN HEMTs is extremely compressed [9] by the dc-RF dispersion or current collapse.

Deep conditions on the polarized surface of the AlGaN barrier layer[3],[5],[7] and/or inside the semi-insulating (Al)GaN buffer[3],[4],[10],[11] are established as the two key sources of the current collapse. The SiNx[11]–[15] or AlN passivation[16]–[17] will effectively avoid the surface-state-induced current collapse. Although coping with buffer-related collapse is a challenging task because it is difficult to achieve growth in metal organic chemical vapor deposition (MOCVD) as a defect-free GaN buffer . Usually a hybrid AlGaN / GaN buffer alone typically has more defects than traditional GaN buffers. Besides the low-Al composition buffer technology, deep-level dopants like carbon and iron are often purposely inserted into the buffer to avoid buffer leakage and short

channel effects (SCEs)[18]–[22]. Consequently, the buffer's deep traps of the buffer will eventually affect 2-DEG output once electrons have charged them under a strong RF drain bias. In order to minimize the effect of buffer traps on the 2-DEG transport behaviour, a thin, accidentally doped, high-mobility GaN channel layer is normally developed on top of the semi-insulating GaN buffer, accompanied by an AlGaN barrier layer. There is however, a lack of comprehensive analysis of the results of this high-mobility GaN channel layer thickness on AlGaN / GaN HEMT's RF efficiency, in terms of both small and large-signal features. It is observed that AlGaN / GaN HEMTs with a thicker GaN channel layer manifest decreased small-signal RF efficiency, but significantly improved breakdown and high signal performance characteristics.

In this paper, section 2 deals with the review of different types of GaN and its fabrication technique that arises to a different features and advantages. Section 3 describes the different structures of GaN and its unique features by changing the original structure and moreover section 4 gives the comparison of GaN and gives the explanation whether the highlighted is efficient and user-friendly enough to deal with various applications and the conclusion for the paper is given in Section 5.

Types of GaN:

GaN transistors inherited the very same terminology as their counterparts in silicon: gate, drain and source. Furthermore, a GaN device's on-state resistance and breakdown voltage has a similar significance to their equivalents in silicon. On-state resistance curves ($R_{DS}(ON)$) versus voltage across gate-source curves are similar to MOSFETs in silicon. The on-state resistance temperature coefficient of GaN FETs is comparable to the MOSFET silicon as it is positive, but the value is comparatively low. GaN power devices' basic structure is divided primarily into two groups. One is the planar system manufactured on substrates of Si or Silicon Carbide (SiC). The other is the unit of vertical conduction produced by homoepitaxial. GaN can be classified based on structure as Lateral and Vertical; and based on mode of operation as depletion-mode and enhancement-mode.

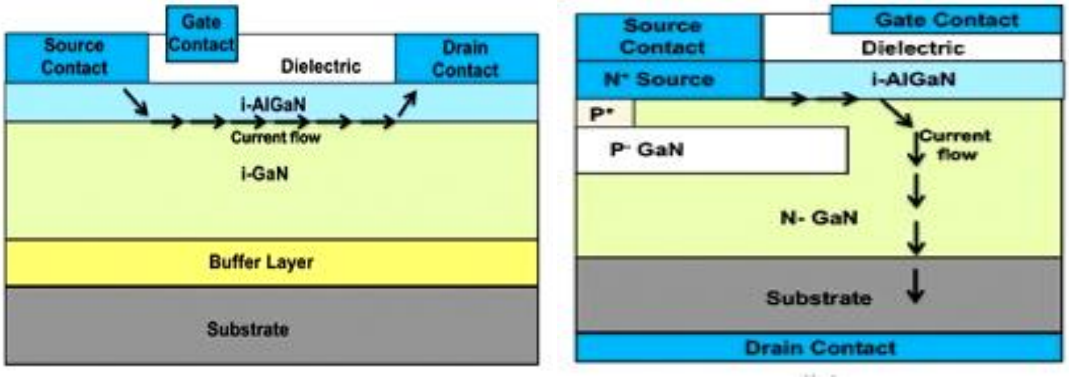
Classification based on structure:

GaN device is classified based on structure as Lateral and Vertical structure and are summarized as below:

The Lateral Structure of GaN devices: Over the past decade, Lateral power devices that rely on heterostructures from AlGaN / GaN achieved outstanding efficiency. Lateral GaN transistors shown in Fig.1(a) are now commercially available on Silicon substrates [33] with maximum operating voltage up to 650 V. In order to reach breakdown voltages above 1 kV, vertical GaN on-GaN diodes and transistors are being tested [34]. Although the lateral structures achieve good operating performance it has certain limitations as follows:

- The size of the lateral device increases dramatically as power increases.
- Requires large lateral dimension in proportion to voltage and current ratings.
- In high voltage applications, cautious management of electrical field profiles in the lateral dimension between contacts is needed. Significant lateral spacing of the gate / drain must be maintained to allow high voltage of breakdown, which decreases the effective current density.
- Thermal handling is made worse by the fact that all current flow is limited near the top surface to a relatively thin portion of the system.
- Such factors combined impede the cost-effective scaling to high voltage / current ratings of lateral devices.

By comparison, these limitations can be solved by a vertical GaN system. It is important to increase Safe operating Range [35] in order to allow higher output power, which is difficult with lateral system design.



(a) **(b)**

Fig.1. Conventional configuration of a GaN transistor: (a) Lateral architecture (b)Vertical architecture.

The Vertical Structure of GaN devices: In contrast to lateral design, a vertical GaN device architecture shown in Fig.1 (b) overcomes the limitations of lateral counterpart because high electric fields occur between contacts on the bottom and top of the structure in the vertical dimension only [36]. Vertical transistors will restrict the area of the device, as the increase in the voltage breakdown is only allowed by increasing the drift layer thickness as displayed in Fig.2. Development of vertical GaN transistors is a technological challenge for potential widespread use of GaN, because the Vertical system easily achieves high-current and high-voltage operations. A new vertical GaN transistor structure is suggested in which the p-type gate is built over the GaN drift layers' V-groove. The vertical system indicates low on-state average resistance of 1.0m Ω / cm^2 and high breakdown voltage of 1.7 kV [35] and it is revealed in Fig.3.

The following are the merits of Vertical GaN architecture.

- The ability to achieve high Safe operating Range with the same size of the chip;
- Easier thermal management
- Vertical GaN devices are most likely to combine currents above 100 A with voltages exceeding 600 V.
- Specific junction designing methods are used to control and form the electrical field at the edges of the devices in order to achieve high breakdown voltage. These include field plate, guard rings, termination of the bevel edge and extension of the end of the junction.
- This is preferable to lateral systems, where current flows near the surface in a 2D electron gas layer generated at the AlGaN / GaN interface [35].

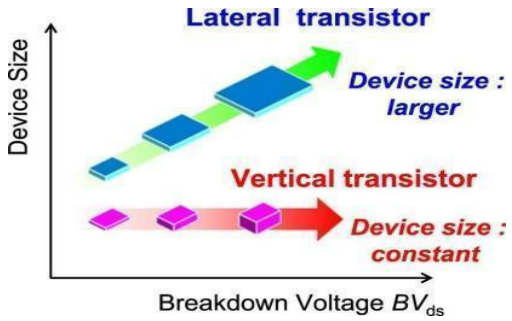
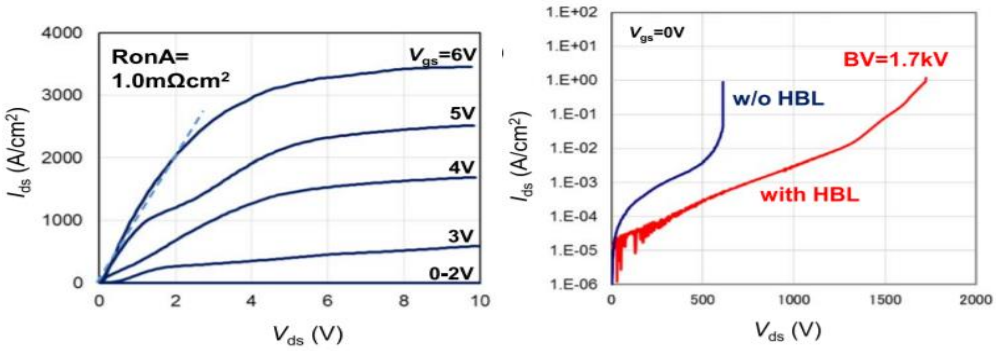


Fig. 2. Device size versus voltage breakdown: comparison of vertical and lateral transistors.



(a) **(b)**

Fig. 3. Output characteristics of the vertical GaN type (a) on-state and (b) off-state

Classification based on Mode of Operation:

(**a) Depletion mode of GaN devices:** The basic structure of a GaN transistor is depicted in Fig. 4. It has gate, source, and drain electrodes similar to power FET. The source and drain electrodes perforate via the upper layer of AlGaN to create an ohmic contact with the 2DEG that lies behind it. When the electrons 2DEG is vanished it makes an electrical circuit between source and drain, and the semi-insulating will obstruct the current flow. A gate electrode replenishes the 2DEG. This gate electrode is developed on many of the early GaN transistors as a Schottky contact to the upper surface. When applying a reverse potential to this gate the Schottky barrier becomes reverse biased and the electrons below are depleted. So turning this device OFF requires a reverse potential comparative to both drain and source electrodes. This kind of transistor is named Heterostructure Field Effect Transistors (HFET) depletion mode, or d- mode.

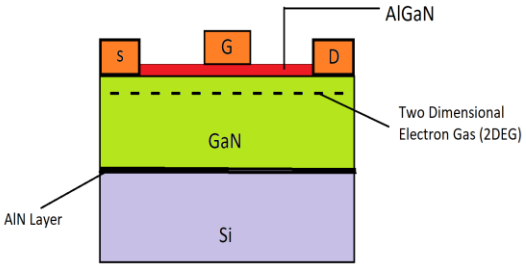


Fig 4. A typical AlGaN/GaN HFET

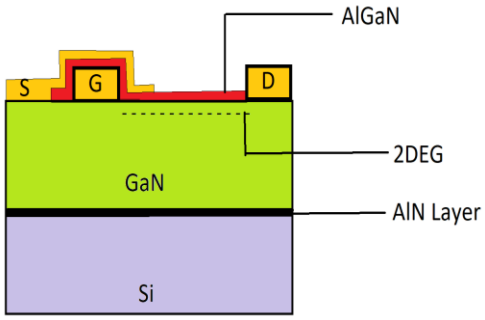


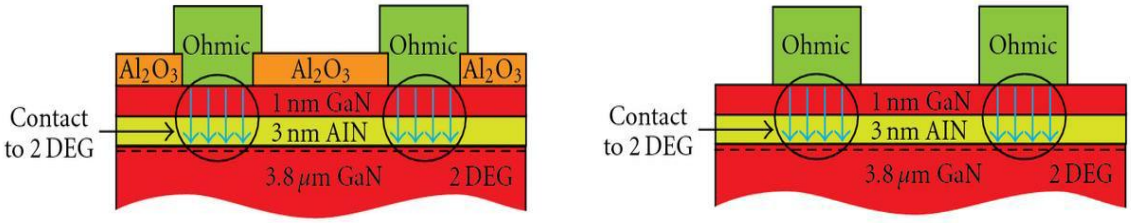
Fig 5. A typical Enhancement-mode GaN FET structure

(b) Enhancement-mode of GaN devices:A thin coating of Aluminium Nitride (AlN) is grown on the silicon to include a base surface for the eventual development of a heterostructure of GaN. On the AlN a heterostructure of Aluminium gallium

nitride (AlGaN) is formed and then GaN. This surface offers a base which creates the GaN FET. On the surface of the highly resistive GaN, a very small layer of AlGaN is grown. This thin layer produces a strained interface between surfaces of crystals GaN and AlGaN. A forward voltage is applied to the gate in the same way as switching on an n-channel, enhancement mode power MOSFET, to improve the FET. A cross-section of the structure is shown in Fig. 5. Extra metal layers are introduced to the electrons route into the gate, drain and source terminals.[38]

Fabrication Techniques in AlN/GaN – based systems:
Features of this material system are high concentrations of 2DEG sheet carrier at the heterojunction interface, high carrier electron speed and large variations of electrical breakdowns, thus attaining superior performance in comparison to AlGaN / GaN products. With advances in material growth and processing methods, good output in this device includes 2DEG sheet carrier concentration above 3 * 10^{13} cm^{-2} with relatively minimal sheet resistance, Rsh < 150 /mm, input drain current density above 2 A / mm and cut-off frequency above 100 GHz[5].

Ohmic Contact Optimisation:
Using less-resistance, thermally stabilized Ohmic contacts(OC) with good surface morphology gives optimal performance of AlN / GaN based HEMT systems.[31] This has been needed for the following facts: (1)obtaining the high drain current, (2) reducing on state-resistance, (3) minimizing power leakage in OC due to large current densities, and (4) obtaining the high external transconductance resulting in an increase in the current gain cut-off frequency, as well as the maximum operating frequency of the devices. For these facts, the processing of OC optimization in the AlN / GaN substance networks for HEMT and MOS-HEMT is essential for achieving better device efficiency. Descriptions of the optimization of the Ohmic touch method have been published in [23] and are summarized here.



(a) **(b)**

Fig 6: Optimized overview of TLM processing for AlN / GaN HEMT samples: (a)Vulnerable and unpassivate.(b) safe and passive.

OCs are fabricated and differentiated by AlN / GaN samples which are both shielded (primarily with an evaporated Al 2 nm later oxidized to form Al_2O_3) and non-protected / unsecured (as grown). Illustration. 6a explains the configured transmission line design methodology (TLM) for unprotected and non-passive AlN / GaN HEMT samples and Fig. 6b. shows a description of the configured AlN / GaN MOS-HEMT data sets for secure and passive TLM processing. A summary of the optimized RC and RSh standards on HEMT and MOS-HEMT is given in Table 1. The protected surface resistance of the sample is 159 range / mm, which is 1/3 of the unprotected sample (450 range / mm). On the side, the TLM tests of unprotected and unpassivated samples showed very low contact resistance with an average value of 0.31· mm. The below details gives an example to handle OC safely.

Table 1: Optimized tests and values in the AlN / GaN material structure for HEMT and MOS-HEMT applications.

Samples	Description	RC(Contact Resistance in Ω/·mm)	RSh(Sheet Resistance in Ω/mm)
A	Unsecured and unpassivated (HEMT)	0.310	480
B	Secured and passivated (MOS-HEMT)	0.490	159

TLM Processing for the system seen in Figure 6b involves optimizing wet etching using $16H_3PO_4$: HNO_3: $2H_2O$ Al etch solution which offers very less contact resistance and very little sheet resistance as described in[23]. Figure 7 shows the measured I-V characteristics on 5 µm TLM gap distance of annealed OC during different Al etch times before deposition of Ohmic metal. The sample B2's treatment systems, in which Al is etched to 20 secs, given the best I-V graph relative to other etching times. This sample 's average RC and RSh values are 0.49Ω / mm, and correspondingly 159 Ω/ mm. Nevertheless, it causes impact in the contact resistance if the sample is maintained longer in the etchant.

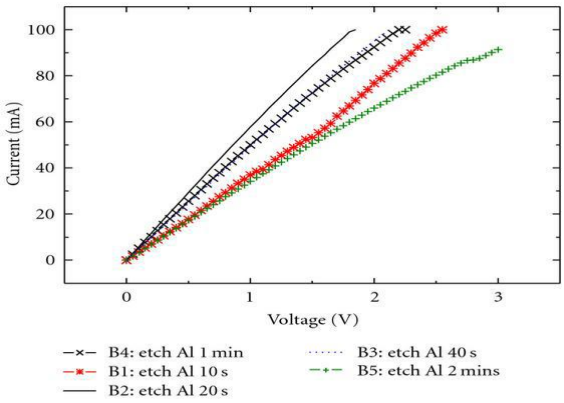


Fig.7 Current versus Voltage characteristics (5 m TLM gap spacing of annealed OC under various Al etch times prior deposition of Ohmic metal)

Gate Wrap-Around MOS-HEMT Optimisation

A method to gate wrap-around configuration [29], where the gate contact covers the drain as depicted in Figure 8, is utilized for process growth and optimisation on AlN/GaN HEMT structures. This method involves metallisation of the Ohmic and the gate, excluding the mesa-isolation process. During process growth, 10 mm x 10 mm of data sets cleaved from a 2 inch wafer are used. Production of the device starts with routine sample cleaning with deionized water, acetone and isopropanol. In Figure 6a, automated Ohmic contact processing is used for the production of unprotected and unpassivated AlN / GaN HEMT units. HCl: 4H2O solution is used for deoxidation before ohmic metal deposition in the OC areas. Ohmic metal contacts are created by evaporation of Ti / Al / Ni / Au, accompanied by a lifting-off step and then annealing at 800 ° C for 30 seconds. Gate metal links are then done by evaporation with Ni / Au followed by lifting-off.

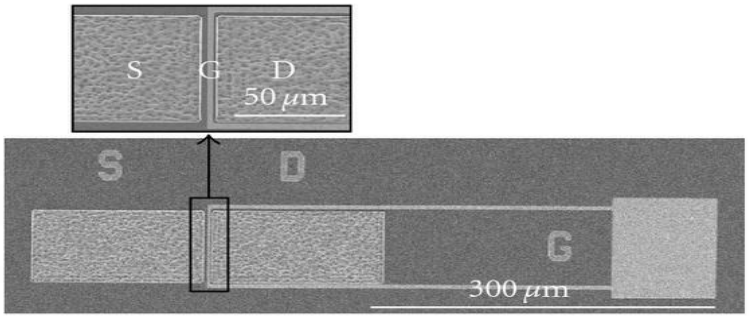
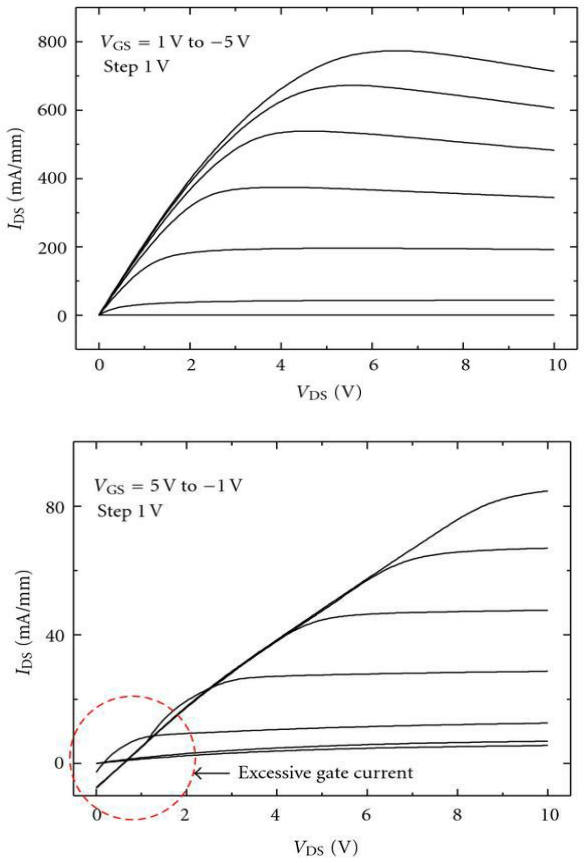


Fig 8: SEM gate wrap-around MOS-HEMT micrograph. Inset: µm device and µm device.

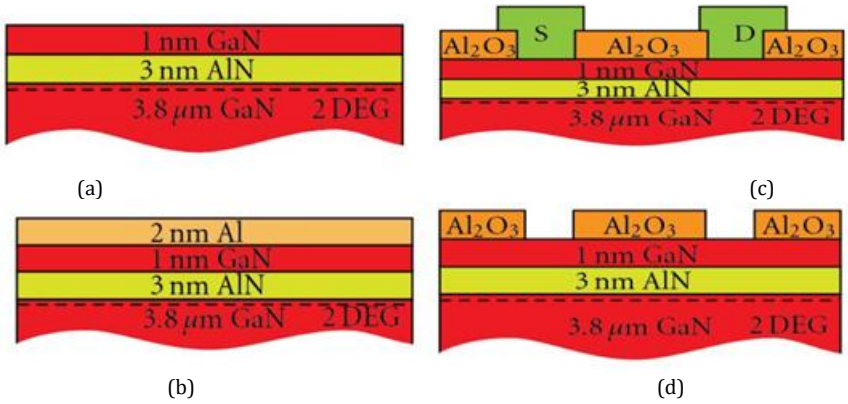
AlN / GaN structures are well understood to be very responsive to liquid treatment, so unsecured and unpassivated AlGaN / GaN HEMTs (from identical growth circumstances) are also handled and manufactured to provide reliable statistics. DC tests are carried out by placing the probe's needles just above source (S), drain (D), and gate (G) structures. Figure 9(a) illustrates the IDS -VDS characteristics of exposed and nonpassive 3 µm devices on the AlGaN / GaN HEMT structure. Devices built on this material system had strong gate regulation of drain currents up to 1 V gate bias and achieved a peak drain current of ~800 mA/mm. The devices also exhibited good pinch-off properties and good saturation. On the other hand, devices built on the AlN / GaN HEMT structure shown in Figure 9(b) showed very high leakage currents and did not pinchoff, and the drain current is very low.

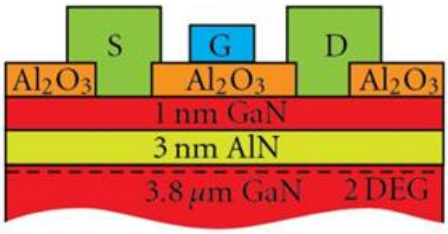


(a) (b)

Fig 9:-Characteristics of non-protected and non-passivated devices with 3 µm (a) AlGaN / GaN HEMT and (b) AlN / GaN HEMT.

These findings, along with the TLM findings detailed in the above chapters, indicate that there are certain issues with the processing of AlN / GaN HEMT structures not seen in AlGaN / GaN HEMTs. Exposure to multiple processing chemicals such as resist developer and solvent solutions may help to reduce OC resistance, and at the same time it may have led to the durability of AlN / GaN epilayer structures deteriorating. Study cited by Fan et al.[23] concerning the production of low OC on n-GaN materials, where reduced OC resistance is caused by damage to the RIE process used prior to depositing the OC metallisation. The devices however suffered from surface vulnerability and heavy leakage currents. Thus the epitaxial layers of AlN / GaN need to be covered during device processing. A new production process for AlN / GaN based devices is therefore developed which involves the use of Al2O3 thermally grown to protect the very sensitive AlN epilayer from exposure to liquid chemicals throughout the process[30] as stated earlier for TLM experiments (Figure 7). This Al2O3 produced by thermal oxidation Al evaporated, acts as a passive surface and a dielectric gate for the transistors.[32]





(e)

Fig 10: Process flow using the gate wrap-around technique to produce covered and passivated AlN / GaN MOS-HEMTs.

The processing includes (a) material cleaning and deoxidation, (b) 2 nm Al deposition, (c) Ohmic region etching and thermal oxidation, (d) ohmic metallisation and annealing, and (e) gate metallisation and unit calculation. To further investigate the impacts of OC optimization on device performance, devices are produced in the OC area using varying Al etching time. Fig.11 shows a typical characteristics of AlN / GaN MOS-HEMT devices produced from 3 µm to 100 µm doors, with different etching times, 10 secs and 20 seconds. The devices are biased from VGS =+3V to -4V with a phase size of 1 V. It is obvious that a 20 sec Al etch has a substantial effect on the output of the system with the drain current (IDS) at zero gate voltage greater than twice that of a system with 10 secs of etching time. Compared to similar findings on the very same epilayer structure for the AlN / GaN HEMT (unprotected and unpassivated system), these findings demonstrate that AlN / GaN MOS-HEMT with far greater and excellent transistor properties protects and passivates the AlN / GaN layers during production[23]-[28].

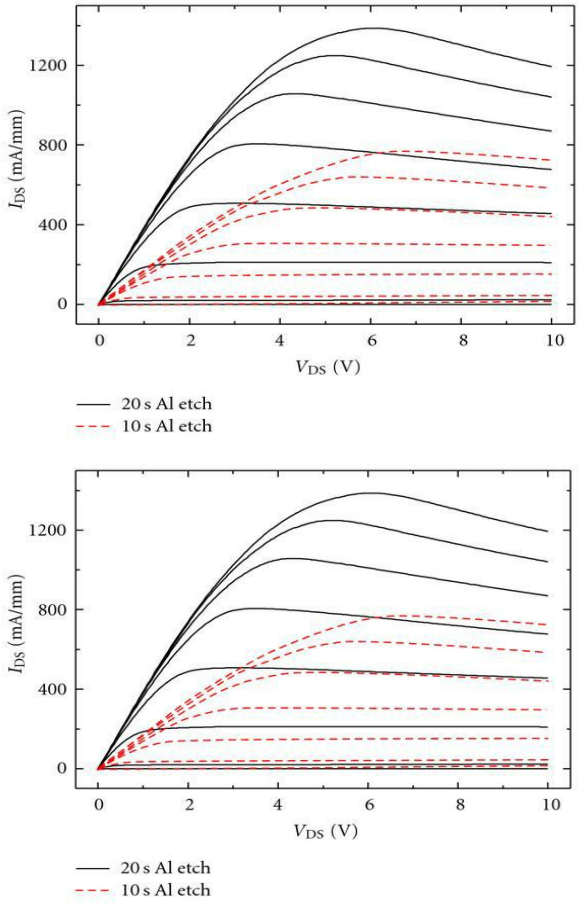


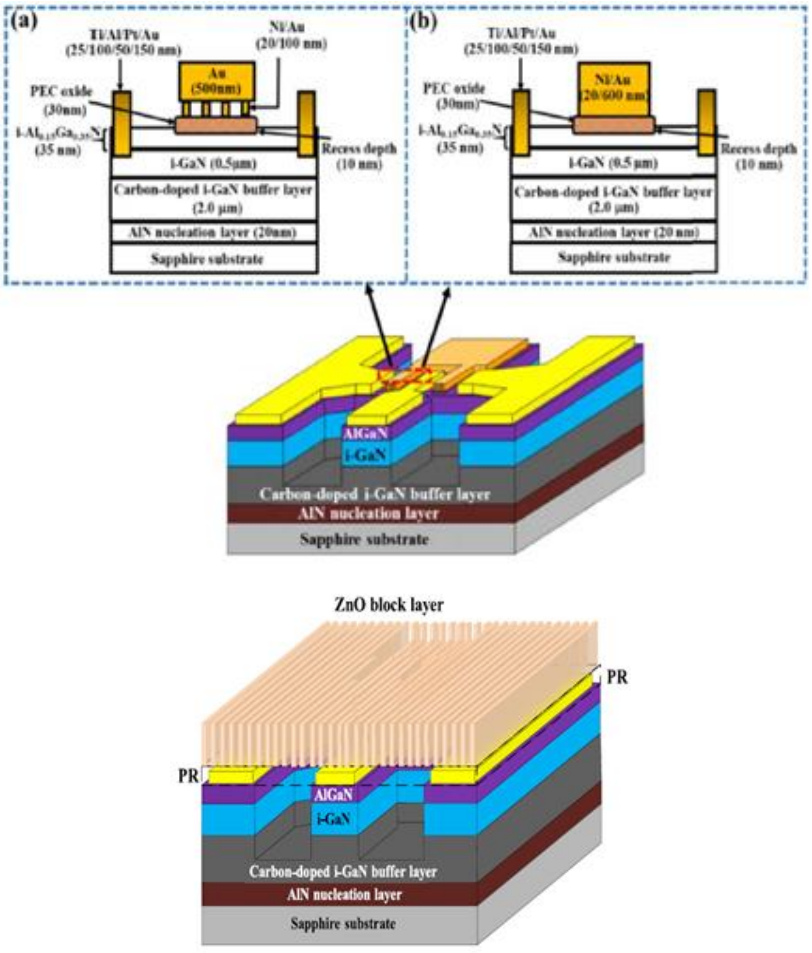
Fig 11: I_{DS} against V_{DS} characteristics of AlN/GaN MOS-HEMT devices with different etching times.

QUADRUPLE GATE (QG) GaN-MOSHEMT

Despite the development of epitaxial growth and production methods, gallium nitride (GaN)-based products are being commonly used in numerous electronic devices, optoelectronic devices, and sensors[47]-[49]. To maximize the effectiveness of GaN-based HEMTs, the modified gate size, the reduced gate-to-channel gap and the lowered parasite resistance and parasitic capacitance have been widely used[40]. By raising the parasitic capacitance of the top metal gate in the T-gate structure[40], the cut-off frequency of the unit gain will be decreased.[40]

Figure 12(a) and (b) demonstrate the QG-embedded T structured GaN-based MOSHEMT and standard GaN-based single gate MOSHEMT schematics. In this analysis, a molecular beam epitaxial ammonia system was used to sequentially grow a 20-nm-thick AlN nucleation surface, a 2.0-µm-thick carbon-doped I layer, an undoped 0.5-µm-thick layer I and an undoped 35nm-thick layer $Al_{0.15}Ga_{0.85}N$ on c-plane sapphire substrates. The BCl_3 etchant has been used to etch and render mesa

regions in a reactive ion etching system with a mesa insulation area of 310 µm/310 µm to generate mesa regions of standard single-gate GaN-based MOSHEMTs and QG-embedded T engineered GaN-based MOSHEMTs. Following the surface treatment process, the source and drain regions of GaN-based MOSHEMTs are modeled using a standard method of photolithography.



(a) (c)

Fig. 12: Schematic configuration: (a) QG-embedded T-structured GaN based MOSHEMTs and (b) Traditional single gate GaN based MOSHEMTs. (c) Stripped ZnO block layer on the devices.

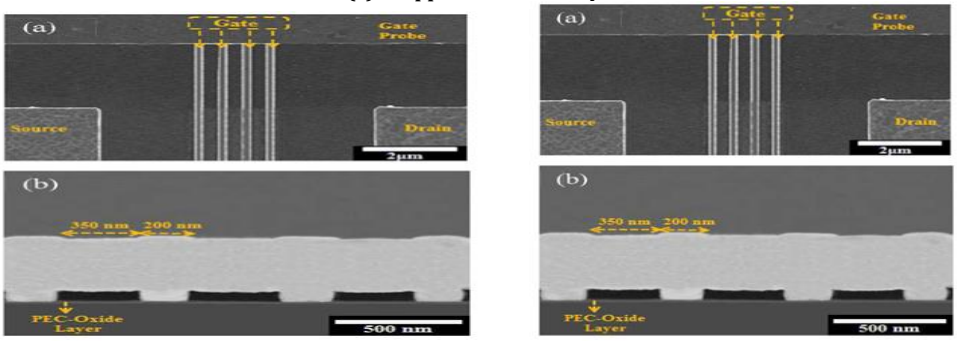
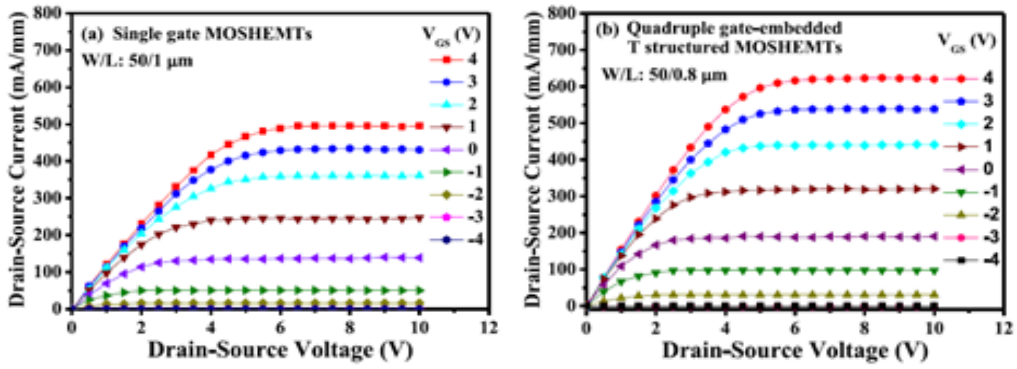


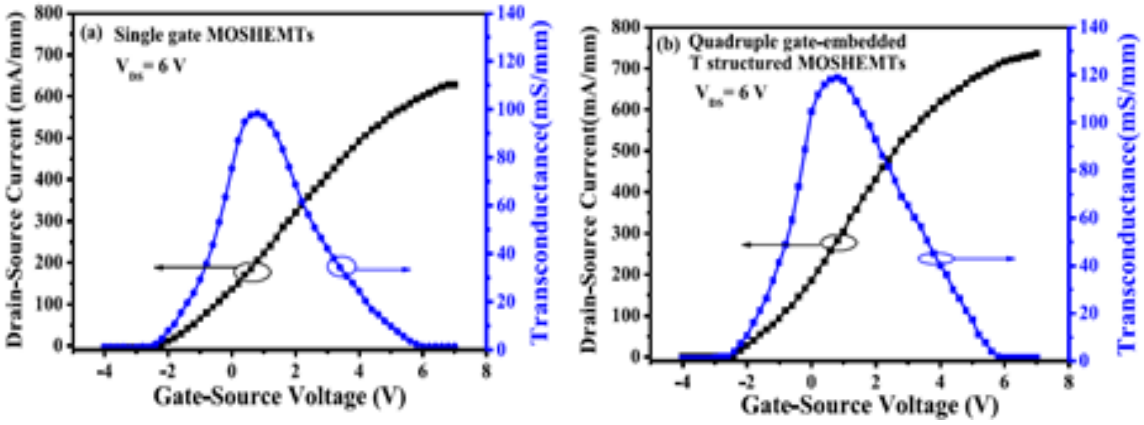
Fig 13: The SEM images: (a) Top view and (b) QG-embedded T cross section organized GaN based MOSHEMTs.

Figure 14(a) and (b) illustrates the drain-source current (IDS) dependence on the drain-source voltage (VDS) of traditional single-gate GaN-based MOHEMTs and four-gate-embedded T structured GaN-based MOSHEMTs operating at different gate-source voltages (VGS). The greater electron drift velocity and the screening effect in the QG-embedded T structured GaN-based MOSHEMTs may cause further enhancement of the drain-source saturation current. Figure 15 respectively (a) and (b), shows the reliance of the drain-source current and the extrinsic transconductance of traditional single-gate GaN-based MOSHEMTs on VGS and the QG-embedded T structured GaN-based MOSHEMTs operating at VDS = 6 V. The QG-embedded T structured GaN-based MOSHEMTs were produced using the photolithography process of laser interference, the process of photo-electrochemical oxidation and the sacrificial layer PMMA. The novel gate structure strengthened the DC efficiency of the consequent devices. The experiment results are discussed in [53].



(a) (b)

Figure 14: I_{DS} Vs V_{DS} Characteristics (a) Single gate GaN based MOSHEMTs and (b) QG-embedded T structured MOSHEMTs.



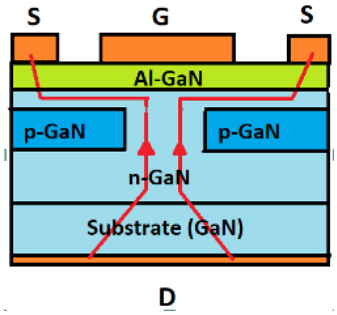
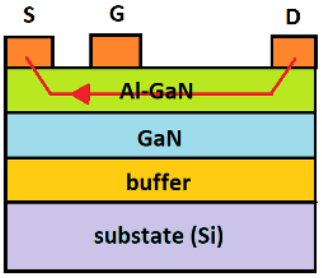
(a) (b)

Figure 15: I_{DS} Vs V_{GS} Characteristics (a) single gate GaN based MOSHEMTs and (b) QG-embedded T structured MOSHEMTs.

Comparisons of GaN :

In this section each model of GaN is compared with its counterpart and it is concluded with the suitable one regarding its advantages.

a) Comparison of Lateral and Vertical Structure of GaN:

	VERTICAL	LATERAL
Structure		
Cost	High	Lower
Speed	Relatively Higher	High
Main issue	Quality of substrates	Current Collapsing
Power	High (>10kW)	Intermediate (few kW)
Thermal management	Easier	Difficult
Size	Smaller	Bigger
Applications	Inverters	Bi-directional switches, High-frequency Converters.

An enhancement-mode GaN vertical fin power FET is explored with sub-micron channels (i.e. fins). A flat vertical finish profile is obtained by mixing dry / wet etch. The developed transistor had a resistance level of 0.36mΩ/cm² and a threshold voltage

of 1 V. A blocking voltage of 800V is accomplished by careful design of the peak electric field distribution. Such findings make this vertical GaN power transistor very appealing for implementations in high-voltage, high-current with low-cost and high-performance circuitry. The above observations are mentioned in [33].

b) Comparison of Depletion Mode and Enhancement Mode of Operation:

Depletion mode devices are inefficient in power converter applications, since a negative bias should first be given to the control devices when starting a control converter or a short circuit will occur. On the other hand, an enhancement mode system does not undergo this restriction. An enhancement-mode device is OFF with zero bias on the gate, and does not conduct current. Figure 16 shows a correlation of the performance characteristics between a depletion-mode and an enhancement-mode FET. Once the first industrial enhancement mode of gallium nitride FETs was introduced by Efficient Power Conversion Corporation it greatly reduced the level of complexity engineering power conversion systems with GaN transistors.

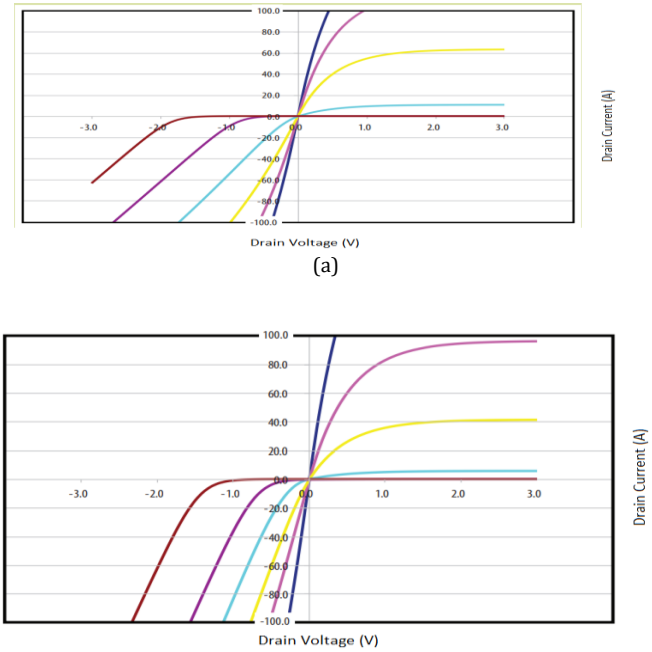


Fig 16. Comparison of performance characteristics of (a) Depletion-mode and (b) Enhancement-mode devices.

c) Comparison of AlN and AlGaN MOS-HEMTs:

The process technology developed has been expanded to incorporate AlN / GaN MOS-HEMTs using traditional system mesa insulation techniques. The method flow for the gate wrap-around devices are identical although with additional mesa isolation and the steps of the bond sheet. Figure 17(a) displays the completed 2- finger 2.5 µm gate length tool SEM micrograph top view. Figure 17 displays, respectively, the schematic cross-section of manufactured MOS-HEMT with (b) unpassive and (c) passive mesa sidewalls.

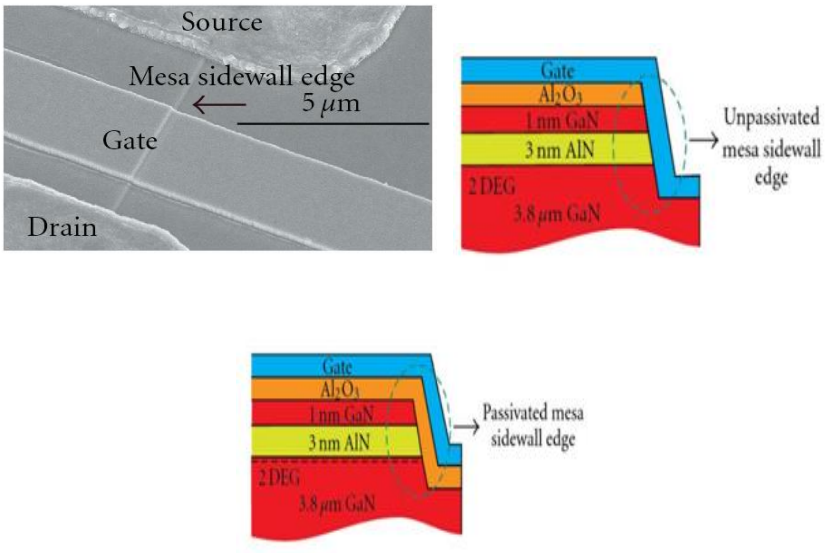


Figure 17: Cross-section schemes for manufactured MOS-HEMT (a) top-view SEM micrograph (for completed 2.5 µm gate length unit).(b)without mesa sidewalls edge passivation, (c) with mesa sidewalls edge passivation.

d) Comparison of QG MOS-HEMT with conventional MOS-HEMT :

Compared with traditional single-gate GaN-based MOSHEMTs, the drain-source saturation current increased from 125 mA / mm to 175 mA / mm, the breakdown voltage increased from −81 V to −92 V, the gate leakage current powered at a VGS of −80 V decreased from 7.6 μA to 0.81 μA, the maximum transconductance increased from 97.3 mS/81 μA.[53].

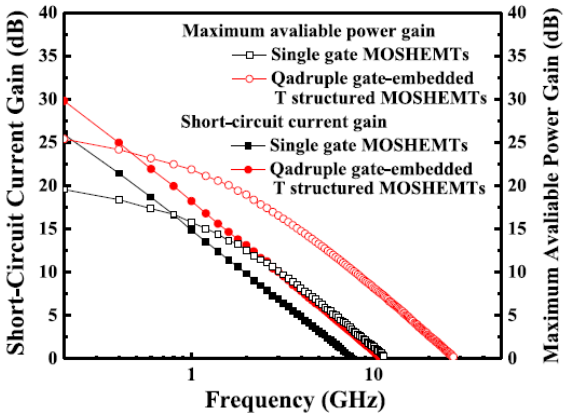


Figure 18: Short-circuit current gain Versus frequency characteristics of single gate MOSHEMT's and QG MOS-HEMT.

CONCLUSION

Power design engineers have been on a hunt for the perfect switch since the beginning of the electronics era over a hundred years ago, one that will quickly and efficiently turn raw electrical energy into a regulated, usable flow of electrons. GaN's potential to conduct electrons more than 1000 times more effectively than silicon, although now it has been well known that it can be generated at a reduced cost than silicon. This paper described numerous advantages and the reasons for using GaN devices. The different structures of GaN devices have been discussed. The fabrication process of AlGaN based HEMT devices has been conserved in this paper. Even a small change in the structural design (at a scale of micrometer) can have a drastic change in its electrical properties. The ideal choice of a GaN device can be the vertical structure, as the pros outweighs the cons of lateral structure. The enhancement-mode of operation is suitable for power electronic applications because of its easy control. Finally, the collected data on the latest GaN devices available, as mentioned in the paper, suggests that these transistors will fundamentally change the entire energy conversion industry because they provide consistent system enhancements by reducing the size and weight of the converters and increasing performance and power density. The novel QG-embedded T structure can be predicted as the suitable candidate for the structure in high performance semiconductor devices, as per the experimental results.

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