

# SYCL/DPC++ - And Introduction

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#### Table of contents

1. Introduction

2. Theory

3. Conclusion



# Introduction

# What programming model to use to target GPU?

- · OpenMP (pragma based)
- · CUDA<sup>1</sup> / Hip / OpenCL (low level)
- Kokkos, raja, OCCA (high level, abstraction layer, academic project)
- · SYCL (high level)

<sup>&</sup>lt;sup>1</sup>Compute Unified Device Architecture

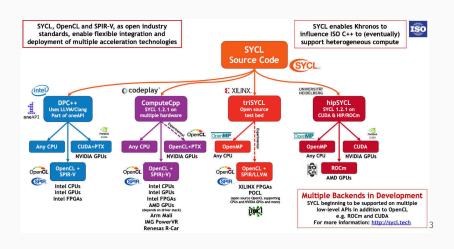
#### What is SYCL™?

- 1. Target C++ programmers (template, lambda)
  - · No language extension
  - No pragmas
  - · No attribute
- 2. Borrow lot of concept from battle tested OpenCL (platform, device, work-group, range)
- 3. Single Source (two compilation pass)
- 4. Implicit data-transfer
- SYCL is a Specification developed by the Khronos Group (OpenCL, SPIR, Vulkan, OpenGL)
  - The current stable SYCL specification is 1.2.
  - SYCL 2020 is expected to be approved at the end of the years<sup>2</sup>.

<sup>&</sup>lt;sup>2</sup>https://www.khronos.org/registry/SYCL/specs/sycl-2020-provisional.pdf



# SYCL Implementation



<sup>&</sup>lt;sup>3</sup>Credit: Khronos groups (https://www.khronos.org/sycl/)



#### What is DPCPP<sup>5</sup>?

- Intel implementation of SYCL<sup>4</sup>
- The name of the SYCL-aware Intel compiler

<sup>&</sup>lt;sup>5</sup>Data Parallel C++



<sup>&</sup>lt;sup>4</sup>Obvious from the name isn't it?

# **DPCPP** specialty

DPCPP implement the SYCL Standard + HPC extension

- Unified Shared Memory
- Reduction
- Magic introspection function
- · Explicit SIMD

Many of DPCPP extension are now merged in the new SYCL2020 standard!



#### DPCT: CUDA to DPCPP translator

- 1. This is **not** a CUDA to DPCPP compiler.
- 2. "Tool Assisted Porting"



#### oneMKL

oneMKL interfaces are an open-source implementation of the oneMKL Data Parallel C++ (DPC++) interface according to the oneMKL specification. It works with multiple devices (backends) using device-specific libraries underneath.

https://github.com/oneapi-src/oneMKL



# Vtunes / Advisor / iprof

- 1. Lot of profiler available.
- 2. Will trace monitor the underlying back-end calls

```
$ iprof ./4_buffer
Running on Intel(R) Gen12LP HD Graphics NEO
A[ 0 ] = 0

== OpenCL ==
API calls | 1 Hostnames | 1 Processes | 1 Threads

Name | Time | Time(%) | Calls | Average |
clBuildProgram | 112.49ms | 97.69% | 1 | 112.49ms |
clCreateBuffer | 1.50ms | 1.30% | 1 | 1.50ms |
clEnqueueNDRangeKernel | 584.20us | 0.51% | 1 | 584.20us |
Total | 115.15ms | 100.00% | 4 |
[...]
```



#### Goal of this talk

- 1. Give you a feel of SYCL/DPCPP so you know if it's maybe for you or not.
- 2. Tease you enough so you want to play with SYCL during the Hands-on<sup>6</sup>
- 3. Question are welcomed!

<sup>&</sup>lt;sup>6</sup>Or at least watch me going through some examples



# Theory

# First thing first: $\lambda$ !

Constructs a closure: an unnamed function object capable of capturing variables in scope.

#### Lambda Hello World<sup>7</sup>

```
int main() {
    //[] -> Capture; [=] capture by value, [&] capture by reference
    //() -> Parameter
4    //{} -> Body
5    [](){};
6    return 0;
7 }

1   void printVector(vector<int> v) {
    const offset = 0;
    // lambda expression to print vector
4    for_each(v.begin(), v.end(), [=](int i) {
        cout << offset + i << endl;
    });
7 }</pre>
```

<sup>&</sup>lt;sup>7</sup>Yes, it look like APL

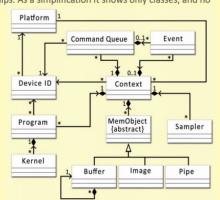


# A picture is worth a thousand words<sup>8</sup>

#### **OpenCL Class Diagram**

The figure below describes the OpenCL specification as a class diagram using the Unified Modeling Language<sup>1</sup> (UML) notation. The diagram shows both nodes and edges which are classes and their relationships. As a simplification it shows only classes, and no attributes or operations.

Annotations Relationships abstract classes {abstract} aggregations inheritance Δ relationship ^ navigability Cardinality many one and only one 1 0..1 optionally one 1.\* one or more



<sup>1</sup> Unified Modeling Language (http://www.uml.org/) is a trademark of Object Management Group (OMG).

<sup>&</sup>lt;sup>8</sup>and this is a UML diagram so maybe more!



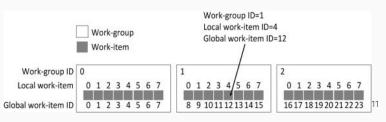
# Memory management: SYCL innovation

- 1. Buffers encapsulate your data
- 2. Accessors describe how you access those data
- 3. Buffer destruction will cause synchronization
  - Or you can also use Unified shared memory



# **Implicit Loop**

- A Kernel is invoked once for each work item <sup>9</sup>
- · local work size Work items are grouped into a work group 10
- The total number of all work items is specified by the global work size



<sup>&</sup>lt;sup>9</sup>similar to *MPI\_rank* 

<sup>&</sup>lt;sup>11</sup>Credit The OpenCL Programming Book by Fixstars

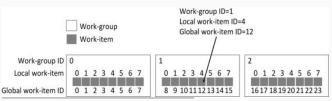


<sup>&</sup>lt;sup>10</sup>similar to *pragma omp simdlen/safelen* 

# Implicit Loop: Example!

```
global_work_size = 24; local_work_size = 8
SYCL / Opencl / CUDA
parallel_for<global_work_size,local_work_size>(mykernel);
OpenMP<sup>12</sup>
```

```
# wG = work_group; wC = work_item
for (wG_id=0; wG_id++; wG_id < (global_work_size / local_work_size)
for (local_wI_id=0; local_wI_id++; local_wI_id < local_work_size)
global_wI_id = local_wI_id + wG_id*local_wG_size</pre>
```



<sup>&</sup>lt;sup>12</sup>Using chunking / tilling / vectorization technique



#### SYCL Example

```
std::vector<int> A(global_range);
{
    sycl::buffer<sycl::cl_int, 1> bufferA(A.data(), A.size());
    sycl::queue myQueue;
    myQueue.submit([&](sycl::handler &cgh) {
        auto accessorA = bufferA.get_access<sycl::access::mode::write>(cgh);
        cgh.parallel_for<class hello_world>(
            sycl::range<1>(global_range),
        [=](sycl::id<1> idx) { accessorA[idx] = idx[0];}
    );
}
};
};
```



#### "Pro" tips

- 1. Queue creation are expensive. Try to reuse the queue<sup>13</sup>
- 2. The easiest way to achieved parallel execution of kernel, is to use mutiple queue.
- You need also to pass ID around, sometime it can be tedious. dpcpp provide an extension to emulate OpenCL get\_global\_id()

<sup>&</sup>lt;sup>13</sup>You already pass *mpi\_com\_world* around, just do the same things.



# Conclusion

#### Conclusion

- 1. For better or worth, SYCL is C++
- 2. Many vendors (Intel, Nvidia, AMD) and hardware (CPU, GPU, FPGA) supported
- 3. Implicit data-movement by default (Buffer / Accessors concepts)



# Lot of goods resources online

#### Spec

- 1. https://www.khronos.org/registry/SYCL/specs/ sycl-1.2.1.pdf
- 2. https://www.khronos.org/files/sycl/ sycl-121-reference-card.pdf

#### Examples

- 1. https://github.com/alcf-perfengr/sycltrain
- 2. https://github.com/codeplaysoftware/ computecpp-sdk/tree/master/samples
- https://github.com/jeffhammond/dpcpp-tutorial

#### **Documentations**

- 1. https://svcl.tech/
- 2. Mastering DPC++ for Programming of Heterogeneous Systems Argonne ♠ using C++ and SYCL (ISBN 978-1-4842-5574-2)

#### Q&A

Thanks you! Do you have any questions?

