

SYCL/DPC++ - An Introduction

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Table of contents

- 1. Introduction
- 2. DPCPP (and the associated ecosystem)
- 3. Theory
- 4. Conclusion



Goal of this talk

- 1. Give you a feel of SYCL/DPCPP
- 2. Tease you enough so you want to play with SYCL during the Hands-on¹
- 3. Question are welcomed!

¹Or at least watch me going through some examples... on Exclusive Hardware!



Introduction

What programming model to use to target GPU?

- Parallel STL
- · OpenMP (pragma based)
- · CUDA² / HIP³ / OpenCL⁴ (low level)
- Kokkos, raja, OCCA (high level, abstraction layer, academic project)
- · SYCL (high level) / DPCPP⁵

⁵Data Parallel C++



²Compute Unified Device Architecture

³Heterogeneous-Compute Interface

⁴Open Computing Language

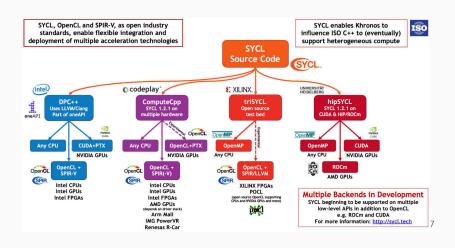
What is SYCL™?

- 1. Target C++ programmers (template, lambda)
 - · No language extension
 - No pragmas
 - · No attribute
- 2. Borrow lot of concept from battle tested OpenCL (platform, device, work-group, range)
- 3. Single Source (two compilation pass)
- 4. Implicit data-transfer
- SYCL is a Specification developed by the Khronos Group (OpenCL, SPIR, Vulkan, OpenGL)
 - The current stable SYCL specification is 1.2.
- SYCL 2020 is expected to be approved at the end of the years⁶.

⁶https://www.khronos.org/registry/SYCL/specs/sycl-2020-provisional.pdf



SYCL Implementation



⁷Credit: Khronos groups (https://www.khronos.org/sycl/)



What is DPCPP¹⁰?

- Intel implementation of SYCL⁸
- The name of the SYCL-aware Intel compiler9

¹⁰ Data Parallel C++: https://github.com/intel/llvm/releases



⁸Obvious from the name isn't it?

⁹So you don't need to pass *-fsycl*

DPCPP (and the associated ecosystem)

DPCPP a high potential SYCL implementation

DPCPP implement the SYCL Standard + extension¹¹

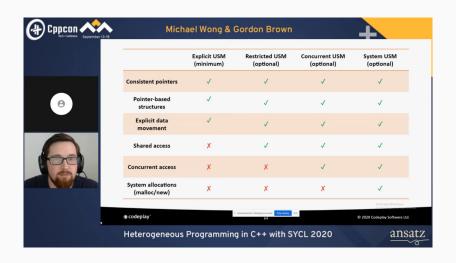
- · Unnamed Lambda
- · Unified Shared Memory
- Reduction
- Magic introspection function
- Explicit SIMD

Many of DPCPP extension are now merged in the new SYCL2020 standard!

¹¹https://github.com/intel/llvm/tree/sycl/sycl/doc/extensions



A note on USM





Interoperability

- · SYCL2020: with Native programming model (OpenCL, Cuda, ...)
 - · Creating sycl Buffer with cl_men
 - · Creating sycl Kernel from Opencl Kernel
- DPCPP: With OpenMP. Not yet memory compatibly. But on the pipeline¹²

//software.intel.com/content/www/us/en/develop/documentation/
oneapi-programming-guide/top/software-development-process/
composability/c-c-openmp-and-dpc-composability.html



¹² https:

DPCT: CUDA to DPCPP translator¹⁴

- 1. This is not a CUDA to DPCPP source to source compiler¹³.
- 2. "Tool Assisted Porting", not part of th
- 3. module load dpct ON JLSE

//software.intel.com/content/www/us/en/develop/documentation/
oneapi-programming-guide/top/software-development-process/
migrating-code-to-dpc/migrating-from-cuda-to-dpc.html



¹³It's a little more complex than a perl script

¹⁴https:

oneMKL¹⁵

oneMKL interfaces are an open-source implementation of the oneMKL Data Parallel C++ (DPC++) interface according to the oneMKL specification. It works with multiple devices (backends) using device-specific libraries underneath.

https://github.com/oneapi-src/oneMKL

¹⁵https://software.intel.com/content/www/us/en/develop/tools/oneapi/components/onemkl.html



Vtunes / Advisor / iprof

- 1. Lot of profiler available ¹⁶.
- 2. Will trace the underlying back-end calls

```
$ iprof ./4_buffer
Running on Intel(R) Gen12LP HD Graphics NEO
A[ 0 ] = 0
== OpenCL ==
API calls | 1 Hostnames | 1 Processes | 1 Threads

Name | Time | Time(%) | Calls | Average |
clBuildProgram | 112.49ms | 97.69% | 1 | 112.49ms |
clCreateBuffer | 1.50ms | 1.30% | 1 | 1.50ms |
clEnqueueNDRangeKernel | 584.20us | 0.51% | 1 | 584.20us |
Total | 115.15ms | 100.00% | 4 |
```

[...]

¹⁶For iprof *module load iprof*



Theory

First thing first: λ !

Constructs a closure: an unnamed function object capable of capturing variables in scope.

Lambda Hello World¹⁷

```
int main() {
    //[] -> Capture; [=] capture by value, [&] capture by reference
    //() -> Parameter
    //{} -> Body
    [](){};
    return 0;
    }

void printVector(vector<int> v) {
    const offset = 0;
    // lambda expression to print vector
    for_each(v.begin(), v.end(), [=](int i) {
        cout << offset + i << endl;
    });
}</pre>
```

¹⁷Yes, it look like APL

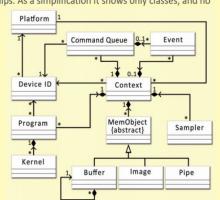


A picture is worth a thousand words¹⁸

OpenCL Class Diagram

The figure below describes the OpenCL specification as a class diagram using the Unified Modeling Language¹ (UML) notation. The diagram shows both nodes and edges which are classes and their relationships. As a simplification it shows only classes, and no

attributes or operations. Annotations Relationships abstract classes {abstract} aggregations inheritance Δ relationship ^ navigability Cardinality many one and only one 1 0..1 optionally one 1.* one or more



¹ Unified Modeling Language (http://www.uml.org/) is a trademark of Object Management Group (OMG).

¹⁸and this is a UML diagram so maybe more!



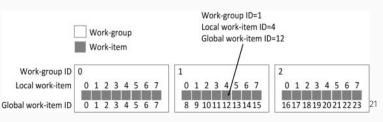
Memory management: SYCL innovation

- 1. Buffers encapsulate your data
- 2. Accessors describe how you access those data
- 3. Buffer destruction will cause synchronization
 - Or you can also use Unified shared memory



Implicit Loop

- A Kernel is invoked once for each work item ¹⁹
- · local work size Work items are grouped into a work group 20
- The total number of all work items is specified by the global work size



¹⁹similar to *MPI_rank*

²¹Credit The OpenCL Programming Book by Fixstars



²⁰similar to *pragma omp simdlen/safelen*

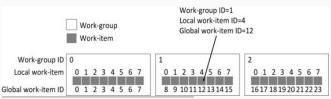
Implicit Loop: Example!

```
global_work_size = 24 ; local_work_size = 8
SYCL / Opencl / CUDA
```

parallel_for<global_work_size,local_work_size>(mykernel);

OpenMP²²

```
# wG = work_group; wC = work_item
for (wG_id=0; wG_id++; wG_id < (global_work_size / local_work_size)
for (local_wI_id=0; local_wI_id++; local_wI_id < local_work_size)
global_wI_id = local_wI_id + wG_id*local_wG_size</pre>
```



²²Using chunking / tilling / vectorization technique



SYCL Example

```
std::vector<int> A(global_range);
{
    sycl::buffer<sycl::cl_int, 1> bufferA(A.data(), A.size());
    sycl::queue myQueue;
    myQueue.submit([&](sycl::handler &cgh) {
        auto accessorA = bufferA.get_access<sycl::access::mode::write>(cgh);
        cgh.parallel_for<class hello_world>(
            sycl::range<1>(global_range),
        [=](sycl::id<1> idx) { accessorA[idx] = idx[0];}
    );
}
};
};
```



Teasing: SYCL Explicit SIMD Example

```
q.submit([&](handler &cgh) {
          auto PA = bufa.get access<access::mode::read>(cgh);
          auto PB = bufb.get_access<access::mode::read>(cgh);
          auto PC = bufc.get access<access::mode::write>(cgh);
          cgh.parallel for<class Test>(
5
              GlobalRange * LocalRange, [=](id<1> i) SYCL_ESIMD_KERNEL {
                 using namespace sycl::INTEL::gpu;
                 unsigned int offset = i * VL * sizeof(float);
                 simd<float, VL> va = block load<float, VL>(PA, offset);
                 simd<float, VL> vb = block load<float, VL>(PB, offset);
10
                 simd<float, VL> vc = va + vb;
11
                block store(PC, offset, vc);
12
              });
13
        }):
14
```



"Pro" tips

- 1. Queue creation are expensive. Try to reuse the gueue²³
- 2. The easiest way to achieved parallel execution of kernel, is to use mutiple queue.
- You need also to pass ID around, sometime it can be tedious. dpcpp provide an extension to emulate OpenCL get_global_id()
- 4. Use compatibility and USM to ease the porting

²³You already pass *mpi_com_world* around, just do the same things.



Conclusion

Conclusion

- 1. For better or worth, SYCL is C++
- 2. Many vendors (Intel, Nvidia, AMD) and hardware (CPU, GPU, FPGA) supported
- 3. Implicit data-movement by default (Buffer / Accessors concepts)



Lot of goods resources online

1.2.1 Spec

- 1. https://www.khronos.org/registry/SYCL/specs/ sycl-1.2.1.pdf
- 2. https://www.khronos.org/files/sycl/ sycl-121-reference-card.pdf

Examples

- 1. https://github.com/alcf-perfengr/sycltrain
- 2. https://github.com/codeplaysoftware/ computecpp-sdk/tree/master/samples
- https://github.com/jeffhammond/dpcpp-tutorial

Documentations (oneline and books)

- 1. https://svcl.tech/
- 2. Mastering DPC++ for Programming of Heterogeneous Systems Argonne using C++ and SYCL (ISBN 978-1-4842-5574-2)

Q&A

Thank you! Do you have any questions?

