

# NTB5860NL, NTP5860NL, NVB5860NL

## N-Channel Power MOSFET

### 60 V, 220 A, 3.0 mΩ

#### Features

- Low  $R_{DS(on)}$
- High Current Capability
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant
- NVB Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	60	V
Gate-to-Source Voltage – Continuous			$V_{GS}$	$\pm 20$	V
Continuous Drain Current, $R_{\theta JC}$	Steady State	$T_A = 25^{\circ}\text{C}$	$I_D$	220	A
		$T_A = 100^{\circ}\text{C}$		156	
Power Dissipation, $R_{\theta JC}$	Steady State	$T_A = 25^{\circ}\text{C}$	$P_D$	283	W
Pulsed Drain Current	$t_p = 10\ \mu\text{s}$		$I_{DM}$	660	A
Current Limited by Package			$I_{DMmax}$	130	A
Operating and Storage Temperature Range			$T_J, T_{stg}$	-55 to +175	$^{\circ}\text{C}$
Source Current (Body Diode)			$I_S$	130	A
Single Pulse Drain-to-Source Avalanche Energy ( $L = 0.3\ \text{mH}$ )			$E_{AS}$	735	mJ
Lead Temperature for Soldering Purposes (1/8" from Case for 10 Seconds)			$T_L$	260	$^{\circ}\text{C}$

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State	$R_{\theta JC}$	0.53	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	28	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

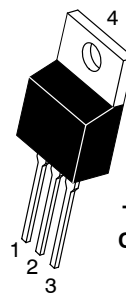
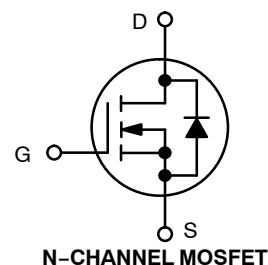
1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).



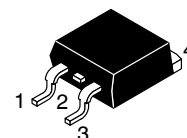
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	3.0 mΩ @ 10 V	220 A
	3.6 mΩ @ 4.5 V	

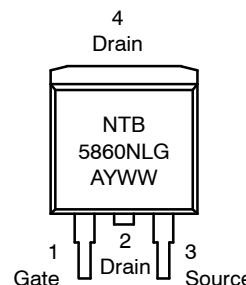
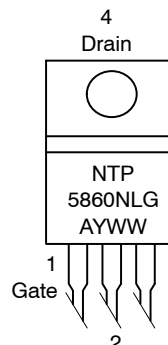


TO-220AB  
CASE 221A  
STYLE 5



D<sup>2</sup>PAK  
CASE 418B  
STYLE 2

#### MARKING DIAGRAMS & PIN ASSIGNMENTS



G = Pb-Free Device  
 A = Assembly Location  
 Y = Year  
 WW = Work Week

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTB5860NL, NTP5860NL, NVB5860NL

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ Unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
-----------------	--------	----------------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		6.1		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$ $V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ $V_{DS} = 60\text{ V}$	$T_J = 125^\circ\text{C}$		100	
Gate-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.0		3.0	V
Threshold Temperature Coefficient	$V_{GS(th)}/T_J$			-7.7		mV/°C
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		2.4	3.0	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		2.8	3.6	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		47		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{iss}$	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		13216		pF
Output Capacitance	$C_{oss}$			1127		
Transfer Capacitance	$C_{rss}$			752		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V},$ $I_D = 40\text{ A}$		220		nC
Threshold Gate Charge	$Q_{G(TH)}$			13		
Gate-to-Source Charge	$Q_{GS}$			37		
Gate-to-Drain Charge	$Q_{GD}$			54		

### SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DD} = 48\text{ V},$ $I_D = 100\text{ A}, R_G = 2.5\text{ }\Omega$		25		ns
Rise Time	$t_r$			58		
Turn-Off Delay Time	$t_{d(off)}$			98		
Fall Time	$t_f$			144		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}$ $I_S = 40\text{ A}$	$T_J = 25^\circ\text{C}$		0.76	1.1	$V_{dc}$
			$T_J = 125^\circ\text{C}$		0.60		
Reverse Recovery Time	$t_{rr}$	$V_{GS} = 0\text{ V}, I_S = 100\text{ A},$ $dI_S/dt = 20\text{ A}/\mu\text{s}$			50		ns
Charge Time	$t_a$				25		
Discharge Time	$t_b$				25		
Reverse Recovery Stored Charge	$Q_{RR}$				71		nC

2. Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

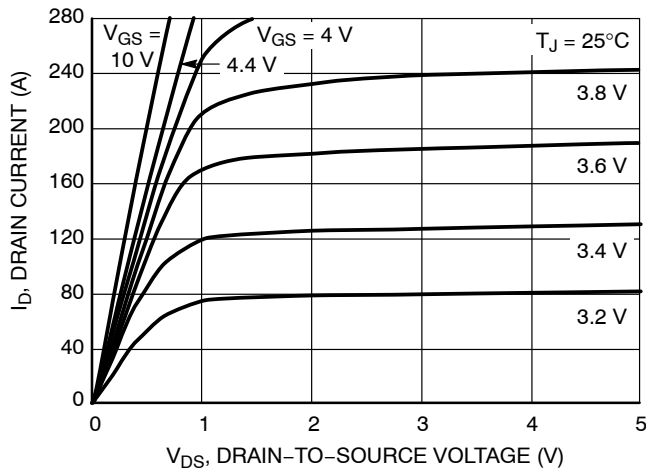


Figure 1. On-Region Characteristics

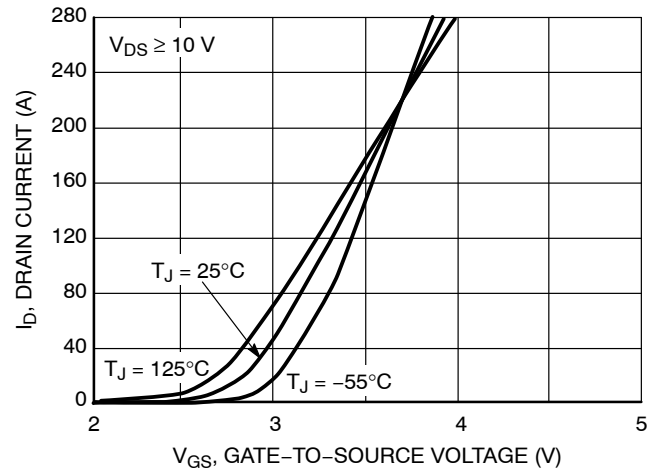


Figure 2. Transfer Characteristics

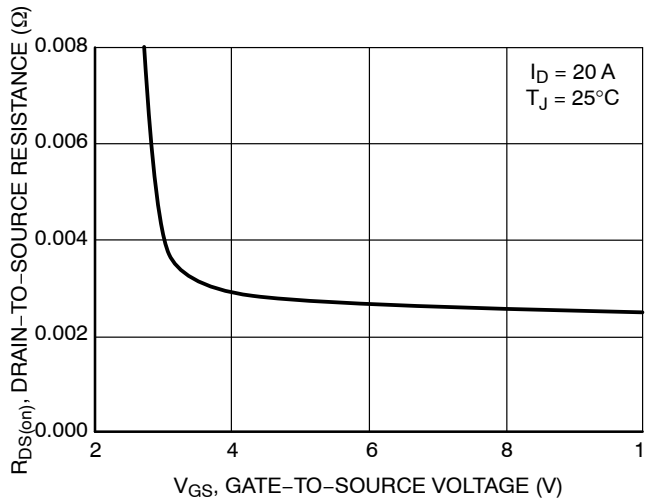


Figure 3. On-Resistance vs. Gate Voltage

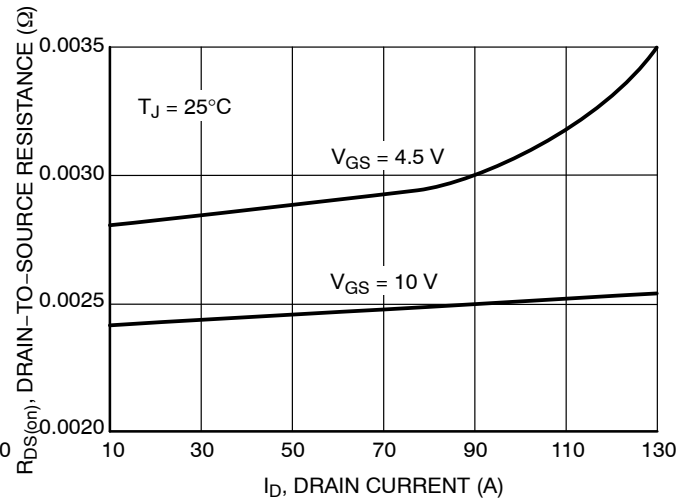


Figure 4. On-Resistance vs. Drain Current

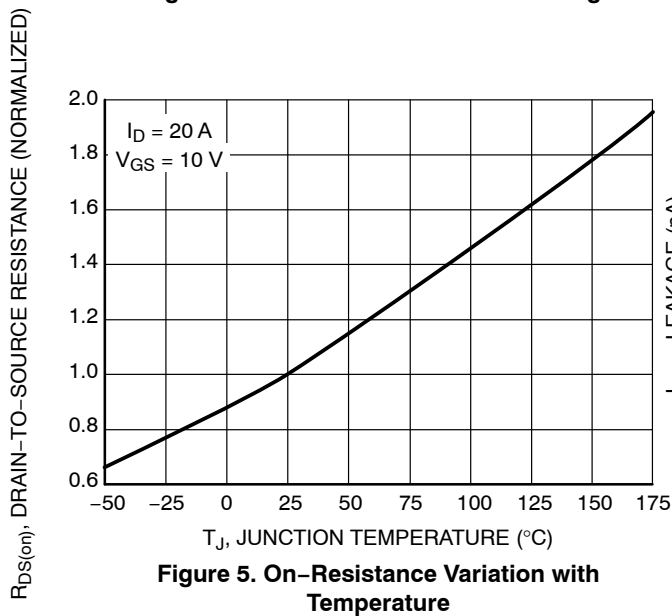


Figure 5. On-Resistance Variation with Temperature

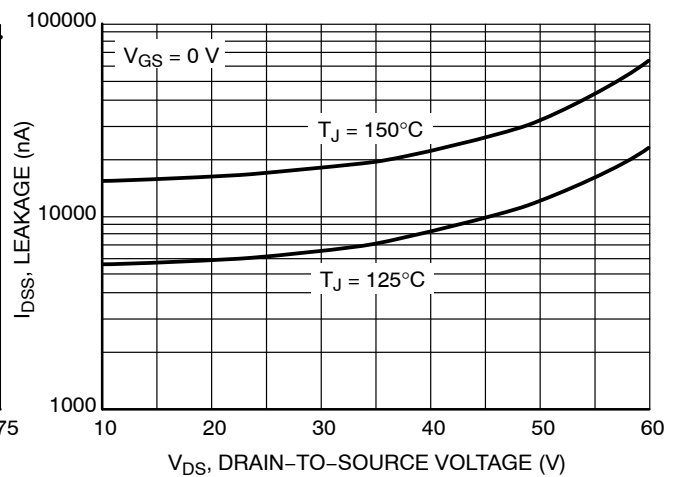


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

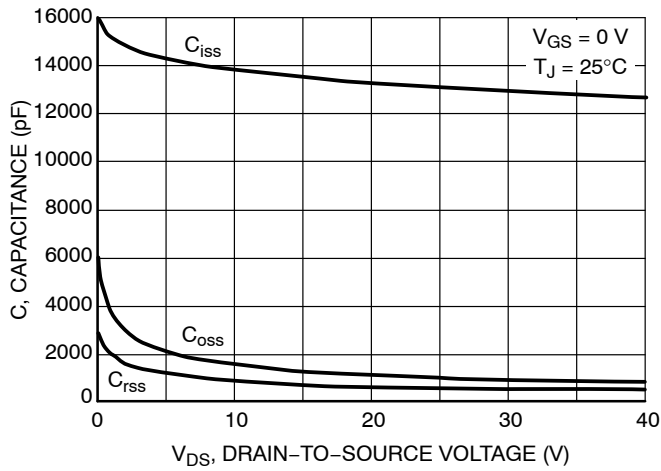


Figure 7. Capacitance Variation

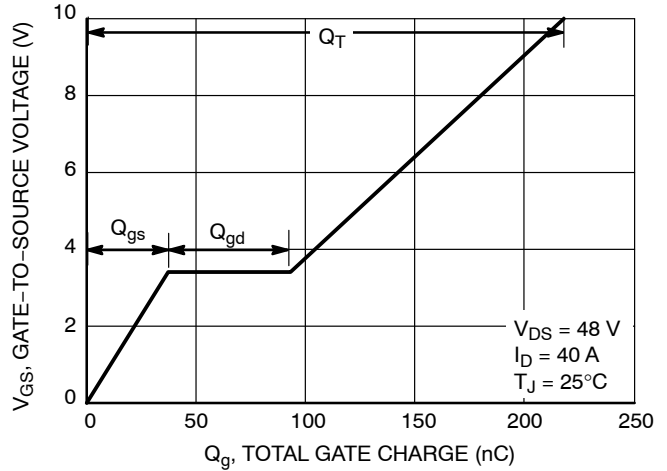


Figure 8. Gate-to-Source vs. Total Charge

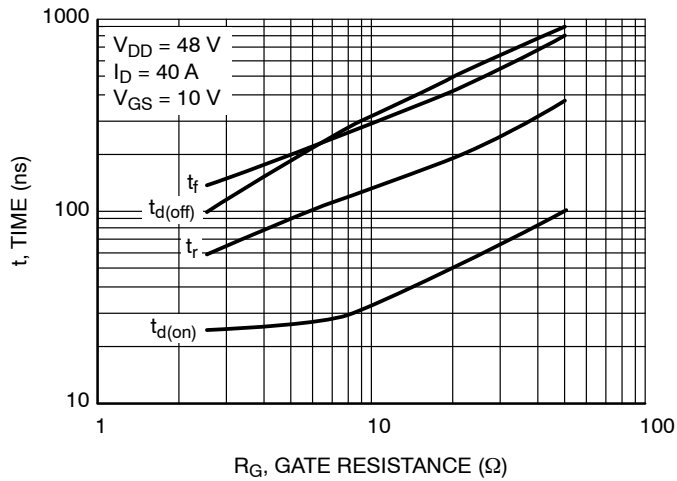


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

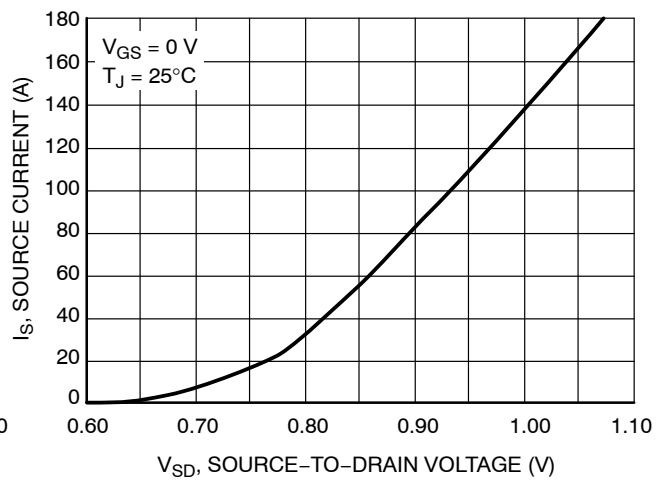


Figure 10. Diode Forward Voltage vs. Current

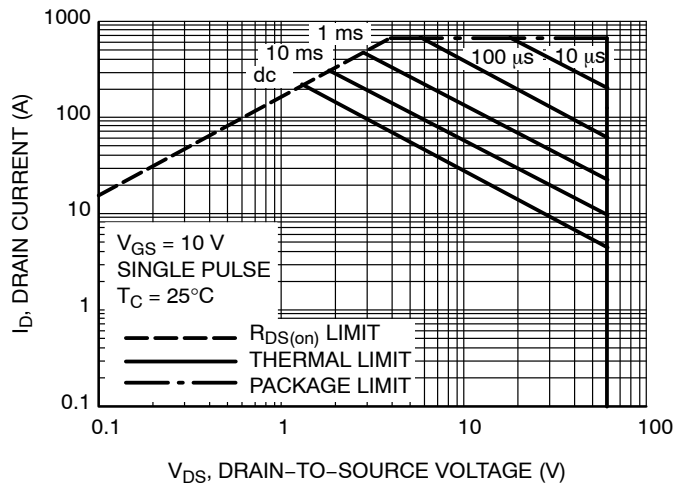


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NTB5860NL, NTP5860NL, NVB5860NL

## TYPICAL CHARACTERISTICS

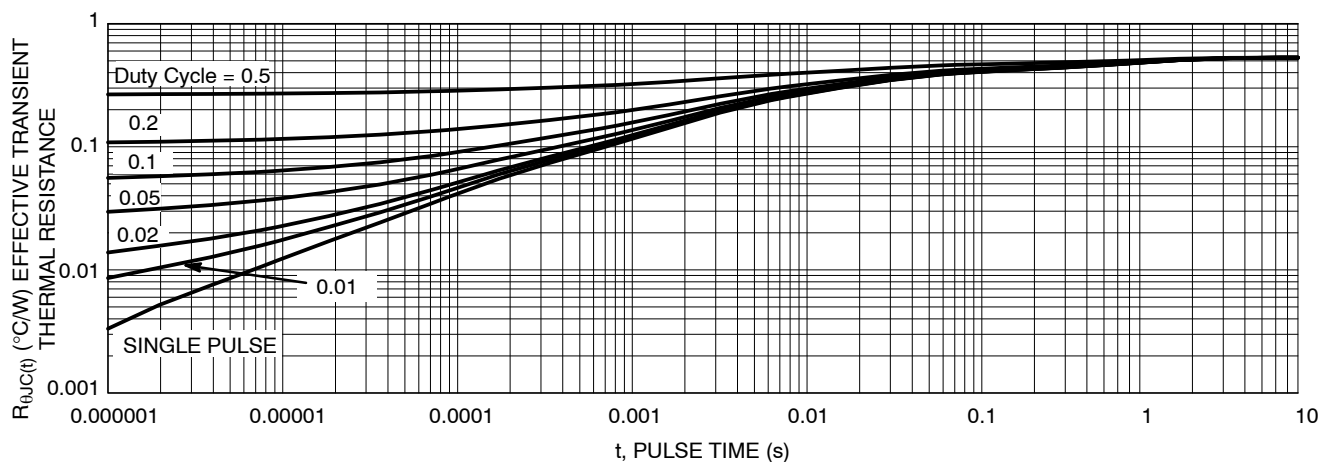


Figure 12. Thermal Response

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTP5860NLG	TO-220AB (Pb-Free)	50 Units / Rail
NTB5860NLT4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel
NVB5860NLT4G*	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel

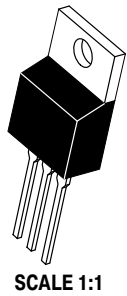
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NVB Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE

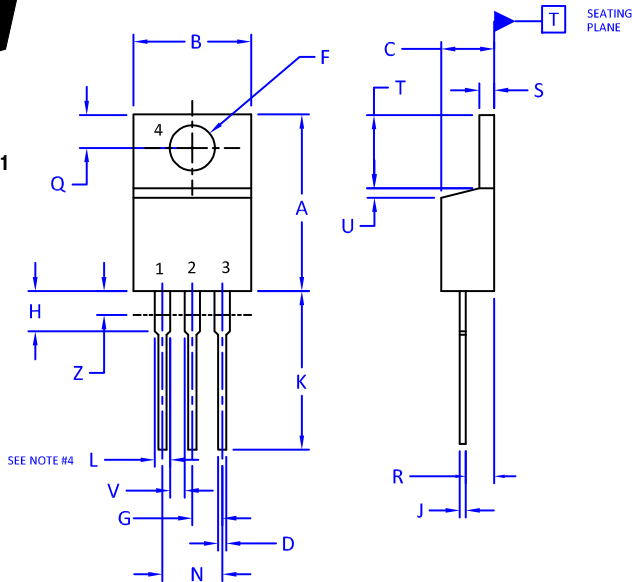
## PACKAGE DIMENSIONS

ON Semiconductor®



### TO-220 CASE 221A-09 ISSUE AJ

DATE 05 NOV 2019



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

STYLE 2:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR  
4. EMITTER

STYLE 3:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE

STYLE 4:  
PIN 1. MAIN TERMINAL 1  
2. MAIN TERMINAL 2  
3. GATE  
4. MAIN TERMINAL 2

STYLE 5:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

STYLE 6:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE

STYLE 7:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. ANODE

STYLE 8:  
PIN 1. CATHODE  
2. ANODE  
3. EXTERNAL TRIP/DELAY  
4. ANODE

STYLE 9:  
PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

STYLE 10:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN  
4. SOURCE

STYLE 11:  
PIN 1. DRAIN  
2. SOURCE  
3. GATE  
4. SOURCE

STYLE 12:  
PIN 1. MAIN TERMINAL 1  
2. MAIN TERMINAL 2  
3. GATE  
4. NOT CONNECTED

DOCUMENT NUMBER: 98ASB42148B

Electronic versions are uncontrolled except when accessed directly from the Document Repository.  
Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

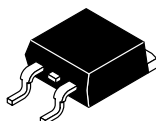
DESCRIPTION: TO-220

PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

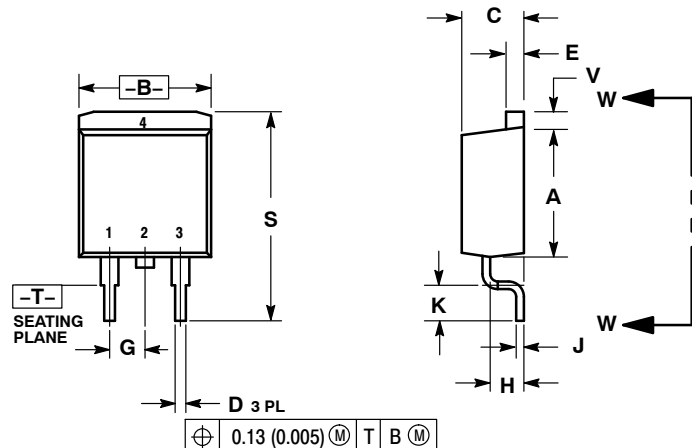
ON Semiconductor®



**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

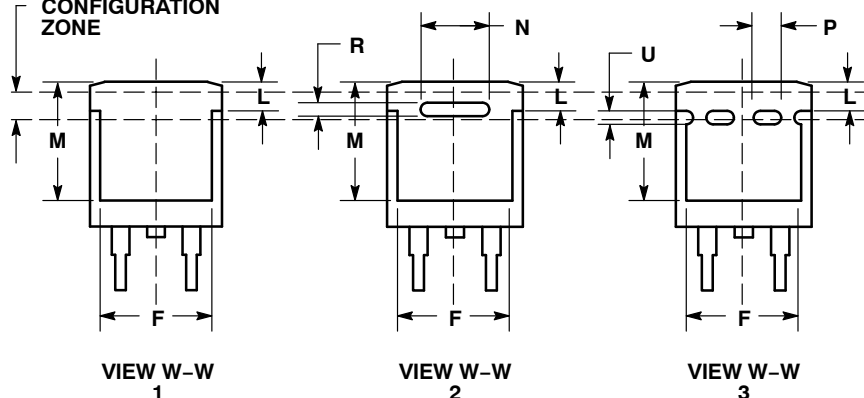


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

## VARIABLE CONFIGURATION ZONE



### STYLE 1:

- PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

### STYLE 2:

- PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

### STYLE 3:

- PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE

### STYLE 4:

- PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

### STYLE 5:

- PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. ANODE

### STYLE 6:

- PIN 1. NO CONNECT  
2. CATHODE  
3. ANODE  
4. CATHODE

## MARKING INFORMATION AND FOOTPRINT ON PAGE 2

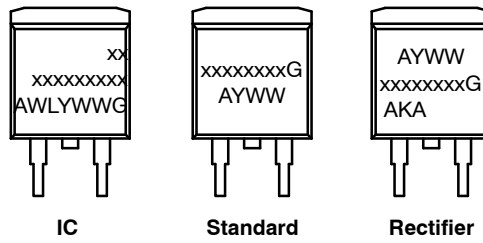
DOCUMENT NUMBER:	98ASB42761B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	D <sup>2</sup> PAK 3	PAGE 1 OF 2

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

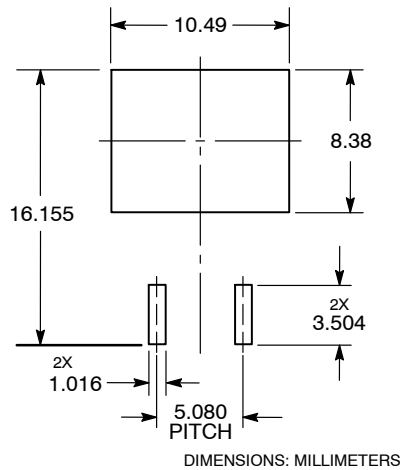
**GENERIC  
MARKING DIAGRAM\***



xx        = Specific Device Code  
A        = Assembly Location  
WL      = Wafer Lot  
Y        = Year  
WW      = Work Week  
G        = Pb-Free Package  
AKA     = Polarity Indicator


\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98ASB42761B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>D<sup>2</sup>PAK 3</b>	<b>PAGE 2 OF 2</b>

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.



**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative