TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

Department of Electrical and Computer Engineering, Técnico, University of Lisbon

Laboratory Assignment T3:

AC/DC

CONVERTER

MEAer

Group 15

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1 Introduction

For this laboratory assignment, our objective was to create a circuit that would transform an input AC voltage into an output DC voltage, with an amplitude of 12V. In Figure 1 the stated circuit is presented. In this report, we, first, proceeded to analyze the AC/DC converter, composed by an Envelope Detector Circuit and a Voltage Regulator Circuit, through a theoretical approach. Additionally, in Section 2, we obtained some insights on the non-linearity behaviour of the circuit by presenting an approximate solution (for the envelope detector and voltage ripple calculation) as well as combined OP and incremental analysis in the voltage regulator circuit, where we superimposed both solutions referred and studied the precision (variation of V_o - which should be as small as possible). To conclude this section, we consider it is important to refer that we bared in mind the quality of the circuit and to determine it we calculated a merit value, which acted as a system that took into account the cost of the components used, as well as the ripple and average amplitude of the output voltage.

Simultaneously, the circuit is analyzed by computational simulation tools, via NGSpice, in section 3. Then, the simulation results are compared with the theoretical ones, obtained in Section 2. Finally, the conclusions of this study are presented in Section 4.

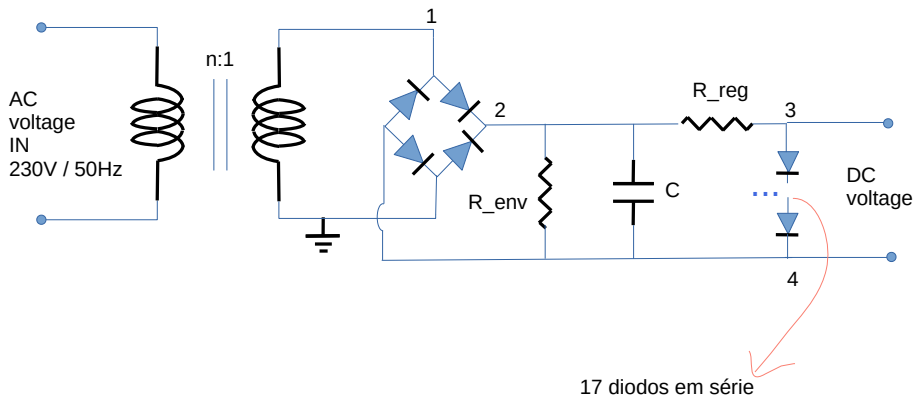


Figure 1: Circuit that will be analysed in this lab.

2 Theoretical Analysis

In this section, we shall analyze the circuit shown in Figure 1. Unlike the circuits analyzed in the previous laboratory classes, which only contained linear components (voltage and current sources, resistors and capacitors), the AC/DC converter circuit presents a non-linear behaviour, due to the presence of diodes, which are semiconductor components. The design of the AC/DC converter consisted, then, in two different stages, as described in the theoretical lectures: the Envelope Detector and the Voltage Regulator. We were given the freedom to use whatever component we wanted in order to achieve a DC Voltage of 12 V at the output of the Voltage Regulator circuit, although at the cost of some predefined monetary units (MU), as it will be reflected on our figure of merit.

2.1 Stage 1: Envelope Detector

The first part of our circuit was to design a proper Envelope Detector, in which the input sinusoidal voltage ($v_{IN} = Acos(\omega t)[V]$)would be converted to a signal with no negative values of voltage, while also intending to attenuate the voltage fall to zero (characteristic of the sinusoidal behaviour), with the goal of getting a more constant output voltage, in preparation for the Voltage Regulator part of the circuit (discussed in the next subsection). This was possible due to the use of diodes and a capacitor.

The diodes' function in the Envelope Detector was to rectify the input voltage, which was defined as being sinusoidal, as required in the laboratory guide. It was taught in the theoretical classes that a forwardly biased diode would only let pass through voltages with the same direction as the forward bias one. Therefore, a forwardly biased diode with its positive terminal connected to the positive terminal of a voltage source only conducts positive levels of voltage superior to a predetermined level, dubbed V_{ON}, which is a characteristic property of the diode (in this case, we considered it as approximately 0,7 V). This interesting property allows to establish the so-called Diode Bridge, a device consisting of four diodes disposed as shown in Figure 1, whose output voltage corresponds to the absolute value of the input voltage. Hence, implementing a Diode Bridge in our circuit would allow to not only rectify the input signal, but also diminish the time constant ($\tau = R_{eq}C$) required to have the smallest ripple (difference between the maximum and the minimum of the output voltage) possible. That's why we decided to implement a Diode Bridge into our design.

On the other hand, it was necessary to include a capacitor, that, by discharging, would allow to make the output signal as constant as possible, thus reducing the ripple.

We also added a resistor in parallel with the capacitor, as we stated that this addition would simplify our theoretical calculations, by making the circuit more similar to the one presented in the theoretical classes.

Now, we shall proceed to the theoretical analysis of the Envelope Detector circuit. First, we must note that the two inductors which constitute the transformer can be modeled by a current controlled current source on the primary and a voltage controlled voltage source (v_S) on the secondary. In what concerns to this analysis, only the voltage source matters, inputting a sinusoidal voltage with amplitude $\frac{A}{n}$ to the circuit, where A is the amplitude of the input signal at the transformer (230 V, as given in the laboratory guide) and n is the ratio between the number of spires on the primary and the one on the secondary. Then, for a matter of simplicity and convenience, we modeled each diode as a set of a voltage source, $V_{ON} = 0,7V$, and an ideal diode. As a result of the Diode Bridge behaviour, only two diodes will be on at each instant: two when the input sinusoidal voltage is positive, and the other two when it presents negative values. As we defined each diode as a group of a voltage source and an ideal diode, the allowed voltage levels in the circuit are the ones for which $|v_S| - 2V_{ON}$ is positive; when this value is negative, the voltage in the circuit will be null. This behaviour is shown in Figure 2.

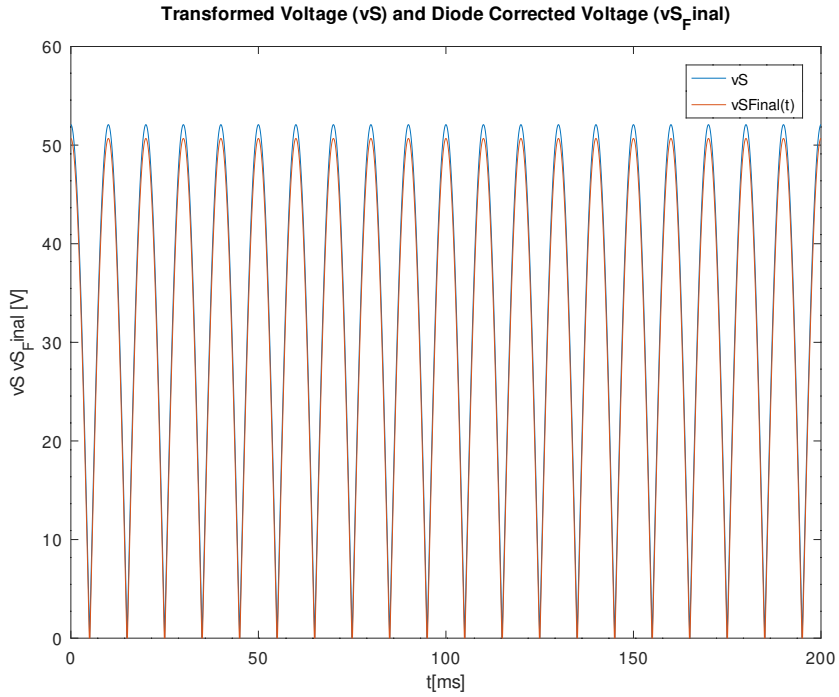


Figure 2: Modeled Diode Rectified Voltage Signal

We must, now, explain how we modeled the voltage in capacitor (and, consequently, in the resistor in parallel). As explained in the theoretical classes, this voltage presents two stages: a sinusoidal stage and an exponential stage. In fact, the sinusoidal input signal will charge the capacitor up to its amplitude value and, then, the capacitor discharges, as long as the negative exponential presents greater values than the sinusoidal signal. When the sinusoidal signal becomes the one with superior values again, the capacitor returns to charging, and the envelope output becomes sinusoidal again. In short, the voltage in the capacitor is, at each instant, the greater of two values: the one obtained through the rectified sinusoidal signal presented in Figure 2 and the one derived from the negative exponential, defined by the equation:

$$negativeExponential(t) = (\frac{A}{n} - 2V_{ON})e^{-\frac{t-t_{Aux}}{R_{eq}C}} \tag{1}$$

In the equation, t is the time instant, C is the capacitor's capacity [F], t_{Aux} [s]is a constant corresponding to the translation of the exponential, and R_{eq} is the equivalent resistor [Ω] as seen by the capacitor:

$$R_{eq} = \frac{1}{\frac{1}{R_{env}} + \frac{1}{R_{volt}+n_d r_d}} \tag{2}$$

The described behaviour is, then, repeated periodically, producing a plot resembling saw teeth, as shown in Figure 3 We also add that this is an approximated behaviour, that further simplified the analysis of this part of the circuit.

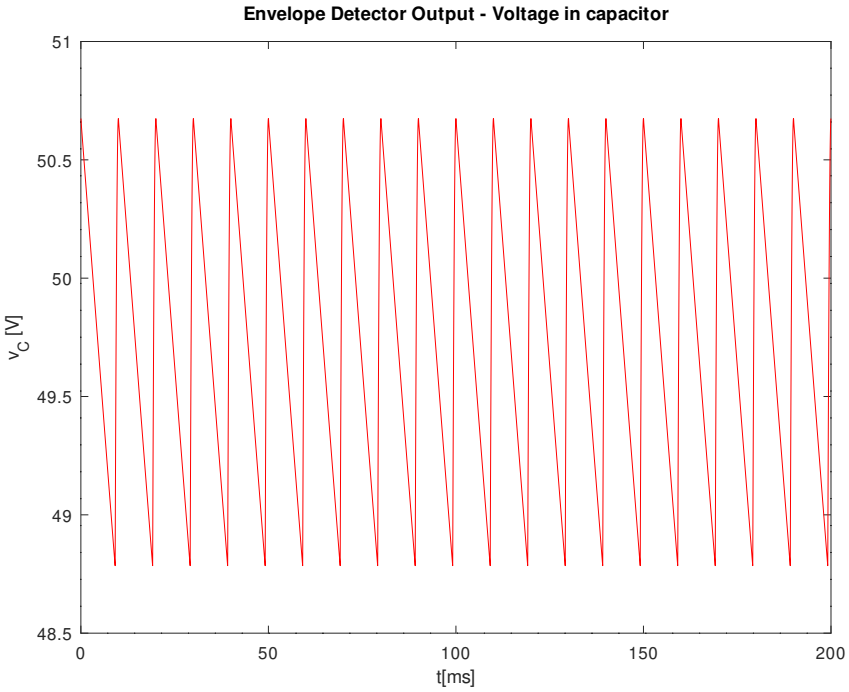


Figure 3: Envelope Detector Output Voltage

2.2 Stage 2: Voltage Regulator

We are, now, going through the analysis of the second part of the circuit, the Voltage Regulator, whose purpose is to attenuate the ripple in the output voltage of the Envelope Detector, aiming to achieve a final output of 12 V with the shortest ripple possible. For that, we connected a series of a resistor and a total of n_D diodes to the terminals of the capacitor. This solution is similar to the one presented in the theoretical classes, and can be explained using Incremental Analysis, which proved to be a very useful tool. According to Incremental Analysis, the output voltage, V_o, is defined as the sum of two components:

$$V_o = V_O + v_o \tag{3}$$

V_O is the DC component of the output voltage, corresponding to a steady value of 12 V, as intended. On the other hand, v_o is the incremental component of the output voltage, defined as an almost infinitesimal variation of V_o.

Starting by the study of the incremental components, we should first note that, in an incremented model, each diode is represented by the respective incremental resistor, whose resistance (r_d) can be obtained by:

$$r_d = \frac{\eta V_T}{I_S e^{\frac{V_D}{\eta V_T}}} [\Omega] \tag{4}$$

I_S is the saturation current [A], V_T is the thermal voltage [V], η is the material constant (assumed as 1) and V_D is the voltage in each diode [V], as assumed by the incremental model.

Then, by applying applying Kirchhoff Voltage Law (KVL) to the Voltage Regulator mesh, we could extract the following relation for v_o, where i_d [A] is the incremental current in the diodes and the resistor (with resistance R_{volt}) and v_c [V] is the incremental voltage in the capacitor, given by the difference between the total voltage in the the capacitor and its DC component, V_C, computed as its average.

$$v_o = n_D r_d i_d = \frac{n_D r_d}{R_{volt} + n_D r_d} v_c \tag{5}$$

We note, as a result, that for a resistance R_{volt} much greater than r_d, the incremental output voltage (correspondent to the ripple) tends to zero. That's why R_{volt} should be as great as possible. However, R_{volt} shall also be far inferior to the resistance in parallel with the capacitor, so that the latter tends to behave like an open circuit, and thus driving more current to the Voltage Regulator.

Next, by running an operating point analysis, we deduced the following relation for the voltage in each diode, V_D, which is assumed as a constant:

$$V_D = n_d r_d i_d = \frac{V_O}{n_D} \tag{6}$$

This equations allowed, hence, to produce the plots for V_o and v_o, where we can easily notice the saw teeth-like behaviour of the output signal, like in the voltage in the capacitor. However, this time, the ripple was severely reduced, and the average output voltage is very close to 12 V, as intended. In fact, the ripple obtained through this analysis is just 0.021365 V, a very small value when compared with V_O = 12 V.

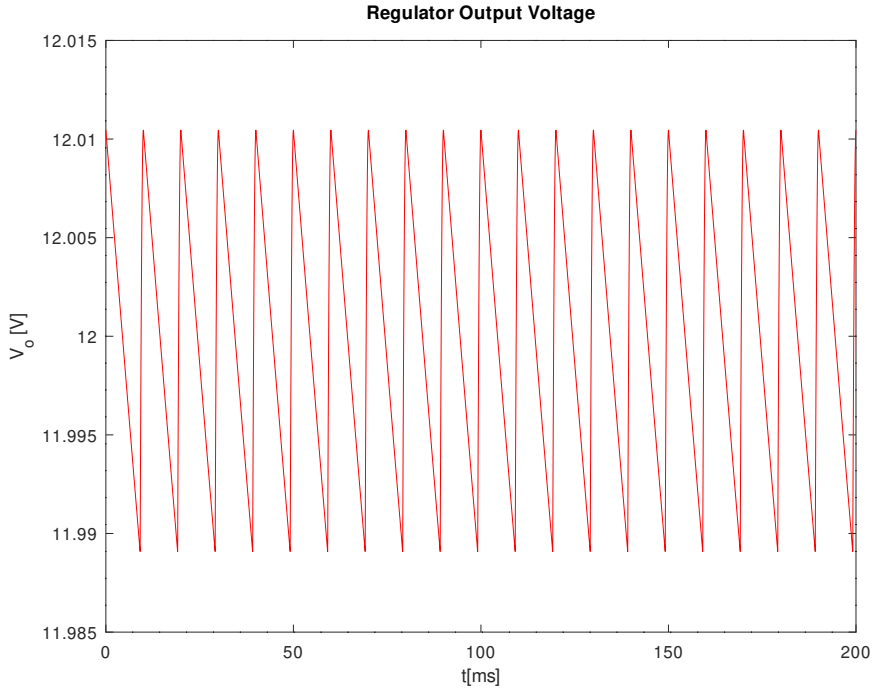


Figure 4: Regulator Output Voltage

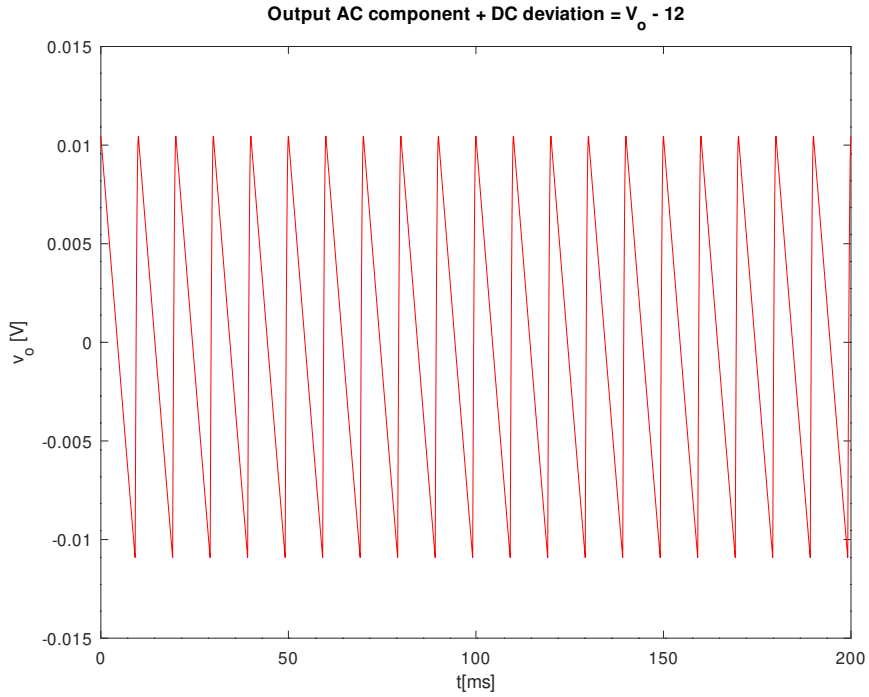


Figure 5: Output AC component + DC Deviation

After some trial runs with NGSpice, we adopted the following values, as they produced the most favorable output voltage:

A = 230 V (Input Voltage Amplitude);
n = 4.416766044 (Primary-Secondary Ratio);
f = 50 Hz (Voltage Source Frequency);
ω = 2*pi*f [rad/s] (Radian Frequency);
R_{env} = 15000 Ω (Envelope Detector Resistor);
C = 60e-6 F (Envelope Detector Capacitor);
V_{ON} = 0.7 V (Model Diode Voltage);
I_s = 1e-14 A (Saturation Current);
η = 1 (Material Constant);
T_{nom} = 300.15 K (Nominal Temperature);
k = 1.38064852e-23 J/K (Boltzmann Constant);
q = 1.60217662e-19 C (Electron Charge);
V_T = (k*Tnom)/q = 25,86491702e-3 V (Thermal Voltage);
n_D = 17 (Number of Diodes in the Voltage Regulator);
V_O = 12 V (DC Voltage Output);
R_{reg} = 5400 Ω (Voltage Regulator Resistor);

3 Simulation Analysis

In this section we defined our AC/DC transformer (seen in Figure 1) in NGSpice.

First off, we started by defining a transformer using the ideal model that says that we can substitute the inductor on the transformer's primary with a current dependent current source and the secondary's inductor is replaced by a voltage dependent voltage source, and defining the given voltage on the primary as v_{IN} and the voltage that results from the transformer as v_S, using the model mentioned above we will have $v_S = \frac{v_{IN}}{n}$. For reference, we will be referring to the DC output voltage as V_o.

After that we defined all the sources we designed for our circuit, used the default diode model and obtained the following plots of the Voltage outputs in $Volt$ for 10 periods: the time used was from 1.006 to 1.206 seconds because we found it would be an equivalent time interval to the one used in the theoretical analyses from 0 to 0.2 seconds. We did not use the same time intervals because in the theoretical analyses we didn't take into account possible variations that happened while initializing the circuit. But truthfully there is a different variation of the output voltages in the beginning for low time stamps. That's also why, for NGSpice, we used $t > 1$ so that the circuit's output voltage was already regular.

The two graphs bellow show the DC output voltage source and that same plot next to the transformed voltage v_S, respectively.

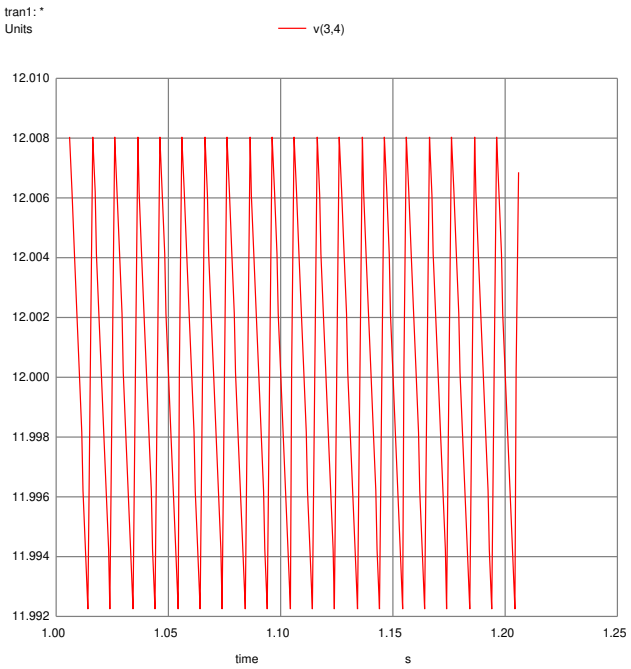


Figure 6: V_{DC} output voltage

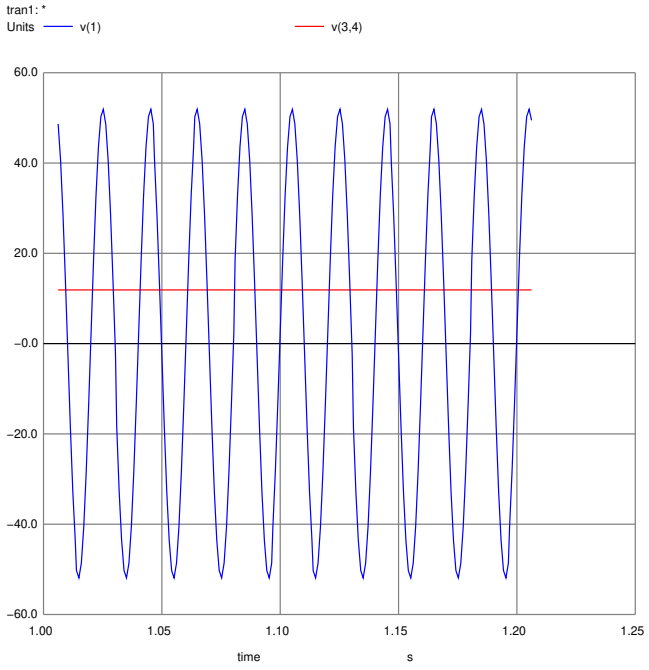


Figure 7: V_S (v(1)) and V_{DC} (v(3,4)) side by side

As we can see, there are oscillations (Figure 6), but these are almost null in comparison to the V_S voltage (Figure 7), so much that it appears to be a straight line, which would be the case if the AC/DC converter was perfect.

Unfortunately this is almost impossible, therefore we did not obtain a perfect straight line in Figure 6, so we calculated the average and ripple values obtained in NGSpice. These results are presented in the following table:

Name	**NGSpice Value [V]**
vavg	1.200016e+01
vmin	1.199225e+01
vmax	1.200806e+01

Table 1: Average (vavg),Minimum (vmin)and Maximum (vmax) values of v_O

We also calculated the absolute of some error values, such as:

Name	**NGSpice Value [V]**
abs(vmax-vmin)	1.581000e-02
abs(vavg-12)	1.600000e-04
abs(vavg-12)+abs(vmax-vmin)	1.597000e-02

Table 2: Ripple (vmax-vmin), Average error (vavg-12) and the sum of both errors for v_O

As we can see, the average is very close to 12, and the error is very low. The ripple is also low, but it could have been better if we had used higher values of C or R, however we also had to balance the costs to achieve a good merit. So we accepted this error value as it is still low. With both errors we will be able to calculate the merit of the circuit with the formula given in the lab assignment. This will be done in Section 4.

At this point, let's take a look to the outputs of our Envelope Detector and Voltage Regulator. The first one consisted of the Diode Bridge, the resistor R_{env} and the capacitor C. So the output of this part of the circuit is the same as the voltage flowing through the capacitor: v_C. This result is in the following plot.

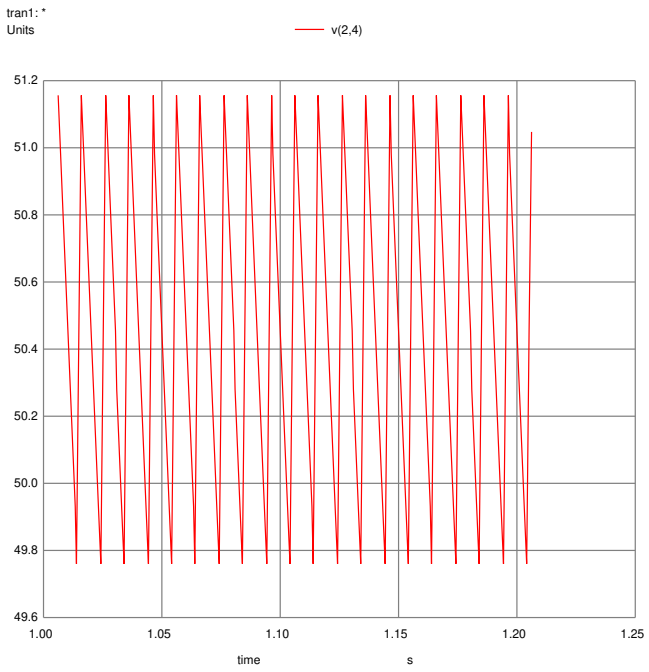


Figure 8: Envelope Detector Output

The Voltage Divider was constituted by the resistance R_{reg} and the 17 diodes in series. Obviously, its output is the same as the DC output voltage, that we repeat in the next image.

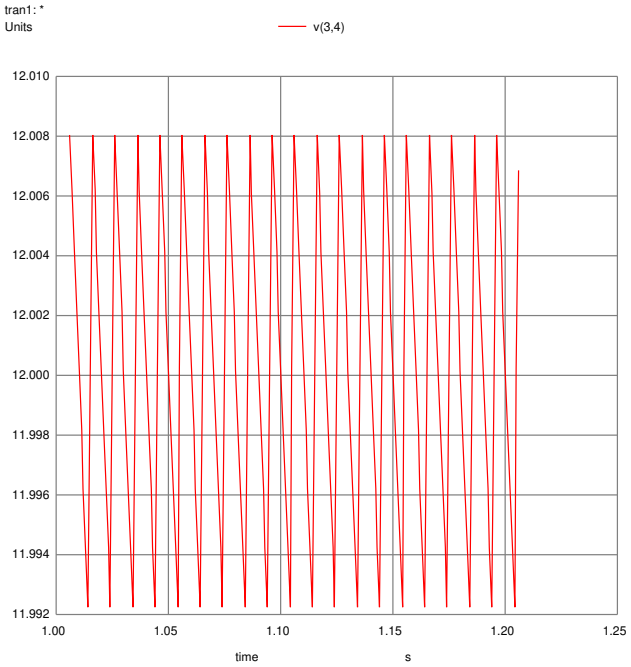


Figure 9: Voltage Detector Output

Finally, we obtained the graph of $V_{DC} - 12$, this is, the output AC component + DC deviation.

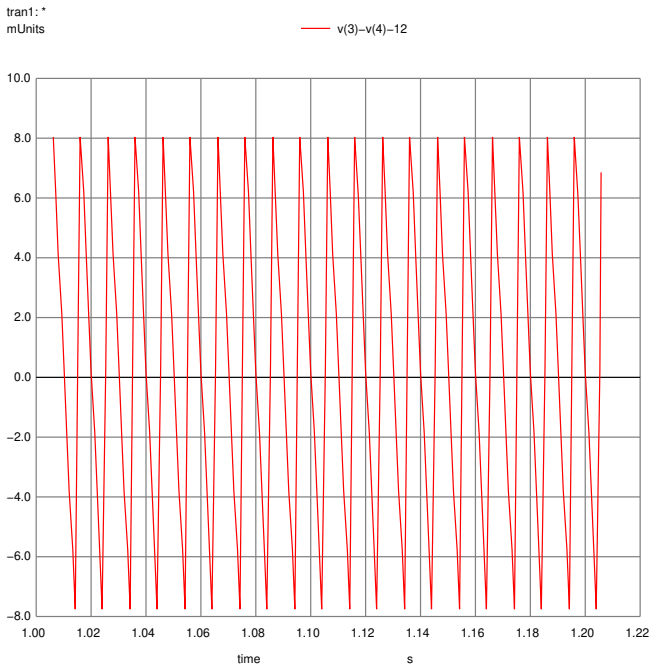


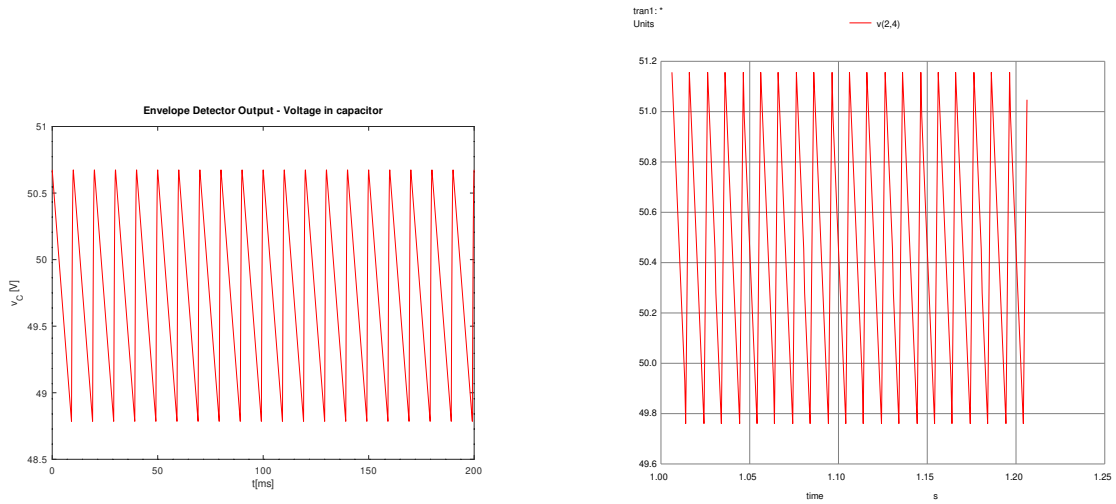
Figure 10: v_O AC component + DC deviation

Given that this graph is shown in the order of mV, we can say that the results are quite good and this variation is low enough to consider this a successful AC/DC transformer.

4 Conclusion

To start this conclusion we will compare all the results we obtained in NGSpice and in Octave side by side. As explained in Section 3, although the time intervals for Octave and NGSpice plots are different, they are equivalent. This is because this circuit's output voltage, even if it's not a sinusoidal function, will be periodical, so for different, but equivalent time intervals, they should have the same plots.

Starting of with the Envelope Detector v_C plots:

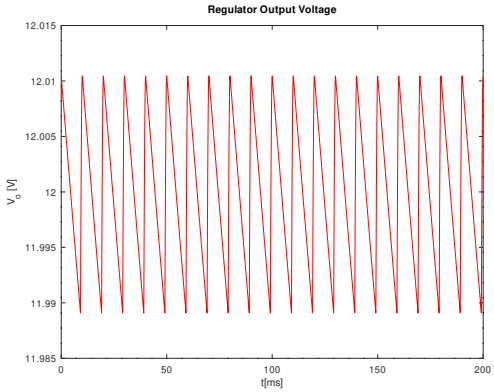


(a) Octave (b) NGSpice

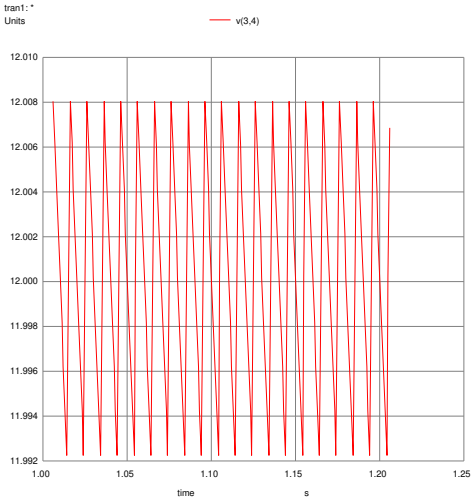
Figure 11: Envelope Detector Output

As we can see these are quite similar but show some differences when it comes to their Y axis. This will happen for all plots because of the different assumptions that took place in the making of this analysis, such as modeling each diode as a set of a Voltage Source V_{ON} and an ideal diode in the theoretical analyses, opposite to NGSpice that doesn't follow the same model.

Let's see if these differences affect the Voltage Regulator's results:



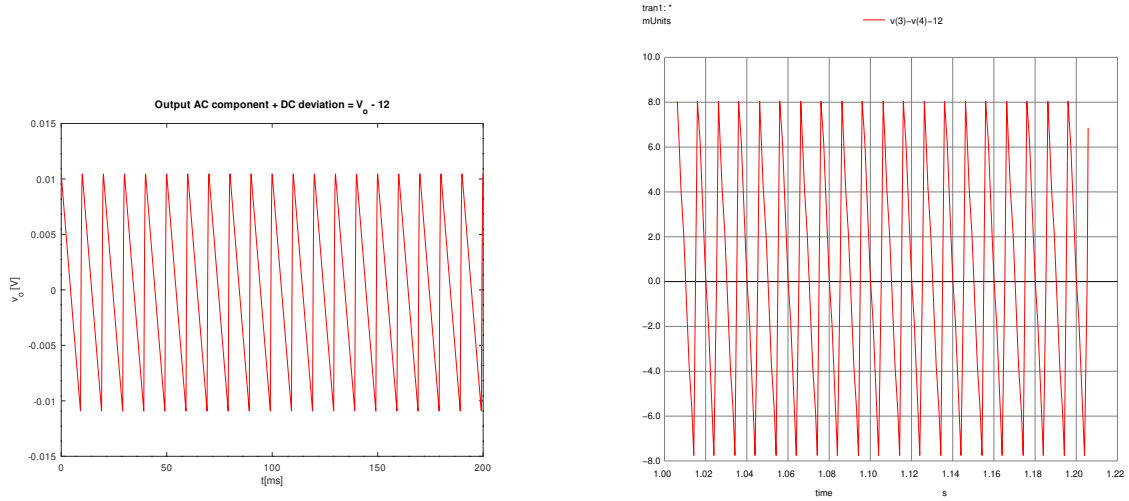
(a) Octave



(b) NGSpice

Figure 12: Voltage Regulator Output

There are also some differences shown above. Again, this happens because we used different models. Also, whilst in the theoretical analyses we immediately used $V_O = 12$V as the DC component of the voltage output, this was not the case in the NGSpice model, therefore they show a lag in the Y axis, because their average values will differ. However this difference is quite low, so it can go unnoticed by the human eye. There's also a small variation in the range of values for both plots, just like in Figure 11. The same explanation is applied here.



(a) Octave (b) NGSpice

Figure 13: Output AC component + DC deviation

As explained before, there is a lag in the Y axis for the DC Voltage output V_o, so the graphics above are off in their v_o values by a constant difference that is the error od the DC deviation. But the AC component is also expected to show differences, once again, because of the different models used in each analyses.

Given that the final output voltage V_o is the Voltage detector output, we won't present the same graphics again and this comparison has already been done in the side by side Voltage Detector graphics.

Finally, let's see how was our merit. Knowing that we used 21 diodes in total, two resistances with a summed value of 20.4 $k\Omega$ and a capacitor of 60 μF, the final cost will be:

$$Cost = 21 \cdot 0.1 + 20.4 \cdot 1 + 60 \cdot 1 = 82.5M.U. \tag{7}$$

Therefore, using the equation given in the instructions, our merit is given by:

$$Merit = \frac{1}{82.5 \cdot ((1.597 \cdot 10^{-2}) + 10^{-6})} \tag{8}$$

We programmed NGSpice to give us this value, and the result is in the following table:

Name	**NGSpice Value [V]**
1/((abs(vavg-12)+abs(vmax-vmin)+0.000001)*(60+15+5.4+2.1))	7.589514e-01

Table 3: Merit calculated in NGSpice

Therefore our merit was $M = 0.7589514$ This came from a combination of how the values adjusted considering n (characteristic of the transformer), trying to balance a low cost with low errors, even thought high capacitance and resistor values would mean lower error, we found that the values used gave us the best merit we were able to achieve.