TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

Department of Electrical and Computer Engineering, Técnico, University of Lisbon

Laboratory Assignment T4: Audio Amplifier

MEAer

Group 15

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1 Introduction

For this laboratory assignment, our objective was to create an audio amplifier circuit that would receive an audio input with an amplitude of 10mV and would connect to an 8 Ohm speaker. This amplifier was made of Bipolar Junction Transistors, specifically Philips models: BC557A (PNP) and BC547A (NPN), and was composed of two different stages, being the first one a Gain stage, with the purpose of having the maximum gain possible, being this a crucial step because a good voltage amplifier has to have a high gain due to the fact that we want to amplify the sound. The second one was an Output stage, which allowed us to lower the impedance of the Amplifier to achieve a better connection to the Load. In this second stage, a PNP transistor was used. Also, as we will present further through this report, a merit classification system was created to determine and ensure the quality of the audio amplifier.

In this report, it will be presented a theoretical analysis, in Section 2, where we used Operating Point (DC) to obtain important values for the then applied incremental analysis (AC), as studied in the theoretical classes, in order to predict the gain and the input and output impedances for each of the stages mentioned above, followed by a software simulation analysis, in the Section 3, made by a computational simulation tool: *Ngspice*. To sum up the report, the conclusions of this study are presented in Section 4, where the simulation results obtained in Section 3, are compared to the theoretical results obtained in Section 2.

Complete Circuit

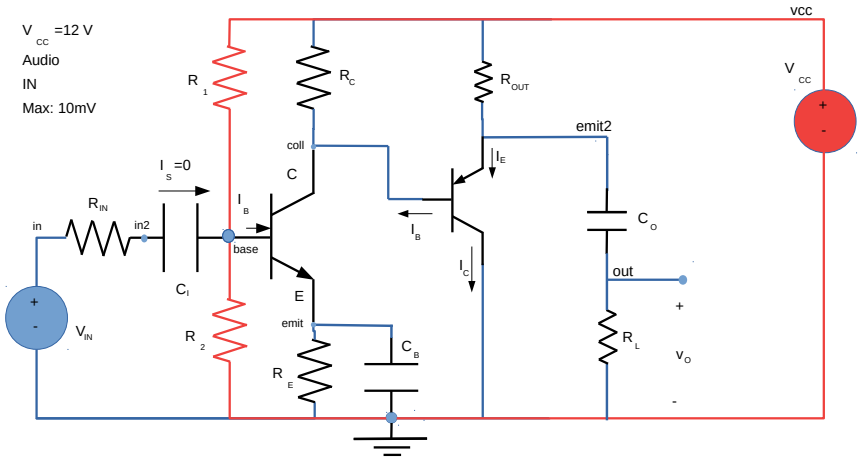


Figure 1: Circuit that will be analysed in this lab.

2 Theoretical Analysis

In this section, we aim to describe the behaviour of the Audio Amplifier circuit, presented in Figure 1, using the concepts we learned in the theoretical lectures. First, we shall note that this circuit is divided in two different stages, each one with its specific purpose: the Gain Stage and the Output Stage. Therefore, it is important to analyze each stage separately, by applying both Operating Point and Incremental Analyses, before focusing on a more generic analysis of the complete circuit. This process will allow us to determine a series of parameters, such as the Voltage Gain, the Bandwidth and the Input and Output Impedances, which define whether the Amplifier has a good performance or not. That is why some of these parameters were chosen to contribute to our figure of merit.

We will finish this section by studying the frequency response of the amplifier circuit, in particular how the voltage gain relates with the frequency of the input signal.

2.1 Gain Stage

We will, now, start our analysis by the first stage of the circuit: the Gain Stage. This stage is implemented with the single purpose of achieving the highest gain possible, thus composing the amplifying part that gives the circuit its name. This part of the circuit relies on a common emitter configuration, using an NPN type transistor, in order to accomplish the referred goal, as it is shown in Figure 2, which is characterized by having a high Input Impedance, which is a desirable feature, as it will not degrade the input signal too much, but also a high Output Impedance, which is prejudicial, because, as will explain further, it will consume the gain if directly connected to the 8 Ω Load Resistor.

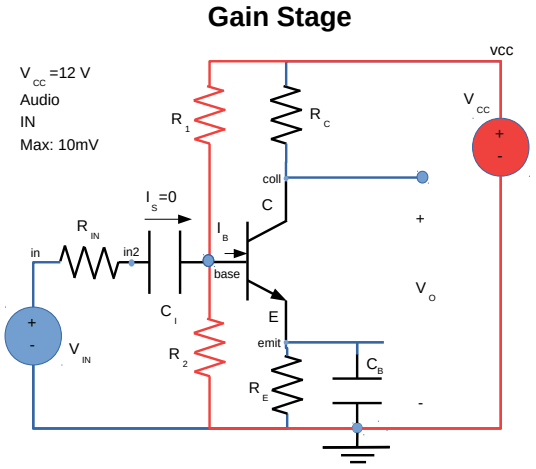


Figure 2: Gain Stage

2.1.1 Operating Point Analysis

We will begin the study of the Gain Stage by submitting it to the Operating Point Analysis. We find, as we start, a problem: we can't connect the signal voltage source directly to the base of the NPN transistor. This is due to the fact that the small source signal has a DC component of 0 V (which is typical in this kind of circuits), a value that is insufficient to guarantee that the transistor operates in the Forward Active Region (F.A.R), as it is recommended (and required). The solution for this issue is to implement a Coupling Capacitor and a Bias Circuit. The Coupling Capacitor, placed between the internal resistance of the source, R_{in}, and the

base of the transistor, acts as a DC block, filtering the DC component of the source signal and ensuring that only the AC component (the one which contains relevant information) flows through. However, the Coupling Capacitor also filters signals with low frequencies. That's why amplifier devices tend to struggle with small frequency signals. It is also important to refer that we should choose a high Coupling Capacitance (in the order of the mF), enough to guarantee a stable gain in the human audible range of frequencies. A low Coupling Capacitance (in the order of the μF) would correspond to a too high Lower Cut-Off Frequency, leading to a smaller bandwidth and stealing audible frequencies to the operating range of the amplifier, which is undesirable. On the other side, the Bias Circuit is composed by two resistors, R_{B1} and R_{B2}, and a supply DC voltage source, V_{CC}. Each resistor is connected to V_{CC} and to the base of the transistor, as the Figure 2 shows. This implementation imposes a proper DC voltage to the base of transistor, thus ensuring that the Base-Emitter Junction (BEJ) is on, this is, the transistor is operating in the F.A.R, as intended. We are, now, able to run the Operating Point Analysis. First, we note that, as the Coupling Capacitor behaves as an open circuit from the DC point of view (because it filtrates low frequency signals, in particular, DC signals, whose frequency is 0 Hz), the DC source voltage, V_S, the internal resistance, R_{in}, and the Coupling Capacitance are excluded from the OP analysis. Then, to simplify the analysis, we computed the Thévenin's equivalent of the Bias Circuit, as seen from the base of the transistor. The equivalent resistance (R_B) and voltage (V_{eq}) are given by the following equations:

$$R_B = R_{B1}||R_{B2} = \frac{R_{B1}R_{B2}}{R_{B1} + R_{B2}} \tag{1}$$

$$V_{eq} = \frac{R_{B2}}{R_{B1} + R_{B2}}V_{CC} \tag{2}$$

By applying Kirchhoff Voltage Law (KVL) to the Bias mesh, we can compute the base current, I_B, having in mind that the emitter current I_E is given by $I_E = (1 + \beta_F)I_B$ and that the Base-Emitter Voltage, V_{BEON}, is approximately 0.7 V:

$$I_B = \frac{V_{eq} - V_{BEON}}{R_B + (1 + \beta_F)R_E} \tag{3}$$

Then, the colector current, I_C, is simply given by:

$$I_C = \beta_F I_B \tag{4}$$

Applying KVL on the right side mesh allows us to determine the Static Output Voltage of the Gain Stage:

$$V_O = V_{CC} - R_C I_C = 7.9058V \tag{5}$$

We also need to be sure that this stage is operating in the F.A.R. This happens when the Collector-Emitter Voltage, V_{CE}, is higher than V_{BEON}. V_{CE} is given by:

$$V_{CE} = V_O - V_E = V_O - R_E(1 + \beta_F)I_B = 6.7295V > V_{BEON} \tag{6}$$

This confirms that this part of the circuit operates in the F.A.R, and, with this statement, we conclude the OP Analysis of the Gain Stage.

It is also relevant to refer that this stage corresponds to an Inverting Amplifier, because the output signal suffers a phase variation of π radians relatively to the input signal, which means that the output signal is inverted face to the input signal. This is not a problem, though, because the human ear can distinguish if a signal is inverted or not.

2.1.2 Incremental Analysis (Medium Frequencies)

We shall, now, proceed to the Incremental Analysis of the Gain Stage. We note that this analysis is valid for medium frequencies, because the capacitors behave as short-circuits in this range of frequencies. First, we need to replace the transistor with its incremental model. Each resistor keeps connected to the same nodes: R_{in} is connected to the incremental voltage source,v_i, R_B is placed between R_{in} and the base, R_E between the emitter and the ground and R_C between the collector and the ground. We note that V_{CC} is not considered in this analysis, because it does not have any AC component. On the other hand, v_i and R_{in} are now considered, because the Coupling Capacitor does not filtrate the AC component of the circuit; moreover, in this analysis, it behaves as a shot-circuit, as it was mentioned earlier. To simplify the analysis, we determined the Thévenin's equivalent for v_i, R_{in} and R_B:

$$R_{eq} = R_B||R_{in} = \frac{R_B R_{in}}{R_B + R_{in}} \tag{7}$$

$$V_{eq} = \frac{R_B}{R_B + R_{in}} v_i \tag{8}$$

We also computed the incremental parameters of the transistor:

$$g_m = \frac{I_C}{V_T} \tag{9}$$

$$r_\pi = \frac{\beta_F}{g_m} \tag{10}$$

$$r_o \approx \frac{V_A}{I_C} \tag{11}$$

, where V_T is the thermal voltage, V_A is the Early voltage, β_F is the forward common emitter current gain, g_m is the transconductance, r_π is the transitor's input (incremental) impedance and r_o is the transitor's output (incremental) impedance.

We now have all it is needed to determine the Voltage Gain, as well as the Input and the Output Impedances of the Gain Stage, which are all incremental parameters. The Voltage Gain, as it was deducted in the theoretical classes, is given by:

$$\frac{v_o}{v_i} = \frac{R_B}{R_b + R_{in}} R_C \frac{R_E - g_m r_\pi r_o}{(r_o + R_C + R_E)((R_B||R_{in}) + r_\pi + R_E) + g_m R_E r_o r_\pi - R_E^2} = -3.3704 \tag{12}$$

This value is negative, which confirms the gain Stage acts as an Inverting Amplifier. However, the Voltage Gain obtained is kind of unsatisfactory. One explanation for the low gain is the presence of R_E, whose function is to stabilize the effect of the temperature variation in the circuit, but with the disadvantage of lowering the Gain. One solution for this problem is to implement a Bypass Capacitor between the emitter and the ground (in parallel with R_E). This capacitor behaves as an open-circuit for low frequencies, and as a short-circuit for medium frequencies. In the low frequency range, in particular, for DC values (f = 0 Hz), the stabilization of the temperature effect provided by R_E is quite important, so, for this case, the current must flow through R_E, which is compatible with the Bypass Capacitor acting as an open-circuit (it is like the capacitor is not even there). But, in the case of medium frequencies, the Gain becomes more relevant; so, the Bypass Capacitor, working as a short-circuit, allows to effectively pass over (bypass) the resistor R_E, avoiding the prejudicial effect of R_E in the Gain and, thus, maximizing it. Therefore, the insertion of this component in the circuit guarantees the stability of the OP and, consequently, of the incremental parameters, such as g_m. The Voltage Gain in the

Gain Stage, after the implementation of the Bypass Capacitor, is equivalent to set $R_E = 0\Omega$, and is given by:

$$R_E = 0 \Rightarrow \frac{v_o}{v_i} = -g_m(R_C||r_o)v_\pi = -g_m(R_C||r_o)\frac{r_\pi||R_{B1}||R_{B2}}{R_{in} + (r_\pi||R_{B1}||R_{B2})}v_s = -136.02 \quad (13)$$

, which is a higher (and better) value for the Gain. The next plots show the difference between the Gains obtained without ($R_E = 100\Omega$) and with the implementation of the Bypass Capacitor ($R_E = 0\Omega$), and their effect in the Output Voltage of the Gain Stage.

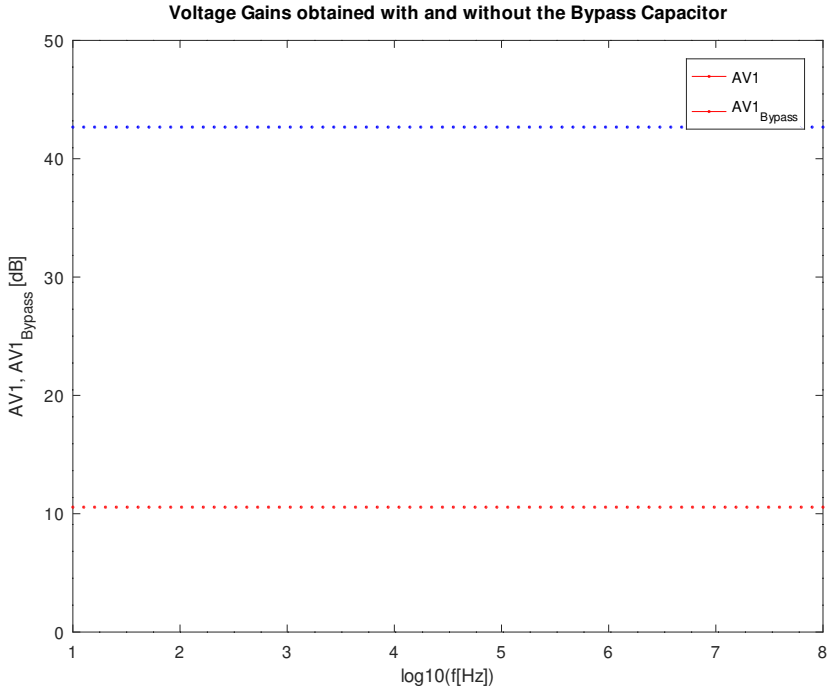


Figure 3: Voltage Gains Obtained with and without the Bypass Capacitor

We note that, in the previous plot and from now on, we will consider a frequency of 1 kHz in the plots in function of time.

We will now discuss the effects of the Bypass Capacitance in the bandwidth. If the value chosen is too low (in the order of the μF), we will obtain a low gain in part of the desirable bandwidth, specially in the human audible rande, which is the relevant part. We would only have a high and stable gain for frequencies superior to 20 kHz, but those are out of the human audible range, so, the Audio Amplifier would not achieve its purpose. Therefore, we should choose a higher value for the Bypass Capacitance (in the order of the mF), for which we would obtain a high and stable gain in the desirable passband (20 Hz - 20kHz) and in even higher frequencies.

We shall, now, compute the Input and the Output Impedances for the Gain Stage (Z_I and Z_O, repectively). As we learned in the theoretical classes, these are given, for the case where the Bypass Capacitor is implemented, by:

$$Z_I = R_{B1}||R_{B2}||r_\pi = 8383.0\Omega \quad (14)$$

$$Z_O = R_C||r_o = 661.16\Omega \quad (15)$$

We see that the Input Impedance is quite high ($R_{in} << Z_I$), which is a good result, meaning the input signal will not be too much degraded by it. Therefore, there's no problem in connecting

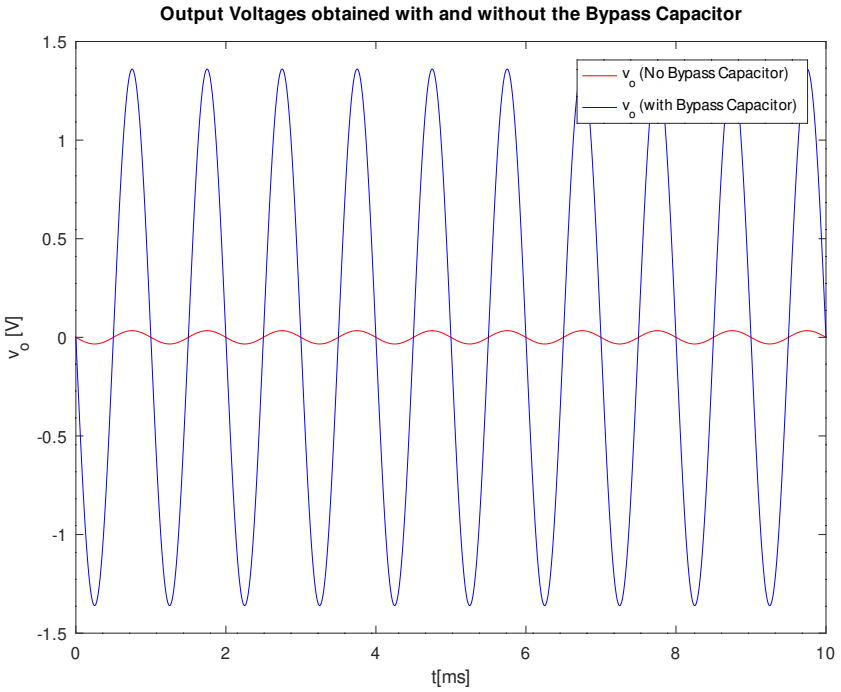


Figure 4: Output Voltages Obtained with and without the Bypass Capacitor

the signal source to the amplifier. However, the Output Impedance is too high to be connected to a load resistor with 8 Ω (a typical value among these devices), because the greater part of the voltage would be retained by Z_O, thus degrading a lot the output voltage signal in the load. The high Gain achieved in the Gain Stage would be lost, and the amplifier device would be ineffective. Therefore, we need to add an Output Stage to the circuit, with a very low Output Impedance, so that the greater part of the Gain Stage Output Voltage would be secured by the Load Resistor, protecting the Gain previously obtained.

2.2 Output Stage

We will now analyze the Output Stage, whose purpose was already discussed in the previous section. This part of the circuit uses, now, a PNP-type transistor, as required in the laboratory guide, and relies on a common collector configuration to achieve a very low Output Impedance, as presented in Figure 1.

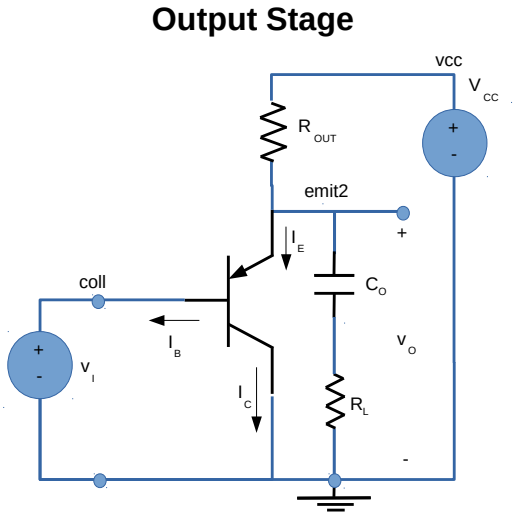


Figure 5: Output stage.

2.2.1 Operating Point Analysis

We will start our analysis of the Output Stage by computing its Operating Point. First, we should note that the (common) collector of the transistor is now connected to the ground,and not to V_{CC}, as the current flows from the emitter to the collector (we are dealing with a PNP transistor, now). Besides, even though the signal continues to be applied at the base of the transistor, the Output Voltage is now computed on the emitter. We also refer that the Emitter-Base Voltage, V_{EBON} is, approximately, 0.7 V, just as V_{BEON} in the Gain Stage. The input voltage, V_I in this stage is the output voltage of the Gain Stage. With that in mind, by applying KVL to the outer loop, we can determine the emitter current, I_E:

$$I_E = \frac{V_{CC} - V_{EBON} - V_I}{R_E} \tag{16}$$

The currents at the collector and at the base are then computed, using the following equations:

$$I_E = I_B + I_C \tag{17}$$

$$I_E = (1 + \beta_F) I_B \tag{18}$$

We can, now, determine the Static Output Voltage on this Stage, by applying KVL to the right side mesh:

$$V_O = V_{CC} - R_E I_E = 8.6058V \tag{19}$$

Alternatively, we can use a rather convenient formula, by applying KVL to the left side mesh:

$$V_O = V_I + V_{EBON} = 8.6058V \tag{20}$$

We note that, in this stage, the emitter current is much stronger than in the Gain Stage. This is a good achievement, as part of this current will feed the Load. However, it is important to note that a very high current leads to an also high dissipated power, making this stage quite inefficient in terms of energy. This is a common problem among Class A Amplifiers, like the one we are studying.

We can also predict that the Voltage Gain will be approximately unitary, as $V_E = V_O \approx V_B + 0.7 = V_I + 0.7$. The input and output voltages have the same AC amplitude, differing in a DC offset of 0.7 V, which translates in an unitary gain. In fact, the purpose of this stage is just supplying current to the load, or achieving a very low Output Impedance. The high Gain resposible for amplifying the signal was already obtained in the Gain Stage.

2.2.2 Incremental Analysis

We will now run the Incremental Analysis in the Output Stage. The process is, in all, similar to the one applied in the Gain Stage. First, we replace the PNP transistor with its incremental model, and connect each resistor to the respective nodes, having in mind that V_{CC} is not considered. The parameters g_m, r_π and r_o are computed in the same way as in the Gain Stage. However, at this point, it is easier to work with their respective admitances: $g_\pi = \frac{1}{r_\pi}$, $g_E = \frac{1}{R_E}$ and $g_o = \frac{1}{r_o}$. After applying Kirchhoff Current Law (KCL), we reach this formula for the Output Stage Voltage Gain:

$$\frac{v_o}{v_i} = \frac{g_m}{g_\pi + g_E + g_o + g_m} = 0.98768 \tag{21}$$

The obtained value for the Gain in this stage is almost unitary, as predicted in the previous subsection.

As we learned from the theoretical classes, the Input and the Output Impedances (Z_I and Z_O, respectively) for this stage are given by:

$$Z_I = \frac{g_\pi + g_E + g_o + g_m}{g_\pi(g_\pi + g_E + g_o)} = 8192.1\Omega \tag{22}$$

$$Z_O = \frac{1}{g_\pi + g_E + g_o + g_m} = 0.43841\Omega \tag{23}$$

Having in mind that Z_I must be far greater than the Output Impedance of the gain Stage, so the signal doesn't get degraded, we considered that the value we obtained for it was acceptable. On the other hand, the determined value for Z_O is very low, when compared with the 8 Ω Load Resistance. Therefore, the signal that reaches the load will not suffer a significant degradation, which means the Output Stage is fulfilling its purpose, and that we can connect the Output Stage to the Load Resistor without concern.

The next plot compares the Output Stage input voltage with its Output Voltage.

Finally, we note that we need to add another Coupling Capacitor between the emitter and the Load Resistor, in order to filter the DC component of the Output Signal, so that it doesn't affect the performance of whatever circuit we would want to connect to the Load Resistor. Also, the Output Stage consists on a Non-Inverting Amplifier, as the phase of the Output Voltage remains the same as the Input Voltage's.

The next plot compares the Output Stage input voltage with its Output Voltage (in terms of the AC component, because the DC component will be filtrated by the Coupling Capacitor). It is quite visible that the gain is almost unitary.

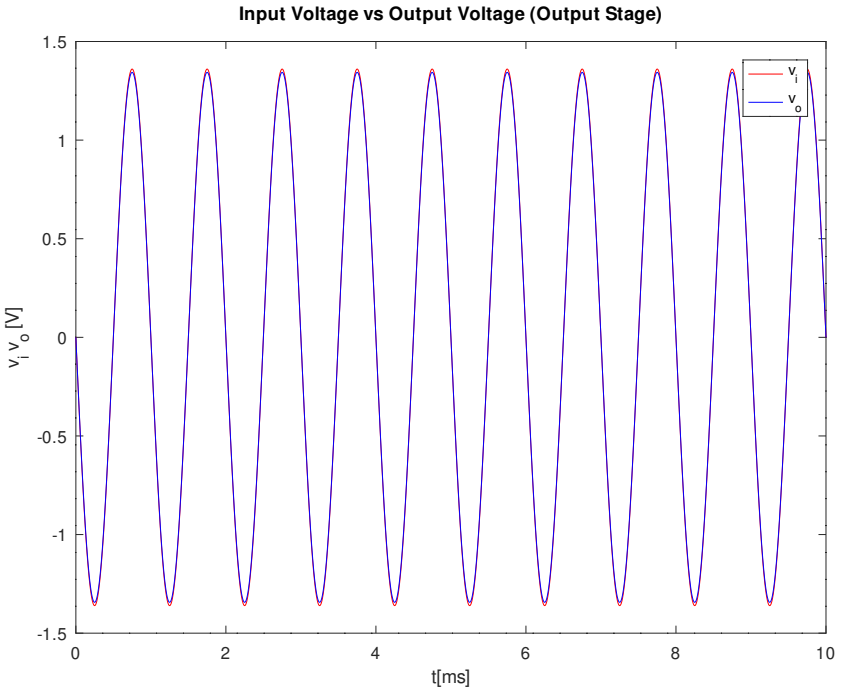


Figure 6: Input Voltage vs Output Voltage (AC Component)

2.3 Complete Circuit Analysis

Now that we analysed each part of the circuit separately, we will now present the equations for the gain and the Input and Output Impedances relative to the circuit as a whole. These formulae were obtained by replacing the circuit with its incremental model, in a medium frequency regime (the capacitors act as short-circuits). We will use the index 1 for parameters in the Gain Stage, and the index 2 for parameters relative to the Output Stage. The Voltage Gain of the entire circuit is given by:

$$\frac{v_o}{v_i} = \frac{\frac{1}{r_{\pi 2}+Z_{O1}} + \frac{g_{m2}r_{\pi 2}}{r_{\pi 2}+Z_{O1}}}{\frac{1}{r_{\pi 2}+Z_{O1}} + \frac{1}{R_{E2}} + \frac{1}{r_{o2}} + \frac{g_{m2}r_{\pi 2}}{r_{\pi 2}+Z_{O1}}} A_{v1} = -128.24 \tag{24}$$

The Input Impedance for the whole circuit is the same as for the Gain Stage:

$$Z_I = Z_{I1} = 729.02\Omega \tag{25}$$

The Output Impedance for the complete circuit is determined by:

$$Z_O = \frac{1}{g_{o2} + g_{m2}\frac{r_{\pi 2}}{r_{\pi 2}+Z_{O1}} + g_{E2} + \frac{1}{r_{\pi 2}+Z_{O1}}} = 3.1470\Omega \tag{26}$$

This confirms that the circuit has a high Input Impedance and an acceptably low Output Impedance, as intended. The Output Voltage of the circuit is compared to the one inputted by the source signal in the next plot (once more, just in terms of the AC component).

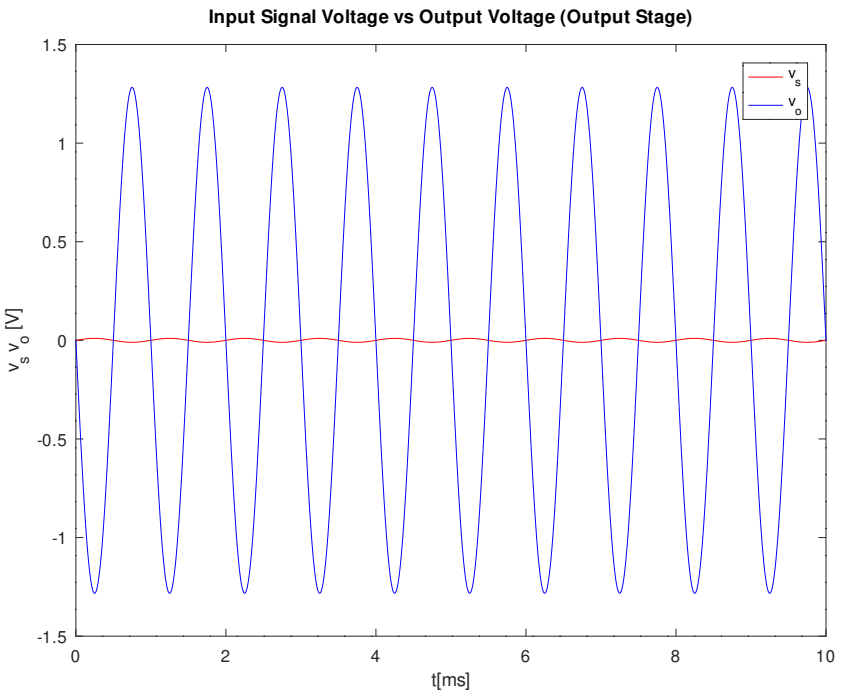


Figure 7: Input Signal Voltage vs Output Voltage (AC Component)

2.4 Frequency Response Analysis

The final part of the Theoretical Analysis of the Audio Amplifier circuit consists in the study of its frequency response, in particular, how the frequency affects the value of the Gain. In the previous subsections, the computed gain was constant, as it depended on the values of resistances and conductances. However, as it was referred in those subsections, this approximation was only valid for medium frequencies. In this section, we will analyze the behaviour of the circuit when operating with other frequency values, in particular with low frequencies. For that, we need to determine the Lower Cut-Off Frequency, which constitutes a flag for the edge between the constant gain passband and the low frequency band. The Lower Cut-Off Frequency is defined as the frequency for which the gain is inferior to the stable gain in 3 dB. This value can be calculated using the Time Constants Method. To apply this method, we need to determine, for each capacitor used, the Thévenin's equivalent resistance as seen by the capacitor's terminals when all the other capacitors are replaced with short-circuits. The equivalent resistance as seen by the Coupling Capacitor (C_i)in the Gain Stage (R_{eq1}) corresponds to the series of R_{in} and Z_I (Input Impedance for the whole circuit):

$$R_{eq1} = R_{in} + Z_I = 829.02 \tag{27}$$

The equivalent resistance as seen by the Coupling Capacitor (C_o) in the Output Stage (R_{eq2}) corresponds to the series of the Load Resistor R_L and Z_O (Output Impedance for the whole circuit):

$$R_{eq2} = R_L + Z_O = 11.147\Omega \tag{28}$$

In order to compute the equivalent resistance as seen by the Bypass Capacitor (C_b), we applied the Mesh Method to the incremental model of the Gain Stage. We replaced the Bypass Capacitor with a predefined voltage source; then, we computed the current flowing through this source. The equivalent resistance corresponds to the quotient between the predefined voltage and the computed current: $R_{eq3} = 4.6993\Omega$.

Having calculated all the equivalent resistances, and according to the Time Constants Method, the Lower Radian Cut-Off Frequency is given by:

$$\omega_L = \frac{1}{R_{eq1}C_i} + \frac{1}{R_{eq2}C_o} + \frac{1}{R_{eq3}C_b} = 209.32 rad/s \tag{29}$$

The Lower Cut-Off Frequency is, then, given by:

$$f_L = \frac{\omega_L}{2\pi} = 33.314 Hz \tag{30}$$

In order to present the plot for the frequency response of the Complete Circuit, we made a linear approximation for the low frequency region. We should note, first, that, for a null frequency (corresponding to DC values), the Voltage Gain will also be null, because, in this case, all the voltage would be filtered by the Coupling Capacitors. With that in mind, we approximate the low frequency region by a linear function defined by the origin of the referential and the point corresponding to the Lower Cut-Off Frequency (whose Gain is inferior to the Stable Gain in 3 dB). The point of the linear function whose gain would be equal to the Stable Gain determines, then, the beginning of the Stable Gain passband. For simplicity, we considered the Higher Cut-Off Frequency to be infinite; thus, in this approximation, the passband remains constant after the beginning of the passband.

The next plot shows the results we obtained for the frequency response.

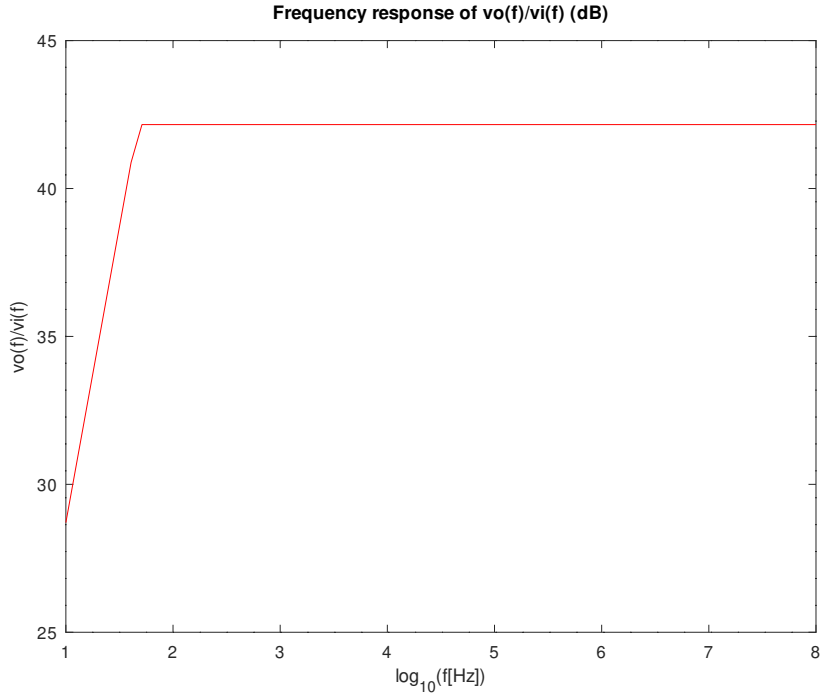


Figure 8: Frequency Response of the Complete Circuit

3 Simulation Analysis

In this section we used the NGSpice script provided and added the needed alterations.

Coupling Capacitors[1]

[1] These topics were already explained in class, therefore we will only make a small summary of what was already approached in class.

First off, we must understand the importance of the coupling capacitors. Two examples of these are the capacitors Ci and Co. As explained in class, these capacitors will be important to decrease the lower cut-off frequency of the circuit, while maintaining the higher cut-off frequency, therefore increasing the bandwidth. This because if it's impedance is $\frac{1}{2\pi fCj}$, if we decrease the frequency, the impedance will increase, tending to an open circuit. To avoid this and allow the circuit to pass more frequencies, we can increase the C value to compensate the decrease of frequency. Therefore we increased the value of Co from 1μF to 0.8mF.

Bypass Capacitor

The bypass capacitor of this circuit was Cb. This capacitor has the main function of increasing the gain, because when in parallel with Re, it will act like a short-circuit for higher frequencies (Z$\rightarrow$0), making v(emit)=0. And if we analyze Figure 2 we see that the output voltage of the Gain Stage will increase by decreasing v(emit). So the gain of the Gain Stage will be higher, which will eventually lead to a bigger gain of the total circuit for medium and high frequencies. Also, with higher values of C, we will have lower impedances, so we will need lower frequencies to have a short circuit approximation in place of the capacitor. For this, we changed the Cb value from 1mF to 2.5mF.

Rc importance

Finally, as seen in the theoretical analyses, during the gain stage, the resistor Rc will also have an influence on the gain. However this influence is not linear. So for this circuit we actually found that values smaller than the original one (1kΩ) gave us better merit results, despite slightly decreasing our gain value, because it also increased the higher cut-off frequency, and lower values also gave us lower output impedances, which we will see later why that was preferable. We ended up choosing a value of 700Ω.

With this, we printed Table 2 with all the values we used.

Component	**Value ([Ω] or [F])**
R1	80000
R2	20000
Rc	700
Re	200
Rl	8
Rout	60
Ci	0.0001
Cb	0.0025
Co	0.0008

Table 1: Circuit Component's values

After that we ran an Operating Point (OP) Analyses, and will later compare the theoretical and simulated results.

Name	Value [A] or [V]
@q1[ib]	3.230371e-05
@q1[ic]	5.910659e-03
-@q1[ie]	5.942963e-03
v(emit)	1.188593e+00
v(coll)	8.080741e+00
v(coll)-v(emit)	6.892148e+00
-@q2[ie]	5.225002e-02
@q2[ic]	5.193830e-02
v(emit2)	8.864999e+00

Table 2: OP analyses.

While we were still under the OP analyses section we verified if the transistors were acting in the Forward Active Region (F.A.R.). For this the NPN transistor (Q1) must obey the following equation:

$$V_{CE} > V_{BE} \Leftrightarrow \text{v(coll)-v(emit)} > \text{v(base)-v(emit)} \tag{31}$$

The following table shows those values.

Voltage	Value [V]
v(coll)-v(emit)	6.892148e+00
v(base)-v(emit)	6.945481e-01

Table 3: F.A.R. analyses - NPN transistor

Equation 31 is validated, so the transistor in the gain part of the circuit is in F.A.R. For the PNP transistor, the equation that tells us if the component is in F.A.R is:

$$V_{EC} > V_{EB} \Leftrightarrow \text{v(emit2)} > \text{v(emit2)-v(coll)} \tag{32}$$

The table that will give us the values to verify the equation is the following:

Voltage	Value [V]
v(emit2)	8.864999e+00
v(emit2)-v(coll)	7.842582e-01

Table 4: F.A.R. analyses - PNP transistor

Once again, equation 32 is followed, so we can move on with our analyses because both transistors are acting in the forward active region.

After the OP analyses, given that there wasn't much interest in doing a transient analyses, once that the objective was to make an audio amplifier, we moved on to a frequency analyses. Starting of with the circuit's gain: $\frac{v_o(f)}{v_i(f)}$, we plotted the following graph in dB, so that it would be easier to compare to the theoretical results later on.

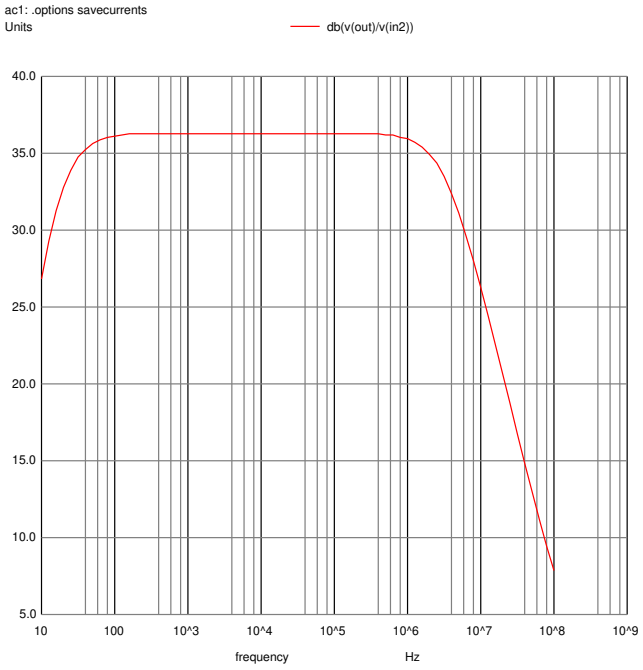


Figure 9: $v_o(f)/v_i(f)$ - Frequency Analysis

This gain is above zero, which means that the true gain value will actually be bellow zero because during the gain stage, the circuit acts as an inverting amp, which means that the signal will show a difference of 180 degrees in the phase, or basically the output signal will be symmetrical to the initial one. But the output stage acts like a non inverting amp, so the output signal will not change signal. Therefore the final output voltage will show a negative gain, but that won't matter in the hearing of the audio, what will be important is the absolute value. By analyzing the graph we see that in the pass-band area we have a gain of about 36 dB. That corresponds to a ratio of almost 65 in absolute value[2]. The exact value will be shown in Table 5, alongside the values of the bandwidth, lower and higher cut-off frequencies (in Hz).

Name	Value
gain	6.533673e+01
f1	2.119037e+01
f2	2.472595e+06
bandwidth	2.472574e+06

Table 5: Gain, lower and higher cut of frequencies and bandwidth

Finally we calculated the input and output impedance, both shown in the following table.

[2] $10^{\frac{36}{20}} = 63.096$

Input Impedance	Value [Ω]
Zin	843.46 + -125.344 j
Zin - Amplitude	852.723

(a) Input Impedance

Output Impedance	Value [Ω]
Zout	5.97291 + 0.254524 j
Zout - Amplitude	5.97833

(b) Output Impedance

Table 6: Input and Output Impedance

It would be ideal for the input impedance to have a very big value, much greater than the value of $Rs = 100\Omega$, as explained in the Theoretical Analysis. The obtained value of about 850Ω isn't that ideal, as it is only about 8.5 times bigger. But we weren't able to find better results without compromising the merit, so we decided to keep this impedance result.

Also the output impedance isn't much lower than 8Ω, which is not ideal. It would be better for the output impedance to be much smaller than 8Ω so that the major part of the signal wouldn't be lost. However we weren't able to achieve better values until the date of the assignment, so we accepted these values and focused on the merit. For this we also calculated the necessary values and obtained the following table. This will be better discussed in the conclusion.

	Value
cost	3.501168e+03
gain	6.533673e+01
f1	2.119037e+01
bandwidth	2.472574e+06
merit	2.177485e+03

Table 7: Merit.

4 Conclusion

To start this conclusion we will compare all the results we obtained in NGSpice and in Octave side by side.

Starting of with the Operating Point analyses:

Name	Value [A] or [V]
I_{B1}	0.0000327301
I_{C1}	0.0058488641
I_{E1}	0.0058815941
V_{E1}	1.1763188294
V_{O1}	7.9057951482
V_{CE}	6.7294763188
I_{E2}	0.0565700809
I_{C2}	0.0563222925
V_{O2}	8.6057951482

(a) Theoretical

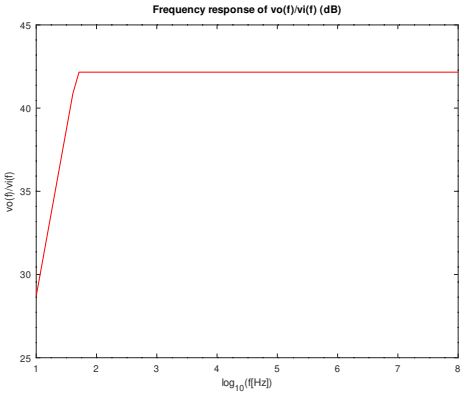
Name	Value [A] or [V]
@q1[ib]	3.230371e-05
@q1[ic]	5.910659e-03
-@q1[ie]	5.942963e-03
v(emit)	1.188593e+00
v(coll)	8.080741e+00
v(coll)-v(emit)	6.892148e+00
-@q2[ie]	5.225002e-02
@q2[ic]	5.193830e-02
v(emit2)	8.864999e+00

(b) Simulated

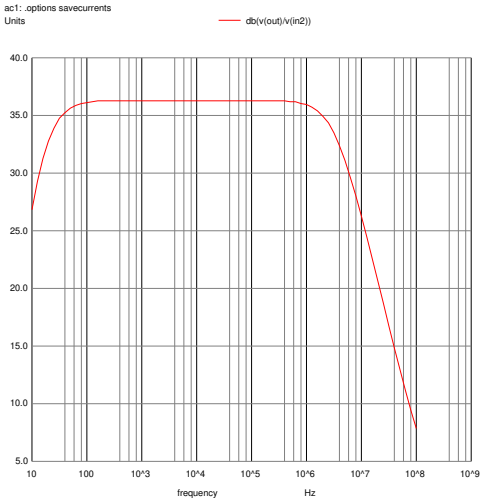
Table 8: Operating Point Analysis

These values show some differences, but those discrepancies are small enough, and we can associate them to the fact that NGSpice uses much more complex models than the one we

used, given that we simplified many components of the circuit and used a model that approximates the real circuit. But still the values are quite close, so the model used in the theoretical analysis, in what concerns to the operating point, is a good approximation of the real circuit.



(a) Octave



(b) NGSpice

Figure 10: Frequency analysis - $v_o(f)/v_i(f)$

It's worth noticing that the theoretical Gain Value was an absolute value of 128.24, whilst the simulated value was of 65.3367. These values are quite different, and this can be explained by the previous explanation of the use of different models. But this big error is also associated to resistances r_π and R_C. While we used constant values for all parameters for the theoretical analyses, the truth is these values change according to the frequency, and NGSpice's parameters take that into account, because NGSpice considers capacitors and inductors in the transistor model. The simplification of the theoretical model could have also led to getting a higher gain value in the theoretical analysis.

Also an obvious approximation we made was considering the gain behavior to be linear in the theoretical analysis for low frequencies, which isn't exactly true. Also the fact that we assumed the higher cut-off frequency to be ∞ is obviously not true, as we can see in the simulated plot.

After this, let's compare the values of the Input and Output Impedances of the complete circuit:

	Value [Ω]
Z_I	729.0208256575
Z_O	3.1469781727

Table 9: Input and Output Impendances - Theoretical

Input Impedance	**Value [Ω]**
Zin	843.46 + -125.344 j
Zin - Amplitude	852.723

(a) Input Impedance

Output Impedance	**Value [Ω]**
Zout	5.97291 + 0.254524 j
Zout - Amplitude	5.97833

(b) Output Impedance

Table 10: Input and Output Impedance - Simulated

These values are also quite different. As explained before, the used models were also different, which might have led to the discrepant results.

Finally, as we saw in Table 7, our final merit value was $M = 2177.485$ which came from a compromise between trying to get good gain and bandwidth values and a low cost.