Department of Electrical and Computer Engineering, UAH
CPE 323 – Introduction to Embedded Computer Systems
Quiz #5

1 (12)	2 (10)	Total (22)

1. (12 points) Circle the correct answer, true or false?

1.A (True | False) In MSP430's active mode clock signals MCLK is up and running, and SMCLK and ACLK are turned off.

1.B (True | False) In MSP430's active mode the main clock signal, MCLK, can be increased from the default clock (~ 1 MHz) from software.

1.C (True | False) TimerB operating in its UP mode counts up to the value stored in its CCR0.

1.D (True | False) TimerB can be configured to generate multiple pulse-with modulated signals with customizable duty cycle.

1.E (True | False) The MSP430's watchdog timer time interval can take any value from 1 to (2^{16}-1) source clock ticks.

1.F (True | False) DMA Controller can be used to transfer samples coming from the ADC12 to a buffer in RAM memory.

2. (10 points)

2.A. (2 points) The MSP430's watchdog timer operates in its interval mode and counts 8,192 clocks. How many interrupts it will generate if its source clock comes from 32,768 Hz ACLK?

__4____

2.B. (4 points) Describe configuration of TimerB that will generate a periodic signal that is 0.5 ms at a logic '0' and 1.5 ms at a logic '1'. Assume that the period of the source clock for TimerB is set to 1 microsecond, and capture and compare block 1 is used to generate the signal.

TimerB mode:__UP_____

CCR0:_____1,999_____

CCR1:_____ 499_____

CCR1 output mode:_set/reset_____

2.C (4 points). What is the operating time in days of a platform that draws 4 mA on average if it is powered with a two AA batteries with capacity of 2200 mAh?

OT = BT/Iavg = 2200/4 = 550 hours / 24 h = 22.91 days.