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CPE 324

## **Lab Report #8**

### **Temperature Sensor**

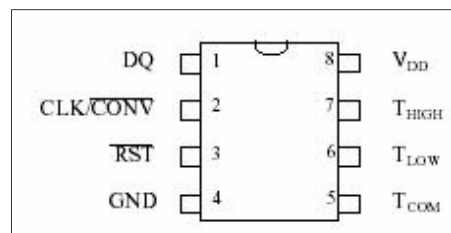


## Introduction

In this lab we operate with some level of real-world scenario by designing a single module to integrate with an existing set of IP written in a variety of formats. These modules will still operate and synthesize in the Quartus IDE, but will require some additional posturing to continue development as a normal Verilog project. We also look at some higher level peripheral communication from the FPGA package than previous labs where the system designed is contained on the DE2-115. Another aspect of working with the VHDL and separate temperature package is to simulate working in a team/workgroup environment, as laid out by the lab manual. By creating, simulating, integrating, synthesizing, and testing this lab with the supplied IP we will effectively operate with virtual coworkers.

## Theory and Analysis

Much of the analytic basis for this lab has been squared away via the initial set of modules in Verilog and VHDL we have to work with. Most of the communication theory boils down to the provided state machine which dictates the parsing of serial data between the DE2-115 and DS-1620.



Rather than use the T<sub>high</sub>, T<sub>low</sub>, or T<sub>com</sub> pins on the DS1620, we'll use the device in "three wire" mode where DQ handles input for commands and output for serial temperature data.

## Procedures

Procedure was followed as closely as possible from the lab manual, "Laboratory Assignment #8, Temperature Sensor". There was some confusion on integrating VHDL components into the project, but on the third attempt the instructions listed at the end of the manual worked to allow the project to synthesize.

## Results

The downloaded project operated in a reasonably precise manner, returning to the same value after being heated up by convection. The measured temperature was not accurate, however, as the display read roughly 1-2% lower than the real value. Simulation of the program appeared to return correct values, but a intricacy of the state machine may still be at fault for the discrepancy.

Flow Summary	
Flow Status	Successful - Fri Apr 17 13:38:51 2015
Quartus II 32-bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Full Version
Revision Name	lab8
Top-level Entity Name	lab8
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	41 / 114,480 ( < 1 % )
Total combinational functions	41 / 114,480 ( < 1 % )
Dedicated logic registers	8 / 114,480 ( < 1 % )
Total registers	8
Total pins	34 / 529 ( 6 % )
Total virtual pins	0
Total memory bits	0 / 3,981,312 ( 0 % )
Embedded Multiplier 9-bit elements	0 / 532 ( 0 % )
Total PLLs	0 / 4 ( 0 % )

```

#
# Stimulus
# [0] is LSB
# SUB_ADD: 0=add (A+B), 1=subtract (A-B)
# Library: cycloneive_ver
#
force CLR 1 0, 0 100
force DQ_IN 1 0, 0 40 -repeat 80
force CLK_IN 0 0, 1 20 -repeat 40
run 4000

```

ps	delta	/DS1620_INTERFACE/CLR	/DS1620_INTERFACE/TRI_EN	/DS1620_INTERFACE/CLK_IN	/DS1620_INTERFACE/DQ_IN	/DS1620_INTERFACE/TEMP	/DS1620_INTERFACE/DQ_OUT	/DS1620_INTERFACE/CLK_OUT	/DS1620_INTERFACE/count	/DS1620_INTERFACE/RST	/DS1620_INTERFACE/dq_out_buff
0	+0	St1	St0	xxxxxxxx	x x	x St1	x 00000	000000000			
20	+0	St1	St1	000000000	1 x	x St1	x 00001	000000000			
40	+0	St1	St0	000000000	1 x	x St0	x 00001	000000000			
60	+0	St1	St1	000000000	1 x	x St0	x 00001	000000000			
80	+0	St1	St0	000000000	1 x	x St1	x 00001	000000000			
100	+0	St0	St1	000000000	1 1	0 St1	1 00010	000000000			
120	+0	St0	St0	000000000	0 1	0 St0	1 00010	000000000			
140	+0	St0	St1	000000000	1 1	1 St0	0 00011	000000000			
160	+0	St0	St0	000000000	0 1	1 St1	0 00011	000000000			
180	+0	St0	St1	000000000	1 1	1 St1	1 00100	000000000			
200	+0	St0	St0	000000000	0 1	1 St0	1 00100	000000000			
220	+0	St0	St1	000000000	1 1	1 St0	0 00101	000000000			
240	+0	St0	St0	000000000	0 1	1 St1	0 00101	000000000			
260	+0	St0	St1	000000000	1 1	1 St1	1 00110	000000000			
280	+0	St0	St0	000000000	0 1	1 St0	1 00110	000000000			
300	+0	St0	St1	000000000	1 1	1 St0	0 00111	000000000			
320	+0	St0	St0	000000000	0 1	1 St1	0 00111	000000000			
340	+0	St0	St1	000000000	1 1	1 St1	1 01000	000000000			
360	+0	St0	St0	000000000	0 1	1 St0	1 01000	000000000			
380	+0	St0	St1	000000000	1 1	1 St0	0 01001	000000000			
400	+0	St0	St0	000000000	0 1	1 St1	0 01001	000000000			
420	+0	St0	St1	000000000	1 1	1 St1	1 01010	000000000			
440	+0	St0	St0	000000000	0 1	1 St0	1 01010	000000000			
460	+0	St0	St1	000000000	1 1	1 St0	1 01011	000000000			
480	+0	St0	St0	000000000	0 1	1 St1	1 01011	000000000			
500	+0	St0	St1	000000000	1 1	0 St1	1 01100	000000001			
520	+0	St0	St0	000000000	0 1	0 St0	1 01100	000000001			
540	+0	St0	St1	000000000	1 1	0 St0	1 01101	000000010			
560	+0	St0	St0	000000000	0 1	0 St1	1 01101	000000010			
580	+0	St0	St1	000000000	1 1	0 St1	1 01110	000000101			
600	+0	St0	St0	000000000	0 1	0 St0	1 01110	000000101			
620	+0	St0	St1	000000000	1 1	0 St0	1 01111	000001010			
640	+0	St0	St0	000000000	0 1	0 St1	1 01111	000001010			
660	+0	St0	St1	000000000	1 1	0 St1	1 10000	000010101			
680	+0	St0	St0	000000000	0 1	0 St0	1 10000	000010101			
700	+0	St0	St1	000000000	1 1	0 St0	1 10001	000101010			
720	+0	St0	St0	000000000	0 1	0 St1	1 10001	000101010			
740	+0	St0	St1	000000000	1 1	0 St1	1 10010	010101010			
760	+0	St0	St0	000000000	0 1	0 St0	1 10010	010101010			
780	+0	St0	St1	000000000	1 1	0 St0	1 10011	010101010			
800	+0	St0	St0	000000000	1 1	0 St1	1 10011	010101010			
820	+0	St0	St1	101010110	1 1	0 St1	1 10100	010101010			
840	+0	St0	St0	101010110	1 1	0 St0	1 10100	010101010			
860	+0	St0	St1	101010110	1 0	0 St0	1 10101	010101010			
880	+0	St0	St0	101010110	1 0	0 St1	1 10101	010101010			
900	+0	St0	St1	101010110	1 0	0 St1	1 10110	010101010			

Simulation output shows the system correctly processing DQ input and providing parsed temperature output. Other factors in the physical implementation may include the breadboard connections, true voltage supplied, and DS1620 quality/condition.

### **Conclusion and Discussion**

Implementing the DS1620 has been one of the more challenging labs for this class thus far, as working with other modules and VHDL required more time to investigate the language's syntax and overall project structure. It's the belief of this lab member that a more appropriate or well designed Verilog module can be made for the lab's DS1620\_INTERFACE, but time and resource limitations had the item left at its current state of completeness. Operation of the DS1620 was taken from the Dallas Semiconductor datasheet, "DS1620 Digital Thermometer and Thermostat". The IC operates on a 3-wire serial interface in which the temperature, when requested, is converted into a 9-bit value within one second and sent as a reply over the DQ pin. This is a new method of serial communication than discussed in previous classes, though it does appear to model SPI in several views.