The University of Alabama in Huntsville
ECE Department
Homework Assignments
CPE 431/531 01/91/92
Fall 2015
Homework #3 Solution

3.21(10), 3.22(10) use 0xD780 0000, 3.23(10) using 279.4375, 3.24(10) using 279.4375, 3.28(20), 4.3.1(10), 4.3.2(10), 4.7.4(10), 4.7.5(10)

3.21 If the bit pattern 0x0C00 0000 is placed into the Instruction Register, what MIPS instruction will be executed?

0x0C00 0000 = 0000 1100 0000 0000 0000 0000 0000 0000
opcode – 000011 j-type instruction, jal 0
$ra PC of the instruction + 8
PC PC + 8[31..28] & 0000 0000 0000 0000 0000 0000 0000

3.22 What decimal number does the bit pattern 0xD780 0000 represent if it is a floating point number? Use the IEE 754 standard.

0xD780 0000 = 1101 0111 1000 0000 0000 0000 0000 0000
S = 1, number is negative
EXP + BIAS = 1010 1111 = 175, EXP = 175 -127 = 48
Fraction = 0.0000 0000 0000 0000 0000 000
Number is -(1.0 x2^{48}) = -281,474,976,710,656

3.23 Write down the binary representation of the decimal number 279.4375 assuming the IEEE 754 single precision format.

```
          0   1              x2    0.4375
/2        1   0              x2    0.8750    0
/2        2   0              x2    1.750     1
/2        4   0              x2    1.50      1
/2        8   1              x2    1.00      1
/2       17   0
/2       34   1
/2       69   1
/2      139   1
/2      279
```

100010111.0111 = 1.0001 0111 0111 x 2^{8}
S = 0, EXP + BIAS = 8 + 127 = 135 = 1000 0111
Fraction = 0001 0111 0111
0100 0011 1000 1011 1011 1000 0000 0000 = 0x438B B800

3.24 Write down the binary representation of the decimal number 279.4375 assuming the IEEE 754 double precision format.

100010111.0111 = 1.0001 0111 0111 x 2^8
S = 0, EXP + BIAS = 8 + 1023 = 1031 = 1000 0000 111
Fraction = 0001 0111 0111
0100 0000 0111 0001 0111 0111 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 = 0x4071 7700 0000 0000

3.28 The Hewlett-Packard 2114, 2115, and 2116 used a format with the leftmost 16 bits being the fraction stored in two's complement format, followed by another 16-bit field which had the leftmost 8 bits as an extension of the fraction (making the fraction 24 bits long), and the rightmost 8 bits representing the exponent. However, in an interesting twist, the exponent was stored in sign-magnitude format with the sign bit on the far right! Write down the bit pattern to represent -1.5625 x 10^{-1} assuming this format. No hidden 1 is used. Comment on how the range and accuracy of this 32-bit pattern compares to the IEEE 754 single precision standard.

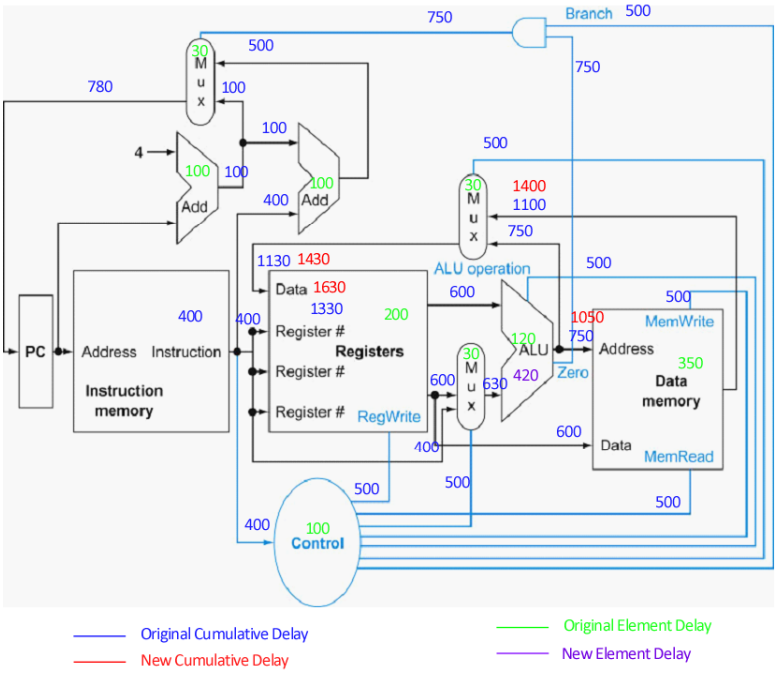
The number is negative, S = 1, 1.5625 × 10^{-1} = 0.00101 = 0.101 × 2^{-2}
Exponent : 0000 0101
Fraction 2s comp of 0101 0000 0000 0000 0000 0000 =
1011 0000 0000 0000 0000 0000 0000
All together: 1011 0000 0000 0000 0000 0000 0000 0101 = 0xB000 0005

The range of numbers for single precision is from -1.111 1111 1111 1111 1111 1111 × 2^{127} to 1.111 1111 1111 1111 1111 1111 × 2^{127}, while the range for Hewlett Packard is -1 × 2^{127} to 0111 1111 1111 1111 1111 1111 × 2^{127-24} = 0111 1111 1111 1111 1111 1111 × 2^{103}
The smallest number that can be represented in single precision is 1.0 × 2^{-126} while the smallest number that can be represented in Hewlett Packard is 1.0 × $2^{-127-24}$ = 1.0 × 2^{-151}

4.3 When processor designers consider a possible improvement to the processor datapath, the decision usually depends on the cost/performance trade-off. In the following three problems, assume that we are starting with a datapath from Figure 4.2, where I Mem, Add, Mux, ALU, Regs, D Mem, and Control blocks have latencies of 400 ps, 100 ps, 30 ps, 120 ps, 200 ps, 350 ps, and 100 ps, respectively, and costs of 1000, 30, 10, 100, 200, 2000, and 500, respectively.

Consider the addition of a multiplier to the ALU. This addition will add 300 ps to the latency of the ALU and will add a cost of 600 to the ALU. The result will be 5% fewer instructions executed since we wil no longer need to emulate the MUL instruction.

4.3.1 What is the clock cycle time with and without this improvement?



The clock cycle without this improvement is 1330 ps and the clock cycle with this improvement is 1630 ps.

4.3.2 What is the speedup achieved by adding this improvement?

$$\frac{P_{new}}{P_{old}} = \frac{ET_{old}}{ET_{new}}$$

$$= \frac{IC_{old} * CPI_{old} * CT_{old}}{IC_{new} * CPI_{old} * CT_{new}} = \frac{IC_{old} * 1 * 1330\,ps}{0.95IC_{old} * 1 * 1630\,ps} = 0.86$$

4.7 In this exercise we examine in detail how an instruction is executed in a single-cycle datapath. Problems in this exercise refer to a clock cycle in which the processor fetches the following instruction word:

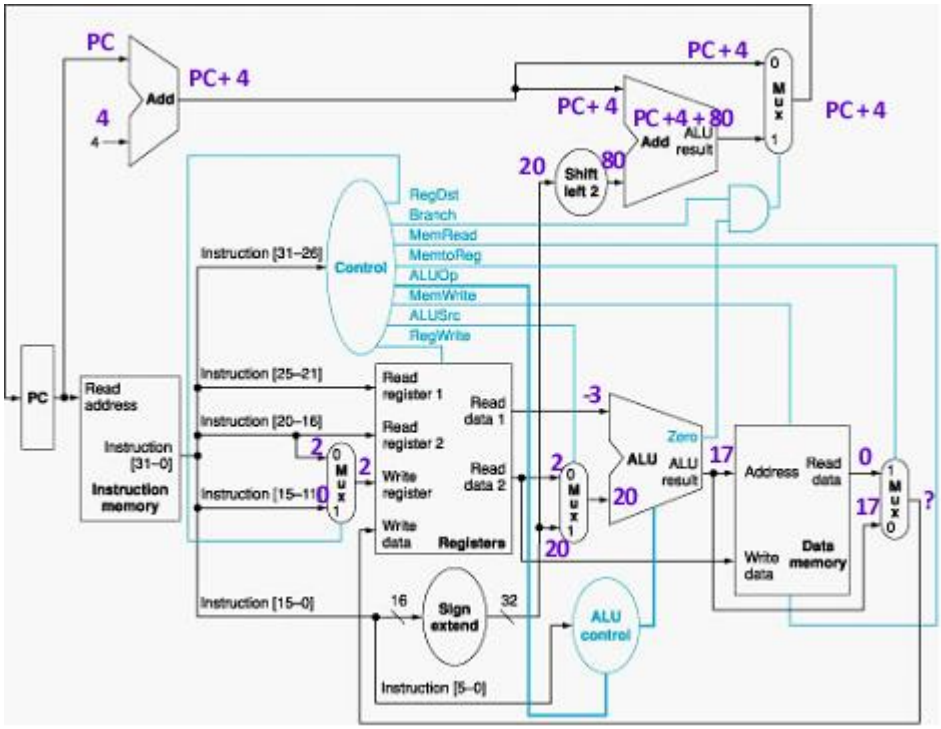
1010 1100 0110 0010 0000 0000 0001 0100

Assume that data memory is all zeros and that the processor's registers have the following values at the beginning of the cycle in which the above instruction word is fetched.

r0	r1	r2	r3	r4	r5	r6	r8	r12	r31
0	-1	2	-3	-4	10	6	8	2	-16

4.7.4 For each Mux, show the value of its data output during the execution of this instruction and these register values.

Opcode = 101011 = 43 = sw, rs = 00011 = 3 or $v1, rt = 00010 = 2 or $v0, offset = 0000 0000 0001 0100 = 20



4.7.5 For the ALU and the two add units, what are their data input values?

See figure for 4.7.4.