Department of Electrical and Computer Engineering
University of Alabama in Huntsville
CPE 323 – Introduction to Embedded Computer Systems
Quiz #4: Keys

1 (10)	2 (12)	Total (22)

1. (10 points) Circle the correct answer, true or false, or fill in the blank space.

A. (2 points) (True | False) I^2C is a serial synchronous communication protocol relying on a two-wire bus connecting multiple devices.

B. (2 points) (True | False) SPI (Serial Peripheral Interface) requires the total of two wires running between the master and a slave. (False – requires 3 or 4 wires, plus common ground).

C. (2 points) (True | False) UART type of serial connection requires a shared clock between the receiver and transmitter. (False – the UART is asynchronous link, no shared clock between Ran T).

D. (2 points) (True | False) UART message starts with a START bit which a logic '0'.

E. (2 points) A serial communication interface is sending a character '0' in UART mode (ascii('0')=0x30). It is configured as follows: 8-bit data, a parity bit (odd), 1 stop bit. How many bits are sent and what is the value of the parity bit?

N = _11_(8 + 1(start)+1(parity)+1(stop)
P =__'1'_____

2. (12 points)

A. (2 points) (True | False) The start of an ADC12 analog-to-digital conversion can ONLY be initiated explicitly from software (e.g., setting a start bit in the ADC12 control register), i.e., it cannot be started using hardware triggers (e.g., from timers). (False – a trigger can come from a Timer CC block).

B. (2 points) (True | False) ADC12 can be used to sample multiple analog signals by using an input multiplexer to select a desirable input. (True - Sequence of channels mode).

C. (2 points) (True | False) DAC12 is configured in the 8-bit mode with Vref+=2.5 V and Vref-=0, no scaling. If DAC12_DATA0 = 100, the output analog signal is ~0.98 V.

D. (4 points) An analog-to-digital conversion of an input signal of 1.0 V using 12-bit ADC12 with Vref+=3V and Vref-=0V. What decimal value will be read from the ADC buffers at the end of conversion?

*4095*1/(3-0) = 1365.*

E (bonus, 2 points). If you have a clock speed of 2,097,152 Hz and a waveform comprised of 1024 samples per period, how often (in clock cycles) must you update the DAC output value in order to achieve a waveform output frequency of 40 Hz?

*40*1024 = 40,960 samples per second => 2,097,152 /40,960 = 51,2 clock cycles.*