Lab # 04
Implement the Digital to Analog Converter Using Op-Amp

Purpose

The goal of this laboratory is to explore how an Op-Amp and binary resistive ladder network can be used to construct a simple Digital to Analog (D/A) Converter. The concepts of step size, maximum output range, resolution, and accuracy will also be introduced.

Theoretical Background

A Digital to Analog Converter translates digital information, in the form of discrete bits, into equivalent analog information. A resistive binary ladder can be used as the basis for a Digital to Analog Converter. Additional circuitry is required for a standalone design. However, we will not pursue to discuss that circuitry here. Rather we will study and design the main ladder circuit in conjunction with an Op-Amp, which is the main construct of the D/A Converter.

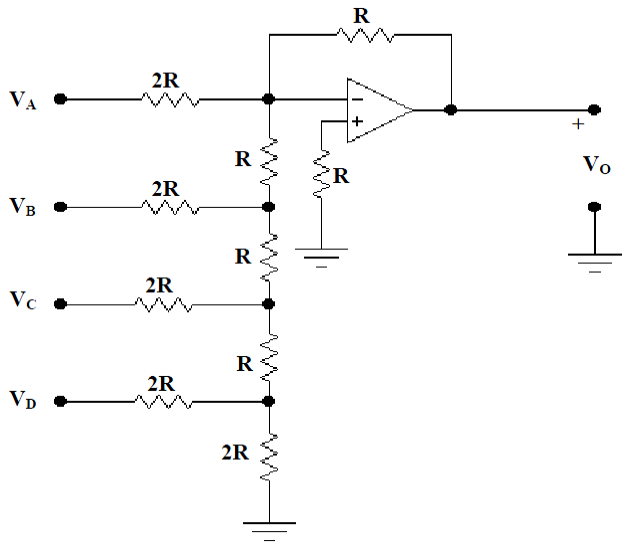


Figure 4.1

In Figure 4.1, a binary resistive ladder circuit is connected to the negative terminal of the operational amplifier. A resistance R has been added to the positive input to null any stray currents at the negative input. This is the basic design of a simple D/A Converter. Inorder to describe how the circuit converts a digital input into an analog output, we begin by finding the Op-Amp output V_O. To do so a step by step Thevenin equivalent approach is used. Let the output due to only input V_D be defined as V_{OD} as shown in Figure 4.2.

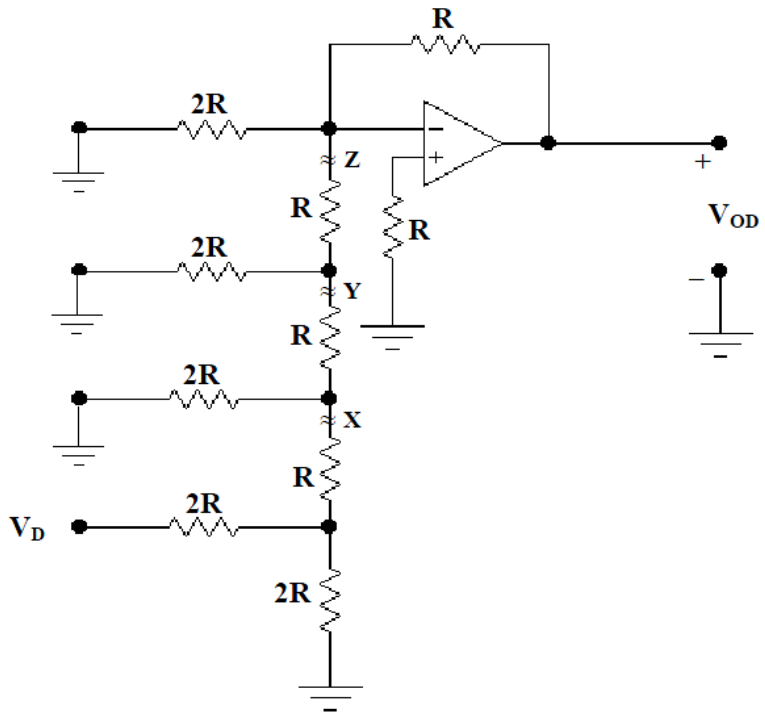


Figure 4.2

First cut the circuit in Figure 4.2 along the jagged line X. This will reduce the circuit to that shown in Figure 4.3.

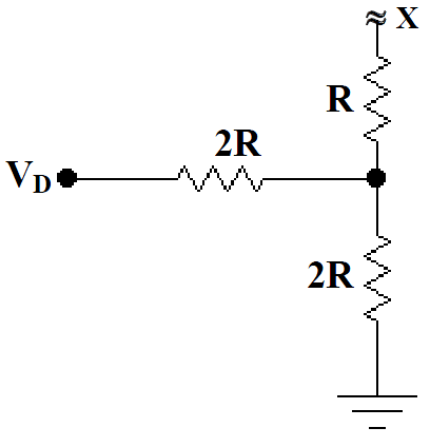


Figure 4.3

Now applying Thevenin's Theorem between terminal X and ground in Figure 4.3 leads to the Thevenin equivalent resistance of

$$R_{TH} = 2R||2R + R = 2R$$

The Thevenin voltage is

$$V_{TH} = \frac{V_D}{2R+2R} 2R$$

$$= \frac{V_D}{2}$$

The Thevenin equivalent drawing is shown in Figure 4.4

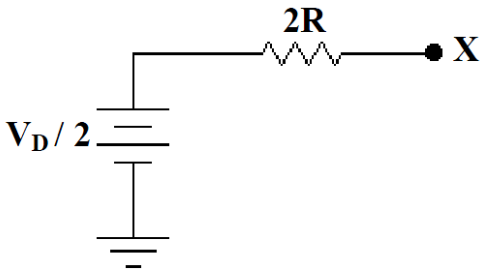


Figure 4.4

Using the same approach at the jagged line denoted by Y, you could cut and redraw the circuit as shown in Figure 4.5.

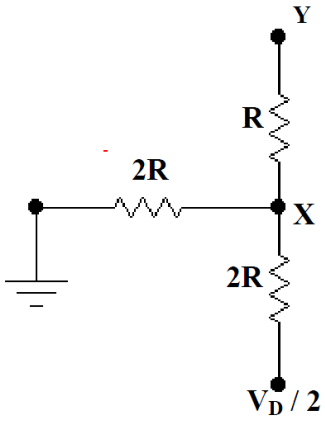


Figure 4.5

Now, applying the same steps as before leads to the Thevenin equivalent circuit shown in Figure 4.6. Where now the Thevenin equivalent resistance is

RTH = 2R||2R + R = = 2R

And the Thevenin voltage is given by

$$V_{TH} = \frac{V_D/2}{2R+2R}2R$$

$$= \frac{V_D}{4}$$

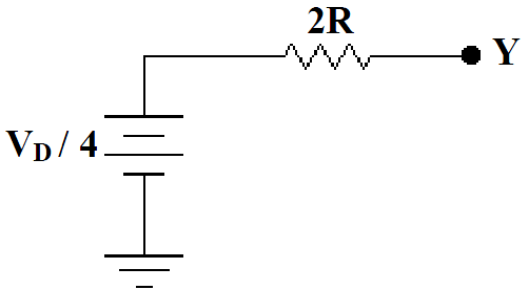


Figure 4.6

Apply the same procedure one more time at point Z to get the circuit shown in Figure 4.7.

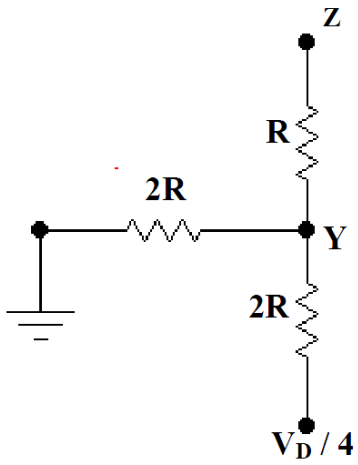


Figure 4.7

The new Thevenin equivalent circuit is shown in Figure 4.8 and the Thevenin equivalent resistance is

RTH = 2R||2R + R = 2R

The final Thevenin voltage for the input VD is

$$V_{TH} = \frac{V_D/4}{2R+2R}2R$$

$$= \frac{V_D}{8}$$

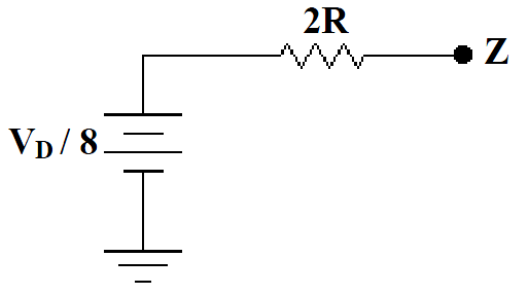


Figure 4.8

Next the circuit is reassembled and the final equivalent form, for input V_D, is shown in Figure 4.9. Note that it is not necessary to include the resistor 2R, originally connected to V_A which is now at ground, because one terminal of the resistor is at ground and the other terminal at point Z is at virtual ground.

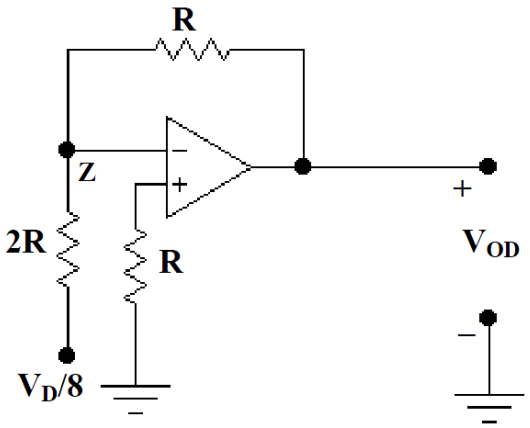


Figure 4.9

The output voltage contributed by the input V_D can now be written as

$$V_{OD} = -\frac{R}{2R}\frac{V_D}{8}$$

$$= -\frac{V_D}{16}$$

Similarly, the rest of the outputs can be found by repeating the procedures at each input. The resulting equations are

For input V_A: $V_{OA} = -\frac{V_A}{2}$. (With V_B, V_C, and V_D at ground)

For input V_B: $V_{OB} = -\frac{V_B}{4}$. (With V_A, V_C, and V_D at ground)

For input V_C: $V_{OC} = -\frac{V_C}{8}$. (With V_A, V_B, and V_D at ground)

By applying superposition the final output (V_O), which results from all four inputs, can be written as

$$V_O = V_{OA} + V_{OB} + V_{OC} + V_{OD}$$

$$V_O = -(\frac{V_A}{2} + \frac{V_B}{4} + \frac{V_C}{8} + \frac{V_D}{16})$$

Now so that the output can be described, the input values must be defined and their significance in the D/A configuration must be determined. If we choose the same level for all input voltages, which will be the actual case in this laboratory, it is evident that the maximum output voltage contribution will be from the input at V_A. Because V_A contributes the maximum output, it is defined as the Most Significant Bit or MSB. Similarly by inspection, it can be seen that V_D represents the Least Significant Bit or LSB making the smallest voltage contribution. The bit order can now be defined from MSB to LSB as V_A, V_B, V_C, and V_D in that order. By choosing the HIGH inputs to be represented by a single voltage, say 5V, and the LOW inputs all equal to a single voltage, say 0V, we can further define the system as follows on the next page.

The total number of possible inputs producing a unique output can be found using the following equation.

Num_ Permutations = 2^N

N = Number of inputs or Bits

For example, one possible input of 1 0 1 0, where 1 represents HIGH and 0 represents LOW, will produce the unique output voltage of

$V_O = -(5/2 + 0/4 + 5/8 + 0/16) = -2 * 5/8$ V

The number of steps associated with this N Bit system, or the number of voltages increases needed to go from zero to the maximum output voltage considering all possible permutations, can be found using

$$Num\_Steps = 2^N - 1$$

And the step size, or the output voltage increase due to adding 1 LSB, is defined as

$$Step\_Size = \frac{V_{IN}}{2^N}$$

Where VIN is defined to be the voltage contribution of the Least Significant Bit at the input. Once the number of steps and step size have been determined, the maximum output voltage is found from

$$Max\_Output = Num\_Steps \times Step\_Size$$

The D/A resolution can be defined as:

$$\mathrm{Res} = \frac{Step\_Size}{2}$$

The accuracy of the D/A output is usually described by a percent error, which describes the reliability of the device giving the expected output value. To calculate the percent error the following equation is used.

$$Percent\_Error = \frac{V_{O\_Expected} - V_{O\_Measured}}{V_{O\_Expected}} \times 100\%$$

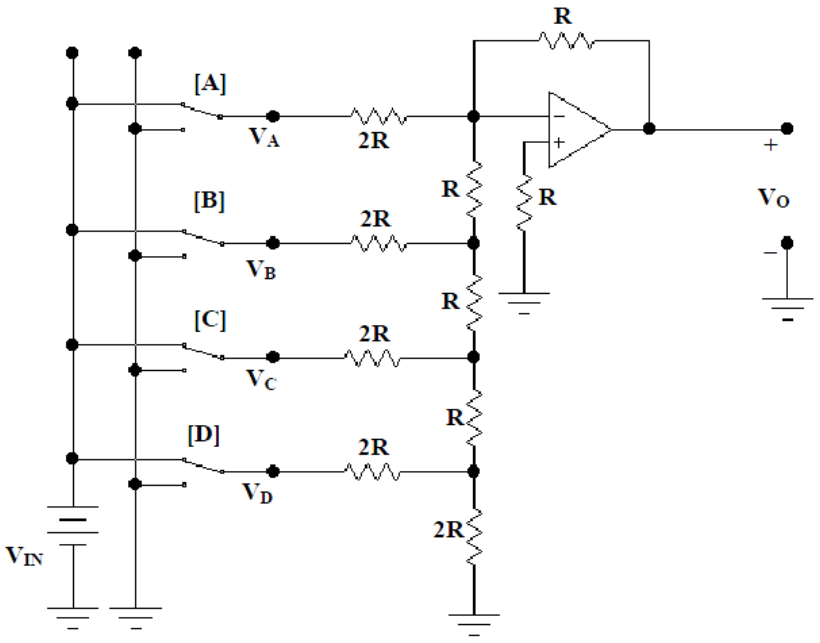


Figure 4.10

Simulation

For the simulation section define V_{IN} = 5 V and R = 1K Ohm. Draw the circuit as shown in Figure 4.1 using Electronics Workbench.

Assume ON is equivalent to Logic '1', and OFF is equivalent to Logic '0'.

Fill up Table 1 to produce all possible input sets. Measure V_O by using the virtual DC Voltmeter.

- Plot output V_O vs. input.

Laboratory Procedure

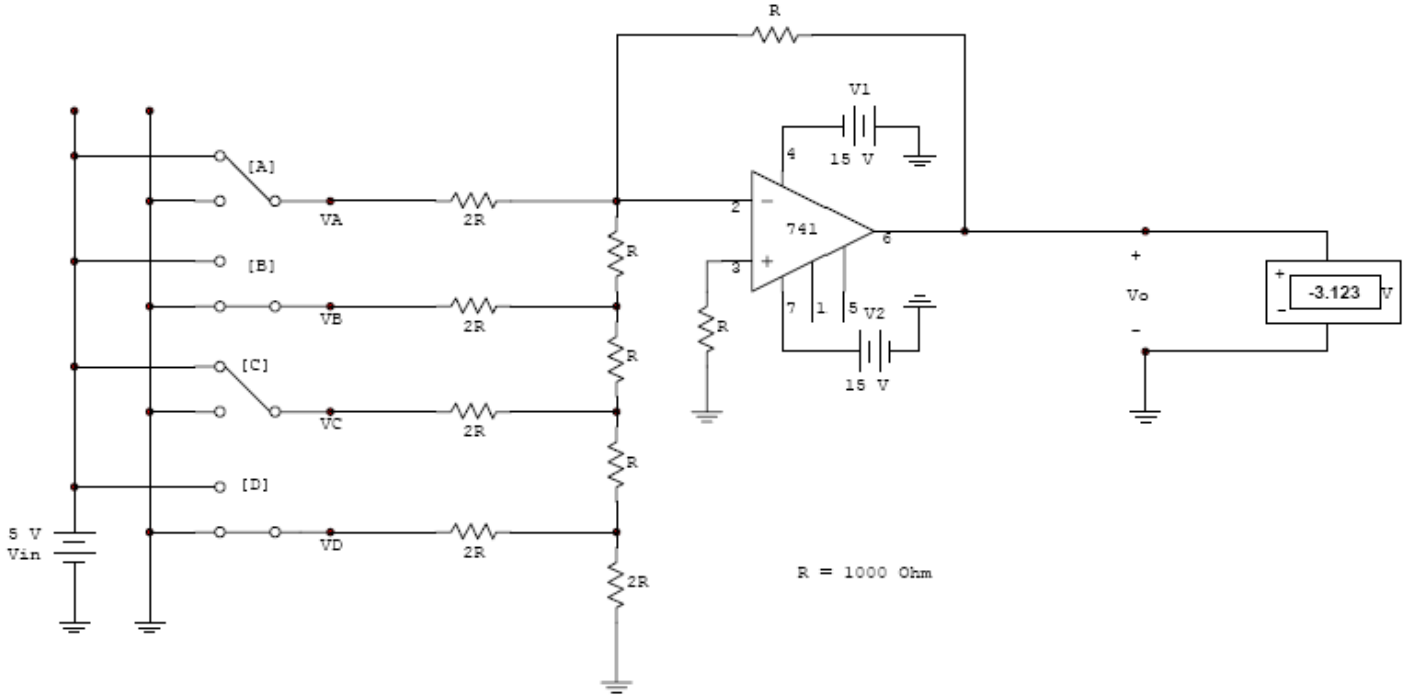
NOTE: The outputs of the trainer board are not **5 volts**!!!!

- Repeat all the steps from simulation and build the circuit as shown in Figure 4.10.
- Plot output V_O vs. input.

One exemplary result is shown below for information purpose ONLY.

Table 1

	V_A	V_B	V_C	V_D	V_O (V)
0	0	0	0	0	0.002
1	0	0	0	1	-0.310
2	0	0	1	0	-0.623
3	0	0	1	1	-0.935
4	0	1	0	0	-1.248
5	0	1	0	1	-1.560
6	0	1	1	0	-1.873
7	0	1	1	1	-2.185
8	1	0	0	0	-2.498
9	1	0	0	1	-2.810
10	1	0	1	0	-3.123
11	1	0	1	1	-3.435
12	1	1	0	0	-3.748
13	1	1	0	1	-4.060
14	1	1	1	0	-4.373
15	1	1	1	1	-4.685



**You need to note down the outputs for every other inputs (0000-1111).

Here, the input is:
VA=1, VB=0, VC=1, VD=0