CPE/EE 422/522 **EXAM I** **Name** KEY

Class _____

Spring Semester 2012

Work should be performed systematically and neatly with the final answer being underlined. This exam is closed book, closed notes, closed neighbor. Allowable items on desk include: exam, data manual, pencils, straight edge, and calculator. All other items must be removed from student's desk. Students have approximately 90 minutes (1 1/3 hours) to complete this exam. Best wishes!

1. [3 points] What is the primary difference between sequential logic and combinational logic?

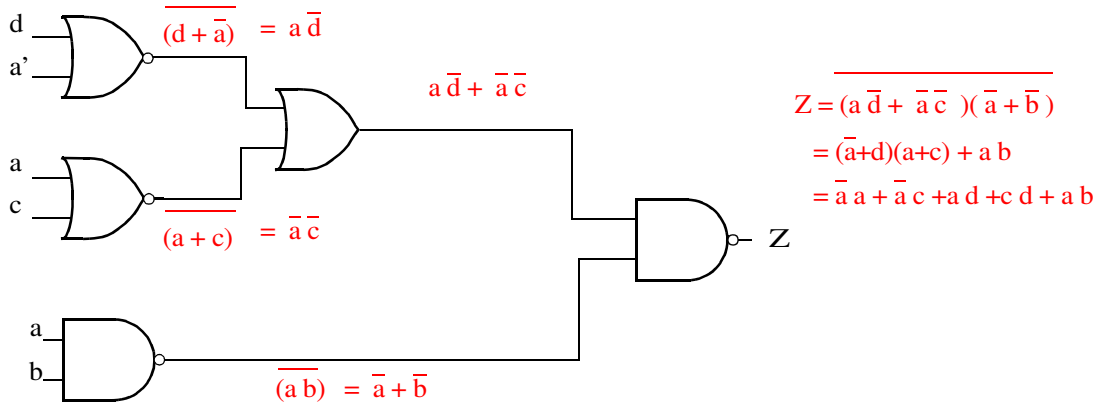
In combinational logic, the outputs depend only on the current logic vlues of the set of inputs. In sequential logic, the outputs depend upon both the current values of the inputs and previous input values. Sequential logic has memory and combination logic does not.

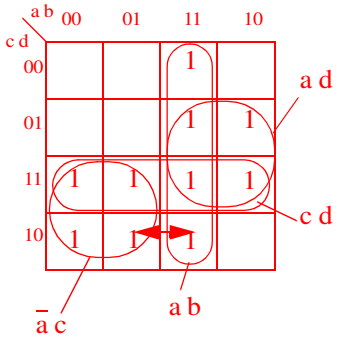
2. [12 points] In general, what are static hazards in a combinational network?

A hazard is an unwanted switching transient that appear on the output of a combinational network. These transients are caused by different delay paths from input to the outputs. Static hazards the output momentarily goes to the incorrect value when an input changes when it should remain constant.

For the network shown below, find any/all static 1-hazards. For any 1-hazard found specify the conditions which will cause the hazard to appear at the output (i.e. specify the logic values of the variables which are constant and the variable which is changing).

SAME PROBLEM AS 1.7 of HW

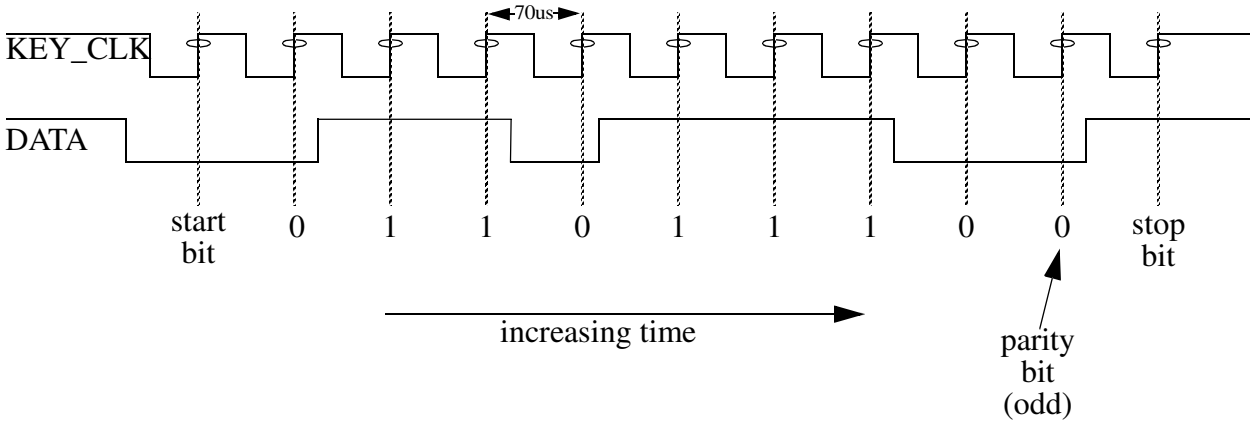




One Hazard Exists
a changes
b=1,c=1,d=0

8. [10 points] Laboratory inspired problem: Design a logic circuit that will continuously output the last byte of data that is set to it from a PS-2 keyboard when it is configured in the manner that was shown in part 1 of lab #2. The inputs to this circuit are the KEY_CLK and DATA lines which are each one bit wide. The output from this circuit should simply be the last keyboard code byte that was sent from the keyboard -- not the seven segment value that drives the hexadecimal display as in the lab. The following is a brief description of the base PS-2 protocol:

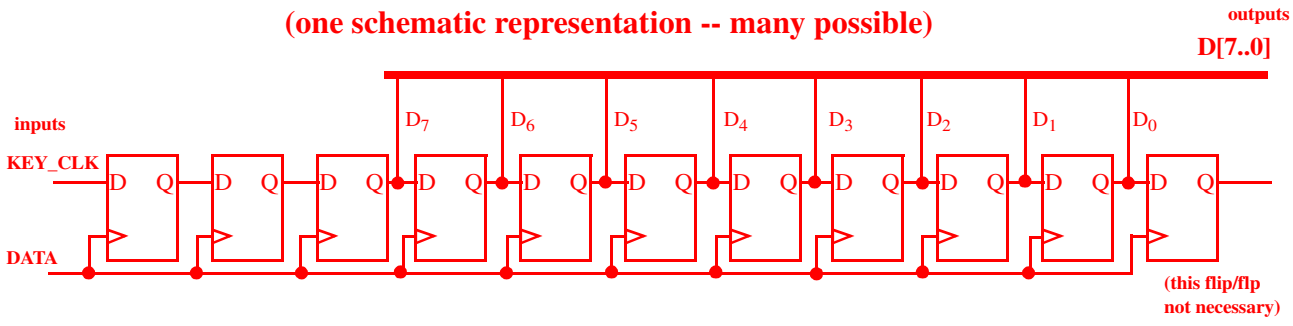
Each byte that is sent from the keyboard utilizes the keyboard clock and data lines, which are labeled, KEY_CLK and DATA, respectively, in the manner shown in the figure. Normal operation is for each key pressed the keyboard will send each byte in the make/break byte sequence across the data line at a data transfer rate of approximately 14285 bits per second. It does this by first forcing the DATA line low to create a start bit and then initiating the keyboard clock sequence by first forcing the KEY_CLK line low for one half clock cycle. Information is then sent from the keyboard, with each bit being valid at the leading edge of each clock pulse. First the start bit is sent, then eight data bits (least significant bit first), then a parity bit, and then a stop bit. After which the DATA and KEY_CLK lines are returned to the inactive state until the next byte is sent. The figure illustrates the waveform that will appear when the keyboard sends out the value 76 hexadecimal (which corresponds to the last byte of the make/break code for the escape key).



Example serial pattern for final make/break code for the Escape Key

NOTE: Either schematic or VHDL implementations are acceptable.

(one schematic representation -- many possible)



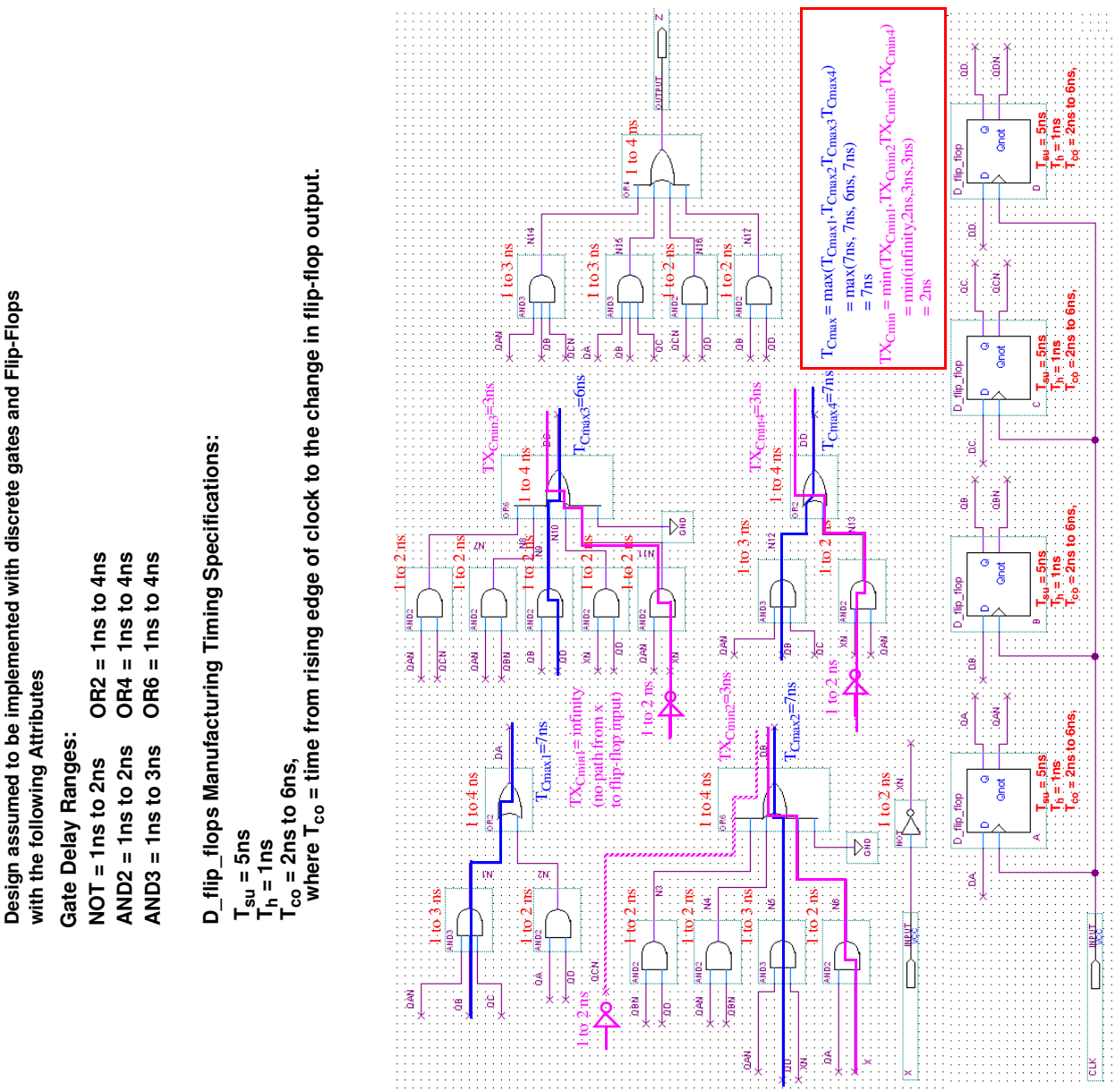
9. [15 points] In the following VHDL model fragment (which corresponds to a portion of the architecture section of a VHDL file) A, B, C, and D are all integers that have a value of 0 at time = 10ns. If E changes from '0' to '1' at time 20 ns, specify the times (s) at which each signal will change and the value to which it will change. List these changes in chronological order. List any delta delays as a separate entry.

```
P1: process
    begin
       wait on E;
       A <= transport 2 after 5 ns;
       B <= A + 2;
       wait for 0 ns;
       A <= transport A + 5 after 5 ns;
       B <= B + 1;
     end process P1;

P2: process(B)
    begin
       C <= B after 5 ns;
    end process P2;
D <= B after 10 ns;
```

Time	A	B	C	D	E
10 ns	0	0	0	0	0
20 ns	0	0	0	0	1
20 ns + Δ	0	2	0	0	1
20 ns + 2Δ	0	3	0	0	1
25 ns	5	3	3	0	1
30 ns	5	3	3	3	1

10.[10 points] For the synchronous sequential network shown below, determine the following:.

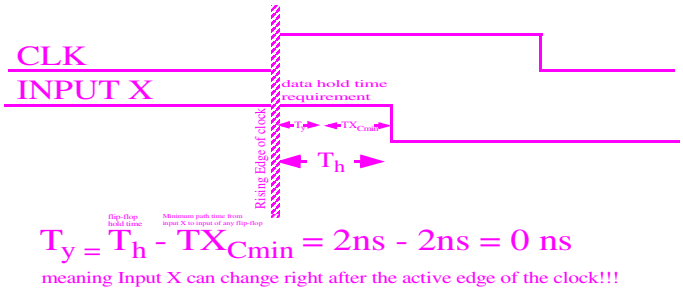


a) What is the maximum clock frequency for proper operation of the network if input X is driven in the appropriate manner by the external circuitry?

$T_{min} = T_{su} + T_{Cmax} + T_{co(max)} = 5ns + 7ns + 6ns = 18ns$

$f_{max} = 1/T_{min} = 1/18ns = 55.5Mhz$

b) What is the earliest time <u>after</u> the rising clock edge that input X is allowed to change?



$T_y = T_h - TX_{Cmin} = 2ns - 2ns = 0\ ns$

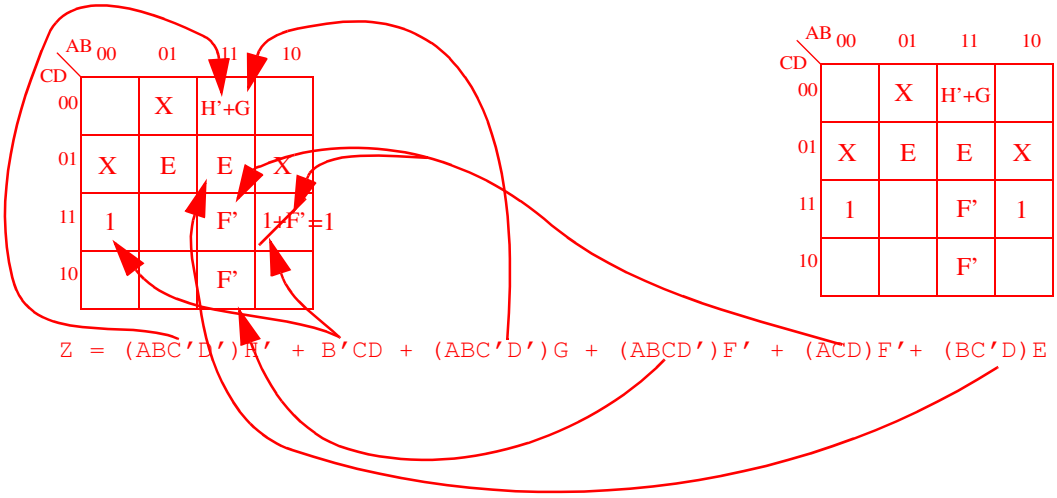
meaning Input X can change right after the active edge of the clock!!!

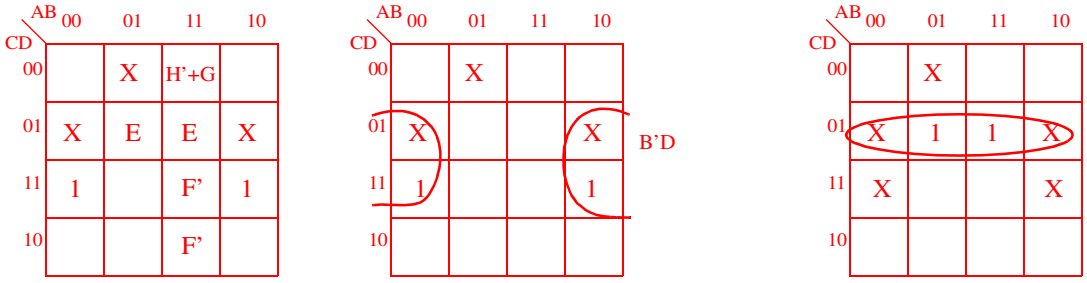
11. [9 points] For the Boolean function shown below find the minimum <u>sum of products (SOP)</u> using a four-variable map with map-entered variables. ABCD represents the state of a control circuit. Assume that the circuit can never be in state 0001, 0100, or 1001.

Z = ABC'D'H' + B'CD + ABC'D'G + ABCD'F' + ACDF'+ BC'DE

Same as Problem 1.3 of HW

Using variables ABCD for K map and variables EFG as map-entered variables.



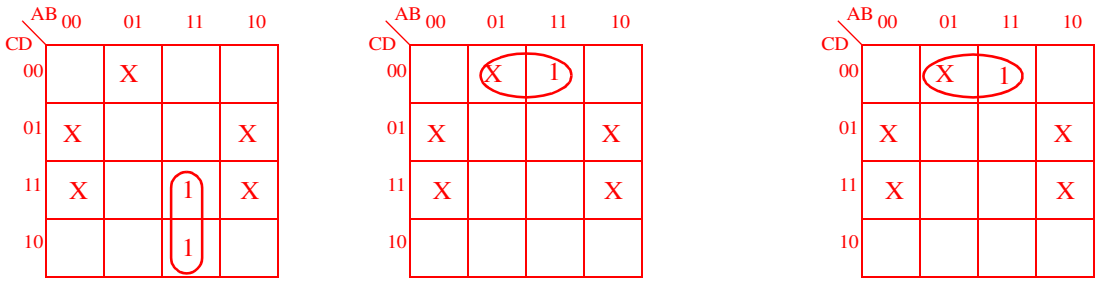


Turn all map-entered variables off
(make them or complements false on map)
E=0, F'=0, H'=0, G=0

$MS_0 = B'D$

E=1, F'=0, H'=0, G=0

$MS_1 = C'D$



E=0 F'=1, H'=0, G=0

$MS_2 = ABC$

E=0 F'=0 H'=1 G=0

$MS_3 = BC'D'$

E=0 F'=0 H'=0 G=1

$MS_4 = BC'D'$

$$Z = MS_0 + EMS_1 + F'MS_2 + H'MS_3 + GMS_4$$
$$= B'D + EC'D + F'ABC + H'BC'D' + GBC'D'$$

12. [8 points] For the state table shown below if we are using discrete logic and desire to employ the minimum number of flip/flops to represent our states,

Current State	Next State		Output
	X=0	X=1	
S_0	S_1	S_2	0
S_1	S_3	S_4	1
S_2	S_4	S_5	0
S_3	S_6	S_7	1
S_4	S_7	S_8	0
S_5	S_7	S_8	1
S_6	S_9	S_{10}	0
S_7	S_9	S_{10}	1
S_8	S_{10}	--	0
S_9	S_1	S_2	0
S_{10}	S_1	S_2	1

State Assignment Number 1

$Q_AQ_BQ_CQ_D$

$S_0 = 0\ 0\ 0\ 0$
$S_1 = 0\ 0\ 0\ 1$
$S_2 = 0\ 0\ 1\ 0$
$S_3 = 0\ 0\ 1\ 1$
$S_4 = 0\ 1\ 0\ 0$
$S_5 = 0\ 1\ 0\ 1$
$S_6 = 0\ 1\ 1\ 0$
$S_7 = 0\ 1\ 1\ 1$
$S_8 = 1\ 0\ 0\ 0$
$S_9 = 1\ 0\ 0\ 1$
$S_{10} = 1\ 0\ 1\ 0$

State Assignment Number 2

$Q_AQ_BQ_CQ_D$

$S_0 = 0\ 0\ 1\ 0$
$S_1 = 0\ 1\ 1\ 1$
$S_2 = 0\ 1\ 1\ 0$
$S_3 = 1\ 1\ 1\ 1$
$S_4 = 1\ 0\ 1\ 1$
$S_5 = 1\ 0\ 0\ 1$
$S_6 = 1\ 0\ 1\ 0$
$S_7 = 1\ 1\ 1\ 0$
$S_8 = 1\ 1\ 0\ 0$
$S_9 = 0\ 0\ 0\ 0$
$S_{10} = 0\ 1\ 0\ 0$

which state assignment is the most optimal in terms of reducing the complexity of the combinational logic portion of the design?

State Assignment Number 2

Justify your answer using the state assignment heuristics that were discussed in class and a state assignment table. (To receive credit, valid justification must be included.)

NOTE THIS IS THE STATE ASSIGNMENT TABLE FOR MOORE IMPLEMENTATION OF BCD TO EXCESS 3 DESIGN DISCUSSED IN CLASS

Rule (heuristic) priority 1: States that have the same next state should be given adjacent assignemnts;

1.1 (S_0,S_9,S_{10}) -- have same next states for X=0 and X=1
1.2 (S_4,S_5) -- have same next states for X=0 and X=1
1.3 (S_6,S_7) -- have same next states for X=0 and X=1

Rule (heuristic) priority 2: States which are the next states of the same state should be given adjacent assignments;

2.1 (S_1,S_2) -- are next states of S_0,S_9, and S_{10}
2.2 (S_3, S_4) -- are next states of S_1
2.3 (S_4,S_5) -- are next states of S_2
2.4 (S_6,S_7) -- are next states of S_3 and S_4
2.5 (S_7,S_8) -- are next states of S_5
2.6 (S_9,S_{10}) -- are next states of S_6 and S_7

Rule (heuristic) priority 3: States with the same output for a given input should be given adjacent assignments;

3.1 (S_0,S_2,S_4,S_6,S_8,S_9) -- have an output 0 for all values of X
3.2 (S_1,S_3,S_5,S_7,S_{10}) -- have an output 1 for all values of X

Q_AQ_B State Assignment 1

Q_CQ_D	00	01	11	10
00	S_0	S_4		S_8
01	S_1	S_5		S_9
11	S_3	S_7		
10	S_2	S_6		S_{10}

State Assignment Map

Rule 1:
1.1 Not met
1.2 Met
1.3 Met
Rule 2:
2.1 Not Met
2.2 Not Met
2.3 Met
2.4 Met
2.5 Not Met
2.6 Not Met

Q_AQ_B State Assignment 2

Q_CQ_D	00	01	11	10
00	S_9	S_{10}	S_8	
01				S_5
11		S_1	S_3	S_4
10	S_0	S_2	S_7	S_6

State Assignment Map

Rule 1:
1.1 Met*
1.2 Met
1.3 Met
Rule 2:
2.1 Met
2.2 Met
2.3 Met
2.4 Met
2.5 Met
2.6 Met

*As closely as possible -- two of the states are adjacent to the third

Priority Rule 3 groupings are about equally met be both assignments

State assignment 2 is better because it met all of Rule 1 and Rule 2 adjacent groupings!

13. [10 Points] A synchronous sequential circuit has one input and one output. If the input sequence 0101 or 0110 occurs, an output of two successive 1's will occur. The first of these 1's should occur coincident with the last input of the 0101 or 0110 sequence. The circuit should reset when the second 1 output occurs. For example,

input sequence: X = 0 1 0 0 1 1 1 0 1 0 1 0 1 0 1 1 0 1 ...

output sequence: Z = 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 1 1 ...

Derive a Mealy state graph with a minimum number of 6 states.

SAME PROBLEM AS 1.11 OF HW