Christopher Bero
10-2-2015
CPE 322

Simulation Assignment 01

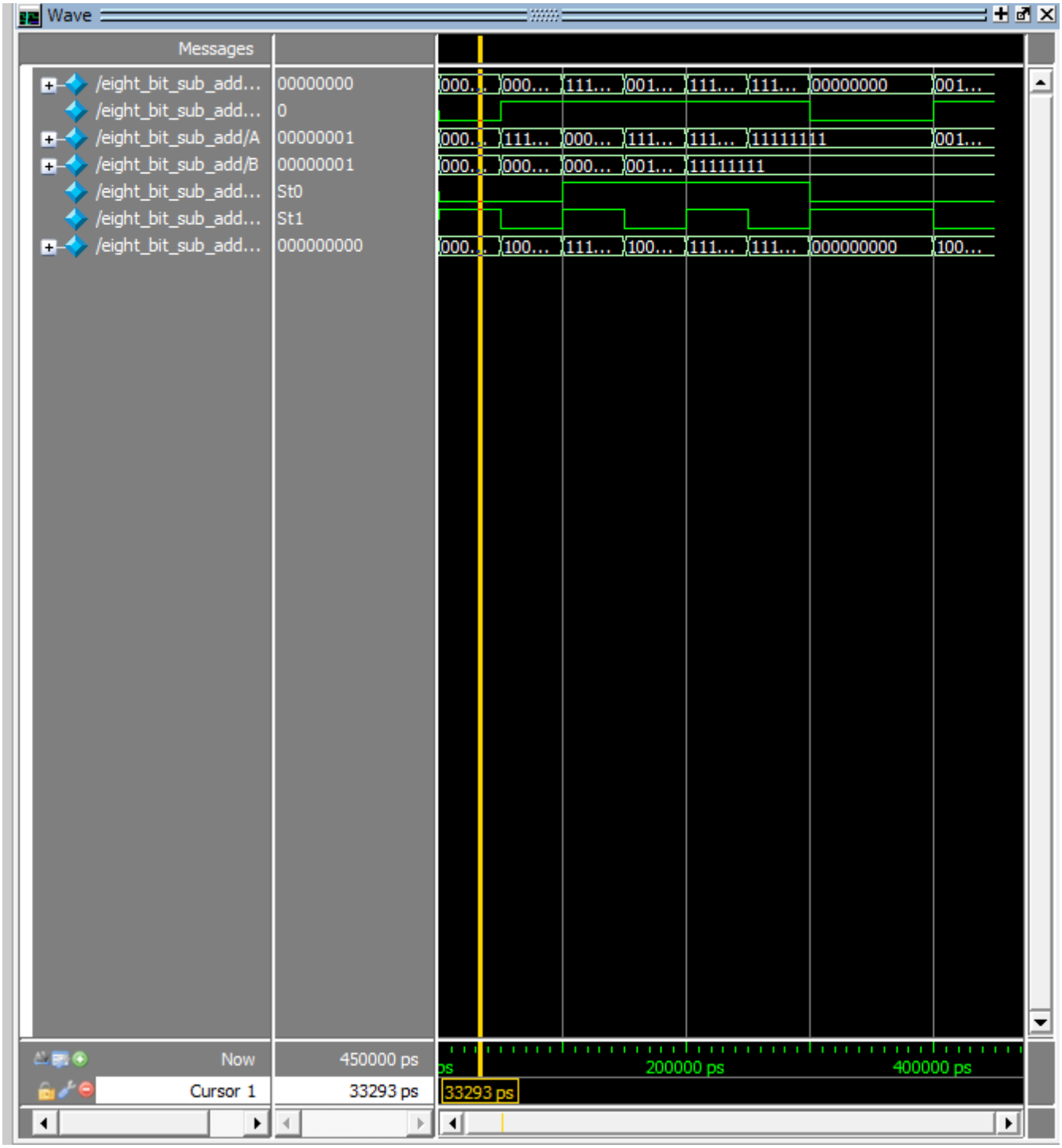
“RTL & Post FPGA Layout Timing Simulation of two an [sic] 8-bit Subtractor/Adder”

Stimulus

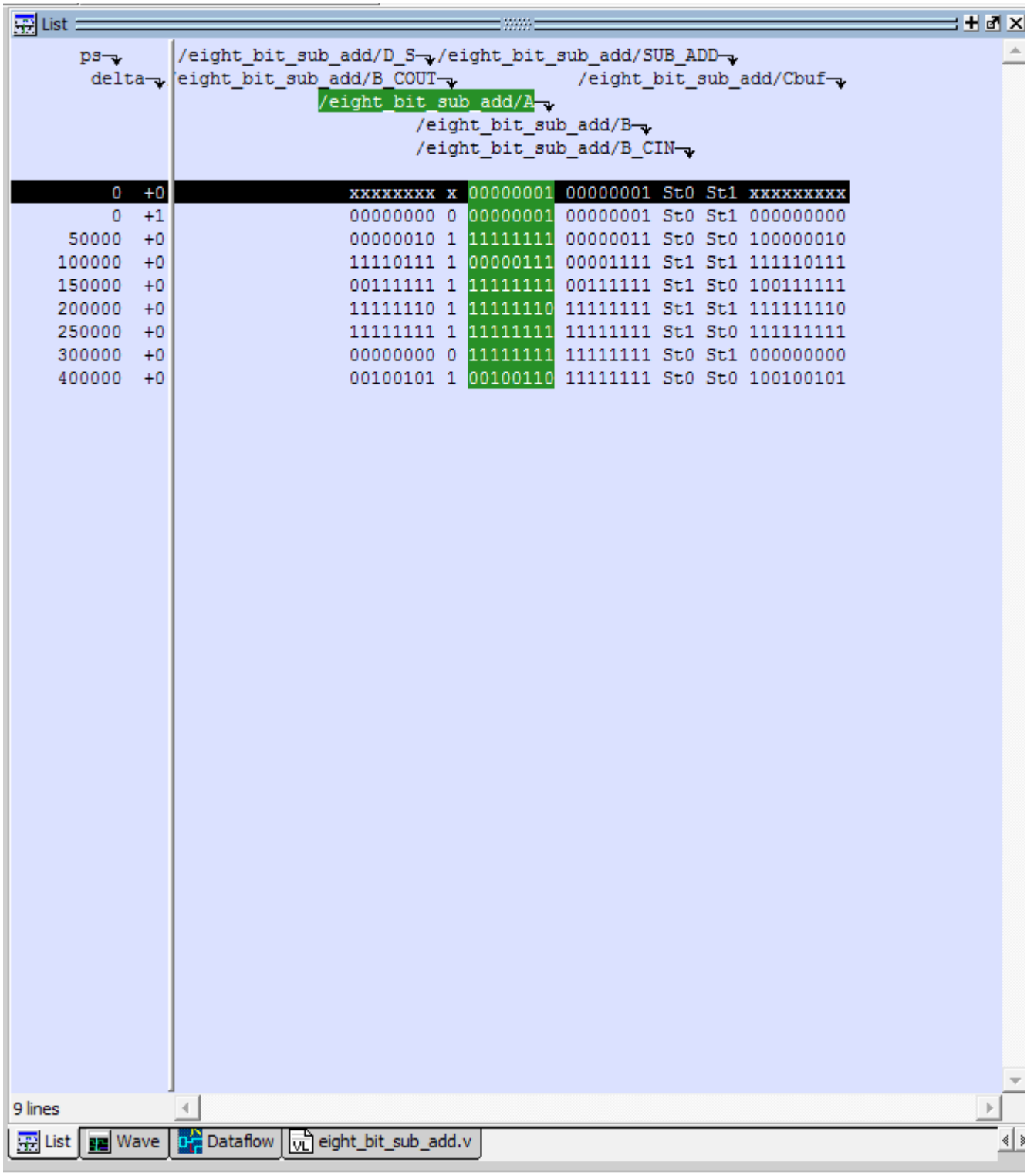
```
#
# Stimulus for Behavioral Model
# [0] is LSB
# SUB_ADD: 0=add (A+B), 1=subtract (A-B)
# Library: cycloneive_ver
#

force {sim:/eight_bit_sub_add/B_CIN}     0 0ns, 0 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns

force {sim:/eight_bit_sub_add/A[0]}      0 0ns, 1 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 1 400ns
force {sim:/eight_bit_sub_add/A[1]}      0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 1 400ns
force {sim:/eight_bit_sub_add/A[2]}      0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/A[3]}      0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/A[4]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight_bit_sub_add/A[5]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight_bit_sub_add/A[6]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight_bit_sub_add/A[7]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 0 200ns,
0 250ns, 1 300ns, 1 350ns, 0 400ns
F
force {sim:/eight_bit_sub_add/B[0]}      0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 1 400ns
force {sim:/eight_bit_sub_add/B[1]}      0 0ns, 0 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[2]}      0 0ns, 0 50ns, 1 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[3]}      0 0ns, 0 50ns, 1 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[4]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[5]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[6]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[7]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
0 250ns, 1 300ns, 1 350ns, 0 400ns

force {sim:/eight_bit_sub_add/SUB_ADD}   0 0ns, 1 50ns, 0 100ns, 1 150ns, 0 200ns,
1 250ns, 0 300ns, 1 350ns, 0 400ns

run 500ns
```

```
#
# Stimulus for Structural Model
# [0] is LSB
# SUB_ADD: 0=add (A+B), 1=subtract (A-B)
# Library: cycloneive_ver
#

force {sim:/eight_bit_sub_add/B_CIN}     0 0ns, 0 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns

force {sim:/eight_bit_sub_add/A[0]}      0 0ns, 1 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 1 400ns
force {sim:/eight_bit_sub_add/A[1]}      0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 1 400ns
force {sim:/eight_bit_sub_add/A[2]}      0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/A[3]}      0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/A[4]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight_bit_sub_add/A[5]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight_bit_sub_add/A[6]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight_bit_sub_add/A[7]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 0 200ns,
0 250ns, 1 300ns, 1 350ns, 0 400ns
F
force {sim:/eight_bit_sub_add/B[0]}      0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 1 400ns
force {sim:/eight_bit_sub_add/B[1]}      0 0ns, 0 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[2]}      0 0ns, 0 50ns, 1 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[3]}      0 0ns, 0 50ns, 1 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[4]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[5]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[6]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[7]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
0 250ns, 1 300ns, 1 350ns, 0 400ns

force {sim:/eight_bit_sub_add/SUB_ADD}   0 0ns, 1 50ns, 0 100ns, 1 150ns, 0 200ns,
1 250ns, 0 300ns, 1 350ns, 0 400ns

run 500ns
```

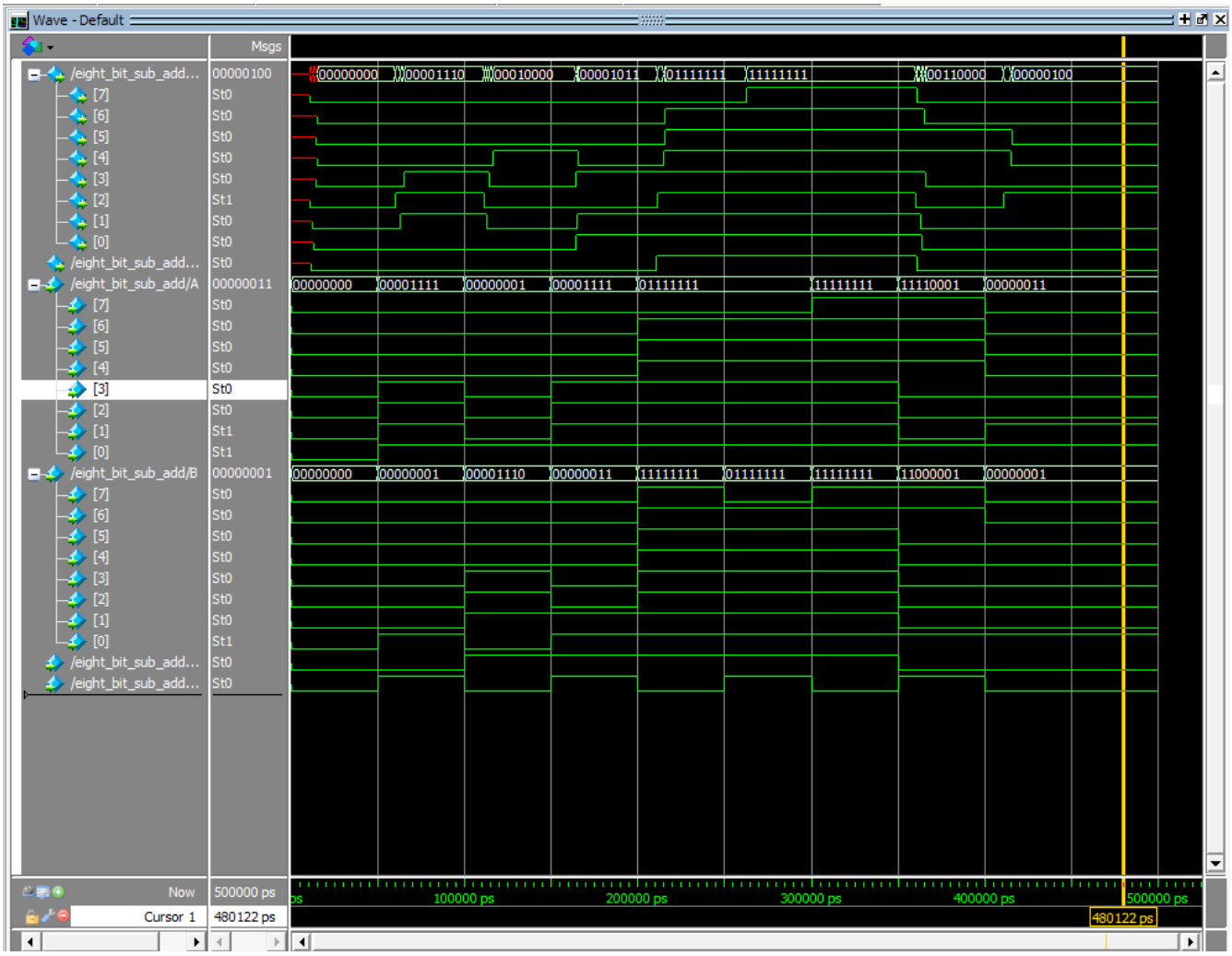
Behavioral:RTL:Waveform



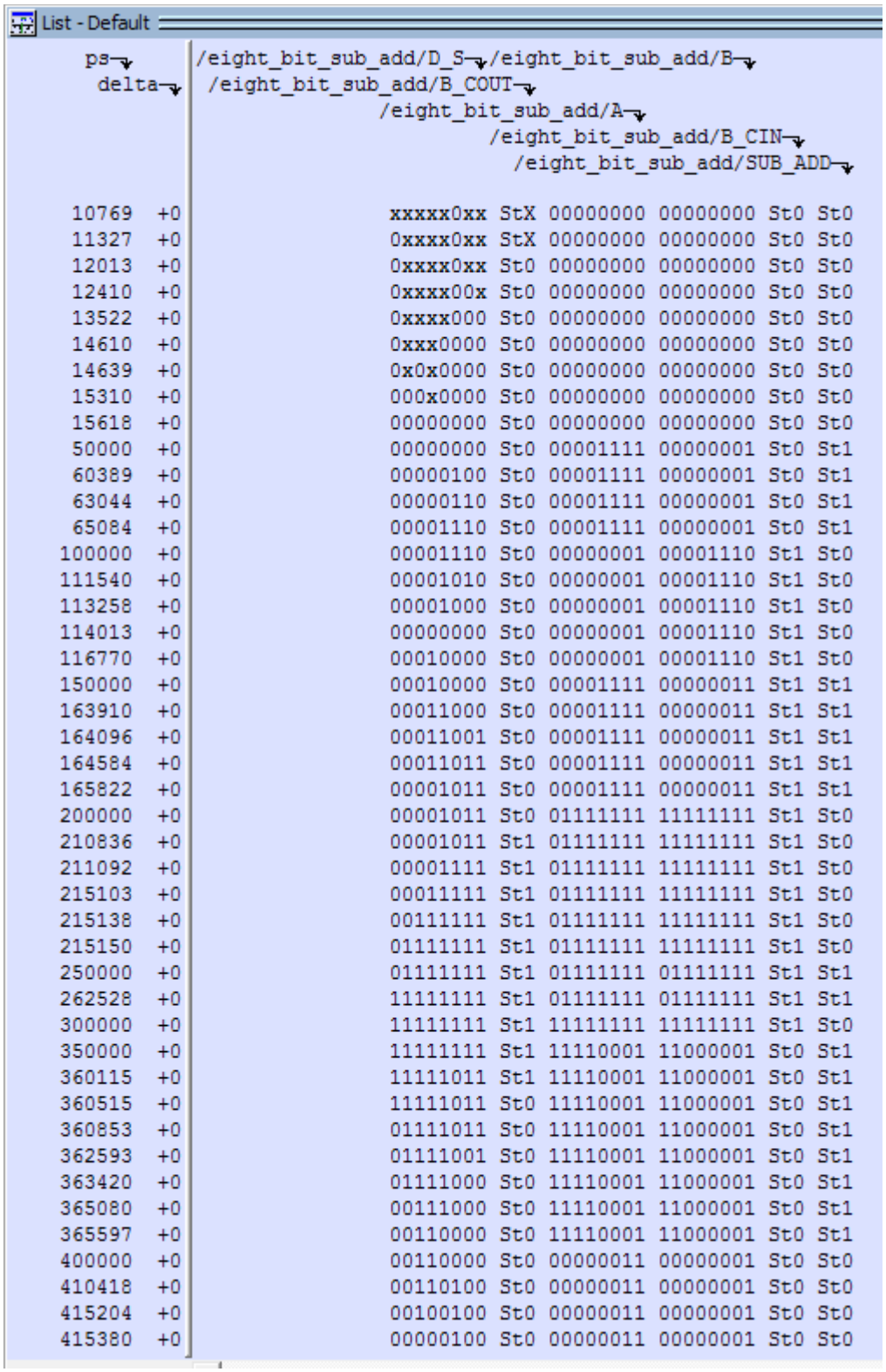
Behavioral:RTL:List



Behavioral:Gate:Slow:85:Waveform



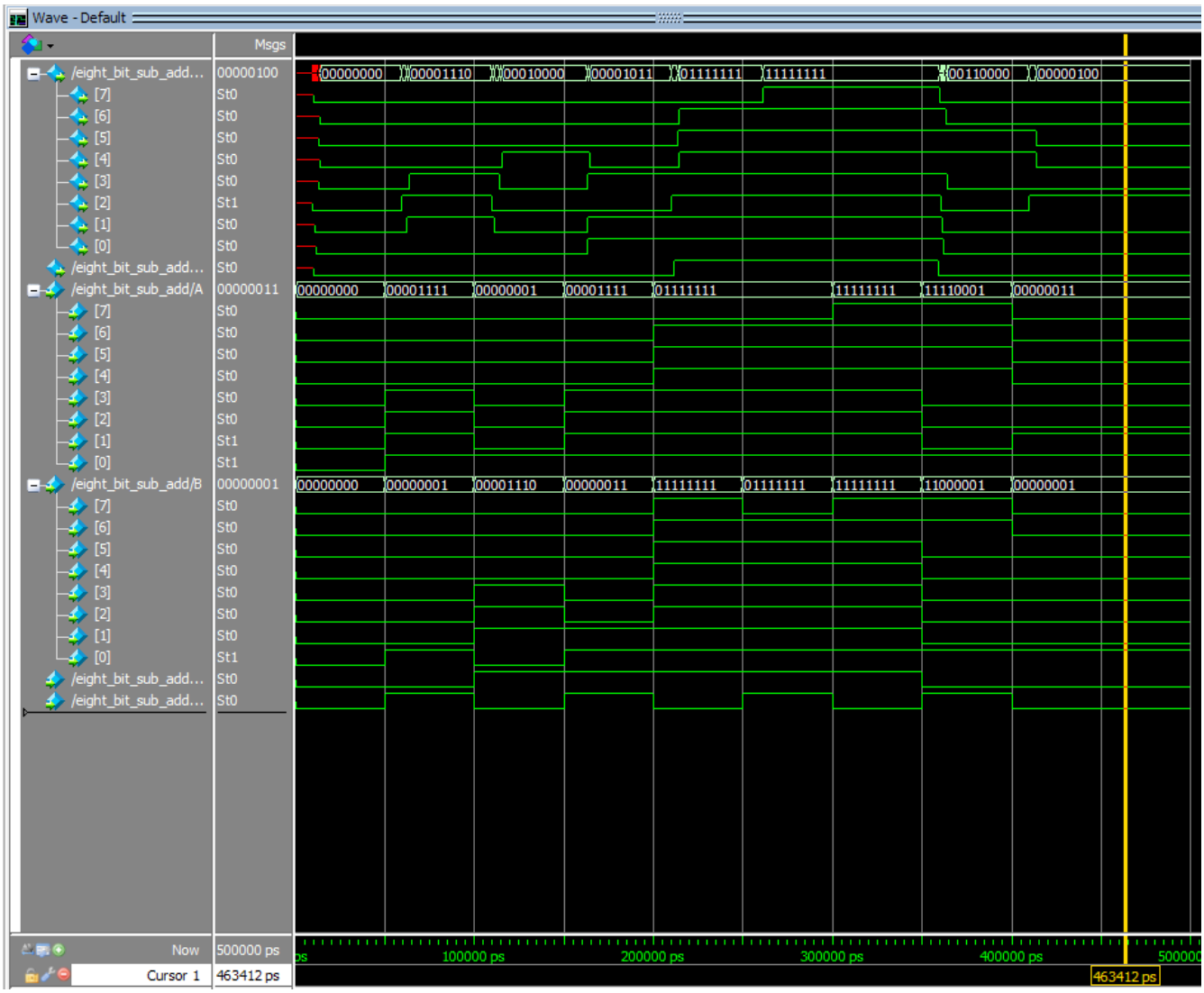
Behavioral:Gate:Slow:85:List



List - Default

ps delta	/eight_bit_sub_add/D_S /eight_bit_sub_add/B_COUT	/eight_bit_sub_add/B /eight_bit_sub_add/A	/eight_bit_sub_add/B_CIN	/eight_bit_sub_add/SUB_ADD
10769 +0	xxxxx0xx	StX 00000000	00000000	St0 St0
11327 +0	0xxxx0xx	StX 00000000	00000000	St0 St0
12013 +0	0xxxx0xx	St0 00000000	00000000	St0 St0
12410 +0	0xxxx00x	St0 00000000	00000000	St0 St0
13522 +0	0xxxx000	St0 00000000	00000000	St0 St0
14610 +0	0xxx0000	St0 00000000	00000000	St0 St0
14639 +0	0x0x0000	St0 00000000	00000000	St0 St0
15310 +0	000x0000	St0 00000000	00000000	St0 St0
15618 +0	00000000	St0 00000000	00000000	St0 St0
50000 +0	00000000	St0 00001111	00000001	St0 St1
60389 +0	00000100	St0 00001111	00000001	St0 St1
63044 +0	00000110	St0 00001111	00000001	St0 St1
65084 +0	00001110	St0 00001111	00000001	St0 St1
100000 +0	00001110	St0 00000001	00001110	St1 St0
111540 +0	00001010	St0 00000001	00001110	St1 St0
113258 +0	00001000	St0 00000001	00001110	St1 St0
114013 +0	00000000	St0 00000001	00001110	St1 St0
116770 +0	00010000	St0 00000001	00001110	St1 St0
150000 +0	00010000	St0 00001111	00000011	St1 St1
163910 +0	00011000	St0 00001111	00000011	St1 St1
164096 +0	00011001	St0 00001111	00000011	St1 St1
164584 +0	00011011	St0 00001111	00000011	St1 St1
165822 +0	00001011	St0 00001111	00000011	St1 St1
200000 +0	00001011	St0 01111111	11111111	St1 St0
210836 +0	00001011	St1 01111111	11111111	St1 St0
211092 +0	00001111	St1 01111111	11111111	St1 St0
215103 +0	00011111	St1 01111111	11111111	St1 St0
215138 +0	00111111	St1 01111111	11111111	St1 St0
215150 +0	01111111	St1 01111111	11111111	St1 St0
250000 +0	01111111	St1 01111111	01111111	St1 St1
262528 +0	11111111	St1 01111111	01111111	St1 St1
300000 +0	11111111	St1 11111111	11111111	St1 St0
350000 +0	11111111	St1 11110001	11000001	St0 St1
360115 +0	11111011	St1 11110001	11000001	St0 St1
360515 +0	11111011	St0 11110001	11000001	St0 St1
360853 +0	01111011	St0 11110001	11000001	St0 St1
362593 +0	01111001	St0 11110001	11000001	St0 St1
363420 +0	01111000	St0 11110001	11000001	St0 St1
365080 +0	00111000	St0 11110001	11000001	St0 St1
365597 +0	00110000	St0 11110001	11000001	St0 St1
400000 +0	00110000	St0 00000011	00000001	St0 St0
410418 +0	00110100	St0 00000011	00000001	St0 St0
415204 +0	00100100	St0 00000011	00000001	St0 St0
415380 +0	00000100	St0 00000011	00000001	St0 St0

Behavioral:Gate:Slow:0:Waveform

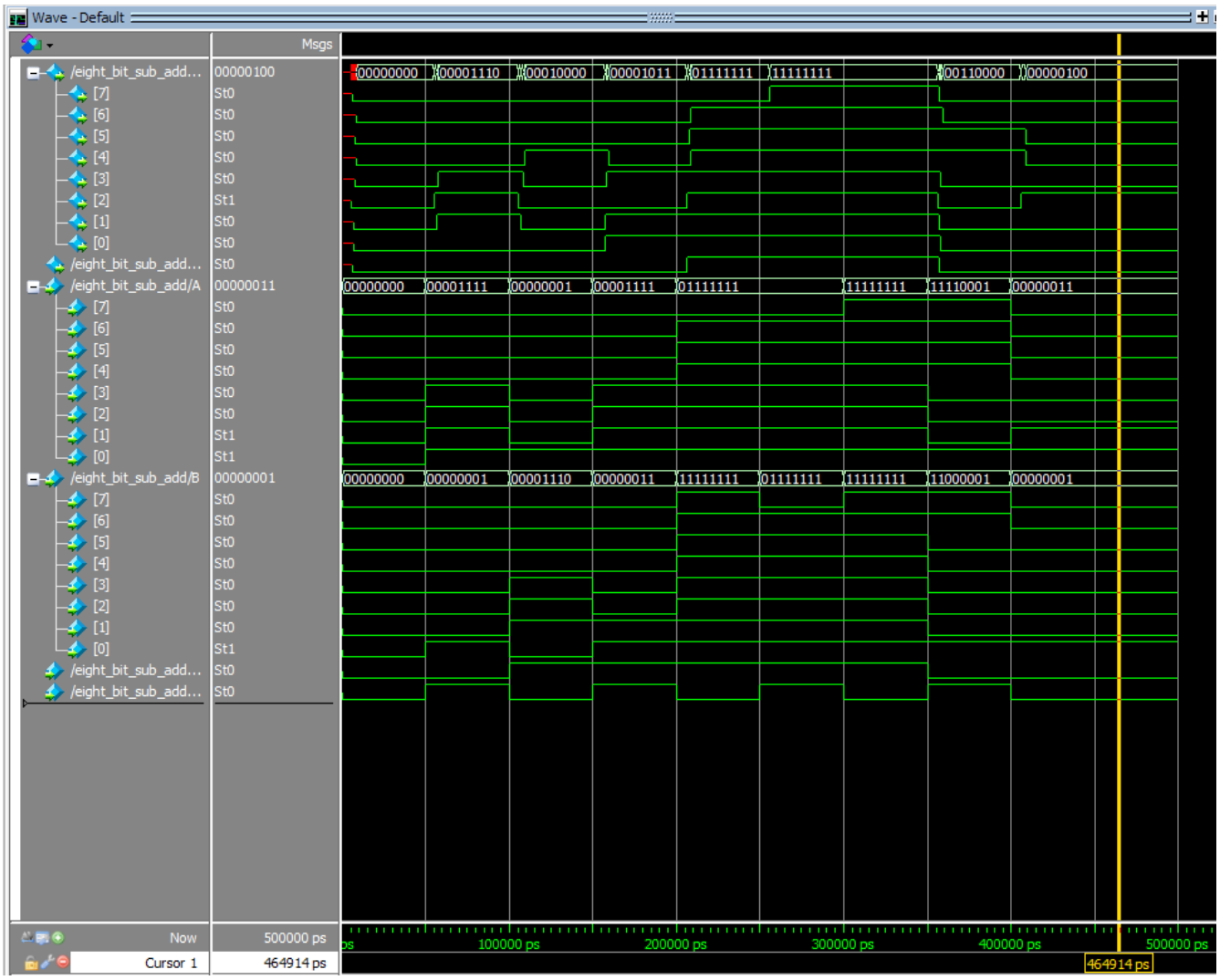


Behavioral:Gate:Slow:0:List

List - Default

ps delta	/eight_bit_sub_add/D_S /eight_bit_sub_add/B_COUT	/eight_bit_sub_add/B /eight_bit_sub_add/A	/eight_bit_sub_add/B_CIN	/eight_bit_sub_add/SUB_ADD
9503 +0	xxxxx0xx	StX 00000000	00000000	St0 St0
9990 +0	0xxxx0xx	StX 00000000	00000000	St0 St0
10605 +0	0xxxx0xx	St0 00000000	00000000	St0 St0
10994 +0	0xxxx00x	St0 00000000	00000000	St0 St0
11984 +0	0xxxx000	St0 00000000	00000000	St0 St0
12966 +0	0xxx0000	St0 00000000	00000000	St0 St0
13013 +0	0x0x0000	St0 00000000	00000000	St0 St0
13591 +0	000x0000	St0 00000000	00000000	St0 St0
13878 +0	00000000	St0 00000000	00000000	St0 St0
50000 +0	00000000	St0 00001111	00000001	St0 St1
59350 +0	00000100	St0 00001111	00000001	St0 St1
61864 +0	00000110	St0 00001111	00000001	St0 St1
63821 +0	00001110	St0 00001111	00000001	St0 St1
100000 +0	00001110	St0 00000001	00001110	St1 St0
110000 +0	00001010	St0 00000001	00001110	St1 St0
111197 +0	00001000	St0 00000001	00001110	St1 St0
113683 +0	00000000	St0 00000001	00001110	St1 St0
115395 +0	00010000	St0 00000001	00001110	St1 St0
150000 +0	00010000	St0 00001111	00000011	St1 St1
162732 +0	00011000	St0 00001111	00000011	St1 St1
162817 +0	00011001	St0 00001111	00000011	St1 St1
163234 +0	00011011	St0 00001111	00000011	St1 St1
164201 +0	00001011	St0 00001111	00000011	St1 St1
200000 +0	00001011	St0 01111111	11111111	St1 St0
210042 +0	00001111	St0 01111111	11111111	St1 St0
211295 +0	00001111	St1 01111111	11111111	St1 St0
213835 +0	00101111	St1 01111111	11111111	St1 St0
213855 +0	00111111	St1 01111111	11111111	St1 St0
213900 +0	01111111	St1 01111111	11111111	St1 St0
250000 +0	01111111	St1 01111111	01111111	St1 St1
261317 +0	11111111	St1 01111111	01111111	St1 St1
300000 +0	11111111	St1 11111111	11111111	St1 St0
350000 +0	11111111	St1 11110001	11000001	St0 St1
359346 +0	11111111	St0 11110001	11000001	St0 St1
359665 +0	01111111	St0 11110001	11000001	St0 St1
360228 +0	01111011	St0 11110001	11000001	St0 St1
361197 +0	01111001	St0 11110001	11000001	St0 St1
361930 +0	01111000	St0 11110001	11000001	St0 St1
363475 +0	00111000	St0 11110001	11000001	St0 St1
363911 +0	00110000	St0 11110001	11000001	St0 St1
400000 +0	00110000	St0 00000011	00000001	St0 St0
409336 +0	00110100	St0 00000011	00000001	St0 St0
413545 +0	00100100	St0 00000011	00000001	St0 St0
413704 +0	00000100	St0 00000011	00000001	St0 St0

Behavioral:Gate:Fast:0:Waveform

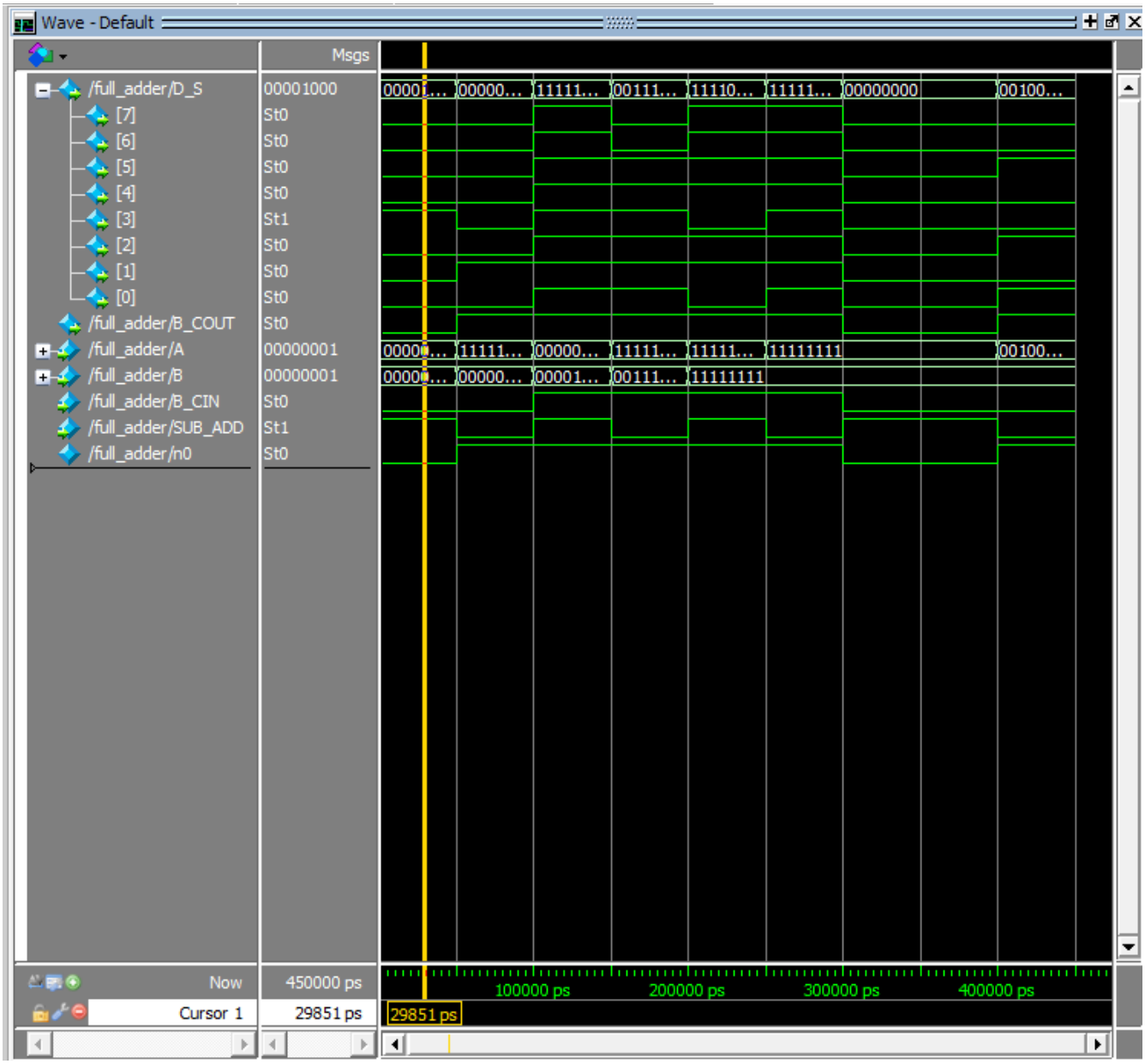


Behavioral:Gate:Fast:0:List

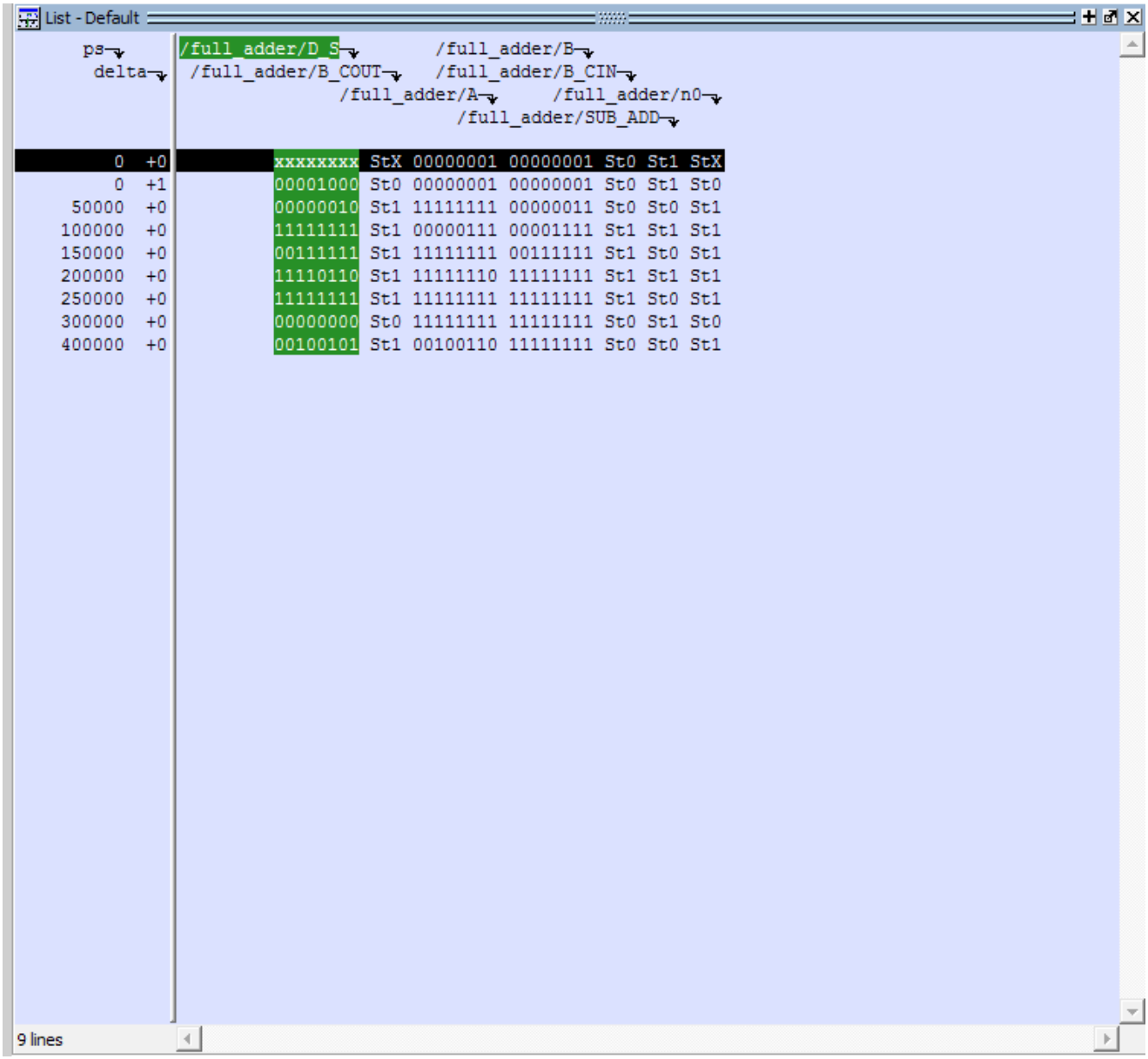
List - Default

ps delta	/eight_bit_sub_add/D_S /eight_bit_sub_add/B_COUT	/eight_bit_sub_add/B /eight_bit_sub_add/A	/eight_bit_sub_add/B_CIN	/eight_bit_sub_add/SUB_ADD
5858 +0	xxxxx0xx	StX 00000000	00000000	St0 St0
6137 +0	0xxxx0xx	StX 00000000	00000000	St0 St0
6337 +0	0xxxx0xx	St0 00000000	00000000	St0 St0
6854 +0	0xxxx00x	St0 00000000	00000000	St0 St0
7396 +0	0xxxx000	St0 00000000	00000000	St0 St0
8086 +0	0xxx0000	St0 00000000	00000000	St0 St0
8134 +0	0x0x0000	St0 00000000	00000000	St0 St0
8431 +0	000x0000	St0 00000000	00000000	St0 St0
8614 +0	00000000	St0 00000000	00000000	St0 St0
50000 +0	00000000	St0 00001111	00000001	St0 St1
55304 +0	00000100	St0 00001111	00000001	St0 St1
56624 +0	00000110	St0 00001111	00000001	St0 St1
57620 +0	00001110	St0 00001111	00000001	St0 St1
100000 +0	00001110	St0 00000001	00001110	St1 St0
105836 +0	00001010	St0 00000001	00001110	St1 St0
107249 +0	00001000	St0 00000001	00001110	St1 St0
108587 +0	00000000	St0 00000001	00001110	St1 St0
108994 +0	00010000	St0 00000001	00001110	St1 St0
150000 +0	00010000	St0 00001111	00000011	St1 St1
157112 +0	00010001	St0 00001111	00000011	St1 St1
157321 +0	00010011	St0 00001111	00000011	St1 St1
158062 +0	00011011	St0 00001111	00000011	St1 St1
159582 +0	00001011	St0 00001111	00000011	St1 St1
200000 +0	00001011	St0 01111111	11111111	St1 St0
205955 +0	00001011	St1 01111111	11111111	St1 St0
206163 +0	00001111	St1 01111111	11111111	St1 St0
207383 +0	00101111	St1 01111111	11111111	St1 St0
208264 +0	01101111	St1 01111111	11111111	St1 St0
208648 +0	01111111	St1 01111111	11111111	St1 St0
250000 +0	01111111	St1 01111111	01111111	St1 St1
255571 +0	11111111	St1 01111111	01111111	St1 St1
300000 +0	11111111	St1 11111111	11111111	St1 St0
350000 +0	11111111	St1 11110001	11000001	St0 St1
356510 +0	11111011	St1 11110001	11000001	St0 St1
357087 +0	01111011	St1 11110001	11000001	St0 St1
357249 +0	01111001	St1 11110001	11000001	St0 St1
357271 +0	01111001	St0 11110001	11000001	St0 St1
357605 +0	01111000	St0 11110001	11000001	St0 St1
358082 +0	01110000	St0 11110001	11000001	St0 St1
359336 +0	00110000	St0 11110001	11000001	St0 St1
400000 +0	00110000	St0 00000011	00000001	St0 St0
405723 +0	00110100	St0 00000011	00000001	St0 St0
408701 +0	00010100	St0 00000011	00000001	St0 St0
409185 +0	00000100	St0 00000011	00000001	St0 St0

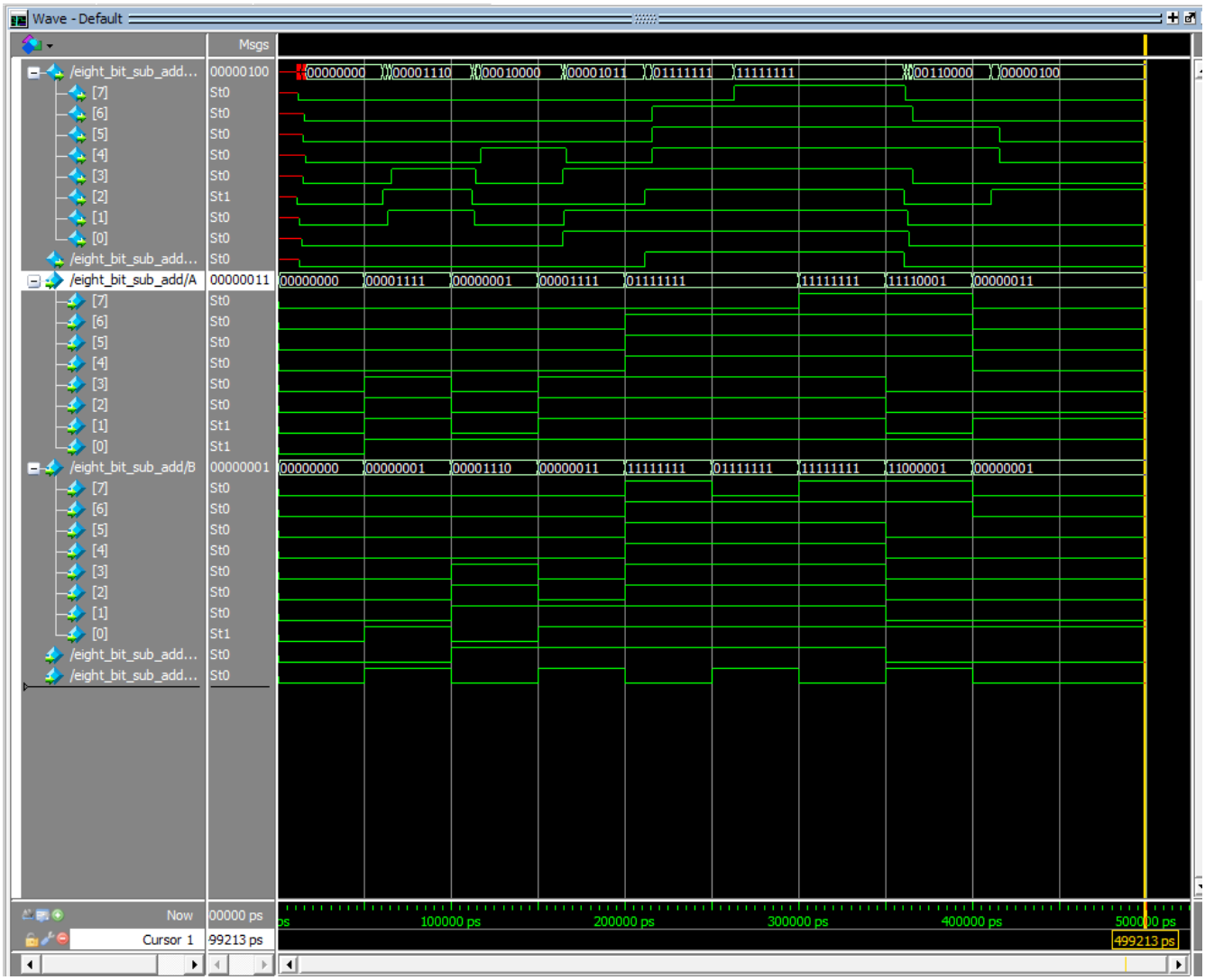
Structural:RTL:Waveform



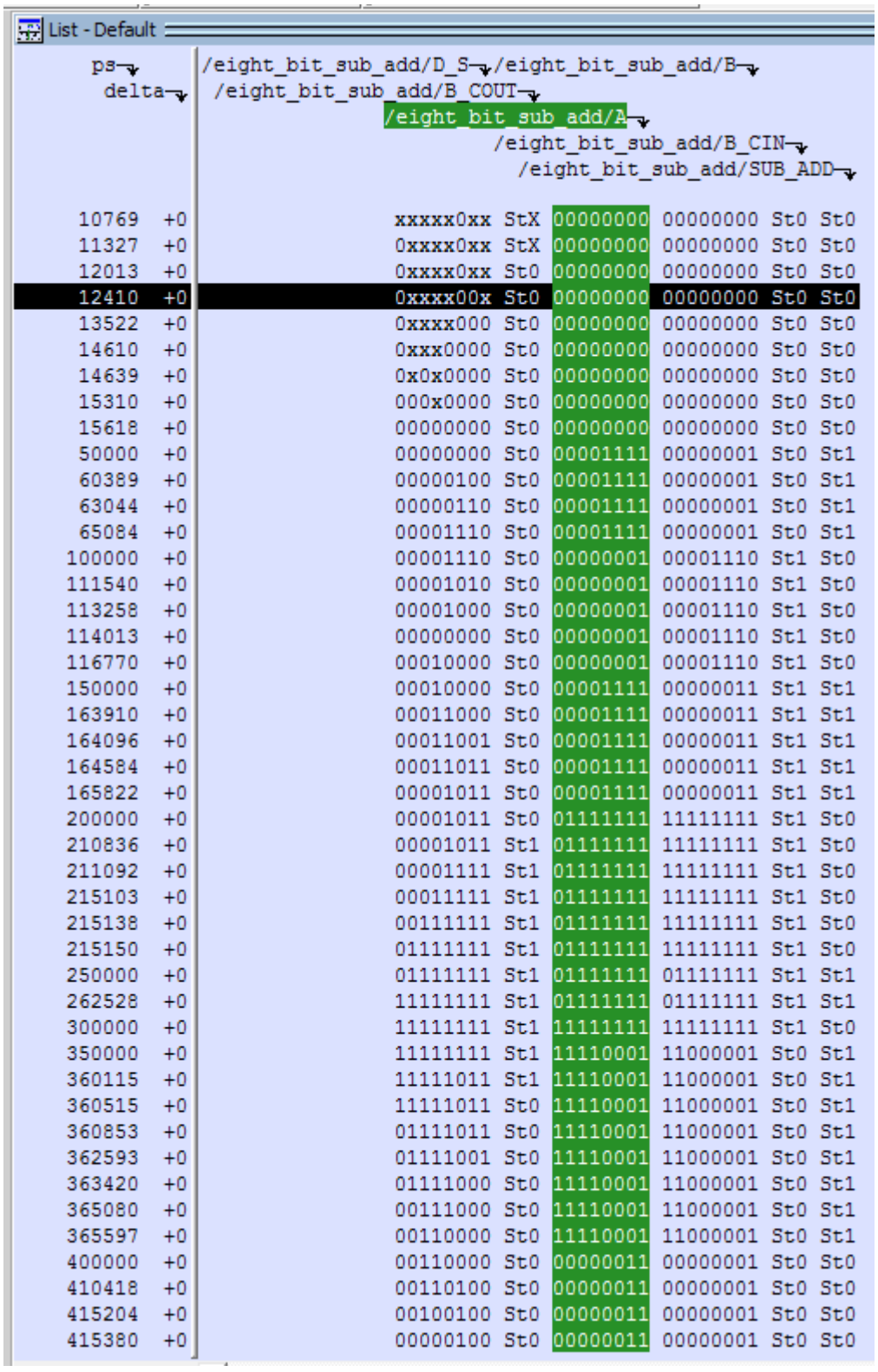
Structural:RTL:List



Structural:Gate:Slow:85:Waveform



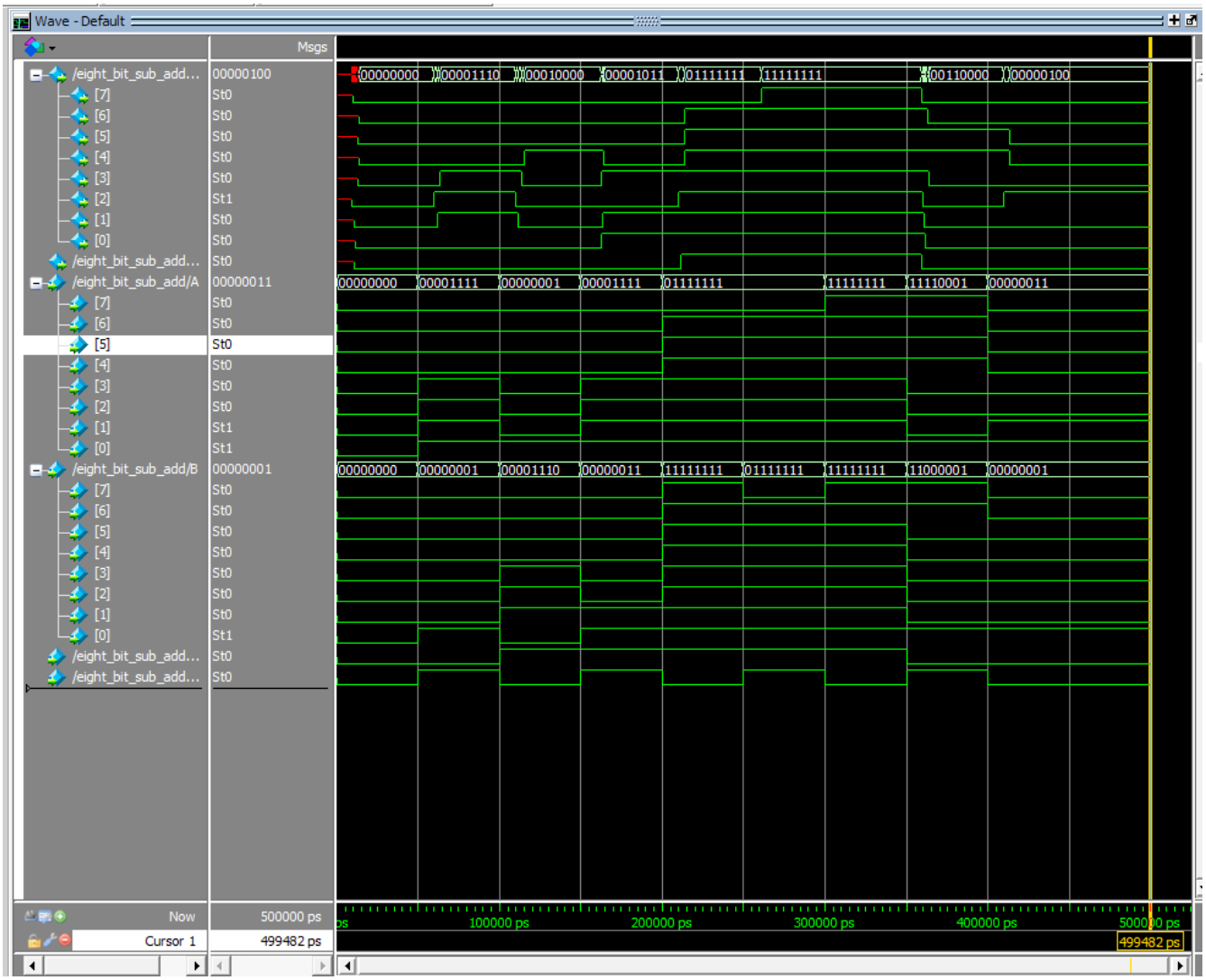
Structural:Gate:Slow:85:List



List - Default

ps	delta	/eight_bit_sub_add/D_S	/eight_bit_sub_add/B	/eight_bit_sub_add/B_COUT	/eight_bit_sub_add/A	/eight_bit_sub_add/B_CIN	/eight_bit_sub_add/SUB_ADD
10769	+0	xxxxx0xx	StX	00000000	00000000	St0	St0
11327	+0	0xxxx0xx	StX	00000000	00000000	St0	St0
12013	+0	0xxxx0xx	St0	00000000	00000000	St0	St0
12410	+0	0xxxx00x	St0	00000000	00000000	St0	St0
13522	+0	0xxxx000	St0	00000000	00000000	St0	St0
14610	+0	0xxx0000	St0	00000000	00000000	St0	St0
14639	+0	0x0x0000	St0	00000000	00000000	St0	St0
15310	+0	000x0000	St0	00000000	00000000	St0	St0
15618	+0	00000000	St0	00000000	00000000	St0	St0
50000	+0	00000000	St0	00001111	00000001	St0	St1
60389	+0	00000100	St0	00001111	00000001	St0	St1
63044	+0	00000110	St0	00001111	00000001	St0	St1
65084	+0	00001110	St0	00001111	00000001	St0	St1
100000	+0	00001110	St0	00000001	00001110	St1	St0
111540	+0	00001010	St0	00000001	00001110	St1	St0
113258	+0	00001000	St0	00000001	00001110	St1	St0
114013	+0	00000000	St0	00000001	00001110	St1	St0
116770	+0	00010000	St0	00000001	00001110	St1	St0
150000	+0	00010000	St0	00001111	00000011	St1	St1
163910	+0	00011000	St0	00001111	00000011	St1	St1
164096	+0	00011001	St0	00001111	00000011	St1	St1
164584	+0	00011011	St0	00001111	00000011	St1	St1
165822	+0	00001011	St0	00001111	00000011	St1	St1
200000	+0	00001011	St0	01111111	11111111	St1	St0
210836	+0	00001011	St1	01111111	11111111	St1	St0
211092	+0	00001111	St1	01111111	11111111	St1	St0
215103	+0	00011111	St1	01111111	11111111	St1	St0
215138	+0	00111111	St1	01111111	11111111	St1	St0
215150	+0	01111111	St1	01111111	11111111	St1	St0
250000	+0	01111111	St1	01111111	01111111	St1	St1
262528	+0	11111111	St1	01111111	01111111	St1	St1
300000	+0	11111111	St1	11111111	11111111	St1	St0
350000	+0	11111111	St1	11110001	11000001	St0	St1
360115	+0	11111011	St1	11110001	11000001	St0	St1
360515	+0	11111011	St0	11110001	11000001	St0	St1
360853	+0	01111011	St0	11110001	11000001	St0	St1
362593	+0	01111001	St0	11110001	11000001	St0	St1
363420	+0	01111000	St0	11110001	11000001	St0	St1
365080	+0	00111000	St0	11110001	11000001	St0	St1
365597	+0	00110000	St0	11110001	11000001	St0	St1
400000	+0	00110000	St0	00000011	00000001	St0	St0
410418	+0	00110100	St0	00000011	00000001	St0	St0
415204	+0	00100100	St0	00000011	00000001	St0	St0
415380	+0	00000100	St0	00000011	00000001	St0	St0

Structural:Gate:Slow:0:Waveform

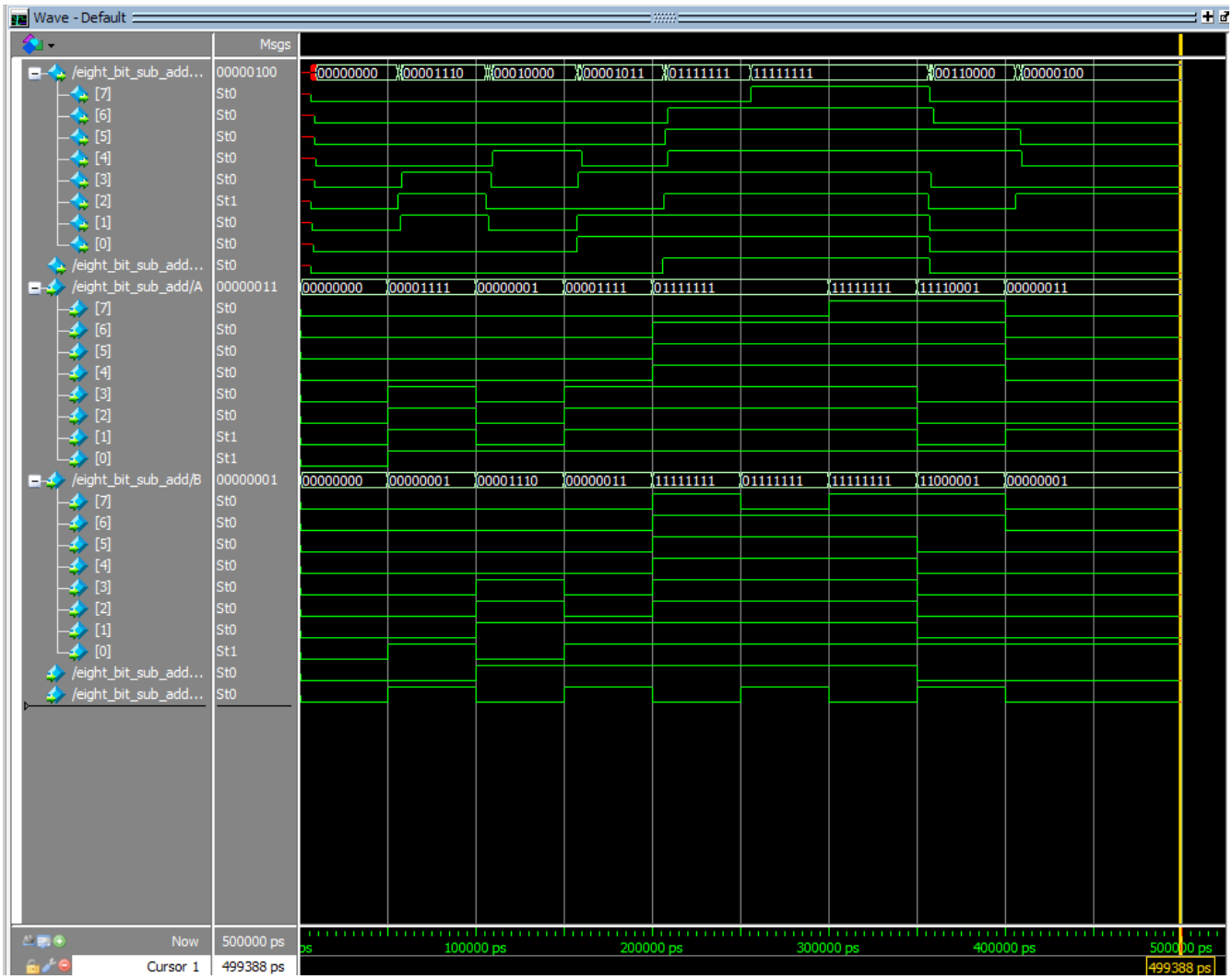


Structural:Gate:Slow:0:List

List - Default

ps delta	/eight_bit_sub_add/D_S	/eight_bit_sub_add/B /eight_bit_sub_add/B_COUT	/eight_bit_sub_add/A	/eight_bit_sub_add/B_CIN	/eight_bit_sub_add/SUB_ADD
0 +0	xxxxxxxx	StX	00000000	00000000	St0 St0
0 +1	zzzzzzzz	HiZ	00000000	00000000	St0 St0
0 +2	xxxxxxxx	StX	00000000	00000000	St0 St0
9503 +0	xxxxx0xx	StX	00000000	00000000	St0 St0
9990 +0	0xxxx0xx	StX	00000000	00000000	St0 St0
10605 +0	0xxxx0xx	St0	00000000	00000000	St0 St0
10994 +0	0xxxx00x	St0	00000000	00000000	St0 St0
11984 +0	0xxxx000	St0	00000000	00000000	St0 St0
12966 +0	0xxx0000	St0	00000000	00000000	St0 St0
13013 +0	0x0x0000	St0	00000000	00000000	St0 St0
13591 +0	000x0000	St0	00000000	00000000	St0 St0
13878 +0	00000000	St0	00000000	00000000	St0 St0
50000 +0	00000000	St0	00001111	00000001	St0 St1
59350 +0	00000100	St0	00001111	00000001	St0 St1
61864 +0	00000110	St0	00001111	00000001	St0 St1
63821 +0	00001110	St0	00001111	00000001	St0 St1
100000 +0	00001110	St0	00000001	00001110	St1 St0
110000 +0	00001010	St0	00000001	00001110	St1 St0
111197 +0	00001000	St0	00000001	00001110	St1 St0
113683 +0	00000000	St0	00000001	00001110	St1 St0
115395 +0	00010000	St0	00000001	00001110	St1 St0
150000 +0	00010000	St0	00001111	00000011	St1 St1
162732 +0	00011000	St0	00001111	00000011	St1 St1
162817 +0	00011001	St0	00001111	00000011	St1 St1
163234 +0	00011011	St0	00001111	00000011	St1 St1
164201 +0	00001011	St0	00001111	00000011	St1 St1
200000 +0	00001011	St0	01111111	11111111	St1 St0
210042 +0	00001111	St0	01111111	11111111	St1 St0
211295 +0	00001111	St1	01111111	11111111	St1 St0
213835 +0	00101111	St1	01111111	11111111	St1 St0
213855 +0	00111111	St1	01111111	11111111	St1 St0
213900 +0	01111111	St1	01111111	11111111	St1 St0
250000 +0	01111111	St1	01111111	01111111	St1 St1
261317 +0	11111111	St1	01111111	01111111	St1 St1
300000 +0	11111111	St1	11111111	11111111	St1 St0
350000 +0	11111111	St1	11110001	11000001	St0 St1
359346 +0	11111111	St0	11110001	11000001	St0 St1
359665 +0	01111111	St0	11110001	11000001	St0 St1
360228 +0	01111011	St0	11110001	11000001	St0 St1
361197 +0	01111001	St0	11110001	11000001	St0 St1
361930 +0	01111000	St0	11110001	11000001	St0 St1
363475 +0	00111000	St0	11110001	11000001	St0 St1
363911 +0	00110000	St0	11110001	11000001	St0 St1
400000 +0	00110000	St0	00000011	00000001	St0 St0

Structural:Gate:Fast:0:Waveform



Structural:Gate:Fast:0:List

List - Default

ps / delta	/eight_bit_sub_add/D_S	/eight_bit_sub_add/B	/eight_bit_sub_add/B_COUT	/eight_bit_sub_add/A	/eight_bit_sub_add/B_CIN	/eight_bit_sub_add/SUB_ADD
5858 +0	xxxxx0xx	StX	00000000	00000000	St0	St0
6137 +0	0xxxx0xx	StX	00000000	00000000	St0	St0
6337 +0	0xxxx0xx	St0	00000000	00000000	St0	St0
6854 +0	0xxxx00x	St0	00000000	00000000	St0	St0
7396 +0	0xxxx000	St0	00000000	00000000	St0	St0
8086 +0	0xxx0000	St0	00000000	00000000	St0	St0
8134 +0	0x0x0000	St0	00000000	00000000	St0	St0
8431 +0	000x0000	St0	00000000	00000000	St0	St0
8614 +0	00000000	St0	00000000	00000000	St0	St0
50000 +0	00000000	St0	00001111	00000001	St0	St1
55304 +0	00000100	St0	00001111	00000001	St0	St1
56624 +0	00000110	St0	00001111	00000001	St0	St1
57620 +0	00001110	St0	00001111	00000001	St0	St1
100000 +0	00001110	St0	00000001	00001110	St1	St0
105836 +0	00001010	St0	00000001	00001110	St1	St0
107249 +0	00001000	St0	00000001	00001110	St1	St0
108587 +0	00000000	St0	00000001	00001110	St1	St0
108994 +0	00010000	St0	00000001	00001110	St1	St0
150000 +0	00010000	St0	00001111	00000011	St1	St1
157112 +0	00010001	St0	00001111	00000011	St1	St1
157321 +0	00010011	St0	00001111	00000011	St1	St1
158062 +0	00011011	St0	00001111	00000011	St1	St1
159582 +0	00001011	St0	00001111	00000011	St1	St1
200000 +0	00001011	St0	01111111	11111111	St1	St0
205955 +0	00001011	St1	01111111	11111111	St1	St0
206163 +0	00001111	St1	01111111	11111111	St1	St0
207383 +0	00101111	St1	01111111	11111111	St1	St0
208264 +0	01101111	St1	01111111	11111111	St1	St0
208648 +0	01111111	St1	01111111	11111111	St1	St0
250000 +0	01111111	St1	01111111	01111111	St1	St1
255571 +0	11111111	St1	01111111	01111111	St1	St1
300000 +0	11111111	St1	11111111	11111111	St1	St0
350000 +0	11111111	St1	11110001	11000001	St0	St1
356510 +0	11111011	St1	11110001	11000001	St0	St1
357087 +0	01111011	St1	11110001	11000001	St0	St1
357249 +0	01111001	St1	11110001	11000001	St0	St1
357271 +0	01111001	St0	11110001	11000001	St0	St1
357605 +0	01111000	St0	11110001	11000001	St0	St1
358082 +0	01110000	St0	11110001	11000001	St0	St1
359336 +0	00110000	St0	11110001	11000001	St0	St1
400000 +0	00110000	St0	00000011	00000001	St0	St0
405723 +0	00110100	St0	00000011	00000001	St0	St0
408701 +0	00010100	St0	00000011	00000001	St0	St0
409185 +0	00000100	St0	00000011	00000001	St0	St0

Discussion

Without a definition for glitch to act as a basis for the assignment, pinpointing one is a nontrivial task. As observed, we did not notice anything worthy of a glitch, as the system appeared to operate correctly after troubleshooting to start Model-Sim was successful. Again, significant is not described to us, and the models appeared to have very similar output which leads us to believe that there is not a significant difference between behavioral and structural representations of the system in verilog. Since we have not implemented any activity based on the output of the simulation, determining the merits of waveform and list output is a dubiously wasteful and unadvantageous exercise. Nevertheless, it is this student's stance that the waveform view makes understanding the progression of the combinational circuit easier, while the list output makes immediate instantaneous analysis and debugging faster.