THE UNIVERSITY OF ALABAMA IN HUNTSVILLE

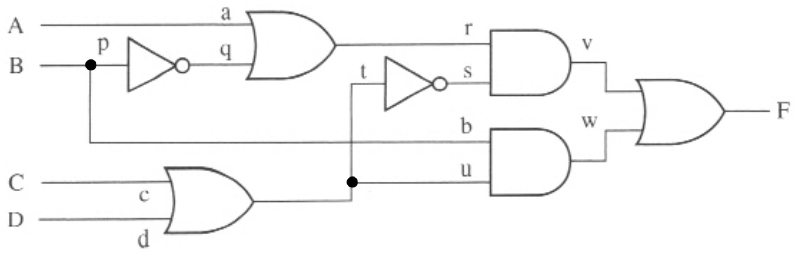
Department of Electrical and Computer Engineering

CPE 322 Digital Hardware Design Fundamentals

Stuck-at Fault Detection/Test Patern Generation Practice Problems

1)

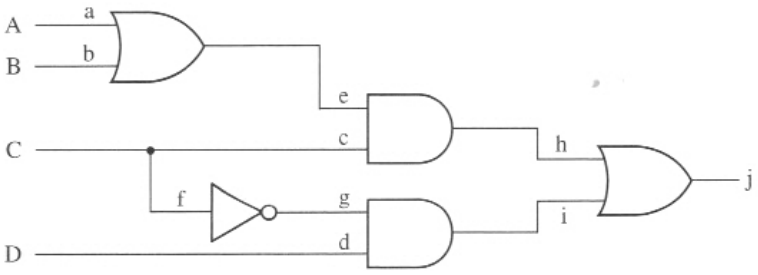
(a) Determine the necessary inputs to the following circuit to test for *u* stuck-at-0.
(b) For this set of inputs, determine which other stuck-at faults can be tested.
(c) Repeat (a) and (b) for *r* stuck-at-1.



2)

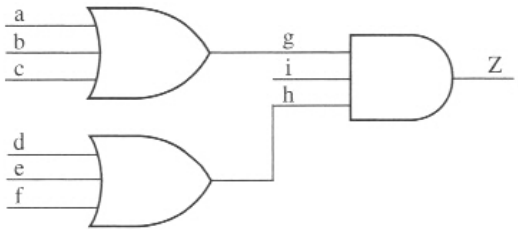
For the following circuit,

(a) Determine the values of *A*, *B*, *C*, and *D* necessary to test for *e* s-a-1. Specify the other faults tested by this input vector.
(b) Repeat (a) for *g* s-a-0.



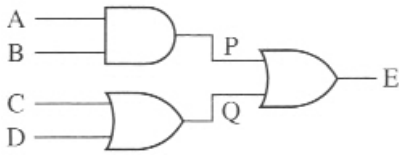
3)

Find a minimum set of tests that will test all single stuck-at-0 and stuck-at-1 faults in the following circuit. For each test, specify which faults are tested for s-a-0 and for s-a-1.



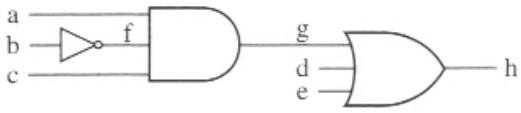
4)

Give a minimum set of test vectors that will test for all stuck-at faults in the following circuit. List the faults tested by each test vector.



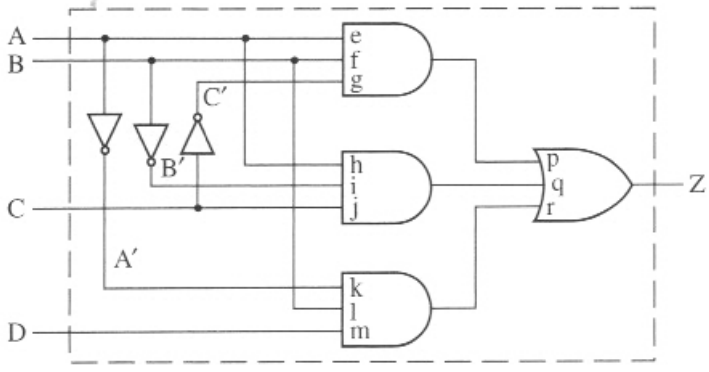
5)

For the following circuit, specify a minimum set of test vectors for *a, b, c, d*, and *e* that will test for all stuck-at faults. Specify the faults tested by each vector.



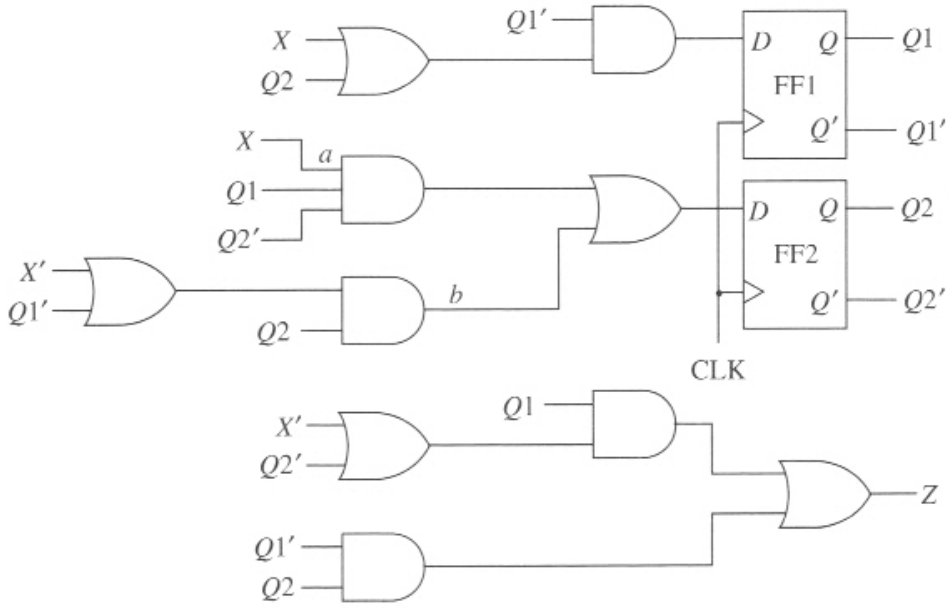
6)

For the following circuit, find a minimum number of test vectors that will test all s-a-0 and s-a-1 faults at the AND and OR gate inputs. For each test vector, specify the values of *A, B, C* and *D*, and the stuck-at faults that are tested.

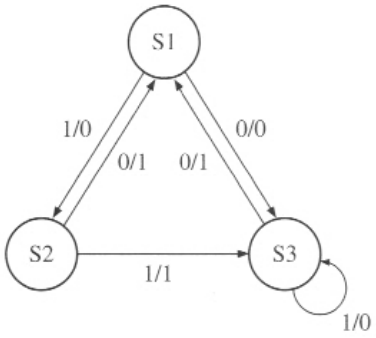


7)

Find a test sequence to test for *b* s-a-0 in the following sequential circuit:



8) A sequential circuit has the following State Trasistion Graph, STG.



The three states can be distinguished from one another in properly operating logic network using the input sequence 11 and observing the output. The circuit has a reset input, R, that resets it to the state S1. Give a set of test sequences that will test every state transition and give the transition tested by each sequence.

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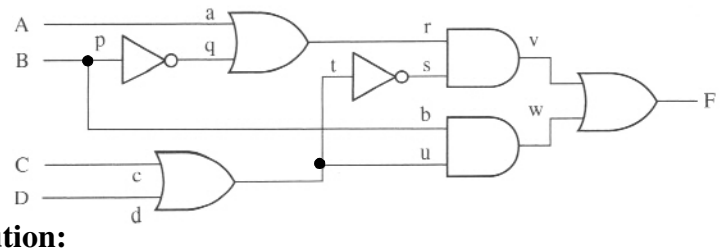
CPE 322 Digital Hardware Design Fundamentals

Stuck-at Fault Detection/Test Patern Generation Practice Problems Solutions

1)

(a) Determine the necessary inputs to the following circuit to test for *u* stuck-at-0.
(b) For this set of inputs, determine which other stuck-at faults can be tested.
(c) Repeat (a) and (b) for *r* stuck-at-1.



Solution:

(a) & (b)

A	B	C	D	Faults Tested
X	1	0	1	u0, b0, d0, w0
X	1	1	0	u0, b0, c0, w0

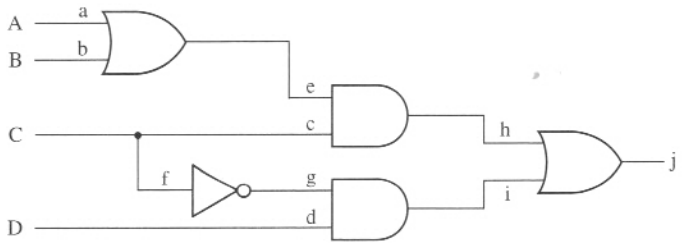
(c)

A	B	C	D	Faults Tested
0	1	0	0	a1, c1, d1, q1, r1, u1, v1, w1, p0

2)

For the following circuit,

(a) Determine the values of *A*, *B*, *C*, and *D* necessary to test for *e* s-a-1. Specify the other faults tested by this input vector.
(b) Repeat (a) for *g* s-a-0.



Solution:

(a)

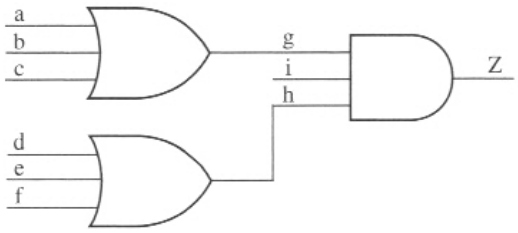
A	B	C	D	Faults Tested
0	0	1	X	a1, b1, e1, g1, h1, i1, j1, f0

(b)

A	B	C	D	Faults Tested
X	X	0	1	d0, g0, i0, j0, f1

3)

Find a minimum set of tests that will test all single stuck-at-0 and stuck-at-1 faults in the following circuit. For each test, specify which faults are tested for s-a-0 and for s-a-1.

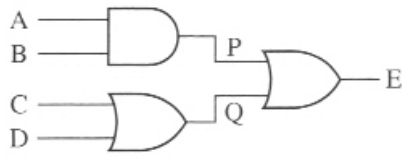


Solution:

a	b	c	d	e	f	i	Faults Tested					
1	0	0	1	0	0	1	a0,	d0,	g0,	h0,	i0,	Z0
0	1	0	0	1	0	1	b0,	e0,	g0,	h0,	i0,	Z0
0	0	1	0	0	1	1	c0,	f0,	g0,	h0,	i0,	Z0
0	0	0	1	X	X	1	a1,	b1,	c1,	g1,	Z1	
1	X	X	0	0	0	1	d1,	e1,	f1,	h1,	Z1	
1	X	X	1	X	X	0	i1,	Z1				

4)

Give a minimum set of test vectors that will test for all stuck-at faults in the following circuit. List the faults tested by each test vector.

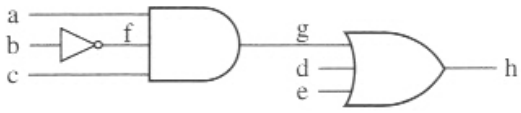


Solution:

A	B	C	D	Faults Tested					
1	1	0	0	A0,	B0,	P0,	E0		
0	X	1	0	C0,	Q0,	E0			
0	X	0	1	D0,	Q0,	E0			
0	1	0	0	A1,	C1,	D1,	P1,	Q1,	E1
1	0	0	0	B1,	C1,	D1,	P1,	Q1,	E1

5)

For the following circuit, specify a minimum set of test vectors for *a, b, c, d*, and *e* that will test for all stuck-at faults. Specify the faults tested by each vector.

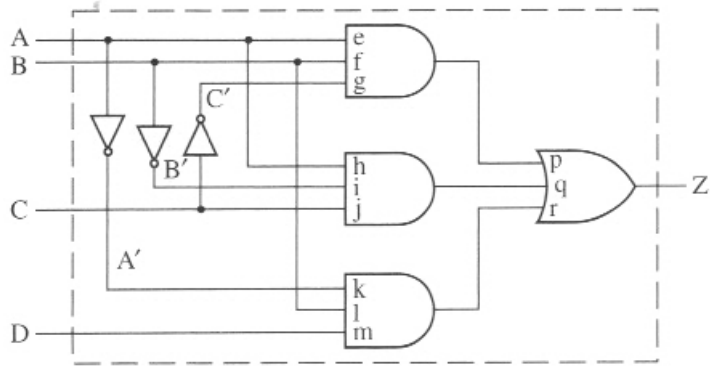


Solution:

a	b	c	d	e	Faults Tested					
1	0	1	0	0	a0,	c0,	f0,	g0,	h0,	b1
0	X	X	1	0	d0,	h0				
0	X	X	0	1	e0,	h0				
0	0	1	0	0	a1,	d1,	e1,	g1,	h1	
1	1	1	0	0	d1,	e1,	f1,	g1,	h1,	b0
1	0	0	0	0	c1,	d1,	e1,	g1,	h1	

6)

For the following circuit, find a minimum number of test vectors that will test all s-a-0 and s-a-1 faults at the AND and OR gate inputs. For each test vector, specify the values of *A, B, C* and *D*, and the stuck-at faults that are tested.

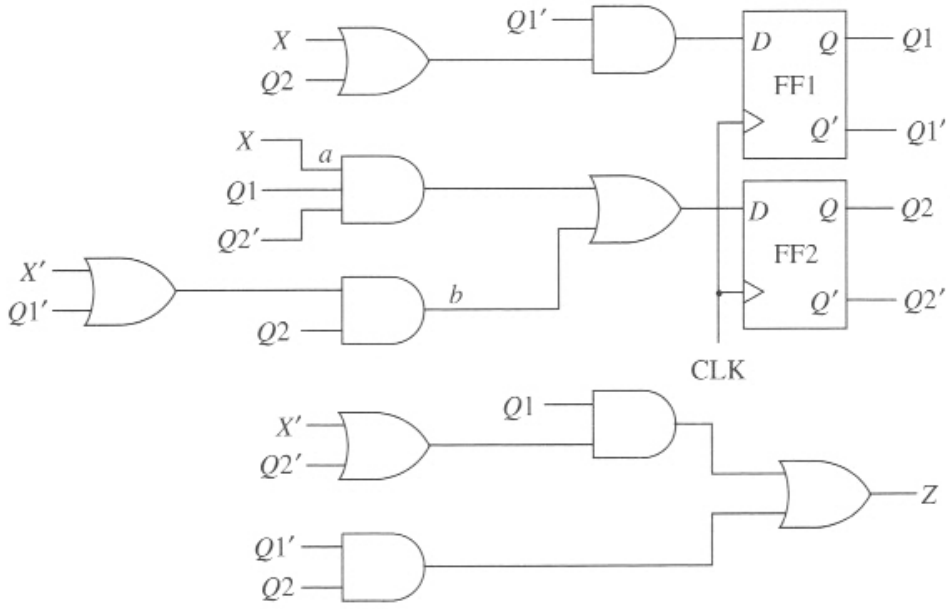


Solution:

A	B	C	D	Faults Tested					
0	1	X	1	k0,	l0,	m0,	r0,	z0	
1	1	0	X	e0,	f0,	g0,	p0,	z0	
1	0	1	X	h0,	i0,	j0,	q0,	z0	
0	0	1	1	h1,	l1,	p1,	q1,	r1,	z1
0	1	0	0	e1,	m1,	p1,	q1,	r1,	z1
1	0	0	X	f1,	j1,	p1,	q1,	r1,	z1
1	1	1	1	g1,	i1,	k1,	p1,	q1,	r1, z1

7)

Find a test sequence to test for *b* s-a-0 in the following sequential circuit:

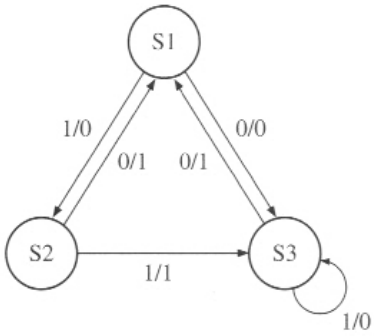


Solution:

Test sequence: '1', '1', '-'. where '-' is a don't care

time	state	input
t0	00	1
t1	10	1
t2	01	-
t3	11 (correct state), 10 (incorrect state)	

8) A sequential circuit has the following State Trasistion Graph, STG.



The three states can be distinguished from one another in properly operating logic network using the input sequence 11 and observing the output. The circuit has a reset input, R, that resets it to the state S1. Give a set of test sequences that will test every state transition and give the transition tested by each sequence.

Solution:

State	Distinguishing Sequence	Output
S1	11	01
S2	11	10
S3	11	00

Testing State	**Input Sequence**	Correct Output	Correct State
S1	**R011**	000	S3
S1	**R111**	010	S2
S2	**R0011**	0101	S1
S2	**R0111**	0000	S3
S3	**R1011**	0101	S1
S3	**R1111**	0100	S3