4.8.1, 4.8.3, 4.9.2, 4.9.4, 4.9.5, 4.9.6,
4.13.1, 4.13.4, 4.15.1, 4.15.2

Chris Bero

HW 4

CPE 431

4.8.1

IF	ID	Ex	Mem	WB
250ps	350ps	150ps	300ps	200ps

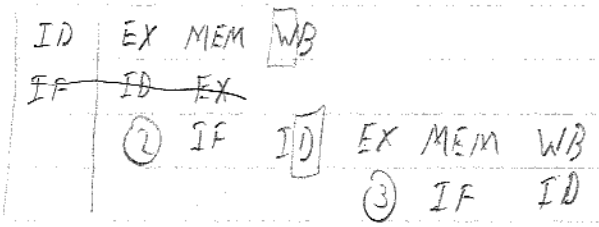
Alu	beq	lw	sw
45%	20%	20%	15%

a. Pipelined: Each section as slow as the slowest. → 350ps
350ps · 5 sections = 1750ps per instruction, but the clock time is 350ps.

a. Non-pipelined: The entire path is one clock cycle: 1250ps

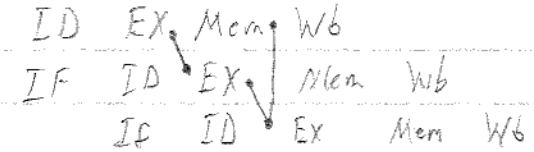
4.8.3 We would split ID into two 175ps stages. The new clock cycle is based off the Mem stage: 300ps · 5 = 1500ps

4.9.2



a.
```
or r1, r2, r3
nop
nop
or r2, r1, r4
nop
nop
or r1, r1, r2
```

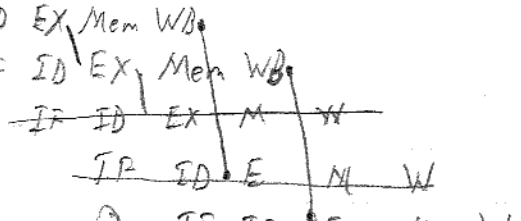
4.9.4



4.9.4 No forwarding: 7 operations, 250ps, 11 cycles → 2750ps
Forwarding: 3 instructions, 300ps, 7 cycles → 2100ps

Speedup: $\left(\frac{11 \cdot 250}{7 \cdot 300}\right) = 1.309 \rightarrow$ 23%

4.9.5 or r1, r2, r3
or r2, r1, r4
or r1, r1, r2



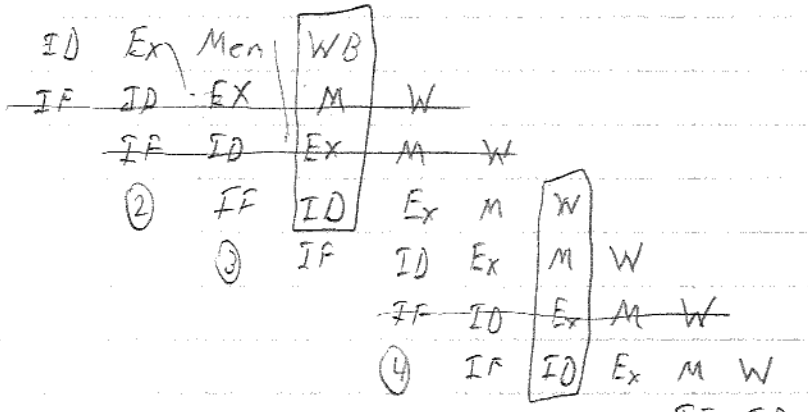
9 or r1, r2, r3
or r2, r1, r4
nop
nop
or r1, r1, r2

4.9.6 ALU-ALU → 9 cycles @ 290ps → 2610ps

Speedup: $\left(\frac{9 \cdot 290}{11 \cdot 250}\right) = 0.95 \rightarrow$ 5%

4.13.1

```
add (r5), r2, r1
lw  (r3), 4(r5)
lw  r2,   0(r2)
or  (r3), r5, (r3)
sw  (r3), 0(r5)
```



a

```
add
nop
nop
lw
lw
nop
or
nop
nop
sw
```

4.13.4

```
1  2  3  4  5
IF ID Ex M  W
   IF ID Ex M  W
      IF ID Ex
         IF ID Ex
            IF ID Ex
```

a Cycle 3: Forward signal
Cycle 5: Hazard signal

4.15.1 Beg → 25% Always taken → 45%
Bad choice 55% of 25% → 13.75%

$0.1375 \cdot 3 = 0.4125$ increase in CPI

4.15.2 $0.25 \cdot 0.45 \cdot 3 = 0.3375$ increase in CPI
Beg Not taken