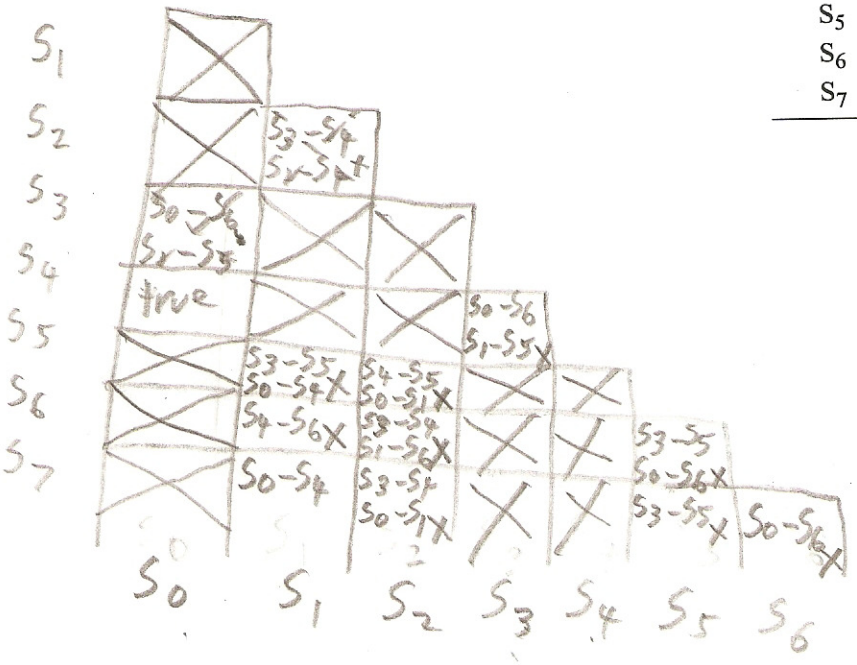
CPE/EE 422/522 **EXAM 1** **Name** KEY

Spring Semester 2009

Work should be performed systematically and neatly with the final answer being underlined. This exam is closed book, closed notes, closed neighbor. Allowable items on desk include: exam, data manual, pencils, straight edge, and calculator. All other items must be removed from student's desk. Students have approximately 90 minutes (1 1/2 hours) to complete this exam. Best wishes!

1. [10 points] Reduce the following state table to a minimum number of states

present state	next state		present output	
	X=0	1	X=0	1
S_0	S_0	S_1	0	0
S_1	S_3	S_4	0	1
S_2	S_4	S_1	0	1
S_3	S_6	S_5	0	0
S_4	S_0	S_1	0	0
S_5	S_5	S_0	0	1
S_6	S_3	S_6	0	1
S_7	S_3	S_0	0	1



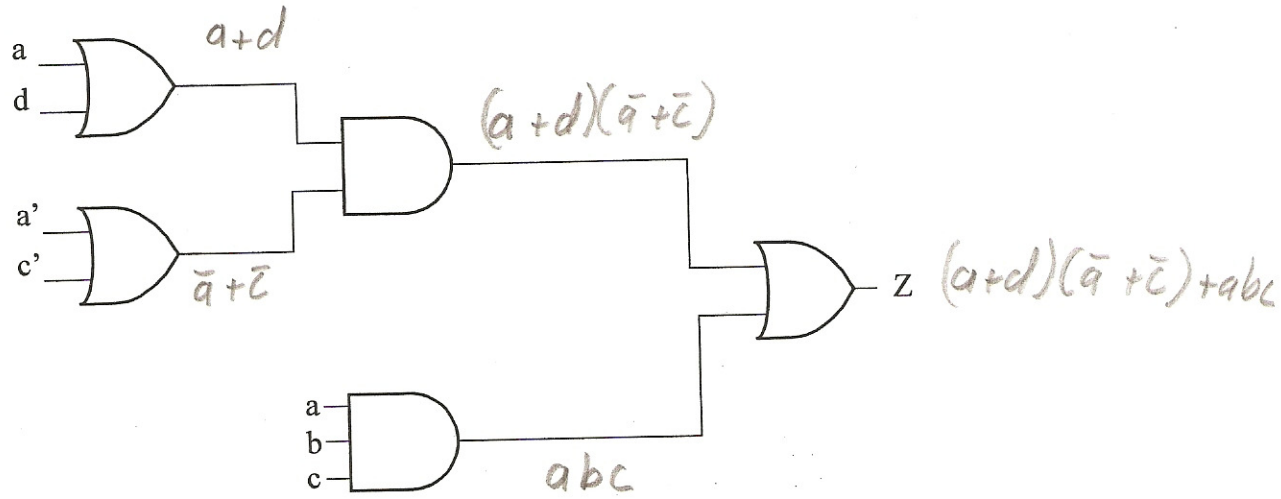
$S_0 \equiv S_4$

$S_1 \equiv S_7$

2. [12 points total] In general, what are static hazards in a combinational network? [2 points]

static hazards are transient incorrect outputs (glitches) that occur in a network that are the result of multiple delay paths from one or more inputs to an output

For the network shown below, find any/all static 0-hazards. For any 0-hazard found specify the conditions which will cause the hazard to appear at the output (i.e. specify the logic values of the variables which are constant and the variable which is changing) [10 points].

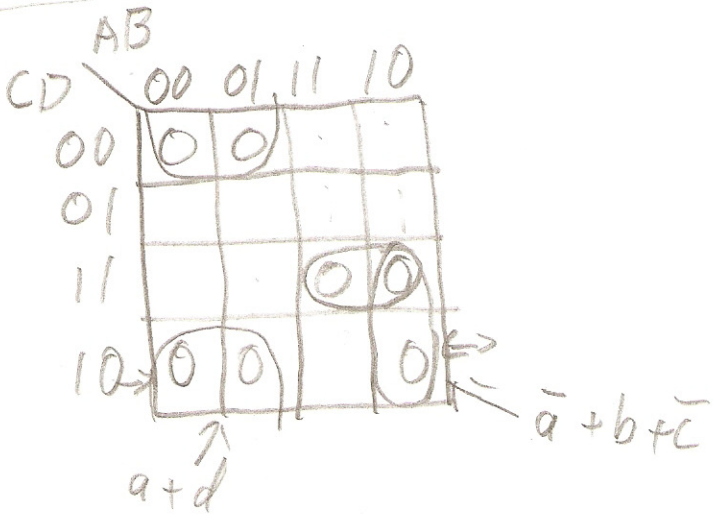


$$F_T = (a+d)(\bar{a}+\bar{c})+abc = [(a+d)(\bar{a}+\bar{c})+a][(a+d)(\bar{a}+\bar{c})+bc]$$
$$= [(a+d)(\bar{a}+\bar{c})+a][\{(a+d)(\bar{a}+\bar{c})+b\}\{(a+d)(\bar{a}+\bar{c})+c\}]$$
$$= [(a+a+d)(a+\bar{a}+\bar{c})][\{(a+d)(\bar{a}+\bar{c})+b\}\{(a+d)(\bar{a}+\bar{c})+c\}]$$
$$= [(a+d)(a+\bar{a}+\bar{c})][\{(a+b+d)(\bar{a}+b+\bar{c})\}\{(a+c+d)(\bar{a}+\bar{c}+c)\}]$$

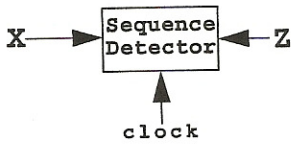
Hazard

A changes

B = 0, C = 1, D = 0

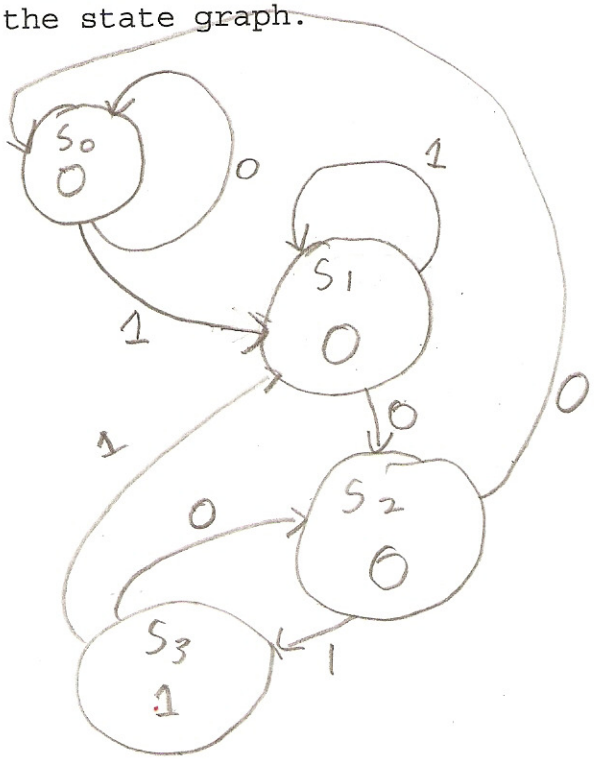


3. [10 points total] Design the state graph of a clocked Moore sequential network implementation of a sequence detector. The network is to examine a strig of 0's and 1's that is supplied on its X input and generate an ouput Z=1 only when a prescribed input sequence occurs (in all other cases an output of Z=0 should be generated). Specifically the network is to be implemented so that any input sequence ending in 101 will produce an output Z=1 coincident (at the same time) with the last 1 in the sequence. The network does not reset with a 1 occurs at the output. The network has the form shown below and a typical input sequence and the corresponding output sequence are also shown below.



X = 0 0 1 1 0 1 1 0 0 1 0 1 0 1 0 0
Z = 0 0 0 0 0 1 0 0 0 0 0 1 0 1 0 0

You are to design the state graph for a Moore sequential network that will implement this design. Use the arc and node labeling convention discussed in the class and label your states S_0, S_1, etc. with S_0 being your beginning state. You are only required to implement the state graph.



4. [5 points] From the next state map of Flip-Flop A shown below, derive the minimized sum-of-products (SOP) input equations for this flip-flop assuming that it is a **T** type Flip-Flop..

Next state map for Flip-Flop A

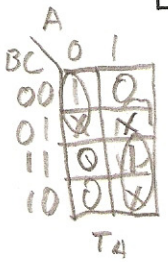
BC \ A	0	1
00	1	1
01	x	x
11	0	0
10	0	x

A^+

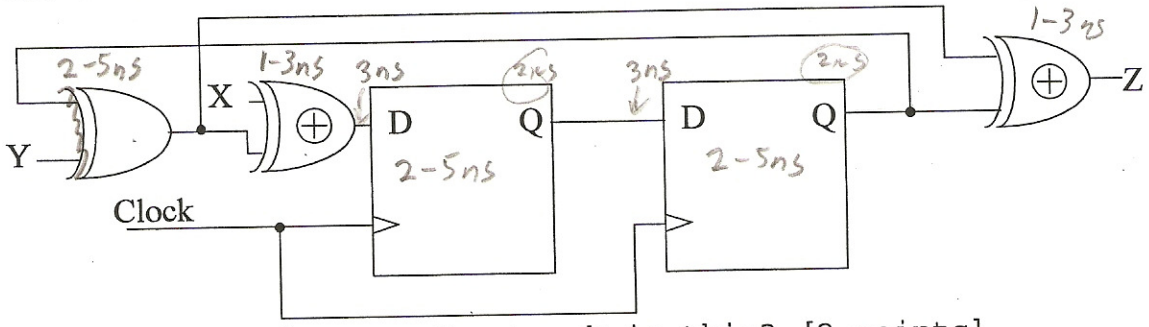
$T_A = \bar{A}\bar{B} + AB$

or

$T_A = \bar{A}\bar{B} + AC$



5. [15 points total] A sequential network is implemented using an OR gate, two XOR gates and two D flip-flops as shown below. Assume that the inputs *X* and *Y* always changes at the same time as the falling edge of the 50% duty cycle clock (clock is high 1/2 cycle then low 1/2 cycle). Also assume the following delay parameters: XOR gate delays range 1 to 3 ns, OR Gate delay ranges from 2 to 5 ns, flip-flop propagation delays range from 2 to 5 ns, setup time requirement 3 ns, hold time requirements are 2 ns.



a) What general type of network is this? [2 points]

Mealy

b) Determine the maximum clock rate for proper synchronous operation. Show all steps [13 points].

Case 1 Flip-flops only

$T_{cyc} \geq 3ns + (5ns + 3ns) + 5ns = 16ns$

($+_{su}$, $+_{cmax}$, T_P)

Case 2 considering the effects of inputs X and Y

$T_X \geq 3ns + (5ns + 3ns) = 11ns$

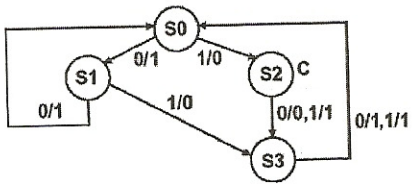
($+_{su}$)

$\frac{1}{2} T_{cyc} \geq T_X$

$T_{cyc} \geq 2 \cdot 11ns = 22ns$

$T_{cmax} = \frac{1}{22ns}$

6. [10 points] Develop a two process VHDL model for the state graph shown below:



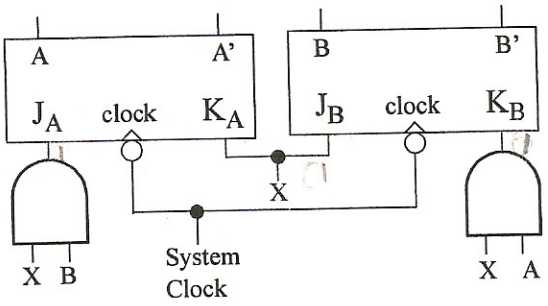

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity SM is
   port(X,CLK: in STD_LOGIC;
            Z : out STD_LOGIC;
   }
end SM;

architecture BEHAVIORAL of SM is
   signal STATE, NEXTSTATE: integer range 0 to 3 :=0;
   begin
      P1:process( STATE, X )
      begin
         if (STATE=0) then
            if (X='1') NEXTSTATE<=2; Z<='1';
            else       NEXTSTATE<=1; Z<='0';
         elseif (STATE=1) then
            if (X='1') then NEXTSTATE<=3; Z<='0';
            else NEXTSTATE<=0; Z<='1';
         else if (STATE=2) then
            NEXTSTATE<=3;
            Z<=X;
         else if (STATE=3) then
            NEXTSTATE<=0;
            Z<='1';
         end if


      end process P1;

      P2:process( CLK      )
      begin
         if (CLK='1') then
            STATE<=NEXTSTATE;
         end if

      end process P2;
end BEHAVIORAL;
```

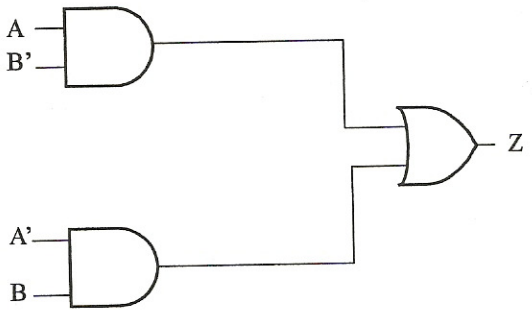
7. [13 points] In the following VHDL model fragment (which corresponds to a portion of the architecture section of a VHDL file) A, B, C, and D are all integers that have a value of 0 at time = 10ns. If E changes from '0' to '1' at time 20 ns, specify the times (s) at which each signal will change and the value to which it will change. List these changes in chronological order. List any delta delays as a separate entry.

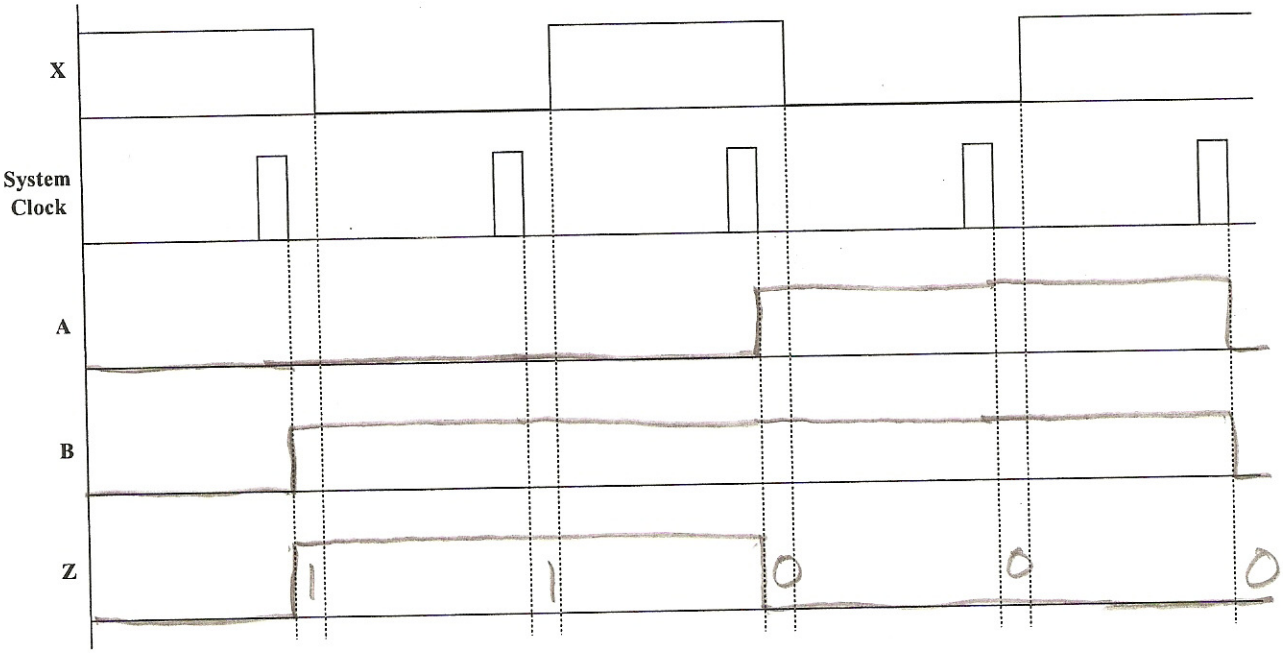
```
P1: process
    begin
       wait on E;
       A <= transport 2 after 7 ns;
       B <= A + 1;
       wait for 0 ns;
       A <= transport A + 5 after 15 ns;
       B <= B + 2;
    end process P1;

C <= A after 10 ns;

P2: process(B)
    begin
       D <= B after 5 ns;
    end process P2;
```

Time	A	B	C	D	E
10 ns	0	0	0	0	0
20ns	0	0	0	0	1
20ns+Δ	0	1	0	0	1
20ns+2Δ	0	3	0	0	1
25ns	0	3	0	3	1
27ns	2	3	0	3	1
35ns	5	3	0	3	1
45ns	5	3	5	3	1

8. [10 points] Complete the following timing diagram for signals A, B, and Z for the network shown below assuming that all setup and hold times for the flip-flops have been met and all propagation delays through the gates and flip-flops are negligible (i.e. zero). Also assume that the two flip-flops are clocked on the falling edge of the system clock and are in the reset state (i.e. A='0' and B='0') at the beginning of the timing diagram.







What type of sequential network is this?

Moore

Write down the output sequence for Z.

1 1 0 0 0

Are there any 'false' outputs on the timing diagram? If so clearly identify them.

no this is a Moore network