Christopher Bero 10-2-2015 CPE 322

Simulation Assignment 01

"RTL & Post FPGA Layout Timing Simulation of two an [sic] 8-bit Subtractor/Adder"

Stimulus

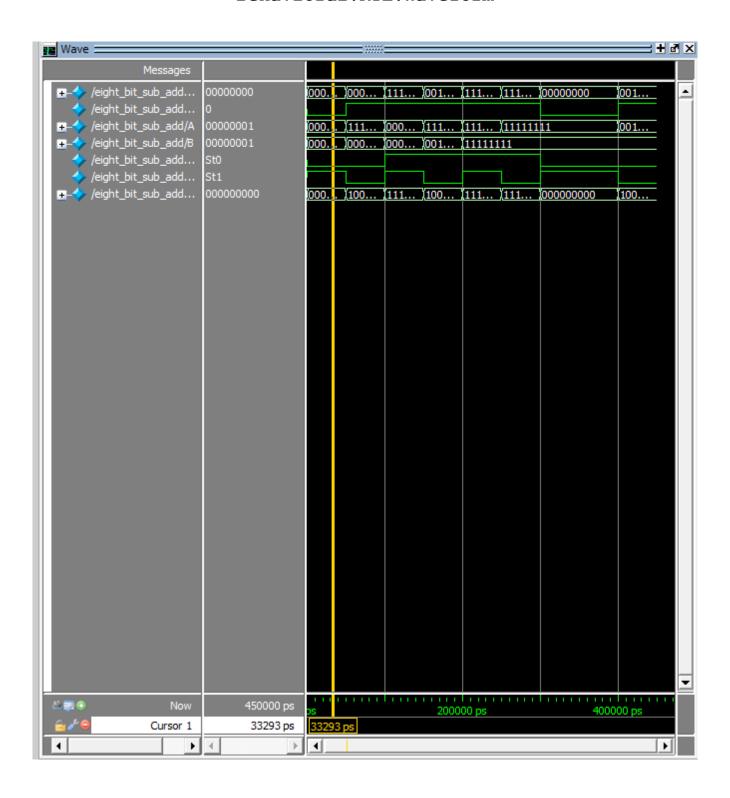
```
# Stimulus for Behavioral Model
# [0] is LSB
# SUB ADD: 0=add (A+B), 1=subtract (A-B)
# Library: cycloneive ver
                                          0 Ons, 0 50ns, 1 100ns, 1 150ns, 1 200ns,
force {sim:/eight bit sub add/B CIN}
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight bit sub add/A[0]}
                                          0 Ons, 1 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 1 400ns
                                          0 Ons, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
force {sim:/eight bit sub add/A[1]}
1 250ns, 1 300ns, 0 350ns, 1 400ns
force {sim:/eight bit sub add/A[2]}
                                          0 Ons, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/A[3]}
                                          0 Ons, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
force {sim:/eight bit sub add/A[4]}
1 250ns, 1 300ns, 1 350ns, 0 400ns
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
force {sim:/eight_bit_sub_add/A[5]}
1 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight bit sub add/A[6]}
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight bit sub add/A[7]}
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 0 200ns,
0 250ns, 1 300ns, 1 350ns, 0 400ns
                                          0 Ons, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
force {sim:/eight bit sub add/B[0]}
1 250ns, 1 300ns, 1 350ns, 1 400ns
force {sim:/eight bit sub add/B[1]}
                                          0 Ons, 0 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[2]}
                                          0 Ons, 0 50ns, 1 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit sub add/B[3]}
                                          0 Ons, 0 50ns, 1 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
force {sim:/eight_bit_sub_add/B[4]}
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight bit sub add/B[5]}
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight bit sub add/B[6]}
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight bit sub add/B[7]}
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
0 250ns, 1 300ns, 1 350ns, 0 400ns
                                          0 Ons, 1 50ns, 0 100ns, 1 150ns, 0 200ns,
force {sim:/eight bit sub add/SUB ADD}
1 250ns, 0 300ns, 1 350ns, 0 400ns
```

run 500ns

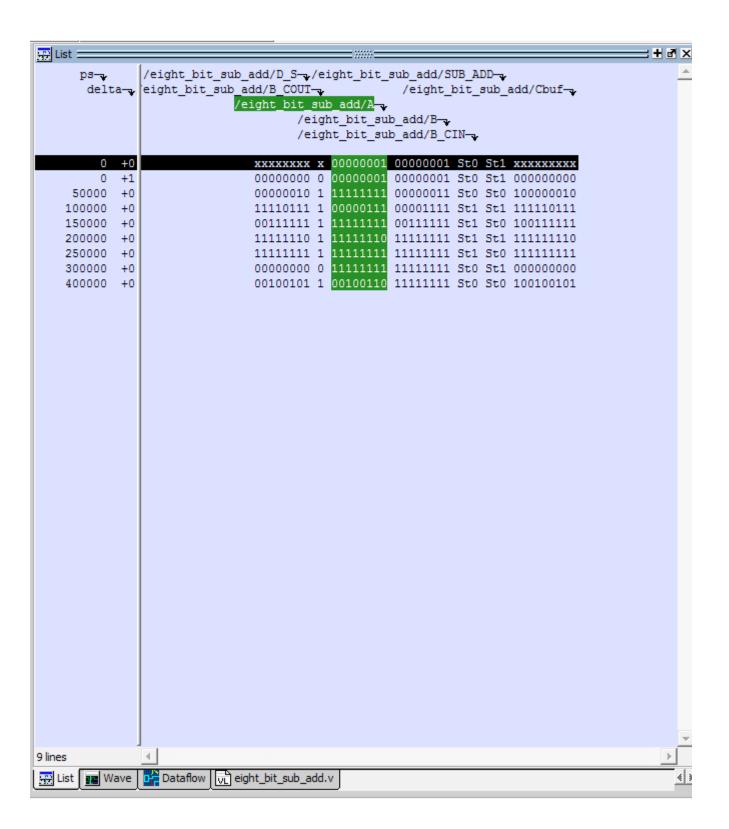
```
# Stimulus for Structural Model
# [0] is LSB
# SUB ADD: 0=add (A+B), 1=subtract (A-B)
# Library: cycloneive ver
                                          0 Ons, 0 50ns, 1 100ns, 1 150ns, 1 200ns,
force {sim:/eight bit sub add/B CIN}
1 250ns, 1 300ns, 0 350ns, 0 400ns
                                          0 Ons, 1 50ns, 1 100ns, 1 150ns, 1 200ns,
force {sim:/eight_bit_sub_add/A[0]}
1 250ns, 1 300ns, 1 350ns, 1 400ns
force {sim:/eight bit sub add/A[1]}
                                          0 Ons, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 1 400ns
force {sim:/eight bit sub add/A[2]}
                                          0 Ons, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
                                          0 Ons, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
force {sim:/eight bit sub add/A[3]}
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight bit sub add/A[4]}
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight_bit_sub_add/A[5]}
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight bit sub add/A[6]}
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight bit sub add/A[7]}
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 0 200ns,
0 250ns, 1 300ns, 1 350ns, 0 400ns
                                          0 Ons, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
force {sim:/eight bit sub add/B[0]}
1 250ns, 1 300ns, 1 350ns, 1 400ns
force {sim:/eight bit sub add/B[1]}
                                          0 Ons, 0 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[2]}
                                          0 Ons, 0 50ns, 1 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
                                          0 Ons, 0 50ns, 1 100ns, 0 150ns, 1 200ns,
force {sim:/eight bit sub add/B[3]}
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[4]}
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 0 350ns, 0 400ns
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
force {sim:/eight bit sub add/B[5]}
1 250ns, 1 300ns, 0 350ns, 0 400ns
force {sim:/eight_bit_sub_add/B[6]}
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight bit sub add/B[7]}
                                          0 Ons, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
0 250ns, 1 300ns, 1 350ns, 0 400ns
force {sim:/eight_bit_sub_add/SUB_ADD}
                                          0 Ons, 1 50ns, 0 100ns, 1 150ns, 0 200ns,
1 250ns, 0 300ns, 1 350ns, 0 400ns
```

run 500ns

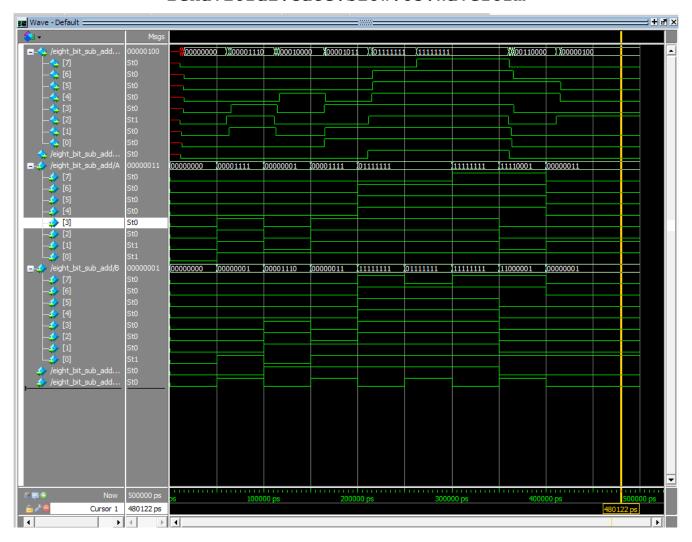
Behavioral:RTL:Waveform



Behavioral:RTL:List



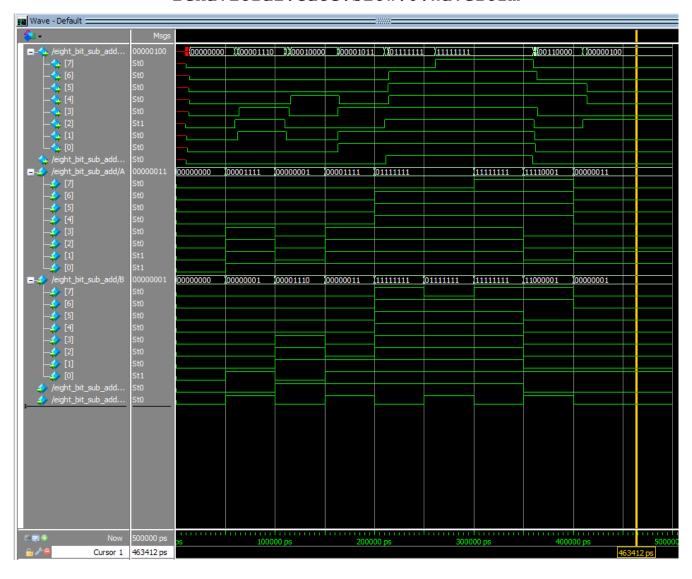
Behavioral: Gate: Slow: 85: Waveform



Behavioral:Gate:Slow:85:List

List - Defaul	t =									
		/eight bit sub add/D S-	/eial	ht bit sul	b add/B					
- +		/eight_bit_sub_add/D_S-,/eight_bit_sub_add/B-, /eight_bit_sub_add/B_COUT-,								
4010	Ψ		/eight_bit_sub_add/A-							
				ht bit sul		TN				
		· '		ight_bit_s						
			, -	rg.no_bro	_uua, 5		*			
10769	+0	xxxxx0xx	StX	00000000	00000000	St0	St0			
11327				00000000						
12013	+0			00000000						
12410	+0	0xxxx00x	St0	00000000	00000000	St0	St0			
13522	+0	0xxxx000	St0	00000000	00000000	St0	St0			
14610	+0	0xxx0000	St0	00000000	00000000	St0	St0			
14639	+0	0x0x0000	St0	00000000	00000000	St0	St0			
15310	+0	000x0000	St0	00000000	00000000	St0	St0			
15618	+0	00000000	St0	00000000	00000000	St0	St0			
50000	+0			00001111						
60389	+0	00000100	St0	00001111	00000001	St0	St1			
63044	+0	00000110	St0	00001111	00000001	St0	St1			
65084	+0			00001111						
100000	+0			00000001						
111540	+0			00000001						
113258	+0			00000001						
	+0			00000001						
116770				00000001						
150000	+0			00001111						
163910				00001111						
164096				00001111						
164584 165822	+0			00001111						
200000	+0			01111111						
210836	+0			01111111						
211092	+0			01111111						
215103	+0			01111111						
215138	+0			01111111						
215150	+0			01111111						
250000	+0			01111111						
262528	+0			01111111						
300000	+0	11111111	St1	11111111	11111111	St1	St0			
350000	+0	11111111	St1	11110001	11000001	St0	St1			
360115	+0	11111011	St1	11110001	11000001	St0	St1			
360515	+0	11111011	St0	11110001	11000001	St0	St1			
360853	+0	01111011	St0	11110001	11000001	St0	St1			
362593	+0	01111001	St0	11110001	11000001	St0	St1			
363420	+0			11110001						
365080	+0			11110001						
365597	+0			11110001						
400000	+0			00000011						
410418	+0			00000011						
415204	+0			00000011						
415380	+0	00000100	St0	00000011	00000001	St0	St0			

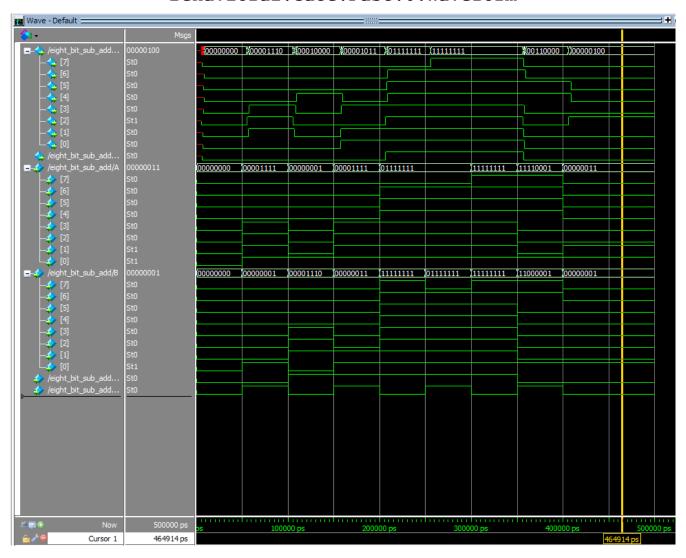
Behavioral: Gate: Slow: 0: Waveform



Behavioral:Gate:Slow:0:List

Eist - Defau	lt =						
		/eight_bit_sub_add/D_S	/eia	ht bit sul	b add/B		
		/eight_bit_sub_add/B_CO					
	v	/eight bit		b add/A			
				ht bit sul	b add/B C	TN	
		·		ight_bit_			DD—.
			, -	-9			₩
9503	+0	xxxxx0xx	StX	00000000	00000000	St0	St0
9990	+0			00000000			
10605	+0	0xxxx0xx	St0	00000000	00000000	St0	St0
10994	+0	0xxxx00x	St0	00000000	00000000	St0	St0
11984	+0	0xxxx000	St0	00000000	00000000	St0	St0
12966	+0	0xxx0000	St0	00000000	00000000	St0	St0
13013	+0	0x0x0000	St0	00000000	00000000	St0	St0
13591	+0	000x0000	St0	00000000	00000000	St0	St0
13878	+0	00000000	St0	00000000	00000000	St0	St0
50000	+0	00000000	St0	00001111	00000001	St0	St1
59350	+0	00000100	St0	00001111	00000001	St0	St1
61864	+0	00000110	St0	00001111	00000001	St0	St1
63821	+0	00001110	St0	00001111	00000001	St0	St1
100000	+0	00001110	St0	00000001	00001110	St1	St0
110000	+0	00001010	St0	00000001	00001110	St1	St0
111197	+0	00001000	St0	00000001	00001110	St1	St0
113683	+0	00000000	St0	00000001	00001110	St1	St0
115395	+0	00010000	St0	00000001	00001110	St1	St0
150000	+0	00010000	St0	00001111	00000011	St1	St1
162732				00001111			
162817				00001111			
163234				00001111			
164201				00001111			
200000				01111111			
210042	+0			01111111			
211295				01111111			
213835				01111111			
213855				01111111			
213900				01111111			
250000 261317				01111111			
	+0			11111111			
300000				11111111			
350000 359346				11110001			
359665				11110001			
360228	+0			11110001			
361197	+0			11110001			
361930	+0			11110001			
363475	+0			11110001			
363911				11110001			
400000				00000011			
409336				00000011			
413545				00000011			
413704	+0			00000011			
220,01		1					

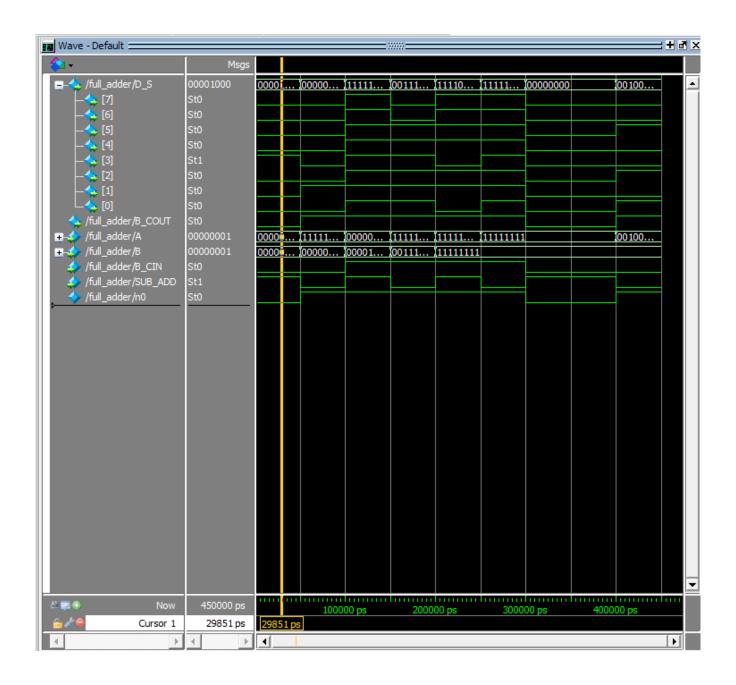
Behavioral:Gate:Fast:0:Waveform



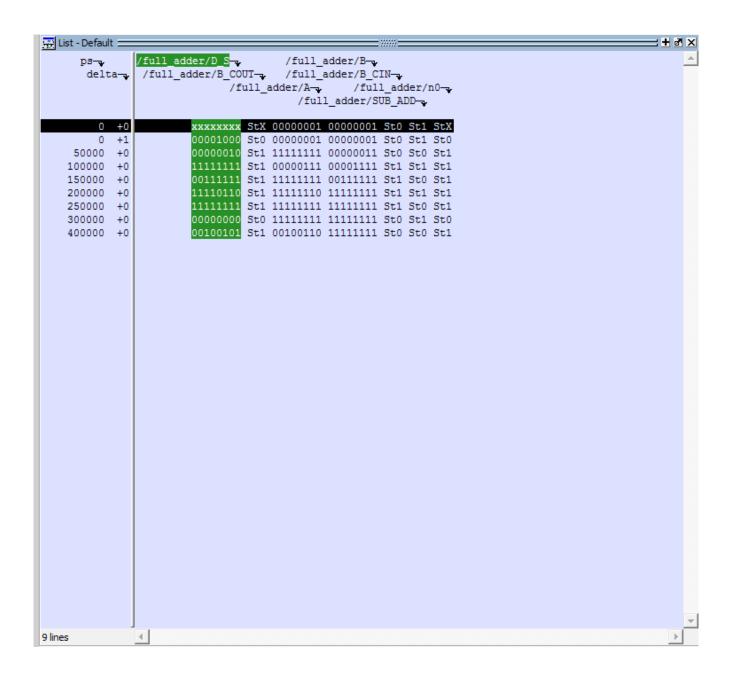
Behavioral:Gate:Fast:0:List

PS- delta	List - Default	,								
delta		(sight hit sub add/D C	/ i1		dd /D					
Feight_bit_sub_add/A										
Feight_bit_sub_add/B_CIN-	αerta⊸•									
		_			44/D C	T3.T				
S858 +0		·					nn.			
6137 +0 6337 +0 6337 +0 0xxxx0xx St0 00000000 00000000 St0 St0 6854 +0 0xxxx00x St0 00000000 00000000 St0 St0 St0 6854 +0 0xxxx000 St0 00000000 00000000 St0 St0 80 0000000 St0 St0 00000000 St0 St0 8086 +0 0xxxx0000 St0 00000000 00000000 St0 St0 8134 +0 0x0x0000 St0 00000000 00000000 St0 St0 8614 +0 0x0x0000 St0 00000000 0000000 St0 St0 8614 +0 0x0x0000 St0 00000000 St0 St0 8614 +0 0x0x0000 St0 00000000 St0 St0 8614 +0 0x0x0000 St0 00000000 St0 St0 St0 St0 8614 +0 0x0x0000 St0 00000000 St0 St0 St0 St0 8614 +0 0x0x0000 St0 00000000 0000000 St0 St0 St0 8614 +0 0x0x0000 St0 00000000 00000000 St0 St0 St0 8614 +0 0x0x0000 St0 00000000 00000000 St0 St0 St0 100000000 St0 St0 St0 100000000 St0 St0 St0 10000000000			/e:	ignt_bit_	sub_add/5	UB_AI	Ψ-αα			
6137 +0 6337 +0 6337 +0 0xxxx0xx St0 00000000 00000000 St0 St0 6854 +0 0xxxx00x St0 00000000 00000000 St0 St0 St0 6854 +0 0xxxx000 St0 00000000 00000000 St0 St0 80 0000000 St0 St0 00000000 St0 St0 8086 +0 0xxxx0000 St0 00000000 00000000 St0 St0 8134 +0 0x0x0000 St0 00000000 00000000 St0 St0 8614 +0 0x0x0000 St0 00000000 0000000 St0 St0 8614 +0 0x0x0000 St0 00000000 St0 St0 8614 +0 0x0x0000 St0 00000000 St0 St0 8614 +0 0x0x0000 St0 00000000 St0 St0 St0 St0 8614 +0 0x0x0000 St0 00000000 St0 St0 St0 St0 8614 +0 0x0x0000 St0 00000000 0000000 St0 St0 St0 8614 +0 0x0x0000 St0 00000000 00000000 St0 St0 St0 8614 +0 0x0x0000 St0 00000000 00000000 St0 St0 St0 100000000 St0 St0 St0 100000000 St0 St0 St0 10000000000	E0E0 TU	vvvvv0vv	C+V	00000000	00000000	S+0	S+O			
6337 +0 6854 +0 0xxxx0xx St0 00000000 00000000 St0 St0 7396 +0 0xxxx000 St0 00000000 00000000 St0 St0 80 8086 +0 0xxx0000 St0 00000000 00000000 St0 St0 8134 +0 0x0x0000 St0 00000000 00000000 St0 St0 8134 +0 0x0x0000 St0 00000000 00000000 St0 St0 8614 +0 0x0x0000 St0 00000000 0000000 St0 St0 8614 +0 0x0x0000 St0 00000000 St0 0000000 St0 St0 St										
6854 +0 OXXXXXOX StD 00000000 00000000 StD StD 80 8086 +0 OXXXX000 StD 00000000 00000000 StD StD 80 8086 +0 OXXXX000 StD 00000000 00000000 StD StD 80 8134 +0 OXXXX000 StD 00000000 00000000 StD StD 80 8134 +0 OXXXX000 StD 00000000 00000000 StD StD 80 8134 +0 OXXXX000 StD 00000000 00000000 StD StD 80 8134 +0 OXXXX000 StD 00000000 00000000 StD StD 80 8134 +0 OXXXX000 StD 00000000 00000000 StD StD 80 8134 +0 OXXXX000 StD 00000000 00000000 StD StD 80 8134 +0 OXXXX000 StD 00000000 0000000 StD StD 8135 +0 OXXXX000 StD 00000111 00000001 StD StD 8135 +0 OXXXX000 StD 00000111 00000001 StD StD 8135 +0 OXXXX000 StD 00000111 00000001 StD 8135 +0 OXXXX000 StD 00000111 0000001 StD 8135 +0 +0 OXXXX000 StD 0000001 00001110 StD 8135 +0										
7396 +0 8086 +0 0xxx0000 St0 00000000 00000000 St0 St0 8134 +0 8134 +0 800000 St0 00000000 00000000 St0 St0 843 +0 8431 +0 8614 +0 00000000 St0 00000000 00000000 St0 St0 863 +0 8614 +0 00000000 St0 00000000 00000000 St0 St0 863 +0 8614 +0 00000000 St0 00000000 00000000 St0 St0 50 8614 +0 00000000 St0 00000111 00000001 St0 St1 55304 +0 00000100 St0 00001111 00000001 St0 St1 55304 +0 0000110 St0 00001111 00000001 St0 St1 10000001 St0 St1 100000000 +0 0000110 St0 00001111 00000001 St0 St1 10000001 St0 St1 1000000000 +0 0000110 St0 00000111 00000001 St0 St1 100000000 +0 0000110 St0 00000011 00001110 St1 St0 10000001 St0 St1 100000000 +0 0000110 St0 00000001 00001110 St1 St0 100000000 +0 0000100 St0 00000001 00001110 St1 St0 10000000 +0 0000000 St0 00000001 00001110 St1 St0 10000000 +0 0001000 St0 00000001 00001110 St1 St1 157112 +0 0001000 St0 00000011 00000011 St1 St1 157321 +0 0001001 St0 00000111 00000011 St1 St1 158062 +0 0001001 St0 00001111 00000011 St1 St1 158062 +0 0001011 St0 00001111 00000011 St1 St1 158062 +0 0001011 St0 00001111 00000011 St1 St1 20000000 +0 0000000 St0 00000111 00000011 St1 St1 158062 +0 0001011 St0 00001111 00000011 St1 St1 200000011 St1 St1 158062 +0 0001011 St0 00001111 St0 00001111 St1 St1 St0 20000000000000000000000000000000000										
8086 +0 0xxx00000 StO 00000000 00000000 StO StO 8134 +0 0x0x00000 StO 00000000 00000000 StO StO 8431 +0 000x00000 StO 00000000 00000000 StO StO 8614 +0 00000000 StO 00000000 00000000 StO StO 50000 +0 00000000 StO 00000111 00000000 StO StO 55304 +0 00000100 StO 0000111 00000001 StO StI 56624 +0 0000110 StO 0000111 00000001 StO StI 100000 +0 0000110 StO 0000001 1000111 StO 105836 +0 00001010 StO 0000001 0000110 StI StO 108949 +0 00001000 StO 0000001 00001110 StI StO 157012 +0 00010000 StO 0000001 00001110 StI StI 157921 +0 00010000 StO 0000001 00001110 StI StI 157000										
8134 +0 0x0x0000 St0 00000000 00000000 St0 St0 St0 8431 +0 000x0000 St0 00000000 00000000 St0 St0 St0 8614 +0 000x0000 St0 00000000 00000000 St0 St0 St0 50000 +0 00000000 St0 00000111 00000001 St0 St1 55304 +0 00000100 St0 00001111 00000001 St0 St1 56624 +0 00001110 St0 00001111 00000001 St0 St1 100000 +0 00001110 St0 00000111 0000001 St0 St1 105836 +0 00001110 St0 0000001 00001110 St1 St0 107249 +0 00001000 St0 0000001 00001110 St1 St0 108587 +0 00000000 St0 0000001 00001110 St1 St0 108994 +0 00010000 St0 0000001 00001110 St1 St0 157112 +0 00010000 St0 0000001 0000111 St1 St1 157321 +0 0001001 St0 0000111 00000011 St1 St1 159582 +0 00010011 St0 0000111 00000011 St1 St1 205955 +0 0001011 St0 0001111 00000011 St1 St1 207383 +0 00001011 St0 0111111 11111111 St1 St0 207383 +0 0010111 St1 0111111 1111111 St1 St0 208648 +0 0111111 St1 0111111 1111111 St1 St0 208648 +0 0111111 St1 0111111 1111111 St1 St0 208648 +0 0111111 St1 11111001 11000001 St0 St1 356510 +0 01111111 St1 1111001 1100001 St0 St1 <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th>										
8431 +0 000x0000 St0 00000000 00000000 St0 St0 St0 8614 +0 00000000 St0 00000000 00000000 St0 St0 S										
8614 +0 50000 +0 50000 +0 50000000 St0 00000000 00000000 St0 St1 55304 +0 00000100 St0 00001111 00000001 St0 St1 56624 +0 00000110 St0 00001111 00000001 St0 St1 100000 +0 105836 +0 105836 +0 105836 +0 107249 +0 10000100 St0 0000001 0000110 St1 St0 108587 +0 108587 +0 108587 +0 108587 +0 108000 St0 0000001 0000110 St1 St0 157321 +0 157321 +0 157321 +0 157321 +0 157321 +0 158062 +0 159080 +0 159										
S0000 +0										
55304 +0 00000100 St0 00001111 00000001 St0 St1 56624 +0 00000110 St0 00001111 00000001 St0 St1 57620 +0 00001110 St0 00001111 00000001 St0 St1 100000 +0 00001110 St0 0000001 00001110 St1 St0 105836 +0 00001010 St0 00000001 00001110 St1 St0 107249 +0 00000000 St0 00000001 00001110 St1 St0 108587 +0 00000000 St0 00000001 00001110 St1 St0 108994 +0 00010000 St0 00000011 00001110 St1 St0 150000 +0 00010000 St0 00000111 00000011 St1 St1 157112 +0 00010001 St0 00001111 00000011 St1 St1 158062 +0 00010011 St0 00001111 00000011 St1 St1 159582 +0 00001001 St0 00001111 00000011 St1 St1 205955 +0 00001011 St0 00111111 11111111 St1 St0 206163 +0 00001011 St1 0111111 11111111 St1 St0 207383 +0 00101111 St1 0111111 11111111 St1 St0 208648 +0 01111111 St1 01111111 1111111 St1 St0 208648 +0 01111111 St1 01111111 1111111 St1 St0 205571 +0 11111111 St1 11111001 11000001 St0 St1 356510 +0 11111111 St1 11110001 11000001 St0 St1 357087 +0 01111001 St0 11110001 11000001 St0 St1										
56624 +0 00000110 St0 00001111 00000001 St0 St1 57620 +0 00001110 St0 00001111 00000001 St0 St1 100000 +0 00001110 St0 00000001 00001110 St1 St0 105836 +0 00001010 St0 00000001 00001110 St1 St0 107249 +0 00001000 St0 00000001 00001110 St1 St0 108587 +0 00000000 St0 00000001 00001110 St1 St0 108994 +0 00010000 St0 0000001 00001110 St1 St0 150000 +0 00010000 St0 00000111 00000011 St1 St1 157321 +0 00010001 St0 00001111 00000011 St1 St1 158062 +0 0001011 St0 00001111 00000011 St1 St1 159582 +0 00001011 St0 00001111 00000011 St1 St1 200000 +0 00001011 St0 01111111 11111111 St1 St0 206163 +0 00001011 St1 0111111 11111111 St1 St0 207383 +0 00101111 St1 01111111 11111111 St1 St0 208648 +0 01111111 St1 01111111 1111111 St1 St0 208648 +0 01111111 St1 01111111 1111111 St1 St0 255571 +0 11111111 St1 01111111 1111111 St1 St0 350000 +0 11111111 St1 111110001 11000001 St0 St1 357087 +0 01111011 St1 11110001 11000001 St0 St1 3576510 +0 11111001 St0 11110001 11000001 St0 St1										
57620 +0 00001110 St0 00001111 00000001 St0 St1 100000 +0 00001110 St0 0000001 00001110 St1 St0 105836 +0 00001010 St0 00000001 00001110 St1 St0 107249 +0 00001000 St0 00000001 00001110 St1 St0 108587 +0 00000000 St0 00000001 00001110 St1 St0 108994 +0 00010000 St0 0000001 00001110 St1 St0 150000 +0 00010000 St0 00001111 00000011 St1 St1 157112 +0 00010001 St0 00001111 00000011 St1 St1 158062 +0 00010011 St0 00001111 00000011 St1 St1 159582 +0 00010011 St0 00001111 00000011 St1 St1 200000 +0 00001011 St0 00001111 00000011 St1 St1 205955 +0 00001011 St1 0111111 11111111 St1 St0 207383 +0 00001011 St1 0111111 11111111 St1 St0 208648 +0 01101111 St1 0111111 11111111 St1 St0 208648 +0 01111111 St1 01111111 1111111 St1 St1 255571 +0 11111111 St1 01111111 11111111 St1 St1 350000 +0 11111111 St1 11110001 11000001 St0 St1 357607 +0 11111011 St1 11110001 11000001 St0 St1 357271 +0 01111001 St0 11110001 11000001 St0 St1 357605 +0 01111001 St0 11110001 11000001 St0 St1										
100000										
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157321 +0 00010011 St0 00001111 00000011 St1 St1 158062 +0 00011011 St0 00001111 00000011 St1 St1 159582 +0 00001011 St0 00001111 00000011 St1 St1 200000 +0 00001011 St0 01111111 11111111 St1 St0 205955 +0 00001011 St1 01111111 11111111 St1 St0 206163 +0 00001111 St1 01111111 11111111 St1 St0 207383 +0 00101111 St1 01111111 11111111 St1 St0 208264 +0 01101111 St1 01111111 1111111 St1 St0 208648 +0 01111111 St1 01111111 1111111 St1 St0 250000 +0 01111111 St1 01111111 0111111 St1 St1 255571 +0 11111111 St1 01111111 0111111 St1 St1 350000 +0 11111111 St1 1111111 1111111 St1 St1 350000 +0 11111111 St1 11111111 1111111 St1 St1 357087 +0 11111111 St1 111110001 11000001 St0 St1 357249 +0 01111001 St1 11110001 11000001 St0 St1 357271 +0 01111001 St0 11110001 11000001 St0 St1 3578082 +0 01110000 St0 11110001 11000001 St0 St1 359336 +0 0110000 St0 11110001 11000001 St0 St1 405723 +0 001101000 St0 00000011 00000001 St0 St0										
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357605 +0 01111000 St0 11110001 11000001 St0 St1 358082 +0 01110000 St0 11110001 11000001 St0 St1 359336 +0 00110000 St0 11110001 11000001 St0 St1 400000 +0 00110000 St0 00000011 00000001 St0 St0 405723 +0 00110100 St0 00000011 00000001 St0 St0										
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400000 +0 00110000 St0 00000011 00000001 St0 St0 405723 +0 00110100 St0 00000011 00000001 St0 St0										
405723 +0 00110100 St0 00000011 00000001 St0 St0										
408701 +0 00010100 St0 00000011 00000001 St0 St0										
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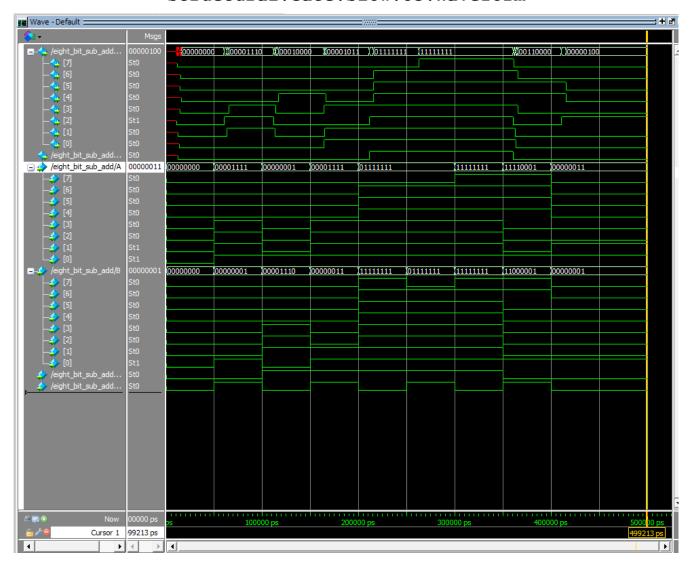
Structural:RTL:Waveform



Structural:RTL:List



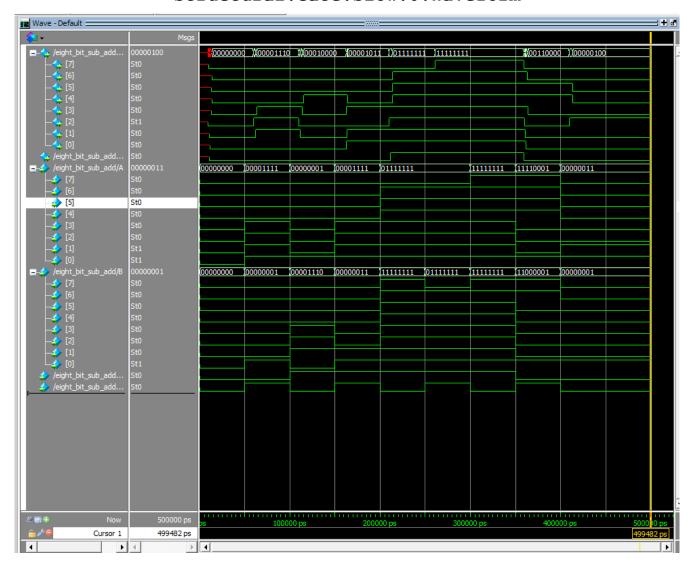
Structural: Gate: Slow: 85: Waveform



Structural:Gate:Slow:85:List

List - Defaul	t <u> </u>	, <u>-</u>					
ps- v		/eight_bit_sub_add/D_S-	/eigl	ht_bit_su	b_add/B-		
delt	.a¥						
		/eight_bit	t_sul	o_add/A <mark>-</mark>			
			/eigl	ht_bit_su	b_add/B_C	IN⊸	
			/e:	ight_bit_	sub_add/S	JB_A	DD⊸•
10769	+0	vvvvv∩vv	S+V	00000000	00000000	S+0	S+O
11327	+0	XXXXXXX			00000000		
12013	+0				00000000		
12410	+0			_	00000000		
13522	+0				00000000		
14610	+0	0xxx0000			00000000		
14639	+0	0x0x0000			00000000		
15310	+0				00000000		
15618	+0	00000000			00000000		
50000	+0	00000000			00000001		
60389	+0	00000100			00000001		
63044	+0	00000110	St0		00000001		
65084	+0	00001110			00000001		
100000	+0	00001110	St0		00001110		
111540	+0	00001010			00001110		
113258	+0	00001000	St0	00000001	00001110	St1	St0
114013	+0	00000000	St0	00000001	00001110	St1	St0
116770	+0	00010000	St0	00000001	00001110	St1	St0
150000	+0	00010000	St0	00001111	00000011	St1	St1
163910	+0	00011000	St0	00001111	00000011	St1	St1
164096	+0	00011001	St0	00001111	00000011	St1	St1
164584	+0	00011011	St0	00001111	00000011	St1	St1
165822	+0	00001011	St0	00001111	00000011	St1	St1
200000	+0	00001011	St0	01111111	11111111	St1	St0
210836	+0	00001011	St1		11111111		
211092	+0	00001111			11111111		
215103	+0	00011111			11111111		
215138	+0	00111111			11111111		
215150	+0	01111111			11111111		
250000	+0	01111111			01111111		
262528	+0				01111111		
300000	_				11111111		
350000	+0				11000001		
360115	+0				11000001		
360515	+0				11000001		
360853	+0				11000001		
362593	+0				11000001 11000001		
363420	+0				11000001		
365080 365597	+0				11000001		
400000	+0				00000001		
410418	+0				00000001		
415204	+0				00000001		
415380	+0				00000001		
110000		00000100	200	55555511	20000001	250	200

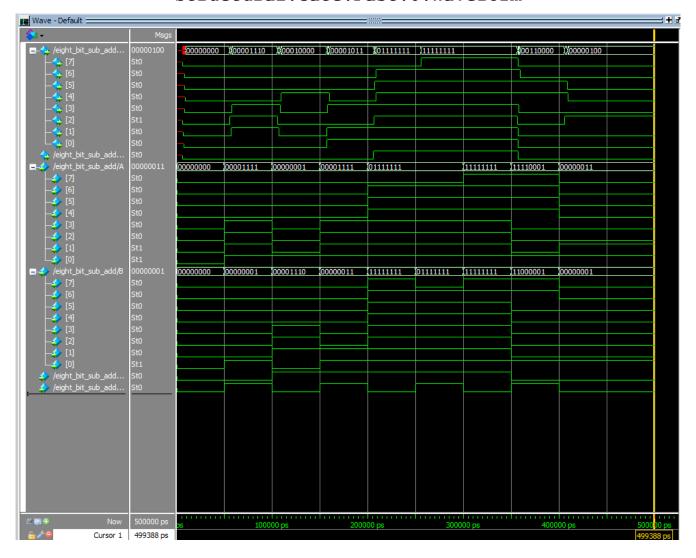
Structural:Gate:Slow:0:Waveform



Structural:Gate:Slow:0:List

	Eist - Defaul	t =	·					
	_		/eight_bit_sub_add/D_S	/aim	ht hit oul	n add/R—		
			/eight bit sub add/B_CO		ic_bic_su	b_add/b-\$		
	dero	,u +	/eight_bit_sub_add/b_com		n add/7.—			
			_			o_add/B_C	TNI	
			·			sub add/SI		nn
				/ -	rgirc_brc	sub_add/5	D_A	DD ₩
	0	+0	xxxxxxxx	StX	00000000	00000000	St.0	St.0
	0	+1				00000000		
	0					00000000		
	9503					00000000		
	9990	+0	0xxxx0xx	StX	00000000	00000000	St0	St0
	10605	+0	0xxxx0xx	St0	00000000	00000000	St0	St0
	10994	+0	0xxxx00x	St0	00000000	00000000	St0	St0
	11984	+0	0xxxx000	St0	00000000	00000000	St0	St0
	12966	+0	0xxx0000	St0	00000000	00000000	St0	St0
	13013	+0	0x0x0000	St0	00000000	00000000	St0	St0
	13591	+0	000x0000	St0	00000000	00000000	St0	St0
	13878	+0	00000000	St0	00000000	00000000	St0	St0
	50000	+0	00000000	St0	00001111	00000001	St0	St1
	59350	+0	00000100	St0	00001111	00000001	St0	St1
	61864	+0	00000110	St0	00001111	00000001	St0	St1
	63821	+0	00001110	St0	00001111	00000001	St0	St1
	100000	+0	00001110	St0	00000001	00001110	St1	St0
	110000	+0	00001010	St0	00000001	00001110	St1	St0
	111197	+0	00001000	St0	00000001	00001110	St1	St0
	113683					00001110		
	115395					00001110		
	150000					00000011		
	162732	+0				00000011		
	162817	+0				00000011		
	163234					00000011		
	164201	+0				00000011		
	200000 210042					11111111		
	211295					11111111		
	213835					111111111		
	213855	+0				111111111		
	213900	+0				11111111		
	250000	+0				01111111		
	261317	+0				01111111		
	300000	+0				11111111		
	350000	+0				11000001		
	359346	+0				11000001		
	359665	+0				11000001		
	360228	+0				11000001		
	361197	+0				11000001		
	361930	+0				11000001		
	363475	+0	00111000	St0	11110001	11000001	St0	St1
	363911	+0	00110000	St0	11110001	11000001	St0	St1
	400000	+0	00110000	St0	00000011	00000001	St0	St0
1								

Structural:Gate:Fast:0:Waveform



Structural:Gate:Fast:0:List

Eist - Defaul	t <u> </u>									
ps- _v		/eight_bit_sub_add/D_S,	/eigi	ht bit sul	b add/B-					
delt	a	/eight_bit_sub_add/B_COUT-								
	•	/eight_bit_sub_add/A-								
		_	/eight_bit_sub_add/B_CIN-							
				ight_bit_			DD-			
5858	+0			00000000						
6137	+0			00000000						
6337	+0			00000000						
6854	+0			00000000						
7396	+0			00000000						
8086	+0			00000000						
8134	+0			00000000						
8431 8614	+0			00000000						
50000	+0			000001111						
55304	+0			00001111						
56624	+0			00001111						
57620	+0			00001111						
100000	+0			00000001						
105836	+0			00000001						
107249	+0	00001000	St0	00000001	00001110	St1	St0			
108587	+0	00000000	St0	00000001	00001110	St1	St0			
108994	+0	00010000	St0	00000001	00001110	St1	St0			
150000	+0	00010000	St0	00001111	00000011	St1	St1			
157112	+0	00010001	St0	00001111	00000011	St1	St1			
157321	+0			00001111						
158062	+0			00001111						
159582	+0			00001111						
200000	+0			01111111						
205955	+0			01111111						
206163 207383	+0			01111111						
207363	+0			01111111						
208648	+0			01111111						
250000	+0			01111111						
255571	+0			01111111						
300000	+0			11111111						
350000	+0	11111111	St1	11110001	11000001	St0	St1			
356510	+0	11111011	St1	11110001	11000001	St0	St1			
357087	+0	01111011	St1	11110001	11000001	St0	St1			
357249	+0	01111001	St1	11110001	11000001	St0	St1			
357271	+0	01111001	St0	11110001	11000001	St0	St1			
357605	+0			11110001						
358082	+0			11110001						
359336	+0			11110001						
400000	+0			00000011						
405723	+0			00000011						
408701	+0			00000011						
409185	+0	00000100	St0	00000011	00000001	StO	StO			

Discussion

Without a definition for glitch to act as a basis for the assignment, pinpointing one is a nontrivial task. As observed, we did not notice anything worthy of a glitch, as the system appeared to operate correctly after troubleshooting to start Model-Sim was successful. Again, significant is not described to us, and the models appeared to have very similar output which leads us to believe that there is not a significant difference between behavioral and structural representations of the system in verilog. Since we have not implemented any activity based on the output of the simulation, determining the merits of waveform and list output is a dubiously wasteful and unadvantageous exercise. Nevertheless, it is this student's stance that the waveform view makes understanding the progression of the combinational circuit easier, while the list output makes immediate instantaneous analysis and debugging faster.