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CPE 322

Simulation Assignment 01

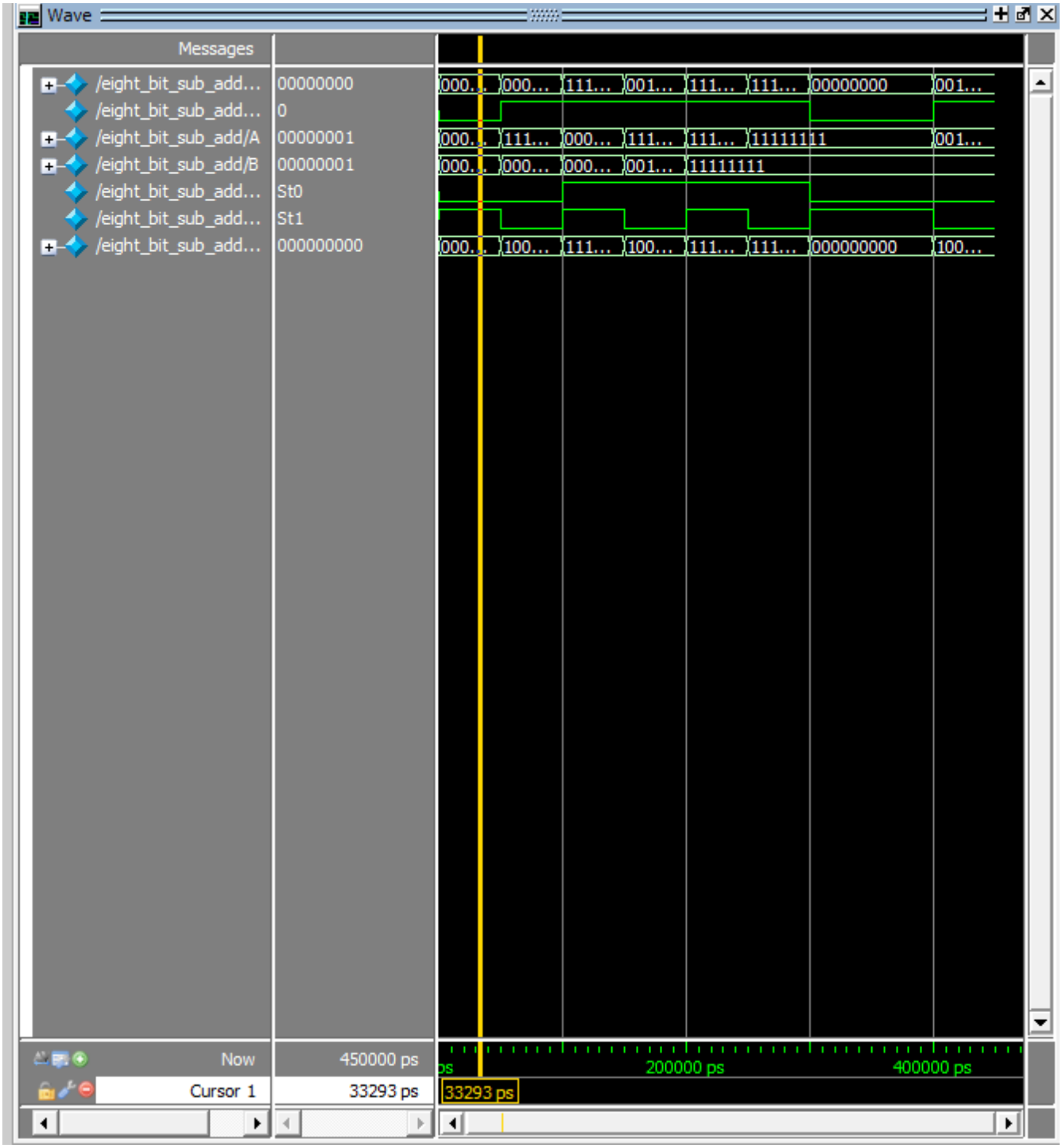
“RTL & Post FPGA Layout Timing Simulation of two an [sic] 8-bit Subtractor/Adder”

Stimulus

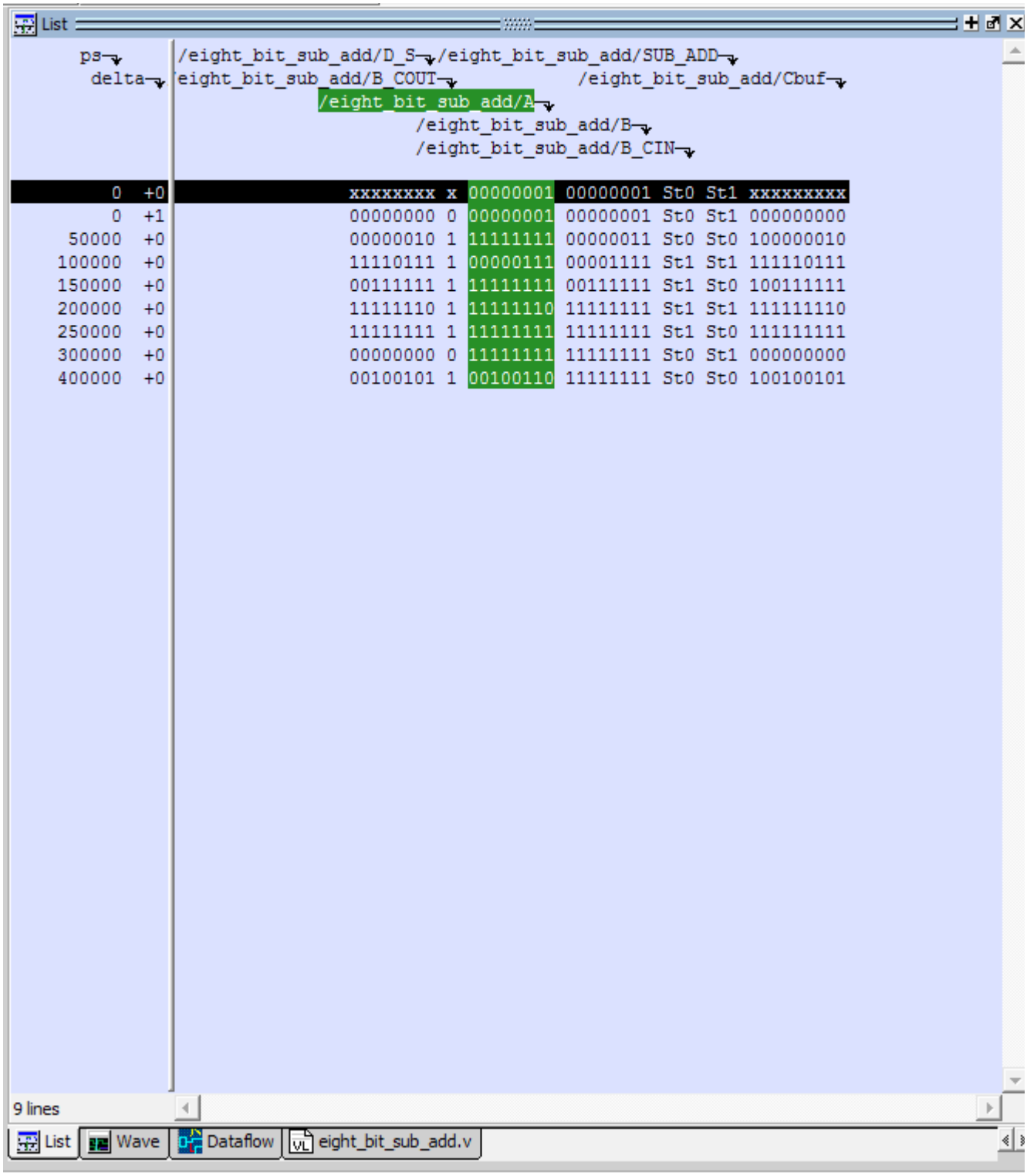
```
#
# Stimulus for Behavioral Model
#

force {sim:/eight_bit_sub_add/B_CIN}     0 0ns, 0 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 0 300ns, 0 400ns

force {sim:/eight_bit_sub_add/A[0]}      1 0ns, 1 50ns, 1 100ns, 1 150ns, 0 200ns,
1 250ns, 1 300ns, 0 400ns
force {sim:/eight_bit_sub_add/A[1]}      0 0ns, 1 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 1 400ns
force {sim:/eight_bit_sub_add/A[2]}      0 0ns, 1 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 1 400ns
force {sim:/eight_bit_sub_add/A[3]}      0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 400ns
force {sim:/eight_bit_sub_add/A[4]}      0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 400ns
force {sim:/eight_bit_sub_add/A[5]}      0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 1 400ns
force {sim:/eight_bit_sub_add/A[6]}      0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 400ns
force {sim:/eight_bit_sub_add/A[7]}      0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 0 400ns

force {sim:/eight_bit_sub_add/B[0]}      1 0ns, 1 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 1 400ns
force {sim:/eight_bit_sub_add/B[1]}      0 0ns, 1 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 1 400ns
force {sim:/eight_bit_sub_add/B[2]}      0 0ns, 0 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 1 400ns
force {sim:/eight_bit_sub_add/B[3]}      0 0ns, 0 50ns, 1 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 1 400ns
force {sim:/eight_bit_sub_add/B[4]}      0 0ns, 0 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 1 400ns
force {sim:/eight_bit_sub_add/B[5]}      0 0ns, 0 50ns, 0 100ns, 1 150ns, 1 200ns,
1 250ns, 1 300ns, 1 400ns
force {sim:/eight_bit_sub_add/B[6]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 400ns
force {sim:/eight_bit_sub_add/B[7]}      0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns,
1 250ns, 1 300ns, 1 400ns

force {sim:/eight_bit_sub_add/SUB_ADD}   1 0ns, 0 50ns, 1 100ns, 0 150ns, 1 200ns,
0 250ns, 1 300ns, 0 400ns

run 450ns
```

```
#
# Stimulus for Structural Model
#

force {sim:/full_adder/B_CIN}      0 0ns, 0 50ns, 1 100ns, 1 150ns, 1 200ns, 1
250ns, 0 300ns, 0 400ns

force {sim:/full_adder/A[0]}  1 0ns, 1 50ns, 1 100ns, 1 150ns, 0 200ns, 1 250ns, 1
300ns, 0 400ns
force {sim:/full_adder/A[1]}  0 0ns, 1 50ns, 1 100ns, 1 150ns, 1 200ns, 1 250ns, 1
300ns, 1 400ns
force {sim:/full_adder/A[2]}  0 0ns, 1 50ns, 1 100ns, 1 150ns, 1 200ns, 1 250ns, 1
300ns, 1 400ns
force {sim:/full_adder/A[3]}  0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns, 1 250ns, 1
300ns, 0 400ns
force {sim:/full_adder/A[4]}  0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns, 1 250ns, 1
300ns, 0 400ns
force {sim:/full_adder/A[5]}  0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns, 1 250ns, 1
300ns, 1 400ns
force {sim:/full_adder/A[6]}  0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns, 1 250ns, 1
300ns, 0 400ns
force {sim:/full_adder/A[7]}  0 0ns, 1 50ns, 0 100ns, 1 150ns, 1 200ns, 1 250ns, 1
300ns, 0 400ns

force {sim:/full_adder/B[0]}  1 0ns, 1 50ns, 1 100ns, 1 150ns, 1 200ns, 1 250ns, 1
300ns, 1 400ns
force {sim:/full_adder/B[1]}  0 0ns, 1 50ns, 1 100ns, 1 150ns, 1 200ns, 1 250ns, 1
300ns, 1 400ns
force {sim:/full_adder/B[2]}  0 0ns, 0 50ns, 1 100ns, 1 150ns, 1 200ns, 1 250ns, 1
300ns, 1 400ns
force {sim:/full_adder/B[3]}  0 0ns, 0 50ns, 1 100ns, 1 150ns, 1 200ns, 1 250ns, 1
300ns, 1 400ns
force {sim:/full_adder/B[4]}  0 0ns, 0 50ns, 0 100ns, 1 150ns, 1 200ns, 1 250ns, 1
300ns, 1 400ns
force {sim:/full_adder/B[5]}  0 0ns, 0 50ns, 0 100ns, 1 150ns, 1 200ns, 1 250ns, 1
300ns, 1 400ns
force {sim:/full_adder/B[6]}  0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns, 1 250ns, 1
300ns, 1 400ns
force {sim:/full_adder/B[7]}  0 0ns, 0 50ns, 0 100ns, 0 150ns, 1 200ns, 1 250ns, 1
300ns, 1 400ns

force {sim:/full_adder/SUB_ADD}     1 0ns, 0 50ns, 1 100ns, 0 150ns, 1 200ns, 0
250ns, 1 300ns, 0 400ns

run 450ns
```

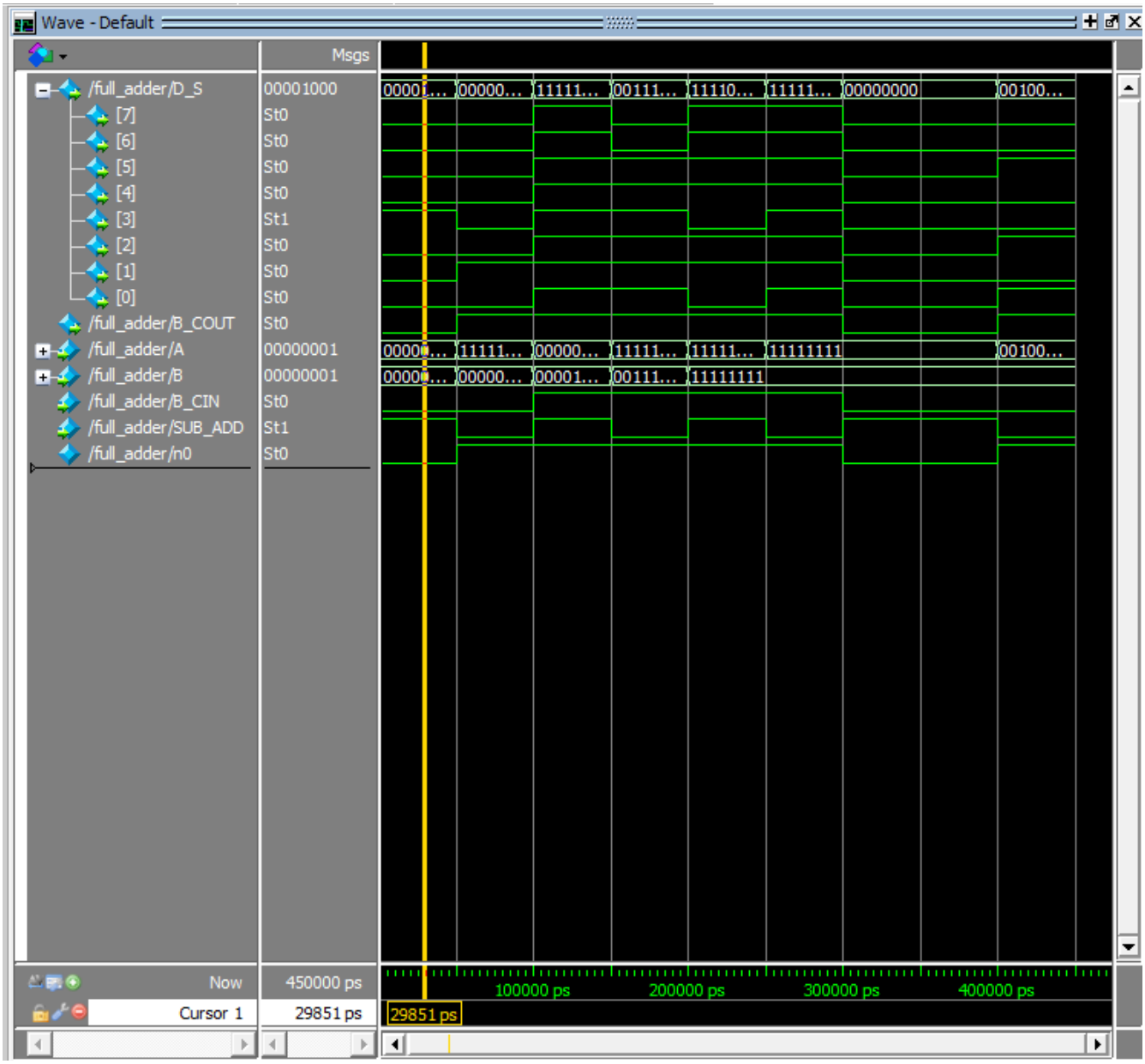
Waveform – Behavioral



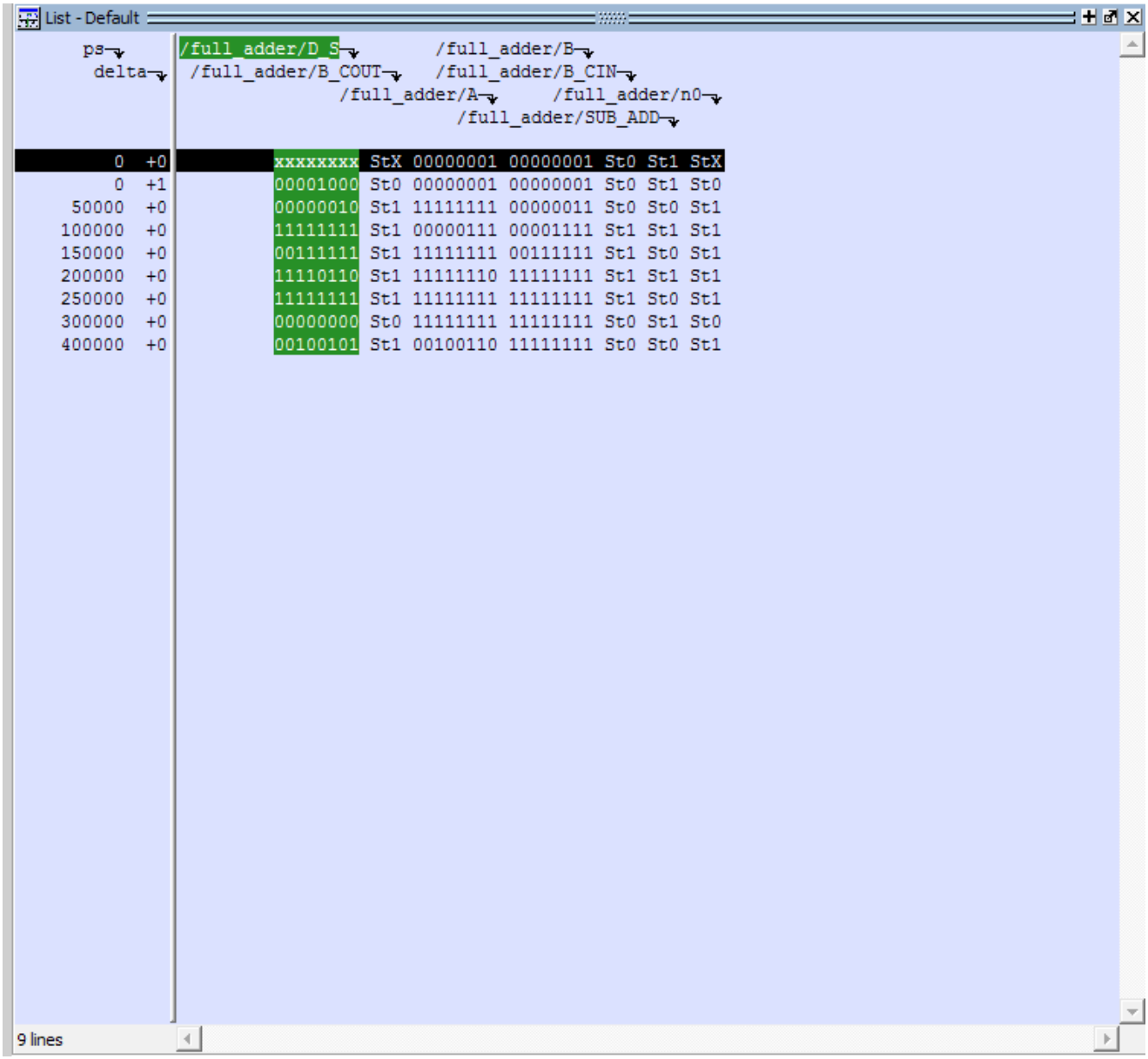
List – Behavioral



Waveform – Structural



List – Structural



Discussion

Only one large glitch was observed for RTL post-layout simulation: the simulation would not start. For the same reason no significant differences were noticed between the two simulation models. In RTL simulation, no significant glitches were detected which could not otherwise be described as a lack of experience with the software or intended but undocumented behavior. Since we have not implemented any activity based on the output of the simulation, determining the merits of waveform and list output is a dubiously wasteful and unadvantageous exercise. Nevertheless, it is this student's stance that the waveform view makes understanding the progression of the combinational circuit easier, while the list output makes immediate instantaneous analysis and debugging faster.