CPE 322 **EXAM II**
Spring Semester 2015

INSTRUCTIONS: **Work in a clear and detailed manner on separate paper all parts of the 4 problems given on this exam. You may use any resources available including class notes, textbooks, internet and research articles but you are not to employ any outside help from any individual. This should be your own work. Students who violate this rule will be considered to be guilty of academic misconduct as defined in the UAH Student Handbook. Exam due date: Tuesday April 28, 2015 at 8:00 AM. Hardcopy turned in directly to instructor.**

1. (a) Write a Verilog **task** that counts the number of 1s in an input bit vector that is up to N bits long (N<31). The output should be 5 bits long. The **task** call should have the following form: (N,A,B) where A is the input and B is the output and is N as a global parameter in the calling module.(b) Write a Verilog module that will call the task in part (a).

2. Design a simple 4-bit ripple adder using discrete AND/OR and NOT gates. If it is assumed that each of these gates have a maximum delay of 5 ns what will be the worst case delay of your 4bit ripple adder? What would be the maximum delay associated with a similarly constructed 16 bit ripple adder? In general derive an expression for maximum delay for an n-bit ripple adder.

3. a) Use Shannon's expansion theorem to expand the following function around A and expand each sub-function around D:

$$Z = AB'CD'E'F + A'BC'D'EF'+B'C'E'F+A'BC'E'F'+ABCDE.$$

Show how this same function could be implemented using two Xilinx Kintex Configurable Logic Blocks called slices that are shown in figure 6-13 on page 355 of the text. On the diagram of each slice, label the inputs to the LUTs and draw the connection paths within the slice. Also give the logic equations implemented by each LUT.

4. Create an equivalent Algorithmic State Machine (SM) Chart to the finite state machine that is represented by the state graph for the scoreboard that is shown in Figure 4-20 on page 227.