Lab 10 Report
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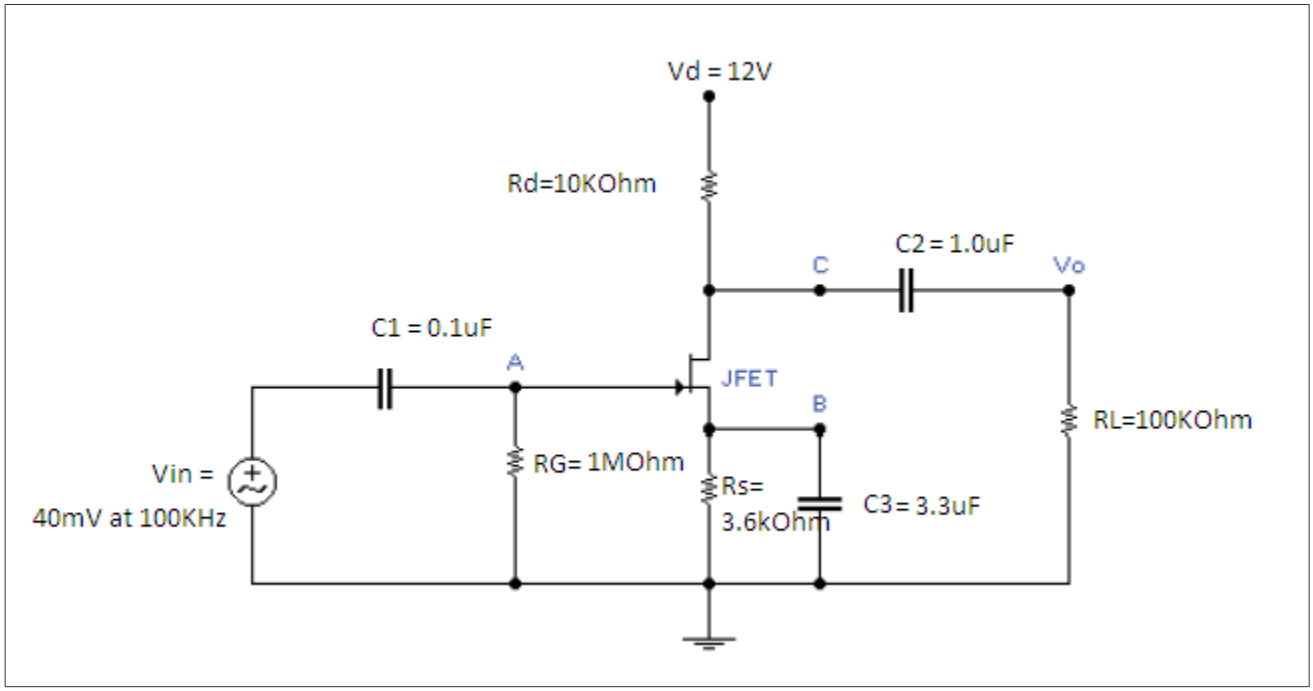
EE 316

Amplification of a Signal Using JFETs

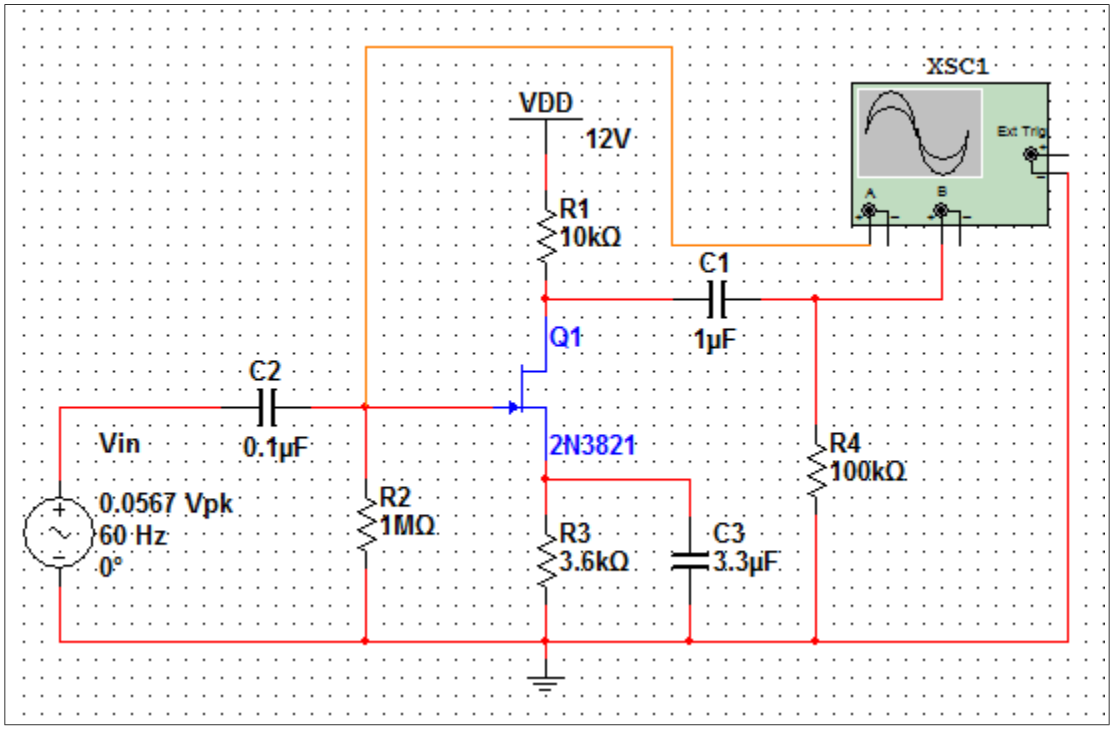
Simulation

The simulation portion of this assignment had us model a circuit from the following layout and test its output voltage against a variety of input frequencies. This shows us how the JFET will respond to a given bandwidth, or range of frequencies.

Circuit Model

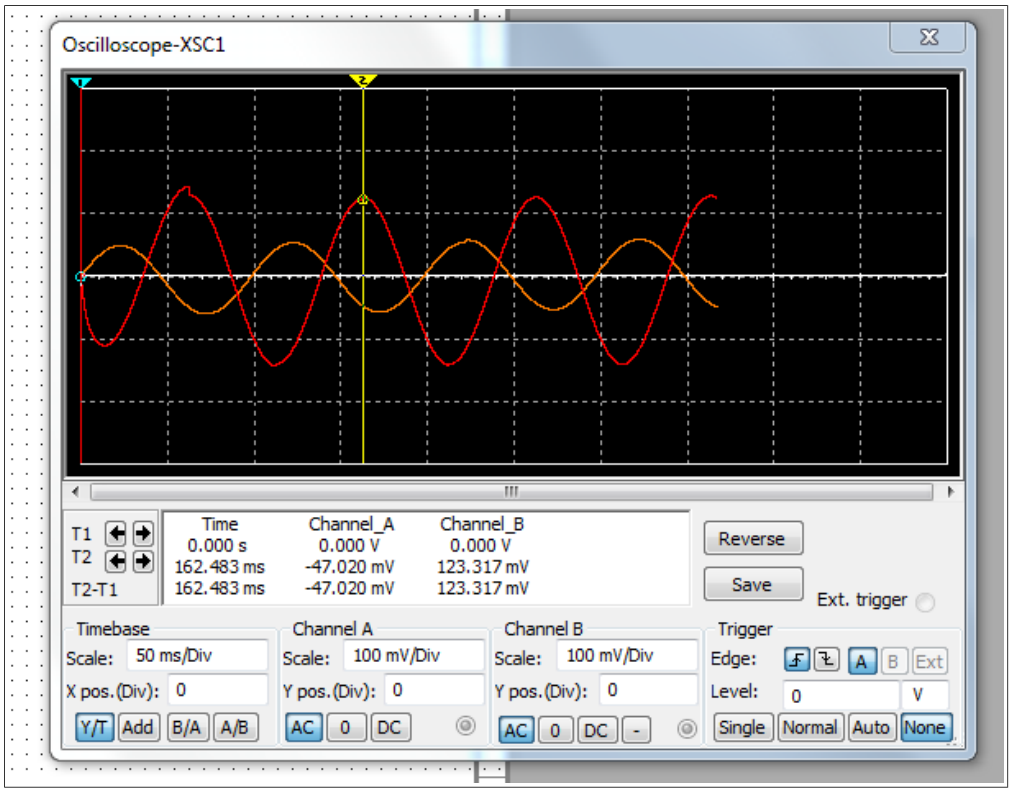


Simulation Circuit

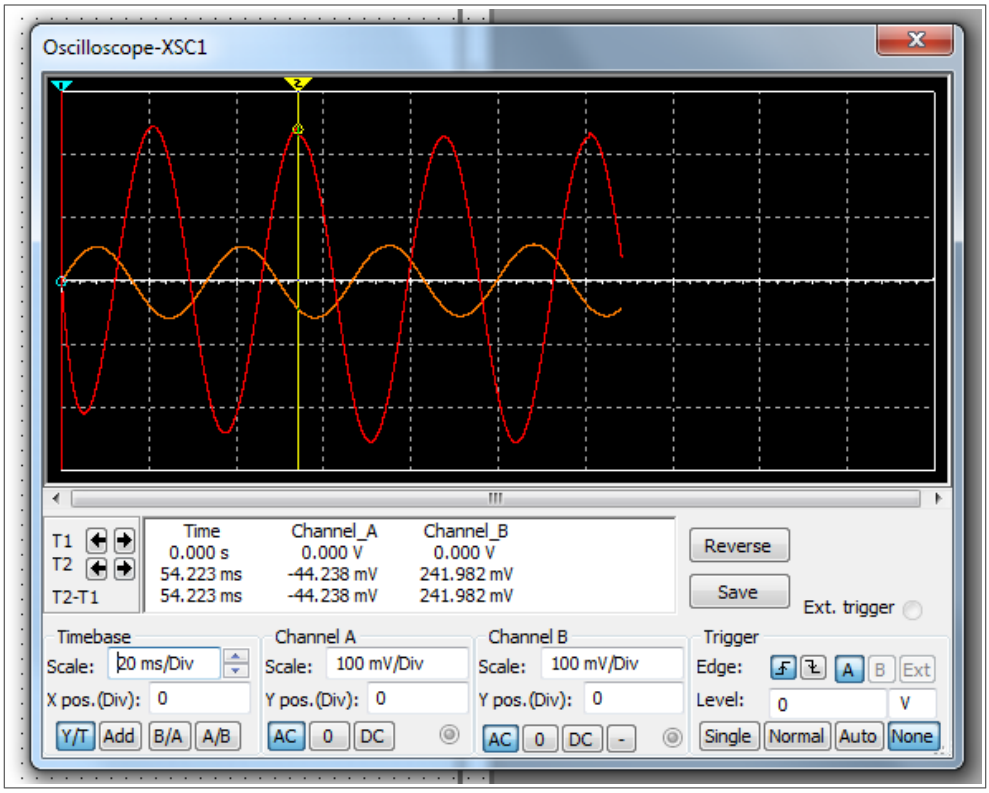


Circuit Responses

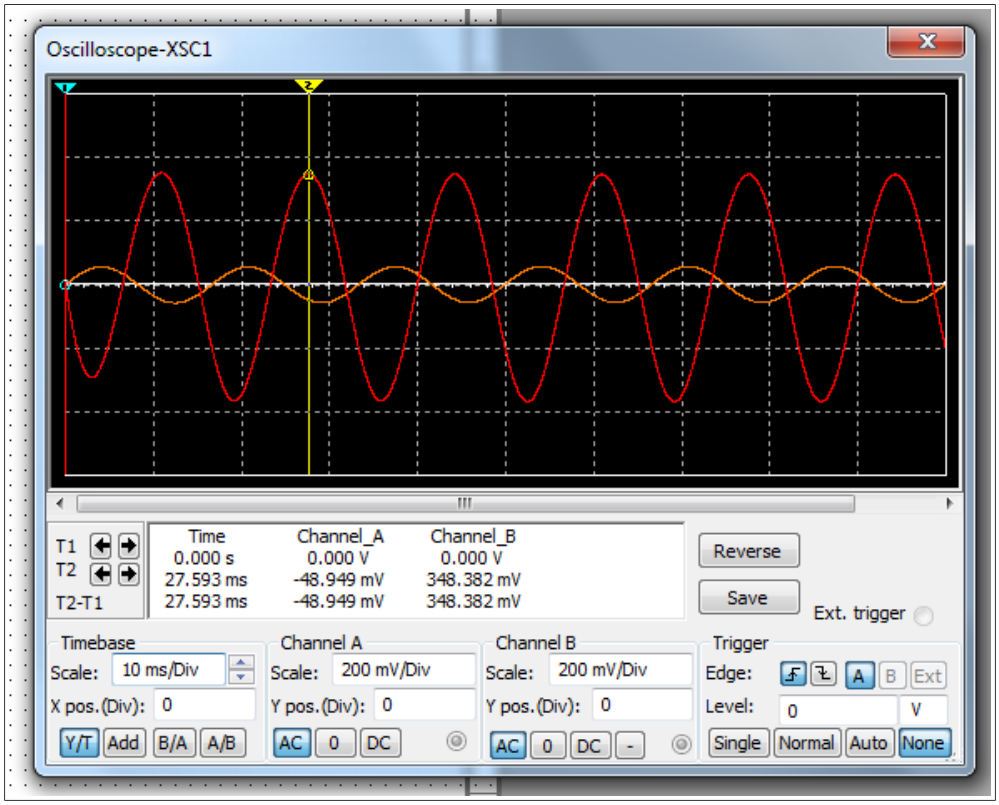
10Hz



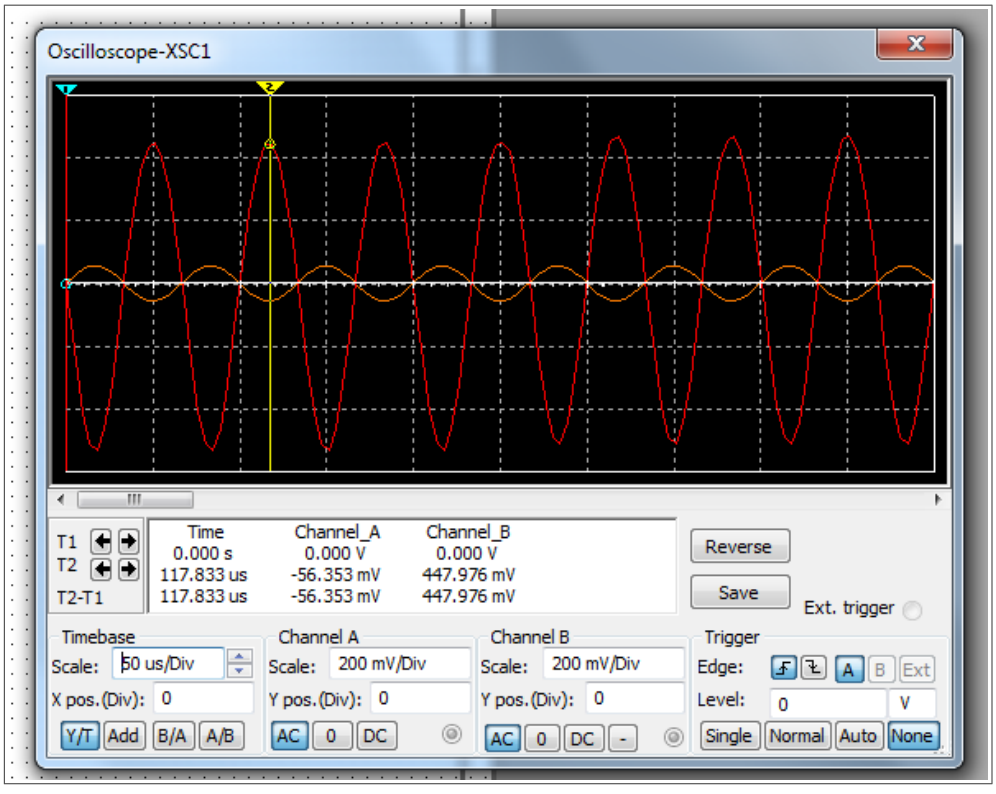
30Hz



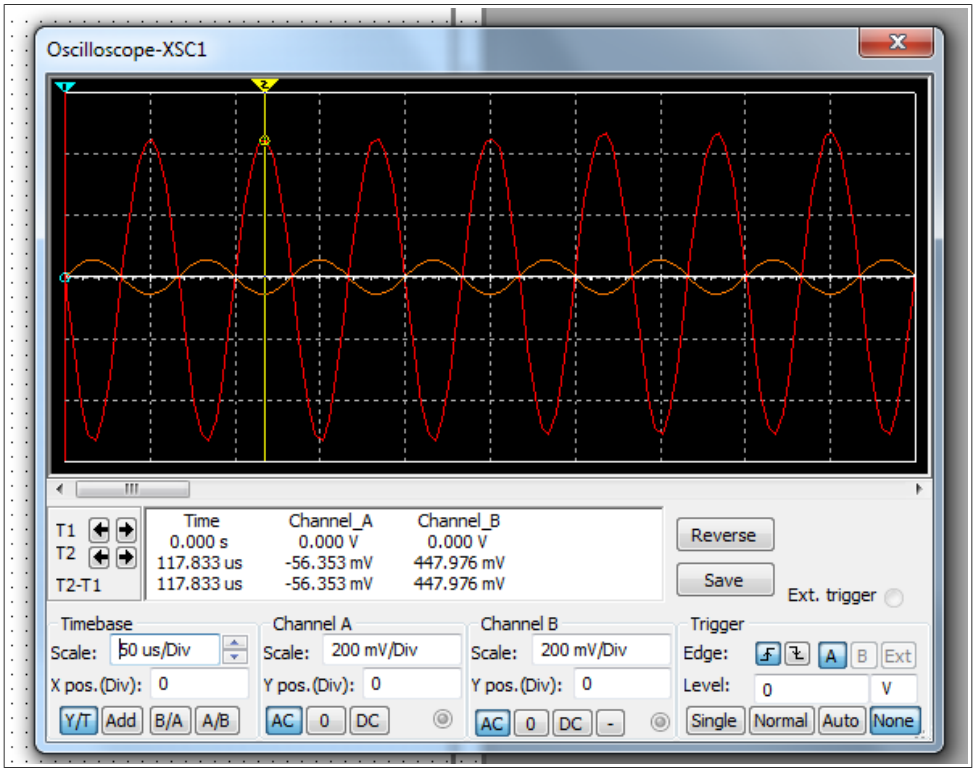
60Hz


Oscilloscope-XSC1
T1
T2
T2-T1
Time
0.000 s
27.593 ms
27.593 ms
Channel_A
0.000 V
-48.949 mV
-48.949 mV
Channel_B
0.000 V
348.382 mV
348.382 mV
Reverse
Save
Ext. trigger
Timebase
Scale: 10 ms/Div
X pos.(Div): 0
Y/T Add B/A A/B
Channel A
Scale: 200 mV/Div
Y pos.(Div): 0
AC 0 DC
Channel B
Scale: 200 mV/Div
Y pos.(Div): 0
AC 0 DC -
Trigger
Edge: A B Ext
Level: 0 V
Single Normal Auto None

1.5KHz


Oscilloscope-XSC1
T1
T2
T2-T1
Time
0.000 s
117.833 us
117.833 us
Channel_A
0.000 V
-56.353 mV
-56.353 mV
Channel_B
0.000 V
447.976 mV
447.976 mV
Reverse
Save
Ext. trigger
Timebase
Scale: 50 us/Div
X pos.(Div): 0
Y/T Add B/A A/B
Channel A
Scale: 200 mV/Div
Y pos.(Div): 0
AC 0 DC
Channel B
Scale: 200 mV/Div
Y pos.(Div): 0
AC 0 DC -
Trigger
Edge: A B Ext
Level: 0 V
Single Normal Auto None

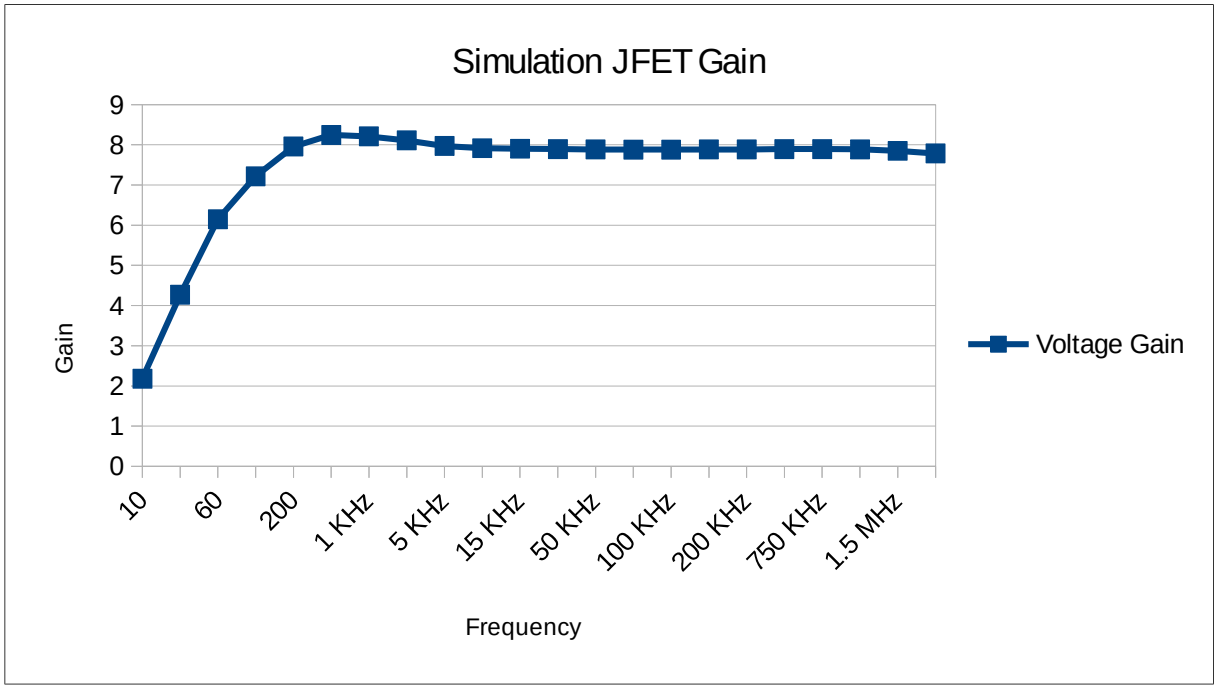
15KHz


Oscilloscope-XSC1
T1
T2
T2-T1
Time
0.000 s
117.833 us
117.833 us
Channel_A
0.000 V
-56.353 mV
-56.353 mV
Channel_B
0.000 V
447.976 mV
447.976 mV
Reverse
Save
Ext. trigger
Timebase
Scale: 50 us/Div
X pos.(Div): 0
Y/T Add B/A A/B
Channel A
Scale: 200 mV/Div
Y pos.(Div): 0
AC 0 DC
Channel B
Scale: 200 mV/Div
Y pos.(Div): 0
AC 0 DC -
Trigger
Edge:
A B Ext
Level: 0 V
Single Normal Auto None

Simulation Results

Frequency	Vout (Vpk)	Voltage Gain
10	0.123317	2.18
30	0.241982	4.27
60	0.348382	6.14
100	0.409094	7.22
200	0.451050	7.96
500	0.467524	8.25
1 KHz	0.465341	8.21
2 kHz	0.459702	8.11
5 KHz	0.451954	7.97
10 KHz	0.448771	7.91
15 KHz	0.447976	7.9
20 KHz	0.447574	7.89
50 KHz	0.446900	7.88
75 KHz	0.446820	7.88
100 KHz	0.446822	7.88
150 KHz	0.446905	7.88
200 KHz	0.447018	7.88
500 KHz	0.447529	7.89
750 KHz	0.447528	7.89
1 MHz	0.447117	7.89
1.5 MHz	0.445025	7.85
2.0 MHz	0.441252	7.78

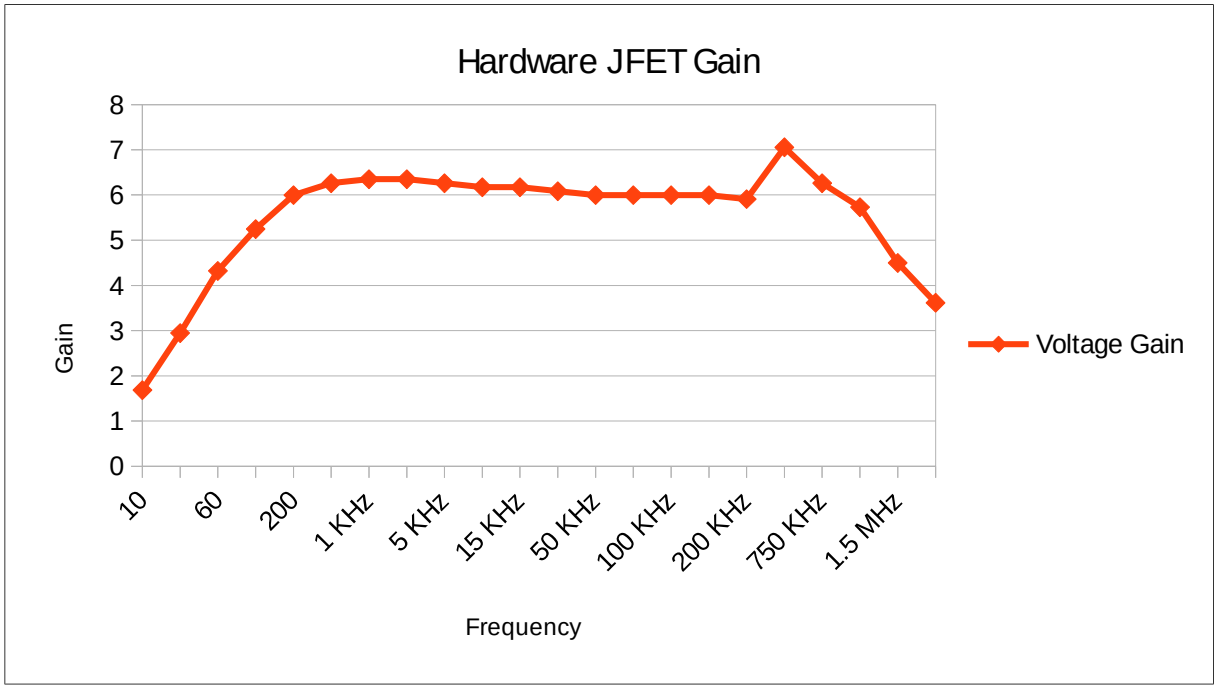
Simulation Results



Hardware Results

Frequency	Vout (Vpk-pk)	Voltage Gain
10	0.191	1.68
30	0.334	2.95
60	0.490	4.32
100	0.595	5.25
200	0.680	6
500	0.710	6.26
1 KHz	0.720	6.35
2 kHz	0.720	6.35
5 KHz	0.710	6.26
10 KHz	0.700	6.17
15 KHz	0.700	6.17
20 KHz	0.690	6.08
50 KHz	0.680	6
75 KHz	0.680	6
100 KHz	0.680	6
150 KHz	0.680	6
200 KHz	0.670	5.91
500 KHz	0.800	7.05
750 KHz	0.710	6.26
1 MHz	0.650	5.73
1.5 MHz	0.510	4.5
2.0 MHz	0.410	3.62

Hardware Results



Conclusion

The JFET circuit used has a very clean gain mapping, where a large area of the frequency spectrum is plateaued. The gain graphs between simulation and hardware circuits were surprisingly agreeable, each showing the same characteristics that we expect. Compared to the MOSFET used in an earlier lab, the JFET has a much larger bandwidth and more leveled gain rather than the ramp plot we see from Lab 08.