CPE 322 Final Exam Study Guide
Spring Semester 2015

Exam Date

Tuesday 8:00 -- 10:30 AM, April 28, 2015, Room 134 Engineering Building

Optional Study Sessions -- 5:30--7:00 PM EB 258

- Friday 4/24/2015
- Monday 4/28/2015

Test Format

The examination will be an in-class closed-book examination. No electronic devices will be permitted. There will be no need for a calculator for this examination.
The following type of questions are possible:

- Short Answer -- concept question that the student provides a concise answer.
- Analysis -- student is supplied a logic diagram, timing diagram or a Verilog HDL model and asked to evaluate its functionality or determine its logical output.
- Model/Design -- student is asked to create an implementation that meets the specification expressed by the problem.

Available Study Resources

- Textbook: See specific page and chapter listings in the table.
- Lecture Notes: your personal lecture notes as well as the powerpoint and recorded presentations present on the course Canvas site.
- Old Examinations: The solutions to eight old examinations dating back to 2008 are presented on the Canvas site. CPE 322 use to be taught at the senior/graduate level but was made a junior level course in 2013.
  Warning: We are using a different textbook than in the past. This is the second year we have incorporated Verilog in the instruction. Also the class progresses at different rates during different semesters.
  With that said, the past Exam 1 and Exam 2 questions from past years should be a good indication of the type of questions that will be presented on this examination. Expect different but similar types of questions.

Topical Outline:

Topics	Textbook, Manuals and Lecture References
Background Topics: Number Representations (BCD, two's complement, etc.)	Review EE 100 or EE 202 Material
Design Methodology: Understanding of each component of Figure 2-1 of the text. Basic understanding of the use of Quartus II and ModelSim. Differences between Simulation and Synthesis. Roles of HDLs in general.	Text pp. 58-61 Simulations 1 & 2
Review of Combinational Logic Design: Simple Gates, Boolean Algebra, Boolean Algebra Simplification, Karnaugh Maps Building Blocks for Logic Design -- NAND-NOR Structures, Multiplexers, Demultiplexers, Encoders, Decoders, Hazard Analysis. PLA's and PALs.	Text pp. 15-30, 161-176. Powerpoint/Video -- "Hazard Detection and Prevention" Homework 1, Homework 2 "Simulating a Verilog HDL Design using the ModelSim® Compiler and Simulator in Stand-Alone Mode" manual
Fundamentals of Sequential Logic Design: Latches (SR and D), Flip-Flops (D, T, and JK, Master/Slave Construction), Busses and Tri-state devices, Design of Sequential Mealy and Moore Finite State Machines (State-Transition Graph construction). State Reduction Techniques, Basic concepts of synchronous design, mechanical switch bounce and debounce methods in hardware.	Text: pp. 103--130, 230-232. Powerpoint/Video -- "Finite State Machines & Verilog" Powerpoint/Video -- "General State Reduction Techniques in Sequential Logic" Powerpoint:/Video -- "Extended State Graph Representation"
Introduction to Verilog. Structural, Dataflow, and Behavioral Implementations of Combinational and basic Sequential logic elements including FSMs. Major things to remember include number format and data types (wire and reg), basic module -- endmodule syntax, structural modeling methods including instantiation of built-in primitives and user created components, continuous assignment statements. Procedural constructs ***initial*** and ***always***. The cyclic operator **@** and how to model edge and level triggered devices using procedural statements. Blocking and non-blocking *procedural* assignment statements. ***if*** and ***case*** procedural statements. Built-in Primitives [Not to be included for this examination are the ***while***, ***for***, ***repeat***, ***task***, ***function***, **casex** and ***casez wait*** and ***fork*** statements]	Text: pp. 62--135 Power point/Video --"Introduction to Verilog Part I" Power point/Video --"Introduction to Verilog Part II" Section 8.4 pp 439-442. Powerpoint -- "Finite State Machines & Verilog"
Verilog Delay Assignment and Static Timing Simulation Proper use of the delay # operator. Inertial Delay assignment using primitives and *continuous assignment* statements. Transport Delay modeling using *procedural non-blocking assignment* statements.	pp 84-87 Powerpoint "Performing Simple Static Timing Analysis in Verilog HDL"

Topical Outline (continued):

Topics	Textbook, Manuals and Lecture References
Sequential Circuit Timing: FF Propagation Delays, Setup and Hold Time Considerations, timing conditions for proper operation, maximum clock frequency, clock skew, synchronous design with clock skew, clock gating issues and rules, etc.	Section 1.10, pp. 30-47. Homework 3 Power point presentation "Timing Considerations in Synchronous Sequential Designs"
Overview of Complex Programmable Logic Devices (CPLDs) and Field Programmable Gate Arrays: Architectural Considerations, device technology considerations. Programmable Logic Blocks, Programmable I/O, Dedicated and Specialized Components (Dedicated Memory, Dedicated Arithmetic Units, DSP Blocks, etc.) Design flow for FPGAs	Sections3.3 & 3.4, pp.176-205
Algorithmic State Machine Charts, ASM: Use of principal components (state box, decision box, conditional output box), equivalence with modified state graph representation, use to represent Moore, Meally, and hybrid Finite State Machines.	Sections 5.1, 5.3, Text pp. 288-309.
Designing with FPGAs: Understanding of how simple logic configurations can be manually be mapped, placed, and routing within an FPGA. Implementing combinational functions using Shannon's Decomposition. Logic block implementation within FPGAs, Dedicated Memory within FPGAs (synchronous versus asynchronous memory implementation using Verilog. Cost of reconfigurability issues in FPGAs. Basic understanding of what common circuit elements will be synthesized by basic Verilog Modeling code. Basic understanding of the typical FPGA design flow (Design Entry, Optimization, Mapping, Placement, & Routing).	Chapter 6 (all sections) pp. 341--389. Power point presentation "Designing with FPGAs Architectural Issues and Features"
Intermediate Verilog Verilog Constants, and Arrays (1 and 2 dimensional), Loops in Verilog (while, for loops). Verilog Functions and Tasks. SRAM Model & Modeling SRAM Read/Write System	Text: Section 2.16, 2.17, and 2.18 pp. 124-133 Section 8.1 & 8.2 pp 431-437 , 8.7 Sections 8.6, pp. 445-452 Power point presentation "Introduction to Verilog II"
Hardware Testing and Design for Testability: Testing Combinational Logic using the stuck at fault model. Test pattern generation to excite and detect specific faults and evaluation of the specific stuck-at faults detected by a specified test vector.	Chapter 10. Section 10.1, pp. 514-518. Power point presentation "