CPE/EE 422/522 **EXAM I** **Name** KEY

Class _____

Spring Semester 2010

Work should be performed systematically and neatly with the final answer being underlined. This exam is closed book, closed notes, closed neighbor. Allowable items on desk include: exam, pencils, straight edge, and calculator. All other items (including cell phones and other personal telecommunication or electronic entertainment/ imaging devices), must be removed from each student's desk and not accessed during the test without the instructors permission. Students have approximately 90 minutes (1 1/2 hours) to complete this exam. Best wishes!

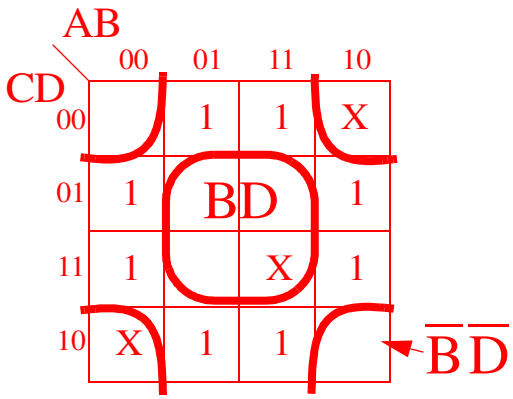
1. [5 points] Write a short VHDL description for a D latch using a single VHDL *process*.

```
library IEEE; -- allows the use of STD_LOGIC and STD_LOGIC Vectors
entity DLATCH is
   port (D, G: in STD_LOGIC;
         Q: out STD_LOGIC);
end DLATCH;

architecture DLATCH_ARCH of DLATCH is
begin

   process(D, G)
      begin
         if G = '1' then
            Q = D;
         end if;
   end process;

end DLATCH_ARCH;
```

← Enter your VHDL Model

2. [5 points] Obtain all minimum <u>product-of-sums</u> two-level logic expressions for the following function:

$$F(A, B, C, D) = \sum m(1, 3, 4, 6, 9, 11, 12, 14) + \sum d(2, 8, 15)$$

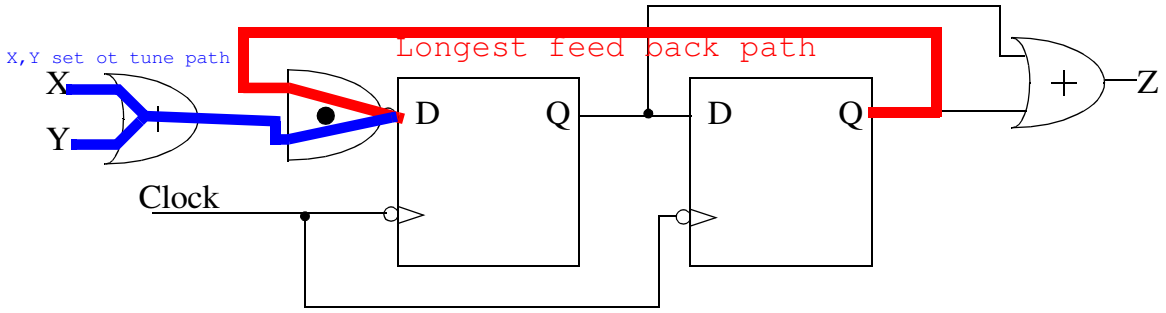


$$\overline{F} = BD + \overline{B}\,\overline{D}$$

$$F = (\overline{B} + \overline{D})(B + D)$$

(pos form)

3. [15 points total] A sequential network is implemented using two **OR** gates one **NAND** gate and two **D flip-flops** as shown below. Assume that the inputs ***X*** and ***Y*** always changes at the same time as the rising edge of the 50% duty cycle clock. Also assume the following delay parameters: **OR** gates delay ranges from 1 to 3 ns; **NAND** gate delay ranges from 2 to 5 ns; **flip-flops** propagation delay ranges from 2 to 6 ns, flip-flop setup time requirement is 4 ns, flip-flop hold time requirement is 1 ns.



a) What general type of network is this? [2 points]

Moore -- the output depends only on the current state (output of FFs).

b) Determine the maximum clock rate for proper synchronous operation. Show all steps [13 points].

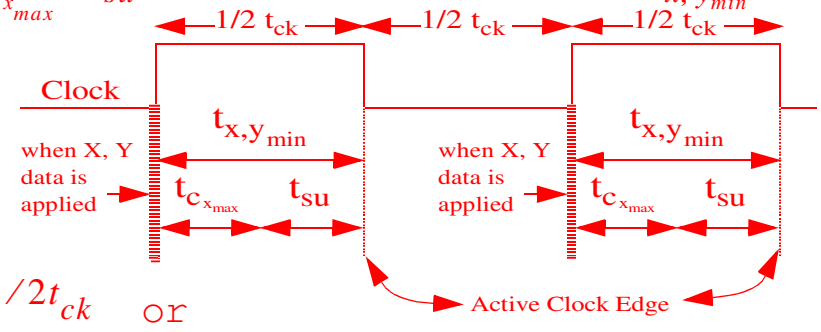
Case 1: Without considering the effect of when Inputs X & Y are applied

$$t_{ck} \geq t_{c_{max}} + t_{p_{max}} + t_{su} = 5\text{ns} + 6\text{ns} + 4\text{ns} = 15\text{ns} = t_{ck_{min}}$$

Case 2: Considering the fact that inputs X & Y are applied on on the edge of the clock that preceeds the edge that the flip flops acquire their data.

$$t_{x,y} \geq t_{C_{x_{max}}} + t_{su} = (3\text{ns} + 5\text{ns}) + 4\text{ns} = 12\text{ns} = t_{x,y_{min}}$$

required set up time for input x & y



$$t_{x,y_{min}} = 1/2t_{ck} \quad \text{or}$$

$$t_{ck_{min}} = 2t_{x,y_{min}} = 2(12\text{ns}) = \underline{24\text{ns}} \leftarrow \text{(Worst Case time)}$$

$$f_{max} = 1/t_{ck_{min}} = 1/24\text{ns} \approx 41.7\text{Mhz}$$

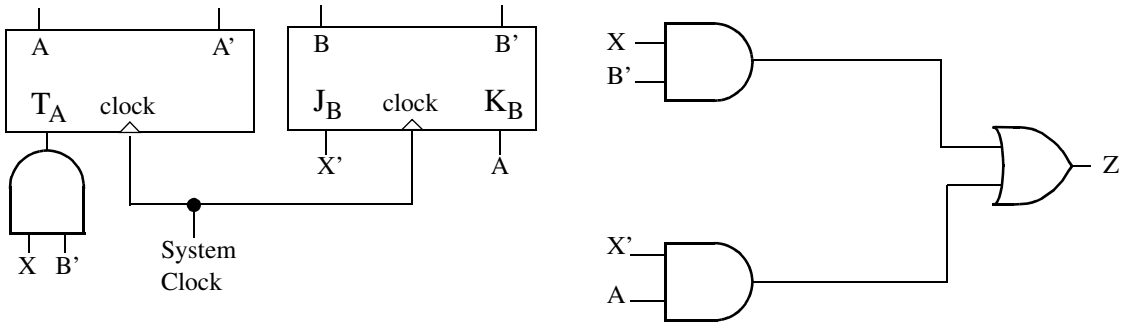
4. [12 points] For the subtractor/adder design you implemented in Laboratory 1, answer the following:

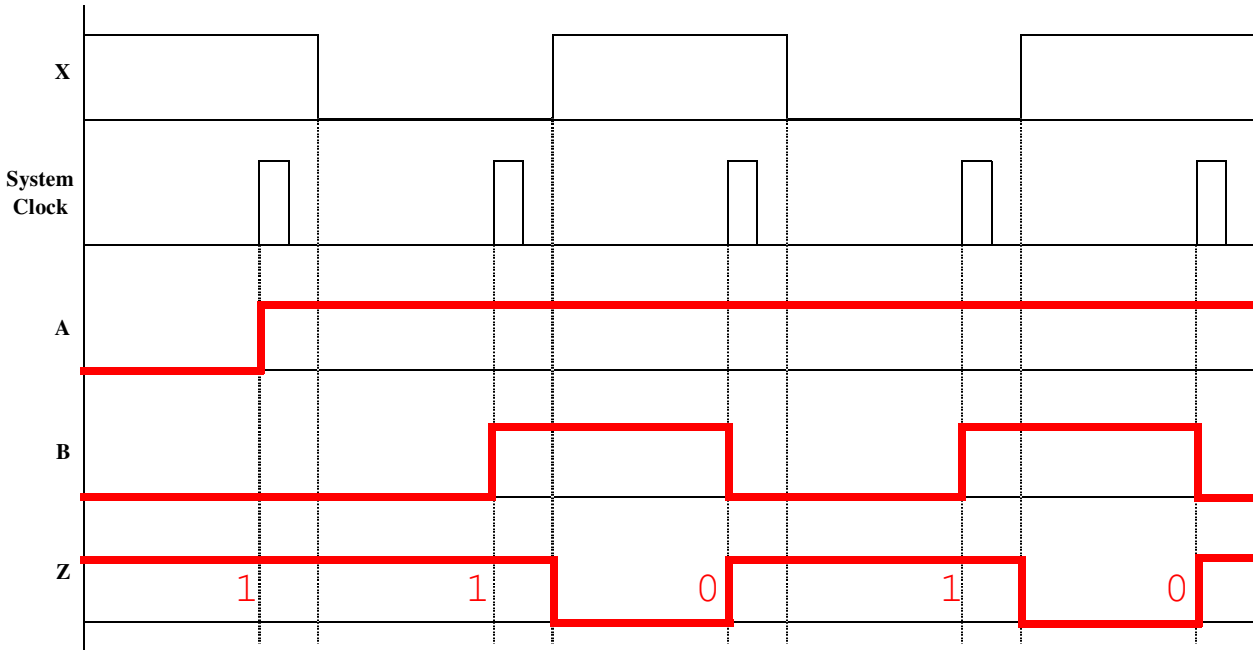
a) How does hierarchical schematic capture and hierarchical structural VHDL design techniques help one manage the complexity of the design process?

b) In general terms, describe the design trade-offs associated with the structural and behavioral versions of your design in terms of ease of design entry, ability to control the low level attributes of the design, and the amount of FPGA resources that were utilized.

c) In general terms, what were the major differences between the Quartus II and ModelSim simulations of the structural version of your Subtractor/Adder VHDL design? Why were these differences present? [Specifically address the effect of the after 10 ns clause within the OR3x and XOR3x components?]

5. [10 points] Complete the following timing diagram for signals A, B, and Z for the network shown below assuming that all setup and hold times for the flip-flops have been met and all propagation delays through the gates and flip-flops are negligible (i.e. zero). Also assume that the two flip-flops are clocked on the rising edge of the system clock and are in the reset state (i.e. A='0' and B='0') at the beginning of the timing diagram.





What type of sequential network is this?

Mealy, -- output value depends on both the state and the input

Write down the output sequence for Z.

11010

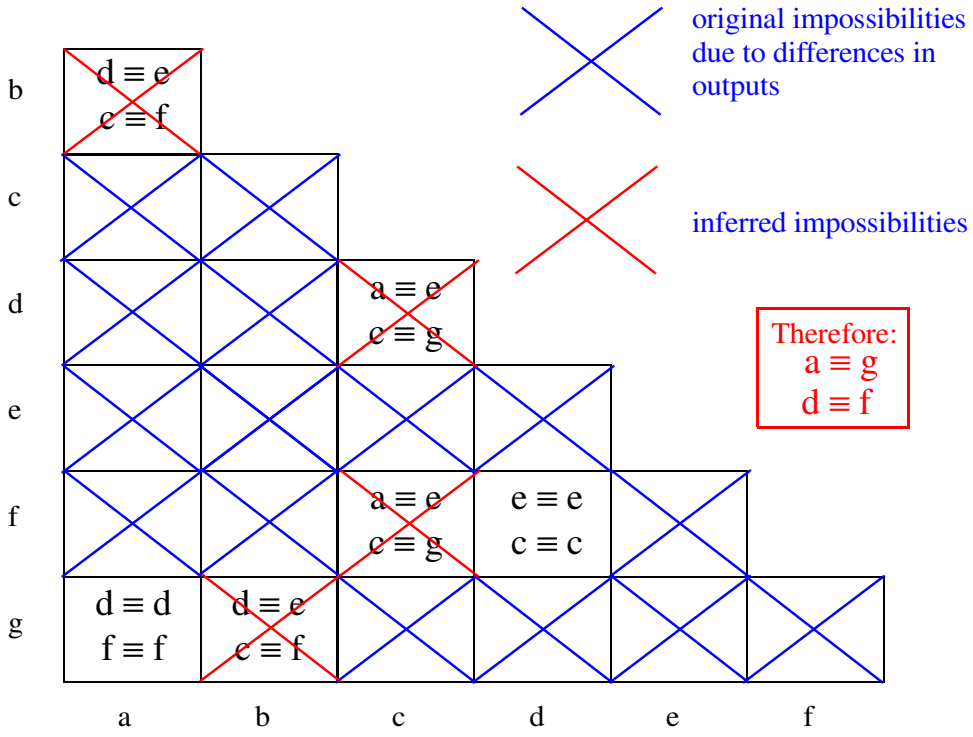
Are there any 'false' outputs on the timing diagram? If so clearly identify them.

In general Mealy networks can have false outputs but none are present for this input pattern.

6. [10 points] Reduce the following state table to a minimum

number of states

present state	next state X=0	1	present output X=0	1
a	d	f	1	0
b	e	c	1	0
c	a	g	0	1
d	e	c	0	1
e	a	g	1	1
f	e	c	0	1
g	d	f	1	0

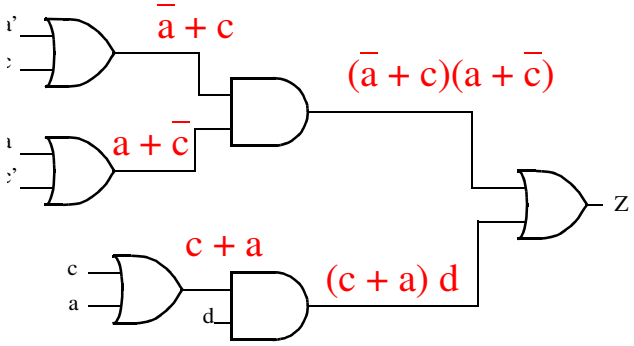


present state	next state X=0	1	present output X=0	1
a	d	d	1	0
b	e	c	1	0
c	a	a	0	1
d	e	c	0	1
e	a	a	1	1

7. [10 points] In general, what are static hazards in a combinational network?

A hazard is an unwanted switching transient that appear on the output of a combinational network. These transients are caused by different delay paths from input to the outputs. Static hazards the output momentarily goes to the incorrect value when an input changes when it should remain constant.

For the network shown below, using the k-map methods outline in the class, find all static 0-hazards (or state that there are no static 0-hazards present). For any 0-hazard found specify the conditions which will cause the hazard to appear at the output (i.e. specify the logic values of the variables which are constant and the variable which is changing).



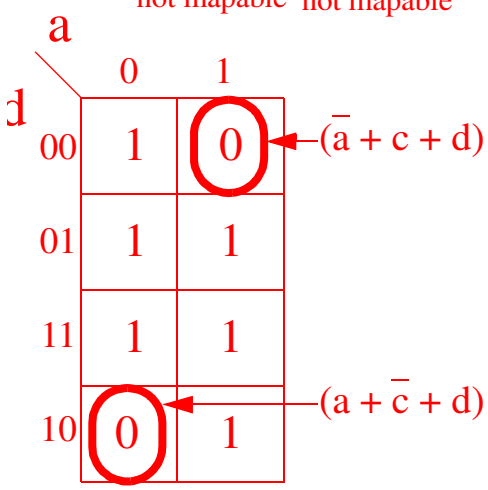
$Z = (\bar{a} + c)(a + \bar{c}) + (c + a)\, d$

$Z = [(\bar{a} + c)\,(a + \bar{c}) + (c + a)][(\bar{a} + c)\,(a + \bar{c}) + d]$ Law 8d

$Z = [\{(\bar{a} + c) + (c + a)\}\{(a + \bar{c}) + (c + a)\}][\{(\bar{a} + c) + d\}\{(a + \bar{c}) + d\}]$ Law 8

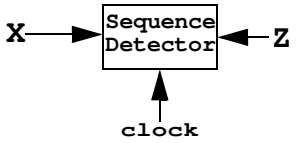
$Z = (\bar{a} + a + c)(a + c + \bar{c})(\bar{a} + c + d)(a + \bar{c} + d)$ Laws 3 & 6

not mapable not mapable



no 0-hazards present!

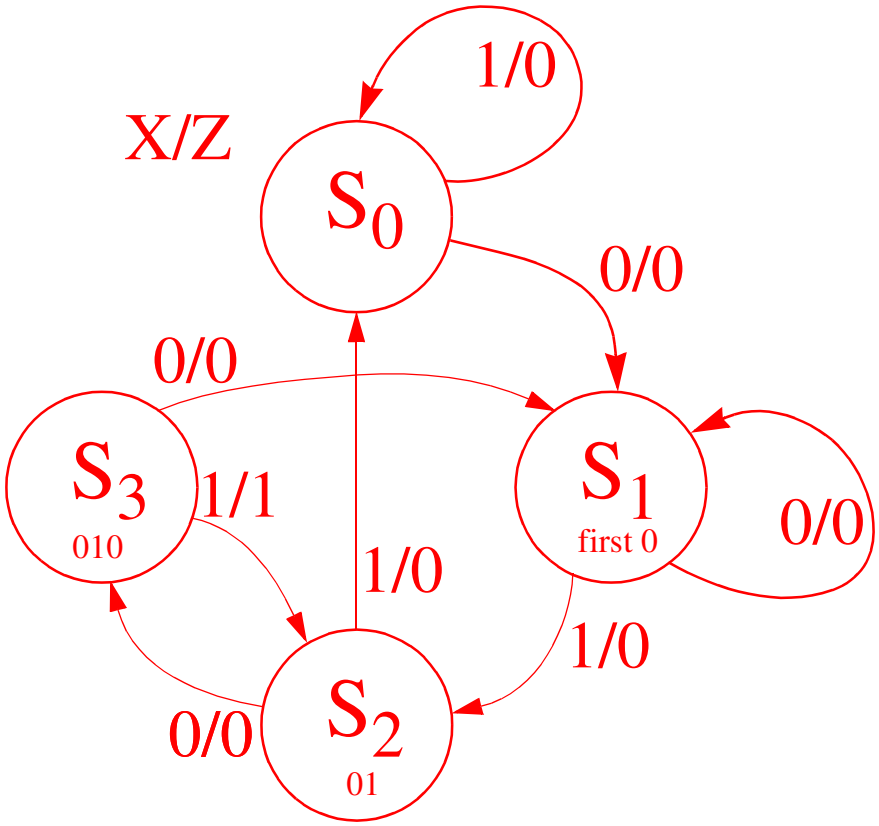
8. [10 points total] Design the state graph of a clocked Mealy sequential network implementation of a sequence detector. The network is to examine a string of 0's and 1's that is supplied on its X input and generate an output Z=1 only when a prescribed input sequence occurs (in all other cases an output of Z=0 should be generated). Specifically the network is to be implemented so that any input sequence ending in 0101 will produce an output Z=1 coincident (at the same time) with the last 1 in the sequence. The network does not reset with a 1 occurs at the output. The network has the form shown below and a typical input sequence and the corresponding output sequence are also shown below.



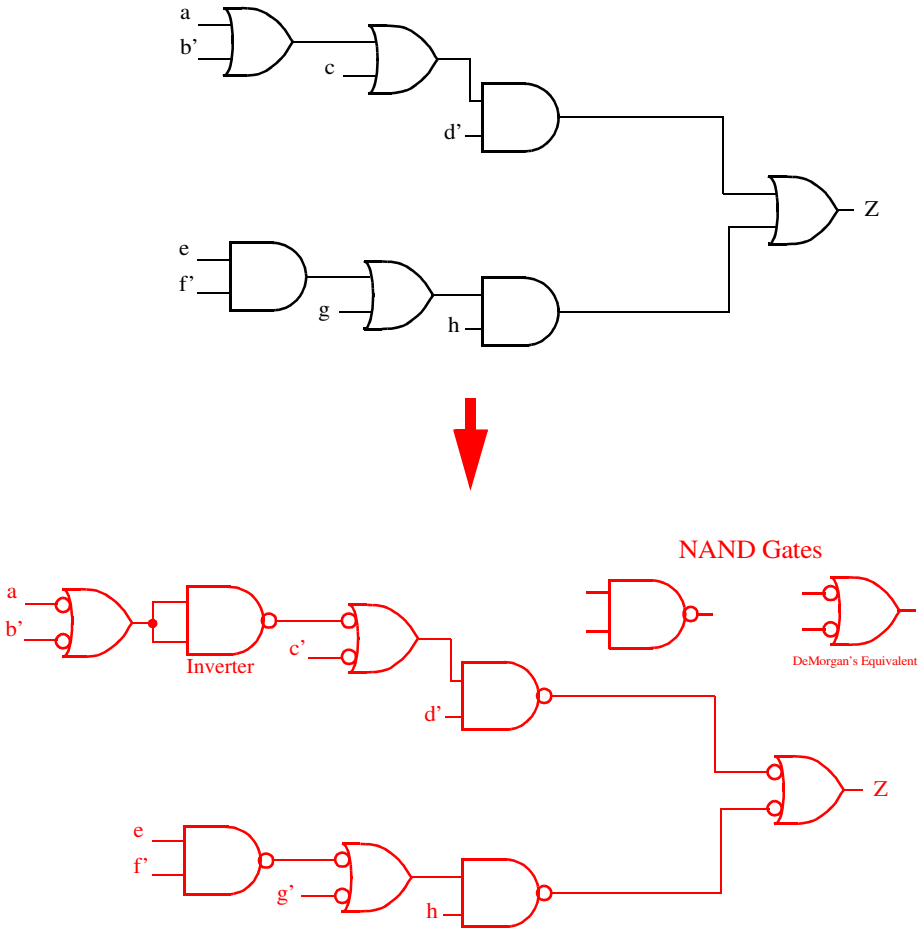
X = 0 0 1 0 1 0 1 0 0 1 0 1 0 1 0 0
Z = 0 0 0 0 1 0 1 0 0 0 0 1 0 1 0 0

You are to design the state graph for a Mealy sequential network that will implement this design. Use the arc and node labeling convention discussed in the class and label your states S_0, S_1, etc. with S_0 being your beginning state. You are only

required to implement the state graph.



9. [8 points] Draw an equivalent multi-level network that is composed entirely of multiple two-input **NAND** gates. Assume that all input variables (a through h) are available in their true and complemented form.



10. [15 points] In the following VHDL process A, B, C, D, and E are all integers that have a value of 0 at time = 10 ns. If E changes from 0 to 1 at time 20 ns, specify the times (s) at which each signal will change and the value to which it will change. List these changes in chronological order. List any delta delays as a separate entry.

```
P1: process
    begin
       wait on E;
       A <= transport 1 after 5 ns;
       B <= A + 7;
       C <= B after 10 ns;
       B <= B + 9;
       wait for 0 ns;
       D <= B after 3 ns;
       A <= transport A + 3 after 5 ns;
       B <= A + 7;
    end process P1;
```

Time	A	B	C	D	E
10 ns	0	0	0	0	0
20 ns	0	0	0	0	1
20 ns + Δ	0	9	0	0	1
20 ns + 2Δ	0	7	0	0	1
23 ns	0	7	0	9	1
25 ns	3	7	0	9	1