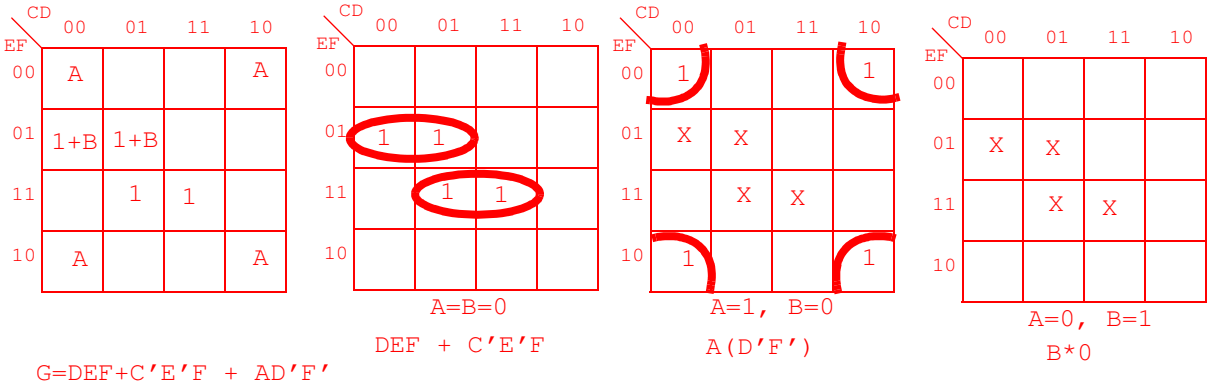
CPE/EE 422/522 **EXAM 1** **Name** KEY

Fall Semester 2008

Work should be performed systematically and neatly with the final answer being underlined. This exam is closed book, closed notes, closed neighbor. Allowable items on desk include: exam, data manual, pencils, straight edge, and calculator. All other items must be removed from student's desk. Students have approximately 90 minutes (1 1/2 hours) to complete this exam. Best wishes!

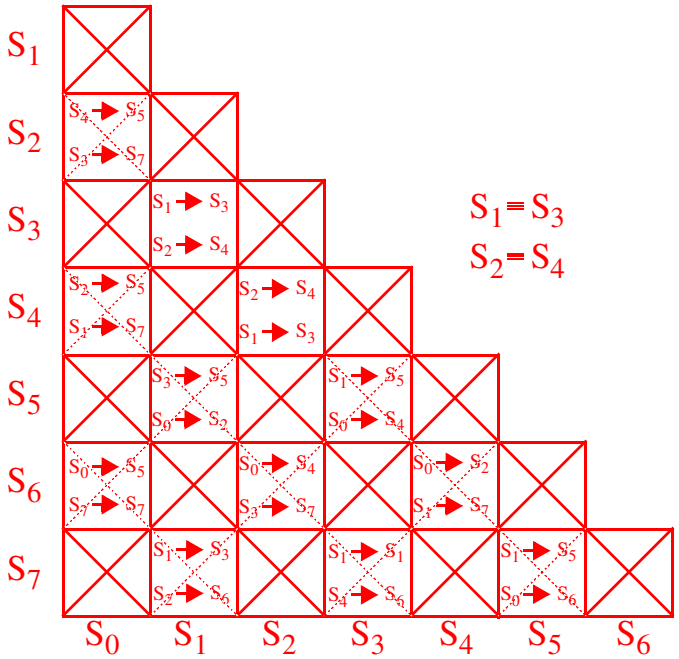
1. [5 points] For the Boolean function shown below find the minimum sum of products (SOP) expression using 4-variable Knaugh map(s) with map-entered variables.

$$G = DEF + C'E'F + AD'EF' + AD'E'F' + BC'E'F$$



G=DEF+C'E'F + AD'F'

2. [10 points] Reduce the following state table to a minimum number of states



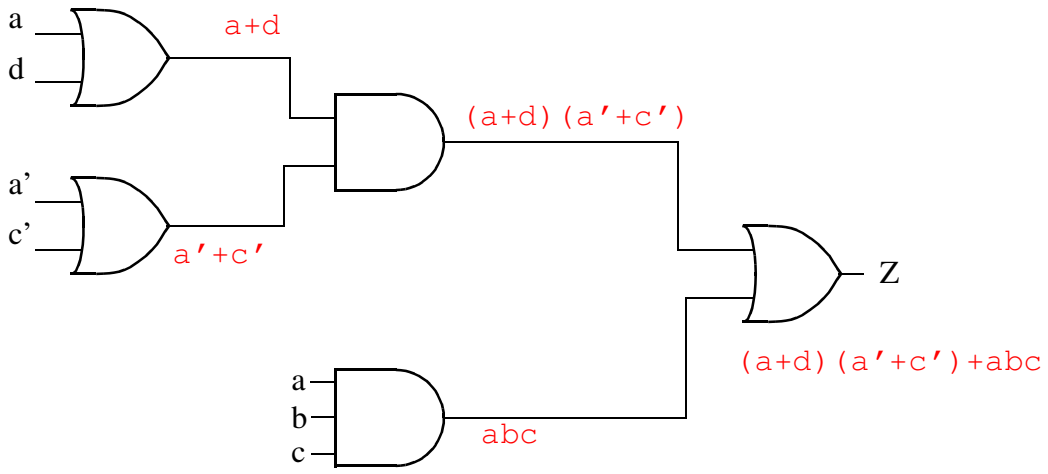
present state	next state X=0	next state 1	present output
S_0	S_5	S_7	0
S_1	S_3	S_2	1
S_2	S_4	S_3	0
S_3	S_1	S_4	1
S_4	S_2	S_1	0
S_5	S_5	S_0	1
S_6	S_0	S_7	0
S_7	S_1	S_6	1

present state	next state X=0	next state 1	present output
S_0	S_5	S_7	0
S_1	S_1	S_2	1
S_2	S_2	S_1	0
S_5	S_5	S_0	1
S_6	S_0	S_7	0
S_7	S_1	S_6	1

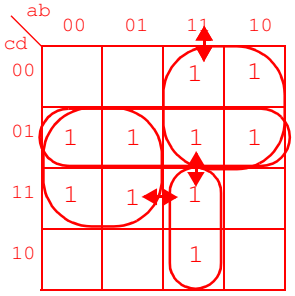
3. [12 points total] In general, what are static hazards in a combinational network? [2 points]

A hazard is an unwanted switching transient that appear on the output of a combinational network. These transients are caused by different delay paths from input to the outputs. Static hazards the output momentarily goes to the incorrect value when an input changes when it should remain constant.

For the network shown below, find any/all static 1-hazards. For any 1-hazard found specify the conditions which will cause the hazard to appear at the output (i.e. specify the logic values of the variables which are constant and the variable which is changing)[10 points].



Z = aa' + ac' + a'd + c'd + abc

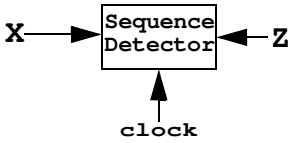


Hazard 1
A=1, B=1, D=0, C changing

Hazard 2
A=1, B=1, D=1, C changing

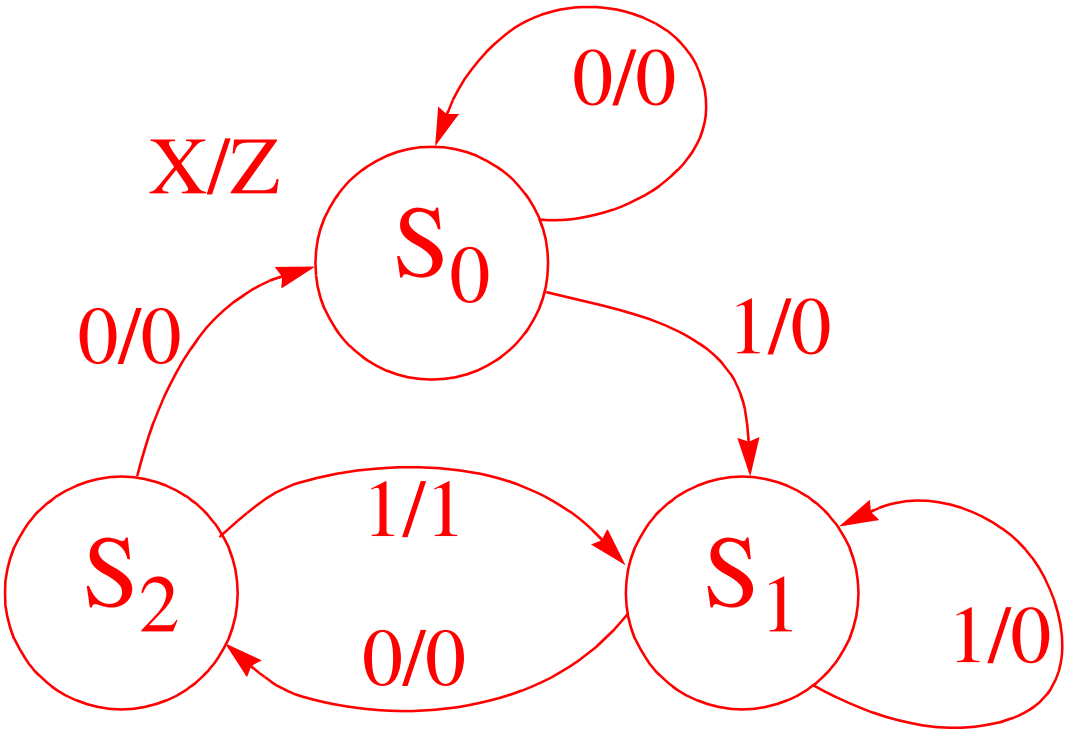
Hazard 3
B=1, C=1, D=1, A changing

4. [10 points total] Design the state graph of a clocked Mealy sequential network implementation of a sequence detector. The network is to examine a strig of 0's and 1's that is supplied on its X input and generate an ouput Z=1 only when a prescribed input sequence occurs (in all other cases an output of Z=0 should be generated). Specifically the network is to be implemented so that any input sequence ending in 101 will produce an output Z=1 coincident (at the same time) with the last 1 in the sequence. The network does not reset with a 1 occurs at the output. The network has the form shown below and a typical input sequence and the corresponding output sequence are also shown below.



X = 0 0 1 1 0 1 1 0 0 1 0 1 0 1 0 0
Z = 0 0 0 0 0 1 0 0 0 0 0 1 0 1 0 0

You are to design the state graph for a three state Mealy sequential network that will implement this design. Use the arc labeling convention discussed in the class and label your states S_0, S_1, and S_2, with S_0 being your beginning state. You are only required to implement the state graph.

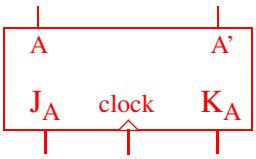


5. [5 points] From the next state map of Flip-Flop A shown below, derive the minimized sum-of-product (SOP) input equations for this flip-flop assuming that it is a J-K type Flip-Flop..

BC \ A	0	1
00	1	1
01	x	x
11	0	0
10	0	x

A^+

Next state map for Flip-Flop A



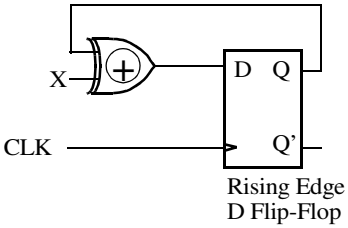
BC \ A	0	1
00	1	1
01	x	x
11	0	x
10	0	x

$J_A = B'$

BC \ A	0	1
00	x	0
01	x	x
11	x	1
10	x	x

$K_A = C$

6. [10 points] For the network shown below, the D flip-flop has a setup time of 5 ns, a hold time of 2 ns, and a propagation delay from the rising edge of the clock to the change in flip-flop output in the range of 6 to 12 ns. The propagation delay of the XOR gate is in the range of 1 to 8 ns.



What is the maximum clock frequency for proper operation of the network?

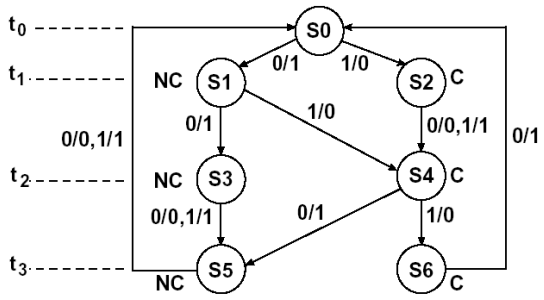
$$t_{clk} \geq t_{pmax} + t_{cmax} + t_{su} = 12\text{ns} + 8\text{ns} + 5\text{ns} = 25\text{ns}$$

$$f_{max} = \frac{1}{t_{clk_{MIN}}} = \frac{1}{25\text{ns}} = 40\text{Mhz}$$

What is the earliest time after the rising clock edge that X is allowed to change?

$$t_y \geq t_h - t_{cxmin} = 2\text{ns} - 1\text{ns} = 1\text{ns}$$

7. [10 points] Develop a two process VHDL model for the state graph shown below:



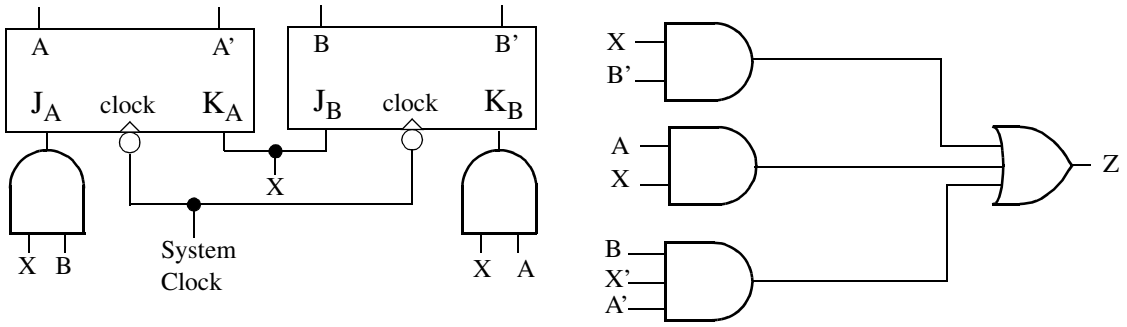

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity SM is
   port(X,CLK: in STD_LOGIC;
            Z : out STD_LOGIC;
   }
end SM;

architecture BEHAVIORAL of SM is
   signal STATE, NEXTSTATE: integer range 0 to 6 :=0;
   begin
      P1:process(STATE,X)
      begin
         case STATE is
            when 0 =>
              if X='0' then Z<='1'; NEXTSTATE<=1; end if;
              if X='1' then Z<='0'; NEXTSTATE<=2; end if;
            when 1 =>
              if X='0' then Z<='1'; NEXTSTATE<=3; end if;
              if X='1' then Z<='0'; NEXTSTATE<=4; end if;
            when 2 =>
              if X='0' then Z<='0'; NEXTSTATE<=4; end if;
              if X='1' then Z<='1'; NEXTSTATE<=4; end if;
            when 3 =>
              if X='0' then Z<='0'; NEXTSTATE<=5; end if;
              if X='1' then Z<='1'; NEXTSTATE<=5; end if;
            when 4 =>
              if X='0' then Z<='1'; NEXTSTATE<=5; end if;
              if X='1' then Z<='0'; NEXTSTATE<=6; end if;
            when 5 =>
              if X='0' then Z<='0'; NEXTSTATE<=0; end if;
              if X='1' then Z<='1'; NEXTSTATE<=0; end if;
           when 6 =>
              if X='0' then Z<='1'; NEXTSTATE<=0; end if;
             when others => null;
         end case;
      end process P1;

      P2:process(CLK)
      begin
         if (CLK='1) then
            STATE <= NEXTSTATE;
         end if;
       end process P2;

end BEHAVIORAL;
```

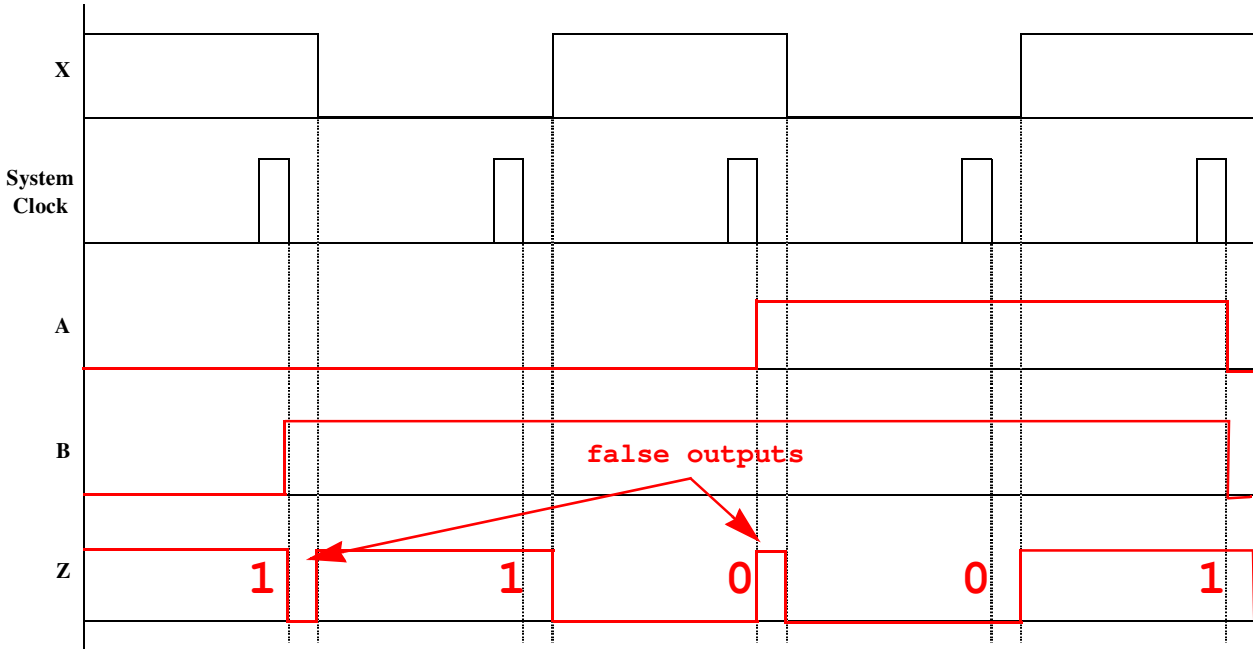
8. [13 points] In the following VHDL model fragment (which corresponds to a portion of the architecture section of a VHDL file) A, B, C, and D are all integers that have a value of 0 at time = 10ns. If E changes from '0' to '1' at time 20 ns, specify the times (s) at which each signal will change and the value to which it will change. List these changes in chronological order. List any delta delays as a separate entry.

```
P1: process
    begin
       wait on E;
       A <= inertial 1 after 5 ns;
       B <= A + 2;
       wait for 0 ns;
       A <= inertial A + 7 after 15 ns;
       B <= B + 5;
     end process P1;

C <= B after 10 ns;

P2: process(B)
    begin
       D <= B after 5 ns;
    end process P2;
```

Time	A	B	C	D	E
10 ns	0	0	0	0	0
20 ns	0	0	0	0	1
20 ns + Δ	0	2	0	0	1
20 ns + 2Δ	0	7	0	0	1
25 ns	0	7	0	7	1
30 ns	0	7	7	7	1
35 ns	7	7	7	7	1

9. [10 points] Complete the following timing diagram for signals A, B, and Z for the network shown below assuming that all setup and hold times for the flip-flops have been met and all propagation delays through the gates and flip-flops are negligible (i.e. zero). Also assume that the two flip-flops are clocked on the falling edge of the system clock and are in the reset state (i.e. A='0' and B='0') at the beginning of the timing diagram.





What type of sequential network is this?
Meally Sequential network because the ouput depends on both the current state and the input.

Write down the output sequence for Z.
Z = 11001 with increasing time -- note out is read before falling edge of clock
Are there any 'false' outputs on the timing diagram? If so clearly identify them. See timing diagram.

10. [15 points] Show the block diagram for your solution to the Keypad Interface Laboratory assignment (you do not have to include the debounce logic). If your solution was entered using schematic capture techniques then show the major components such as counters, decoders, multiplexers, individual logic gates etc. If your solution was VHDL based, show the major model component in the architecture section of your VHDL model.

Answers vary based upon particular design you implemented in the lab.