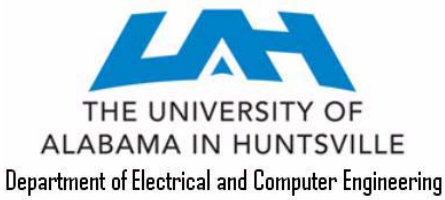

CPE 322 Digital Hardware Design Fundamentals

Simulation Assignment #3

Design of and Simulation of a Temperature Sensor Interface Module

Purpose

The purpose of this simulation assignment is to give each student the chance to develop and fully simulate a component module that can be easily incorporated into a larger system-level design. A goal of this project is for students to gain some proficiency in utilizing the capabilities of Verilog HDL to create logic that can generate arbitrarily specified multi-signal waveforms. The design element that is created and verified through simulation in this assignment will be actually implemented in Laboratory 8 of the CPE 324 Advanced Logic Design Class. The corresponding project in that class will be to develop a temperature sensor interface that employes this module to continuously display the room temperature in both the Fahrenheit and Celsius scales.

Project Overview (Big Picture)

Each student is to assume that he/she is a digital design engineer that is employed at a leading embedded systems corporation. The task at hand is to develop the interface electronics to implement a temperature sensor that is to continuously display the current temperature in Fahrenheit and Celsius. The interface electronics is to be designed using dedicated application specific logic as opposed to a microprocessor, and is to interface to two seven segment display elements (such as LEDs or LCDs). Because of mass procurements of parts by the previous corporate administration (before the Chapter 11 reorganization effort began), it is a design requirement that the design must utilize a Dallas Semiconductor DS1620 integrated circuit. This accommodates another requirement that all temperature readings are to be accurate to plus or minus 0.5 degrees Celsius. The final implementation is to be a dedicated application specific IC but the design will first be rapidly prototyped using within a FPGA. The targeted rapid prototyping platform is to be the be the Teriasic/Altera DE-2 Board used in the CPE 324 lab. On this platform its should provide the following functions. The temperature acquisition process should be continuous but should be able to be reset when one presses and releases the specified clear (CLR) button. Switching between Fahrenheit and Celsius should be accomplished by moving a specified toggle switch from one position to the other position. Digital readouts of the temperature should occur on two of the seven segment LEDs with half temperatures and temperatures over 99 degrees should be indicated through other LEDs.

Portion of the Design to be Simulated

Before his employment contract was terminated during the last round of lay-offs at the company, the person who was responsible for the temperature sensor design had created the high-level design that is shown in Figure 1. In this design, he incorporated the *BINTOHEX*, and the *TEMP2BCD* components that were present in the corporation's Intellectual Property Core (IPC) library. He also developed a PLL based clock division module, *CLOCK_DIVIDE*, to slow down the system clock so that it could be used in an indirect manner to clock the DS1620 IC. It turns out that the only module that needs to be designed is the one that is labeled *DS1620_INTERFACE*. This module is clocked by the divided clock signal and drives the DS 1620's DQ bidirectional signal (using the non-inverting tri-state pin buffer), RST input, and the DS 1620 CLK input.

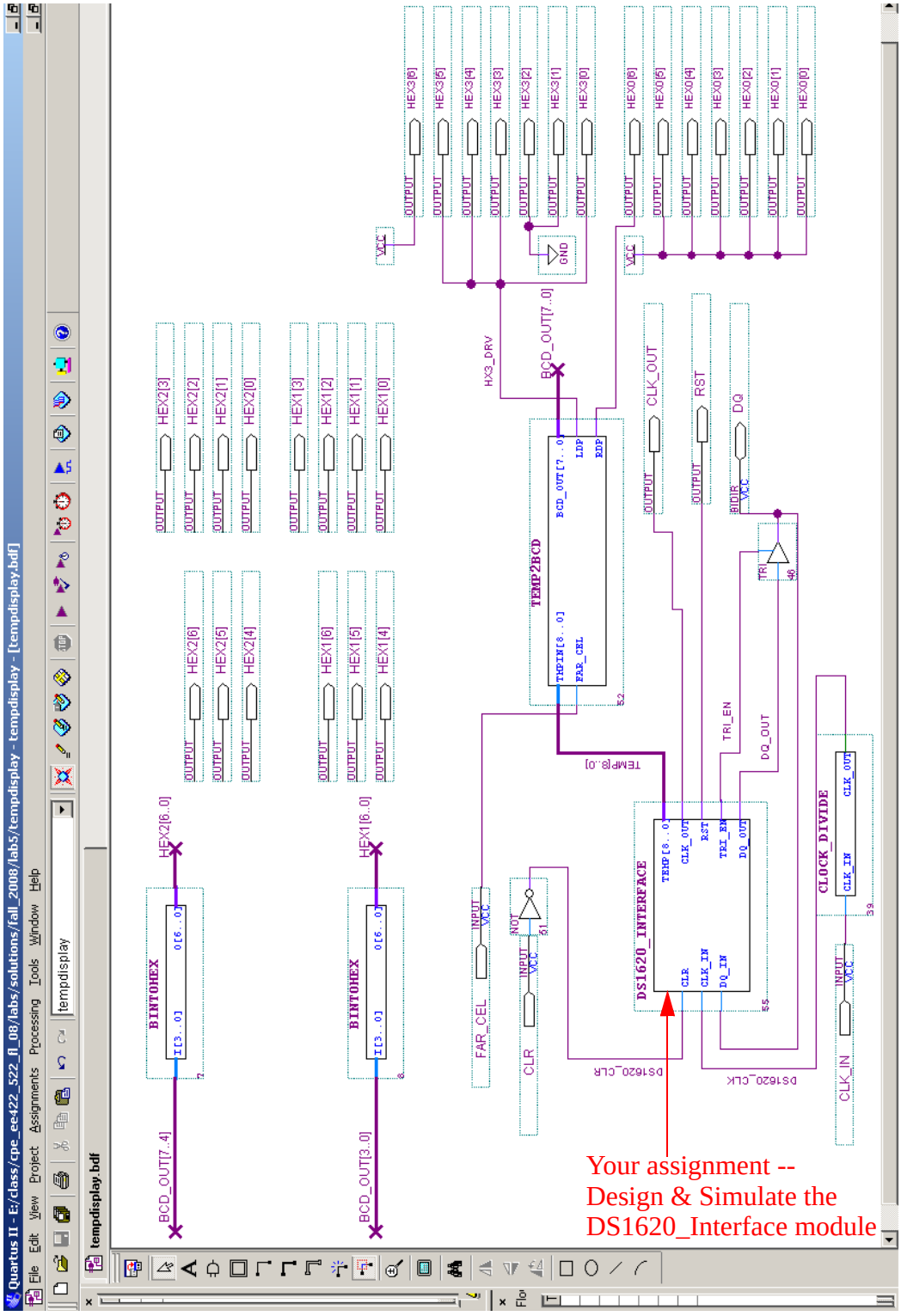

Figure 1. High-level Structural Representation of Temperature Sensor Design

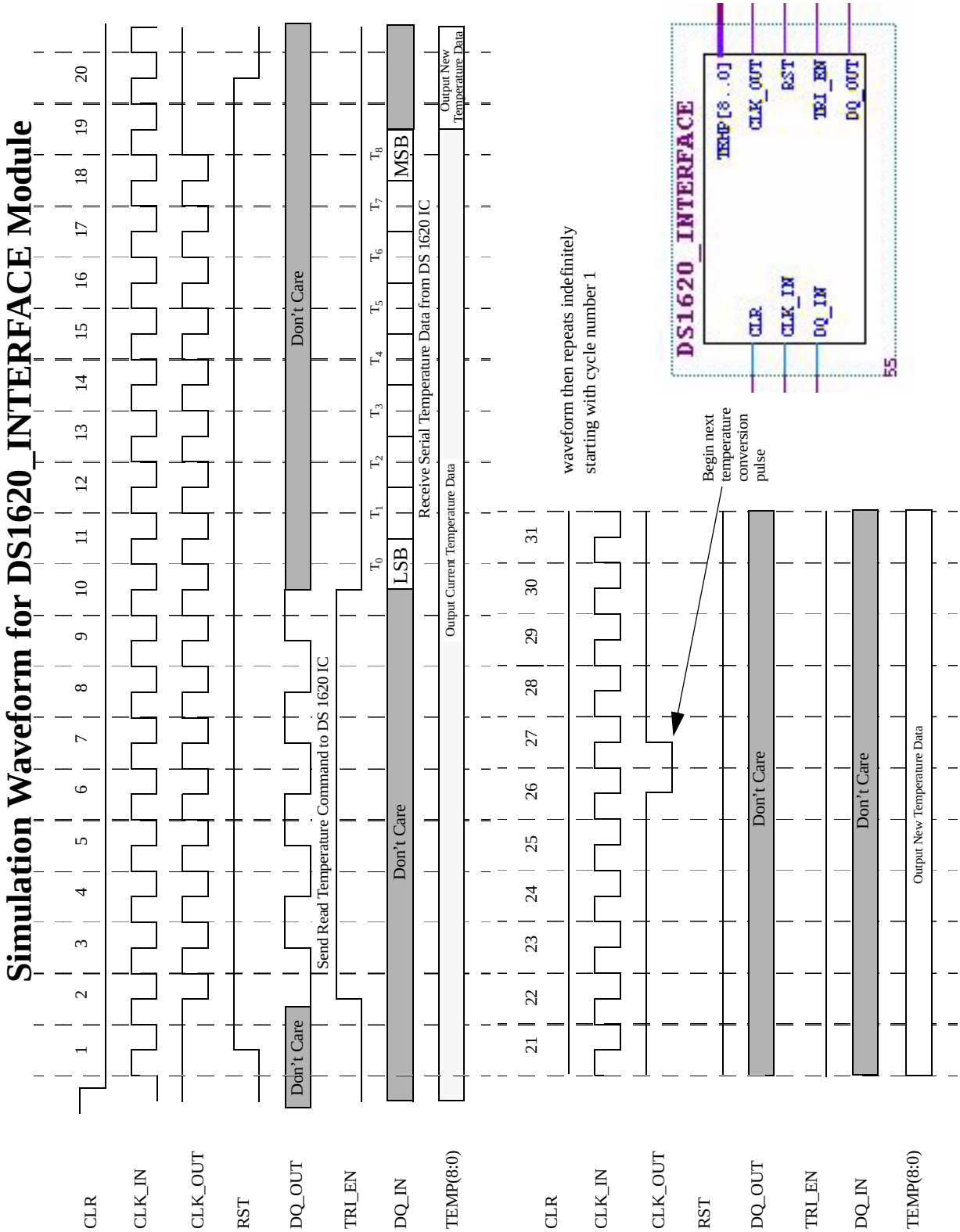

Figure 2. Waveform to be Generated by the DS1620_INTERFACE Module

Waveform Requirements

During his last preliminary design review, before he was laid off, the engineer that preceded you proposed that the DS 1620 IC be run in thermostat mode with the interface logic being designed so it would periodically strobe the CLK/$\overline{\text{CONV}}$ pin of the DS 1620 to cause it to perform continuous temperature measurements and conversions. The temperature would then be read by the interface logic from the DS 1620 using the so called "three wire" mode that is discussed in the DS 1620 Data Sheet (that is also posted on Canvas). In this mode, the DQ pin must first be driven in a serial manner by the interface circuitry that is being designed. Upon receiving the read temperature command, the direction of the DQ pin would then change and the DS 1620 would drive the DQ pin in a serial manner to output the 9 bit temperature reading. Then the process would be repeated in a continuous manner. The complete protocol for the three wire operation is described in detail in the DS 1620 data sheet but the previous design engineer was able to extract from this documentation a detailed timing diagram that related directly to the *DS1620_INTERFACE* element that was to be created. ***This timing diagram is shown in Figure 2. This waveform is composed of 31 cycles and begins after the first rising edge of the divided system clock after the CLR signal has gone low. It then repeats itself indefinitely. Your assignment is to create a Verilog HDL module that exactly replicates this timing and to demonstrate it using through RTL level ModelSim simulation. Important Note: the simulation model must also synthesizable in Quartus II as well simulatable within the ModelSim environment.***

Assignment

This project is already two months behind schedule and your supervisor has assigned you the task of completing the design. She has imposed a deadline of 04/6/15 for you to develop a complete simulation of at least one complete 31 cycle waveform that match the one shown in Figure 2. In your simulation you are to assume a 1 Mhz clock frequency and you are to provide at appropriate portion of the waveform the necessary 9-bit output that will come from the DS 1620 IC as shown in Figure 2. Remember, you need to complete this simulation during the specified time period because the next round of lay-offs has been rumored for next month and your plan to get rich quick in the video gaming market is not panning out as wells as you expected.

The assignment for this simulation includes

1) the design and complete documentation of the *DS1620_INTERFACE* Verilog HDL module
2) the complete simulation of the *DS1620_INTERFACE* design to validate its operation under the same set of stimulus as in Figure 2.

Each student is to work individually.

Deliverables

The final simulation submission should include source Verilog HDL modeling code, and a write up that includes your simulation stimulus commands, and your resulting output waveform that is composed of all signals that are specified in Figure 2.

Simulation Assignment Turn in Procedure

The due date for this simulation is Monday 11:59 PM April 6, 2015. This is to be an electronic submission -- no hardcopy needs to be turned in to the instructor. You are to upload to the course UAH Canvas dropbox a copy of the simulation assignment on or before its due date. Acceptable file formats include pdf, doc, and docx. This simulation assignment will be graded based on correctness, completeness and clarity of presentation.