CPE322
SIM 03 HW
Christopher Bero

DS1620 Module

```
module DS1620_INTERFACE(input CLR, CLK_IN, output reg [8:0] TEMP,
   output reg CLK_OUT,RST,TRI_EN, input DQ_IN, output reg DQ_OUT);

reg [4:0] count = 0;
reg [8:0] dq_out_buff = 0;

//reg CLK_OUT, RST, TRI_EN;

//initial
//begin
     /*DQ_OUT = 0;
     TEMP = 0;
     CLK_OUT = 1;
     RST = 0;
     TRI_EN = 0;*/
//end

always @(CLK_IN)
begin

if (count > 1 && count < 19)
          CLK_OUT = CLK_IN;

if (CLK_IN == 1) // posedge
begin
     // Handle clk_out
     if (count == 26 || count == 27)
          CLK_OUT = 0;
     else if (!(count > 1 && count < 19))
          CLK_OUT = 1;

     if (CLR)
     begin
          count = 1;
          dq_out_buff = 0;
          TEMP = 0;
          CLK_OUT = 1;
     end
     else // CLR not set
     begin
          /*if (count > 31) begin
               count = 1; // Proceed to loop
          end*/

          // Handle RST output
          if (count < 20) begin
               RST = 1;
          end
          else begin
               RST = 0;
          end

          // Handle DQ_OUT
          if (count == 2 || count == 4 || count == 6 || count == 8)
```

```
begin
                DQ_OUT = 0;
           end
           else begin
                DQ_OUT = 1;
           end

           // Handle TRI_EN output
           if (count > 1 && count < 11) begin
                TRI_EN = 1;
           end
           else begin
                TRI_EN = 0;
           end

           // Handle Filling dq_out_buff
           if (count > 9 && count < 19) begin
                dq_out_buff = dq_out_buff << 1; // make room to load
next input
                dq_out_buff[0] = DQ_IN;
           end

           // Handle TEMP output
           if (count == 19) begin
                TEMP = ((~dq_out_buff)+1);
           end

           // Reset buffer
           if (count == 8)
                dq_out_buff = 0;

           count = count + 1; // Prep for next clock cycle
      end
end

end
endmodule
```

Stimulus

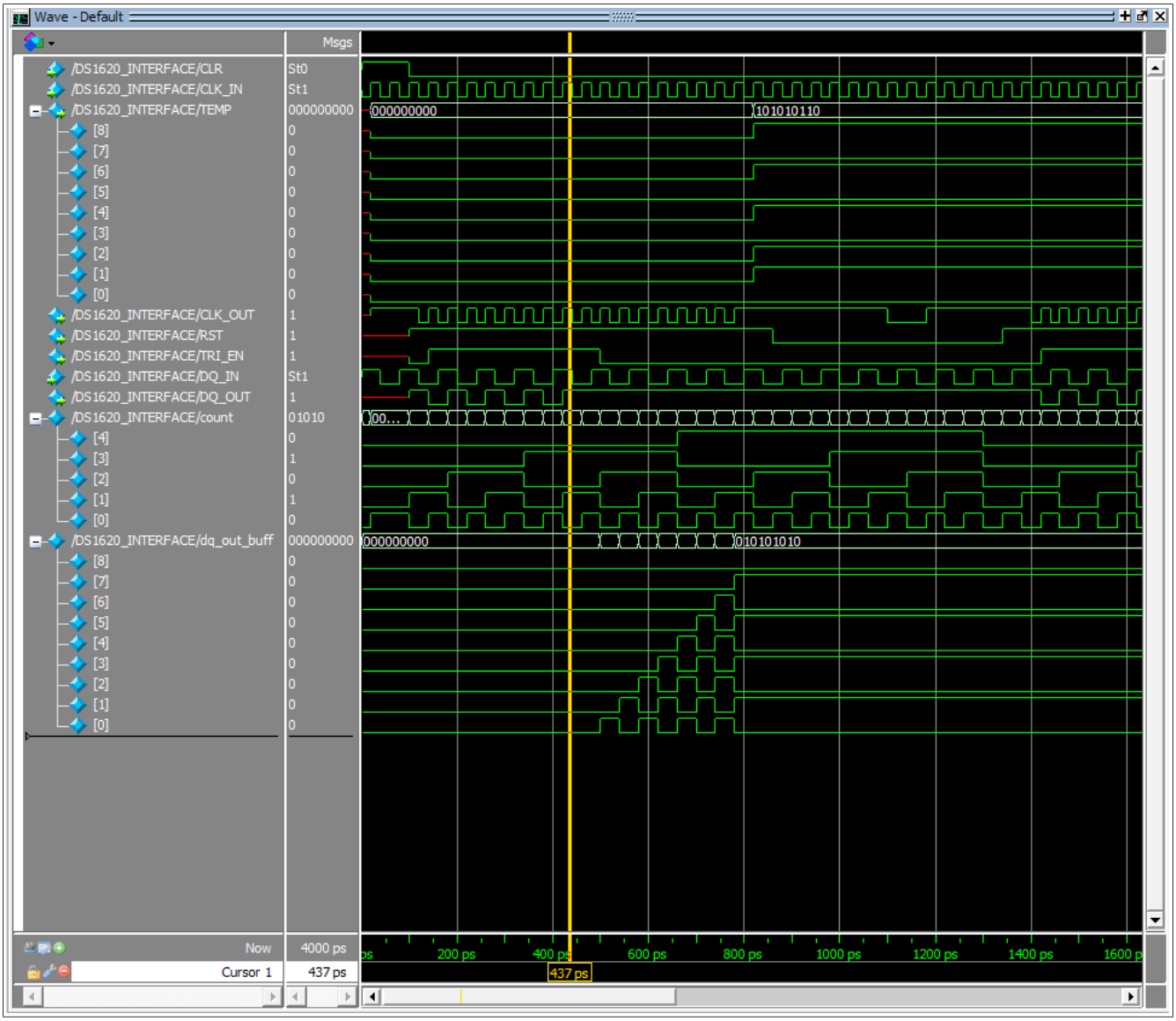
```
#
# Stimulus
# [0] is LSB
# SUB_ADD: 0=add (A+B), 1=subtract (A-B)
# Library: cycloneive_ver
#

force CLR 1 0, 0 100

force DQ_IN 1 0, 0 40 -repeat 80

force CLK_IN 0 0, 1 20 -repeat 40

run 4000
```

Output

List - Default

ps / delta	/CLR	/TRI_EN	/CLK_IN	/DQ_IN	/TEMP	/DQ_OUT	/CLK_OUT	/RST	/count	/dq_out_buff
0 +0	St1	St0	xxxxxxxxx	x	x	x	St1	x	00000	000000000
20 +0	St1	St1	000000000	1	x	x	St1	x	00001	000000000
40 +0	St1	St0	000000000	1	x	x	St0	x	00001	000000000
60 +0	St1	St1	000000000	1	x	x	St0	x	00001	000000000
80 +0	St1	St0	000000000	1	x	x	St1	x	00001	000000000
100 +0	St0	St1	000000000	1	1	0	St1	1	00010	000000000
120 +0	St0	St0	000000000	0	1	0	St0	1	00010	000000000
140 +0	St0	St1	000000000	1	1	1	St0	0	00011	000000000
160 +0	St0	St0	000000000	0	1	1	St1	0	00011	000000000
180 +0	St0	St1	000000000	1	1	1	St1	1	00100	000000000
200 +0	St0	St0	000000000	0	1	1	St0	1	00100	000000000
220 +0	St0	St1	000000000	1	1	1	St0	0	00101	000000000
240 +0	St0	St0	000000000	0	1	1	St1	0	00101	000000000
260 +0	St0	St1	000000000	1	1	1	St1	1	00110	000000000
280 +0	St0	St0	000000000	0	1	1	St0	1	00110	000000000
300 +0	St0	St1	000000000	1	1	1	St0	0	00111	000000000
320 +0	St0	St0	000000000	0	1	1	St1	0	00111	000000000
340 +0	St0	St1	000000000	1	1	1	St1	1	01000	000000000
360 +0	St0	St0	000000000	0	1	1	St0	1	01000	000000000
380 +0	St0	St1	000000000	1	1	1	St0	0	01001	000000000
400 +0	St0	St0	000000000	0	1	1	St1	0	01001	000000000
420 +0	St0	St1	000000000	1	1	1	St1	1	01010	000000000
440 +0	St0	St0	000000000	0	1	1	St0	1	01010	000000000
460 +0	St0	St1	000000000	1	1	1	St0	1	01011	000000000
480 +0	St0	St0	000000000	0	1	1	St1	1	01011	000000000
500 +0	St0	St1	000000000	1	1	0	St1	1	01100	000000001
520 +0	St0	St0	000000000	0	1	0	St0	1	01100	000000001
540 +0	St0	St1	000000000	1	1	0	St0	1	01101	000000010
560 +0	St0	St0	000000000	0	1	0	St1	1	01101	000000010
580 +0	St0	St1	000000000	1	1	0	St1	1	01110	000000101
600 +0	St0	St0	000000000	0	1	0	St0	1	01110	000000101
620 +0	St0	St1	000000000	1	1	0	St0	1	01111	000001010
640 +0	St0	St0	000000000	0	1	0	St1	1	01111	000001010
660 +0	St0	St1	000000000	1	1	0	St1	1	10000	000010101
680 +0	St0	St0	000000000	0	1	0	St0	1	10000	000010101
700 +0	St0	St1	000000000	1	1	0	St0	1	10001	000101010
720 +0	St0	St0	000000000	0	1	0	St1	1	10001	000101010
740 +0	St0	St1	000000000	1	1	0	St1	1	10010	001010101
760 +0	St0	St0	000000000	0	1	0	St0	1	10010	001010101
780 +0	St0	St1	000000000	1	1	0	St0	1	10011	010101010
800 +0	St0	St0	000000000	1	1	0	St1	1	10011	010101010
820 +0	St0	St1	101010110	1	1	0	St1	1	10100	010101010
840 +0	St0	St0	101010110	1	1	0	St0	1	10100	010101010
860 +0	St0	St1	101010110	1	0	0	St0	1	10101	010101010
880 +0	St0	St0	101010110	1	0	0	St1	1	10101	010101010
900 +0	St0	St1	101010110	1	0	0	St1	1	10110	010101010

202 lines


Wave - Default
Msgs
/DS1620_INTERFACE/CLR
/DS1620_INTERFACE/CLK_IN
/DS1620_INTERFACE/TEMP
[8]
[7]
[6]
[5]
[4]
[3]
[2]
[1]
[0]
/DS1620_INTERFACE/CLK_OUT
/DS1620_INTERFACE/RST
/DS1620_INTERFACE/TRI_EN
/DS1620_INTERFACE/DQ_IN
/DS1620_INTERFACE/DQ_OUT
/DS1620_INTERFACE/count
[4]
[3]
[2]
[1]
[0]
/DS1620_INTERFACE/dq_out_buff
[8]
[7]
[6]
[5]
[4]
[3]
[2]
[1]
[0]
St0
St1
000000000
0
0
0
0
0
0
0
0
1
1
1
St1
1
01010
0
1
0
1
0
000000000
0
0
0
0
0
0
0
0
0
000000000
101010110
010101010
Now
4000 ps
Cursor 1
437 ps
200 ps
400 ps
600 ps
800 ps
1000 ps
1200 ps
1400 ps
437 ps