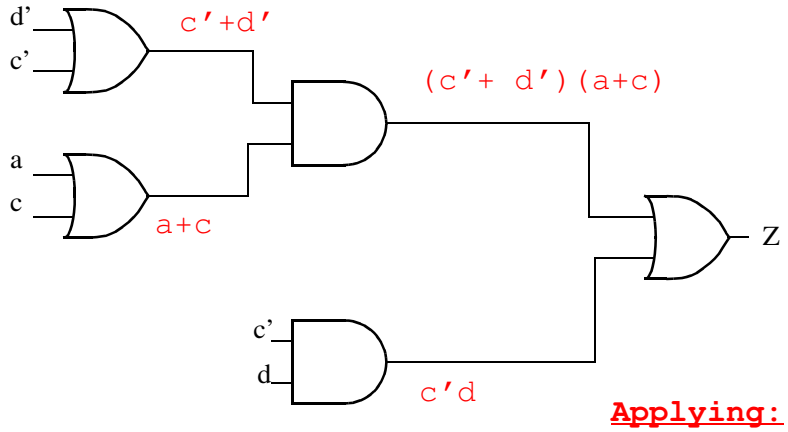
CPE 322 EXAM 2 Name KEY

Class CPE 322

Spring Semester 2014

Work should be performed systematically and neatly with the final answer being underlined. This exam is closed book, closed notes, closed neighbor. Allowable items on desk include: exam, data manual, pencils, straight edge, and calculator. All other items must be removed from student's desk. Students have approximately 150 minutes (2 1/2 hours) to complete this exam. Best wishes!

1. [15 points] For the network shown below, find all static 0-hazards. For each 0-hazard found specify the conditions which will cause the hazard to appear at the output (i.e. specify the logic values of the variables which are constant and clearly specify the variable that is assumed to be changing). If there are no 0-hazards found, use a K'map to show why this is the case.



Applying:

W+XY = (W+X)(W+Y)

Z = (c'+ d')(a+c)+c'd

= [(c'+ d')(a+c)+c'][(c'+d')(a+c)+ d]

= (c'+d'+c')(a+c+c')(c'+d'+d)(a+c+d)

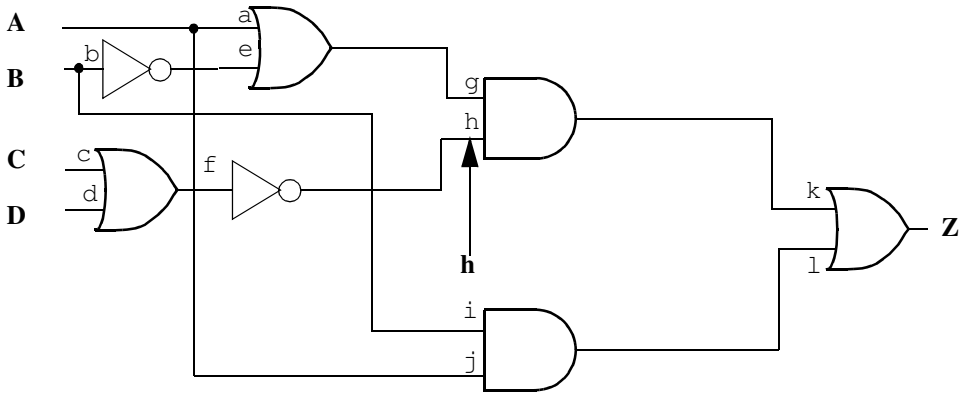
= (c'+d')(a+c+c')(c'+d'+d)(a+c+d) ← (W+X+W) = (W+X)

not mappable
1'hazard possible

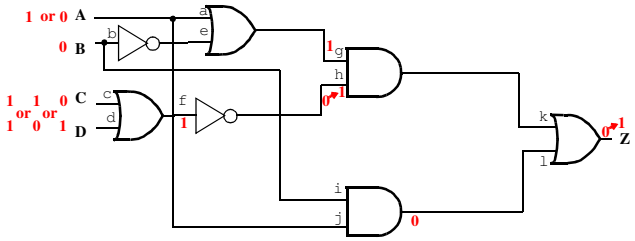
No 0-Hazards Found!

a \ cd	00	01	11	10
0	0		0	
1			0	

2. [15 points]



a) For the network above, if it is possible, determine the necessary inputs to test for a stuck-at-1 fault at point **h** as marked on the schematic diagram shown above? Assume that only points **A, B, C, D,** and **Z** can be accessed for input/output. If it is not possible to create such a test vector clearly state the reasons why this cannot be done.



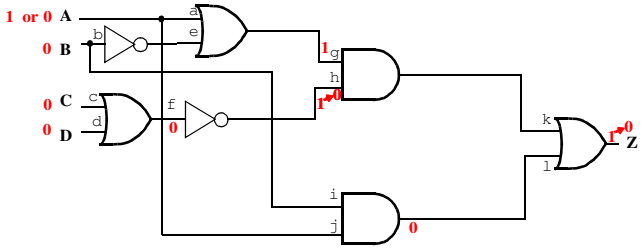
Inputs necessary to detect s-a-1 fault on h

A = X
B = 0
C+D must hold true

b) If you were able to test for the stuck-at-1 fault at point **h** in part a of this problem, determine which other stuck-at faults can be tested when the inputs that were used in part a are applied.

ABCD	Other Faults Detected	ABCD	Other Faults Detected
0001	k1,l1,d0,f0,Z1	1011	i1,k1,l1,f0,Z1
1001	i1,k1,l1,d0,f0,Z1	X001	k1,l1,d0,f0,Z1
0010	k1,l1,c0,f0,Z1	X010	k1,l1,c0,f0,Z1
1010	i1,k1,l1,c0,f0,Z1	X011	k1,l1,f0,Z1
0011	k1,l1,f0,Z1		

c) For the network above, if it is possible, determine the necessary inputs to test for a stuck-at-0 fault at point **h** as marked on the schematic diagram shown above? Assume that only points **A, B, C, D,** and **Z** can be accessed for input/output. If it is not possible to create such a test vector clearly state the reasons why this cannot be done.



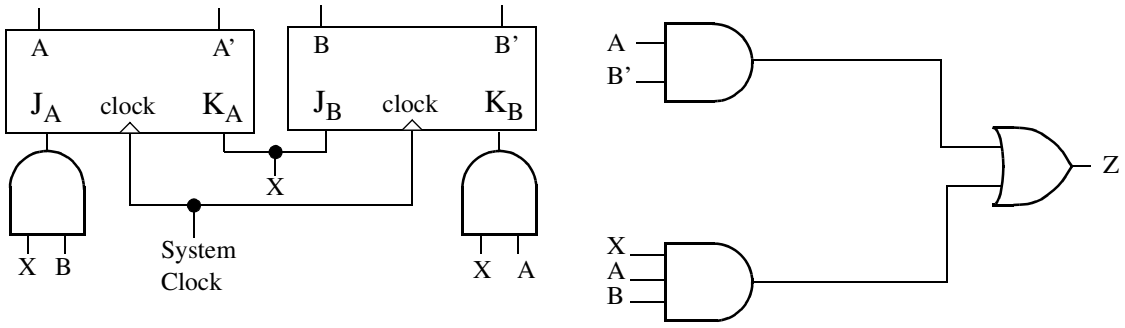
Inputs necessary to detect s-a-0 fault on h

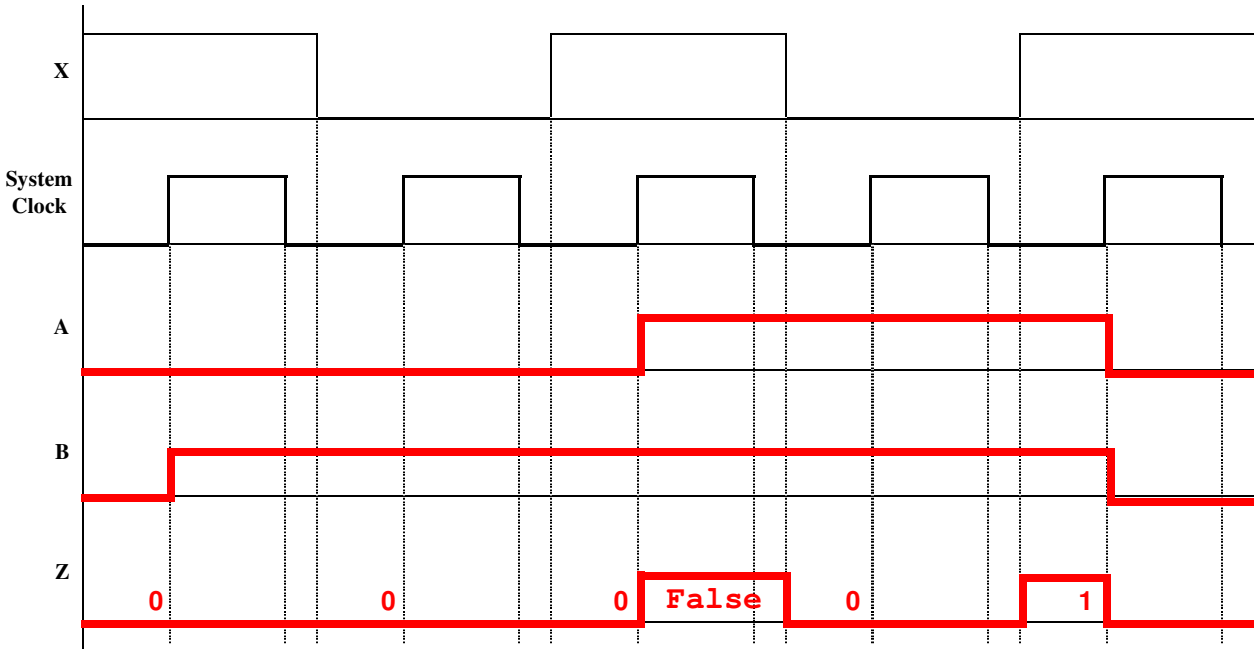
A = X
B = 0
C = 0
D = 0

d) If you were able to test for the stuck-at-0 fault at point **h** in part c of this problem, determine which other stuck-at faults can be tested when the inputs that were used in part a are applied.

ABCD	Other Faults Detected
0000	e0,g0,k0,b1,c1,d1,f1,Z0
1000	g0,k0,c1,d1,f1,Z0
X000	g0,k0,c1,d1,f1,Z0

3. [15 points] Complete the following timing diagram for signals A, B, and Z for the network shown below assuming that all setup and hold times for the flip-flops have been met and all propagation delays through the gates and flip-flops are negligible (i.e. zero). Also assume that the two flip-flops are clocked on the rising edge of the system clock and are in the reset state (i.e. A='0' and B='0') at the beginning of the timing diagram.





What type of synchronous sequential network is this?

Mealy -- output is a function of state, A,B and input X

Write down the output sequence for Z.

Sequence {0,0,0,(1) 0, 1}--read immediately BEFORE active edge in Mealy

False

Are there any 'false' outputs on the timing diagram? If so clearly identify them.

Yes, as labeled on the timing diagram

4. [15 points] Assuming that an RTL type simulation is performed for the hardware model shown below complete the timing diagram below for the internal register signals A, B, and for the output signal Z assuming that the simulation begins at time zero and the input signal X and the CLK signal are driven as shown in the timing diagram.

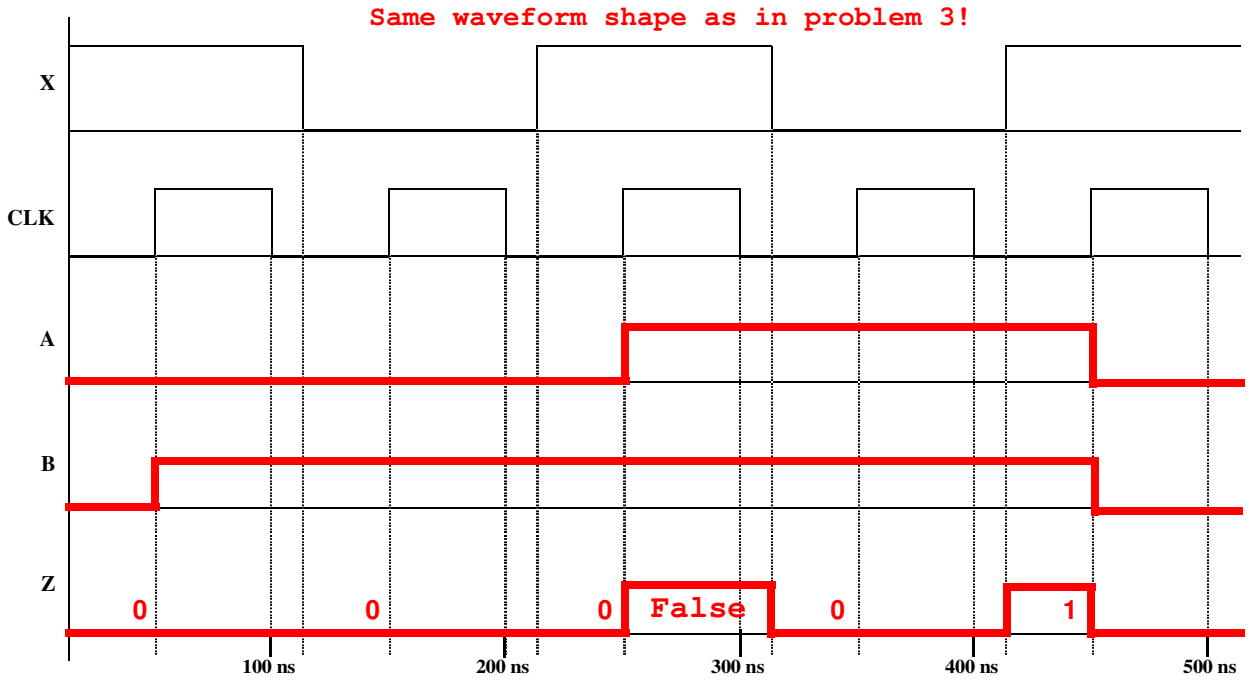
```
`timescale 1 ns / 100 ps
module seq_design(input CLK, X, output reg Z);

   reg A,B;  // Use of registers here imply that something is remembered
             // In this case it is a data flow representation of the state
   initial
      begin
         A = 1'b0;           // same as A=0;
         B = 1'b0;           // same as B=0;
       end

   always @ (posedge CLK) // Change in A and B occurs on rising edge of clock
      begin               // --a function of input and state -- output not affected
         A <= (~X & A) | (X & ~A & B);
         B <= (X & ~A) | (~X & B) | (X & ~B);
      end

   always @ (A,B,X)    // Function of state A & B and Input X -- a Mealy Network
      if (A)
         if (B) Z = X;
         else Z = 1;
      else Z = 0;

endmodule
```



What type of synchronous sequential network is this?

Mealy -- output is a function of state, A,B and input X

Write down the output sequence for Z.

Sequence {0,0,0,(1) 0, 1}--read immediately BEFORE active edge

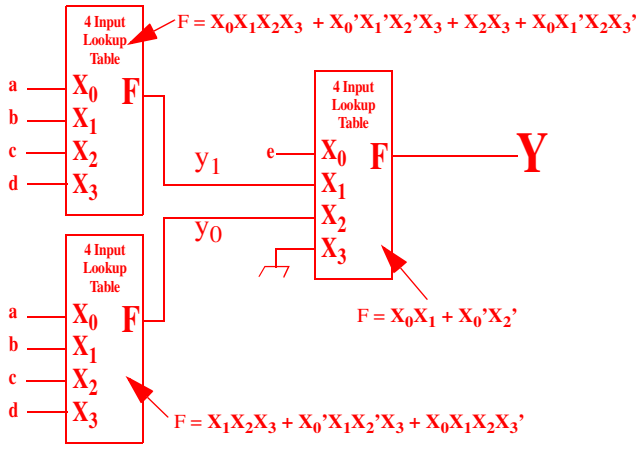
False

5. [12 points] Use Shannon's expansion theorem around **e** for the function

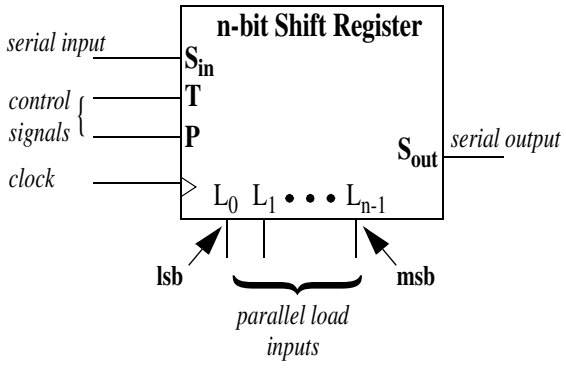
Y = abcde + bcde' + a'b'c'de + cde + ab'cd'e + a'bc'de' + abcd'e'

so that it can be implemented using only four-variable function generators (4 variable LUT). Draw a block diagram to indicate how **Y** can be implemented using only four-variable function generators. Indicate the function realized by each four-variable function generator.

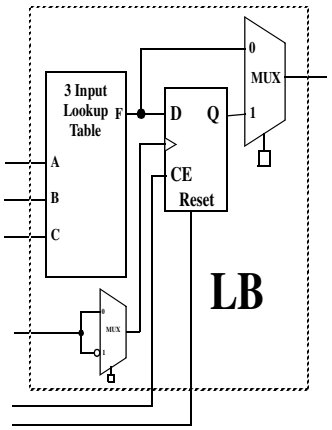
e = 1
y_1 = abcd + a'b'c'd + cd + ab'cd'
e = 0
y_0 = bcd + a'bc'd + abcd'
$Y=ey_1+e'y_0$



6. [15 points total] An multiple bit right shift register with parallel load and a single serial output is to be implemented within an FPGA that has a standard island style architecture where the basic logic blocks have the configurations shown below:



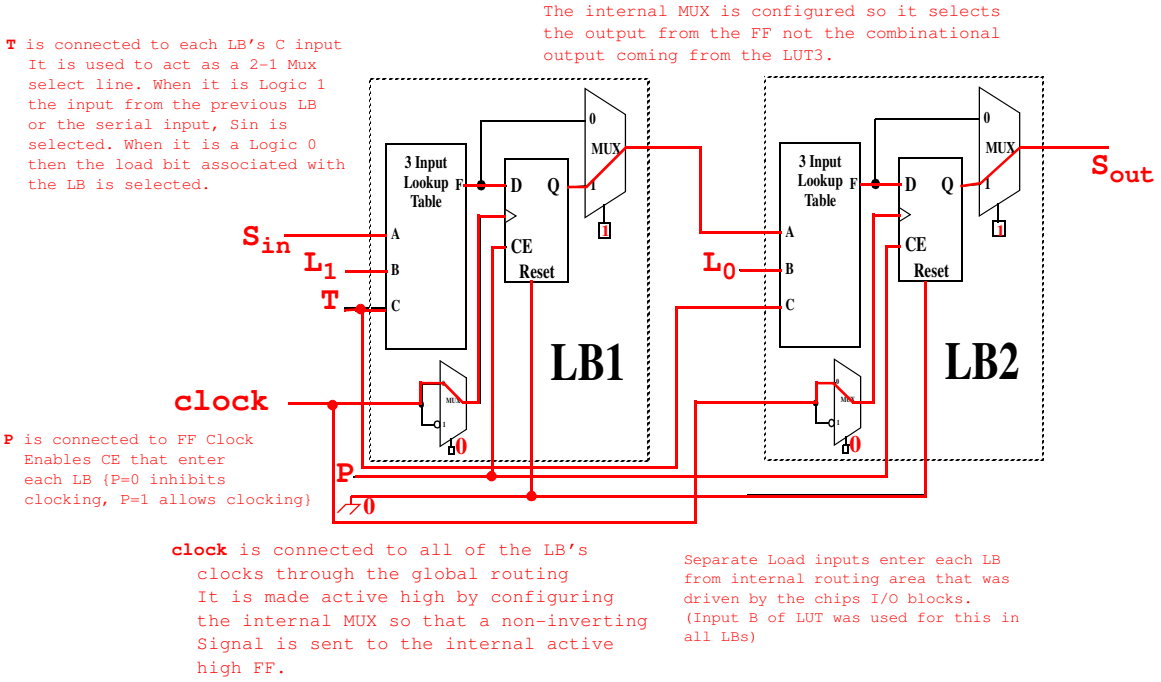
Shift Register Module to be Designed



Internal Logic Block Architecture of Targeted FPGA

The Control Signals P and T operate as follows: P='0', do nothing keep current state; P = '1' and T='1' right shift on next rising edge clock; P='1' and T='0' load values from parallel load inputs into shift register on the next rising clock edge.

a) On the figure below create a two-bit shift register using these logic blocks as basic building elements of your design. Show the necessary internal connections between subcomponents as well as the logical connections between the logic blocks themselves. Also label signals that enter and leave the logic blocks that must originate or terminate on external FPGA I/O pin locations. Such signals include the serial input, control signals, parallel load inputs and the serial output. Use the names shown on the figure.



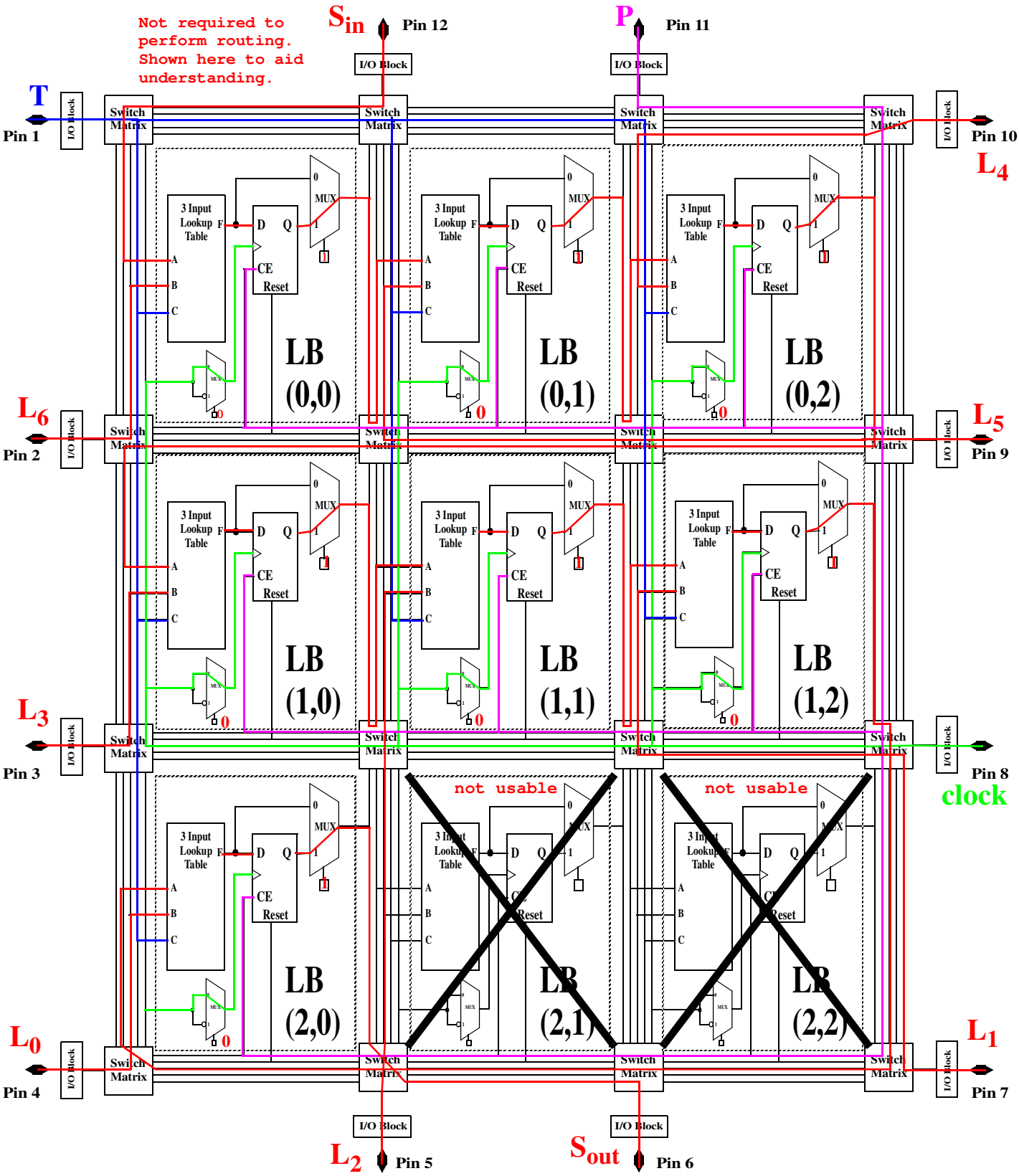
b) What are the logic equations that should be implemented by the lookup tables in the two logic blocks in part (a) of this problem.

Boolean Equation for both 3-Input Lookup Tables in LB1, LB2:

$F = AC + B\overline{C}$

(c) What is the maximum value of n for the n-bit shift register that would fit in the very small FPGA, whose floor plan is shown in the figure on the next page could support? What resource makes this value of n the limiting factor?

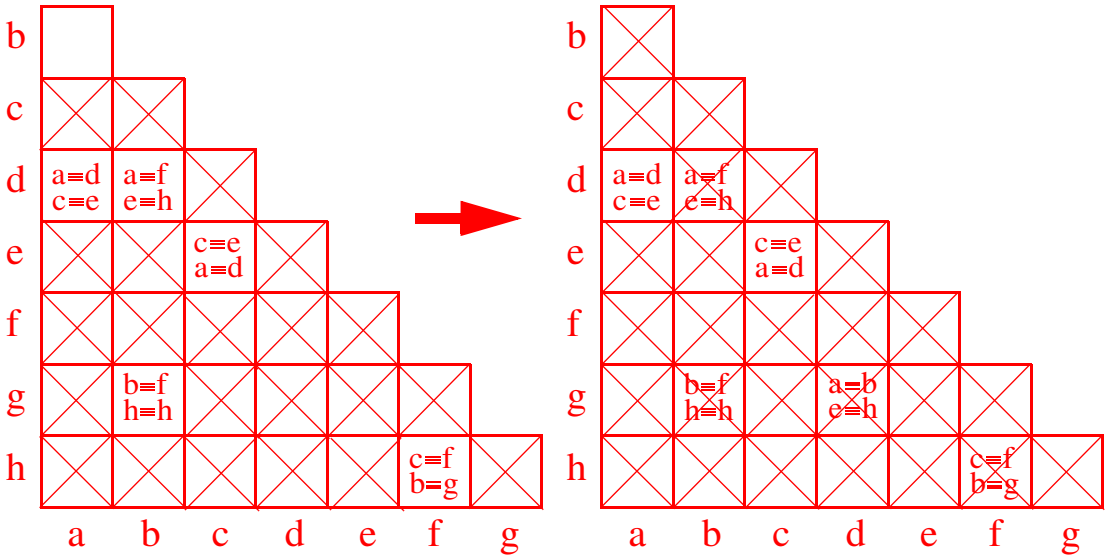
Maximum value for n is 7. Uses up all 12 I/O pins when n=7 (I/O pins are the limiting resource). Needs 4 global inputs (clock, P, T, and S_{in}) 1 global output (S_{out}) and one pin per bit of the shift register. Thus with 12 pins then n=12-(4+1)=7. There is one CLB per bit n and there are 9 CLB so this is not the limiting resource. Also routing appears to be adequate which is shown for clarity on the diagram but not required by the student in order to estimate n.



Floor-plan of Targeted island-style FPGA Device

7. [13 points] Reduce the following state table to a minimum number of states clearing identifying the states that are equivalent with one another. Show the final reduced state table.

present state	next state X=0	1	present output X=0	1
a	d	c	1	0
b	f	h	0	0
c	e	d	0	1
d	a	e	1	0
e	c	a	0	1
f	f	b	1	1
g	b	h	0	0
h	c	g	1	1



Equivalent States:

$a \equiv d$

$c \equiv e$

Reduced State Table

present state	next state X=0	1	present output
a	a	c	0
b	f	h	0
c	c	a	1
f	f	b	1
g	b	h	0
h	c	g	1