THE UNIVERSITY OF ALABAMA IN HUNTSVILLE
Department of Electrical and Computer Engineering

CPE 324 Advanced Logic Design Laboratory

Laboratory Assignment #6

Capacitance Tester

(10% of Final Grade)

Purpose

The purpose of this laboratory project is to give each student the opportunity to develop a simple combined digital/analog instrument design in Verilog HDL that can be used to measure the capacitance of a capacitor over a specified range. Students will be given the opportunity to develop two different versions of the design using Verilog HDL that vary significantly from one another in terms of the level of abstraction that is employed.

Background

In this laboratory students are to use the basic properties of a RC circuit to allow a value of capacitance to be determined by measuring the time it takes for the capacitor to discharge through a known high tolerance resistance. A 555 IC timer is used as an astable multivibrator. A complete tutorial concerning this timer is given at http://williamson-labs.com/480_555.htm. The functional block diagram of the timer is shown in Figure 1 below.

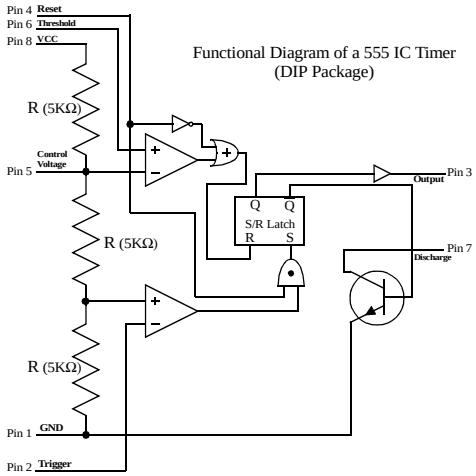


Figure 1: The Functional Block Diagram of the 555 IC Timer

The assumed 555 astable multivibrator circuit and its interface to the DE2-115 trainer are shown in Table 1.

Assignment

Students are to develop two Verilog HDL models that are to be implemented within the Altera Cyclone IV E FPGA based DE2-115 rapid prototyping trainer. The trainer is to be connected to the 555 IC-based astable multivibrator in the manner discussed on the next page. The 555 device will be implemented on a solderless breadboard. The final designs are to continuously display the value of capacitance of a selected capacitor, using four seven-segment LEDs that are present on the DE2-115 board (HEX3 -- HEX0). The design is to support the measurement of capacitances that are in the range of 0.01 µF to 99.99 µF (resolution.01µF). The first Verilog model should be a structural model that closely adheres to the block diagrams shown in Figure 3. The second Verilog model should be a high-level behavioral model that performs the same function but utilizes a single module (i.e. no sub-modules). There are two Verilog HDL templates that are posted on the course's Canvas account. Demonstrate your two designs to your laboratory instructor. In your lab report compare and contrast these two design alternatives in terms of ease of design entry and their FPGA resource utilization.

Table 1: Assumed wiring connections between DE2-115 board and the 555 IC

Signal Name	Cyclone IV E Signal Number	DE2-115 Expansion Cable Wire	555 IC Pin Number(s)	555 IC Pin Name
VCC		red wire	8, 4	$V_{CC,}$ Reset
GND		black wire	1	GND

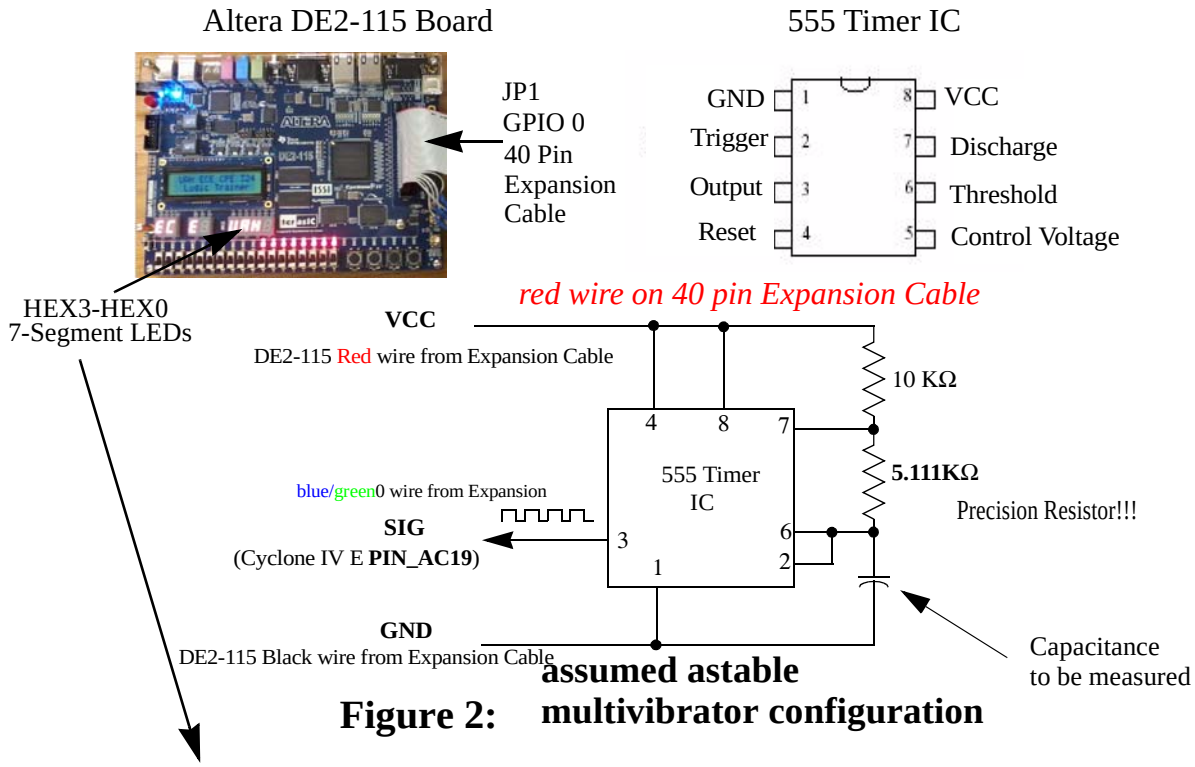


Figure 2: assumed astable multivibrator configuration

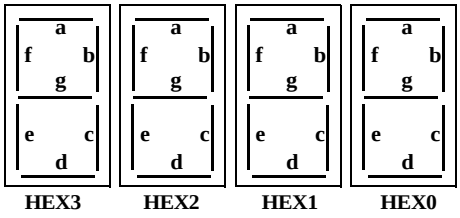


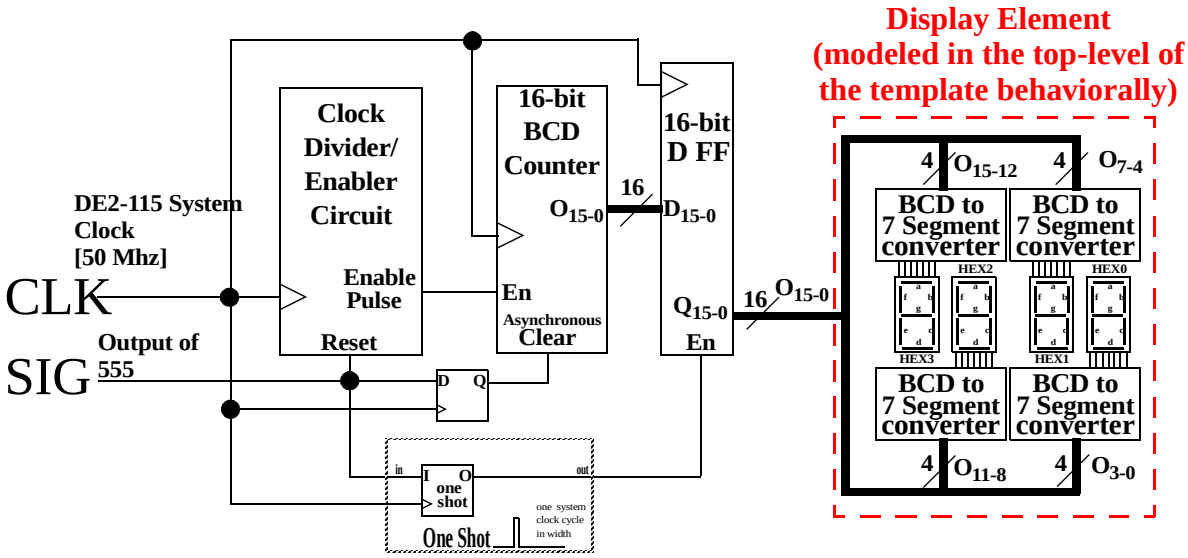
Table 2: Internal DE2-115 Clock

Signal Name	Cyclone IV E Pin Number	Description
CLOCK_50	PIN_Y2	50 MHz clock input

Table 3: Cyclone IV E Pin Numbers for HEX3-HEX0 7-Seg LEDs on DE2-115 Board

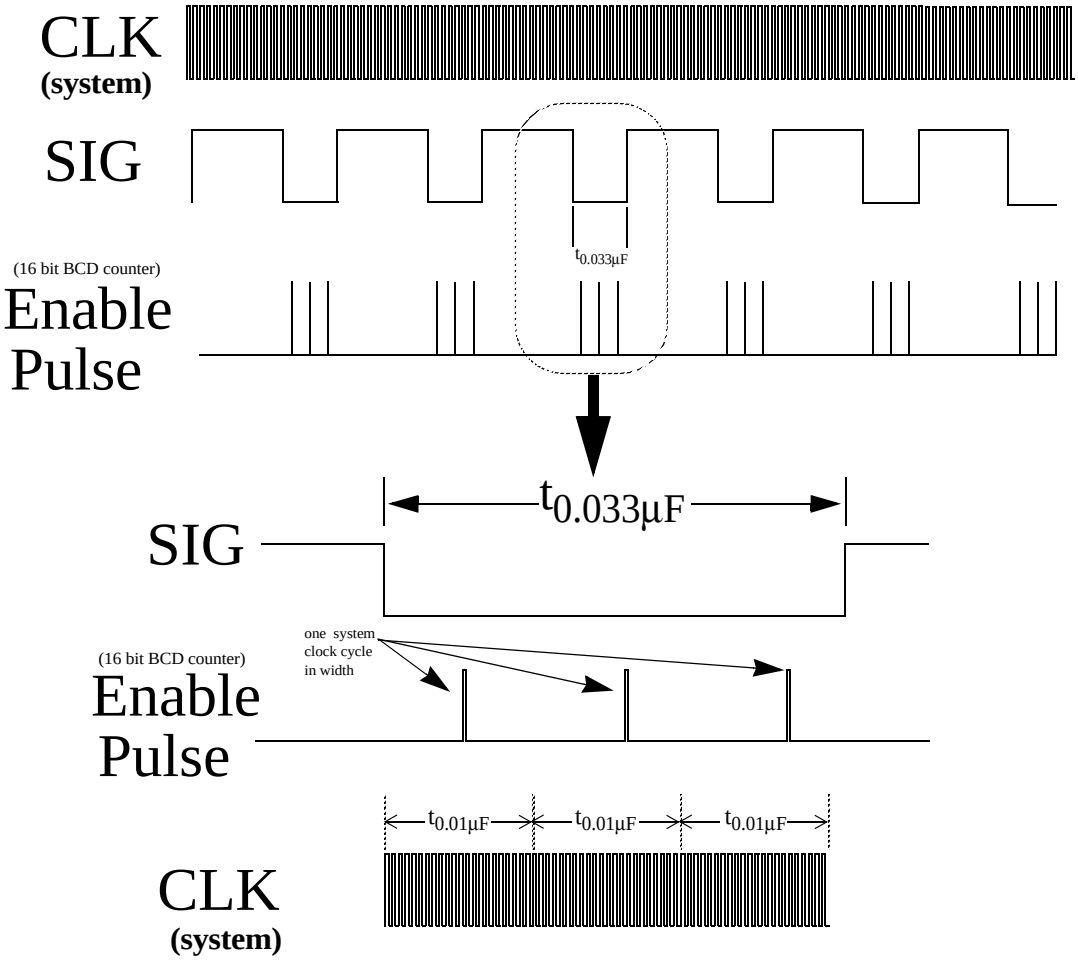
Segment	HEX3		HEX2		HEX1		HEX0	
	Signal Name	Cyclone IV E Pin No.	Signal Name	Cyclone IV E Pin No.	Signal Name	Cyclone IV E Pin No.	Signal Name	Cyclone IV E Pin No.
a	HEX3[0]	PIN_V21	HEX2[0]	PIN_AA25	HEX1[0]	PIN_M24	HEX0[0]	PIN_G18
b	HEX3[1]	PIN_U21	HEX2[1]	PIN_AA26	HEX1[1]	PIN_Y22	HEX0[1]	PIN_F22
c	HEX3[2]	PIN_AB20	HEX2[2]	PIN_Y25	HEX1[2]	PIN_W21	HEX0[2]	PIN_E17
d	HEX3[3]	PIN_AA21	HEX2[3]	PIN_W26	HEX1[3]	PIN_W22	HEX0[3]	PIN_L26
e	HEX3[4]	PIN_AD24	HEX2[4]	PIN_Y26	HEX1[4]	PIN_W25	HEX0[4]	PIN_L25
f	HEX3[5]	PIN_AF23	HEX2[5]	PIN_W27	HEX1[5]	PIN_U23	HEX0[5]	PIN_J22
g	HEX3[6]	PIN_Y19	HEX2[6]	PIN_W28	HEX1[6]	PIN_U24	HEX0[6]	PIN_H22

Figure 3:
Fuctional Block Diagram of one possible Capacitance Measurer Design



Clock Divider/Enabler Waveform Description

(example case when detecting a capacitance of ~0.033µF)



Post Lab Questions

1. Explain the basic operation of the 555 timer when it is placed in multivibrator mode.

2. In terms of accuracy why is it not as important that the 10K resistor have a tight resistance tolerance?

3. How did you modify the parameters to the *count_enabler* module of the mostly structural design? How did you chose the values to use for these parameters that would generate the desired enable rate?

4. In the structural design shown in Figure 3, what is the purpose of the 1-bit D flip-flop? What happens if it is removed?

5. What is the function of a one shot in Figure 3? Why is this important in this design?

6. Describe the thought process for your behavioral design. How did this differ from the mostly structural one?

7. Compare the reported FPGA resource usage of both designs. Which is more efficient in terms of internal logic elements that are utilized? Which was easier to implement? Explain.

This is a one 3-hour laboratory session assignment. The due date is posted as part of the course syllabus on the course Canvas site.