THE UNIVERSITY OF ALABAMA IN HUNTSVILLE
Department of Electrical and Computer Engineering

CPE 322 Digital Hardware Design Fundamentals

Simulation Assignment #2
Simulation of Finite State Machine Designs and Designs that Incorporate Delay Times.

The purpose of this assignment is for students to gain some practical experience using Verilog HDL to simulate Finite State Machines based designs using functional RTL techniques. Students will also gain experience in implementing a gate level simulation that incorporates non-zero user-entered timings. The simulation will be performed using the Mentor Graphics ModelSim® simulation environment.

Reference

In all three parts of this laboratory students are required to use the ModelSim® Simulator in its stand-alone mode. A short guide for this is presented on the CPE 322 Canvas site. It is appropriately entitled "Simulating a Verilog HDL Design using the ModelSim® Compiler and Simulator in Stand-Alone Mode".

Assignment

Part 1: Behavioral Simulation of Mealy FSM using ModelSim®

In this part of the assignment students are to simulate behaviorally the functionality of the STG of the Mealy FSM developed in Part 1 of Homework Assignment 2. They are to demonstrate the correct functionality of the simulation using the same input stimulus sequence that was also developed in Part 1 of Homework Assignment 2. They are to use simple RTL type behavioral simulation (zero delay) and enter their design using ModelSim® in stand-alone mode**.**
In the final report students are to

- Include a copy of their behavioral Verilog Model of their design
- Include the simulation probe and stimulus commands
- Include a screen shot of the waveform *or* listing output that illustrates their results. Students must clearly indicate where they are reading the output relative to the clock in determining the functionality of their design.

Part 2: Behavioral Simulation of Moore FSM using ModelSim®

In this part of the assignment students are to simulate behaviorally the functionality of the STG of the Moore FSM developed in Part 5 of Homework Assignment 2. They are to demonstrate the correct functionality of the simulation using the same input stimulus sequence that was also developed in Part 5 of Homework Assignment 2. They are to use simple RTL type behavioral simulation (zero delay) and enter their design using ModelSim® in stand-alone mode**.**
In the final report students are to

- Include a copy of their behavioral Verilog Model of their design
- Include the simulation probe and stimulus commands
- Include a a screen shot of the waveform or listing output that illustrates their results. Students must indicate where they are reading the output relative to the clock in determining the functionality of their design.

Part 3: Gate-level Timing Simulation of a Sequential Element using ModelSim®

For the gate-level D-latch implementation shown below assume that there is a 1 ns inertial delay on all of the logic gates. Using hazards analysis on the combinational logic portion of the design determine an input stimulus pattern that may generate a pulse due to uneven delay paths between the inputs and the output. Such a pulse could cause the latch's output to oscillate back and forth between logic levels resulting in unstable operation.

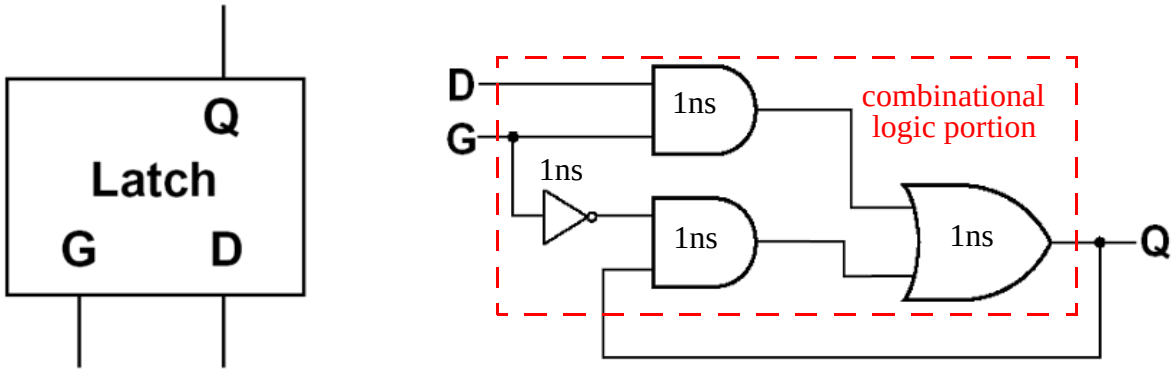

Figure 1: Gate-Level Implementation of a D-Latch with non-zero Delays

If possible verify this phenomena through simulation. Configure your simulation so that the output is at 1 ns and the resolution is 100 ps.
In the final report students are to

- Include a copy of their hazards analysis.
- Include a Structural or Data Flow version of the design that contains the specified delays.
- Include the simulation probe and stimulus commands that caused the phenomena.
- Include a screen shot of a waveform or text listing output that illustrates this result.

After this simulation, modify the original design by adding a single **AND** gate and a bigger **OR** gate. Then re-run the simulation under the same conditions and verify that these oscillations no longer occur.

- Include a picture of the new design.
- Include a new Structural or Data Flow version of the design that contains the specified delays.
- Include the simulation probe and stimulus commands again that originally caused the phenomena in the original design.
- Include a screen shot of a waveform or text listing output that illustrates this result.

Simulation Assignment Turn in Procedure

The due date for this simulation is Thursday February 26, 2015 9:30 AM This is to be an electronic submission -- no hardcopy needs to be turned in to the instructor. You are to upload to the course UAH Canvas dropbox a copy of the simulation assignment on or before its due date. Acceptable file formats include pdf, doc, and docx. This simulation assignment will be graded based on correctness, completeness and clarity of presentation.